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ITU-T G Suppl. 58 (07/2024)

SERIES G: Transmission systems and media, digital systems and networks

Supplements to ITU-T G-series Recommendations

Optical transport network module framer interfaces

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Supplement 58 to ITU-T G-series Recommendations
Optical transport network module framer interfaces

Summary

Supplement 58 to ITU-T G-series Recommendations describes several interoperable component-to-component interfaces (across different vendors) to connect an optical module (with or without digital signal processor) to a framer device in a vendor's equipment supporting 25G, 40G, 50G, 100G or beyond 100G optical transport network (OTN) interfaces.

Only the structure of the 11G, 28G, 56G, or 112G physical lanes of the different OTN module framer interface examples is provided in this Supplement. Electrical parameters for these interfaces can use specifications provided in the relevant clauses of Optical Internetworking Forum common electrical input/output (OIF-CEI) implementation agreement (IA) specifications. For their electrical characteristics, the OIF-CEI IA specifications can be used.

This Supplement relates to Recommendation ITU-T G.709/Y.1331.

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FOIC, framer, interface, module framer interfaces (MFI), module, optical transport lane (OTL), optical transport network (OTN).

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Supplement 58 to ITU-T G-series Recommendations

Optical transport network module framer interfaces

1 Scope

This Supplement describes interfaces between an optical transport network (OTN) framer device and an optical module with or without digital signal processor (DSP) (module framer interfaces (MFIs)). The MFIs described in this Supplement carry optical transport unit k (OTUk; k = 3, 4), optical transport unit 25 or 50 with Reed-Solomon (RS) forward error correction (FEC) (OTU25-RS or OTU50-RS), optical transport unit Cn (OTUCn), or flexible optical transport unit n (FlexO-n(e)) signals. Electrical parameters for these interfaces can use specifications provided in the relevant clauses of the OIF-CEI implementation agreement (IA) [b-OIF-CEI].

2 References

[ITU-T G.695] Recommendation ITU-T G.695 (2018), *Optical interfaces for coarse wavelength division multiplexing applications*.

[ITU-T G.709] Recommendation ITU-T G.709/Y.1331 (2020), *Interfaces for the optical transport network*.

[ITU-T G.709.1] Recommendation ITU-T G.709.1/Y.1331.1 (2024), *Flexible OTN interface common elements*.

[ITU-T G.709.2] Recommendation ITU-T G.709.2/Y.1331.2 (2018), *OTU4 long-reach interface*.

[ITU-T G.709.3] Recommendation ITU-T G.709.3/Y.1331.3 (2024), *Flexible OTN long-reach interfaces*.

[ITU-T G.709.4] Recommendation ITU-T G.709.4/Y.1331.4 (2020), *OTU25 and OTU50 short-reach interfaces*.

[ITU-T G.709.5] Recommendation ITU-T G.709.5/Y.1331.5 (2024), *Flexible OTN short-reach interfaces*.

[ITU-T G.709.6] Recommendation ITU-T G.709.6/Y.1331.6 (2024), *Flexible OTN B400G long-reach interfaces*.

[ITU-T G.959.1] Recommendation ITU-T G.959.1 (2024), *Optical transport network physical layer interfaces*.

3 Definitions

3.1 Terms defined elsewhere

None.

3.2 Terms defined in this Supplement

This Supplement defines the following term:

3.2.1 FOICx.k-MFI: An individual member module framer interface (MFI) interface using k parallel electrical lanes to carry a FlexO-x plus forward error correction (FEC) parity. The order x signifies the interface rate in units of 100G. Note that m FOICx.k-MFI bonded electrical interfaces could be used as a group carrying a FlexO-n information structure (m = [n/x]).

4 Abbreviations and acronyms

This Supplement uses the following abbreviations and acronyms:

AMi	Alignment Marker of index i
AM	Alignment Mechanism field of FlexO frames
AUI	Attachment Unit Interface
BER	Bit Error Ratio
BOH	Basic Overhead area of FlexO frames
B100G	Beyond 100G
B400G	Beyond 400G
CAUI-n	100 Gbit/s chip to chip attachment Unit Interface over n lanes
CEI	Common Electrical Input/output
CWM	Codeword Marker
DSP	Digital Signal Processor
EOH	Extended Overhead area of FlexO frames
FEC	Forward Error Correction
FlexO	Flexible Optical Transport Network
FlexO-n	Flexible optical transport group information structure with n ($n \geq 1$) FlexO instances (i.e., n × 100G bandwidth capacity) carrying one or more $OTUCn_i$ clients and carried over a group of m bonded FlexO-x-<int> interfaces
FlexO-x	FlexO interface information structure of order x (i.e., x × 100G bandwidth capacity), consisting of x ($x \geq 1$) interleaved FlexO instances
FlexO-x-<int>	Information structure consisting of a FlexO-x plus FEC parity and possibly DSP framing. In some instances, <int> name indicates modulation type
FlexO-x-RS	FlexO interface signal of order x with RS10 (544,514) FEC
FlexO-x-RS-m	Group of m bonded short-reach FlexO-x-RS interfaces carrying a FlexO-n
FlexO-ne	Ethernet optimized FlexO group information structure with n ($n \geq 1$) FlexO instances (i.e., n × 100G bandwidth capacity) carrying one or more Ethernet clients and carried over a group of m bonded FlexO-xe-<int> interfaces
FlexO-xe	Ethernet optimized FlexO interface information structure of order x (i.e., x × 100G bandwidth capacity), consisting of x ($x \geq 1$) interleaved FlexO instances
FlexO-xe-<int>	Information structure consisting of a FlexO-xe plus FEC parity and possibly DSP framing. In some instances, <int> name indicates modulation type
FlexO-xe-RS	Ethernet optimized FlexO interface signal of order x with RS10 (544,514) FEC
FlexO-xe-RS-m	Group of m bonded Ethernet optimized FlexO-x-RS interfaces carrying a FlexO-ne
FOI	FlexO interface
FOIC1.k-MFI	100G MFI interface using k parallel electrical lanes carrying a FlexO-1-RS
FOIC2.k-MFI	200G MFI interface using k parallel electrical lanes carrying a FlexO-2-RS
FOIC4.k-MFI	400G MFI interface using k parallel electrical lanes carrying a FlexO-4-RS
FOIC8.k-MFI	800G MFI interface using k parallel electrical lanes carrying a FlexO-8-RS

FOIC1e.k-MFI	100G MFI interface using k parallel physical lanes carrying a FlexO-1e-RS
FOIC4e.k-MFI	400G MFI interface using k parallel physical lanes carrying a FlexO-4e-RS
FOIC1.k-RS	An individual short-reach 100G FlexO-1-RS optical interface using k parallel optical lanes
FOIC2.k-RS	An individual short-reach 200G FlexO-2-RS optical interface using k parallel optical lanes
FOIC4.k-RS	An individual short-reach 400G FlexO-4-RS interface using k parallel optical lanes
FOIC8.k-RS	An individual short-reach 800G FlexO-8-RS interface using k parallel optical lanes
LD	Local Degrade
LLM	Logical Lane Marker
MFI	Module Framer Interface
MUX	Multiplexer
ODSP	Optical line Digital Signal Processor
OH	Overhead
OTL	Optical Transport Lane
OTL4.4-SC	Group of 4 Optical Transport Lanes that carry one OTU4-SC
OTL50.k-RS	Group of k physical Lanes with RS10 (544,514) FEC that carry one OTU50
OTL50u.k-RS	Group of k physical Lanes with RS10 (544,514) FEC that carry one OTU50u
OTLC.4	Group of 4 physical Lanes that carry one OTUC of an OTUCn
OTLk.n	Group of n Optical Transport Lanes that carry one OTUk
OTN	Optical Transport Network
OTU	Optical Transport Unit
OTU25-RS	Optical Transport Unit 25 with CWM and RS10 (544,514) FEC
OTU25u-RS	Optical Transport Unit 25u with CWM and RS10 (528,514) FEC
OTU4-SC	OTU4 with Staircase FEC parity and overhead
OTU50-RS	Optical Transport Unit 50 with AM and RS10 (544,514) FEC
OTU50u-RS	Optical Transport Unit 50u with AM and RS10 (544,514) FEC
OTUCn	Optical Transport Unit Cn
OTUk	Optical Transport Unit k
PAM4	Pulse Amplitude Modulation, Four Level
PMA	Physical Medium Attachment
PMD	Physical Medium Dependent
RS	Reed-Solomon
SC	Staircase
UMx	Unique Marker of index x
UPx	Unique Padding of index x
WDM	Wavelength Division Multiplexing

xGAUI-n x Gbit/s Attachment Unit Interface over n lanes

5 Conventions

Names of information structures and interfaces:

The terms FlexO-n, FlexO-x, FlexO-x-<int>, FlexO-x-<int>-m, and FOICx.k-<int> are used to refer to FlexO information structures and interfaces that are optimized for optical transport network (OTN) bit rates.

The suffix 'e' is added to 'n' or 'x' to indicate the same structure at a bit rate that is optimized for Ethernet clients.

The notation (e) is used as short-hand for "or", e.g., FlexO-x or FlexO-xe.

n: For FlexO interface, the index "n" is used to represent the number of FlexO instances that are in a FlexO group. For OTL (MFI or optical), the index "n" is used to represent the number of lanes on an OTLk.n interface.

x: The index "x" is used to represent the bit rate of the FlexO interface information structure, in 100G increments. For example, x = 1 for 100G, x = 2 for 200G, x = 4 for 400G, etc.

Cx: The index "Cx" is used to represent the bit rate of the FOI (MFI or FlexO) interface with k lane, in 100G increments. For example, Cx = C1 for 100G, Cx = C2 for 200G, Cx = C4 for 400G, etc.

m: The index "m" is used to represent the number of interfaces in a FlexO group.

k: For FOIC interfaces (MFI or optical), the index "k" is used to represent the number of lanes on an FOICx.k-<int> or FOICx.k-MFI interface. For OTL interfaces (MFI or optical) or OTU interfaces, the index "k" is used to represent the capacity (bit rate) of the OTUk or OTLk.n (for example, k = 3 for 40G, k = 4 for 100G).

<int>: The <int> placeholder is used by specific short-reach and long-reach interface Recommendations to provide a unique name to the interface. The interface can be identified by a FEC type or a combination of FEC type and modulation type.

For OTN interfaces, the term "logical lanes" is equivalent to "PCS lanes" for Ethernet BASE-R interfaces. It is used to identify the multiple logical lanes to which an OTUk or FlexO-x(e)-RS signal is distributed to. One or more "logical" lanes can be multiplexed and carried on a physical lane at the MFI or OTSi(G) interface.

Transmission order: The order of transmission of information in all the figures in this Supplement is first from left to right and then from top to bottom. Within each byte, the most significant bit is transmitted first. The most significant bit (bit 1) is illustrated on the left in all figures.

6 Introduction

This Supplement begins with some examples of MFIs for OTU3 and OTU4 signals carried over multiple 11G electrical lanes (using OTL3.4 and OTL4.10 structures, respectively).

Then it describes some examples of MFIs for OTU25-RS, OTU50-RS, OTU4, OTUCn, or FlexO-n signal carried over 28G electrical lanes (using OTU25-RS, OTL50.2-RS, OTL4.4, OTLC.4, FOIC1.4-MFI, FOIC2.8-MFI, or FOIC4.16-MFI structures, respectively), or for OTU25u-RS or OTU50u-RS carried over one or two 26G electrical lanes (using OTU25u-RS or OTL50u.2-RS, respectively). Note that in the case of an OTUCn signal, n OTLC.4 or m FOICx.k-MFI interface structures are used.

Then, it describes some examples MFIs for OTU50-RS, OTU-4, OTUCn or FlexO-n signal carried over 56G electrical lanes (using OTL50.1-RS, OTL4.2, FOIC1.2-MFI, FOIC2.4-MFI, or FOIC4.8-MFI structures, respectively), or for OTU50u-RS carried over one 53G electrical lane (using OTL50u.1-RS).

Finally, it describes some examples of MFIs for OTUCn or FlexO-n signals carried over one or multiple 112G electrical lanes (using FOIC1.1-MFI, FOIC4.4-MFI or FOIC8.8-RS structures, respectively), or for FlexO-ne signals carried over one or multiple 106G electrical lanes (using FOIC1e.1-RS or FOIC4e.4-RS structures, respectively).

Note that a group of m FOICx(e).k-MFI interfaces is used to carry an OTUCn or FlexO-n(e) signal, with m = [n/x].

Users of this Supplement should not assume that possible MFIs are limited to those provided in clauses 7, 8, 9 and 10.

7 Signal formats and rates carried over 11G electrical lanes

This clause describes some MFI structures using 11G physical lanes to carry 40G OTU3 or 100G OTU4 signals. The electrical characteristics of each 11G physical lane may comply with [b-OIF CEI] CEI-11G-xR specifications.

7.1 OTL3.4 structure

The original purpose of the OTL3.4 interface, as specified in clause 8.1 and Annex C of [ITU-T G.709], was to enable the re-use of pluggable modules developed for Ethernet 40GBASE-R applications. Modules developed for [b-IEEE 802.3] 40GBASE-LR4 and 40GBASE-ER4 can have corresponding optical specifications for OTU3 interfaces with application codes C4S1-2D1 and C4L1-2D1, respectively, in [ITU-T G.695]. These modules have a four-lane wavelength division multiplexing (WDM) interface to and from a transmit/receive pair of ITU-T G.652 optical fibres.

These pluggable modules use a four-lane electrical chip-to-module interface, the 40 Gbit/s attachment unit interface, whose specification is found in Annex 83B of [b-IEEE 802.3]. These modules include a simple retimer. This application of the OTL3.4 interface is shown in Figure 7-1.

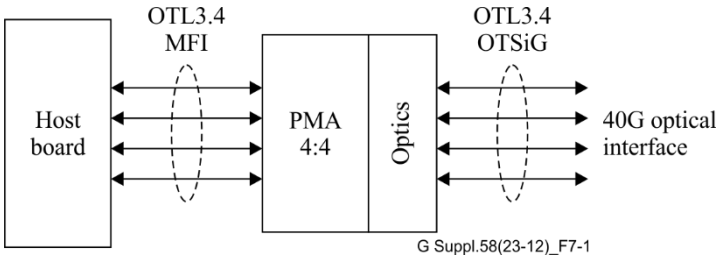


Figure 7-1 – Illustration of the application of an OTL3.4 MFI

Another application example of the OTL3.4 interface is to connect a 40G OTN framer and optical line digital signal processor (ODSP) devices in order to carry an OTU3 signal.

The bit rates of the OTL3.4 lanes are specified in [ITU-T G.709] and listed in Table 7-1.

Table 7-1 – Bit rates of OTL3.4

OTL type	**OTL nominal bit rate** (kbit/s)	**OTL bit-rate tolerance** (ppm)
OTL3.4	4 × 255/236 × 9 953 280	±20
OTL3.4 lane	255/236 × 9 953 280	±20
NOTE – The nominal OTL3.4 lane bit rate is approximately: 10 754 603.390 kbit/s.		

7.2 OTL4.10 structure

The original purpose of the OTL4.10 interface, as defined in clause 8.1 and Annex C of [ITU-T G.709], was to enable the re-use of first-generation pluggable modules developed for Ethernet 100GBASE-R applications. Modules developed for [b-IEEE 802.3] specified 100GBASE-LR4 and 100GBASE-ER4. They have corresponding optical specifications for OTU4 interfaces with the optical parameters as specified for the application codes 4I1-9D1F and 4L1-9C1F, respectively, in [ITU-T G.959.1]. Non-IEEE specified optical interfaces include application code C4S1-9D1F of [ITU-T G.695] and application code 4L1-9D1F of [ITU-T G.959.1]. These modules have a four-lane WDM interface to and from a transmit/receive pair of ITU-T G.652 optical fibres.

These first-generation modules connect to the host board via a ten-lane electrical interface. The conversion between 10 and four lanes is performed using a 100GBASE-R [b-IEEE 802.3] physical medium attachment (PMA) sublayer as specified in clause 83 of [b-IEEE 802.3]. The specification of the 10-lane electrical chip to attachment unit interface (CAUI-10) is found in Annex 83B of [b-IEEE 802.3]. The application of the OTL4.10 interface is illustrated in Figure 7-2.

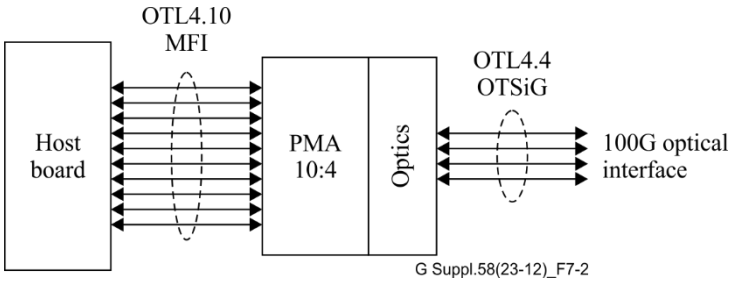


Figure 7-2 – Illustration of the original application of an OTL4.10 MFI

Another application example of the OTL4.10 interface is to connect first generation 100G OTN framers with ODSP devices in order to carry an OTU4 signal.

Each OTL4.10 lane carries two bit-multiplexed 5G logical lanes of an OTU4 as described in Annex C of [ITU-T G.709]. The 5G logical lane format was chosen so that the [b-IEEE 802.3] 10:4 PMA (gearbox) converts the OTU4 signal between a format of 10 lanes of OTL4.10 and four lanes of OTL4.4. Each OTL4.4 lane carries five bit-multiplexed 5G logical lanes of an OTU4 as described in Annex C of [ITU-T G.709].

The bit rates of an OTL4.10 lane are specified in Table 7-2.

Table 7-2 – Bit rates of OTL4.10

OTL type	**OTL nominal bit rate** (kbit/s)	**OTL bit-rate tolerance** (ppm)
OTL4.10	10 × 255/227 × 9 953 280	±20
OTL4.10 lane	255/227 × 9 953 280	±20
NOTE – The nominal OTL4.10 lane bit rate is approximately: 11 180 997.357 kbit/s.		

8 Signal formats and rates carried over 26G or 28G electrical lanes

This clause describes some MFI structures using 28G physical lanes to carry 25G OTU25-RS, 50G OTU50-RS, 100G OTU4, B100G OTUCn or FlexO-n signals, or using 26G physical lanes to carry underclocked 25G OTU25u-RS or 50G OTU50u-RS. The electrical characteristics of each 26G-28G physical lane may comply with [b-OIF CEI] CEI-28G-xR specifications.

8.1 OTL4.4 structure

The original purpose of the OTL4.4 interface, as described in this clause and Annex C of [ITU-T G.709], was to enable the re-use of second (and beyond) generation pluggable modules developed for Ethernet 100GBASE-R applications. Modules developed for [b-IEEE 802.3] specified 100GBASE-LR4 and 100GBASE-ER4. They have corresponding optical specifications for OTU4 interfaces with the optical parameters as specified for the application codes 4I1-9D1F and 4L1-9C1F, respectively, in [ITU-T G.959.1]. Non-IEEE specified optical interfaces include application code C4S1-9D1F of [ITU-T G.695] and application code 4L1-9D1F of [ITU-T G.959.1]. These modules have a four-lane WDM interface to and from a transmit/receive pair of ITU-T G.652 optical fibres.

Most second generation (and beyond) pluggable modules use a four-lane electrical chip-to-module interface (CAUI-4), whose specification is found in Annex 83E of [b-IEEE 802.3]. These modules include a simple retimer (as opposed to the 10:4 gearbox found in first generation modules). This application of the OTL4.4 interface is illustrated in Figure 8-1.

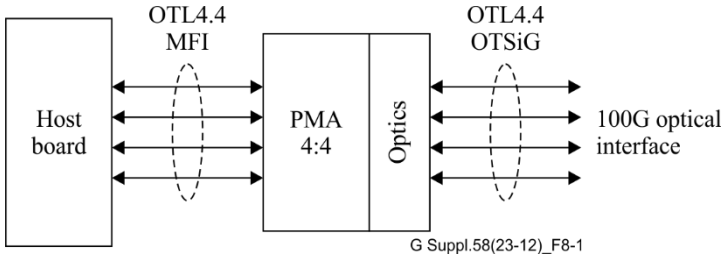


Figure 8-1 – Illustration of the original application of an OTL4.4 MFI

Another application example of the OTL4.4 interface is to connect second generation multi-100G OTN framers with ODSP devices in order to carry independent OTU4 signals and to connect these framers with emerging line side optical modules.

Each OTL4.4 lane carries five bit-multiplexed 5G logical lanes of an OTU4 as described in Annex C of [ITU-T G.709].

The bit rates of the OTL4.4 specified in [ITU-T G.709] are listed in Table 8-1.

Table 8-1 – Bit rates of OTL4.4

OTL type	**OTL nominal bit rate** (kbit/s)	**OTL bit-rate tolerance** (ppm)
OTL4.4	4 × 255/227 × 24 883 200	±20
OTL4.4 lane	255/227 × 24 883 200	±20
NOTE – The nominal OTL4.4 lane bit rate is approximately: 27 952 493.392 kbit/s.		

8.2 OTLC.4 structure

In B100G OTN design, the interfaces between the B100G OTN framer and ODSP devices support OTU4 and OTUCn signals. This interface benefits from a common interface format. The purpose of the OTLC.4 interfaces is to support such a common interface format based on the existing OTL4.4 format. These interfaces carry either four physical lanes of an OTU4 (i.e., OTL4.4) or OTUCn (i.e., OTLC.4). See Figure 8-2.

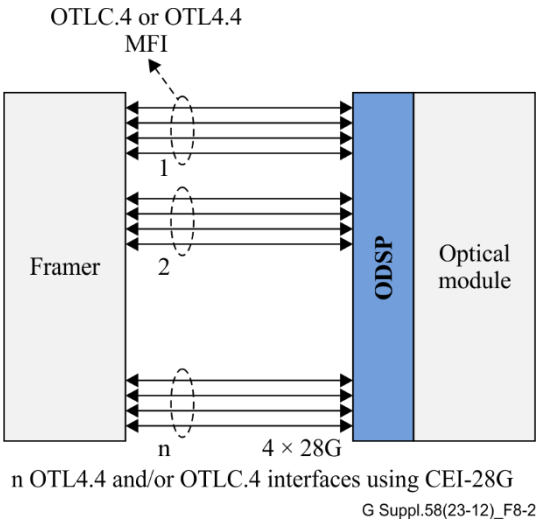


Figure 8-2 – Example applications of an OTL4.4/OTLC.4 MFI

An OTUCn is split into n times OTUC and each OTUC frame is extended with 256 FEC columns at the end of the frame, which contains an RS (255,239) FEC as specified for the OTUk in Annex A of [ITU-T G.709]. Each OTUC frame with RS (255,239) FEC therefore results in an octet-based block frame structure with four rows and 4 080 columns, i.e., the same as an OTUk (k = 1,2,3,4) frame structure. This frame structure is scrambled as specified for the OTUk in clause 11.2 of [ITU-T G.709] and split into twenty 5G logical lanes in accordance with the 5G logical lane specifications for OTL4.4 interface in Annex C of [ITU-T G.709]. The twenty 5G logical lanes of the OTLC are combined into four OTLC.4 physical lanes consistent with the OTL4.4 specifications in Annex C of [ITU-T G.709].

The third OA2 byte in each OTUC with RS (255,239) FEC frame is replaced by a logical lane marker (LLM) byte in accordance with the OTL4.4 specifications in Annex C of [ITU-T G.709] to support the reordering of the 5G logical lanes within the scope of the twenty 5G logical lanes in a 100G OTUC group.

OTL4.4 physical lanes do not support an OTU4 Identifier. Due to this, groups of four OTLx.4 (x = 4, C) physical lanes carrying one OTU4 or one OTUC instance must be connected as a 100G group. Physical lanes within such a 100G group can be interchanged, but the interchanging and reordering of physical lanes of different 100G groups is not defined and as such not supported.

The bit rates of an OTLC.4 lane with RS (255,239) FEC are specified in Table 8-2.

Table 8-2 – Bit rate of OTLCn with RS (255,239) FEC

OTL type	**OTL nominal bit rate** (kbit/s)	**OTL bit-rate tolerance** (ppm)
OTLCn	n × 4 × 255/226 × 24 883 200	±20
OTLC slice	4 × 255/226 × 24 883 200	±20
OTLC.4 lane	255/226 × 24 883 200	±20
NOTE – The nominal OTLCn, OTLC slice and OTLC.4 lane bit rates are approximately and respectively: n × 112 304 707.965 kbit/s, 112 304 707.965 kbit/s and 28.076 176.991 kbit/s.		

8.3 FOIC1.4-MFI structure

The original purpose of a group of n FOIC1.4-RS interfaces (i.e., FlexO-1-RS-n group), as specified in clauses 7 and 11 of [ITU-T G.709.5], is to provide an interoperable modular short-reach OTN interface for B100G OTUCn or FlexO-n (n ≥ 1) transport signals, by bonding n 100G standard-rate interfaces.

As shown in Figures 7-1 and 10-1 or 10-9 of [ITU-T G.709.1], one or more OTUCn_i signals ($n_i \geq 1$ and $\sum n_i = n$) can be mapped over a FlexO-n signal structure composed of n 100G FlexO instances (each carrying an OTUC instance). The FlexO-n signal can be distributed into n FlexO-1 frame structures that will be further adapted and carried over n FlexO-1-<int> bonded interfaces. For short reach optical interfaces and per Figure 7-1 of [ITU-T G.709.5], each individual FlexO-1-RS interface signal (i.e., <int> = RS) is distributed on four lanes (FOIC1.4-RS) and operates at almost the same interface rate as OTL4.4 (with just −4.46 ppm offset between the two nominal rates).

So, second (and beyond) generation pluggable modules developed for Ethernet 100GBASE-R applications and supporting the OTU4 rate and OTL4.4 interface could be seamlessly reused for FlexO-1-RS transport and FOIC1.4-RS interface. Modules developed for [b-IEEE 802.3] specified 100GBASE-LR4 and 100GBASE-ER4. They have corresponding optical specifications for OTU4 (and so for FlexO-1-RS) interfaces with the optical parameters as specified for the application codes 4I1-9D1F and 4L1-9C1F, respectively, in [ITU-T G.959.1]. Non-IEEE specified optical interfaces include application code C4S1-9D1F of [ITU-T G.695] and application code 4L1-9D1F of [ITU-T G.959.1]. These modules have a four-lane WDM interface to and from a transmit/receive pair of ITU-T G.652 optical fibres.

Most of these pluggable modules use a four-lane electrical chip-to-module interface (CAUI-4), whose specification is found in Annex 83E of [b-IEEE 802.3] and includes a simple retimer. For FlexO-1-RS short reach transport application reusing such modules, the FOIC1.4-RS lane structure is also used for FOIC1.4-MFI four-lane electrical chip-to-module interface.

This application of n FOIC1.4-RS bonded interfaces (short-reach FlexO-1-RS-n group) using FOIC1.4-MFI chip-to-module interfaces is shown in Figure 8-3a.

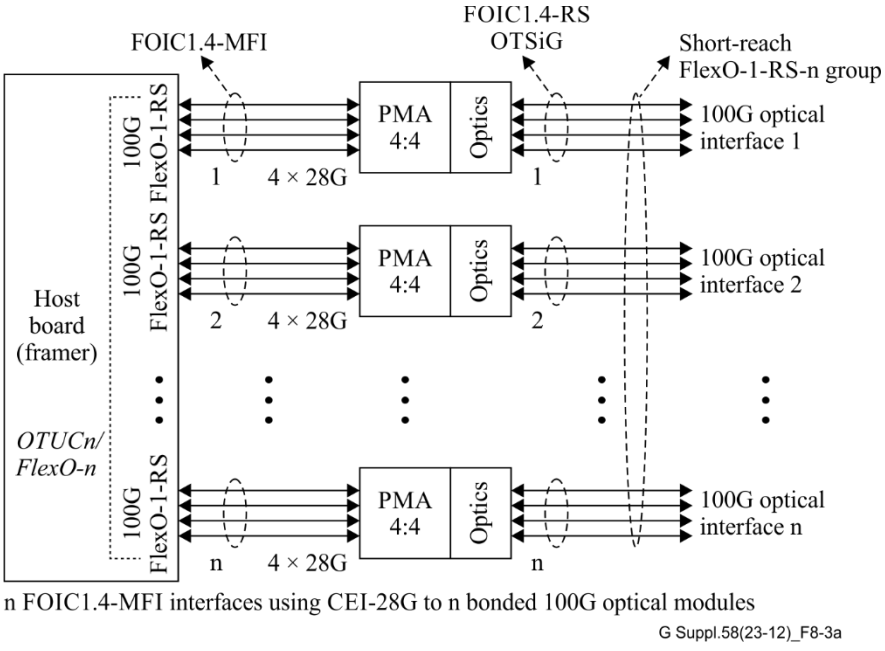


Figure 8-3a – Original application of a FOIC1.4-MFI interface

NOTE – The FOIC1.4-MFI interface could also be used similarly to an OTLC.4 interface to connect a beyond 100G OTN framer with one or more ODSP devices supporting FlexO interfaces on the host side. One possible advantage for implementers is that the FOIC1.4-MFI lane operates at the same rate as an OTL4.4 lane, so slightly slower than an OTLC.4 lane and with a stronger RS10 FEC. Another advantage is that the bit rate of a FOIC1.4-MFI lane is exactly half the bit rate of a FOIC1.2-MFI lane (the FOIC1.2-MFI lane is obtained by simple bit-interleaving of two FOIC1.4-MFI lanes). Depending on the application, implementers could make use of the FlexO overhead (OH). Although some OH may become optional, it is generated at the source and may be ignored at the sink (see clause 9.1 for the handling of FlexO overhead for this type of application). This alternate application is illustrated in Figure 8-3b.

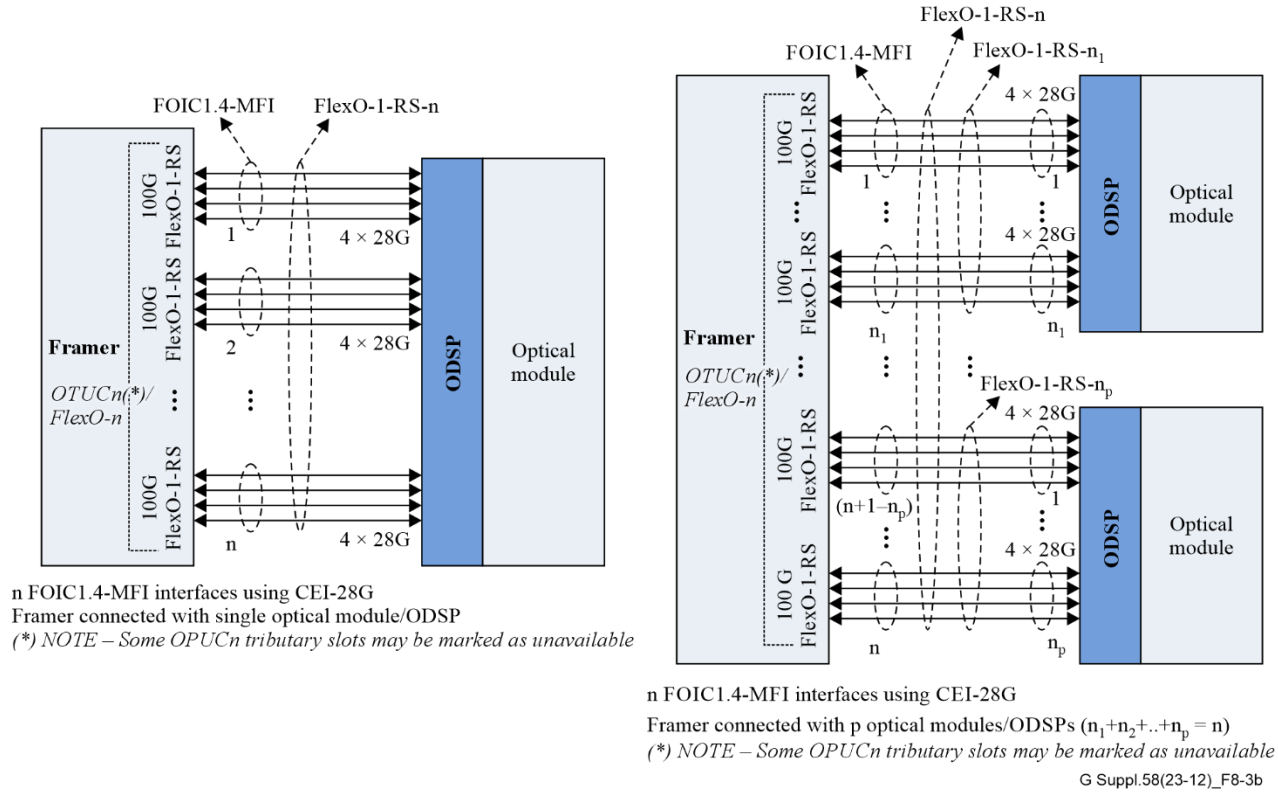


Figure 8-3b – Alternate application of a FOIC1.4-MFI interface

The bit rates of the FOIC1.4-MFI are the same as specified in [ITU-T G.709.5] for FOIC1.4-RS and listed in Table 8-3.

Table 8-3 – Bit rates of FlexO-1-RS-n and FOIC1.4-MFI

Flexible optical transport network interface (FOI) type	**FOI nominal bit rate** (kbit/s)	**FOI bit-rate tolerance** (ppm)
FlexO-1-RS-n	n × 4 × 256/241 × 239/226 × 24 883 200	±20
FOIC1.4-MFI	4 × 256/241 × 239/226 × 24 883 200	±20
FOIC1.4-MFI lane	256/241 × 239/226 × 24 883 200	±20
NOTE – The nominal FOIC1.4-MFI lane bit rate is approximately: 27 952 368.611 kbit/s.		

8.4 FOIC2.8-MFI and FOIC4.16-MFI structures

As shown in Figures 7-1 and 10-1 or 10-9 of [ITU-T G.709.1], one or more OTUCn$_i$ signal ($n_i \geq 1$ and $\sum n_i = n$), full-rate or sub-rated (with some OPUCn$_i$ Tributary Slots marked as unavailable), are mapped over a FlexO-n signal structure composed of n 100G FlexO instances, each carrying an OTUC instance. The FlexO-n structure can be distributed into m FlexO-2 or m FlexO-4 frame

structures further adapted and carried over m FlexO-2-<int> or m FlexO-4-<int> bonded optical interfaces.

For short-reach FlexO-x-RS-m interface group applications (i.e., <int>=RS) with x = 2 or 4, each FlexO-2-RS interface signal (carrying up to two OTUC) is distributed and transported over k physical lanes FOIC2.k-RS interface and each FlexO-4-RS interface signal (carrying up to four OTUC) is distributed and transported over k physical lanes FOIC4.k-RS interface, per Figure 7-1 of [ITU-T G.709.5]. This provides interoperable modular OTN interfaces with short-reach FEC (reusing the same RS10 (544,514) FEC schemes as 200GBASE-R or 400GBASE-R) for B100G OTUCn and FlexO-n ($n \geq 1$) transport signals, by bonding m 200G or m 400G standard-rate optical interfaces or optical lane groups.

The FOIC2.8-RS or FOIC4.16-RS signal structure (k= 8 or 16) could be used for FOIC2.8-MFI or FOIC4.16-MFI interface to connect a beyond 100G OTN framer with one or more 200G or 400G pluggable modules or ODSP devices supporting 28G electrical lanes and FlexO interfaces on the host side. One possible advantage for implementers is that the FEC and lane processing for FOIC2.8-MFI or FOIC4.16-MFI interface is almost identical to 200GAUI-4 or 400GAUI-8, respectively, thus allowing implementers to share digital logic supporting both Ethernet and OTN signals on its host side.

First generation pluggable modules developed for Ethernet 200GBASE-R with eight electrical lanes on the host side and supporting 200G FlexO rate and FOIC2.8-MFI host interface (roughly the same 28G lane bit rate as OTL4.4 with a similar digital format as 200GAUI-8) could also be reused for FlexO-2-RS transport. They have corresponding optical specifications with parameters as specified for the pulse amplitude modulation, four level (PAM4) application codes 4I1-4D1F in [ITU-T G.959.1] and C4S1-4D1F in [ITU-T G.695]. These modules have a four-lane WDM interface to and from a transmit/receive pair of ITU-T G.652 optical fibres.

Similarly, first generation pluggable modules developed for Ethernet 400GBASE-R with 16 electrical lanes on the host side and supporting a 400G FlexO rate and FOIC4.16-MFI host interface (i.e., roughly the same lane bit rate as OTL4.4 with similar digital format as 400GAUI-16) could be reused for FlexO-4-RS transport. They have corresponding optical specifications with optical parameters as specified for the PAM4 application codes 8R1-4D1F or 8I1-4D1F in [ITU-T G.959.1]. These modules have an eight-lane WDM interface to and from a transmit/receive pair of ITU-T G.652 optical fibres.

These applications of m FOIC2.8-MFI bonded interfaces (for short-reach FlexO-2-RS-m group transport) and m FOIC4.16-MFI bonded interfaces (for short-reach FlexO-4-RS-m group transport) are illustrated in Figure 8-4.

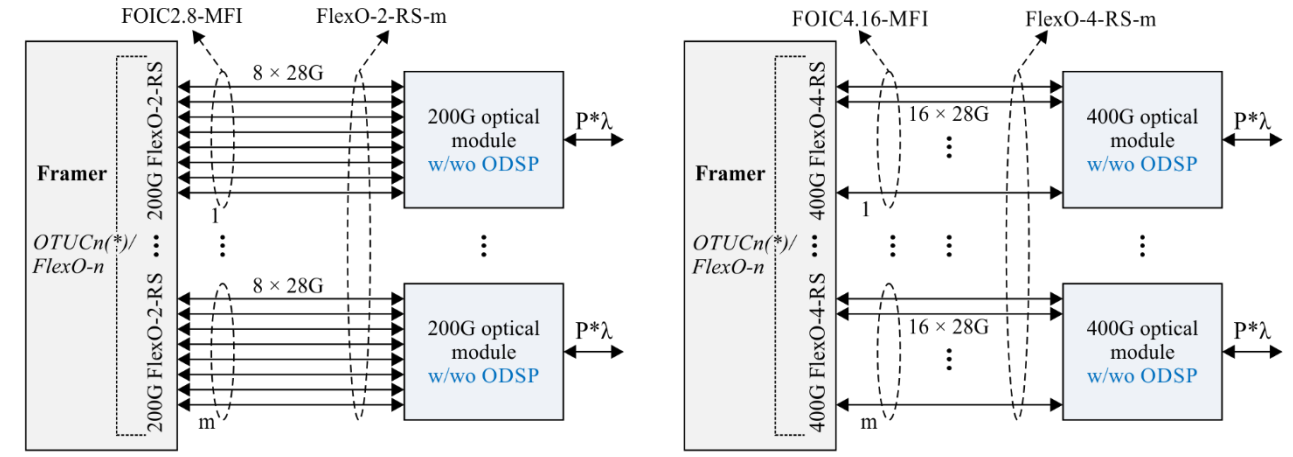


Figure 8-4 – Application of FOIC2.8-MFI and FOIC4.16-MFI interfaces

NOTE – The RS10 (544,514) FEC computing and 200G/400G FlexO-x-RS lane distribution are summarized in clause 9.2 and fully specified in clauses 12 and 13 of [ITU-T G.709.5]. Each electrical lane of a FOIC2.8-MFI or FOIC4.16-MFI corresponds to a 28G logical lane. This FEC scheme and lane architecture follows the same processes as specified in clause 119 of [b-IEEE 802.3] for 200GBASE-R (200GAUI-8) and 400GBASE-R (400GAUI-16) interfaces, respectively. Depending on the application, the RS10 FEC could be used as line FEC, concatenated with another FEC or terminated in an ODSP device. When the RS10 FEC is used as line FEC or concatenated, the 28G lanes on the host interface could be bit multiplexed towards optical lanes. Also, in some applications, implementers could make use of or terminate the FlexO OH in an ODSP device. Although some OH may become optional, it is generated at the source and may be ignored at the sink (see clauses 9.1 and 9.2 for the handling of FlexO OH for this type of application).

The bit rates of the FOIC2.8-MFI and FOIC4.16-MFI are indicated in Tables 8-4a and 8-4b.

Table 8-4a – Bit rates of FlexO-2-RS-m group and FOIC2.8-MFI

FOI type	**FOI nominal bit rate** (kbit/s)	**FOI bit-rate tolerance** (ppm)
FlexO-2-RS-m	m × 8 × 256/241 × 239/226 × 24 883 200	±20
FOIC2.8-MFI	8 × 256/241 × 239/226 × 24 883 200	±20
FOIC2.8-MFI lane	256/241 × 239/226 × 24 883 200	±20
NOTE – The nominal FOIC2.8-MFI lane bit rate is approximately: 27 952 368.611 kbit/s.		

Table 8-4b – Bit rates of FlexO-4-RS-m group and FOIC4.16-MFI

FOI type	**FOI nominal bit rate**	**FOI bit-rate tolerance**
FlexO-4-RS-m	m × 16 × 256/241 × 239/226 × 24 883 200	±20
FOIC4.16-MFI	16 × 256/241 × 239/226 × 24 883 200	±20
FOIC4.16-MFI lane	256/241 × 239/226 × 24 883 200	±20
NOTE – The nominal FOIC4.16-MFI lane bit rate is approximately: 27 952 368.611 kbit/s.		

8.5 OTL4.4-SC structure

As specified in clause 11 of [ITU-T G.709.2], an OTU4-SC (OTU4 with staircase (SC) FEC parity and overhead) signal can be adapted and carried over an OTL4.4-SC interface. The OTU4-SC frame and FEC scheme are specified in clause 8 of [ITU-T G.709.2]. The frame format, OH structure and FEC redundancy of OTU4-SC and OTU4 are identical. Therefore, OTU4-SC is like an OTU4 signal using a strong SC-FEC code, instead of the RS8 (255,239) code of [ITU-T G.709].

The OTL4.4-SC interface could be used to connect a 100G OTU4 framer implementing the hard-decision SC FEC with an ODSP device not supporting that FEC. This implementation enables the interoperable OTU4-SC metro/long reach interface in accordance with [ITU-T G.709.2], in which case the module has optical specifications with the parameters and optical modulation described in [b-ITU-T G.698.2].

This application example of the OTL4.4-SC interface is illustrated in Figure 8-5.

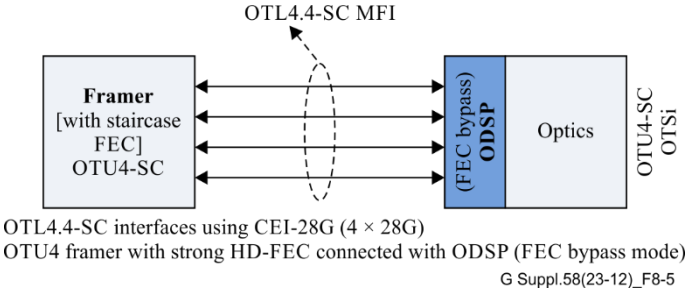


Figure 8-5 – Example application of OTL4.4-SC MFI

Each OTL4.4-SC lane carries five bit-multiplexed 5G logical lanes of an OTU4-SC as described in clause 11 of [ITU-T G.709.2] and Annex C of [ITU-T G.709].

The bit rates of the OTL4.4-SC specified in [ITU-T G.709.2] are listed in Table 8-5.

Table 8-5 – Bit rates of OTL4.4-SC

OTL type	**OTL nominal bit rate** (kbit/s)	**OTL bit-rate tolerance** (ppm)
OTL4.4-SC	4 × 255/227 × 24 883 200	±20
OTL4.4-SC lane	255/227 × 24 883 200	±20
NOTE – The nominal OTL4.4-SC lane bit rate is approximately: 27 952 493.392 kbit/s.		

8.6 OTL50.2-RS and OTL50u.2-RS structures

As described in clause 9.6 of [ITU-T G.709.4], an OTU50-RS signal can be distributed (in groups of 10 bits) over two OTL50.2-RS lanes. The same scheme is used for OTU50u-RS signal distribution over two OTL50u.2-RS lanes.

NOTE – The RS (544, 514, 10) FEC scheme and lane distribution for OTU50-RS and OTU50u-RS signals in accordance with [ITU-T G.709.4] are the same as those specified in clause 134 of [b-IEEE 802.3] for a 50GBASE-R interface.

The OTL50.2-RS or OTL50.2u-RS interface could be used as a two-lane MFI in order to connect a 50G OTN framer with a 50G pluggable module supporting 25G electrical lanes on the host side and a 2:1 multiplexer (MUX).

Within the module, the 50G OTL50(u).1-RS transport lane is formed by simple bit-multiplexing of the two 25G OTL50(u).2-RS lanes from the host side. It provides an interoperable optical interface format for OTU50-RS or OTU50u-RS short-reach interfaces.

The receive module bit-demultiplexes the 50G OTL50(u).1-RS transport lane recovered from the optical interface, into two 25G OTL50(u).2-RS electrical lanes on its host side towards the framer. The framer sink identifies each of the two 25G OTL50(u).2-RS lanes according to its AM specific pattern (unique UMx values). It must accept the two lanes in any position, and after alignment and deskew, interleave these two 25G logical lanes (in groups of 10 bits) into an OTU50(u)-RS frame.

In accordance with Table 8-6b, the OTL50u.2-RS interface operates within the 50GAUI-2 interface bit rate range and with similar FEC and lane format. There is just +15.6 ppm offset between the two nominal rates. So, first generation pluggable modules developed for Ethernet 50GBASE-R applications with a 2:1 MUX and 50GAUI-2 interface on the host side could be reused for underclocked 50G OTN transport (i.e., OTU50u-RS) with an OTL50u.2-RS MFI between the framer and the optical module.

If such a module also supports full-rate 50G OTN signals with OTL50.2-RS MFI on its host side (i.e., 2× 28G electrical lanes with almost the same bit rate as a FOIC1.4 lane and similar FEC and lane format as 50GAUI-2), it could also be reused for OTU50-RS full-rate transport.

Modules developed for [b-IEEE 802.3] are specified 50GBASE-LR and 50GBASE-ER with a PAM4 optical physical medium dependent (PMD) sublayer, and may be used for OTU50(u)-RS interfaces when conforming to the optical specifications and parameters to be determined by application codes for metro networks. Some of these 50G modules may have a single WDM interface to and from a transmit/receive pair of ITU-T G.652 optical fibres.

These applications of OTL50.2-RS and OTL50u.2-RS interfaces (considering metro network transport of OTU50-RS and OTU50u-RS) are illustrated in Figure 8-6.

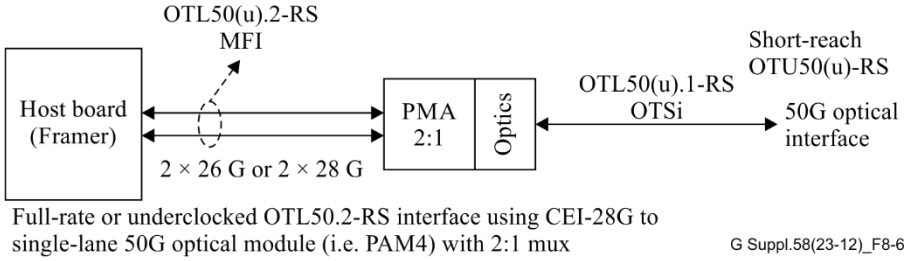


Figure 8-6 – Example application of OTL50.2-RS and OTL50u.2-RS interfaces

The bit rates of these full-rate (i.e., OTL50.2-RS) and underclocked (i.e., OTL50u.2-RS) interfaces and lanes are listed in Tables 8-6a and 8-6b, in accordance with [ITU-T G.709.4] specifications.

Table 8-6a – Bit rates of OTL50.2-RS

OTL type	**OTL nominal bit rate** (kbit/s)	**OTL bit-rate tolerance** (ppm)
	a	
OTL50.2-RS	2 × 255/227 × 24 833 200	±20
OTL50.2-RS lane	255/227 × 24 883 200	±20
NOTE – The nominal OTL50.2-RS lane bit rate is approximately: 27 952 493.392 kbit/s.		

Table 8-6b – Bit rates of OTL50u.2-RS

OTL type	OTL nominal bit rate	OTL bit-rate tolerance
OTL50u.2-RS	2 × 680/637 × 24 833 200	±20
OTL50u.2-RS lane	680/637 × 24 833 200	±20
NOTE – The nominal OTL50u.2-RS lane bit rate is approximately: 26 562 913.658 kbit/s.		

8.7 OTU25-RS and OTU25u-RS structures

Clause 8.6 and Annex B of [ITU-T G.709.4] specify the interface formats of OTU25-RS and OTU25u-RS signals as single lane OTU25-RS and single lane OTU25u-RS, respectively.

NOTE – The RS (528, 514, 10) FEC scheme for OTU25u-RS in accordance with Annexes B and C of [ITU-T G.709.4], is the same as that specified in clause 108 of [IEEE 802.3] for a 25GBASE-R interface. The RS (544, 514, 10) FEC scheme for OTU25-RS in accordance with Annex A of [ITU-T G.709.4], is similar to the 50GBASE-R FEC.

The OTU25-RS or OTU25u-RS interface could be used as a single lane MFI to connect a 25G OTN framer with a 25G pluggable module.

These modules include a simple retimer and provide an interoperable optical interface format for OTU25-RS or OTU25u-RS short-reach interfaces.

In accordance with Table 8-7b, the OTU25u-RS interface operates within the 25GAUI interface bit rate range and with similar FEC and lane format. There is just +15.6 ppm offset between the two nominal rates. So, pluggable modules developed for Ethernet 25GBASE-R applications could be reused for underclocked 25G OTN transport (i.e., OTU25u-RS) with an OTU25u-RS MFI between the framer and the optical module.

If such a module also supports full-rate the 25G OTN interface and OTU25-RS MFI on its host side (i.e., 28G electrical lane with same bit rate as OTL4.4 lane), it could also be reused for OTU25-RS full-rate transport.

Modules developed for [b-IEEE 802.3] are specified 25GBASE-LR and 25GBASE-ER, and may be used for OTU25(u)-RS optical interfaces, when conforming to the optical specifications and parameters to be determined by application codes for metro networks. Some of these 25G modules may have a single WDM interface to and from a transmit/receive pair of ITU-T G.652 optical fibres.

These applications of OTU25-RS and OTU25u-RS interfaces (considering metro network transport of OTU25-RS and OTU25u-RS) are illustrated in Figure 8-7.

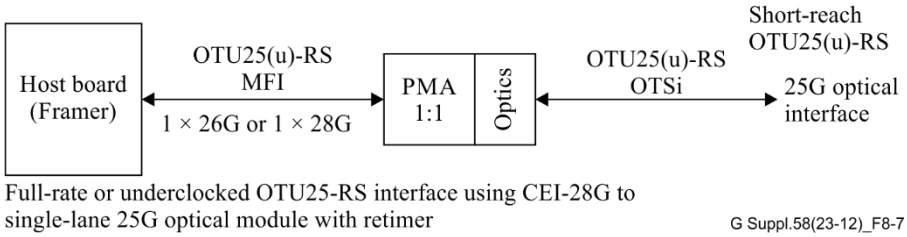


Figure 8-7 – Example application of single lane OTU25-RS and OTU25u-RS interfaces

The bit rates of these full-rate (i.e., OTU25-RS) and underclocked (i.e., OTU25u-RS) interfaces and lanes are indicated in Tables 8-7a and 8-7b, in accordance with [ITU-T G.709.4] specifications.

Table 8-7a – Bit rate of single-lane OTU25-RS

Lane type	**Lane nominal bit rate** (kbit/s)	**Lane bit-rate tolerance** (ppm)
OTU25-RS lane	255/227 × 24 883 200	±20
NOTE – The nominal OTU25-RS lane bit rate is approximately: 27 952 493.392 kbit/s.		

Table 8-7b – Bit rate of single-lane OTU25u-RS

Lane type	**Lane nominal bit rate**	**OTL bit-rate tolerance**
OTU25u-RS lane	660/637 × 24 833 200	±20
NOTE – The nominal OTU25u-RS lane bit rate is approximately: 25 781 651.491 kbit/s.		

9 Signal formats and rates carried over 53G or 56G electrical lanes

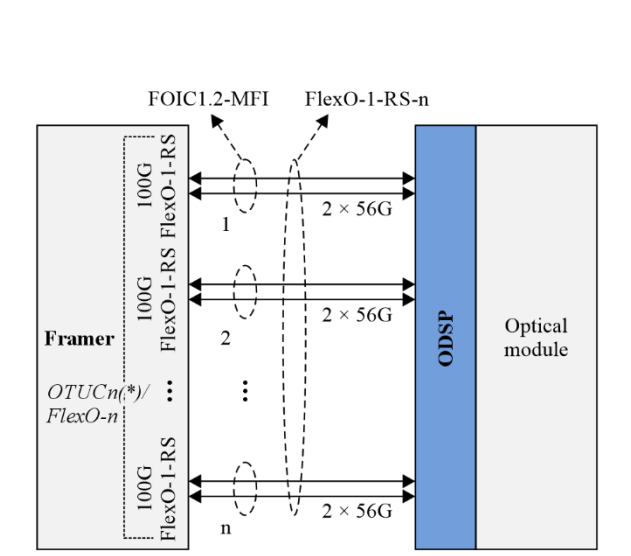
This clause describes some MFI structures using 56G physical lanes to carry 50G OTU50-RS or B100G OTUCn or FlexO-n ($n \geq 1$) signals, or using 53G single physical lane to carry underclocked 50G OTU50u-RS. The electrical characteristics of each 56G physical lane may comply with [b-OIF CEI] CEI-56G-xR-PAM4 specifications.

9.1 FOIC1.2-MFI structure

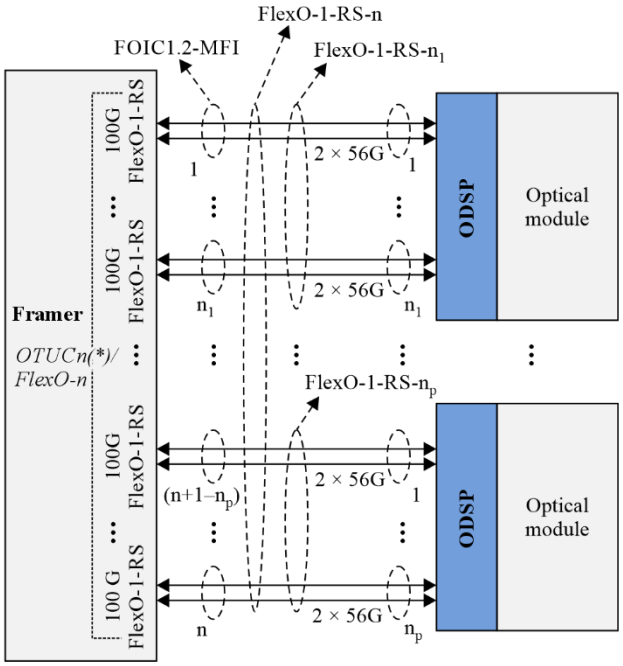
As shown in Figures 7-1 and 10-1 or 10-9 of [ITU-T G.709.1], one or more $OTUCn_i$ signal ($n_i \geq 1$ and $\sum n_i = n$), full-rate or sub-rated (with some $OPUCn_i$ tributary slots marked as unavailable) can be mapped over a FlexO-n signal structure composed of n 100G FlexO instances (each carrying an OTUC instance). The FlexO-n structure can be distributed into n FlexO-1 frame structures (each corresponding to a FlexO instance) further adapted and carried over n FlexO-1-<int> bonded interfaces.

For short-reach FlexO-1-RS-n interface group applications (i.e., <int>= RS), with x = 1 and k = 2, each FlexO-1-RS interface signal can be adapted and carried over two 56G physical lanes of a FOIC1.2-RS interface per Figure 7-1 of [ITU-T G.709.5].

The FOIC1.2-RS lane structure can also be used for FOIC1.2-MFI interface to connect beyond 100G OTN framers with ODSP devices over 56G electrical lanes. This first application example of connecting B100G framers with line side optical modules is illustrated in Figure 9-1, showing an OTUCn (or FlexO-n) carried over n FOIC1.2-MFIs.



n FOIC1.2-MFI interfaces using CEI-56G
Framer connected with single optical module/ODSP
(*) *NOTE – Some OPUCn tributary slots may be marked as unavailable*



n FOIC1.2-MFI interfaces using CEI-56G
Framer connected with p optical modules/ODSPs ($n_1+n_2+...+n_p = n$)
(*) *NOTE – Some OPUCn tributary slots may be marked as unavailable*

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Figure 9-1a – First example applications of an FOIC1.2-MFI interface

Per the mapping specifications in clause 10.1 or 10.3 of [ITU-T G.709.1], the OTUCn is split into n times OTUC, and each OTUC is mapped into an individual 100G FlexO instance of a FlexO-n structure. Each 100G FlexO instance corresponds to a FlexO-1 frame and consists of frame alignment mechanism field (AM), extended overhead field (EOH), basic overhead field (BOH), and payload area in which the OTUC is transported (see clause 8 of [ITU-T G.709.1]).

After FEC parity area addition to the FlexO-1 frame, synchronous scrambling, alignment markers (AMi) insertion and FEC [RS10(544,514)] parity computation (see clauses 11.3 and 11.4 of [ITU-T G.709.5]), each individual FlexO-1-RS frame is distributed (in groups of 10 bits) on four 28G logical lanes as described for FOIC1.4-RS in clause 11.5.1 of [ITU-T G.709.5].

Each 56G lane of a FOIC1.2-RS is formed by simple bit-multiplexing of two 28G logical lanes from the same FlexO-1-RS, and then carried over an FOIC1.2-MFI electrical lane. At the sink, the bits from each individual 56G FOIC1.2-MFI lane are deinterleaved into two 28G logical lanes.

When the RS FEC is terminated, the sink identifies each of the four 28G logical lanes within a two-lane FOIC1.2-MFI interface according to its AMi specific pattern (unique UMx and UPx values as specified in clauses 9.1 and 11.5.1 of [ITU-T G.709.5]). The sink must support the four 28G logical lanes in any position, and in addition to 28G logical lane alignment and deskew, proceed to reorder these four 28G logical lanes prior to reassembly into a FlexO-1-RS frame. After FEC termination and descrambling of the FlexO-1-RS frame, if FlexO-1 is partially or fully terminated the FlexO OH may be processed, and the OTUC may be demapped. At the framer sink, the receive line pre-FEC LD status bit is extracted from the FlexO OH area and the n OTUC that are demapped from the n FOIC1.2 interfaces are deskewed to retrieve the original OTUCn signal. At the ODSP sink, n_i OTUC demapped from n_i FOIC1.2 interfaces could be aligned, deskewed, crunched (removing unavailable tributary slots), and assembled as the OTUCn_i digital signal to be transmitted.

Groups of two FOIC1.2-MFI physical lanes carrying one FlexO-1-RS frame (so one OTUC instance) must be connected as a 100G group. Physical lanes within such a 100G group can be interchanged, but the interchanging and reordering of physical lanes of different 100G groups is not defined and as such not supported.

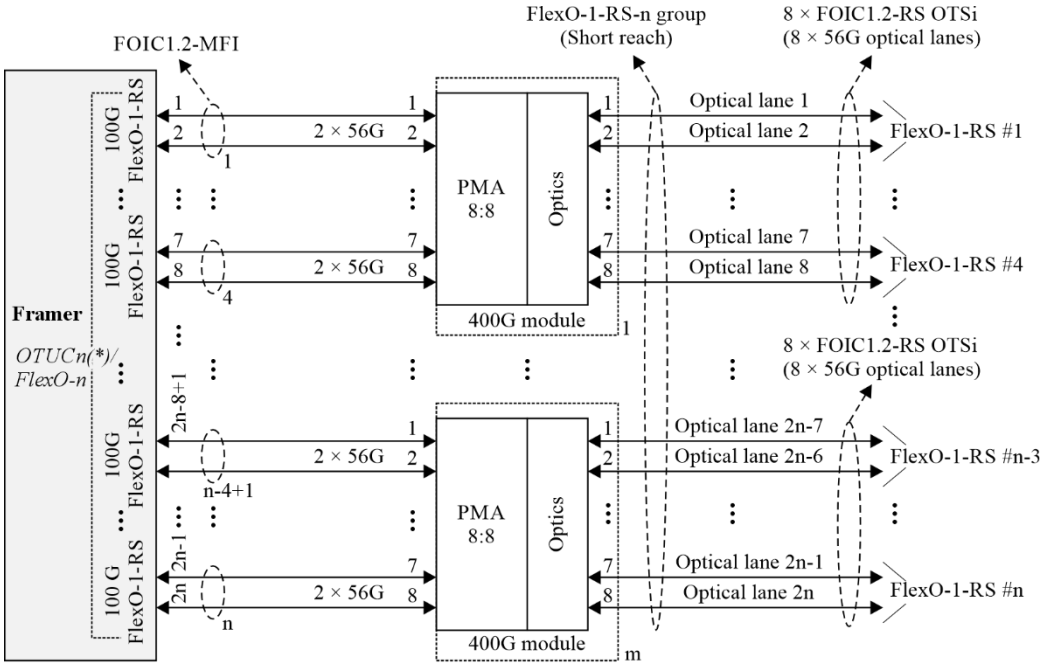
Two possible cases are considered for the application examples illustrated in Figure 9-1a:

– In the first case, each FlexO-1 frame is terminated at both ends of the MFI. Thus, some FlexO OH area becomes optional and, although it is generated at the source, it may be ignored at the sink. The FlexO multi-frame alignment signal is generated at the source and fully interpreted at the sink in accordance with clause 9.2.1 of [ITU-T G.709.1]. The use of the OTN synchronization messaging channel and FlexO communications channel OH across the MFI is for further study. Additionally, the receive line pre-FEC detected local degrade (LD) status bit is optionally carried in bit 8 of the STAT field of the BOH per Figure 9-2d. Note that the receive line pre-FEC LD could also be forwarded through the MFI in bit 8 of the RSTAT EOH field. The receive ODSP detects the receive line pre-FEC LD and forwards the LD status bit to the receive framer device through the MFI.

– In the second case, the FlexO is terminated at the framer and either fully or partially passed through at the ODSP. Depending on the type of module, in the ODSP the 28G logical lanes and RS FEC may be terminated or carried transparently, the FlexO extended OH may be terminated or carried transparently, the FlexO basic OH may be terminated or carried transparently, and the n_i OTUC demapped and aligned or not. This would correspond to different levels of transparency and processing within the module, for segmented vs. concatenated or transparent FEC, FlexO-x regenerator, or FlexO-n multiplexing applications. Note that when FlexO extended overhead is not carried transparently, the receive line pre-FEC LD could be processed as specified in clause 9.3.3.2.2 of [ITU-T G.709.1] and forwarded through the MFI in bit 8 of FlexO EOH RSTAT field.

The FOIC1.2-RS signal structure could alternately be used for FOIC1.2-MFI interface to connect a beyond 100G OTN framer with short reach pluggable modules supporting 56G electrical lanes and FlexO bit rate on their host side. For example, eight-lane pluggable modules developed for Ethernet 400GBASE-R applications and supporting FlexO bit rate could be reused for short reach optical transport applications of multiple FlexO-1-RS signals. They have corresponding optical specifications for 56G FOIC1.2-RS per lane with the optical parameters as specified for the PAM4 application codes 8R1-4D1F or 8I1-4D1F of [ITU-T G.959.1]. They have an eight-lane WDM interface to and from a transmit/receive pair of ITU-T G.652 optical fibres. Most of these pluggable modules use an eight-lane electrical chip-to-module interface (400GAUI-8) per Annex 120E of [b-IEEE 802.3]. Four FOIC1.2-MFI interfaces, each carrying a FlexO-1-RS signal using FOIC1.2-RS two-lane format, could be used to connect the host side of such pluggable optical module using 56G electrical lanes with a multi-100G OTN framer or the host side of a B100G ODSP device.

In the application example of Figure 9-1b, [m × 4] FOIC1.2-MFIs connect m 400G pluggable modules with a multi-100G OTN framer. In such application, the OTUCn signal ($n \geq 1$, $n \leq m \times 4$) is carried over n FOIC1.2-RS bonded short reach optical lanes (FlexO-1-RS-n group). Each set of two FOIC1.2-RS lanes carries a FlexO-1-RS frame (carrying a single OTUC instance). This provides interoperable modular short-reach OTN interfaces for B100G OTUCn ($n \geq 1$) transport signals, by bonding [n × 2] 56G standard optical lanes.



Framer with n FOIC1.2-MFI interfaces connected through CEI-56G electrical lanes with m 400G pluggable modules with eight 56G optical lane each ($n \leq m \times 4$)

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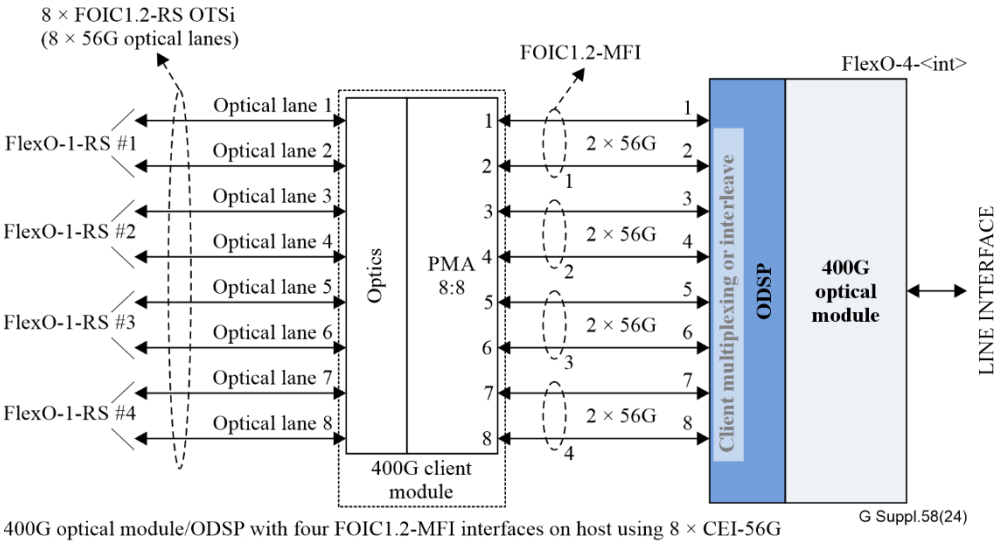
Figure 9-1b – Second example application of an FOIC1.2-MFI interface

In Figure 9-1c application example, four FOIC1.2-MFIs could be used to connect four FlexO-1-RS client signals between the host side of an eight-lane 400G pluggable module and the host side of a 400G ODSP device or line side optical module. Each FlexO-1-RS signal is carried over two FOIC1.2-RS optical lanes of the 400G pluggable module. On its host side, the ODSP could integrate four 100G OTN clients multiplexing (the clients could be plesiochronous) or simple interleaving functions (if the clients are source-synchronous) towards the FlexO-4-<int> line interface for single-chip muxponder applications.



400G optical module/ODSP with four FOIC1.2-MFI interfaces on host using 8 × CEI-56G electrical lanes connected with a 400G pluggable module with eight optical lanes

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Figure 9-1c – Third example application of FOIC1.2-MFI interface

The bit rates of FOIC1.2-MFI are specified in Table 9-1.

Table 9-1 – Bit rates of FlexO-1-RS-n and FOIC1.2-MFI

FOI type	**FOI nominal bit rate** (kbit/s)	**FOI bit-rate tolerance** (ppm)
FlexO-1-RS-n	n × 2 × 256/241 × 239/226 × 49 766 400	±20
FOIC1.2-MFI	2 × 256/241 × 239/226 × 49 766 400	±20
FOIC1.2-MFI lane	256/241 × 239/226 × 49 766 400	±20
NOTE – The nominal FOIC1.2-MFI lane bit rate is approximately: 55 904 737.223 kbit/s.		

9.2 FOIC2.4-MFI and FOIC4.8-MFI structures

As shown in Figure 7-1 and Figure 10-1 or 10-9 of [ITU-T G.709.1], one or more OTUCn_i signal ($n_i \geq 1$ and $\sum n_i = n$), full-rate or sub-rated (with some OPUCn_i tributary slots marked as unavailable), are mapped over a FlexO-n signal structure composed of n 100G FlexO instances, each carrying an OTUC instance. The FlexO-n structure can be distributed into m FlexO-2 or m FlexO-4 frame structures further adapted and carried over m FlexO-2-<int> or m FlexO-4-<int> bonded optical interfaces.

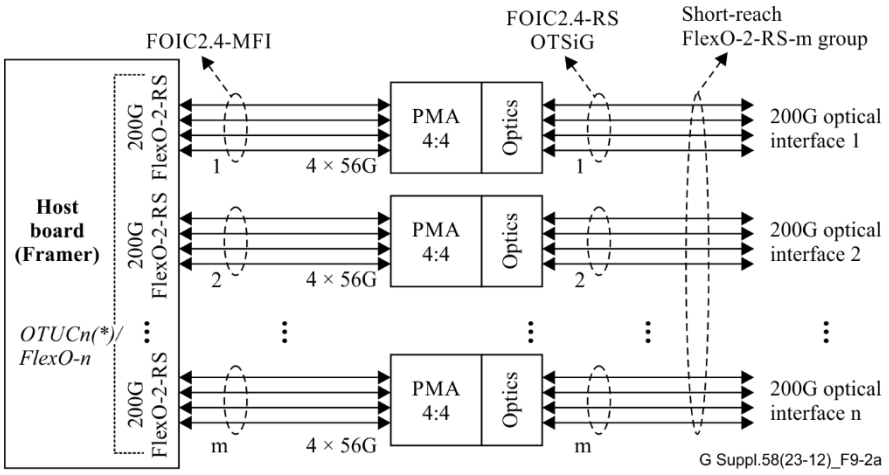
For short-reach FlexO-x-RS-m interface group application (i.e., <int>=RS) with {x,k} = {2,4} or {4,8} respectively, each FlexO-2-RS interface signal (carrying up to two OTUC) is distributed and transported over four physical lanes FOIC2.4-RS interface and each FlexO-4-RS frame (carrying up to four OTUC) is distributed and transported over eight physical lanes FOIC4.8-RS interface per Figure 7-1 of [ITU-T G.709.5]. This provides interoperable modular short-reach OTN interfaces for B100G OTUCn and FlexO-n (n ≥ 1) transport signals, by bonding m 200G or m 400G standard-rate optical interfaces or optical lane groups.

Four-lane pluggable modules developed for Ethernet 200GBASE-R applications and supporting the FlexO rate (i.e., about half the OTU4 rate per 56G lane) could be reused for FlexO-2-RS transport and FOIC2.4-RS interface. Eight-lane pluggable modules developed for Ethernet 400GBASE-R applications and supporting the FlexO rate (i.e., about half the OTU4 rate per 56G lane) could also be reused for FlexO-4-RS transport and FOIC4.8-RS interface. Modules developed for [b-IEEE 802.3] specified 200GBASE-FR4, 200GBASE-LR4, 400GBASE-FR8 and 400GBASE-LR8.

They have corresponding optical specifications for FlexO-2-RS and FlexO-4-RS interfaces with the optical parameters as specified for the PAM4 application codes 4I1-4D1F and 8R1-4D1F or 8I1-4D1F, respectively, of [ITU-T G.959.1] and PAM4 application code C4S1-4D1F of [b-ITU-T G.695]. The 200G modules have a four-lane WDM interface and the 400G modules have an eight-lane interface to and from a transmit/receive pair of ITU-T G.652 optical fibres.

Most of these pluggable modules use a four-lane electrical chip-to-module interface (200GAUI-4) or an eight-lane chip-to-module interface (400GAUI-8), whose specifications are found in Annex 120E of [b-IEEE 802.3]. For these optical modules supporting FlexO bit rate, the FOIC2.4-MFI or FOIC4.8-MFI chip-to-module electrical interface could be used, using FOIC2.4-RS or FOIC4.8-RS lane structure, respectively.

These applications of m FOIC2.4-RS bonded interfaces (short-reach FlexO-2-RS-m group) and m FOIC4.8-RS bonded interfaces (short-reach FlexO-4-RS-m group) using FOIC2.4-MFI or FOIC4.8-MFI chip-to-module interfaces are illustrated in Figures 9-2a and 9.2b respectively.



m FOIC2.4-RS short-reach interfaces using CEI-56G to m bonded 200G optical modules (2m ≥ n)
(*) *NOTE – Some OPUCn tributary slots may be marked as unavailable; if 2m = n, then each 200G FlexO-2-RS carries two OTUC; else if 2m > n, some 200G FlexO-2-RS signal frames within the group only carry one OTUC in their first 100G FlexO instance (second 100G FlexO instance being unequipped)*

Figure 9-2a – FOIC2.4-MFI interface main application example

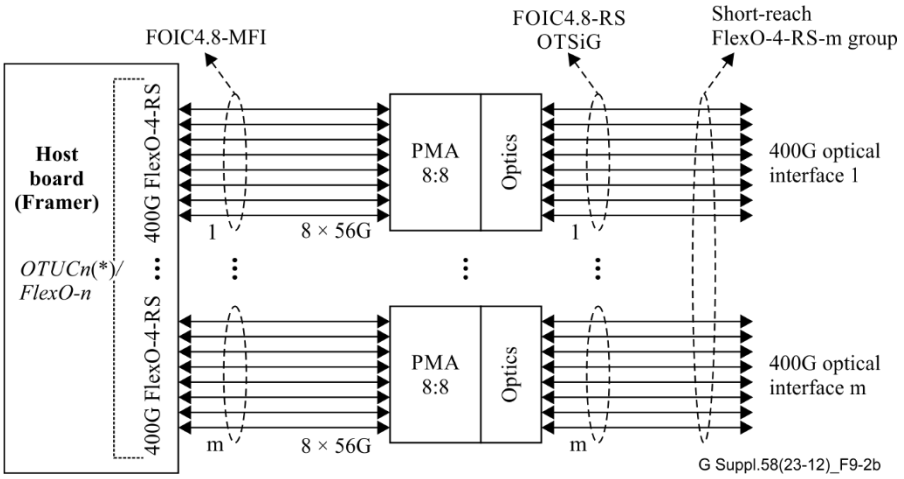
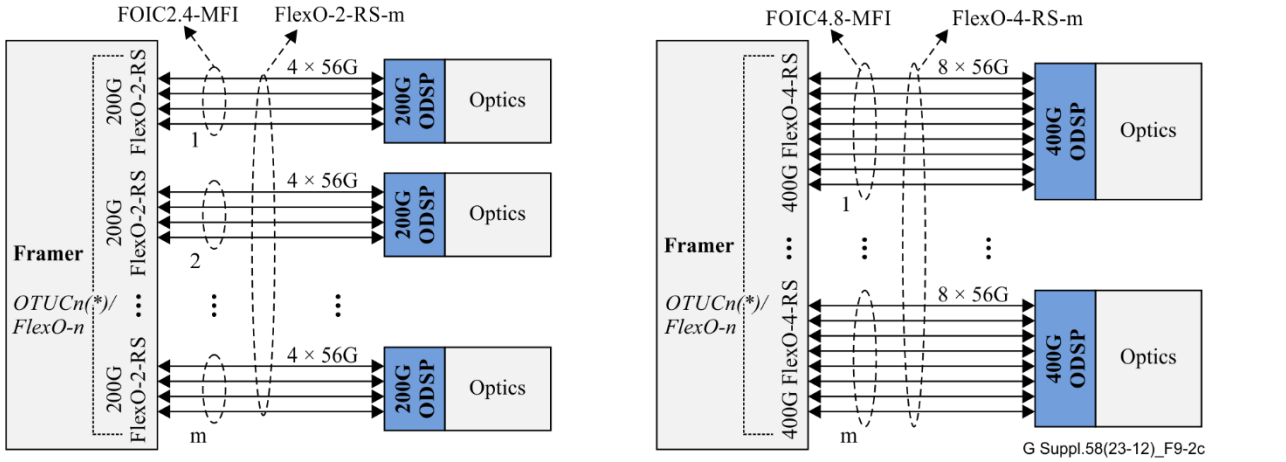


Figure 9-2b – FOIC4.8-MFI interface main application example

The FOIC2.4-MFI or FOIC4.8-MFI interface using FOIC2.4-RS or FOIC4.8-RS lane format could be used instead of two or four FOIC1.4-MFI interfaces to connect a beyond 100G OTN framer with one or more 200G or 400G ODSP devices or optical module supporting FlexO interfaces on the host side. One possible advantage for implementers is that the FEC and lane processing for FOIC2.4-MFI or FOIC4.8-MFI interface is almost identical to 200GAUI-4 or 400GAUI-8, respectively, thus allowing implementers to share digital logic in an optimized DSP supporting both Ethernet and OTN signals on its host side. This alternate application is illustrated in Figure 9-2c.



m FOIC2.4-RS interfaces using CEI-56G
Framer connected with m ODSPs (2m ≥ n)
(*) *NOTE – Some OPUCn tributary slots may be marked as unavailable*

m FOIC4.8-RS interfaces using CEI-56G
Framer connected with m ODSPs (4m ≥ n)
(*) *NOTE – Some OPUCn tributary slots may be marked as unavailable*

Figure 9-2c – Alternate application of FOIC2.4-MFI and FOIC4.8-MFI interfaces

Depending on the application or type of optical module, the module may be agnostic and fully transparent to the FOIC2.4-RS or FOIC4.8-RS lane structure or the RS FEC may be terminated. In the second case the FlexO-2 or FlexO-4 may be fully terminated (the OTUC instances are mapped/demapped to/from FlexO instances) or partially terminated (RS FEC and part of FlexO overhead is terminated). For partial termination, different FlexO overhead fields may be terminated or carried transparently in the ODSP.

Per the mapping specifications in clause 10.1 or 10.3 of [ITU-T G.709.1], one or more $OTUCn_i$ signals ($n_i \geq 1$ and $\sum n_i = n$) is split into n times OTUC, and each OTUC is mapped into an individual 100G FlexO instance of a FlexO-n structure. Each 100G FlexO frame consists of frame alignment mechanism field (AM) , extended overhead field (EOH), basic overhead field (BOH), and payload area in which the OTUC is transported (see clause 8 of [ITU-T G.709.1]).

Then, as described in clauses 12.1 and 12.5.4 of [ITU-T G.709.5] for FlexO-2-RS, each pair of 100G FlexO instances (A,B) of the FlexO-n are interleaved (on a 10-bit basis) into a FlexO-2 frame that is adapted to a FlexO-2-RS frame signal including RS FEC parity. m FlexO-2-RS frames carry the FlexO-n ($n \leq 2$ m). If [$n = 2$ m], then each 200G frame carries two OTUC. When [$n < 2$ m], then [i] 200G frames carry two OTUC, while [m-i] 200G frames only carry one OTUC in their first 100G FlexO instance (the second 100G FlexO instance being unequipped).

As described in clauses 13.1 and 13.5.5 of [ITU-T G.709.5] for FlexO-4-RS, each set of four 100G FlexO instances of the FlexO-n are interleaved (on a 10-bit basis) into a FlexO-4 frame that is adapted to a FlexO-4-RS frame signal including RS FEC parity. m FlexO-4-RS frames carry the FlexO-n ($n \leq 4$ m). If [$n = 4$ m], then each 400G frame carries four OTUC. If [$n < 4$ m], then, some 400G frames carry fewer than four, but at least one OTUC [the last one, two or three 100G FlexO instance(s) being unequipped].

When FlexO basic OH is not carried transparently in the ODSP, see clause 9.1 for this type of application. In this case, the receive ODSP detects the receive line pre-FEC LD and optionally forwards the LD status bit to the receive framer device through the MFI, as carried in bit 8 of the STAT field of the first 100G FlexO instance OH of the 200G or 400G FlexO-x-RS frame per Figure 9-2d. Alternatively, when FlexO extended overhead is not carried transparently, the receive line pre-FEC LD could be processed as specified in clause 9.3.3.2.2 of [ITU-T G.709.1] and forwarded through the MFI is bit 8 of the RSTAT field of all four FlexO instance EOH.

The FlexO-x to FlexO-x-RS adaptation process (x = 2 or 4) consists in FEC parity area addition, scrambling, alignment markers values (AMi) insertion, and RS10 (544,514) FEC parity calculation based on two interleaved RS10 codewords. For FlexO-2-RS, the resulting 200G signal is distributed on eight 28G logical lanes as per the FOIC2.k-RS interface specifications in clause 12.5 of [ITU-T G.709.5]. For FlexO-4-RS, the resulting 400G signal is distributed on sixteen 28G logical lanes as per the 400G FOIC4.k-RS interface specifications in clause 13.5 of [ITU-T G.709.5]. FEC calculation and lane distribution (in groups of 10 bits) follow the same processes as specified in clause 119 of [b-IEEE 802.3] for 200GBASE-R and 400GBASE-R interfaces, respectively.

Each 56G lane of a FOIC2.4-MFI or FOIC4.8-MFI using FOIC2.4-RS or FOIC4.8-RS lane format is formed by simple bit-multiplexing of two 28G logical lanes from the same FlexO-2-RS or FlexO-4-RS, respectively. At the sink, the bits from each individual 56G FOIC2.4-MFI or 56G FOIC4.8-MFI lane are deinterleaved into two 28G logical lanes.

When the RS FEC is terminated, the sink identifies each of the eight 28G logical lanes within a FOIC2.4-MFI interface according to its AMi specific pattern (UMx and UPx values). The sink must support the eight 28G logical lanes in any position, and in addition to 28G logical lane alignment and deskew, proceed to reorder these eight 28G logical lanes prior to reassembly into a FlexO-2-RS frame. Similarly, in the case of FOIC4.8-MFI, the sink must support the sixteen 28G logical lanes in any position, and in addition to 28G logical lane alignment and deskew, proceed to reorder these sixteen 28G logical lanes prior to reassembly into a FlexO-4-RS frame.

After FEC termination and descrambling of the 200G or 400G FlexO-x frame, the FlexO OH may be processed, and, depending on the application, each OTUC can be demapped from its deinterleaved 100G FlexO instance and aligned if FlexO-x is fully terminated. At the framer sink, the receive line pre-FEC LD status bit is extracted from the FlexO OH area and the n_i OTUC of each OTUCn_i client port demapped from the FlexO-n structure extracted from the m FOIC2.4-MFI or m FOIC4.8-MFI interfaces are deskewed to retrieve the original OTUCn_i signal(s). At the ODSP sink, and if applicable, n_j OTUC demapped from FlexO-2 (extracted from FOIC2.4-MFI) or demapped from FlexO-4 (extracted from FOIC4.8-MFI interface) could be aligned, deskewed, crunched (removing unavailable tributary slots) and assembled as the digital signal to be optically transmitted. See Figure 9-2d.

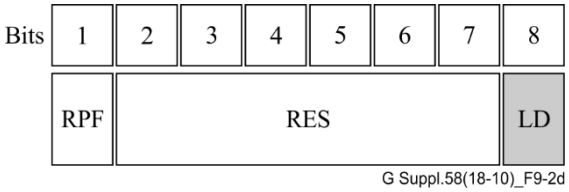


Figure 9-2d – Optional receive line pre-FEC local degrade status bit location in first instance of FlexO BOH STAT field (Receive ODSP to framer direction)

The bit rates of the FOIC2.4-MFI and FOIC4.8-MFI are specified in [ITU-T G.709.5] for FOIC2.4-RS and FOIC4.8-RS and indicated in Tables 9-2a and 9-2b, respectively.

Table 9-2a – Bit rates of FlexO-2-RS-m and FOIC2.4-MFI

FOI type	**FOI nominal bit rate** (kbit/s)	**FOI bit-rate tolerance** (ppm)
FlexO-2-RS-m	m × 4 × 256/241 × 239/226 × 49 766 400	±20
FOIC2.4-MFI	4 × 256/241 × 239/226 × 49 766 400	±20
FOIC2.4-MFI lane	256/241 × 239/226 × 49 766 400	±20
NOTE – The nominal FOIC2.4-MFI lane bit rate is approximately: 55 904 737.223 kbit/s.		

Table 9-2b – Bit rates of FlexO-4-RS-m and FOIC4.8-MFI

FOI type	FOI nominal bit rate	FOI bit-rate tolerance
FlexO-4-RS-m	m × 8 × 256/241 × 239/226 × 49 766 400	±20
FOIC4.8-MFI	8 × 256/241 × 239/226 × 49 766 400	±20
FOIC4.8-MFI lane	256/241 × 239/226 × 49 766	±20
NOTE – The nominal FOIC4.8-RS lane bit rate is approximately: 55 904 737.223 kbit/s.		

9.3 OTL50.1-RS and OTL50u.1-RS structures

As described in clause 9.6 of [ITU-T G.709.4], an OTU50-RS signal can be distributed (in groups of 10 bits) over two 28G logical lanes that can be bit-multiplexed into a single OTL50.1-RS lane. The same scheme is used to adapt an OTU50u-RS signal into an OTL50u.1-RS lane.

NOTE – The RS (544, 514, 10) FEC scheme and lane distribution for OTU50-RS and OTU50u-RS signals in accordance with [ITU-T G.709.4], are the same as specified in clause 134 of [IEEE 802.3] for 50GBASE-R interface.

The OTL50.1-RS or OTL50u.1-RS interface could be used as a single lane MFI in order to connect a 50G OTN framer with a 50G pluggable module supporting a 50G electrical lane on its host side.

These modules include a simple retimer and provide an interoperable optical interface format for OTU50-RS or OTU50u-RS short-reach interfaces.

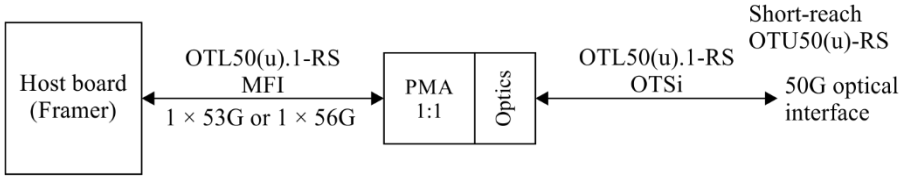
The framer sink bit-demultiplexes the 50G OTL50(u).1-RS electrical lane (MFI received from the module) into two 26G logical lanes and identifies each of the two 26G logical lanes according to its AMi specific pattern (UMx values). After alignment and deskew, these two 26G logical lanes are interleaved (in groups of 10 bits) into an OTU50(u)-RS frame.

In accordance with Table 9-3b, the OTL50u.1-RS interface operates within the 50GAUI-1 interface bit rate range and with similar lane and FEC format. There is just a +15.6 ppm offset between the two nominal rates. So, pluggable modules developed for Ethernet 50GBASE-R applications with simple retimer and 50GAUI-1 interface on the host side could be reused for underclocked 50G OTN signal transport (i.e., OTU50u-RS) with an OTL50u.1-RS MFI between the framer and the optical module.

If such a module also supports a full-rate 50G OTN interface with a single lane OTL50.1-RS MFI on its host side (i.e., 56G electrical lane with almost the same bit rate as the FOIC1.2 lane and similar FEC and lane format to 50GAUI-1), it could also be reused for OTU50-RS full-rate transport.

Modules developed for [b-IEEE 802.3] are specified 50GBASE-LR and 50GBASE-ER with a PAM4 optical PMD sublayer, and may be used for OTU50(u)-RS interfaces when conforming to the optical specifications and parameters to be determined by application codes for metro networks. Some of these 50G modules may have a single WDM interface to and from a transmit/receive pair of ITU-T G.652 optical fibres.

These applications of OTL50.1-RS and OTL50u.1-RS interfaces (considering metro network transport of OTU50-RS and OTU50u-RS) are illustrated in Figure 9-3.



Full-rate or underclocked OTL50.1-RS interface using CEI-56G to single-lane 50G optical module (i.e. PAM4)

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Figure 9-3 – Example application of single lane OTL50.1-RS and OTL50u.1-RS interfaces

The bit rates of these full-rate (i.e., OTL50.1-RS) and underclocked (i.e., OTL50u.1-RS) interfaces and lanes are listed in Tables 9-3a and 9-3b, in accordance with [ITU-T G.709.4] specifications.

Table 9-3a – Bit rates of single lane OTL50.1-RS

OTL type	**OTL nominal bit rate** (kbit/s)	**OTL bit-rate tolerance** (ppm)
OTL50.1-RS	1 × 255/227 × 49 766 400	±20
OTL50.1-RS lane	255/227 × 49 766 400	±20
NOTE – The nominal OTL50.1-RS lane bit rate is approximately: 55 904 986.784 kbit/s.		

Table 9-3b – Bit rates of single-lane OTL50u.1-RS

OTL type	**OTL nominal bit rate**	**OTL bit-rate tolerance**
OTL50u.1-RS	1 × 680/637 × 49 766 400	±20
OTL50u.1-RS lane	680/637 × 49 766 400	±20
NOTE – The nominal OTL50u.1-RS lane bit rate is approximately: 53 125 827.316 kbit/s.		

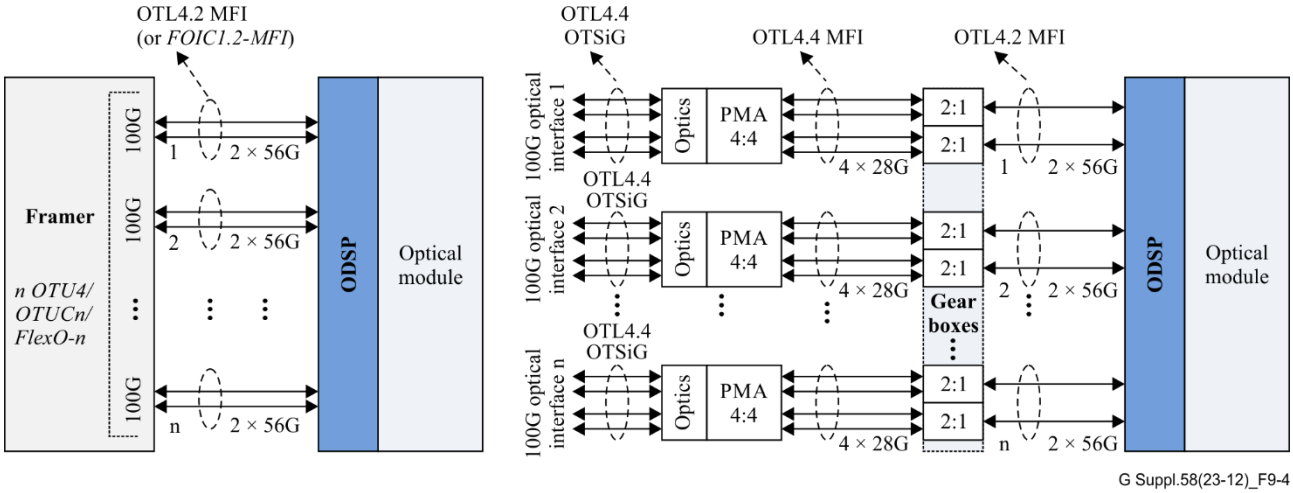
9.4 OTL4.2 structure

The purpose of the OTL4.2 interface is to carry an OTU4 signal over two 56G physical lanes.

As described in Annex C of [ITU-T G.709], the scrambled OTU4 frame is split, distributed, and adapted to twenty 5G OTL4 logical lanes, each carrying an LLM number as a unique identifier. Each 56G physical lane of the OTL4.2 is formed by simple bit-multiplexing of ten of these 5G logical lanes. At the sink, the bits from each individual 56G OTL4.2 lane are deinterleaved into ten 5G logical lanes. The sink identifies each of the twenty 5G logical lanes within an OTL4.2 interface according to its LLM number. The sink must support the twenty 5G logical lanes in any position, and in addition to 5G logical lane alignment and deskew, proceed to reorder these twenty 5G logical lanes prior to reassembly into the OTU4 frame.

The OTL4.2 MFI could be used to connect OTU4 signals to the host side of a B100G ODSP device using 56G electrical lanes. Such a device may only support 56G electrical lanes on its host side for multiple OTU4 and OTUCn/FlexO-n client interfaces to be multiplexed towards its line side interface. In this application example, the OTL4.2 interface could connect a B100G ODSP device with a multi-100G OTN framer as shown on the left side of Figure 9-4. Alternatively, the OTL4.2 interface could connect a B100G ODSP device with a 2 × 56G PAM-4 to 4 × 28G NRZ OTL4.4 gearbox device connected to a 100G four-lane pluggable module in a muxponder application as shown on the right side of Figure 9-4.

NOTE – The OTU4 RS8 FEC combined with the OTL4.2 lane striping was not specified considering 56G PAM4 electrical lane characteristics and may encounter significant performances degradation when exposed to correlated burst errors. So, to guarantee proper operation, implementers could for example limit the reach of the electrical interface or ensure that the raw bit error ratio (BER) on each OTL4.2 electrical lane is several decades lower than the highest raw BER on a 56G PAM4 electrical lane that is specified in [b-OIF CEI].



n OTL4.2 (*and/or FOIC1.2-MFI*) interfaces using CEI-56G Framer connected with optical module/ODSP

Single optical module/ODSP with n OTL4.2 interfaces on host using CEI-56G connected (Through 1:2 gear boxes) with n 100G 4-lane OTL4.4 pluggable modules

Figure 9-4 – Example applications of an OTL4.2 interface

The bit rates of OTL4.2 are specified in Table 9-4.

Table 9-4 – Bit rates of OTL4.2

OTL type	**OTL nominal bit rate** (kbit/s)	**OTL bit-rate tolerance** (ppm)
OTL4.2	2 × 255/227 × 49 766 400	±20
OTL4.2 lane	255/227 × 49 766 400	±20
NOTE – The nominal OTL4.2 lane bit rate is approximately: 55 904 986.784 kbit/s.		

10 Signal formats and rates carried over 112G electrical lanes

This clause describes some MFI structures using 112G physical lanes to carry B100G OTUCn or FlexO-n signals or using 106G physical lanes to carry Ethernet optimized FlexO-ne signals ($n \geq 1$). The electrical characteristics of each 112G or 106G physical lane may comply with [b-OIF CEI] CEI-112G-*x*R-PAM4 specifications.

10.1 FOIC1.1-MFI structure

As shown in Figures 7-1 and 10-1 or 10-9 of [ITU-T G.709.1], one or more $OTUCn_i$ signal ($n_i \geq 1$ and $\sum n_i = n$), full-rate or sub-rated (with some $OPUCn_i$ tributary slots marked as unavailable), can be mapped over a FlexO-n signal structure composed of n 100G FlexO instances, each carrying an OTUC instance.

In order to connect beyond 100G OTN framers with ODSP devices and line side optical modules over 112G electrical lanes, the FlexO-n structure can be distributed into n FlexO-1 frames (each carrying an OTUC) further adapted into n FlexO-1-RS frame signals per Figure 7-1 of [ITU-T G.709.5]. Each FlexO-1-RS is then adapted into a FOIC1.1-RS lane format carried over single electrical lane FOIC1.1-MFI interface.

Figure 10-1a provides such application examples of an OTUCn signal carried over n FOIC1.1-MFIs (FlexO-1-RS-n group signal, with x = 1 and k = 1).

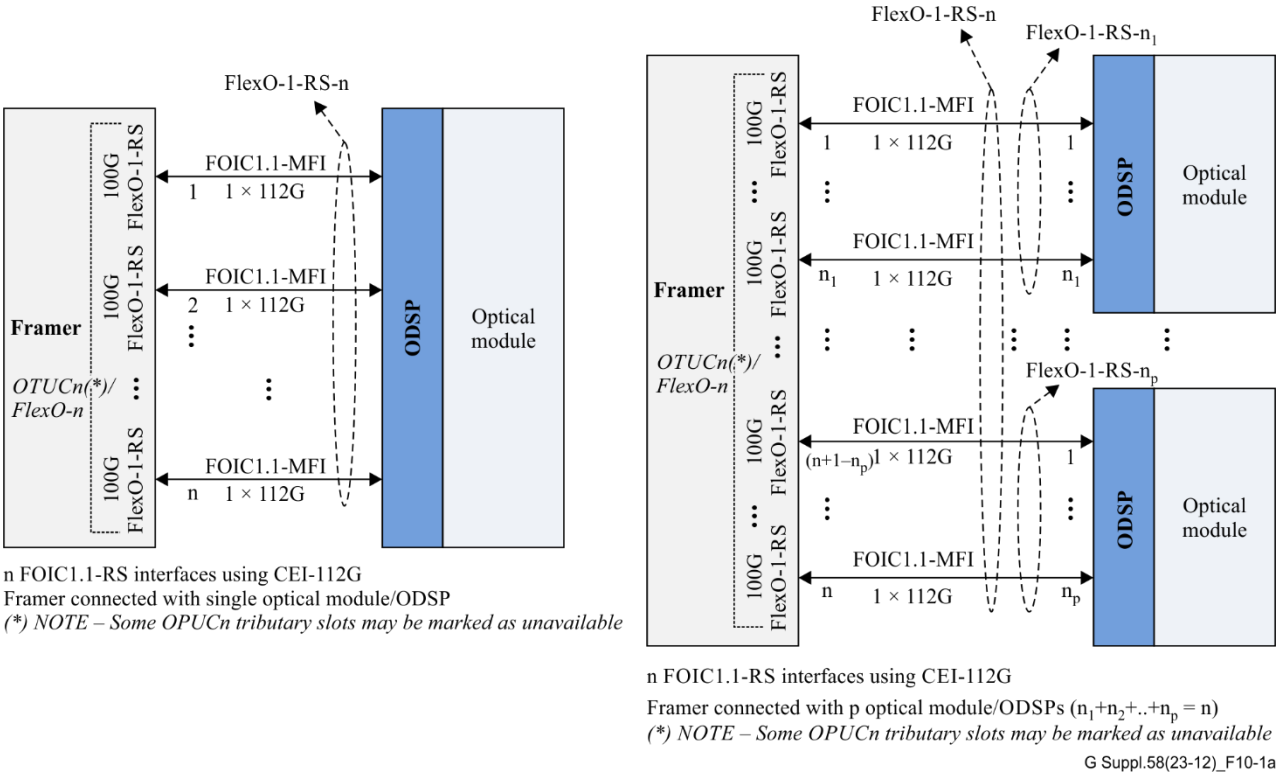


Figure 10-1a – First example applications of a FOIC1.1-MFI interface

Per the mapping specifications in clause 10.1 or 10.3 of [ITU-T G.709.1] the OTUCn is split into n times OTUC, and each OTUC is mapped into an individual 100G FlexO instance of a FlexO-n structure. Each 100G FlexO instance corresponds to a FlexO-1 frame and consists of frame alignment mechanism field (AM), extended overhead field (EOH), basic overhead field (BOH), and payload area in which the OTUC is transported (see clause 8 of [ITU-T G.709.1]).

After FEC parity area addition over the FlexO-1 frame, synchronous scrambling, alignment markers (AMi) insertion and FEC [RS10(544,514)] parity computation (see clauses 11.3 and 11.4 of [ITU-T G.709.5]), each individual FlexO-1-RS frame is distributed (in groups of 10 bits) on four 28G logical lanes as described for FOIC1.4-RS in clause 11.5.1 of [ITU-T G.709.5].

As described in clause 11.5.5 of [ITU-T G.709.5], the 112G FOIC1.1-RS lane structure is formed by simple bit-multiplexing of all four 28G logical lanes from the same FlexO-1-RS, and then carried over single lane FOIC1.1-MFI electrical interface. At the sink, the bits from each individual 112G FOIC1.1-MFI lane are deinterleaved into four 28G logical lanes.

When the RS FEC is terminated, the sink identifies each of the four 28G logical lanes within a FOIC1.1-RS interface according to its AMi specific pattern (UMx and UPx values). The sink must support the four 28G logical lanes in any position, and in addition to 28G logical lane alignment and deskew, proceed to reorder these four 28G logical lanes prior to reassembly into a FlexO-1-RS frame. After FEC termination and descrambling of the FlexO-1-RS frame, the FlexO OH may be processed, and the OTUC demapped and aligned if FlexO-1 is terminated. At the framer sink, the receive line pre-FEC LD status bit is extracted from the FlexO OH area and the n OTUC that are demapped from the n FOIC1.1-MFI interfaces are deskewed to retrieve the original OTUCn signal. At the ODSP sink, n_i OTUC demapped from n_i FOIC1.1-RS interfaces could be aligned, deskewed, crunched (removing unavailable tributary slots), and assembled as the $OTUCn_i$ digital signal to be transmitted.

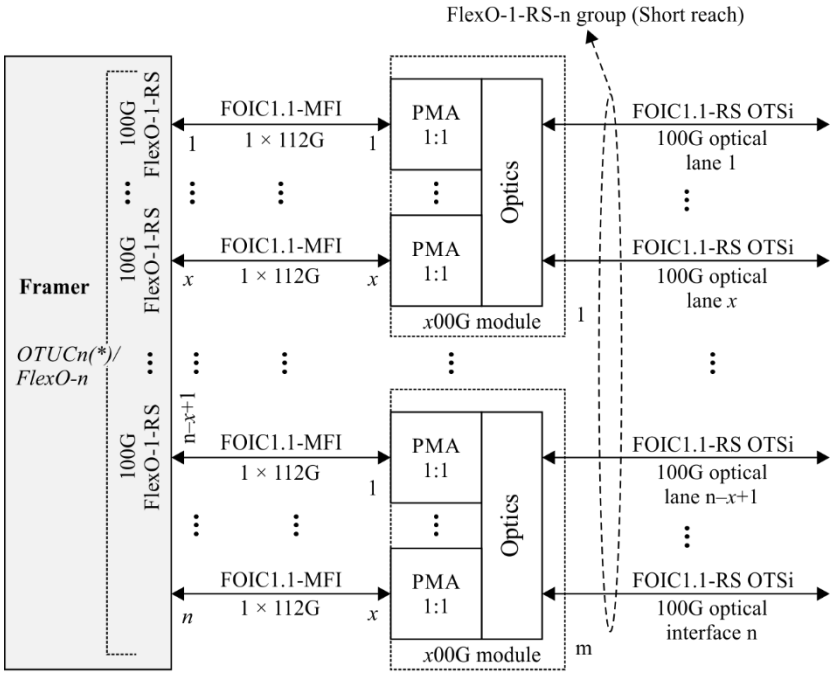
In the ODSP and depending on the application, the 28G logical lanes and RS FEC of the FOIC1.1-RS signal may be terminated or carried transparently, the FlexO extended OH may be terminated or carried transparently, the FlexO basic OH may be terminated or carried transparently, and the n_i OTUC demapped and aligned or not. This would correspond to different levels of transparency and

processing within the module, for segmented vs. concatenated or transparent FEC, FlexO-x regenerator, or FlexO-n multiplexing applications.

When FlexO basic overhead is not carried transparently in the ODSP, see clause 9.1 for this type of application; in this case the receive ODSP detects the receive line pre-FEC LD and optionally forwards the LD status bit to the receive framer device through the MFI, in bit 8 of FlexO BOH STAT field (see Figure 9-2d). Alternatively, when FlexO extended overhead is not carried transparently, the receive line pre-FEC LD could be processed as specified in clause 9.3.3.2.2 of [ITU-T G.709.1] and forwarded through the MFI in bit 8 of FlexO EOH RSTAT field.

Pluggable modules with 100G per lane developed for Ethernet 100GBASE-R applications and supporting the FlexO rate could be reused for FlexO-1-RS short reach optical transport applications. They have corresponding optical specifications for FlexO-1-RS per lane with the optical parameters as specified for the PAM4 application codes. Some of these pluggable modules may use single or multiple 100G electrical lane chip-to-module interface (e.g., *x* ×100GAUI-1 or *x*00GAUI-*x*, with $x \geq 1$) per Annex 120G of [b-IEEE 802.3ck]. One or multiple FOIC1.1-MFI interface carrying FlexO-1-RS signals with FOIC1.1-RS single lane format could be used to connect the host side of such pluggable optical module using 112G electrical lane(s) with a multi-100G OTN framer or the host side of a B100G ODSP device.

In Figure 10-1b application example, [m × *x*] FOIC1.1-MFIs connect m [*x* × 100G-lane] pluggable modules (e.g., *x* = 1,4,8) with a multi-100G OTN framer. In such application, the OTUCn signal ($n \geq 1$, $n \leq m \times x$) is carried over n FOIC1.1-RS bonded short reach optical lanes (FlexO-1-RS-n group). Each FOIC1.1-RS lane carries a FlexO-1-RS frame (carrying a single OTUC instance). This provides interoperable modular short-reach OTN interfaces for B100G OTUCn ($n \geq 1$) transport signals, by bonding n 100G standard optical lanes.



Framer with n FOIC1.1-MFI interfaces connected through CEI-112G electrical lanes with m *x*00G pluggable modules with *x* 100G optical lane each ($n \leq m \times x$)

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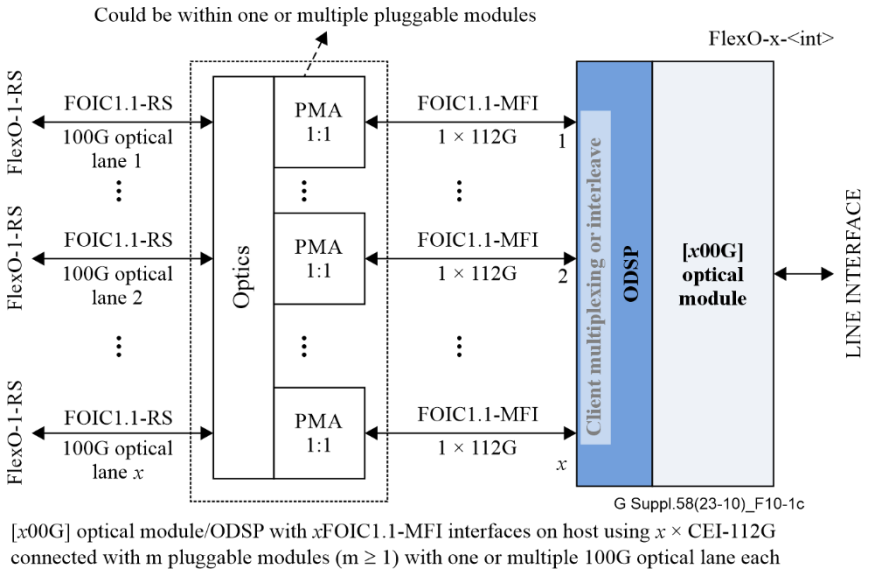
Figure 10-1b – Second example application of FOIC1.1-MFI interface

In Figure 10-1c application example, the FOIC1.1-MFI could be used to connect FlexO-1-RS signals between one or multiple pluggable modules (with 100G-class optical lane(s)) and the host side of a [*x* × 100G] ODSP device or line side optical module. On its host side, the ODSP could integrate

multiple 100G OTN clients multiplexing (the clients could be plesiochronous) or simple interleaving functions (if the clients are source-synchronous) for single-chip muxponder applications.

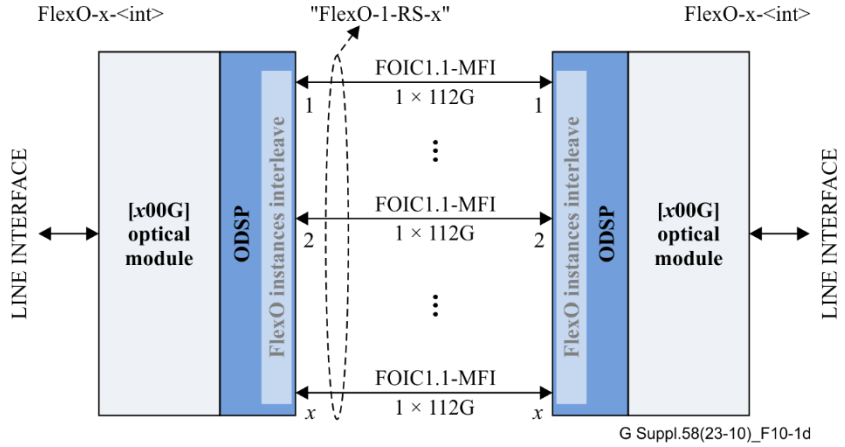


[x00G] optical module/ODSP with *x*FOIC1.1-MFI interfaces on host using *x* × CEI-112G connected with m pluggable modules (m ≥ 1) with one or multiple 100G optical lane each

Figure 10-1c – Third example application of FOIC1.1-MFI interface

For FlexO-x-<int> regenerator applications, two line side optical modules could be connected through their host interfaces over x 112G electrical lanes to carry a FlexO-x client signal. The FlexO-x frame signal can be distributed into x FlexO-1 frames, further adapted into x FlexO-1-RS frame signals. Each FlexO-1-RS is then adapted into a FOIC1.1-RS lane carried over single electrical lane FOIC1.1-MFI interface.

Figure 10-1d provides such FlexO regenerator application example of a FlexO-x signal carried over x FOIC1.1-RS MFIs ("FlexO-1-RS-x").



Two [x00G] optical module/ODSP connected through x FOIC1.1-MFI interfaces on host using x CEI-112G electrical lanes (x ≥ 1)

Figure 10-1d – Fourth example application of FOIC1.1-MFI interface

After receive line side FEC termination and FlexO regenerator sink overhead processing, at the MFI source the FlexO-x frame signal is z-bit deinterleaved into x 100G FlexO instances (e.g., z = 10 or 128 depending on the type of FlexO-x-<int> line interface). Then each FlexO-1 frame is adapted into a FlexO-1-RS frame per clause 11 of [ITU-T G.709.5]. Each resulting FlexO-1-RS frame is distributed (in groups of 10 bits) on four 28G logical lanes which are bit-multiplexed into a 112G FOIC1.1-RS lane carried over single lane FOIC1.1-MFI electrical interface. Note that receive line pre-FEC LD is

processed as specified in clause 9.3.3.2.2 of [ITU-T G.709.1] and forwarded through the MFI in bit 8 of FlexO EOH RSTAT field.

At the sink, the bits from each individual 112G FOIC1.1-MFI lane are deinterleaved into four 28G logical lanes. Each 28G logical lane is identified within a FOIC1.1-MFI interface according to its AMi specific pattern (UMx and UPx values). The sink must support the four 28G logical lanes in any position, and in addition to 28G logical lane alignment and deskew, proceed to reorder these four 28G logical lanes prior to reassembly into a FlexO-1-RS frame. Note that the interchanging and reordering of 112G FOIC1.1-MFI electrical lanes is currently not defined and as such not supported. After FEC termination and descrambling of the FlexO-1-RS frame, the resulting x FlexO-1 frames are deskewed and z-bit interleaved into a FlexO-x signal (e.g., z = 10 or 128 depending on the type of FlexO-x<int> line interface) towards the transmit line interface. FlexO regenerator overhead source processing is performed and Line FEC is inserted towards the remaining transmit optical line side processing functions.

The bit rates of FOIC1.1-MFI are the same as specified in [ITU-T G.709.5] for FOIC1.1-RS and indicated in Table 10-1.

Table 10-1 – Bit rates of FlexO-1-RS-n and FOIC1.1-MFI

FOI type	**FOI nominal bit rate** (kbit/s)	**FOI bit-rate tolerance** (ppm)
FlexO-1-RS-n	n × 256/241 × 239/226 × 99 532 800	±20
FOIC1.1-MFI	256/241 × 239/226 × 99 532 800	±20
FOIC1.1-MFI lane	256/241 × 239/226 × 99 532 800	±20
NOTE – The nominal FOIC1.1-MFI electrical lane bit rate is approximately: 111 809 474.446 kbit/s.		

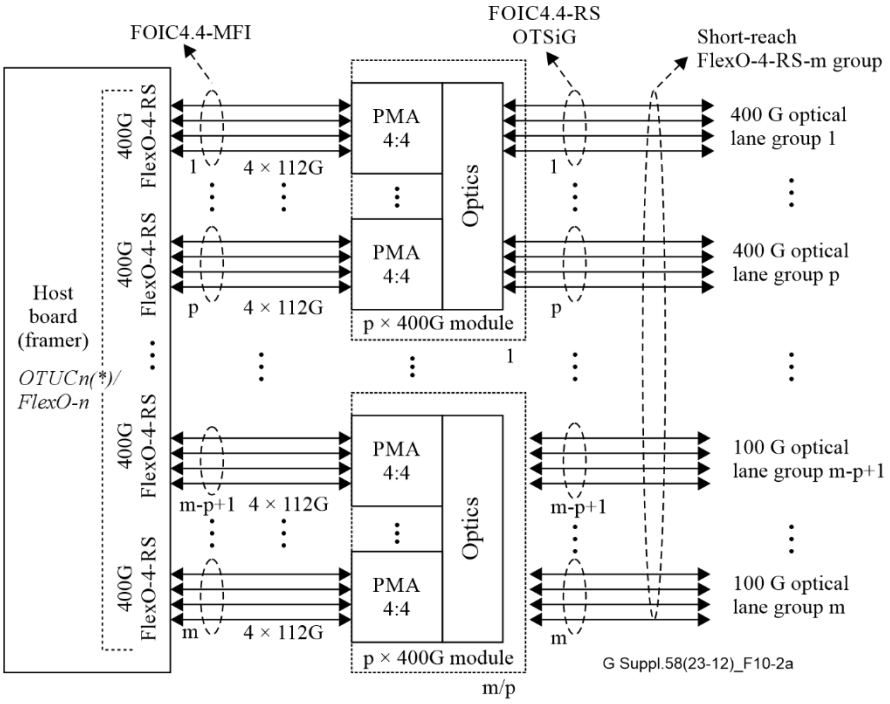
10.2 FOIC4.4-MFI structure

As shown in Figures 7-1 and 10-1 or 10-9 of [ITU-T G.709.1], one or more OTUCn_i signal ($n_i \geq 1$ and $\sum n_i = n$), full-rate or sub-rated (with some OPUCn_i tributary slots marked as unavailable), is mapped over a FlexO-n signal structure composed of n 100G FlexO instances, each carrying an OTUC instance. The FlexO-n structure can be distributed into m FlexO-4 frame structures further adapted and carried over m FlexO-4-<int> bonded optical interfaces.

For short reach FlexO-4-RS-m interface group applications (i.e., <int> = RS) with {x,k} = {4,4}, each FlexO-4-RS interface signal (carrying up to four OTUC) is distributed and transported over four 112G physical lanes FOIC4.4-RS interface per Figure 7-1 of [ITU-T G.709.5]. This provides interoperable modular short-reach OTN interfaces for B100G OTUCn and FlexO-n (n ≥ 1) transport signals, by bonding m 400G optical interfaces or optical lane groups.

Pluggable modules with 100G per lane developed for Ethernet 400GBASE-R applications and supporting short-reach FlexO rate (that is ~112 Gbit/s per lane) could be reused for FlexO-4-RS transport and FOIC4.4-RS interface. They have corresponding optical specifications for FlexO-4-RS interfaces with the optical parameters as specified for the PAM4 application codes. These modules have a [p × 4] 100G lanes to and from a transmit/receive pair of ITU-T G.652 optical fibres. These pluggable modules may use [p × 4] 100G electrical lanes chip-to-module interface (p 400GAUI-4, with $p \geq 1$), whose specifications are found in Annex 120G of [b-IEEE 802.3ck]. For these optical modules supporting FlexO bit rate, p FOIC4.4-MFI chip-to-module electrical interfaces could be used, each with FOIC4.4-RS lane structure.

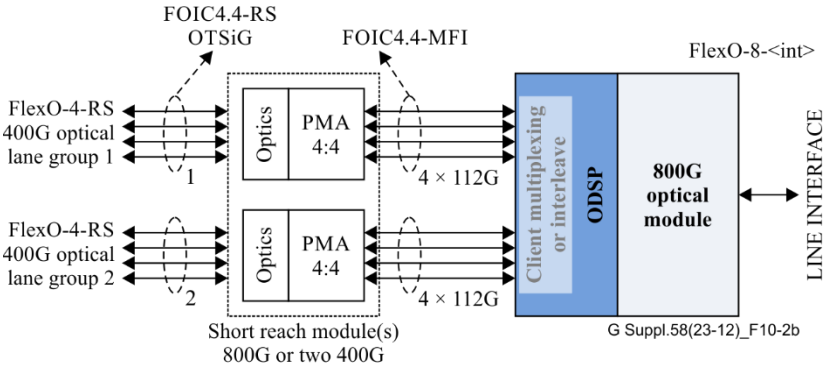
This application of m FOIC4.4-RS bonded interfaces (short-reach FlexO-4-RS-m group) using FOIC4.4-MFI chip-to-module interfaces is illustrated in Figure 10-2a.



m FOIC4.4-MFI interfaces using CEI-112G to m/p bonded [p × 400G] pluggable modules (4m ≥ n)
One or more 400G optical lane group (FOIC4.4-RS) could be within the same [p × 4 × 100G] module with p ≥ 1
(*) NOTE – Some OPUCn Tributary slots may be marked as unavailable; if 4m = n, then each 400G FlexO-4-RS carries four OTUC; else if 4m > n, some 400G FlexO-4-RS signal frames within the group only carry one, two or three OTUC in their first 100G FlexO instance(s) (The last 100G FlexO instance(s) being unequipped).

Figure 10-2a – First example application of FOIC4.4-MFI interface

In Figure 10-2b application example, the FOIC4.4-MFI could be used to connect FlexO-4-RS signals between a [*p*×400G] pluggable optical module and the host side of a B400G ODSP device integrating *p* × 400G OTN client multiplexing (the clients could be plesiochronous) or supporting simple interleaving functions (if the clients are source-synchronous) for single-chip muxponder applications.



Single 800G optical module/ODSP with two FOIC4.4-MFI interfaces on host using 8 × CEI-112G lanes connected with either an 800G 8-lane pluggable module or two 400G 4-lane pluggable modules

Figure 10-2b – Second example application of FOIC4.4-MFI interface

The FOIC4.4-MFI interface using FOIC4.4-RS lane structure could also be used to connect beyond 400G OTN framer with one or more optical line DSP (ODSP) devices. Such device may be limited to 400G client granularity on its host side (e.g., multiple synchronous 400G or 800G MFI interface). Depending on the application or type of optical module, the module may be agnostic and fully transparent to the FOIC4.4-RS lane structure or the RS FEC may be terminated. In the second case the FlexO-4-RS may be fully terminated (the OTUC instances are mapped/demapped to/from FlexO-4) or partially terminated (RS FEC and part of FlexO overhead is terminated). For partial termination, different FlexO overhead fields may be terminated or carried transparently in the ODSP.

When FlexO basic overhead is not carried transparently in the ODSP, see clause 9.1 for this type of application; in this case, the receive ODSP detects the Rx line pre-FEC Local Degrade (LD) and optionally forwards the LD status bit to the receive framer device through the MFI, as carried in bit 8 of the STAT field of the first 100G FlexO instance basic overhead (BOH) of the FlexO-4-RS frame, per Figure 9-2d. Alternatively, when FlexO extended overhead is not carried transparently, the receive line pre-FEC LD could be processed as specified in clause 9.3.3.2.2 of [ITU-T G.709.1] and forwarded through the MFI is bit 8 of the RSTAT field of all four FlexO instance EOH. This application is illustrated in Figure 10-2c with the example of 400G or 800G ODSP/optical modules.

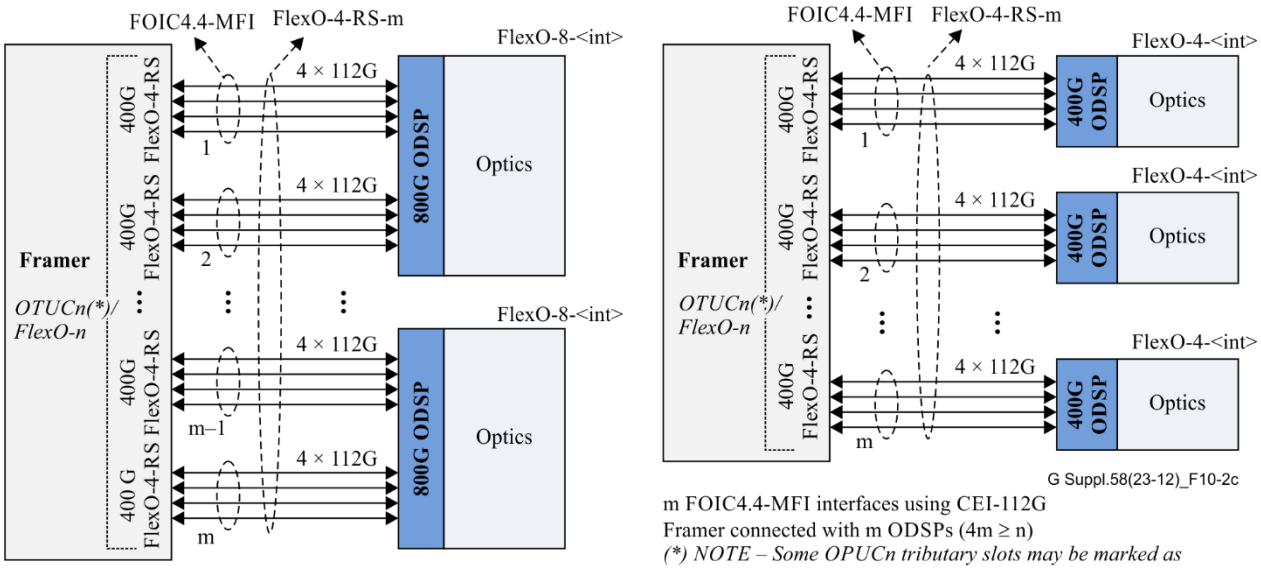


Figure 10-2c – Third example applications of FOIC4.4-MFI interface

As described in clause 13.5.6 of [ITU-T G.709.5], each 112G lane of FOIC4.4-MFI using FOIC4.4-RS lane format is formed by simple bit-multiplexing of four 28G logical lanes from the same FlexO-4-RS. At the sink, the bits from each individual 112G FOIC4.4-MFI lane are deinterleaved into four 28G logical lanes. The sink could identify each of the sixteen 28G logical lanes within a FOIC4.4-MFI interface according to its alignment marker specific pattern (unique UMx and UPx values).

When the RS FEC is terminated, the sink must be able to accept the sixteen 28G logical lanes in any position, and in addition to 28G logical lanes alignment and deskew, proceed to reorder these sixteen 28G logical lanes prior to reassembly into a FlexO-4-RS frame. Note that the interchanging and reordering of 112G electrical lanes from different FOIC4.4-MFI interfaces is currently not defined and as such not supported.

For full termination of the FOIC4.4-MFI, and per the mapping and framing specifications in clause 10.1 or 10.3 of [ITU-T G.709.1] one or more $OTUCn_i$ signals are split into n times OTUC ($n_i \geq 1$ and $\sum n_i = n$), and each OTUC is mapped into an individual 100G FlexO instance of a FlexO-n structure. Each 100G FlexO instance frame consists of frame alignment mechanism field (AM), extended overhead field (EOH), basic overhead field (BOH), and payload area in which the OTUC is carried (see clause 8 of [ITU-T G.709.1]). As described in clauses 13.1 and 13.5.5 of [ITU-T G.709.5], each set of four 100G FlexO instance of the FlexO-n is interleaved (on a 10-bit basis) into a FlexO-4 frame that is adapted into a FlexO-4-RS frame signal. m FlexO-4-RS frames carry the FlexO-n. If [n = 4 m], then each 400G frame carry four OTUC. If [n < 4 m], then, some 400G frames carry fewer than four, but at least one OTUC [the last one, two or three 100G FlexO instance(s) being unequipped]. The FlexO-4 to FlexO-4-RS adaptation process consists of FEC parity area addition,

scrambling, alignment markers (AMi) values insertion and RS10 (544,514) FEC parity calculation based on two interleaved RS10 codewords. The resulting FlexO-4-RS signal is distributed on sixteen 28G logical lanes which are bit multiplexed into four FOIC4.4-MFI lanes as per the FOIC4.4-RS interface specifications in clause 13.5.6 of [ITU-T G.709.5]. FEC calculation and lane distribution (in group of 10 bits) follow the same processes as specified in clause 119 of [b-IEEE 802.3] for 400GBASE-R interface. At the sink, the n OTUC that are demapped from the m FOIC4.4-RS interfaces are aligned and deskewed per $OTUCn_i$ group signal to retrieve the original $OTUCn_i$ signal(s). At the ODSP sink, the demapped $OTUCn_i$ signals could be crunched (removing unavailable tributary slots) prior to optical transmission. At the framer sink, the receive line pre-FEC LD status bit (if present) is extracted from the FlexO overhead area.

The bit rates of the FOIC4.4-MFI are specified in [ITU-T G.709.5] for FOIC4.4-RS and indicated in Tables 10-2.

Table 10-2 – Bit rates of FlexO-4-RS-m and FOIC4.4-MFI

FOI type	FOI nominal bit rate	FOI bit-rate tolerance
FlexO-4-RS-m	m × 4 × 256/241 × 239/226 × 99 532 800 kbit/s	±20 ppm
FOIC4.4-MFI	4 × 256/241 × 239/226 × 99 532 800 kbit/s	±20 ppm
FOIC4.4-MFI lane	256/241 × 239/226 × 99 532 800 kbit/s	±20 ppm
NOTE – The nominal FOIC4.4-MFI lane bit rate is approximately: 111 809 474.446 kbit/s.		

10.3 FOIC1e.1-MFI structure

As shown in Figures 7-1 and 10-4 of [ITU-T G.709.1], one or more [y_i × 100G] Ethernet client signals ($y_i \geq 1$ and $\sum y_i = n$), can be mapped over a FlexO-ne signal structure composed of n Ethernet optimized 100G FlexO instances. The FlexO-ne can then be distributed in m [x × 100G] FlexO-xe frame signals ($x \geq 1$, and $[m \times x] \leq n$), further adapted and carried over m FlexO-xe-<int> optical interfaces. For FlexO-xe-<int> optical interfaces specified in [ITU-T G.709.6], the value of m always equals 1. FlexO-ne could also be distributed and adapted in m [x × 100G] FlexO-xe-RS frame signals ($x \geq 1$, and $[m \times x] \leq n$) carried over m FOICxe.k-RS-MFI electrical interfaces, with $m \geq 1$. When m > 1, then a deskew process across the m FlexO-xe signals must be implemented in the MFI sink function.

For FlexO-xe-<int> regenerator applications, two line side optical modules could be connected through their host interfaces over x 106G electrical lanes to carry a FlexO-xe client signal. The FlexO-xe frame signal can be distributed into x FlexO-1e frames, further adapted into x FlexO-1e-RS frame signals. Each FlexO-1e-RS is then adapted into a FOIC1e.1-RS lane carried over single electrical lane FOIC1e.1-MFI interface.

Figure 10-3a provides such FlexO regenerator application example of a FlexO-xe signal carried over x FOIC1e.1-RS MFIs.

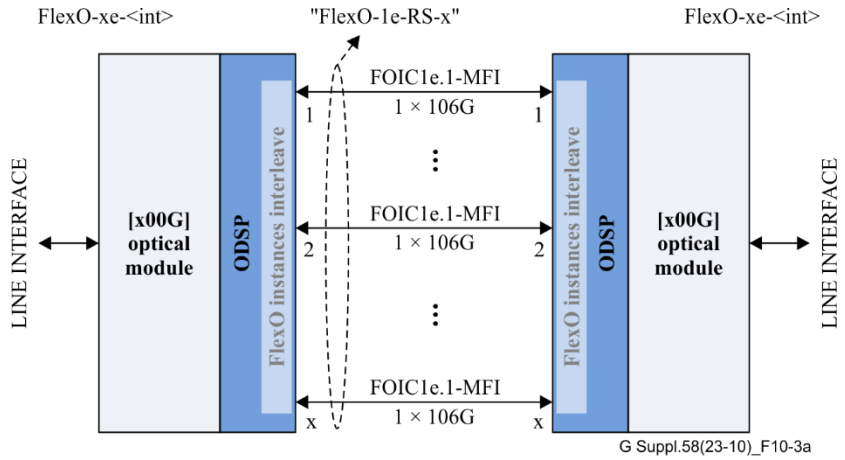
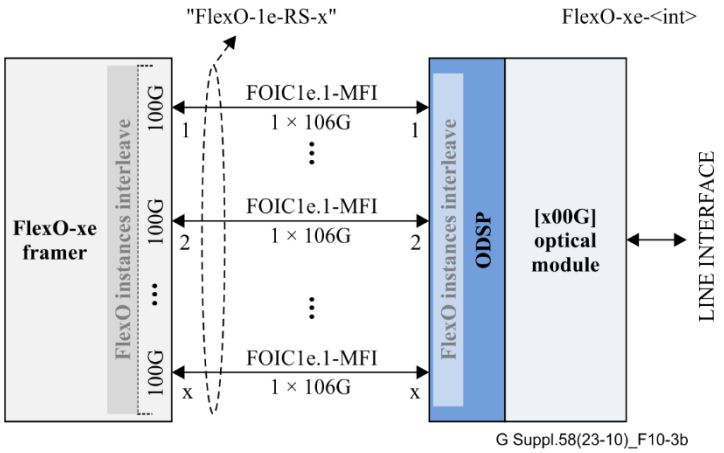


Figure 10-3a – First example application of FOIC1e.1-MFI interface

After receive line side FEC termination and FlexO regenerator overhead sink processing (using extracted FlexO extended overhead fields), at the MFI source the FlexO-xe frame signal is z-bit deinterleaved into x Ethernet optimized 100G FlexO instances (e.g., z = 10 or 128 depending on the type of FlexO-x-<int> line interface). Each 100G instance corresponds to a FlexO-1e frame and consists of frame alignment mechanism field (AM), extended overhead field (EOH), basic overhead field (BOH), and payload area in which the Ethernet client is carried (see clause 8 of [ITU-T G.709.1]). Then each FlexO-1e frame is adapted into a FlexO-1e-RS frame, reusing FlexO-1-RS format specified in clause 11 of [ITU-T G.709.5]. FlexO-1e to FlexO-1e-RS adaptation process consists of RS FEC parity area addition, frame synchronous scrambling, alignment markers insertion (AMi) and RS10 FEC [RS10(544,514)] parity computation (see clauses 11.3 and 11.4 of [ITU-T G.709.5]). Each resulting FlexO-1e-RS frame is distributed (in groups of 10 bits) on four 26G logical lanes using the FOIC1.4-RS lane format specified in clause 11.5.1 of [ITU-T G.709.5]. The 106G FOIC1e.1-RS lane is formed by simple bit-multiplexing of all four 26G logical lanes from the same FlexO-1e-RS, and then carried over single lane FOIC1e.1-MFI electrical interface. Note that the received line pre-FEC LD is processed as specified in clause 9.3.3.2.2 of [ITU-T G.709.1] and forwarded through the MFI in bit 8 of FlexO EOH RSTAT field.

At the sink, the bits from each individual 106G FOIC1e.1-MFI lane are deinterleaved into four 26G logical lanes. Each logical lane is identified within a FOIC1e.1-MFI interface according to its AMi specific pattern (UMx and UPx values). The sink must be able to accept the four 26G logical lanes in any position, and in addition to 26G logical lane alignment and deskew, proceed to reorder these four 26G logical lanes prior to reassembly into a FlexO-1e-RS frame. Note that the interchanging and reordering of 106G FOIC1e.1-MFI electrical lanes is currently not defined and as such not supported. After FEC termination and descrambling of the FlexO-1e-RS frame, the resulting x FlexO-1e frames are deskewed and z-bit interleaved (e.g., z = 10 or 128 depending on the type of FlexO-xe-<int> line interface) into a FlexO-xe signal towards the transmit line interface. FlexO regenerator overhead source processing is performed and Line FEC is inserted towards the remaining transmit optical line side processing functions.

In Figure 10-3b second application example, x FOIC1e.1-MFIs carrying a FlexO-xe signal could be used to connect an x00G FlexO-xe framer with an ODSP device and line side optical module over x 106G electrical lanes ("FlexO-1e-RS-x").



Framer with x FOIC1e.1-MFI interfaces connected through CEI-106G electrical lanes with [x00G] ODSP/optical module (x ≥ 1)

Figure 10-3b – Second example application of FOIC1e.1-MFI interface

At the framer source and per the mapping specifications in clauses 10.2 of [ITU-T G.709.1], N y_i00G Ethernet client signal ($y_i \geq 1$ and $\sum y_i \leq x$) are mapped into a FlexO-xe structure (i.e., n = x). Then FlexO-xe frame is adapted and distributed over x single-lane FOIC1e.1-MFI electrical interfaces as described above for the first application example. At the framer sink the adaption from x FOIC1e.1-MFI lane to FlexO-xe also follows the same process as described above. Then FlexO-xe frame is fully terminated and the N y_i00G Ethernet client signals are demapped.

At both ODSP MFI sink and source functions, the adaptation from each FOIC1e.1-MFI to/from four 26G logical lanes is performed as described above. Depending on the application, the 26G logical lanes and RS FEC may be terminated or carried transparently. This would correspond to different levels of transparency and processing within the module, for segmented vs. concatenated or transparent FEC. When the RS FEC is terminated, FlexO basic overhead may be processed or carried transparently within the ODSP, depending on whether the framer fully or partially terminates these overhead fields. In this case FlexO extended overhead may typically be terminated in the ODSP and receive line pre-FEC LD could be processed as specified in clause 9.3.3.2.2 of [ITU-T G.709.1] and forwarded to the framer through the MFI in bit 8 of FlexO EOH RSTAT field.

The bit rates of FlexO-xe instance and frame are specified in [ITU-T G.709.1] and the bit rates of FOIC1e.1-MFI are indicated in Table 10-3.

Table 10-3 – Bit rates of FlexO-1e-RS-x and FOIC1e.1-MFI

FOI type	**FOI nominal bit rate** (kbit/s)	**FOI bit-rate tolerance** (ppm)
FlexO-1e-RS-x	x × 1445/1624 × 766 × 156 250	±20
FOIC1e.1-MFI	1 × 1445/1624 × 766 × 156 250	±20
FOIC1e.1-MFI lane	1445/1624 × 766 × 156 250	±20
NOTE – The nominal FOIC1e.1-MFI lane bit rate is approximately: 106 495 343.288 kbit/s.		

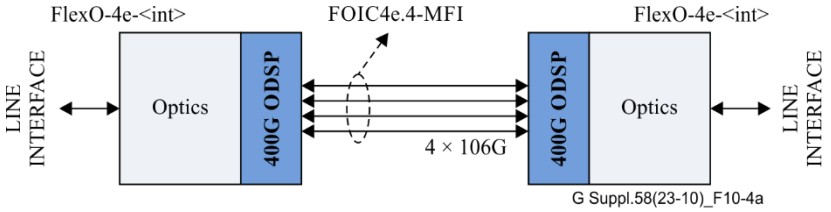
10.4 FOIC4e.4-MFI structure

As shown in Figures 7-1 and 10-4 of [ITU-T G.709.1], one or more [y_i × 100G] Ethernet client signals ($y_i \geq 1$ and $\sum y_i = n$), can be mapped over a FlexO-ne signal structure composed of n Ethernet optimized 100G FlexO instances. The FlexO-ne can then be distributed into m [x × 100G] FlexO-xe frame signals (x ≥ 1, and [m × x] ≤ n), further adapted and carried over m FlexO-xe-<int> optical interfaces. For FlexO-xe-<int> optical interfaces specified in [ITU-T G.709.6], the value of m always equals 1. FlexO-ne could also be distributed and adapted in m [x×100G] FlexO-xe-RS frame signals

(x ≥ 1, and [m × x] ≤ n) carried over m FOICxe.k-RS-MFI electrical interfaces, with m ≥ 1. When m > 1, then a deskew process across the m FlexO-xe signals must be implemented in the MFI sink function.

For FlexO-xe-<int> regenerator applications, two line side optical modules could be connected through their host interfaces over [4 × m] 106G electrical lanes to carry a FlexO-xe client signal (4 × m ≥ x). The FlexO-xe frame signal can be distributed into m FlexO-4e frames, further adapted into m FlexO-4e-RS frame signals. Each FlexO-4e-RS is then adapted into four-lane FOIC4e.4-RS structure carried over four electrical lanes FOIC4e.4-MFI interface.

Figure 10-4a provides a 400G FlexO regenerator application example with a FlexO-4e signal carried over one FOIC4e.4-MFI.



Two [400G] optical modules/ODSP connected through FOIC4e.4-MFI interface on host using 4 × CEI-106G electrical lanes

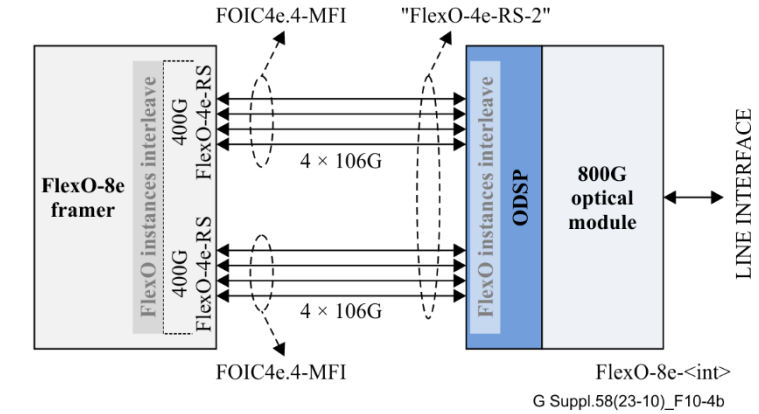
Figure 10-4a – First example application of FOIC4e.4-MFI interface

After receive line side FEC termination and FlexO regenerator overhead sink processing (using extracted FlexO extended overhead fields), at the MFI source the FlexO-xe frame signal is z-bit deinterleaved into x Ethernet optimized 100G FlexO instances (e.g., z = 10 or 128 depending on the type of FlexO-x-<fec-<mod>> line interface). Each set of four FlexO instances are 10-bit interleaved into a FlexO-4e frame, resulting in m FlexO-4e frames with m ≥ [4 × x]. In the case of less than four FlexO frame instances from FlexO-xe can be interleaved into a FlexO-4e (e.g., if x is not a multiple of 4), the last instances of the FlexO-4e are unequipped. Each 100G instance consists of frame alignment mechanism field (AM), extended overhead field (EOH), basic overhead field (BOH), and payload area in which the Ethernet client is carried (see clause 8 of [ITU-T G.709.1]). Then each FlexO-4e frame is adapted into a FlexO-4e-RS frame, reusing FlexO-4-RS format specified in clause 13 of [ITU-T G.709.5]. FlexO-4e to FlexO-4e-RS adaptation process consists of RS FEC parity area addition, frame synchronous scrambling, alignment markers (AMi) insertion and RS10 FEC [RS10(544,514)] parity computation (see clauses 13.3 and 13.4 of [ITU-T G.709.5]) based on two interleaved RS10 codewords. Each resulting FlexO-4e-RS frame is distributed on sixteen 26G logical lanes as per the 400G FOIC4.k-RS interface specifications in clause 13.5 of [ITU-T G.709.5]. FEC calculation and 26G logical lanes distribution (in groups of 10 bits) follow the same processes as specified in clause 119 of [b-IEEE 802.3] for 400GBASE-R interface. Each 106G lane of FOIC4e.4-MFI using FOIC4.4-RS lane format is formed by simple bit-multiplexing of four 26G logical lanes from the same FlexO-4e-RS. Note that the receive line pre-FEC LD is processed as specified in clause 9.3.3.2.2 of [ITU-T G.709.1] and forwarded through the MFI in bit 8 of FlexO EOH RSTAT field.

At the sink, the bits from each individual 106G FOIC4e.4-MFI lane are deinterleaved into four 26G logical lanes. Each 26G logical lane is identified within a FOIC4e.4-MFI interface according to its AMi specific pattern (UMx and UPx values). The sink must be able to accept the sixteen 26G logical lanes in any position, and in addition to 26G logical lane alignment and deskew, proceed to reorder these sixteen 26G logical lanes prior to reassembly into a FlexO-4e-RS frame. Note that the interchanging and reordering of 106G electrical lanes from different FOIC4e.4-MFI interfaces is currently not defined and as such not supported. After FEC termination and descrambling of the FlexO-4e-RS frame, the resulting m FlexO-4e frames are deskewed and 10-bit deinterleaved into x 100G FlexO instances. The FlexO instances are then z-bit interleaved to retrieve the original FlexO-

xe signal (e.g., z = 10 or 128 depending on the type of FlexO-x-<int> line interface). FlexO regenerator overhead source processing is performed and Line FEC is inserted towards the transmit optical line side functions.

In Figure 10-4b second application example with x = 8 and m = 2, two FOIC4e.4-MFIs carrying a FlexO-8e signal (m = ceiling[x/4]) could be used to connect an 800G Ethernet optimized FlexO framer over eight 106G electrical lanes with an ODSP device and FlexO-8e-<int> line side optical module.



Single 800G optical module/ODSP with 2 FOIC4e.4-RS interfaces on host using 8 × CEI-106G electrical lanes connected with external framer

Figure 10-4b – Second example application of FOIC4e.4-MFI interface

At the framer source and per the mapping specifications in clause 10.2 of [ITU-T G.709.1], N y_i00G Ethernet client signal ($y_i \geq 1$ and $\sum y_i \leq x$) are mapped into a FlexO-xe structure. Then FlexO-xe frame is adapted and distributed over m four-lane FOIC4e.4-MFI electrical interfaces ($m \geq 4 \times x$) as described above for the first application example. At the framer sink the adaptation from m FOIC4e.4-MFI lane to FlexO-xe also follows the same process as described above. Then FlexO-xe frame is fully terminated and the N y_i00G Ethernet client signals are demapped.

At both the ODSP MFI sink and source functions, the adaptation from each FOIC4e.4-MFI to/from sixteen 26G logical lanes is performed as described above. Depending on the application, the 26G logical lanes and RS FEC may be terminated or carried transparently. This would correspond to different levels of transparency and processing within the module, for segmented vs. concatenated or transparent FEC. When the RS FEC is terminated, FlexO basic overhead may be processed or carried transparently within the ODSP, depending on whether the framer fully or partially terminates these overhead fields. In this case FlexO extended overhead may typically be terminated in the ODSP and receive line pre-FEC LD could be processed as specified in clause 9.3.3.2.2 of [ITU-T G.709.1] and forwarded to the framer through the MFI in bit 8 of FlexO EOH RSTAT field.

The bit rates of FlexO-xe instance and frame are specified in [ITU-T G.709.1] and the bit rates of FOIC4e.4-MFI are indicated in Table 10-4, with m = ceiling[x/2].

Table 10-4 – Bit rates of FlexO-4e-RS-m and FOIC4e.4-MFI

FOI type	**FOI nominal bit rate** (kbit/s)	**FOI bit-rate tolerance** (ppm)
FlexO-4e-RS-m	m × 4 × 1445/1624 × 766 × 156 250	±20
FOIC4e.4-MFI	4 × 1445/1624 × 766 × 156 250	±20
FOIC4e.4-MFI lane	1445/1624 × 766 × 156 250	±20
NOTE – The nominal FOIC4e.4-MFI lane bit rate is approximately: 106 495 343.288 kbit/s.		

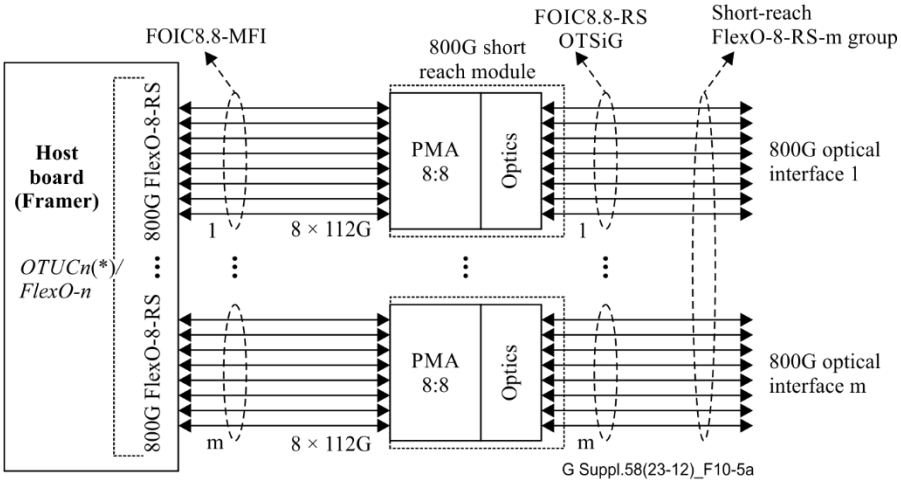
10.5 FOIC8.8-MFI structure

As shown in Figure 7-1 and 10-1 or 10-9 of [ITU-T G.709.1], one or more OTUCn_i signal ($n_i \geq 1$ and $\sum n_i = n$), full-rate or sub-rated (with some OPUCn_i tributary slots marked as unavailable), is mapped over a FlexO-n signal structure composed of n 100G FlexO instances, each carrying an OTUC instance. The FlexO-n structure can be distributed into m FlexO-8 frame structures that will be further adapted and carried over m FlexO-8-<int> bonded optical interfaces.

For short-reach FlexO-8-RS-m interface group applications (i.e., <int> = RS) with {x,k} = {8,8} and [8 × m] ≥ n, each FlexO-8-RS interface signal (carrying up to eight OTUC) is distributed and transported over eight 112G physical lanes FOIC8.8-RS interface per Figure 7-1 of [ITU-T G.709.5]. This provides interoperable modular short-reach OTN interfaces for B100G OTUCn and FlexO-n (n ≥ 1) transport signals, by bonding m 800G optical interfaces or optical lane groups.

Pluggable modules with 100G per lane developed for Ethernet 800GBASE-R applications and supporting short-reach FlexO rate (that is ~112 Gbit/s per lane) could be reused for FlexO-8-RS transport and FOIC8.8-RS interface. They have corresponding optical specifications for FlexO-8-RS interfaces with the optical parameters as specified for the PAM4 application codes. These modules have a [*p* × 8] 100G lanes to and from a transmit/receive pair of ITU-T G.652 optical fibres. These pluggable modules may use [*p* × 8] 100G electrical lanes chip-to-module interface (*p* 800GAUI-8, with $p \geq 1$), whose specifications are found in Annex 120G of [b-IEEE 802.3ck]. For these optical modules supporting the FlexO bit rate, *p* FOIC8.8-MFI chip-to-module electrical interfaces could be used, each with FOIC8.8-RS lane structure.

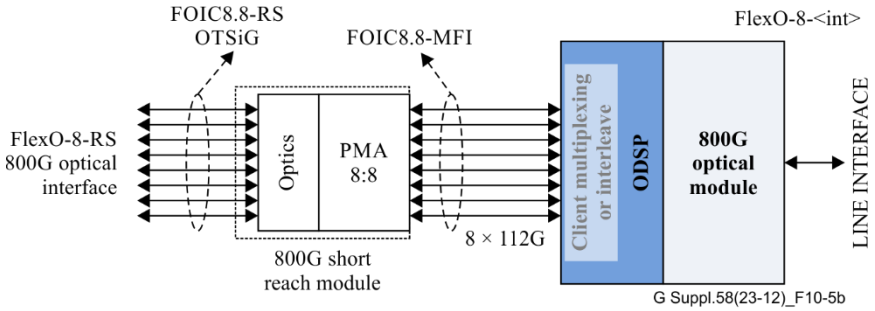
This application of m FOIC8.8-RS bonded interfaces (short-reach FlexO-8-RS-m group) using FOIC8.8-MFI chip-to-module interfaces is illustrated in Figure 10-5a.



Framer with m FOIC8.8-MFI interfaces connected through CEI-112G electrical lanes with m 800G pluggable module (8×m ≥ n)

Figure 10.5a – FOIC8.8-MFI interface main application example

In Figure 10-5b application example, the FOIC8.8-MFI could be used to connect FlexO-8-RS signal between an 800G pluggable optical module and the host side of an 800G ODSP device. Client side and line side could be plesiochronous if the ODSP device supports OTUC8 demapping/mapping from/to FlexO-8 on client side and asynchronous GMP mapping/demapping to/from FlexcO-8 on the line side. Alternatively, the client and line side shall be synchronous in case of FlexO-8 regenerator for single chip transponder applications.

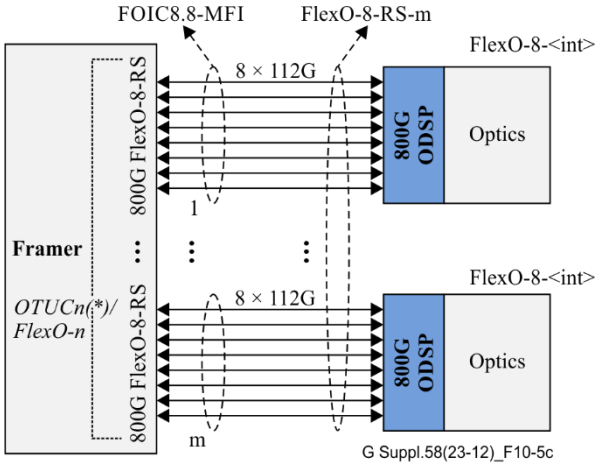


Single 800G optical module/ODSP with two FOIC8.8-RS interfaces on host using 8 × CEI-112G connected with 800G 8-lane pluggable module

Figure 10-5b – Second example application of FOIC8.8-MFI interface

The FOIC8.8-MFI interface using FOIC8.8-RS lane structure could also be used to connect beyond 400G OTN framer with one or more optical line DSP (ODSP) devices. Such devices may be limited to 800G client granularity on its host side (e.g., one or multiple synchronous 800G MFI interfaces). Depending on the application or type of optical module, the module may be agnostic and fully transparent to the FOIC8.8-RS lane structure or the RS FEC may be terminated. In the latter case the FlexO-8-RS may be fully terminated (the OTUC instances are mapped/demapped to/from FlexO-8) or partially terminated (RS FEC and part of FlexO overhead is terminated). For partial termination, different FlexO overhead fields may be terminated or carried transparently in the ODSP.

When FlexO basic overhead is not carried transparently in the ODSP, see clause 9.1 for this type of application; in this case, the receive ODSP detects the receive line pre-FEC Local Degrade (LD) and optionally forwards the LD status bit to the receive framer device through the MFI, as carried in bit 8 of the BOH STAT field of the first 100G FlexO instance overhead of the FlexO-8-RS frame (see Figure 9-2d). Alternatively, when FlexO extended overhead (EOH) is not carried transparently, the receive line pre-FEC LD could be processed as specified in clause 9.3.3.2.2 of [ITU-T G.709.1] and forwarded through the MFI in bit 8 of the RSTAT field of all eight FlexO instance EOH. This third application example is illustrated in Figure 10-5c with the example of 800G ODSP/optical modules.



m FOIC8.8-RS interfaces using CEI-112G
Framer connected with m ODSPs (8 × m ≥ n)
(*) *NOTE – Some OPUCn tributary slots may be marked as unavailable*

Figure 10-5c – Third example application of FOIC8.8-MFI interfaces

Each 112G lane of the FOIC8.8-MFI is formed by bit-multiplexing of four 28G logical lanes from the two 400G flows (flow 0 and flow 1) of the same FlexO-4-RS, following the processing described in clause 14.5.1 of [ITU-T G.709.5] for FOIC8.8-RS lane format. At the sink, the bits from each

individual 112G FOIC8.8-MFI lane are deinterleaved into four 28G logical lanes. The sink could identify each of the thirty-two 28G logical lanes within a FOIC8.8-MFI interface according to its alignment marker specific pattern (unique UMx and UPx values).

When the RS FEC is terminated, the sink must support the thirty-two 28G logical lanes in any position, and in addition to 28G logical lanes alignment and deskew, proceed to reorder these thirty-two 28G logical lanes prior to reassembly into two 400G flows (flow 0 and flow 1) of the FlexO-8-RS frame.

For full termination of the FOIC8.8-MFI, and per the mapping specifications in clause 10.1 or 10.3 of [ITU-T G.709.1] one or more OTUCn_i signals are split into n times OTUC ($n_i \geq 1$ and $\sum n_i = n$), and each OTUC is mapped into an individual 100G FlexO instance of a FlexO-n structure. Each 100G FlexO instance frame consists of frame alignment mechanism field (AM), extended overhead field (EOH), basic overhead field (BOH), and payload area in which the OTUC is carried (see clause 8 of [ITU-T G.709.1]). As described in clauses 14.1 and 14.5.5 of [ITU-T G.709.5], each set of eight 100G FlexO instance of the FlexO-n is interleaved (on a 10-bit basis) into a FlexO-8 frame that is adapted into a FlexO-8-RS frame format after FEC parity area insertion. m FlexO-8-RS frames carry the FlexO-n. If [$n = 8 \times m$], then each 800G frame carry eight OTUC. If [$n < 8 \times m$], then, some 800G frames carry fewer than eight, but at least one OTUC [the last one, two, three, …, or seven 100G FlexO instance(s) possibly being unequipped].

The FlexO-8-RS is then deinterleaved 40-bit at a time into two FlexO-4-RS flows, with the first 400G flow [0] carrying 100G FlexO instances 1 to 4 and the second 400G flow [1] carrying 100G FlexO instances 5 to 8. Then the processing of each 400G flow consists of scrambling, alignment markers (AMi) values insertion and RS10 (544,514) FEC parity calculation based on two interleaved RS10 codewords as specified in clauses 14.3 and 14.4 of [ITU-T G.709.5]. Each resulting 400G flow is distributed on sixteen 28G logical lanes on a 10-bit basis, resulting into thirty-two 28G logical lanes, per 800G FOIC8.k-RS interface specifications in clause 14.5 of [ITU-T G.709.5], which are then bit multiplexed into the eight 112G FOIC8.8-MFI lanes. FEC calculation, 28G logical lanes distribution (in group of 10 bits), and 28G logical lanes bit-multiplexing into eight 112G physical lanes follow the same processes as specified in clause 172 of [b-IEEE 802.3df] for 800GBASE-R interface. At the sink, the n OTUC that are demapped from the m FOIC8.8-RS interfaces are aligned and deskewed per OTUCn_i group signal to retrieve the original OTUCn_i signal(s). At the ODSP sink, the demapped OTUCn_i signals could be crunched (removing unavailable tributary slots) prior to optical transmission. At the framer sink, the receive line pre-FEC LD status bit (if present) is extracted from the FlexO overhead area (either from bit 8 of STAT BOH byte or RSTAT EOH byte).

The bit rates of the FOIC8.8-MFI are specified in [ITU-T G.709.5] for FOIC8.8-RS and indicated in Tables 10-5.

Table 10-5 – Bit rates of FlexO-8-RS-m and FOIC8.8-MFI

FOI type	FOI nominal bit rate	FOI bit-rate tolerance
FlexO-8-RS-m	m × 8 × 256/241 × 239/226 × 99 532 800 kbit/s	±20 ppm
FOIC8.8-MFI	8 × 256/241 × 239/226 × 99 532 800 kbit/s	±20 ppm
FOIC8.8-MFI lane	256/241 × 239/226 × 99 532 800 kbit/s	±20 ppm
NOTE – The nominal FOIC8.8-MFI lane bit rate is approximately: 111 809 474.446 kbit/s.		

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[b-IEEE 802.3] IEEE 802.3-2022, *IEEE Standard for Ethernet*.

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