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SERIES G: TRANSMISSION SYSTEMS AND MEDIA, DIGITAL SYSTEMS AND NETWORKS

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# Optical transport network module framer interfaces

ITU-T G-series Recommendations – Supplement 58

ITU-T

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## Supplement 58 to ITU-T G-series Recommendations

# Optical transport network module framer interfaces


### Summary

Supplement 58 to ITU-T G-series Recommendations describes several interoperable component-to-component multilane interfaces (across different vendors) to connect an optical module [with or without a digital signal processor (DSP)] to a framer device in a vendor's equipment supporting 40G, 100G or beyond 100G optical transport network (OTN) interfaces.

Only the structure of the 11G, 28G or 56G physical lanes of the different OTN module framer interface (MFI) examples is provided in this Supplement. For their electrical characteristics, the OIF-CEI Implementation Agreement (IA) specifications can be used.

This Supplement relates to Recommendation ITU-T G.709/Y.1331.


### History

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### Keywords

FOIC, Framer, interface, module, MFI, OTL, OTN.


* To access the Recommendation, type the URL http://handle.itu.int/ in the address field of your web browser, followed by the Recommendation's unique ID. For example, http://handle.itu.int/11.1002/1000/11830-en.

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# Supplement 58 to ITU-T G-series Recommendations

## Optical transport network module framer interfaces

## 1 Scope

This Supplement describes multilane interfaces between an optical transport network (OTN) framer device and an optical module with or without a digital signal processor (DSP) (module framer interface). The module framer interfaces (MFIs) described in this Supplement carry optical transport unit k (OTUk; k = 3, 4) or optical transport unit Cn (OTUCn) signals. Electrical parameters for these interfaces can use specifications provided in the relevant clauses of OIF-CEI Implementation Agreement (IA) specifications.

## 2 References


[ITU-T G.652] Recommendation ITU-T G.652 (2016), *Characteristics of a single-mode optical fibre and cable*.

[ITU-T G.695] Recommendation ITU-T G.695 (2018), *Optical interfaces for coarse wavelength division multiplexing applications*.

[ITU-T G.709] Recommendation ITU-T G.709/Y.1331 (2016), *Interfaces for the optical transport network*.

[ITU-T G.709.1] Recommendation ITU-T G.709.1/Y.1331.1 (2018), *Flexible OTN short-reach interface*.

[ITU-T G.959.1] Recommendation ITU-T G.959.1 (2018), *Optical transport network physical layer interfaces*.


## 3 Definitions

None.

## 4 Abbreviations and acronyms

This Supplement uses the following abbreviations and acronyms:

AM Alignment Marker

DSP Digital Signal Processor

FCC FlexO Communications Channel

FEC Forward Error Correction

FlexO Flexible Optical transport network

FlexO-m group of m bonded short-reach FlexO-SR interfaces that carry an OTUCn

FOIC FlexO-SR Interface

IA Implementation Agreement

LD Local Degrade

LLM Logical Lane Marker

MFAS Multi-Frame Alignment Signal

MFI Module Framer Interface

| | |
|---|---|
| ODSP | Optical line DSP |
| OH | Overhead area |
| OSMC | OTN Synchronization Messaging Channel |
| OTL | Optical Transport Lane |
| OTN | Optical Transport Network |
| OTUCn | Optical Transport Unit Cn |
| OTUk | Optical Transport Unit k |
| PAD | pad area |
| PAM4 | Pulse Amplitude Modulation, four-level |
| RS | Reed-Solomon |
| WDM | Wavelength Division Multiplexing |

## 5 Conventions

Transmission order: The order of transmission of information in all the figures in this supplement is first from left to right and then from top to bottom. Within each byte, the most significant bit is transmitted first. The most significant bit (bit 1) is illustrated at the left in all the figures.

## 6 Introduction

This Supplement begins with some examples of first generation MFIs for OTU3 and OTU4 signals carried over multiple 11G electrical lanes (using OTL3.4 and OTL4.10 structures, respectively).

Then this Supplement describes some examples of second generation MFIs for OTU4 and OTUCn signals carried over multiple 28G electrical lanes (using OTL4.4, OTLC.4, FOIC1.4, FOIC2.8 or FOIC4.16 structures, respectively). Note that in the case of an OTUCn signal, n OTLC.4 or m FOICx.k interface structures are used.

Finally, this Supplement describes some examples of third generation MFIs for OTUCn signals carried over multiple 56G electrical lanes (using FOIC1.2, FOIC2.4 or FOIC4.8 structures, respectively). Note that m FOICx.k interfaces (FlexO-m group) are used to carry an OTUCn signal.

Users of this Supplement should not assume that possible MFIs are limited to the ones provided in clauses 7, 8 and 9.

## 7 Signal formats and rates carried over 11G electrical lanes

This clause describes some MFI structures using 11G physical lanes in order to carry 40G OTU3 or 100G OTU4 signals. The electrical characteristics of each 11G physical lane may comply with [b-OIF-CEI IA] CEI-11G-*x*R specifications.

### 7.1 OTL3.4 structure

The original purpose of the OTL3.4 interface, as defined in clause 8.1 and Annex C of [ITU-T G.709], was to enable the re-use of pluggable modules developed for Ethernet 40GBASE-R applications. Modules developed for b-IEEE 802.3 40GBASE-LR4 and 40GBASE-ER4 can have corresponding optical specifications for OTU3 interfaces with application codes C4S1-2D1 and C4L1-2D1, respectively, in [ITU-T G.695]. These modules have a four-lane wavelength division multiplexing (WDM) interface to and from a transmit/receive pair of ITU-T G.652 optical fibres.

These pluggable modules use a four-lane electrical chip-to-module interface (XLAUI), whose specification is found in Annex 83B of [b-IEEE 802.3]. These modules include a simple retimer. This application of the OTL3.4 interface is found in Figure 7-1.

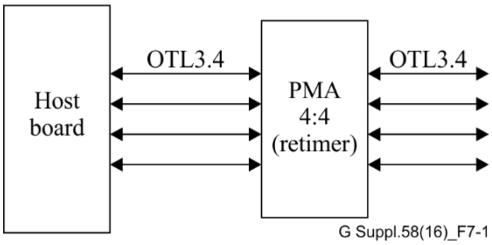



**Figure 7-1 – Illustration of the application of an OTL3.4 interface**

Another application example of the OTL3.4 interface is to connect a 40G OTN framer and optical line DSP (ODSP) devices in order to carry an OTU3 signal.

The bit rates of the OTL3.4 lanes are specified in [ITU-T G.709] and indicated in Table 7-1.

**Table 7-1 – Bit rates of OTL3.4**

| Optical transport lane (OTL) type | OTL nominal bit rate | OTL bit-rate tolerance |
|---|---|---|
| OTL3.4 | 4 × 255/236 × 9 953 280 kbit/s | ±20 ppm |
| OTL3.4 lane | 255/236 × 9 953 280 kbit/s | ±20 ppm |
| NOTE – The nominal OTL3.4 lane bit rate is approximately: 10 754 603.390 kbit/s. | | |

## 7.2 OTL4.10 structure

The original purpose of the OTL4.10 interface, as defined in clause 8.1 and Annex C of [ITU-T G.709], was to enable the re-use of first generation pluggable modules developed for Ethernet 100GBASE-R applications. Modules developed for [b-IEEE 802.3] specified 100GBASE-LR4 and 100GBASE-ER4. They have corresponding optical specifications for OTU4 interfaces with the optical parameters as specified for the application codes 4I1-9D1F and 4L1-9C1F, respectively, in [ITU-T G.959.1]. Non-IEEE specified optical interfaces include ITU-T G.695 application code C4S1-9D1F and ITU-T G.959.1 application code 4L1-9D1F. These modules have a four-lane WDM interface to and from a transmit/receive pair of ITU-T G.652 optical fibres.

These first generation modules connect to the host board via a 10-lane electrical interface. The conversion between 10 and four lanes is performed using a 100GBASE-R b-IEEE 802.3 PMA sublayer as specified in clause 83 of [b-IEEE 802.3]. The specification of the 10-lane electrical chip-to-module interface (CAUI-10) is found in Annex 83B of [b-IEEE 802.3]. The application of the OTL4.10 interface is illustrated in Figure 7-2.

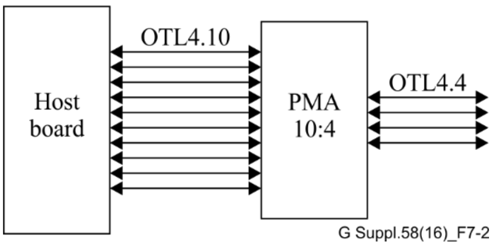



**Figure 7-2 – Illustration of the original application of an OTL4.10 interface**

Another application example of the OTL4.10 interface is to connect first generation 100G OTN framers with ODSP devices in order to carry an OTU4 signal.

Each OTL4.10 lane carries two bit-multiplexed logical lanes of an OTU4 as described in Annex C of [ITU-T G.709]. The logical lane format has been chosen so that the b-IEEE 802.3 10:4 PMA (gearbox) will convert the OTU4 signal between a format of 10 lanes of OTL4.10 and four lanes of OTL4.4. Each OTL4.4 lane carries five bit-multiplexed logical lanes of an OTU4 as described in Annex C of [ITU-T G.709].

The bit rate of an OTL4.10 lane is specified in Table 7-2.

**Table 7-2 – Bit rates of OTL4.10**

| OTL type | OTL nominal bit rate | OTL bit-rate tolerance |
|---|---|---|
| OTL4.10 | 10 × 255/227 × 9 953 280 kbit/s | ±20 ppm |
| OTL4.10 lane | 255/227 × 9 953 280 kbit/s | ±20 ppm |
| NOTE – The nominal OTL4.10 lane bit rate is approximately: 11 180 997.357 kbit/s. | | |

## 8 Signal formats and rates carried over 28G electrical lanes

This clause describes some MFI structures using 28G physical lanes in order to carry 100G OTU4 or B100G OTUCn signals. The electrical characteristics of each 28G physical lane may comply with [b-OIF-CEI IA] CEI-28G-*x*R specifications.

### 8.1 OTL4.4 structure

The original purpose of the OTL4.4 interface, as defined in this clause and Annex C of [ITU-T G.709], was to enable the re-use of second (and beyond) generation pluggable modules developed for Ethernet 100GBASE-R applications. Modules developed for [b-IEEE 802.3] specified 100GBASE-LR4 and 100GBASE-ER4. They have corresponding optical specifications for OTU4 interfaces with the optical parameters as specified for the application codes 4I1-9D1F and 4L1-9C1F, respectively, in [ITU-T G.959.1]. Non-IEEE specified optical interfaces include [ITU-T G.695] application code C4S1-9D1F and ITU-T G.959.1 application code 4L1-9D1F. These modules have a four-lane WDM interface to and from a transmit/receive pair of ITU-T G.652 optical fibres.

Most second generation (and beyond) pluggable modules use a four-lane electrical chip-to-module interface (CAUI-4), whose specification is found in Annex 83E of [b-IEEE 802.3]. These modules include a simple retimer (as opposed to the 10:4 gearbox found in first generation modules). This application of the OTL4.4 interface is illustrated in Figure 8-1.

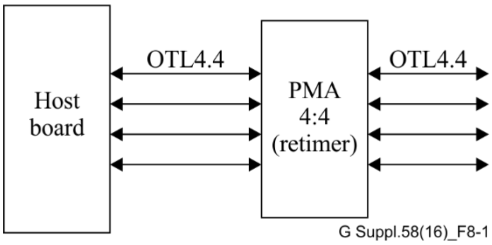



**Figure 8-1 – Illustration of the original application of an OTL4.4 interface**

Another application example of the OTL4.4 interface is to connect second generation multi-100G OTN framers with ODSP devices in order to carry independent OTU4 signals and to connect these framers with emerging line side optical modules.

Each OTL4.4 lane carries five bit-multiplexed logical lanes of an OTU4 as described in Annex C of [ITU-T G.709].

The bit rates of the OTL4.4 are specified in [ITU-T G.709] indicated in Table 8-1.

**Table 8-1 – Bit rates of OTL4.4**

| OTL type | OTL nominal bit rate | OTL bit-rate tolerance |
|---|---|---|
| OTL4.4 | 4 × 255/227 × 24 883 200 kbit/s | ±20 ppm |
| OTL4.4 lane | 255/227 × 24 883 200 kbit/s | ±20 ppm |
| NOTE – The nominal OTL4.4 lane bit rate is approximately: 27 952 493.392 kbit/s. | | |

## 8.2 OTLC.4 structure

In B100G OTN design, the interfaces between the B100G OTN framer and ODSP devices will support OTU4 and OTUCn signals. This interface benefits from a common interface format. The purpose of the OTLC.4 interfaces is to support such a common interface format based on the existing OTL4.4 format. These interfaces carry either four physical lanes of an OTU4 (i.e., OTL4.4) or OTUCn (i.e., OTLC.4). See Figure 8-2.

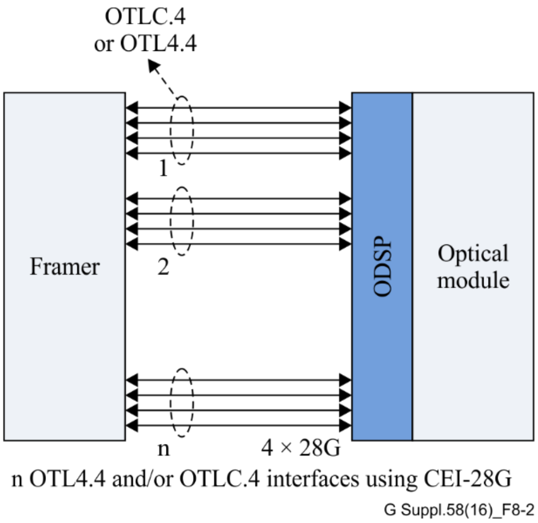



**Figure 8-2 – Example applications of an OTL4.4/OTLC.4 interface**

An OTUCn is split into n times OTUC and each OTUC frame is extended with 256 FEC columns at the end of the frame that contain a Reed-Solomon (RS) (255,239) FEC as specified for the OTUk in Annex A of [ITU-T G.709]. Each OTUC frame with RS (255,239) FEC therefore results in an octet-based block frame structure with four rows and 4 080 columns, that is the same as an OTUk (k = 1,2,3,4) frame structure. This frame structure is scrambled as specified for the OTUk in clause 11.2 of [ITU-T G.709] and split into 20 5G OTLC logical lanes as per 5G OTL4 logical lane specification in Annex C of [ITU-T G.709]. 5G OTLC logical lanes are combined into four OTLC.4 physical lanes as per the OTL4.4 specifications in Annex C of [ITU-T G.709].

The third OA2 byte in each OTUC with RS (255,239) FEC frame is replaced by a logical lane marker (LLM) byte as per the OTL4.4 specifications in Annex C of [ITU-T G.709] to support the reordering of the 5G OTL4 and OTLC logical lanes within the scope of the 20 logical lanes in a 100G OTU4 or OTUC group.

OTL4.4 physical lanes do not support an OTU4 identifier. Due to this, groups of four OTLx.4 (x = 4, C) physical lanes carrying one OTU4 or one OTUC instance have to be connected as a 100G group. Physical lanes within such a 100G group can be interchanged, but physical lanes of different 100G groups must not be interchanged.

The bit rates of an OTLC.4 lane with RS (255,239) FEC are specified in Table 8-2.

**Table 8-2 – Bit rate of OTLCn with RS (255,239) FEC**

| OTL type | OTL nominal bit rate | OTL bit-rate tolerance |
|---|---|---|
| OTLCn | n × 4 × 255/226 × 24 883 200 kbit/s | ±20 ppm |
| OTLC slice | 4 × 255/226 × 24 883 200 kbit/s | ±20 ppm |
| OTLC.4 lane | 255/226 × 24 883 200 kbit/s | ±20 ppm |
| NOTE – The nominal OTLCn, OTLC slice and OTLC.4 lane bit rates are approximately and respectively: n × 112 304 707.965 kbit/s, 112 304 707.965 kbit/s and 28.076 176.991 kbit/s. | | |

## 8.3 FOIC1.4 structure

The original purpose of the n*FOIC1.4 interface (i.e., FlexO-n group), as defined in clause 11 of [ITU-T G.709.1], is to provide an interoperable modular short-reach OTN interface for B100G OTUCn (n ≥ 1) transport signals, by bonding n * 100G standard-rate interfaces.

As the OTUCn is split into n times OTUC, each individual 100G FlexO-SR interface (FOIC; carrying an OTUC) is distributed on four lanes (FOIC1.4) and operates at almost the same interface rate as OTL4.4 (with just −4.46 ppm offset between the two nominal rates).

So, second (and beyond) generation pluggable modules developed for Ethernet 100GBASE-R applications and supporting the OTU4 rate and OTL4.4 interface could be seamlessly reused for 100G FlexO-SR transport and the FOIC1.4 interface. Modules developed for [b-IEEE 802.3] specified 100GBASE-LR4 and 100GBASE-ER4. They have corresponding optical specifications for OTU4 (and so for 100G FlexO-SR) interfaces with the optical parameters as specified for the application codes 4I1-9D1F and 4L1-9C1F, respectively, in [ITU-T G.959.1]. Non-IEEE specified optical interfaces include ITU-T G.695 application code C4S1-9D1F and ITU-T G.959.1 application code 4L1-9D1F. These modules have a four-lane WDM interface to and from a transmit/receive pair of ITU-T G.652 optical fibres.

Most of these pluggable modules use a four-lane electrical chip-to-module interface (CAUI-4), whose specification is found in Annex 83E of [b-IEEE 802.3], and include a simple retimer.

This application of n*FOIC1.4 bonded interfaces (short-reach FlexO-n group) is illustrated in Figure 8-3a.

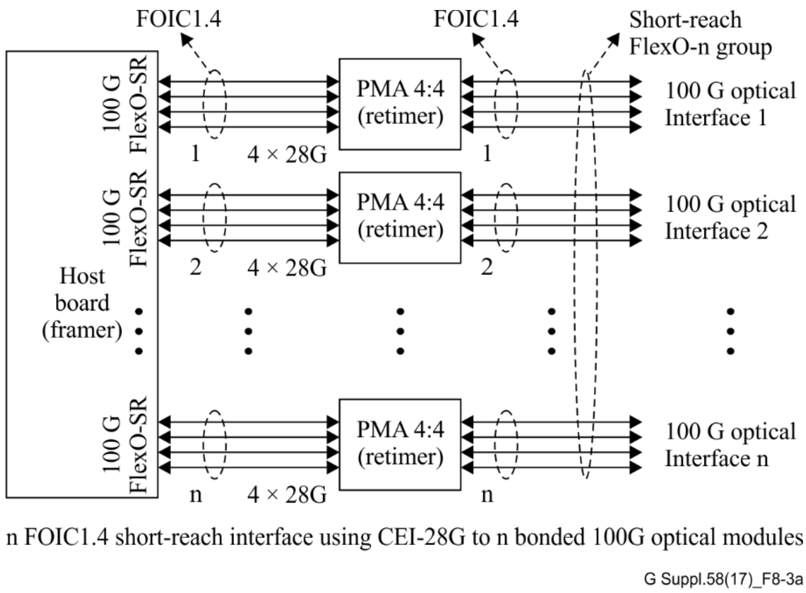



**Figure 8-3a – Original application of a FOIC1.4 interface**

NOTE – The FOIC1.4 interface could also be used similarly to an OTLC.4 interface in order to connect a beyond 100G OTN framer with one or more ODSP devices supporting FlexO interfaces on the host side. One possible advantage for implementers is that the FOIC1.4 lane operates at the same rate as an OTL4.4 lane, so slightly slower than an OTLC.4 lane and with a stronger RS10 FEC. Another advantage is that the bit rate of a FOIC1.4 lane is exactly half the bit rate of a FOIC1.2 lane (the FOIC1.2 lane is obtained by simple bit-interleaving of two FOIC1.4 lanes). Depending on the application, implementers could make use of the FlexO overhead. Although some overhead may become optional, they are generated at the source and may be ignored at the sink (see clause 9.1 for the handling of FlexO overhead for this type of application). This alternate application is illustrated in Figure 8-3b.

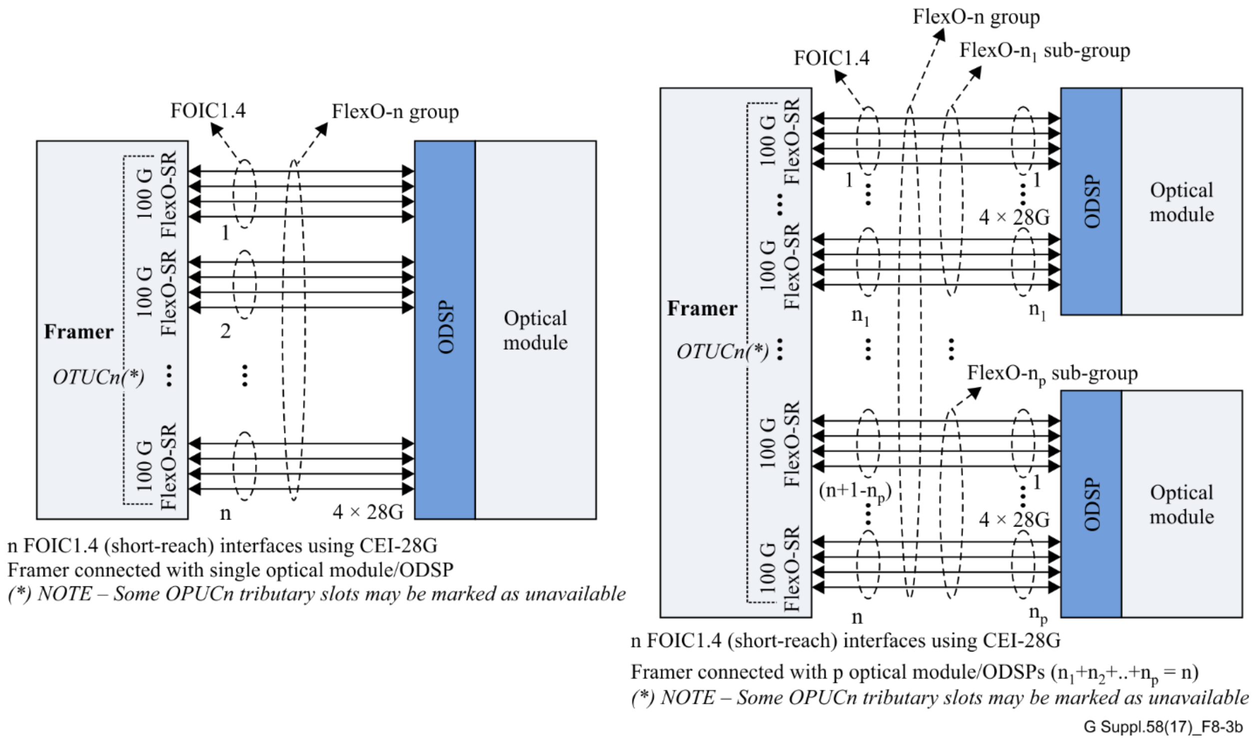



**Figure 8-3b – Alternate application of a FOIC1.4 interface**

The bit rates of the FOIC1.4 specified in [ITU-T G.709.1] are indicated in Table 8-3.

**Table 8-3 – Bit rates of short-reach FlexO-n and FOIC1.4**

| FOIC type | FOIC nominal bit rate | FOIC bit-rate tolerance |
|---|---|---|
| FlexO-n (SR) | n × 4 × 256/241 × 239/226 × 24 883 200 kbit/s | ±20 ppm |
| FOIC1.4 | 4 × 256/241 × 239/226 × 24 883 200 kbit/s | ±20 ppm |
| FOIC1.4 lane | 256/241 × 239/226 × 24 883 200 kbit/s | ±20 ppm |
| NOTE – The nominal FOIC1.4 lane bit rate is approximately: 27 952 368.611 kbit/s. | | |

## 8.4 FOIC2.8 and FOIC4.16 structures

As shown in Figure 7-1 and 10-1 of [ITU-T G.709.1], an OTUCn signal (n ≥ 1), full-rate or sub-rated (with some OPUCn tributary slots marked as unavailable), can be carried over m*FOIC2.8 or m*FOIC4.16 bonded interfaces [short-reach FlexO-m group, with {x,k} = {2,8} or {4,16} respectively]. Each FOIC2.8 interface contains eight physical lanes of a 200G FlexO-SR frame (carrying up to two OTUC). Each FOIC4.16 interface contains 16 physical lanes of a 400G FlexO-SR frame (carrying up to four OTUC).

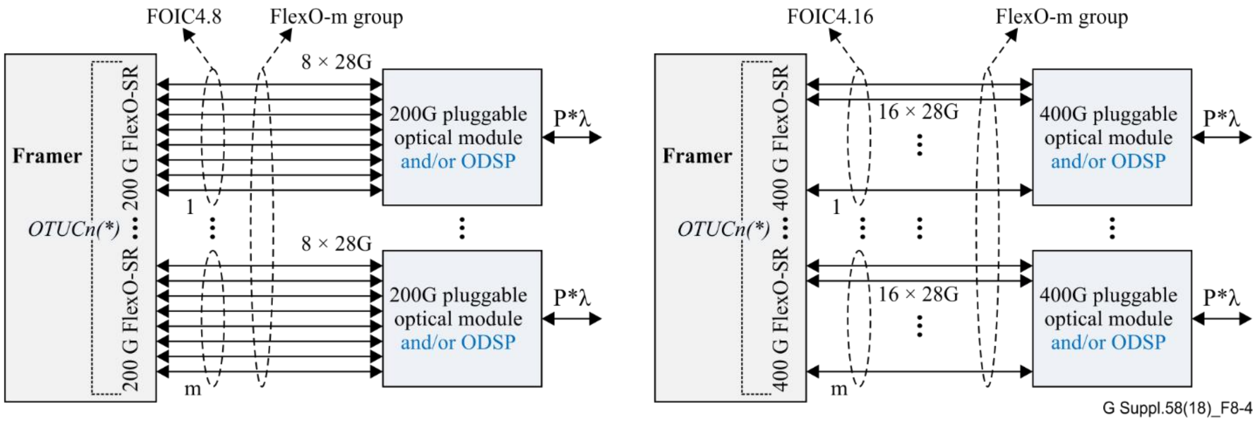
This provides interoperable modular OTN interfaces with short-reach FEC (reusing same KP4 RS10 FEC schemes as 200GBASE-R or 400GBASE-R) for B100G OTUCn (n ≥ 1) transport signals, by bonding m * 200G or m * 400G standard-rate interfaces.

The FOIC2.8 or FOIC4.16 interface could be used in order to connect a beyond 100G OTN framer with one or more 200G or 400G pluggable modules or ODSP devices supporting 28G electrical lanes and FlexO interfaces on the host side. One possible advantage for implementers is that the FEC and lane processing for a 200G FOIC2.8 or 400G FOIC4.16 interface is almost identical to that of a 200GAUI-4 or 400GAUI-8, respectively, thus allowing digital logic supporting both Ethernet and OTN signals to be shared on its host side.

First generation pluggable modules developed for Ethernet 200GBASE-R with eight electrical lanes on the host side, and supporting the 200G FlexO rate and FOIC2.8 host interface (roughly the same bit rate as that of the OTL4.4 per 28G lane with similar digital format to 200GAUI-8) could also be reused for 200G FlexO-SR transport. They have corresponding optical specifications with optical parameters as specified for the four-level pulse amplitude modulation (PAM4) application codes 4I1-4D1F in [ITU-T G.959.1] and C4S1-4D1F in [ITU-T G.695]. These modules have a four-lane WDM interface to and from a transmit/receive pair of ITU-T G.652 optical fibres.

Similarly, first generation pluggable modules developed for Ethernet 400GBASE-R with 16 electrical lanes on the host side, and supporting 400G FlexO rate and FOIC4.16 host interface (that is roughly the same bit rate as OTL4.4 bit rate with similar digital format as 400GAUI-16) could be reused for 400G FlexO-SR transport. They have corresponding optical specifications with optical parameters as specified for the PAM4 application codes 8R1-4D1F or 8I1-4D1F in [ITU-T G.959.1]. These modules have an eight-lane WDM interface to and from a transmit/receive pair of ITU-T G.652 optical fibres.

These applications of m*FOIC2.8 bonded interfaces (short-reach m*200G FlexO-m group) and m*FOIC4.16 bonded interfaces (short-reach m*400G FlexO-m group) are illustrated in Figure 8-4.




m FOIC2.8 (short-reach) interfaces using CEI-28G (2m ≥ n)
Framer connected with m Pluggable Modules and/or ODSPs
*(*) NOTE – Some OPUCn Tributary Slots may be marked as unavailable.*

m FOIC4.16 (short-reach) interfaces using CEI-28G (4m ≥ n)
Framer connected with m Pluggable Optics and/or ODSPs
*(*) NOTE – Some OPUCn Tributary Slots may be marked as unavailable.*

**Figure 8-4 – Application of FOIC2.8 and FOIC4.16 interfaces**

NOTE – The RS10 (544,514) FEC computing and 200G/400G FlexO-SR lane distribution is summarized in clause 9.2 and fully specified in clauses 12 and 13 of [ITU-T G.709.1]. For FOIC2.8 and FOIC4.16, each physical lane corresponds to a 28G FlexO logical lane. This FEC scheme and lane architecture follow the same processes as specified in clause 119 of [b-IEEE 802.3bs] for 200GBASE-R (200GAUI-8) and 400GBASE-R (400GAUI-16) interfaces, respectively. Depending on the application, the RS10 FEC could be used as line FEC or terminated in an ODSP device. When the RS10 FEC is used as line FEC, the 28G lanes on the host interface could be bit multiplexed towards optical lanes. Also, in some applications, implementers could make, use or terminate the FlexO overhead in an ODSP device. Although some overheads may become optional, they are generated at the source and may be ignored at the sink (see clauses 9.1 and 9.2 for the handling of FlexO overhead for this type of application).

The bit rates of the FOIC2.8 and FOIC4.16 are indicated in Tables 8-4a and 8.4b.

**Table 8-4a – Bit rates of short-reach m*200G FlexO-m and FOIC2.8**

| FOIC type | FOIC nominal bit rate | FOIC bit-rate tolerance |
|---|---|---|
| FlexO-m (SR) | m × 8 × 256/241 × 239/226 × 24 883 200 kbit/s | ±20 ppm |
| FOIC2.8 | 8 × 256/241 × 239/226 × 24 883 200  kbit/s | ±20 ppm |
| FOIC2.8 lane | 256/241 × 239/226 × 24 883 200 kbit/s | ±20 ppm |
| NOTE – The nominal FOIC2.8 lane bit rate is approximately: 27 952 368.611 kbit/s. | | |

**Table 8-4b – Bit rates of short-reach m*400G FlexO-m and FOIC4.16**

| FOIC type | FOIC nominal bit rate | FOIC bit-rate tolerance |
|---|---|---|
| FlexO-m (SR) | m × 16 × 256/241 × 239/226 × 24 883 200 kbit/s | ±20 ppm |
| FOIC4.16 | 16 × 256/241 × 239/226 × 24 883 200 kbit/s | ±20 ppm |
| FOIC4.16 lane | 256/241 × 239/226 × 24 883 200 kbit/s | ±20 ppm |
| NOTE – The nominal FOIC4.16 lane bit rate is approximately: 27 952 368.611 kbit/s. | | |

## 9 Signal formats and rates carried over 56G electrical lanes

This clause describes some MFI structures using 56G physical lanes in order to carry B100G OTUCn (n ≥ 1) signals. The electrical characteristics of each 56G physical lane may comply with [b-OIF-CEI IA] CEI-56G-*x*R-PAM4 specifications.

### 9.1 FOIC1.2 structure

As shown in Figures 7-1 and 10-1 of [ITU-T G.709.1], an OTUCn signal (n ≥ 1), full-rate or sub-rated (with some OPUCn tributary slots marked as unavailable), can be carried over n*FOIC1.2 bonded interfaces (short-reach FlexO-n group, with v=1 and k=2). Each FOIC1.2 interface carry two physical lanes of a 100G FlexO-SR frame (carrying an OTUC).

An application example of the FOIC1.2 interface is to connect third generation beyond 100G OTN framers with ODSP devices over 56G electrical lanes and connecting these framers with emerging line side optical modules. See Figure 9-1.

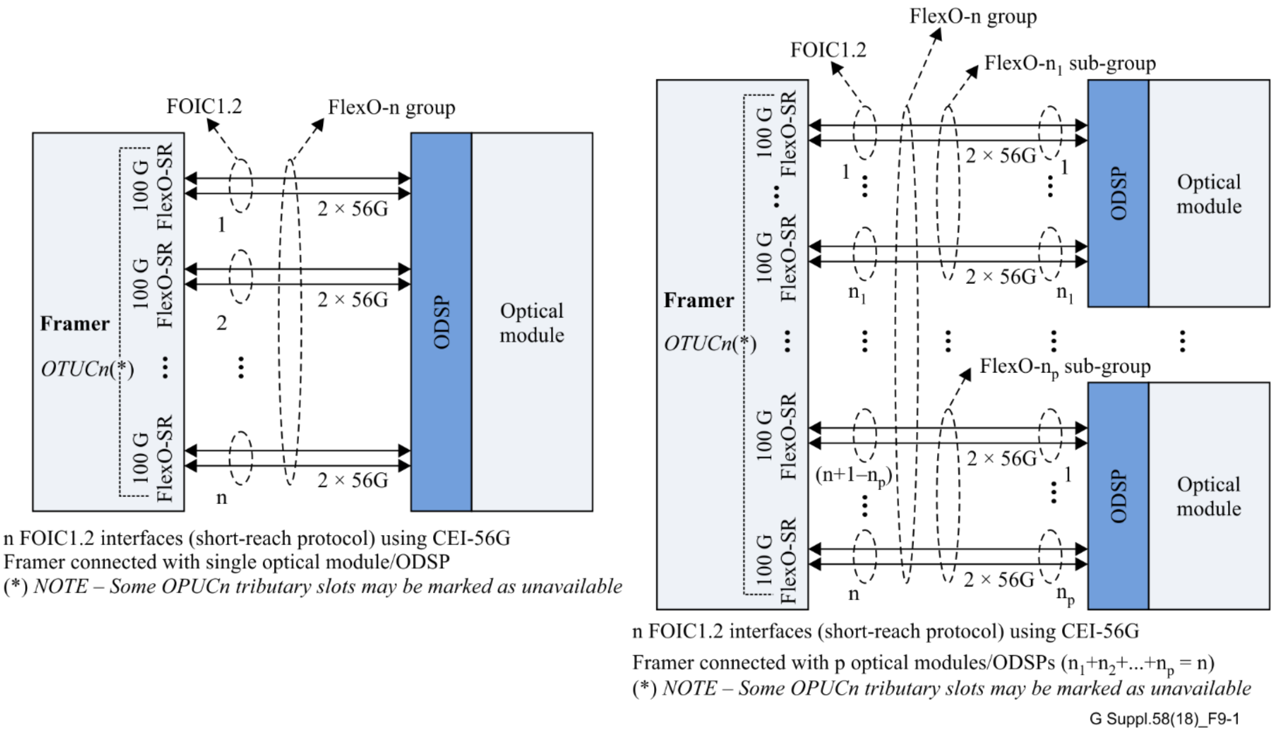



**Figure 9-1 – Example applications of a FOIC1.2 interface**

As per the mapping and framing specifications in clause 10 and 11 of [ITU-T G.709.1], the OTUCn is split into n times OTUC, and each OTUC is synchronously mapped and carried into an individual 100G FlexO-SR frame. The 100G FlexO-SR frame consists of frame alignment markers, overhead, FEC [RS10(544,514) parity], and payload area in which the OTUC is transported (see clause 8 of [ITU-T G.709.1]).

Two possible applications examples are considered. In the first case, the FlexO is terminated at both ends of the MFI. In the second case, the FlexO is terminated at the framer and (fully or partially) passed-through at the ODSP. The second case is for further study.

In the first application example, each 100G FlexO-SR frame is terminated at both ends of the MFI.

Thus, some FlexO OH become optional and though they are generated at the source, they may be ignored at the sink.

The FlexO multi-frame alignment signal (MFAS) is generated at the source and fully interpreted at the sink per clause 9.2.1 of [ITU-T G.709.1].

The use of the OTN synchronization messaging channel (OSMC) and FlexO communications channel (FCC) overhead across the MFI is for further study.

Additionally, the Rx Line pre-FEC detected local degrade (LD) status bit is optionally carried in bit 8 of the STAT field.

The Rx ODSP detects the Rx line pre-FEC LD and forwards the LD status bit to the Rx framer device through the MFI.

After synchronous scrambling and RS10 FEC parity insertion (see clauses 11.4 and 11.5 of [ITU-T G.709.1]), each individual 100G FlexO-SR frame is distributed (in groups of 10 bits) on four 28G FlexO logical lanes as described for FOIC1.4 in clause 11.6.1 of [ITU-T G.709.1].

Each 56G physical lane of a FOIC1.2 is formed by simple bit-multiplexing of two 28G FlexO logical lanes from the same 100G FlexO. At the sink, the bits from each individual 56G FOIC1.2 lane are disinterleaved into two 28G FlexO logical lanes. The sink will identify each of the four 28G FlexO logical lanes within a FOIC1.2 interface according to their alignment marker specific pattern (unique UMx and UPx values). The sink must be able to accept the four 28G FlexO logical lanes in any position, and in addition to 28G FlexO logical lanes alignment and deskew, proceed to reordering of these four logical 28G FlexO lanes prior to reassembly into a 100G FlexO-SR frame. Following this 100G FlexO-SR frame alignment, the FlexO overhead is terminated, and the OTUC is demapped and aligned. At the framer sink, the Rx line pre-FEC LD status bit is extracted from the FlexO overhead area and the n OTUC demapped from the n FOIC1.2 interfaces are deskewed to retrieve the original OTUCn signal. At the ODSP sink, $n_i$ OTUC demapped from $n_i$ FOIC1.2 interfaces could be deskewed, crunched (removing unavailable tributary slots), and assembled as the $OTUCn_i$ digital signal to be transmitted.

Groups of two FOIC1.2 physical lanes carrying one 100G FlexO-SR frame (so one OTUC instance) have to be connected as a 100G group. Physical lanes within such a 100G group can be interchanged, but physical lanes of different 100G groups must not be interchanged.

The bit rates of FOIC1.2 are specified in Table 9-1.

**Table 9-1 – Bit rates of short-reach FlexO-n and FOIC1.2**

| FOIC type | FOIC nominal bit rate | FOIC bit-rate tolerance |
|---|---|---|
| FlexO-n (SR) | n × 2 × 256/241 × 239/226 × 49 766 400 kbit/s | ±20 ppm |
| FOIC1.2 | 2 × 256/241 × 239/226 × 49 766 400 kbit/s | ±20 ppm |
| FOIC1.2 lane | 256/241 × 239/226 × 49 766 400 kbit/s | ±20 ppm |
| NOTE – The nominal FOIC1.2 lane bit rate is approximately: 55 904 737.223 kbit/s. | | |

## 9.2 FOIC2.4 and FOIC4.8 structures

As shown in Figure 7-1 and 10-1 of [ITU-T G.709.1], an OTUCn signal (n ≥ 1), full-rate or sub-rated (with some OPUCn tributary slots marked as unavailable), can be carried over m*FOIC2.4 or m*FOIC4.8 bonded interfaces (short-reach FlexO-m group, with {x,k} = {2,4} or {4,8} respectively). Each FOIC2.4 interface contains four physical lanes of a 200G FlexO-SR frame (carrying up to two OTUC). Each FOIC4.8 interface contains eight physical lanes of a 400G FlexO-SR frame (carrying up to four OTUC).

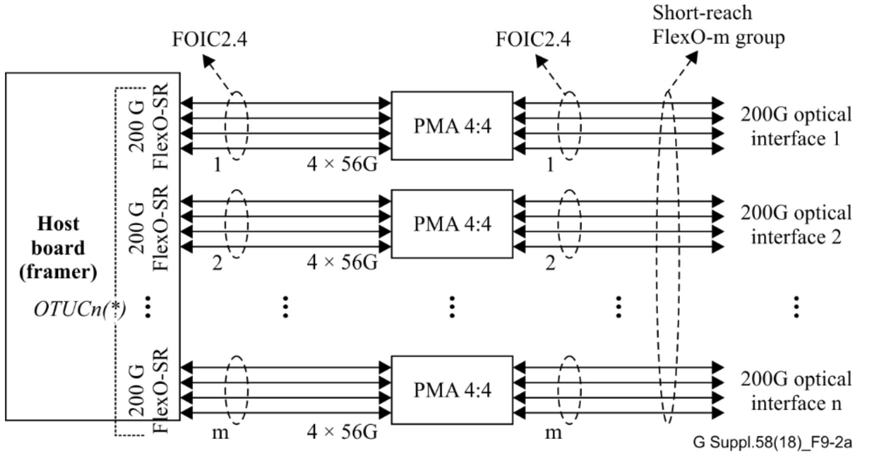
This provides interoperable modular short-reach OTN interfaces for B100G OTUCn (n ≥ 1) transport signals, by bonding m * 200G or m * 400G standard-rate interfaces.

Four-lane pluggable modules developed for Ethernet 200GBASE-R applications and supporting the FlexO rate (that is ~½ the OTU4 rate per 56G lane) could be reused for 200G FlexO-SR transport and FOIC2.4 interface. Eight-lane pluggable modules developed for Ethernet 400GBASE-R applications and supporting the FlexO rate (that is ~½ the OTU4 rate per 56G lane) could also be reused for 400G FlexO-SR transport and the FOIC4.8 interface. Modules developed for [b-IEEE 802.3bs] specified 200GBASE-FR4, 200GBASE-LR4, 400GBASE-FR8 and 400GBASE-LR8.

They have corresponding optical specifications for 200G FlexO-SR and 400G FOICs with the optical parameters as specified for the PAM4 application codes 4I1-4D1F and 8R1-4D1F or 8I1-4D1F, respectively, in [ITU-T G.959.1] and ITU-T G.695 PAM4 application code C4S1-4D1F. The 200G modules have a four-lane WDM interface and the 400G modules have an eight-lane to and from a transmit/receive pair of ITU-T G.652 optical fibres.

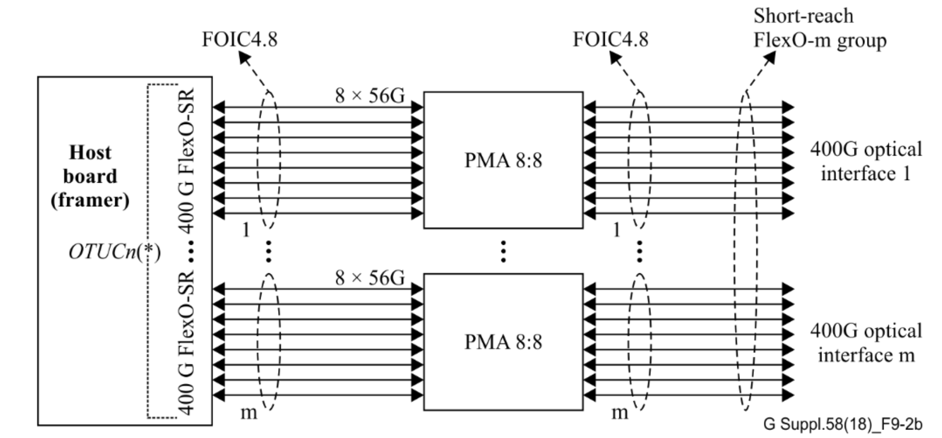
Most of these pluggable modules use a four-lane electrical chip-to-module interface (200GAUI-4) or an eight-lane chip-to-module interface (400GAUI-8), whose specifications are found in Annex 120E of [b-IEEE 802.3bs].

These applications of m*FOIC2.4 bonded interfaces (short-reach m*200G FlexO-m group) and m*FOIC4.8 bonded interfaces (short-reach m*400G FlexO-m group) are illustrated in Figures 9-2a and 9.2b respectively.




m FOIC2.4 short-reach interfaces using CEI-56G to m bonded 200G optical modules (2m ≥ n)
(*) *NOTE – Some OPUCn tributary slots may be marked as unavailable; if 2m = n, then each 200G FlexO-SR carries two OTUC; else if 2m > n, some 200G FlexO-SR signal frames within the group only carry one OTUC in their first 100G FlexO instance (second 100G FlexO instance being unequipped)*

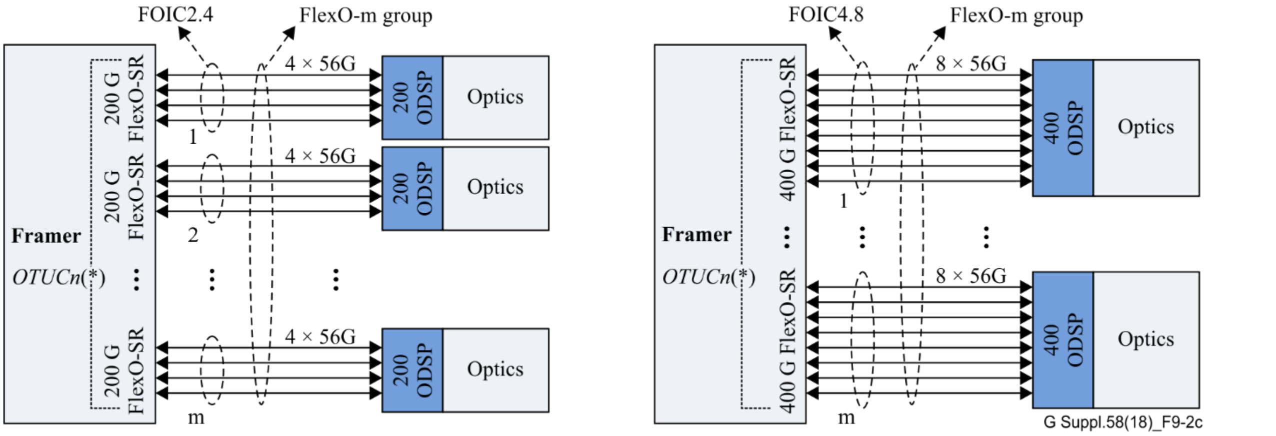
**Figure 9-2a – FOIC2.4 interface main application example**




m FOIC4.8 short-reach interfaces using CEI-56G to m bonded 400G optical modules (4m ≥ n)
*(*) NOTE – Some OPUCn tributary slots may be marked as unavailable; if 4m = n, then each 400G FlexO-SR carries two OTUC; else if 4m > n, some 400G FlexO-SR signal frames within the group carry fewer than four, but at least one OTUC (the last one, two or three 100G FlexO instance(s) being unequipped)*

**Figure 9-2b – FOIC4.8 interface main application example**

The FOIC2.4 or FOIC4.8 interface could be used alternately to two or four FOIC1.4 interfaces in order to connect a beyond 100G OTN framer with one or more 200G or 400G ODSP devices supporting FlexO interfaces on the host side. One possible advantage for implementers is that the FEC and lane processing for 200G FOIC2.4 or 400G FOIC4.8 interface is almost identical to 200GAUI-4 or 400GAUI-8, respectively, thus allowing digital logic in an optimized DSP supporting both Ethernet and OTN signals on its host side to be shared. This alternative application is illustrated in Figure 9-2c.




m FOIC2.4 (short-reach) interfaces using CEI-56G
Framer connected with m ODSPs (2m ≥ n)
(*) *NOTE – Some OPUCn tributary slots may be marked as unavailable*

m FOIC4.8 (short-reach) interfaces using CEI-56G
Framer connected with m ODSPs (4m ≥ n)
(*) *NOTE – Some OPUCn tributary slots may be marked as unavailable*

**Figure 9-2c – Alternative application of FOIC2.4 and FOIC4.8 interfaces**

As per the mapping specification in clause 10 of [ITU-T G.709.1], the OTUCn is split into n times OTUC, and each OTUC is synchronously mapped into an individual 100G FlexO instance/frame. Each 100G FlexO frame consists of frame alignment markers (AMs), pad area (PAD), overhead area (OH), and payload area in which the OTUC is transported (see clause 8 of [ITU-T G.709.1]).

Then, as described in clause 12 of [ITU-T G.709.1] for 200G FlexO-SR, each set of two 100G FlexO instances (A, B) corresponds to a 200G FlexO frame, and m* 200G FlexO-SR frames carry the OTUCn (n ≤ 2m). If [n=2m], then each 200G frame carries two OTUC. When [n < 2m], then [i]* 200G frames carry two OTUC, while [m-i]* 200G frames only carry one OTUC in their first 100G FlexO instance (the second 100G FlexO instance being unequipped).

As described in clause 13 of [ITU-T G.709.1] for 400G FlexO-SR, each set of two 100G FlexO is interleaved (on a 10-bit basis) as a 200G FlexO Instance, and the resulting set of two 200G FlexO instances corresponds to a 400G FlexO frame. m* 400G FlexO-SR frames carry the OTUCn. If [n = 4m], then each 400G frame carries four OTUC. If [n < 4m], then, some 400G frames carry fewer than four, but at least one OTUC [the last one, two or three 100G FlexO instance(s) being unequipped].

Depending on the application, the FlexO overhead may be terminated or carried transparently in the ODSP. When it is terminated in the ODSP, see clause 9.1 for the handling of FlexO overhead for this type of application.

For both applications, the Rx ODSP detects the Rx line pre-FEC LD and optionally forward the LD status bit to the Rx framer device through the MFI, as carried in bit 8 of the STAT field of the first 100G FlexO instance overhead of the 200G or 400G FlexO-SR frame.

After FEC area insertion, interleaving (on a 10-bit basis) of the two 100G FlexO instances (200G FlexO-SR) or two 200G FlexO instances (400G FlexO-SR) and scrambling of the 200G/400G FlexO-SR frame, the AM values are inserted. Then, the RS10(544,514) FEC parity is calculated based on two interleaved RS10 codewords. For 200G FlexO-SR, the resulting 200G signal is distributed on eight 28G FlexO logical lanes as per the 200G FOIC specifications in clause 12.6 of [ITU-T G.709.1]. For 400G FlexO-SR, the resulting 400G signal is distributed on 16 28G FlexO logical lanes as per the 400G FOIC specifications in clause 13.6 of [ITU-T G.709.1]. FEC calculation and lane distribution (in group of 10 bits) follow the same processes as specified in clause 119 of [b-IEEE 802.3bs] for 200GBASE-R and 400GBASE-R interfaces, respectively.

Each 56G physical lane of a FOIC2.4 or FOIC4.8 is formed by simple bit-multiplexing of two 28G FlexO logical lanes from the same 200G FlexO-SR or 400G FlexO-SR, respectively. At the sink, the bits from each individual 56G FOIC2.4 or 56G FOIC4.8 lane are deinterleaved into two 28G FlexO logical lanes. The sink will identify each of the eight 28G FlexO logical lanes within a FOIC2.4 interface according to its alignment marker specific pattern (unique UMx and UPx values). The sink must be able to accept the eight 28G FlexO logical lanes in any position, and in addition to 28G FlexO logical lanes alignment and deskew, proceed to reordering of these eight 28G FlexO logical lanes prior to reassembly into a 200G FlexO-SR frame. Similarly, in the case of FOIC4.8, the sink must be able to accept the 16 28G FlexO logical lanes in any position, and in addition to 28G FlexO logical lanes alignment and deskew, proceed to reordering of these 16 28G FlexO logical lanes prior to reassembly into a 400G FlexO-SR frame.

Following this 200G or 400G FlexO-SR frame alignment, FEC termination and descrambling, the FlexO overhead is terminated, and, depending on the application, each OTUC can be demapped from its deinterleaved 100G FlexO instance and aligned. At the framer sink, the Rx line pre-FEC LD status bit is extracted from the FlexO overhead area and the n OTUC demapped from the m FOIC2.4 or m FOIC4.8 interfaces are deskewed to retrieve the original OTUCn signal. At the ODSP sink, and if applicable, n OTUC demapped from an FOIC2.4 or FOIC4.8 interface could be deskewed, crunched (removing unavailable tributary slots), and assembled as the OTUCn digital signal to be transmitted.

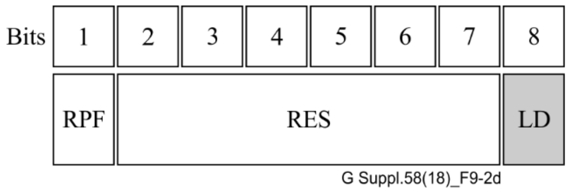



**Figure 9-2d – Optional Rx line pre-FEC local degrade status bit location in the first instance of FlexO OH STAT field (Rx ODSP to framer direction)**

The bit rates of the FOIC2.4 and FOIC4.8 specified in [ITU-T G.709.1] are indicated in Table 9-2a and 9-2b, respectively.

**Table 9-2a – Bit rates of short-reach m*200G FlexO-m and FOIC2.4**

| FOIC type | FOIC nominal bit rate | FOIC bit-rate tolerance |
|---|---|---|
| FlexO-m (SR) | m × 4 × 256/241 × 239/226 × 49 766 400 kbit/s | ±20 ppm |
| FOIC2.4 | 4 × 256/241 × 239/226 × 49 766 400 kbit/s | ±20 ppm |
| FOIC2.4 lane | 256/241 × 239/226 × 49 766 400 kbit/s | ±20 ppm |
| NOTE – The nominal FOIC2.4 lane bit rate is approximately: 55 904 737.223 kbit/s. | | |

**Table 9-2b – Bit rates of short-reach m*400G FlexO-m and FOIC4.8**

| FOIC type | FOIC nominal bit rate | FOIC bit-rate tolerance |
|---|---|---|
| FlexO-m (SR) | m × 8 × 256/241 × 239/226 × 49 766 400 kbit/s | ±20 ppm |
| FOIC4.8 | 8 × 256/241 × 239/226 × 49 766 400 kbit/s | ±20 ppm |
| FOIC4.8 lane | 256/241 × 239/226 × 49 766 400 kbit/s | ±20 ppm |
| NOTE – The nominal FOIC4.8 lane bit rate is approximately: 55 904 737.223 kbit/s. | | |

# Bibliography


[b-IEEE 802.3] IEEE Std. 802.3 (2015), *IEEE Standard for Ethernet*.

[b-IEEE 802.3bs] IEEE Std 802.3bs-2017, *IEEE Standard for Ethernet Amendment 10: Media access control parameters, physical layers and management parameters for 200 Gb/s and 400 Gb/s operation.*

[b-OIF-CEI IA] Optical Internetworking Forum Implementation Agreement OIF-CEI-04.0 (2017), *Common electrical I/O (CEI) – Electrical and jitter interoperability agreements for 6G+ bps, 11G+ bps,25G+ bps and 56G+ bps I/O*.

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