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SERIES G: TRANSMISSION SYSTEMS AND MEDIA, DIGITAL SYSTEMS AND NETWORKS

Access networks – In premises networks

Indoor optical camera communication transceivers – System architecture, physical layer and data link layer specification

Recommendation ITU-T G.9992

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Recommendation ITU-T G.9992

Indoor optical camera communication transceivers – System architecture, physical layer and data link layer specification

Summary

Recommendation ITU-T G.9992 specifies the system architecture, physical (PHY) layer and data link layer (DLL) for indoor optical camera communication transceivers.

History

Edition	Recommendation	Approval	Study Group	Unique ID*
1.0	ITU-T G.9992	2019-03-22	15	11.1002/1000/13782

Keywords

DLL, MIMO, OCC, PHY, SISO, UPPM, UPWM.

* To access the Recommendation, type the URL http://handle.itu.int/ in the address field of your web browser, followed by the Recommendation's unique ID. For example, http://handle.itu.int/11.1002/1000/11830-en.

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Indoor optical camera communication transceivers – System architecture, physical layer and data link layer specification

1 Scope

This Recommendation specifies the system architecture and functionality for all components of the physical layer (PHY) and data link layer (DLL) of optical camera communication (OCC) transceivers for in-premises applications.

In particular, this Recommendation specifies:

– the OCC system architecture and reference models;

– the physical layer (PCS, PMA and PMD); and

– the data link layer.

2 References

The following ITU-T Recommendations and other references contain provisions which, through reference in this text, constitute provisions of this Recommendation. At the time of publication, the editions indicated were valid. All Recommendations and other references are subject to revision; users of this Recommendation are therefore encouraged to investigate the possibility of applying the most recent edition of the Recommendations and other references listed below. A list of the currently valid ITU-T Recommendations is regularly published. The reference to a document within this Recommendation does not give it, as a stand-alone document, the status of a Recommendation.

[IEEE 802.1ad] IEEE 802.1ad-2005, *IEEE Standard for Local and metropolitan area networks: Provider Bridges*.

[IEEE 802.1D] IEEE 802.1D -2004, *IEEE Standard for Local and metropolitan area networks Media Access Control (MAC) Bridges*.
<http://standards.ieee.org>

[IEEE 802.1Q] IEEE 802.1Q-2005, *IEEE Standard for Local and Metropolitan Area Networks – Virtual Bridged Local Area Networks – Revision.*
<http://standards.ieee.org>

[IEEE 802.3] IEEE 802.3-2008, *IEEE Standard for Information technology-Specific requirements – Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications*.
<http://standards.ieee.org>

3 Definitions

3.1 Terms defined elsewhere

This Recommendation uses the following terms defined elsewhere:

3.1.1 channel [b-ITU-T G.9960]: A transmission path between nodes. One channel is considered to be one transmission path. Logically, a channel is an instance of a communication medium used for the purpose of passing data between two or more nodes.

3.1.2 coding overhead [b-ITU-T G.9960]: A part of the overhead used to carry the coding redundancy (such as redundancy bits of error correction coding or cyclic redundancy check (CRC)).

3.1.3 data [b-ITU-T G.9960]: Bits or bytes transported over the medium or via a reference point that individually convey information. Data includes both user (application) data and any other auxiliary information (overhead, including control, management, etc.). Data does not include bits or bytes that, by themselves, do not convey any information, such as the preamble.

3.1.4 data rate [b-ITU-T G.9960]: The average number of bits communicated (transmitted) in a unit of time. The usual unit of time for data rate is 1 second.

3.1.5 logical (functional) interface [b-ITU-T G.9960]: An interface in which the semantic, syntactic, and symbolic attributes of information flows are defined. Logical interfaces do not define the physical properties of signals used to represent the information. It is defined by a set of primitives.

3.1.6 physical interface [b-ITU-T G.9960]: An interface defined in terms of physical properties of the signals used to represent the information transfer. A physical interface is defined by signal parameters such as power (power spectrum density), timing, and connector type.

3.1.7 primitives [b-ITU-T G.9960]: Basic measures of quantities obtained locally or reported by other nodes of the domain. Performance primitives are basic measurements of performance-related quantities, categorized as events, anomalies and defects. Primitives may also be basic measures of other quantities (e.g., a.c. or battery power).

3.1.8 reference point [b-ITU-T G.9960]: A location in a signal flow, either logical or physical, that provides a common point for observation and/or measurement of the signal flow.

3.2 Terms defined in this Recommendation

This Recommendation defines the following terms:

3.2.1 alien domain: Any group of non-ITU-T G.9992 nodes connected to the same medium or that operate in close proximity.

NOTE – The bridging function to an alien domain, as well as coordination with an alien domain to avoid mutual interference is beyond the scope of this Recommendation.

3.2.2 domain: An ITU-T G.9992 network comprising the domain master and all those nodes that are registered with the same domain master.

NOTE – In the context of this Recommendation, use of the term "domain" without a qualifier means "ITU-T G.9992 domain". Additional qualifiers (e.g., "OCC") may be added to "domain".

3.2.3 domain master (DM): A node supporting the domain master functionality that manages (coordinates) all other nodes of the same domain (i.e., assigns bandwidth resources and manages priorities). Only one active domain master is allowed in a domain, and all nodes within a domain are managed (coordinated) by a single domain master.

3.2.4 global master (GM): A function that provides coordination between different domains (such as communication resources, policies of domain masters). A global master may also convey management functions initiated by the remote management system (e.g., the Broadband Forum CPE WAN management protocol) to support broadband access.

3.2.5 node: Any network device that contains an ITU-T G.9992 transmitter/receiver/transceiver.

NOTE – In the context of this Recommendation, use of the term "node" without a qualifier means "ITU-T G.9992 node". Additional qualifiers may be added to either "node".

3.2.6 unidirectional broadcasting node: A node supporting the unidirectional broadcasting node functionality that broadcasts signals in an ITU-T G.9992 system that operates in a unidirectional broadcasting mode.

4 Abbreviations and acronyms

This Recommendation uses the following abbreviations and acronyms:

AAT Address Association Table

ADP Application Data Primitive

AE Application Entity

APC Application Protocol Convergence

APDU Application Protocol Data Unit

CRC Cyclic Redundancy Check

DBM Domain Based Mode

DC Duty Cycle

DID Destination ID

DLL Data Link Layer

DM Domain Master

DPI Destination ID field Present Indication

DSL Digital Subscriber Line

EDR End Delimiter Region

FCS Frame Check Sequence

FEC Forward Error Correction

FLEN Frame Length

FT Frame Type

FTSF Frame-Type Specific Field

GM Global Master

GS Global Shutter

HCS Header Check Sequence

IDB Inter-Domain Bridges

IDR Interval Delimiter Region

LAAT Local Address Association Table

LCDU Link Control Data Unit

LFH Logical link control Frame Header

LED Light Emitting Diode

LLC Logical Link Control

LNIR LED Number Indicating Region

LSB Least Significant Bit

MAC Medium Access Control

MDI Medium-Dependent Interface

MIMO Multiple Input/Multiple Output

MMH	Management Message Header
MMPL	Management Message Parameter List
MPDU	Media access control Protocol Data Unit
MSB	Most Significant Bit
OCC	Optical Camera Communication
PB	Parity Bit
PCS	Physical Coding Sublayer
PFH	PHY-frame headers
PHY	Physical Layer
PI	Preamble Information
PL	Payload Length
PMA	Physical Medium Attachment
PMD	Physical Medium Dependent
PMI	Physical Medium-independent Interface
PON	Passive Optical Network
PSD	Power Spectral Density
PWM	Pulse Width Modulation
RAAT	Remote Address Association Table
RCP	Reduced-Complexity Profile
RS	Rolling Shutter
SDR	Start Delimiter Region
SID	Source ID
SISO	Single Input/Single Output
SS	Spatial Streams
UBM	Unidirectional Broadcasting Mode
UPPM	Undersampled Pulse Position Modulation
UPWM	Undersampled Pulse Width Modulation
VDR	Valid Data Region

5 Conventions

5.1 Bit ordering convention

A block of data composed of multiple octets shall be ordered by octet numbers in ascending order: 'octet 0' for the first octet, 'octet 1' for the second octet, and so on. If a block of data is segmented into multiple fields, the size of each field shall be expressed in terms of bits. The field might not be an integer number of octets. The location of each field within a block of data shall be described as follows:

– The octets of an N-octet data block are ordered with numbers from 0 (first octet) to N–1 (last octet).

– The block is divided into non-overlapping groups of octets. Each group contains an integer number of consecutive octets, numbered from J to $J+V–1$, where V is the size of the group, and is described as a bit string with 'bit 0', the least significant bit (LSB) of the octet with the smallest number (J), and 'bit ($8×V–1$)', the most significant bit (MSB) of the octet with the largest number ($J+V–1$).
– Each group is divided into one or more fields, where the boundaries of each field are determined by the LSB and the MSB of the bits of the group that contains this field.

Any block or partial block of data shall be passed over the protocol stack with the octet having the smallest number first, i.e., octet 0 shall be the first octet of the block to be passed. Within each group of octets, the LSB (bit 0) of each octet shall be passed first.

Table 5-1 shows an example of a field description used throughout this Recommendation. The 'Octet' column represents the octet numbers for a group of octets to which a specific field belongs, and the 'Bits' column represents the bit location within this group of octets. In the example presented, there are 4 groups of octets:

– Group 1 = Octet 0, fields A, B, C, D
– Group 2 = Octets 1 and 2, fields E, F
– Group 3 = Octet 3, field G
– Group 4 = Octets 4 to 7, field H.

Figure 5-1 illustrates a mapping of these fields onto corresponding octets based on the example given in Table 5-1.

Table 5-1 – Example of field description

Field	Octet	Bits	Description
A	0	[2:0]	…
B	0	[3]	…
C	0	[4]	…
D	0	[7:5]	…
E	1	[1:0]	…
F	1-2	[15:2]	…
G	3	[7:0]	…
H	4-7	[31:0]	…

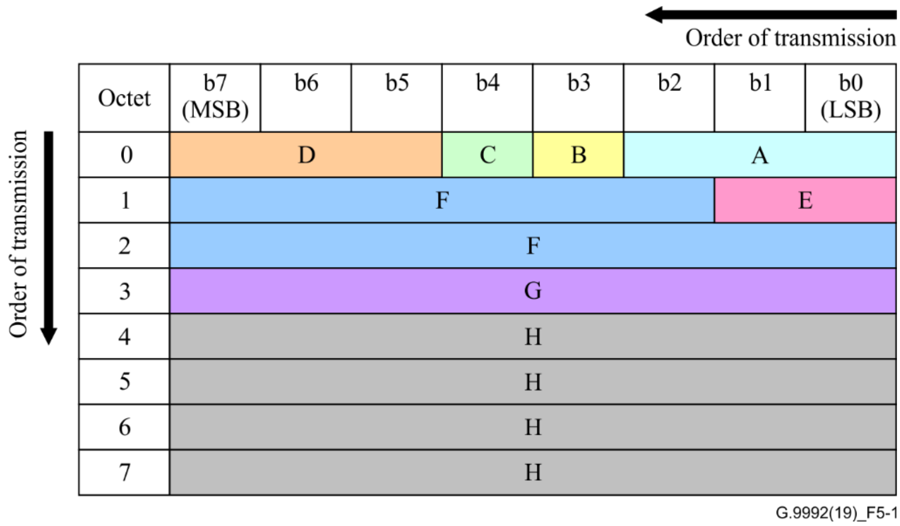


Figure 5-1 – Example of mapping fields onto groups of octets

5.2 Endpoint node

This term is used in this Recommendation according to the context to differentiate between the domain master node functionalities and non-domain master node functionalities in a DBM domain, or between the unidirectional broadcasting node functionalities and non-unidirectional broadcasting node functionalities for unidirectional broadcasting mode.

6 System architecture and reference models

6.1 System architecture and topology

An architectural model of an ITU-T G.9992 home network is presented in Figure 6-1. The model includes one or more unidirectional broadcasting nodes, one or more domains, inter-domain bridges (IDB), and bridges to alien domains such as a Wi-Fi or Ethernet home network, or a digital subscriber line (DSL) or passive optical network (PON) access network. The global master function coordinates resources such as bandwidth reservations, flow priorities, and operational characteristics between domains, and may convey the relevant functions initiated by a remote management system (e.g., as specified in [b-TR-069]) to support broadband access.

NOTE 1 – Detailed specification and use of the global master function is for further study.

NOTE 2 – The specification of bridges to alien domains and to the access network is beyond the scope of this Recommendation.

NOTE 3 − It is not necessary that all inter-domain bridges presented in Figure 6-1 be used. Depending on the application, domains could be daisy-chained, or star-connected, or could use another connection topology. Support of multi-route connections between domains is for further study.

NOTE 4 – It is possible to install multiple ITU-T G.9992 home networks (i.e., not connected by bridges to alien domain and the alien domain) per dwelling.

NOTE 3 – The unidirectional broadcasting nodes are not involved in the coordination performed by the global master.

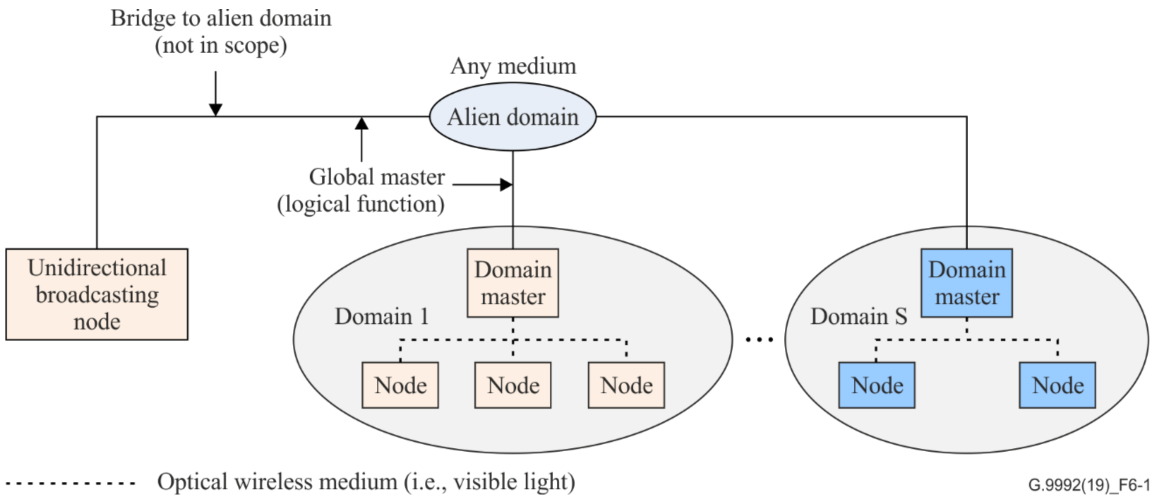


Figure 6-1 – Home network architecture reference model

A domain comprises a domain master (DM) and may contain one or more nodes registered with it. The domain master considers bridges to alien domains as application entities (AEs) of a node with certain requirements.

6.1.1 Modes of operation

An ITU-T G.9992 system can operate in one of the following two modes. A unidirectional broadcasting mode (UBM) and domain based mode (DBM).

In UBM, only unidirectional transmissions are supported. The unidirectional broadcasting node broadcasts signals, while one or more endpoint nodes receive the signals. The establishment of a domain is not needed in a UBM.

In the DBM, the operation of an ITU-T G.9992 system shall be based on the domain, which comprises a domain master and one or more endpoint nodes that registered to the same domain master. Broadcast shall be supported in any domain.

NOTE – The detailed specification of DBM is for further study.

6.1.2 Dual-channel operation

An ITU-T G.9992 transceiver provides two independent channel to the application entity. A low-speed channel and a high-speed channel, and it may operate on any of the two channels, or on both of the two channels simultaneously. The selection of the operation channels shall be vendor discretionary or configured by the user.

6.2 Reference models

6.2.1 Protocol reference model of transceiver

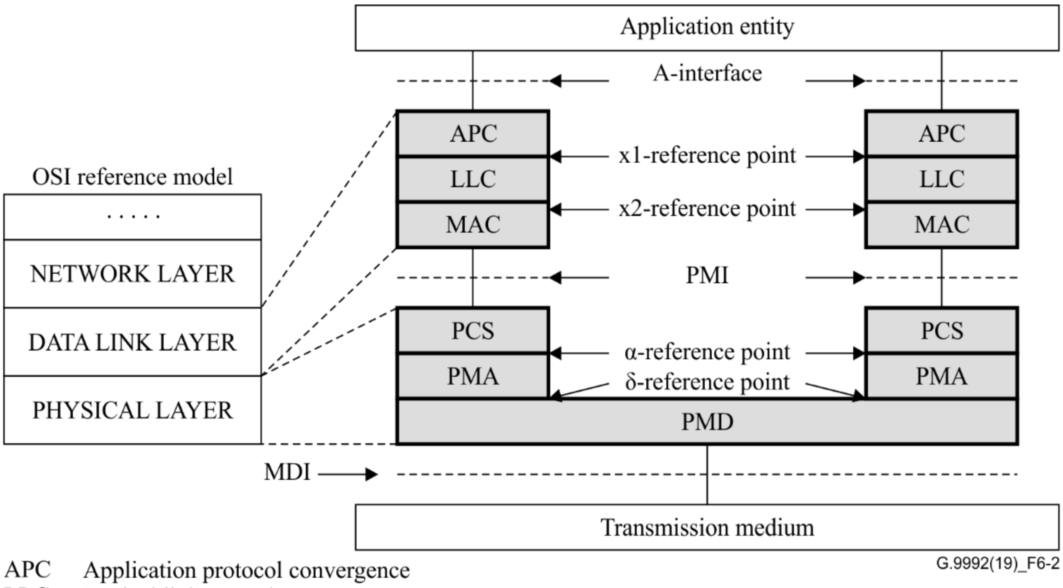
The protocol reference model of an ITU-T G.9992 transceiver is presented in Figure 6-2. For each channel, it includes two main reference points. An application interface (A-interface) and the physical medium-independent interface (PMI). The two channels shares the same medium-dependent interface (MDI). For each channel, two intermediate reference points, x1 and x2, are defined in the data link layer (DLL), and two other intermediate reference points, α and δ, are defined in the PHY layer (Figure 6-2).

The MDI is a physical interface defined in terms of the physical signals transmitted over a specific medium (see clause 6.2.2.3).

The PMI interface is both medium independent and application independent. It is defined in clause 6.2.2.2 as a functional interface, in terms of functional flows and logical signals.

The A-interface is user application-protocol specific (e.g., Ethernet, IP). The functional description of the A-interface is presented in clause 6.2.2.1. The A-interfaces of the two channels are independent.

All intermediate reference points are independent of the type of medium and are defined as functional (logical) interfaces in terms of the functional flows and logical signals.



APC Application protocol convergence
LLC Logical link control
MAC Medium access control
PCS Physical coding sub-layer
PMA Physical medium attachment
PMD Physical medium dependent
PMI Physical medium-independent interface
MDI Medium-dependent interface

Figure 6-2 – Protocol reference model of an ITU-T G.9992 transceiver

The application protocol convergence (APC) sublayer provides an interface with the application entity (AE), which operates with an application-specific protocol, such as Ethernet.

The logical link control (LLC) sublayer coordinates transmission of nodes.

The medium access control (MAC) sublayer controls access of the node to the medium.

The physical coding sublayer (PCS) encapsulates transmit media access control protocol data units (MPDUs) into the PHY frame and adds PHY-related control and management overhead. The physical medium attachment (PMA) provides encoding of PHY frame content for transmission over the medium. The PMD modulates and demodulates PHY frames for transmission using undersampled pulse width modulation (UPWM) or undersampled pulse position modulation (UPPM).

The layers above the data link layer (above the A-interface) are beyond the scope of this Recommendation. Management functions are therefore not presented in Figure 6-2.

6.2.2 Interfaces – functional description

This clause contains the functional description of the ITU-T G.9992 transceiver interfaces (A, PMI, and MDI) in terms of signal flows exchanged between corresponding entities. The description does not imply any specific implementation of the transceiver interfaces.

6.2.2.1 A-interface

The A-interface is described in terms of primitives exchanged between the AE and the DLL. There are six general types of A-interface primitives, as shown in Table 6-1. Each primitive type may consist of one or more primitives, related to control or data, respectively. Data primitives represent the data path of the A-interface, while control primitives represent the control path. The format of the application data primitives (ADPs) is application specific, determined by the AE.

Table 6-1 – A-interface primitive type summary

Primitive type	Direction	Description
AIF_DATA.REQ	AE → DLL	Data from AE to DLL
AIF_DATA.CNF	DLL→AE	Data confirmation from DLL to AE
AIF_DATA.IND	DLL→ AE	Data from DLL to AE
AIF_CTRL.REQ	AE → DLL	Control from AE to DLL
AIF_CTRL.CNF	DLL → AE	Control confirmation from DLL to AE
AIF_CTRL.IND	DLL → AE	Control from DLL to AE

6.2.2.2 Physical medium-independent interface

The physical medium-independent interface (PMI) is described in terms of primitives exchanged between the DLL and PHY layer presented in Table 6-2. The direction of each primitive flow indicates the originating entity of the primitive. Both transmit and receive data primitives are exchanged in MPDUs.

Table 6-2 – PMI primitive description

Primitive	Direction	Description
PMI_DATA.REQ	DLL → PHY	Flow of MPDUs for transmission
PMI_CTRL-RxDis.REQ	DLL→ PHY	Disables receive of PHY frames
PMI_DATA.IND	PHY → DLL	Flow of received MPDUs
PMI_CTRL-ERR.IND	PHY → DLL	Error primitive that accompanies an MPDU received with errors
RX ENABLE	DLL → PHY	Enable receive function in the PHY layer
NOTE – Primitives presented in this table are exclusively for descriptive purposes and do not imply any specific implementation.		

6.2.2.3 Medium-dependent interface

Functional characteristics of the medium-dependent interface (MDI) are described by two signal flows:

– transmit signal (TX DATA) is the flow of frames transmitted on to the medium;

– receive signal (RX DATA) is the flow of frames received from the medium.

6.2.3 Functional model of an ITU-T G.9992 transceiver

The functional model of an ITU-T G.9992 transceiver is presented in Figure 6-3. It addresses nodes without extended capabilities, as well as nodes with extended capabilities such as domain master, and relaying (including DAP), which differ by their MAC, LLC and upper layer functionalities.

The PMD function depends on the channels on which the transceiver operates. It can be configured for single-channel or dual-channel operation. The PCS encapsulates transmit MPDUs into PHY frames. The transmit PHY frame is further encoded in the PMA to meet the corresponding PMD.

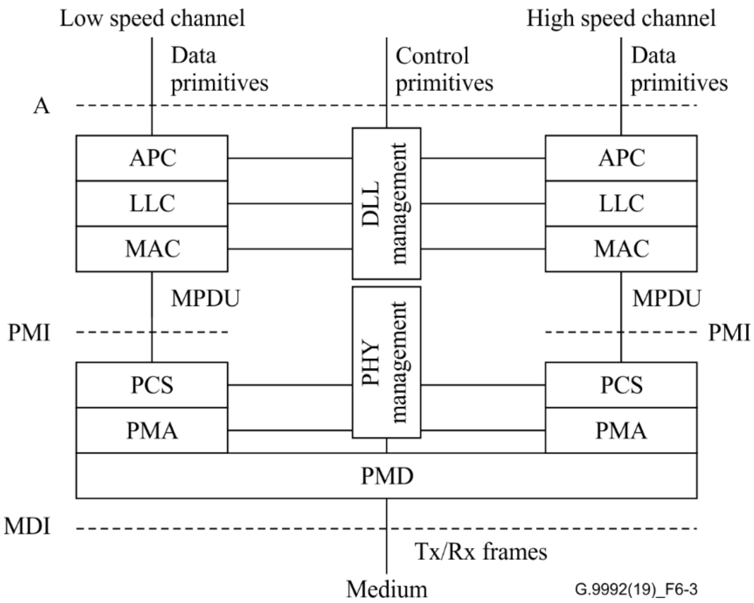


Figure 6-3 − Functional model of an ITU-T G.9992 transceiver

The detailed description of the functional model of the PHY layer is presented in clause 8.1.1. The DLL is specified in clause 9.

7 Profiles

Profiles are intended to specify nodes with significantly different levels of complexity and functionality. A more complex profile is a superset of a less complex profile and shall interoperate with that profile. A node shall be classified into particular profiles according to its degree of complexity and functionality. For compliance with this Recommendation, a node is required to support one profile, at a minimum. Profiles are summarized in Table 7-1.

Table 7-1 – Profiles

Profile name	Transmission mode	Description
Reduced-complexity profile	Single input/single output (SISO)	Only low speed channel is supported
	UPWM-based multiple input/multiple output (MIMO)	
Standard profile	SISO	Dual channels are supported
	UPPM-based MIMO	
NOTE 1 – The classification of profiles is applicable to the transmit direction only. An ITU-T G.9992 node shall be capable of receiving from nodes that are classified into any profile. NOTE 2 – Regardless of profile, if multiple TX ports are used, the node shall only implement MIMO, and if only one TX port is used, the node shall only implement SISO.		

7.1 Reduced-complexity profile

Table 7-2 describes the features and valid values of parameters for the reduced-complexity profile (RCP) that differentiate it from the standard profile.

Table 7-2 – Features and valid parameters for the reduced-complexity profile

Parameter/feature	Description
Modulation	UPWM
Maximum number of TX ports	4096
MIMO	UPWM-based MIMO

7.2 Standard profile

Table 7-3 describes the features and valid values of parameters for the standard profile that differentiate it from the reduced-complexity profiles.

Table 7-3 – Features and valid parameters for the standard profile

Parameters	Description
Modulation	UPWM, UPPM
Maximum number of TX ports	4
MIMO	UPPM-based MIMO

8 Physical layer specification

8.1 SISO transmission

8.1.1 Functional model of the PHY

The functional model of the PHY is represented in Figure 8-1. The PMI and DMI are, respectively, two demarcation reference points between the PHY and MAC and between the PHY and the transmission medium. Internal reference points δ and α show separation between the PMD and PMA, and between the PCS and PMA, respectively.

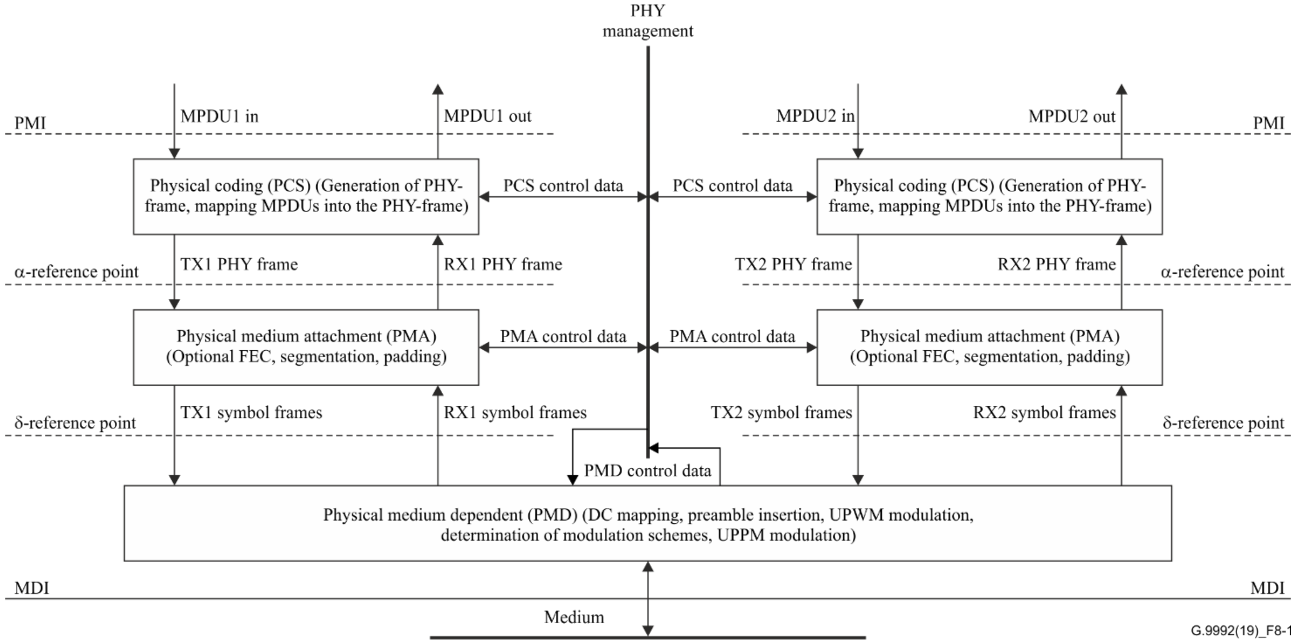


Figure 8-1 – Functional model of the PHY

In the transmit direction, for each channel, data enters the PHY from the MAC via the PMI in blocks of bytes called MPDUs. The incoming MPDU is mapped into a PHY frame in the PCS, encoded in the PMA, modulated in the PMD, and transmitted over the medium. If the transceiver only operates on the low speed channel, the TX symbol frames are modulated using UPWM modulation with relevant parameters, and in the PMD, a preamble is added to assist synchronization and phase compensation in the receiver. If the transceiver operates on the high speed channel, the TX symbol frames are modulated using UPPM modulation with pre-defined duty cycles (DCs). If the transceiver operates on dual channels, the TX symbol frames of the high speed channel are modulated using UPPM modulation with the DCs obtained from the DC mapping of the TX symbol frames of the low speed channel.

In the receive direction, frames entering from the medium via the MDI are demodulated and decoded. The recovered MPDUs are forwarded to the MAC via the PMI. The recovered PHY-frame headers are processed in the PHY to extract the relevant frame parameters specified in clause 8.1.2.3.

For unidirectional broadcasting mode, only one of the directions is enabled for a particular node.

8.1.2 Physical coding sublayer

The functional model of the PCS is presented in Figure 8-2. It is intended to describe in more detail the PCS functional block presented in Figure 8-1.

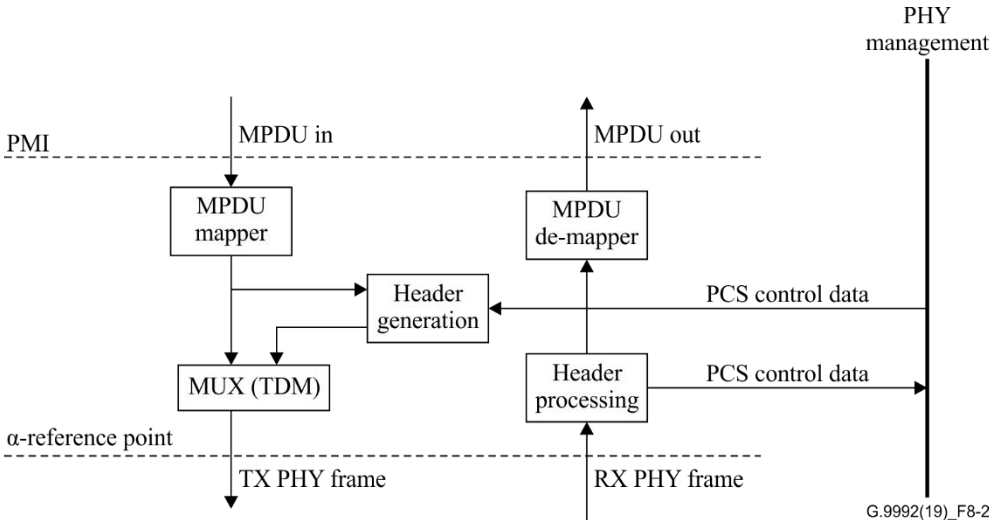


Figure 8-2 – Functional model of PCS

In the transmit direction, the incoming MPDU is mapped into a payload field of a PHY frame (clause 8.1.2.1) as described in clause 8.1.2.2. The PHY-frame header (clause 8.1.2.3) is then added to form a TX PHY frame. The TX PHY frame is passed across the α-reference point for further processing in the PMA.

In the receive direction, the decoded PHY-frame payload and header are processed, and originally transmitted MPDUs are recovered from the payloads of received PHY frames and submitted to the PMI. Relevant control information conveyed in the PHY-frame header is processed and submitted to the PHY management entity.

8.1.2.1 PHY frame

The format of the PHY frame is presented in Figure 8-3. The PHY frame at the α-reference point includes a header, and a payload. The preamble is added to the PHY frame in the PMD, as described in clause 8.1.4.1.3. The preamble is intended for synchronization, phase-error detection and nonlinear information acquisition. It also carries some control information.

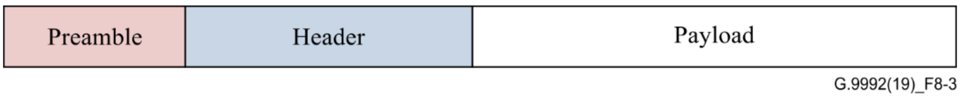


Figure 8-3 – Format of the PHY frame

All components of the PHY frame (preamble, header and the payload) consist of an integer number of UPWM symbols.

The length of the PHY-frame header is variable. The modulation order for the header shall be the same as the payload.

The payload is intended to carry one or more MPDUs and possible management information. The length of a payload may vary from frame to frame, and the payload may be of zero length, which means that a PHY frame may not include the payload.

The types of PHY frames used in this Recommendation are summarized in Table 8-1.

Table 8-1 – PHY frame types

Type	Header	Payload	Description	Reference
ID	√	None	ID frame	Clause 8.1.2.3.2.1
MSG-D	√	√	Data and management frame, including ID information.	Clause 8.1.2.3.2.2
MSG-S	√	√	Data and management frame, not including ID information.	Clause 8.1.2.3.2.3

8.1.2.2 MPDU mapping

MPDUs are passed to the PHY as an ordered sequence of bytes that are processed as an ordered string of bits from LSB to MSB within each byte. The first bit of the MPDU shall be the first transmitted bit of the payload.

8.1.2.3 PHY-frame header

The PHY frame header is composed of a common part and a variable part. The common part contains fields that are common for all PHY frame types (FTs). The variable part contains fields according to the PHY frame type. The type is indicated by the FT field. The variable part comprises a fixed length part (FTSF_F), a parity bit (PB), and a variable length part (FTSF_V). The content of the common part and the fixed length part of the variable part of the PHY frame header is protected by the parity bit, the content of the second part of the variable part of the PHY frame header is protected by an 8-bit header check sequence (HCS). The PHY frame header format is defined in Table 8-2.

Table 8-2 – PHY frame header format

Field	Octet	Bits	Description
FT	0	[2:0]	Frame type
FTSF_F		[6:3]	The first part of the frame-type specific field
PB		[7]	The parity bit
FTSF_V	var	Variable	The second part of the frame-type specific field
HCS	var	[7:0]	Header check sequence

The ordering of bits and bytes of the PFH is detailed in clause 8.1.2.3.3.

8.1.2.3.1 Common part fields

8.1.2.3.1.1 Frame type

The frame type (FT) field is a 3-bit field which indicates the type of PHY frame as described in Table 8-3.

Table 8-3 – Encoding of the FT field

Frame type	Value ($b_2b_1b_0$)
ID	000
MSG-D	001
MSG-S	010
Reserved	011-111

8.1.2.3.1.2 Header check sequence

The HCS field is intended for PHY frame verification. The HCS is an 8-bit cyclic redundancy check (CRC) and shall be computed over the FTSF_V field of the PHY-frame header in the order they are transmitted, starting with the LSB of the first field of the FTSF_V and ending with the MSB of the last field of the FTSF_V.

The HCS shall be computed using the following generator polynomial of degree 8:

$$G(x) = x^8 + x^7 + x^4 + x^3 + x + 1$$

The value of the HCS shall be the remainder after the contents (treated as a polynomial where the first input bit is associated with the highest degree, $X^{PHY_H - 17}$, where PHY_H is the header length in bits, and the last input bit is associated with X^0) of the calculation field is multiplied by x^8 and then divided by $G(x)$.

The HCS field shall be transmitted starting with the coefficient of the highest order term.

8.1.2.3.2 Variable part fields

This clause details the frame-type specific field (FTSF), a variable part of the PHY-frame header fields separately defined for each PHY-frame type.

8.1.2.3.2.1 ID PHY-frame type specific fields

Table 8-4 lists the PHY-frame header fields which are specific to the ID frame type. For the ID frame type, the FTSF_F field is composed of the ID Length field and destination ID field present indication (DPI) field; the FTSF_V field is composed of the source ID (SID) field and an optional destination ID (DID) field.

Table 8-4 – ID PHY-frame type specific fields

Field	Octet	Bits	Description	Reference
ID Length	0	[5:3]	The length of the SID and DID field	Clause 8.1.2.3.2.1.1
DPI		[6]	Destination ID field present indication	Clause 8.1.2.3.2.1.2
PB		[7]	The odd parity bit	Clause 8.1.2.3.2.1.3
SID	var	var	ID of the source node	Clause 8.1.2.3.2.1.4
DID	var	var	ID of the source node. This field only exists when DPI field is set to 1	Clause 8.1.2.3.2.1.5

8.1.2.3.2.1.1 ID Length

The ID length field shall contain the length of the ID of the source node. If the DID field is present, the length of the ID of the destination node shall also be indicated by the ID length field.

The ID length field shall be set as shown in Table 8-5.

Table 8-5 – Value of ID length

Length of ID in bits	Value ($b_2b_1b_0$)	Description
8	000	An 8-bit ID
16	001	A 16-bit ID
32	010	A 32-bit ID
48	011	A 48-bit ID
64	100	A 64-bit ID
Reserved	101-111	Reserved by ITU-T

8.1.2.3.2.1.2 Destination ID field present indication

If the destination ID field present indication (DPI) bit is set to zero, the DID field shall not be contained in the PHY-frame header. If the DPI bit is set to one, the DID field shall contain the ID of the destination nodes.

8.1.2.3.2.1.3 Parity bit

The PB field is an odd parity bit that is intended for PHY frame verification. The PB field shall be set to 1, if the count of bits in FT field, ID Length and DPI field with a value of 1 is even. The PB field shall be set to 0, if the count of bits in FT field, ID Length and DPI field with a value of 1 is odd.

8.1.2.3.2.1.4 Source ID

The SID field shall contain the ID of the source node of the PHY frame. The length of the SID is vendor discretionary, and indicated by the ID Length field.

8.1.2.3.2.1.5 Destination ID

The DID field shall contain the ID of the destination node of the PHY frame. This field only exists when DPI field is set to 1. The length of the DID shall be the same as that of the SID, and indicated by the ID Length field.

8.1.2.3.2.2 MSG-D PHY-frame type specific fields

Table 8-6 lists the PHY-frame header fields which are specific to the MSG-D frame type. For the MSG-D frame type, the FTSF_F field is composed of the ID Length field and DPI field. The FTSF_V field is composed of the SID field, an optional DID field and the PL field.

Table 8-6 – MSG-D PHY-frame type specific fields

Field	Octet	Bits	Description	Reference
ID length	0	[5:3]	The length of the SID and DID field	Clause 8.1.2.3.2.2.1
DPI		[6]	Destination ID field present indication	Clause 8.1.2.3.2.2.2
PB		[7]	The odd parity bit	Clause 8.1.2.3.2.2.3
SID	var	var	ID of the source node	Clause 8.1.2.3.2.2.4
DID	var	var	ID of the source node. This field only exists when DPI field is set to 1	Clause 8.1.2.3.2.2.5
PL	var	[7:0]	The length of the payload of this PHY frame	Clause 8.1.2.3.2.2.6

8.1.2.3.2.2.1 ID length

The ID length field shall be as described in clause 8.1.2.3.2.1.1.

8.1.2.3.2.2.2 Destination ID field present indication

The DPI field shall be as described in clause 8.1.2.3.2.1.2.

8.1.2.3.2.2.3 Parity bit

The PB field shall be as described in clause 8.1.2.3.2.1.3.

8.1.2.3.2.2.4 Source ID

The SID field shall be as described in clause 8.1.2.3.2.1.4.

8.1.2.3.2.2.5 Destination ID

The DID field shall be as described in clause 8.1.2.3.2.1.5.

8.1.2.3.2.2.6 Payload length (PL)

The PL field shall indicate the length of the payload of this PHY frame and shall contain the value of the number of bytes in the payload. It shall be represented as an 8-bit unsigned integer with valid values in the range from 00_{16} to FF_{16}.

8.1.2.3.2.3 MSG-S PHY-frame type specific fields

Table 8-7 lists the PHY-frame header fields which are specific to the MSG-S frame type. For the ID frame type, the FTSF_F field is composed of the Reserved field; the FTSF_V field is composed of the PL field.

Table 8-7 – MSG-S PHY-frame type specific fields

Field	Octet	Bits	Description	Reference
Reserved	0	[6:3]	Reserved by ITU-T (Note)	
PB		[7]	The odd parity bit	Clause 8.1.2.3.2.3.1
PL	1	[7:0]	The length of the payload of this PHY frame	Clause 8.1.2.3.2.3.2
NOTE – Bits that are reserved by ITU-T shall be set to zero by the transmitter and ignored by the receiver.				

8.1.2.3.2.3.1 Parity bit (PB)

The PB field shall be as described in clause 8.1.2.3.2.1.3.

8.1.2.3.2.3.2 Payload length

The PL field shall be as described in clause 8.1.2.3.2.2.6.

8.1.3 Physical medium attachment sublayer

The functional model of the PMA is presented in Figure 8-4. It is intended to describe in more detail the PMA functional block presented in Figure 8-1.

In the transmit direction, the incoming PHY frame (except for preamble) at the α-reference point has a format as defined in clause 8.1.2. The header and payload are segmented into an integer number of symbol frames as described in clauses 8.1.3.1 and 8.1.3.2. The obtained symbol frames of the header and the payload are submitted to the PMD (at the δ-reference point) for modulation and transmission over the medium.

In the receive direction, the received symbol frames are concatenated and then submitted to the α-reference point for further processing in the PCS.

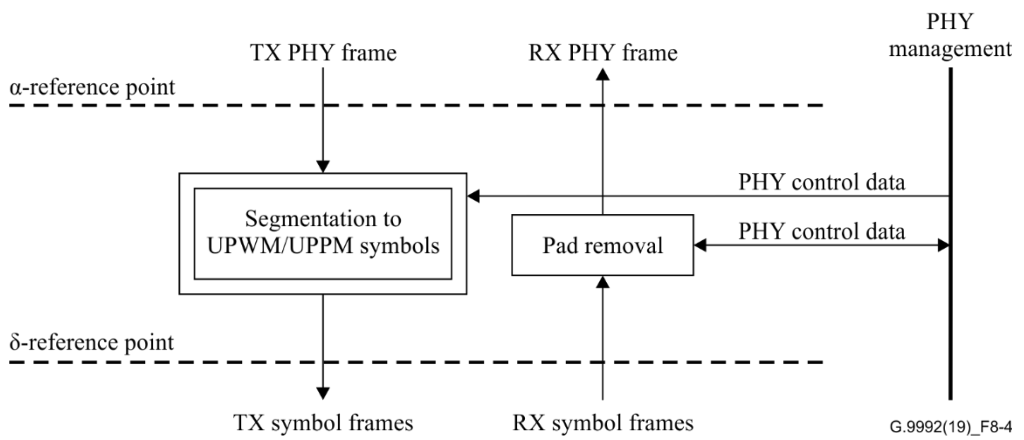


Figure 8-4 – Functional model of PMA sublayer

8.1.3.1 Segmentation to UPWM symbols

The incoming TX PHY frame shall be segmented into symbol frames in sequence according to the modulation order *m*. The number of bits in each symbol frames shall be *b*. TX PHY frame segmentation is illustrated in Figure 8-5.

If the modulation order is the integral power of 2, each symbol frame will be modulated to generate one UPWM symbols. The incoming TX PHY frame shall be segmented in sequence, the frame shall contain b bits, where $b = log_2 m$. N_{sf} symbol frames are obtained, and each of the N_{sf}–1 symbol frames shall contain b bits, while the last symbol frame may contain b bits or less than b bits. If the last symbol frame contains less than b bits, it shall be padded with zeros.

If the modulation order is not the integral power of 2, each symbol frame will be modulated to generate two UPWM symbols. The incoming TX PHY frame shall be segmented in sequence, and the first frame shall contain the first b bits, and the second frame shall contain the second b bits and so on, until the last symbol frame, where $b = floor(log_2 m^2)$. N_{sf} symbol frames are obtained, and each of the first N_{sf}–1 symbol frames shall contain b bits, while the last symbol frame may contain b bits or less than b bits. If the last symbol frame contains less than b bits, it shall be padded with zeros.

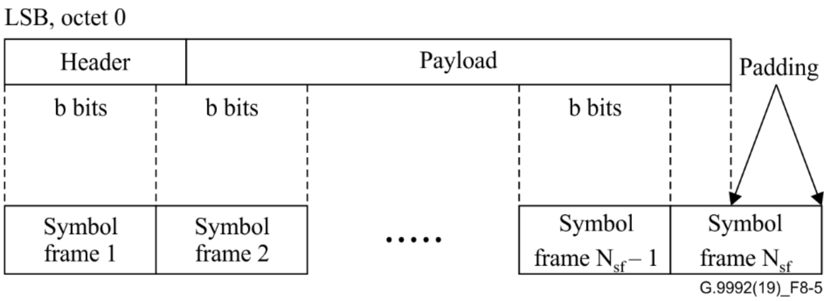


Figure 8-5 – TX PHY frame segmentation for UPWM

8.1.3.2 Segmentation to UPPM symbols

The incoming TX PHY frame shall be segmented into even number of symbol frames in sequence according to the following parameters:

1) DC D_i either determined by the m-DC mapper (see clause 8.1.4.1.1) or a pre-defined value, which is vendor discretionary;
2) valid data region information (see clause 8.1.4.2.3.2) of a UPPM waveform segment.

TX PHY frame segmentation is illustrated in Figure 8-6.

The incoming TX PHY frame shall be segmented in sequence, $2N_{sf1} + 2$ symbol frames are obtained. If the symbol frame is the first symbol frame (i.e., symbol frame 1), it shall contain $(N_{ppm} – 2) \times \log_2 M$ bits, where N_{ppm} and M are parameters determined by valid data region information (see clause 8.1.4.2.3.2) of a UPPM waveform segment, the second symbol frame shall contain $N_{ppm} \times \log_2 M$ bits. Symbol frame No. 2n + 1 and symbol frame No. 2n + 2 (n ≥ 1) shall contain the same number of bits. If symbol frame No. 1 contains less than $(N_{ppm} – 2) \times \log_2 M$ bits, both symbol No. 1 and No. 2 shall be padded with zeros. If only symbol frame No. 2 contains less than $N_{ppm} \times \log_2 M$ bits, it shall be padded with zeros. If symbol frame No. 2n + 1 (n ≥ 1) contains less than $N_{ppm} \times \log_2 M$ bits, both symbol No. 2n + 1 and No. 2n + 2 shall be padded with zeros. If only symbol frame No. 2n + 2 contains less than $N_{ppm} \times \log_2 M$ bits, it shall be padded with zeros.

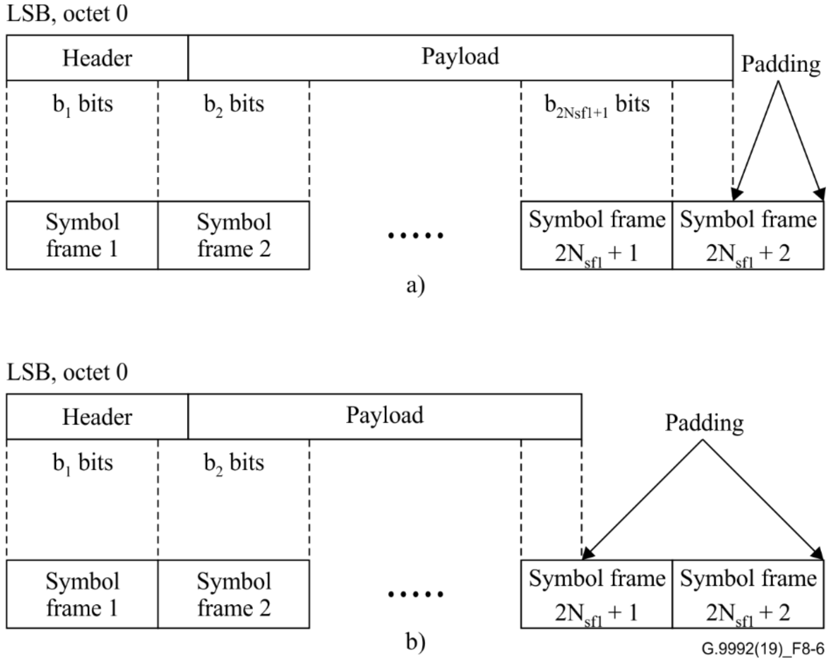


Figure 8-6 – TX PHY frame segmentations for UPPM

8.1.4 Physical medium dependent sublayer

The functional model of the physical medium dependent (PMD) is presented in Figure 8-7. In the transmit direction, the m-DC mapper maps the incoming TX1 symbol frames to m-ary DC sequences, as specified in clause 8.1.4.1.1. If only the low speed channel is enabled, the duty cycle (DC) sequences of the UPWM preamble and the DC sequences obtained from the m-DC mapping of the incoming TX1 symbol frames are fed into a UPWM modulator where non-flickering signals are generated as described in clause 8.1.4.1.2. After that, the generated UPWM signals, which contain the preamble, header and payload (as shown in Figure 8-3), are fed into a digital light emitting diode (LED) driver, and are transmitted using visible light. Parameters of the preamble are determined by the PHY management. If two channels are enabled, the DC sequences of the prepending preamble and the DC sequences obtained from the m-DC mapping of the incoming TX1 symbol frames are fed into the UPPM modulation selector.

The incoming TX2 symbol frames are fed into a UPPM modulator where non-flickering signals are generated as described in clause 8.1.4.2.2. The UPPM modulation selector determines the UPPM modulation scheme. The DC of the final UPPM symbol may be determined in accordance with the current m-ary DC generated by the m-DC mapper or by a predefined DC. The preamble and delimiters signals are fed into the UPPM modulator to finalize the generation of the transmit signal, which is then fed into an LED driver and transmitted using visible light.

NOTE – Either TX1 or TX2 symbol frames may both exist or exist by themselves depending on the enabled channels. PHY management also receives the following parameters from the PMD sub-layer to assist PMA sub-layer in carrying out its function, that is, the output of m-DC mapper, VPPM modulation order or pre-defined DC value, and UPPM preamble/delimiter/valid data timing information.

Frames are output on to the medium without inter-frame gaps.

In the receive direction, a camera with a frame rate of f_c is employed to detect and record the optical signal. The receiver exposure duration can be set to T_e to receive TX1 symbol frames from low-speed channel only. The receiver exposure duration can be set to T_e' to receive TX1 and TX2 symbol frames from both low-speed and high-speed channels or to receive TX2 symbol frames only from the high-speed channel. When the exposure is set to T_e', if at least two UPPM waveform segments are received in a captured video frame, data from the high-speed channel can be obtained and a DC generated by a m-DC mapper from the low-speed channel may also be received. If at least two UPPM waveform segments cannot be received, the exposure duration may be changed to T_e to detect the optical signal to receive symbol frames in low-speed channel only. With the help of the preamble detection and PI extraction, the undersampled-recorded UPWM data from low-speed channel are compensated and demodulated. If at least two UPPM waveform segments are received in a captured video frame, with the help of preamble and delimiter detection, the recorded stripes from high-speed channel are processed and the obtained V*M*PPM (e.g., V2PPM, V4PPM or V8PPM) signal are processed and demodulated, the DC mapper generated DCs from the low-speed channel may also be obtained if both high speed and low speed channels are enabled, then processed and demodulated. The recovered symbol frames from either the low-speed or the high-speed channel are transferred to the PMA via δ-reference point. The preamble are processed and the processing result are passed to the PHY management entity.

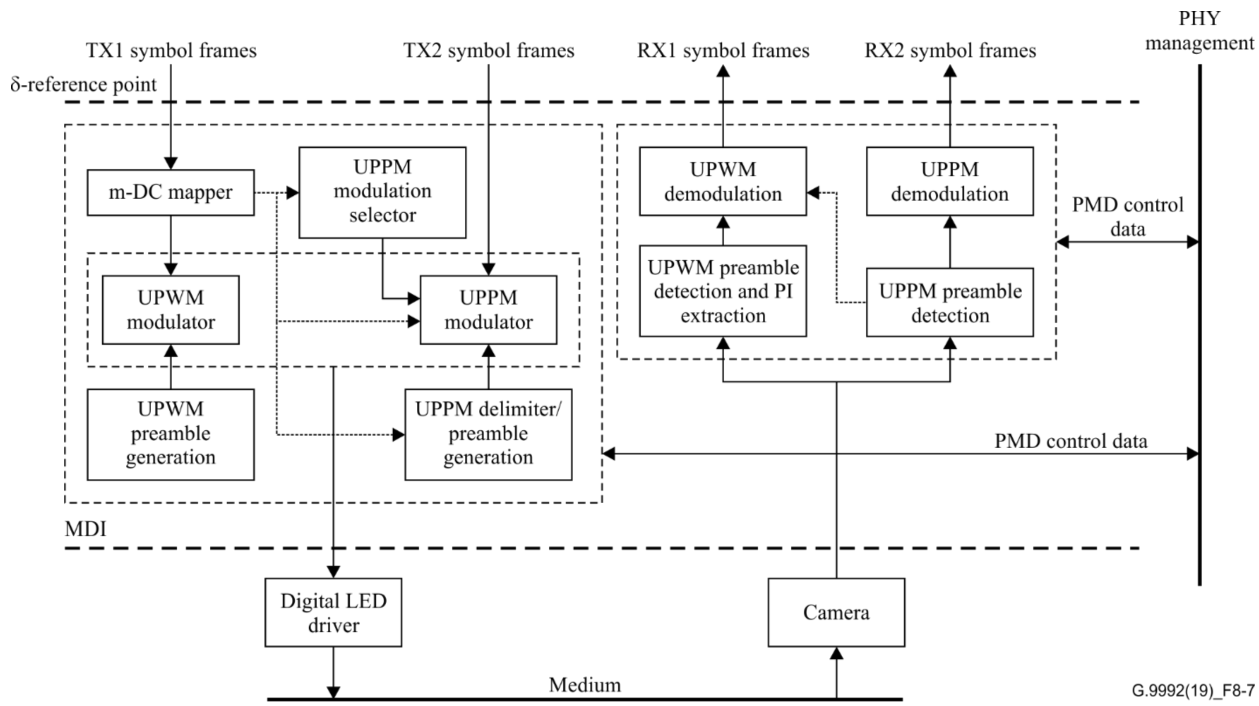


Figure 8-7 – Functional model of the PMD

8.1.4.1 UPWM modulation

8.1.4.1.1 *m*-DC mapping

m-DC mapping associates every group of bits into one or two DCs. Each incoming group of b bits $\{d_{b-1}, d_{b-2}, \dots, d_0\}$ shall be associated with one or two specific DC values as described in this clause. Support of all the specified modulation orders (m = 2, 3, 4, 6, 8, 12, 16, 23, 32) shall be mandatory at both the transmitter and the receiver. The relationship between valid m and b is described in Table 8-8. Each group of bits $\{d_{b-1}, d_{b-2}, \dots d_0\}$ shall be mapped on to the m-DC mapper with the LSB bit, d_0, first.

Table 8-8 – Relationship between *m* and *b*

m	*b*	*Number of associated DCs for a specific 'b'*
2	1	1
3	3	2
4	2	1
6	5	2
8	3	1
12	7	2
16	4	1
23	9	2
32	5	1

When transmitting a PHY frame, the transmitter shall first obtain DCs for preamble, header and payload (if payload exists), respectively, which may be generated with one or more specific modulation orders.

NOTE – The payload may be not present in some PHY frames, for example, in the ID frame.

8.1.4.1.1.1 *m*-DC mapping when *m* is the integral power of 2

If the modulation order m is the integral power of 2, each incoming group of b bits $\{d_{b-1}, d_{b-2}, \ldots, d_0\}$ shall be associated with one specific value of DC, where $b = log_2 m$. DC mapping for m = 2 is presented in Table 8-9.

Table 8-9 – Mapping for *m* = 2

Bit d_0	DC
0	33.3%
1	66.7%

DC mapping for m = 4 is presented in Table 8-10.

Table 8-10 – Mapping for *m* = 4

Bit d_1	Bit d_0	DC
0	0	20%
0	1	40%
1	0	60%
1	1	80%

DC mapping for m = 8 is presented in Table 8-11.

Table 8-11 – Mapping for *m* = 8

Bit d_2	Bit d_1	Bit d_0	DC
0	0	0	11.1%
0	0	1	22.2%
0	1	0	33.3%
0	1	1	44.4%
1	0	0	55.6%
1	0	1	66.7%
1	1	0	77.8%
1	1	1	88.9%

DC mapping for *m* = 16 is presented in Table 8-12.

Table 8-12 – Mapping for *m* = 16

Bit d_3	Bit d_2	Bit d_1	Bit d_0	DC
0	0	0	0	5.9%
0	0	0	1	11.8%
0	0	1	0	17.6%
0	0	1	1	23.5%
0	1	0	0	29.4%
0	1	0	1	35.3%
0	1	1	0	41.2%
0	1	1	1	47.1%
1	0	0	0	52.9%
1	0	0	1	58.8%
1	0	1	0	64.7%
1	0	1	1	70.6%
1	1	0	0	76.5%
1	1	0	1	82.4%
1	1	1	0	88.2%
1	1	1	1	94.1%

DC mapping for *m* = 32 is presented in Table 8-13.

Table 8-13 – Mapping for *m* = 32

Bit d_4	Bit d_3	Bit d_2	Bit d_1	Bit d_0	DC
0	0	0	0	0	3.0%
0	0	0	0	1	6.1%
0	0	0	1	0	9.1%
0	0	0	1	1	12.1%
0	0	1	0	0	15.2%
0	0	1	0	1	18.2%

Table 8-13 – Mapping for *m* = 32

Bit d_4	Bit d_3	Bit d_2	Bit d_1	Bit d_0	DC
0	0	1	1	0	21.2%
0	0	1	1	1	24.2%
0	1	0	0	0	27.3%
0	1	0	0	1	30.3%
0	1	0	1	0	33.3%
0	1	0	1	1	36.4%
0	1	1	0	0	39.4%
0	1	1	0	1	42.4%
0	1	1	1	0	45.5%
0	1	1	1	1	48.5%
1	0	0	0	0	51.5%
1	0	0	0	1	54.5%
1	0	0	1	0	57.6%
1	0	0	1	1	60.6%
1	0	1	0	0	63.6%
1	0	1	0	1	66.7%
1	0	1	1	0	69.7%
1	0	1	1	1	72.7%
1	1	0	0	0	75.8%
1	1	0	0	1	78.8%
1	1	0	1	0	81.8%
1	1	0	1	1	84.8%
1	1	1	0	0	87.9%
1	1	1	0	1	90.9%
1	1	1	1	0	93.9%
1	1	1	1	1	97.0%

8.1.4.2.1.2 *m*-DC mapping when *m* is non-integral power of 2

If the modulation order m is not the integral power of 2, each incoming group of b bits $\{d_{b-1}, d_{b-2}, \ldots, d_0\}$ shall be associated with two specific value of DC according to the mapping rules specified in this clause, where $b = floor(log_2 m^2)$. Each incoming group of b bits shall be modulated to two consecutive UPWM symbols. DC I and DC II shall be used to generate the two UPWM symbols respectively. In the mapping rules, 2^b of the m^2 combinations of DCs are adopted.

DC mapping for *m* = 3 is presented in Table 8-14.

Table 8-14 – Mapping for m = 3

Bit d_2	Bit d_1	Bit d_0	DC *(I)*	DC *(II)*
0	0	0	25%	25%
0	0	1	25%	50%
0	1	0	25%	75%
0	1	1	50%	25%
1	0	0	50%	50%
1	0	1	50%	75%
1	1	0	75%	25%
1	1	1	75%	50%

DC mapping for m = 6 is presented in Table 8-15.

Table 8-15 – Mapping for m = 6

Bit d_4	Bit d_3	Bit d_2	Bit d_1	Bit d_0	DC *(I)*	DC *(II)*
0	0	0	0	0	14.3%	14.3%
0	0	0	0	1	14.3%	28.6%
0	0	0	1	0	14.3%	42.9%
0	0	0	1	1	14.3%	57.1%
0	0	1	0	0	14.3%	71.4%
0	0	1	0	1	14.3%	85.7%
0	0	1	1	0	28.6%	14.3%
0	0	1	1	1	28.6%	28.6%
0	1	0	0	0	28.6%	42.9%
0	1	0	0	1	28.6%	57.1%
0	1	0	1	0	28.6%	71.4%
0	1	0	1	1	28.6%	85.7%
0	1	1	0	0	42.9%	14.3%
0	1	1	0	1	42.9%	28.6%
0	1	1	1	0	42.9%	42.9%
0	1	1	1	1	42.9%	57.1%
1	0	0	0	0	42.9%	71.4%
1	0	0	0	1	42.9%	85.7%
1	0	0	1	0	57.1%	14.3%
1	0	0	1	1	57.1%	28.6%
1	0	1	0	0	57.1%	42.9%
1	0	1	0	1	57.1%	57.1%
1	0	1	1	0	57.1%	71.4%
1	0	1	1	1	57.1%	85.7%
1	1	0	0	0	71.4%	14.3%
1	1	0	0	1	71.4%	28.6%
1	1	0	1	0	71.4%	42.9%

Table 8-15 – Mapping for *m* = 6

Bit d_4	Bit d_3	Bit d_2	Bit d_1	Bit d_0	DC *(I)*	DC *(II)*
1	1	0	1	1	71.4%	57.1%
1	1	1	0	0	71.4%	71.4%
1	1	1	0	1	71.4%	85.7%
1	1	1	1	0	85.7%	14.3%
1	1	1	1	1	85.7%	28.6%

DC mapping for *m* = 12 is presented in Table 8-16.

Table 8-16 – Mapping for *m* = 12

Bits $d_6\ d_5\ d_4\ d_3\ d_2\ d_1\ d_0$	DC (I)	DC (II)	Bits $d_6\ d_5\ d_4\ d_3\ d_2\ d_1\ d_0$	DC (I)	DC (II)
0000000	7.7%	7.7%	1000000	46.2%	38.5%
0000001	7.7%	15.4%	1000001	46.2%	46.2%
0000010	7.7%	23.1%	1000010	46.2%	53.8%
0000011	7.7%	30.8%	1000011	46.2%	61.5%
0000100	7.7%	38.5%	1000100	46.2%	69.2%
0000101	7.7%	46.2%	1000101	46.2%	76.9%
0000110	7.7%	53.8%	1000110	46.2%	84.6%
0000111	7.7%	61.5%	1000111	46.2%	92.3%
0001000	7.7%	69.2%	1001000	53.8%	7.7%
0001001	7.7%	76.9%	1001001	53.8%	15.4%
0001010	7.7%	84.6%	1001010	53.8%	23.1%
0001011	7.7%	92.3%	1001011	53.8%	30.8%
0001100	15.4%	7.7%	1001100	53.8%	38.5%
0001101	15.4%	15.4%	1001101	53.8%	46.2%
0001110	15.4%	23.1%	1001110	53.8%	53.8%
0001111	15.4%	30.8%	1001111	53.8%	61.5%
0010000	15.4%	38.5%	1010000	53.8%	69.2%
0010001	15.4%	46.2%	1010001	53.8%	76.9%
0010010	15.4%	53.8%	1010010	53.8%	84.6%
0010011	15.4%	61.5%	1010011	53.8%	92.3%
0010100	15.4%	69.2%	1010100	61.5%	7.7%
0010101	15.4%	76.9%	1010101	61.5%	15.4%
0010110	15.4%	84.6%	1010110	61.5%	23.1%
0010111	15.4%	92.3%	1010111	61.5%	30.8%
0011000	23.1%	7.7%	1011000	61.5%	38.5%
0011001	23.1%	15.4%	1011001	61.5%	46.2%
0011010	23.1%	23.1%	1011010	61.5%	53.8%

Table 8-16 – Mapping for $m = 12$

Bits $d_6\ d_5\ d_4\ d_3\ d_2\ d_1\ d_0$	DC (I)	DC (II)	Bits $d_6\ d_5\ d_4\ d_3\ d_2\ d_1\ d_0$	DC (I)	DC (II)
0011011	23.1%	30.8%	1011011	61.5%	61.5%
0011100	23.1%	38.5%	1011100	61.5%	69.2%
0011101	23.1%	46.2%	1011101	61.5%	76.9%
0011110	23.1%	53.8%	1011110	61.5%	84.6%
0011111	23.1%	61.5%	1011111	61.5%	92.3%
0100000	23.1%	69.2%	1100000	69.2%	7.7%
0100001	23.1%	76.9%	1100001	69.2%	15.4%
0100010	23.1%	84.6%	1100010	69.2%	23.1%
0100011	23.1%	92.3%	1100011	69.2%	30.8%
0100100	30.8%	7.7%	1100100	69.2%	38.5%
0100101	30.8%	15.4%	1100101	69.2%	46.2%
0100110	30.8%	23.1%	1100110	69.2%	53.8%
0100111	30.8%	30.8%	1100111	69.2%	61.5%
0101000	30.8%	38.5%	1101000	69.2%	69.2%
0101001	30.8%	46.2%	1101001	69.2%	76.9%
0101010	30.8%	53.8%	1101010	69.2%	84.6%
0101011	30.8%	61.5%	1101011	69.2%	92.3%
0101100	30.8%	69.2%	1101100	76.9%	7.7%
0101101	30.8%	76.9%	1101101	76.9%	15.4%
0101110	30.8%	84.6%	1101110	76.9%	23.1%
0101111	30.8%	92.3%	1101111	76.9%	30.8%
0110000	38.5%	7.7%	1110000	76.9%	38.5%
0110001	38.5%	15.4%	1110001	76.9%	46.2%
0110010	38.5%	23.1%	1110010	76.9%	53.8%
0110011	38.5%	30.8%	1110011	76.9%	61.5%
0110100	38.5%	38.5%	1110100	76.9%	69.2%
0110101	38.5%	46.2%	1110101	76.9%	76.9%
0110110	38.5%	53.8%	1110110	76.9%	84.6%
0110111	38.5%	61.5%	1110111	76.9%	92.3%
0111000	38.5%	69.2%	1111000	84.6%	7.7%
0111001	38.5%	76.9%	1111001	84.6%	15.4%
0111010	38.5%	84.6%	1111010	84.6%	23.1%
0111011	38.5%	92.3%	1111011	84.6%	30.8%
0111100	46.2%	7.7%	1111100	84.6%	38.5%
0111101	46.2%	15.4%	1111101	84.6%	46.2%
0111110	46.2%	23.1%	1111110	84.6%	53.8%
0111111	46.2%	30.8%	1111111	84.6%	61.5%

For $m = 23$, each incoming $b = 9$ bits are represented by a value (Value_Bits) from 0 to 511. The DC I and DC II shall be calculated as presented in Table 8-17 and Table 8-18.

Table 8-17 – Mapping for *m* = 23 (DC I)

floor (Value_Bits/23)	**DC *(I)***
0	4.2%
1	8.3%
2	12.5%
3	16.7%
4	20.8%
5	25.0%
6	29.2%
7	33.3%
8	37.5%
9	41.7%
10	45.8%
11	50.0%
12	54.2%
13	58.3%
14	62.5%
15	66.7%
16	70.8%
17	75.0%
18	79.2%
19	83.3%
20	87.5%
21	91.7%
22	95.8%

Table 8-18 – Mapping for *m* = 23 (DC II)

mod (Value_Bits, 23)	**DC *(II)***
0	4.2%
1	8.3%
2	12.5%
3	16.7%
4	20.8%
5	25.0%
6	29.2%
7	33.3%
8	37.5%

Table 8-18 – Mapping for *m* = 23 (DC II)

mod (Value_Bits, 23)	**DC *(II)***
9	41.7%
10	45.8%
11	50.0%
12	54.2%
13	58.3%
14	62.5%
15	66.7%
16	70.8%
17	75.0%
18	79.2%
19	83.3%
20	87.5%
21	91.7%
22	95.8%

8.1.4.1.2 UPWM modulator

The UPWM modulator shall generate a UPWM symbol for an incoming DC, for example, once a DC D_i is received, a UPWM symbol S_i shall be generated.

The UPWM modulator consists of the following major parts: complementary operation, PWM segment generation, repetition and concatenation. The incoming signal to the modulator in the present frame with an index i, is a DC value generated by the m-DC mapping module, as described in clause 8.1.4.1, or the preamble generator, as described in clause 8.1.4.1.3. The DC value D_i and the complementary DC value$1-D_i$ are used for generating two PWM waveform segments respectively. The two PWM waveform segments are concatenated and duplicated to form a UPWM symbol S_i. The functional diagram of an UPWM modulator is presented in Figure 8-8.

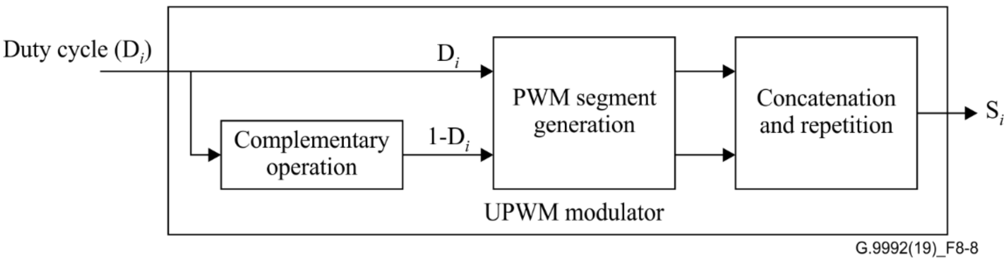


Figure 8-8 – Functional diagram of the UPWM modulator

8.1.4.1.2.1 Complementary operation

For a given D, the complementary operation is defined as: 1-D. The complementary DC $1-D_i$ shall be obtained by imposing the complementary operation on the incoming DC D_i.

8.1.4.1.2.2 PWM segment generation

Two segments of PWM waveform shall be generated using the input DC D_i and the complementary DC 1-D_i, respectively. Each segment of PWM waveform shall have the same duration of T_s, and shall contain multiple basic PWM cycles that have a duration of T_p and a DC of D_i or 1-D_i.

Particularly, T_s shall be equal to T_c / (2k), where T_c is the reciprocal of the camera's frame rate f_c, which shall be fixed to 120 fps, k is an integer ($k \geq 1$) to make sure T_s is less than 5 ms. T_p shall be lower or equal to T_e / 5, which means that when a camera is used to shoot video of an LED which is emitting UPWM signal, the camera could receive at least 10 basic PWM cycles during each exposure period T_e.

NOTE – If a return channel exists, the frame rate of the camera of the receiver node can be adjusted on demand. The mechanism for frame rate negotiation is for further study.

8.1.4.1.2.3 Concatenation and repetition

The two segments of PWM waveform, each of which has a duration of T_s and a DC of D_i and 1-D_i respectively, shall be concatenated sequentially, and then shall be repeated k times. Finally, a UPWM symbol with a duration of T_c shall be formed. Each UPWM symbol consists of k segments of PWM waveform with a DC of D_i, and k segments of PWM waveform with a DC of 1-D_i. Each PWM waveform segment shall have the same duration of T_c / (2k), and each PWM waveform segment with a DC of D_i shall be followed by a PWM waveform segment with a DC of 1-D_i.

The *2k* PWM segments forms a UPWM symbol with a duration of T_c. The generated UPWM symbols are then transmitted via the LED of the transmitter.

8.1.4.1.3 UPWM preamble signal

The preamble is prepended to every PHY frame defined in clause 8.1.2.1. It is intended to assist the receiver in detecting phase error, synchronizing to the frame boundaries, and acquiring the nonlinear information and physical layer parameters such as modulation order.

Figure 8-9 shows the general structure of the preamble. The preamble is composed of three sections, both the first section and the third section include one UPWM symbol, while the second section includes m UPWM symbols, where m is the modulation order for the following part of the PHY frame.

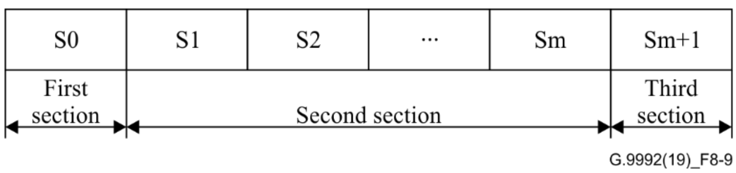


Figure 8-9 – The general structure of the preamble

The DCs for generating each UPWM symbol of the preamble for each modulation order are presented in Table 8-19. The UPWM symbols of preamble shall be generated as specified in clause 8.1.4.2.

Table 8-19 – The structure of the preamble

	First section	Second section	Third section
m=2	0%	33.3%, 66.7%	100%
m=3	0%	25%, 50%, 75%	100%
m=4	0%	20%, 40%, 60%, 80%	100%
m=6	0%	14.3%, 28.6%, 42.9%, 57.1%, 71.4%, 85.7%	100%
m=8	0%	11.1%, 22.2%, 33.3%, 44.4%, 55.6%, 66.7%, 77.8%, 88.9%	100%
m=12	0%	7.7%, 15.4%, 23.1%, 30.8%, 38.5%, 46.2%, 53.8%, 61.5%, 69.2%, 76.9%, 84.6%, 92.3%	100%
m=16	0%	5.9%, 11.8%, 17.6%, 23.5%, 29.4%, 35.3%, 41.2%, 47.1%, 52.9%, 58.8%, 64.7%, 70.6%, 76.5%, 82.4%, 88.2%, 94.1%	100%
m=23	0%	4.2%, 8.3%, 12.5%, 16.7%, 20.8%, 25.0%, 29.2%, 33.3%, 37.5%, 41.7%, 45.8%, 50.0%, 54.2%, 58.3%, 62.5%, 66.7%, 70.8%, 75.0%, 79.2%, 83.3%, 87.5%, 91.7%, 95.8%	100%
m=32	0%	3.0%, 6.1%, 9.1%, 12.1%, 15.2%, 18.2%, 1.2%, 24.2%, 27.3%, 30.3%, 33.3%, 36.4%, 39.4%, 42.4%, 45.5%, 48.5%, 51.5%, 54.5%, 57.6%, 60.6%, 63.6%, 66.7%, 69.7%, 72.7%, 75.8%, 78.8%, 81.8%, 84.8%, 87.9%, 90.9%, 93.9%, 97.0%	100%

8.1.4.2 UPPM modulation

The UPPM modulator shall generate UPPM symbols for incoming symbol frames from only the high speed channel or incoming symbol frames from both the high speed and the low speed channels, depending on the enabled channels.

For the generation of each UPPM symbol, the transmitter shall first determine a modulation scheme according to a DC D_i. If only the high speed channel is enabled, the DC D_i shall be a pre-defined value, which is vendor discretionary. If both high speed and low speed channels are enabled, the DC D_i shall be generated by the m-DC mapper according to the incoming symbol frames from the low speed channel.

Subsequently, according to the determined modulation scheme, the transmitter shall generate a UPPM symbol which shall contain even number of waveform segments with equal duration. The TX symbol frame of the high speed channel shall be divided into two parts which shall be conveyed by the first two adjacent waveform segments (i.e., the first and the second waveform segments) respectively. The following waveform segments are repetition of the first and the second waveform segments. All segments with an odd number shall be a waveform with the determined modulation scheme and an average DC of D_i. All segments with an even number shall be a waveform with the same determined modulation scheme and an average DC of $1-D_i$.

8.1.4.2.1 Determination of modulation schemes for UPPM

The modulation schemes for UPPM waveform segments shall be determined by the corresponding DC D_i generated by the m-DC mapper or the predefined DC D_i according to the following criteria:

– If D_i falls within the interval of (0% ~ 12.5%] or [87.5% ~ 100%), V8PPM shall be adopted;

– If D_i falls within the interval of (12.5% ~ 25%] or [75% ~ 87.5%), V4PPM shall be adopted;

– If D_i falls within the interval of (25% ~ 75%), V2PPM shall be adopted.

8.1.4.2.1.1 V*M*PPM modulation scheme

Each generated symbol with different modulation schemes shall have a constant time duration of T_{ppm}, and contain only one positive square pulse if the DC of this symbol is lower than or equals to 50%, or one negative square pulse if the DC of this symbol is higher than 50%. Each generated symbol with different modulation schemes shall be divided into 2, 4, or 8 time slots depending on the determined modulation scheme, and one square pulse shall be placed in one of the adjacent time slots to represent the 1, 2 or 3 bits base-band information data if V2PPM, V4PPM or V8PPM is adopted, respectively.

If the DC D_i or D_i', which is lower than or equals to 50%, varies within the defined rage, the pulse rising edge shall be fixed at the beginning of one of the time slots, while the pulse width may shrink by shifting the falling edge left or right. Otherwise, if the DC D_i or D_i', which is larger than 50%, varies within the defined rage, the symbol shall be generated by flipping a symbol generated by a certain modulation scheme determined by D_i or D_i' with a complementary DC of 1-D_i or 1-D_i' in the up-down direction.

An example of the V*M*PPM modulation is presented in Figure 8-9.1.

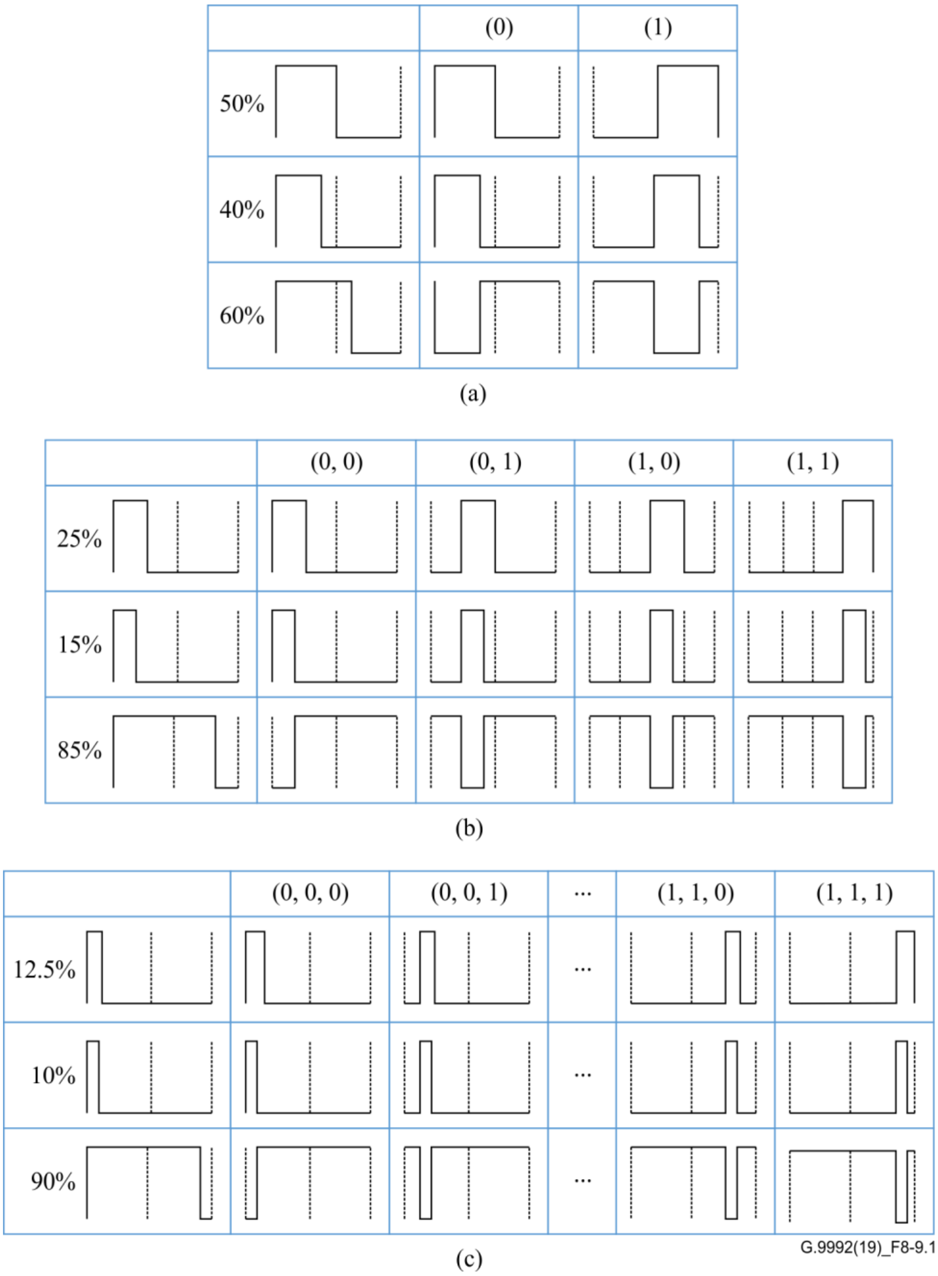


Figure 8-9.1 – Examples of waveforms with different duty cycles of (a) V2PPM, (b) V4PPM, and (c) V8PPM

8.1.4.2.2 UPPM modulator

The UPPM modulator consists of the following major parts: complementary operation, UPPM waveform segment generation, repetition and concatenation. There shall be four inputs for the UPPM modulator, which are UPPM DC, a selected V*M*PPM scheme (e.g., V2PPM, V4PPM or V8PPM), TX symbol frames of the high speed channel and UPPM delimiter/preamble which is described in clause 8.1.4.2.3. The functional diagram of a UPPM modulator is presented in Figure 8-10.

In order to provide compatibility with UPWM and support non-flickering communication, the total number of UPPM waveform segments with odd number in a UPPM symbol shall be equal to that of the UPPM waveform segments with even number during the receiver sampling period.

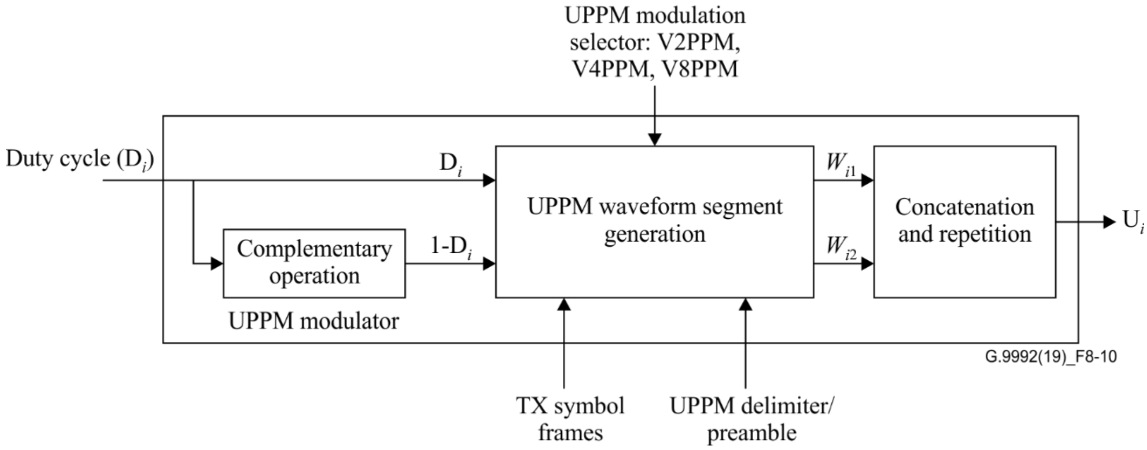


Figure 8-10 – Functional diagram of the UPPM modulator

8.1.4.2.2.1 Complementary operation

See clause 8.1.4.1.2.1.

8.1.4.2.2.2 UPPM waveform segment generation

Two segments of UPPM waveform (W_{i1}, W_{i2}) shall be generated with five inputs: DC D_i, the complementary DC 1-D_i, a selected V*M*PPM scheme (see clause 8.1.4.2.1.1), TX symbol frames and UPPM delimiter/preamble (see clause 8.1.4.2.3). W_{i1}, W_{i2} shall have the same duration of T_s and complementary average DC as determined by D_i and 1-D_i. W_{i1}, W_{i2} shall also have the same structure: a start delimiter region (SDR), a valid data region (VDR) and an end delimiter region (EDR), as shown in Figure 8-11. In addition, each region in W_{i1}, W_{i2} shall use the same frequency, respectively.

NOTE – It is assumed that a camera captures the same number of pulses for both Wi1 and Wi2 during the same sampling period.

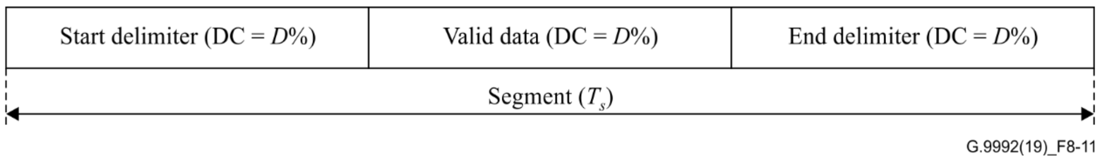


Figure 8-11 – Structure of a UPPM waveform segment

The start delimiter and end delimiter are transmitted in the SDR and EDR, respectively, to facilitate the detection of the boundary of a waveform segment. In addition, the start delimiter also indicates the modulation scheme used in this waveform segment.

The VDRs of the two segments of UPPM waveform (W_{i1}, W_{i2}) in Figure 8-11 shall be generated by an incoming TX symbol frame. The preamble may be prepended before the valid data waveform and transmitted in the VDR if the TX symbol frame is the first symbol frame of the PHY frame.

The format of start delimiter, preamble, valid data and end delimiter waveforms shall be as specified in clause 8.1.4.2.3.

8.1.4.2.2.3 Concatenation and repetition

The two segments of UPPM waveform (W_{i1}, W_{i2}), each of which has a duration of $T_s = T_c /(2k)$ and an average DC of D_i and 1-D_i respectively, shall be concatenated sequentially, and then shall be repeated k times. Finally, a UPPM symbol with a duration of T_c shall be formed. Each UPPM symbol consists of k segments of UPPM waveform with an average DC of D_i, and k segments of UPPM waveform with an average DC of 1-D_i. Each UPPM waveform segment with an average DC of D_i shall be followed by a UPPM waveform segment with an average DC of 1-D_i.

The $2k$ UPPM waveform segments forms a UPPM symbol with a duration of T_c. The generated UPPM symbols are then transmitted via the LED of the transmitter.

8.1.4.2.3 UPPM preamble/delimiter/valid data waveforms

8.1.4.2.3.1 Start delimiter

Each start delimiter of W_{i1}, W_{i2} shall comprise two sections, as shown in Figure 8-12. The first section shall be used to specify the starting position of the UPPM waveform segment, while the second section shall indicate the modulation scheme employed to modulate the incoming symbol frame and generate the valid data waveform. As shown in Figure 8-12, the average DC of both sections shall be equal to D%, which shall be identical to the average DC of the whole UPPM waveform segment (D_i or 1-D_i). The first section of the start delimiter shall be a section of PWM waveform with a duration of T_{ppm}, and the PWM cycle of the PWM pulse T_{appm}. T_{appm} shall be shorter than $T_e'/3$, where T_e' is the exposure duration for receiving UPPM symbol, to ensure that the receiver can receive at least 3 V*M*PPM symbols during each exposure period T_e, guaranteeing a stripe with a brightness of D% can be captured.

The second section shall consist of two V2PPM symbols, each of which shall have the same average DC of D% and the same duration of T_{ppm}.

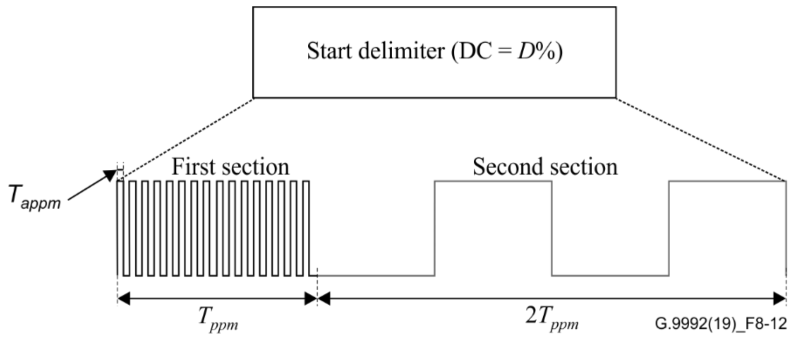


Figure 8-12 –An example of the structure of start delimiter

All valid values for the second section and the corresponding modulation schemes used to generate the valid data waveform in the valid data region that follows shall be as specified in Table 8-20.

Table 8-20 – Modulation order indication

Data in the second section	Modulation schemes used in the following valid data region
01	V2PPM
00	V4PPM
11	V8PPM

8.1.4.2.3.2 Valid data

The incoming symbol frame shall be divided into two parts. If the incoming symbol frame is not the first symbol frame of a PHY frame, these two parts shall have the same number of bits: $N_{ppm} \times \log_2 M$, where $N_{ppm} = (T_s – 4T_{ppm}) / T_{ppm}$. If the incoming symbol frame is the first symbol frame of a PHY frame, the second part shall have $2 \times \log_2 M$ bits more than the first part. The first part of the incoming symbol frame shall be mapped to V*M*PPM symbols which form the valid data of the UPPM waveform segment W_{i1}. The second part of the incoming symbol frame shall be mapped to V*M*PPM symbols which form the valid data of the UPPM waveform segment W_{i2} (see clause 8.1.4.2.1.1). There shall be integer number of V*M*PPM symbols in a valid data region.

8.1.4.2.3.3 End delimiter

An end delimiter waveform shall be inserted following the valid data waveform to specify the ending position of this UPPM waveform segment as presented in Figure 8-11. The waveform in this region shall be the same as the waveform in the first ^{t} section of the start delimiter with the same average DC D%, T_{ppm} and T_{appm}.

8.1.4.2.3.4 UPPM preamble signal

The preamble is prepended to every PHY frame defined in clause 8.1.2.1. It is intended to assist the receiver in detecting the start of a PHY frame.

The preamble shall be a section of PWM waveform, which shares the same parameter of the PWM waveform in the first section of the start delimiter except a duration of $2T_{ppm}$.

8.1.5 PSD mask specifications

No PSD mask is defined by this Recommendation since the power required to drive the emitting device may differ between implementations.

8.1.6 Electrical specifications

8.1.6.1 Transmit clock tolerance

The tolerance of the transmit clock shall not exceed ±50 ppm, including aging.

8.1.7 Transmitter EVM requirements

No EVM requirements are specified for this Recommendation.

8.1.8 Termination impedance

No termination impedance requirements are specified for this Recommendation.

8.1.9 Total transmit power

No total transmit power is defined by this Recommendation since the power required to drive the emitting device may differ between implementations.

8.2 UPWM-based MIMO transmission

8.2.1 Functional model of the PHY

The functional model of the PHY layer of a UPWM-based MIMO transceiver, for cases of MIMO transmission, is presented in Figure 8-13. The physical medium-independent interface (PMI) and the medium-dependent interface MDI are, respectively, two demarcation reference points between the PHY and the medium access control, and between the PHY and transmission medium. Internal reference points δ and α show separation between the PMD and physical medium attachment (PMA), and between the physical coding sub-layer (PCS) and PMA, respectively.

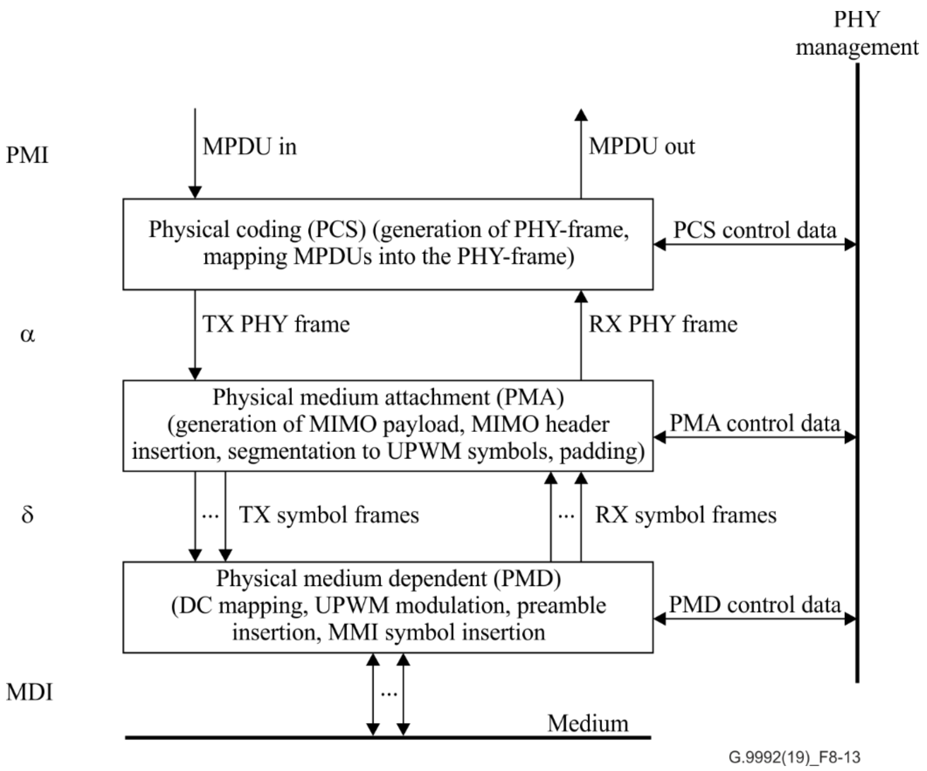


Figure 8-13 – PHY functional model of the MIMO transceiver

In the transmit direction, N_1 MIMO PHY frames are generated and then transmitted through N_1 TX ports (e.g., LEDs). The incoming MPDU is mapped into a PHY frame in the PCS. The PHY frame is parsed into multiple spatial streams (SS) according to the MIMO mode (i.e., diversity mode and multiplexing mode), and a MIMO header is inserted for each stream, which are then segmented into UPWM symbol frames in the PMA. The symbol frames of each of the spatial streams is mapped to DCs, modulated and mapped to TX ports in the PMD and transmitted over the medium with relevant parameters. In the PMD, a preamble is added to assist synchronization and phase compensation in the receiver. Besides, an MMI symbol is added to indicate the MIMO mode.

In the receive direction, frames entering from the medium via the MDI are demodulated and decoded. The recovered MPDUs are forwarded to the MAC via the PMI. The recovered PHY-frame headers (PFH) are processed in the PHY to extract the relevant frame parameters specified in clause 8.1.2.3.

8.2.2 Physical coding sublayer

The functional model of the physical coding sublayer (PCS) is presented in Figure 8-14. It is intended to describe in more detail the PCS functional block presented in Figure 8-13.

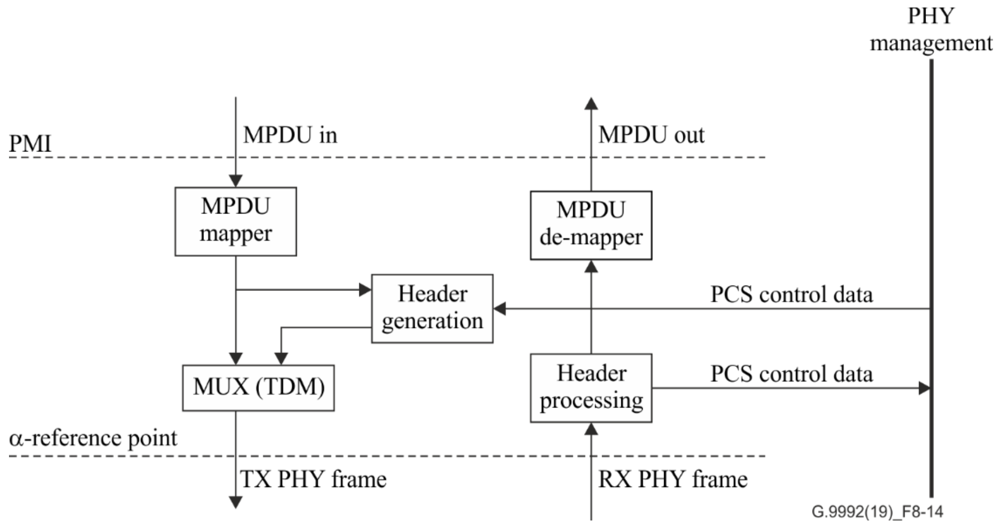


Figure 8-14 – Functional model of PCS

In the transmit direction, the incoming MPDU is mapped into a payload field of a PHY frame (clause 8.2.2.1) as described in clause 8.2.2.2. The PHY-frame header (clause 8.8.2.3) is then added to form a TX PHY frame. The TX PHY frame is passed across the α-reference point for further processing in the PMA.

In the receive direction, the decoded PHY-frame payload and header are processed and originally transmitted MPDUs are recovered from the payloads of received PHY frames and submitted to the PMI. Relevant control information conveyed in the PHY-frame header is processed and submitted to the PHY management entity.

8.2.2.1 PHY frame

The PHY frame at the α-reference point includes a PHY header and PHY payload, as described in clause 8.1.2.1. The PHY frame shall be used to generate the MIMO payload (see clause 8.2.3.3).

8.2.2.2 MPDU mapping

See clause 8.1.2.2.

8.2.2.3 PHY-frame header

See clause 8.1.2.3.

8.2.3 Physical medium attachment sublayer

The functional model of the PMA is presented in Figure 8-15. It is intended to describe in more detail the PMA functional block presented in Figure 8-13.

In the transmit direction, the incoming PHY frame (except for the preamble) at the α-reference point has a format as defined in clause 8.2.2.1. Both the header bits and the payload bits of the incoming frame are used to create the MIMO payload for each TX port as defined in 8.2.3.3. The MIMO header is generated as described in clause 8.2.3.2 and prepended before the MIMO payload. For each TX port, the MIMO header and MIMO payload are segmented into an integer number of symbol frames as described in clause 8.2.3.4. The obtained symbol frames of the MIMO header and the MIMO payload are submitted to the PMD (at the δ-reference point) for modulation and transmission over the medium.

In the receive direction, the MIMO header for each TX port is processed, and all necessary inverse operations of MIMO payload spatial streams de-parsing are performed on the received symbol frames. The recovered PHY-frame header and payload are submitted to the α-reference point for further processing in the PCS.

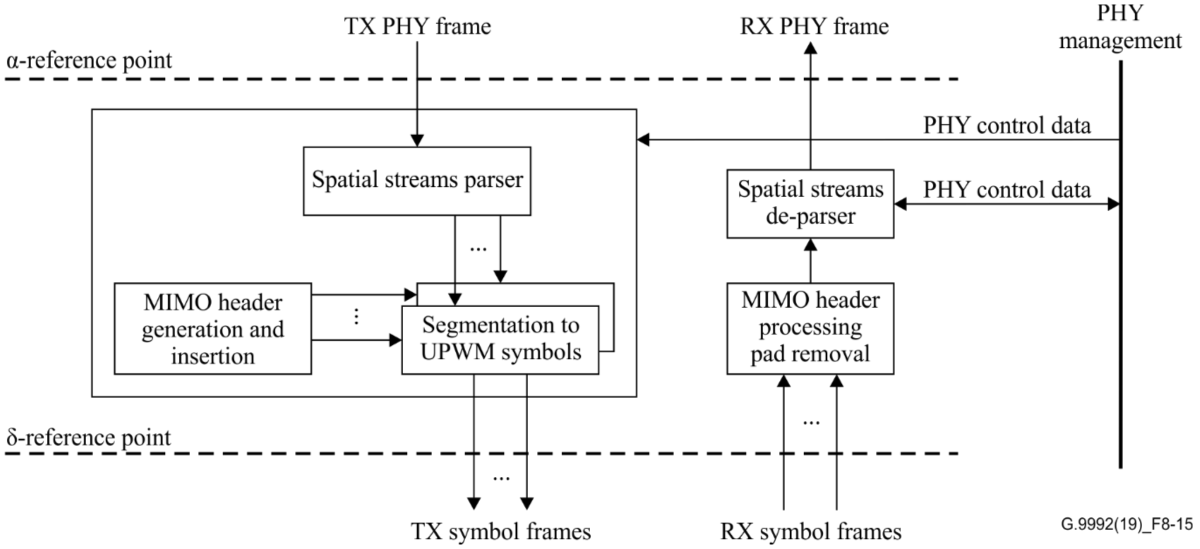


Figure 8-15 – Functional model of PMA

8.2.3.1 UPWM-based MIMO PHY frame

The format of the MIMO PHY frame for UPWM-based MIMO transmission is presented in Figure 8-16. The MIMO payload shall be created in the PMA, as either multiple spatial streams (i.e., multiplexing mode) or a single spatial stream (i.e., diversity mode). The preamble and MIMO mode indication (MMI) symbol are added to the PHY frame in the PMD. The preamble is intended for synchronization and phase compensation. Both the preamble and MMI symbol do not carry any user or management data. In addition, the MIMO header is inserted to the PHY frame in the PMA for the case where the MIMO mode is in multiplexing mode. At the MDI interface the transmission shall adhere to the following (as described in detail in clause 8.2.4):

– The preamble/MMI symbol/MIMO header/payload shall be transmitted simultaneously on all TX ports. The presence of MIMO header is MIMO mode dependent (see clause 8.2.2.3).

– The preamble and the MMI symbol to be transmitted on the first TX port shall be copied to all other TX ports.

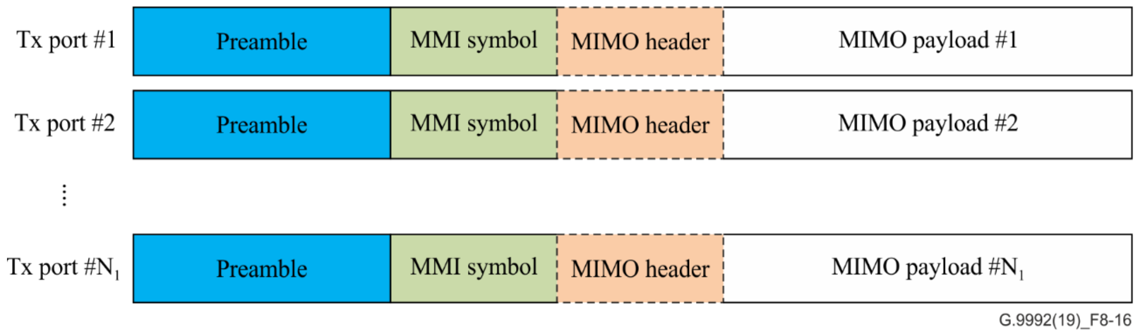


Figure 8-16 – Format of the PHY frame in a UPWM-based MIMO transmission

The MIMO header (if it exists) and MIMO payload shall contain an integer number of UPWM symbols. The length of the MIMO payload may vary from frame to frame.

8.2.3.2 MIMO header

The MIMO header shall be present only if the MMI symbol indicates multiplexing mode (see clause 8.2.4.4). The MIMO header format is defined in Table 8-21.

Table 8-21 – MIMO header format

Field	Octet	Bits	Description	Reference
Ext_Ind	0	[0]	Indication of the presence of the PortID_Ext and PB_Ext fields	Clause 8.2.3.2.1
LastPortInd		[1]	Indication of the last port	Clause 8.2.3.2.2
PortID		[6:2]	The ID of the TX port	Clause 8.2.3.2.3
PB		[7]	The odd parity bit	Clause 8.2.3.2.4
PortID_Ext	1	[6:0]	The extended part of the ID of the TX port	Clause 8.2.3.2.5
PB_Ext		[7]	The odd parity bit	Clause 8.2.3.2.6

8.2.3.2.1 Ext_Ind

If the Ext_Ind field is set to one, the PortID_Ext field and PB_Ext field shall be present. If the Ext_Ind field is set to zero, the PortID_Ext field and PB_Ext field shall not be present.

8.2.3.2.2 LastPortInd

If the LastPortInd field is set to one, the decimal value of the PortID field shall be the number of the TX ports. If the LastPortInd field is set to zero, the decimal value of the PortID field shall be lower than the number of the TX ports.

8.2.3.2.3 PortID

If the Ext_Ind field is set to zero, the PortID field shall be set to the ID of the TX ports from which the MIMO PHY frame is transmitted. It shall be represented as a 5-bit unsigned integer.

If the Ext_Ind field is set to one, the PortID field shall be set to the least significant 5 bits of the ID of the TX ports from which the MIMO PHY frame is transmitted.

8.2.3.2.4 PB

The PB field is an odd parity bit that is intended for MIMO PHY frame verification. The PB field shall be set to 1, if the count of bits in Ext_Ind field, LastPortInd field and PortID field with a value of 1 is even. The PB field shall be set to 0, if the count of bits in Ext_Ind field, LastPortInd field and PortID field with a value of 1 is odd.

8.2.3.2.5 PortID_Ext

The PortID_Ext field shall be present only if the Ext_Ind field is set to one.

The PortID_Ext field shall be set to the most significant 7 bits of the ID of the TX ports from which the MIMO PHY frame is transmitted. The ID of the TX port shall be represented as a 12-bit unsigned integer, combining with the PortID field.

8.2.3.2.6 PB_Ext

The PB_Ext field shall be present only if the Ext_Ind field is set to one.

The PB_Ext field is an odd parity bit that is intended for MIMO PHY frame verification. The PB_Ext field shall be set to 1, if the count of bits in PortID_Ext field with a value of 1 is even. The PB_Ext field shall be set to 0, if the count of bits in PortID_Ext field with a value of 1 is odd.

8.2.3.3 MIMO payload

For the case where the MIMO mode is diversity mode, the MIMO payload of each stream shall be the same, and shall contain a PHY frame passed through α reference point, as described in clause 8.2.2.1.

For the case where the MIMO mode is multiplexing mode, the TX PHY frame passed through α reference point shall be segmented into N_1 segments, where N_1 is the number of the TX ports. If the number of bits of the TX PHY frame k_{PHY} is not an integral multiple of N_1, k_{pad} zeros shall be padding at the tail of the TX PHY frame to guarantee that $(k_{PHY} + k_{pad})/N_1$ is an integer. The incoming TX PHY frame shall be segmented in sequence, and the first segment shall contain the first $(k_{PHY} + k_{pad})/N_1$ bits, and the second frame shall contain the second $(k_{PHY} + k_{pad})/N_1$ bits and so on, until the last segment. Each segment shall be mapped to the corresponding TX port in numerical order, comprising the MIMO payload.

NOTE – kpad should be as little as possible.

8.2.3.4 Segmentation to UPWM symbols

For each TX port, the MIMO header and the MIMO payload shall be segmented into symbol frames in sequence according to the modulation order m. The number of bits in each symbol frames shall be b. The MIMO header and MIMO payload segmentation is illustrated in Figure 8-17.

If the modulation order is the integral power of 2, each symbol frame will be modulated to generate one UPWM symbols. The MIMO Header and the MIMO payload shall be segmented in sequence, the frame shall contain b bits, where $b = log_2 m$. N_{sf} symbol frames are obtained, and each of the N_{sf}-1 symbol frames shall contain b bits, while the last symbol frame may contain b bits or less than b bits. If the last symbol frame contains less than b bits, it shall be padded with zeros.

If the modulation order is not the integral power of 2, each symbol frame will be modulated to generate two UPWM symbols. The MIMO header and the MIMO payload shall be segmented in sequence, and the first frame shall contain the first b bits, and the second frame shall contain the second b bits and so on, until the last symbol frame, where $b = floor(log_2 m^2)$. N_{sf} symbol frames are obtained, and each of the first N_{sf}–1 symbol frames shall contain b bits, while the last symbol frame may contain b bits or less than b bits. If the last symbol frame contains less than b bits, it shall be padded with zeros.

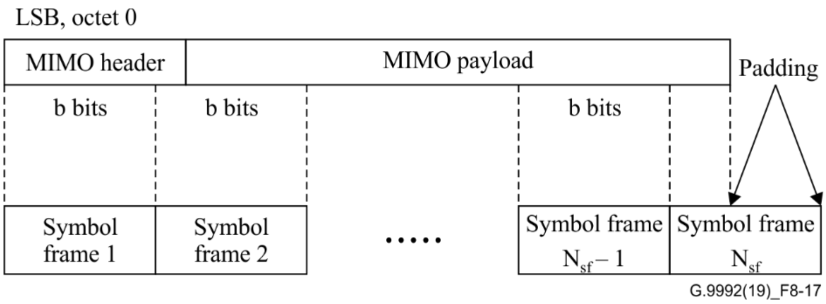


Figure 8-17 – MIMO header and the MIMO payload segmentation

8.2.4 Physical medium dependent sublayer

The functional model of the PMD is presented in Figure 8-18. In the transmit direction, the m-DC mapper maps the incoming symbol frames (for each spatial stream) to m-ary DC sequences, as specified in clause 8.2.4.1. The DC sequences for each spatial stream are fed into a UPWM modulator where non-flickering signals are generated as described in clause 8.2.4.2. After adding the preamble, the transmit signal for each spatial stream is fed into a digital LED driver, and is transmitted using visible light. Parameters of the preamble are determined by the PHY management.

Frames are output on to the medium without inter-frame gaps.

In the receive direction, a camera with a frame rate of f_c and an exposure duration of T_e is employed to detect and record the optical signal. With the help of the preamble detection and PI extraction, the undersampled-recorded data are compensated and demodulated. The recovered symbol frames are transferred to the PMA via δ-reference point. The preamble, MMI symbol and MIMO header are processed and the processing result are passed to the PHY management entity.

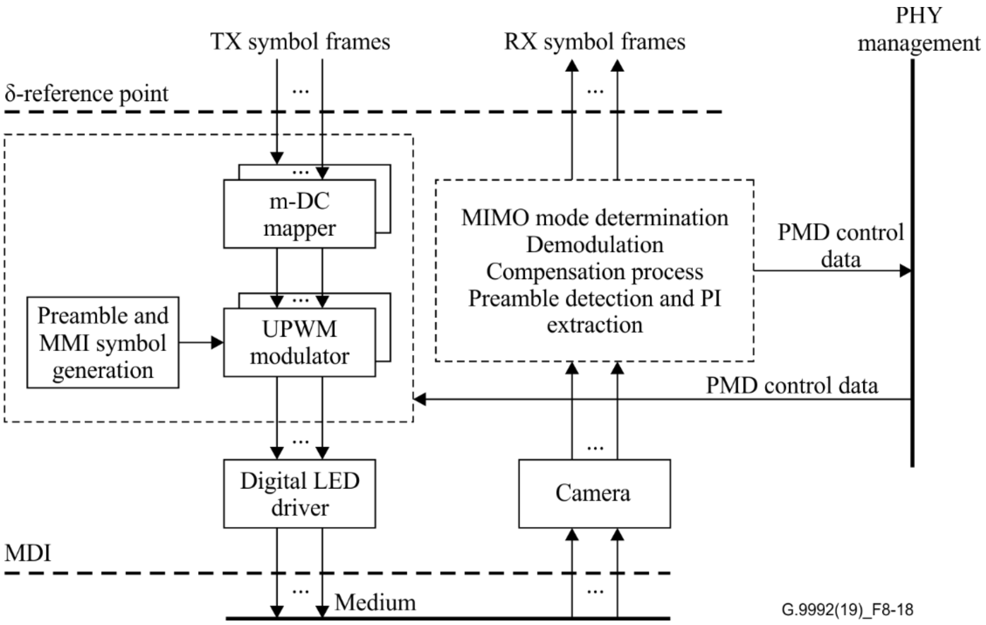


Figure 8-18 – Functional model of the PMD

8.2.4.1 *m*-DC mapping

See clause 8.1.4.1.1.

8.2.4.2 UPWM modulator

See clause 8.1.4.1.2.

8.2.4.3 UPWM preamble signal

See clause 8.1.4.1.3.

8.2.4.4 MMI symbol

The MMI symbol is used to indicate the MIMO modes, which includes multiplexing mode and diversity mode. The MMI symbol comprises of one UPWM symbol, and for each PHY frame, the same UPWM symbol shall be transmitted as the MMI symbol at each TX port. The value of the DC for generating the MMI symbol shall be set according to the configured MIMO mode as shown in Table 8-22.

Table 8-22 – Value of DC for generating the MMI symbol

MIMO mode	Value of DC
Multiplexing	100%
Diversity	0%

8.2.5 PSD mask specifications

See clause 8.1.5.

8.2.6 Electrical specifications

8.2.6.1 Transmit clock tolerance

See clause 8.1.6.1.

8.2.7 Transmitter EVM requirements

See clause 8.1.7.

8.2.8 Termination impedance

See clause 8.1.8.

8.2.9 Total transmit power

See clause 8.1.9.

8.3 UPPM-based MIMO transmission

8.3.1 Functional model of the PHY

The functional model of the PHY layer of a UPPM-based MIMO transceiver, for cases of UPPM-based MIMO transmission, is presented in Figure 8-19. The physical medium-independent interface and the medium-dependent interface are, respectively, two demarcation reference points between the PHY and the medium access control, and between the PHY and transmission medium. Internal reference points δ and α show separation between the physical medium dependent and physical medium attachment, and between the physical coding sub-layer and PMA, respectively.

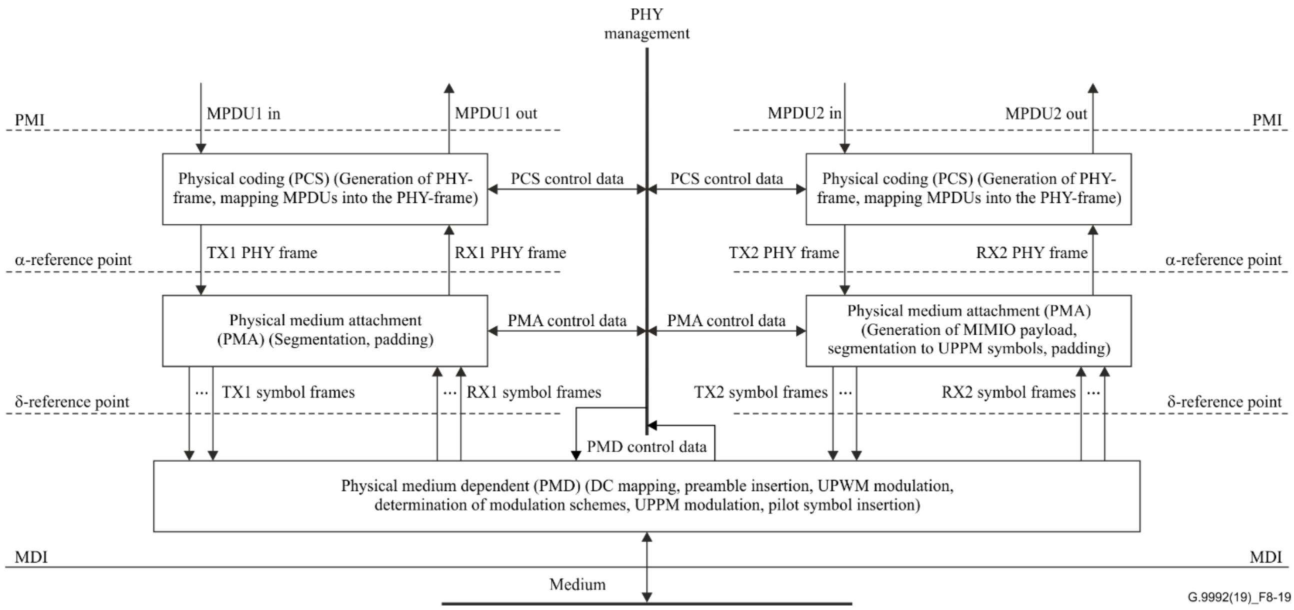


Figure 8-19 – PHY functional model of the UPPM-based MIMO transceiver

In the transmit direction, data enters the PHY from the MAC via the PMI in blocks of bytes called MPDUs. The incoming MPDU is mapped into a PHY frame in the PCS. The PHY frame is parsed into multiple spatial streams according to the number of the TX ports (i.e., LED lamps), then segmented into UPPM symbol frames in the PMA. The symbol frames of each of the spatial streams is modulated to UPPM symbols, and a pilot symbol is inserted for each spatial stream, then mapped to TX ports in the PMD and transmitted over the medium with relevant parameters. In the PMD, a preamble is added to assist synchronization and phase compensation in the receiver.

In the receive direction, frames entering from the medium (reception is also done via multiple Rx ports) via the MDI are demodulated and decoded. The recovered MPDUs are forwarded to the MAC via the PMI. The recovered PHY-frame headers) are processed in the PHY to extract the relevant frame parameters specified in clause 8.1.2.3.

8.3.2 Physical coding sublayer

The functional model of the PCS is presented in Figure 8-20. It is intended to describe in more detail the PCS functional block presented in Figure 8-19.

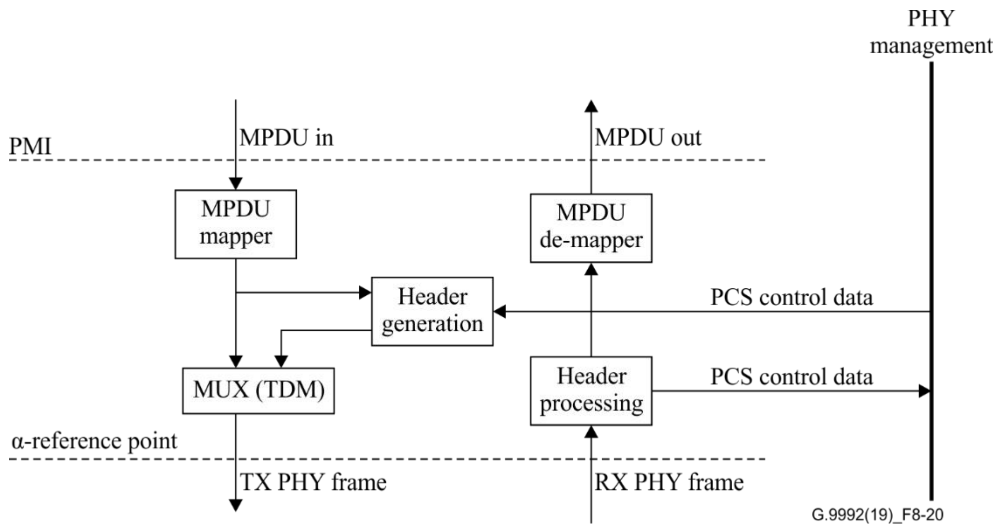


Figure 8-20 – Functional model of PCS

In the transmit direction, the incoming MPDU is mapped into a payload field of a PHY frame (clause 8.3.2.1) as described in clause 8.3.2.2. The PHY-frame header is then added to form a TX PHY frame. The TX PHY frame is passed across the α-reference point for further processing in the PMA.

In the receive direction, the decoded PHY-frame payload and header are processed and originally transmitted MPDUs are recovered from the payloads of received PHY frames and submitted to the PMI. Relevant control information conveyed in the PHY-frame header is processed and submitted to the PHY management entity.

8.3.2.1 PHY frame

The PHY frame at the α-reference point includes a PHY header and PHY payload as described in clause 8.1.2.1. The PHY frame shall be used to generate the MIMO payload (see clause 8.3.3.2).

8.3.2.2 MPDU mapping

See clause 8.1.2.2.

8.3.2.3 PHY-frame header

See clause 8.1.2.3.

8.3.3 Physical medium attachment sublayer

The functional model of the PMA is presented in Figure 8-21. It is intended to describe in more detail the PMA functional block presented in Figure 8-19.

In the transmit direction, the incoming PHY frame (except for the preamble) at the α-reference point has a format as defined in clause 8.3.2.1. Both the header bits and the payload bits of the incoming frame are used to create the MIMO payload for each TX port as defined in clause 8.3.3.2. The spatial stream parser divides the TX PHY frame into N blocks, where N is the number of the TX ports. For each TX port, the MIMO payload are segmented into an integer number of symbol frames as described in clause 8.3.3.3. The obtained symbol frames of the MIMO payload are submitted to the PMD (at the δ-reference point) for modulation and transmission over the medium.

In the receive direction, all necessary inverse operations of MIMO payload spatial streams de-parsing are performed on the received symbol frames. The recovered PHY-frame header and payload are submitted to the α-reference point for further processing in the PCS.

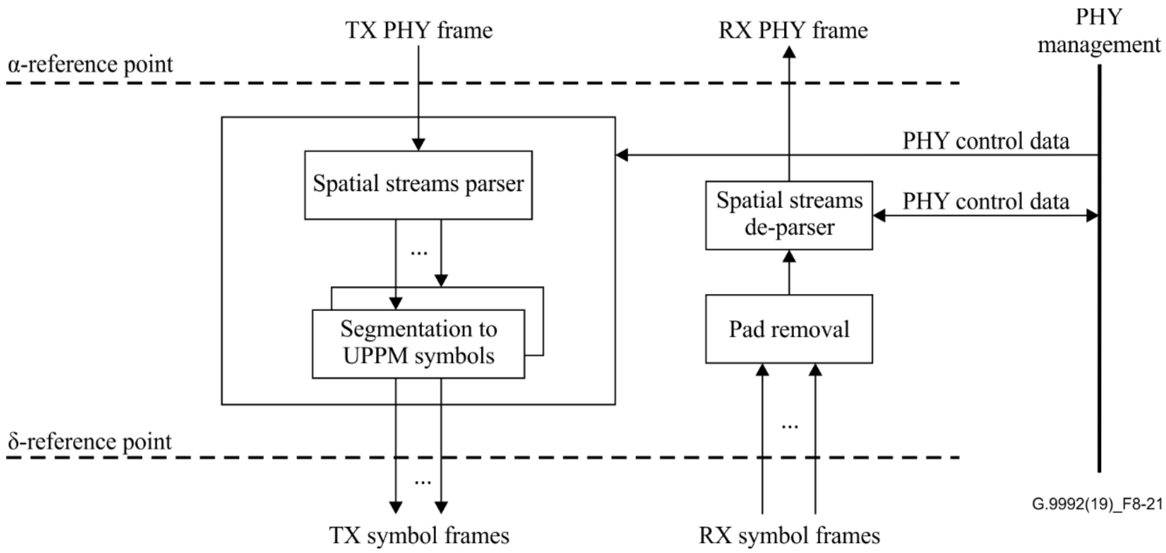


Figure 8-21 – Functional model of PMA

8.3.3.1 UPPM-based MIMO PHY frame

The format of the MIMO PHY frame for UPPM-based MIMO transmission is presented in Figures 8-22 and 8-23. The PHY frame at the α-reference point includes a PHY header (as described in clause 8.1.2.3) and PHY payload (as described in clause 8.1.2.1) specified for SISO transmission. The MIMO payload (as described in clause 8.3.3.2) shall be created by equally dividing the SISO header and PHY payload into N_2 spatial streams. If UPWM SISO transmission is adopted in the low speed channel for each TX port, a UPWM preamble shall be added to each UPPM-based MIMO payload stream in the PMD, and each TX port shall transmit the same UPWM SISO information in the PMD. If UPWM SISO transmission is not adopted in UPPM-based MIMO transmission, a UPWM preamble shall not be added to each UPPM-based MIMO payload stream in the PMD, instead a pre-defined DC value which is vendor discretionary shall be given for generating UPPM symbol. The UPWM preamble is intended for UPWM SISO synchronization and phase compensation. The UPWM preamble do not carry any UPWM user or management data, however, it carries UPPM-based MIMO data. If UPWM SISO transmission is adopted in the low speed channel for each TX port, at the MDI interface the transmission shall adhere to the following (as described in detail in clause 8.3.4):

– The UPWM preamble / UPPM-based MIMO payload shall be transmitted simultaneously on all TX ports.

– The UPWM preamble to be transmitted on the first TX port shall be copied to all other TX ports.

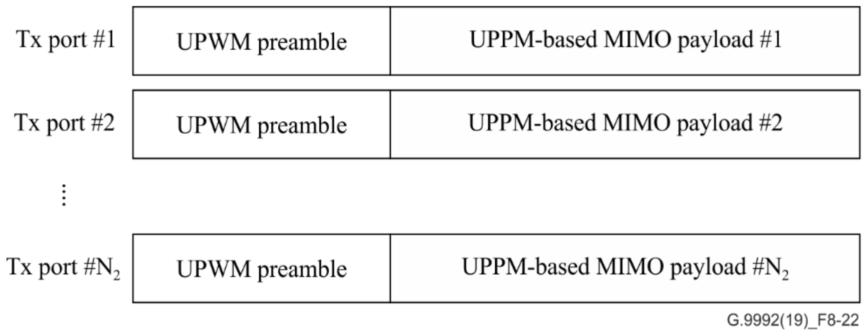


Figure 8-22 – Format of the PHY frame in a UPPM-based MIMO transmission with UPWM SISO transmission

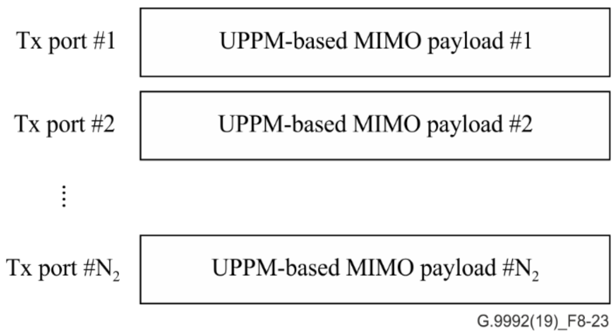


Figure 8-23 – Format of the PHY frame in a UPPM-based MIMO transmission without UPWM SISO transmission

The length of the MIMO payload may vary from frame to frame.

8.3.3.2 UPPM-based MIMO payload

The TX PHY frame passed through α reference point shall be segmented into N_2 segments, where N_2 is the number of the TX ports. If the number of bits of the TX PHY frame k_{PHY} is not an integral multiple of N_2, k_{pad} zeros shall be padding at the tail of the TX PHY frame to guarantee that $(k_{PHY} + k_{pad})/N_2$ is an integer. The incoming TX PHY frame shall be segmented in sequence, and the first segment shall contain the first $(k_{PHY}+ k_{pad})/N_2$ bits, and the second frame shall contain the second $(k_{PHY} + k_{pad})/N_2$ bits and so on, until the last segment. Each segment shall be mapped to the corresponding TX port in numerical order, comprising the MIMO payload.

NOTE – kpad should be as little as possible.

8.3.3.3 Segmentation to UPPM-based MIMO symbols

For each TX port, the incoming UPPM-based MIMO PHY frame from each spatial stream shall be segmented into even number of symbol frames in sequence according to many parameters indicated by the PHY control data which are received through PHY management:

1) DC D_i either determined by the m-DC mapper (see clause 8.1.4.1.1) or a pre-defined value, which is vendor discretionary;
2) valid data region information (see clause 8.1.4.2.3.2) of a UPPM waveform segment. TX PHY frame segmentation is illustrated in Figure 8-24.

For each TX port, the incoming TX PHY frame shall be segmented in sequence, $2N_{sf1} + 2$ symbol frames are obtained. If the symbol frame is the first symbol frame (i.e., symbol frame 1), it shall contain $(N_{ppm} – 2) \times \log_2 M$ bits, where N_{ppm} and M are parameters determined by valid data region information (see clause 8.1.4.2.3.2) of a UPPM waveform segment, the second symbol frame shall contain $N_{ppm} \times \log_2 M$ bits. Symbol frame No. 2n + 1 and symbol frame No. 2n + 2 ($n \geq 1$) shall contain the same number of bits. If symbol frame No. 1 contains less than $(N_{ppm} - 2) \times \log_2 M$ bits, both symbol No. 1 and No. 2 shall be padded with zeros. If only symbol frame No. 2 contains less than $N_{ppm} \times \log_2 M$ bits, it shall be padded with zeros. If symbol frame No. 2n + 1 ($n \geq 1$) contains less than $N_{ppm} \times \log_2 M$ bits, both symbol No. 2n + 1 and No. 2n + 2 shall be padded with zeros. If only symbol frame No. 2n + 2 contains less than $N_{ppm} \times \log_2 M$ bits, it shall be padded with zeros.

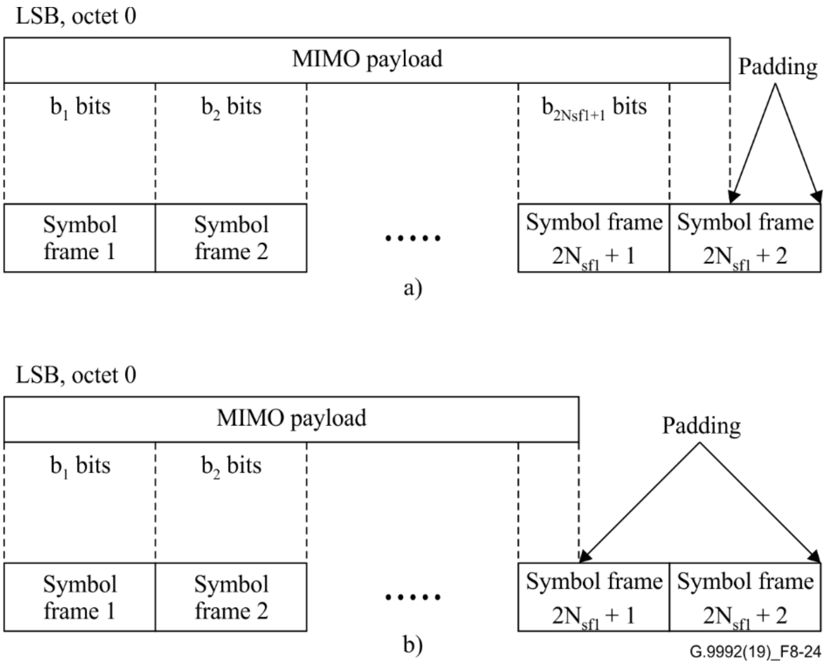


Figure 8-24 – Two TX PHY frame segmentations for each UPPM-based MIMO transmission port

8.3.4 Physical medium dependent sublayer

The functional model of the PMD is presented in Figure 8-25. In the transmit direction, the m-DC mapper maps the incoming TX1 symbol frames to m-ary DC sequences, as specified in clause 8.1.4.1.1. The DC sequences of the prepending preamble and the DC sequences obtained from the m-DC mapping of the incoming TX1 symbol frames are fed into the UPPM modulation selector.

The incoming TX2 symbol frames are fed into multiple UPPM modulators where non-flickering signals are generated as described in clause 8.1.4.2.2. The UPPM modulation selector determines the UPPM modulation scheme. The DC of all final UPPM symbols may be determined in accordance with the current m-ary DC generated by the m-DC mapper or by a predefined DC. The preamble and delimiters signals are fed into all UPPM modulators to generate the parallel transmit signals. Pilot symbols (as described in clause 8.3.4.1) shall then be prepended to each transmit channel, which is then fed into multiple LED drivers and transmitted using visible light.

NOTE – TX1 symbol frames may exist depending on the enabled channels.

Frames are output on to the medium without inter-frame gaps.

In the receive direction, a camera with a frame rate of f_c is employed to detect and record all optical signals. The receiver exposure duration can be set to T_e' to receive TX1 and TX2 symbol frames from both low-speed and high-speed channels or to receive TX2 symbol frames only from the high-speed channel via UPPM-based MIMO link. When the exposure is set to T_e', if at least two UPPM waveform segments of a TX port are received in a captured video frame, pilot symbols are first detected. Thereafter, multiple data streams from the high-speed channel can be obtained and a DC generated by an m-DC mapper from the low-speed channel may also be received. If at least two UPPM waveform segments of a TX port cannot be received, the exposure duration may be changed to T_e to detect the optical signal to receive symbol frames in low-speed channel only. With the help of the preamble detection and PI extraction, the undersampled-recorded UPWM data from low-speed channel are compensated and demodulated if at least two UPPM waveform segments of a TX port are received in a captured video frame. After the pilot symbol detection processing, multiple UPPM channels can be obtained, with the help of preamble and delimiter detection, parallel recorded stripes from high-speed channel are processed and the obtained V*M*PPM (e.g., V2PPM, V4PPM or V8PPM) signal are processed and demodulated in parallel. The DC mapper generated DCs from the low-speed channel may also be obtained if both high speed and low speed channels are enabled, then processed and demodulated. The recovered symbol frames from either the low-speed or the high-speed channel are transferred to the PMA via δ-reference point. The preamble are processed and the processing result are passed to the PHY management entity.

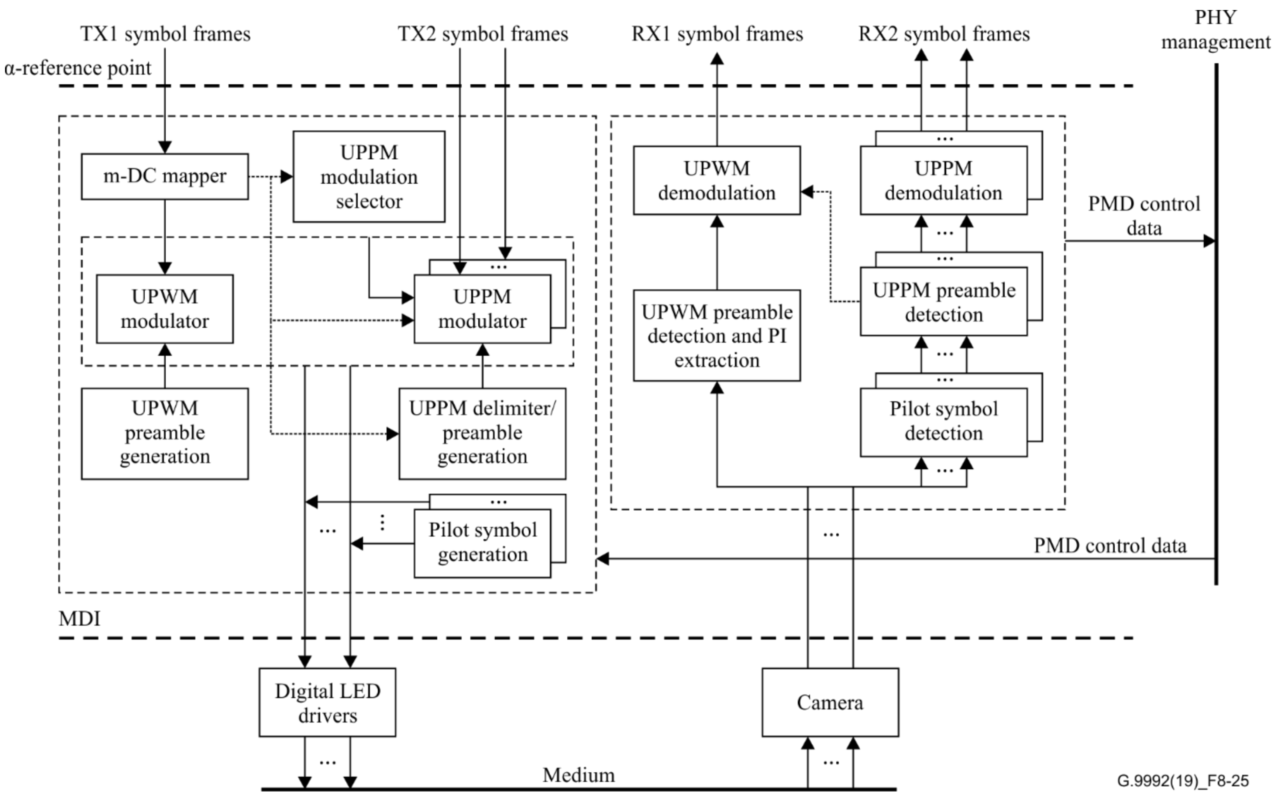


Figure 8-25 – Functional model of the PMD in a UPPM-based MIMO transmission

8.3.4.1 Pilot symbol

A pilot symbol shall be used to indicate the TX port number in UPPM-based MIMO system. All pilot symbols shall be different and each pilot symbol shall represent one TX port. In the transmitting node which contains N_2 independent TX ports (where N_2 is an integer standing for the total number of parallel channel which varies from 2 to 4), N_2 different pilot symbols along with $N_2 \times M1$ UPPM symbols (as described in clause 8.3.3) shall be generated, where $M1$ is an integer representing the number of UPPM symbols for each TX port ($M1 \geq 1$). After that N_2 different pilot symbols shall be prefixed to these $N_2 \times M1$ UPPM symbols synchronously, as shown in Figure 8-26, to make sure each pilot symbol corresponds to a unique TX port. Finally N_2 Pilot symbols and $N_2 \times M1$ UPPM symbols shall be sent via N_2 TX port, more specifically, each LED shall send one pilot symbol followed by the corresponding $M1$ UPPM.

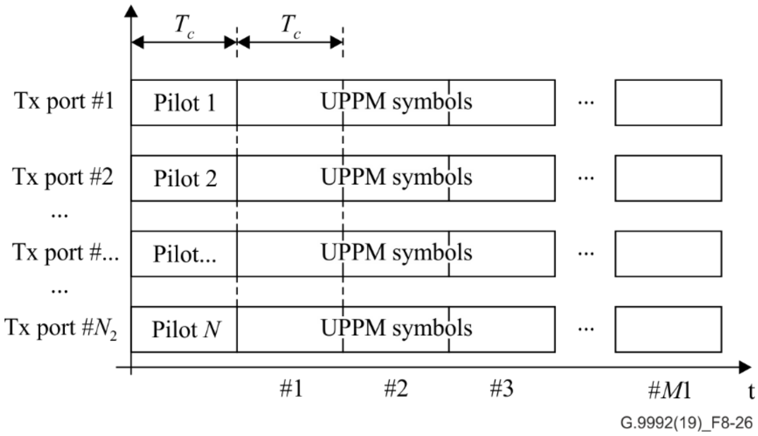


Figure 8-26 – UPPM-based MIMO streams

The duration of each pilot symbol shall be the same as the ordinary UPPM symbol T_c, which is the reciprocal of the frame rate of the camera. Each pilot symbol shall comprise of W ($W = 2k$) segments which are k identical odd-indexed segments and k identical even-indexed segments, e.g., as shown in Table 8-23, $W = 4$. Each odd-indexed segment shall be followed by an even-indexed segment. The average DCs (DCs) of the odd-indexed segments and the even-indexed segments shall be complementary and determined by the DC generated by a m-DC mapper or by a predefined DC (e.g., if the DC generated by the m-DC mapper is D%, then the average DC of the odd-indexed segments shall be D%, the average DC of the even-indexed segments shall be 1-D%).

Table 8-23 shows the proposed structure of the pilot symbols for different port numbers. For $N_2 = 2$, each segment (odd-indexed and even-indexed) comprises three regions, which are, a start delimiter region , an LED number indicating region (LNIR) and an end delimiter region (EDR), each region contains a number of PWM cycles with the same DC which equals to the average DC of the corresponding segment. While for $N_2 = 3$ and 4, each segment comprises five regions, which are, a SDR, the first LED Number Indicating region (LNIR#1), an interval delimiter region (IDR), the 2nd LED number indicating region (LNIR#2), and an EDR. Similarly, each region contains a number of PWM cycles with the same DC which also equals to the average DC of the corresponding segment. Note that, for all types of pilot symbols, the SDR and EDR are employed to indicate the beginning and the end of a segment of the pilot symbol, respectively. The IDR is used to separate two LNIRs (if applicable), the LNIR(s) is/are used to indicate the TX port number in UPPM-based MIMO system (if applicable) by sending PWM signals at different frequencies ($N_2 = 2$) or different frequency groups ($N_2 = 3$ or 4).

Table 8-23 – Waveform diagram of pilot symbols in UPPM-based MIMO transmission

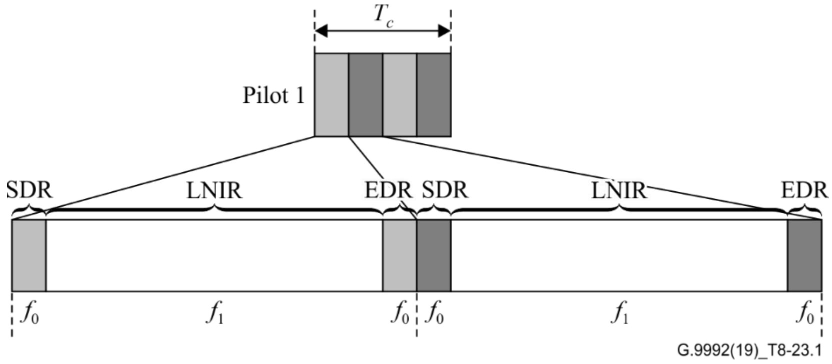
Number of Ports (N)	Port ID	Pilot symbol
$N_2 = 2$	TX port #1	

Table 8-23 – Waveform diagram of pilot symbols in UPPM-based MIMO transmission

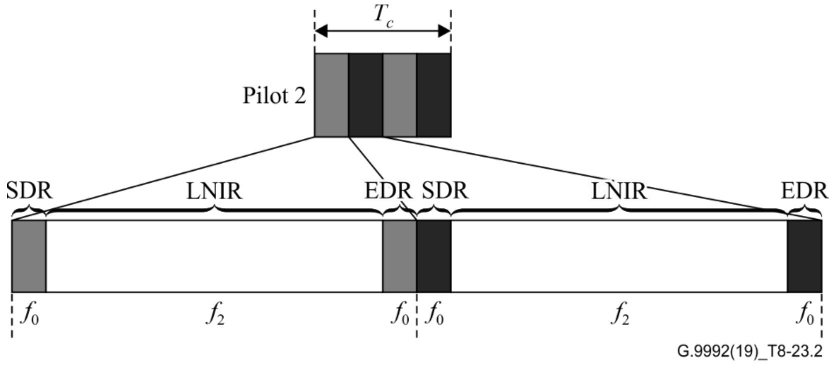
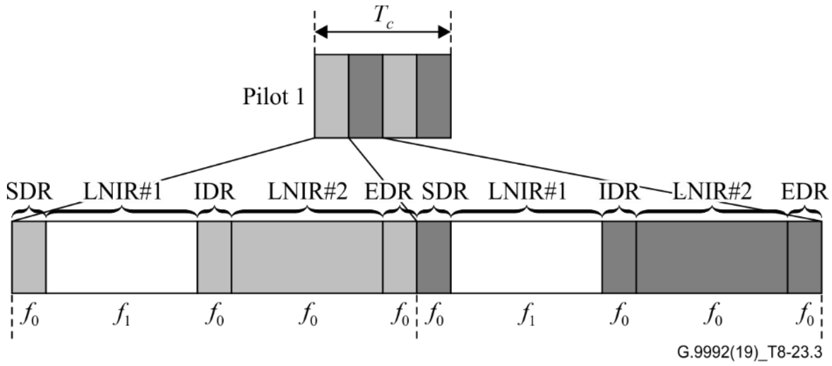
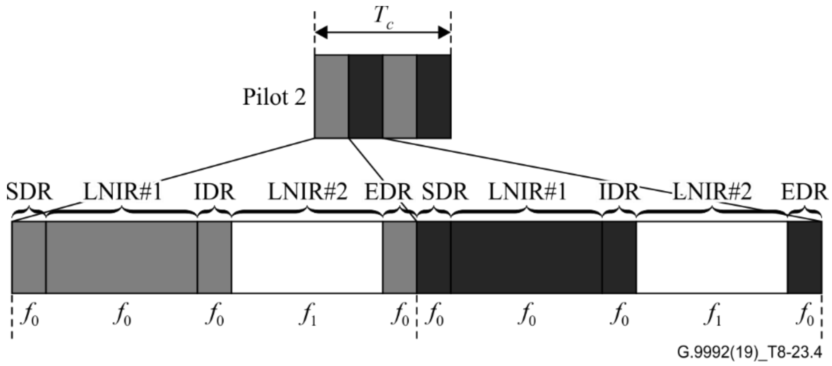
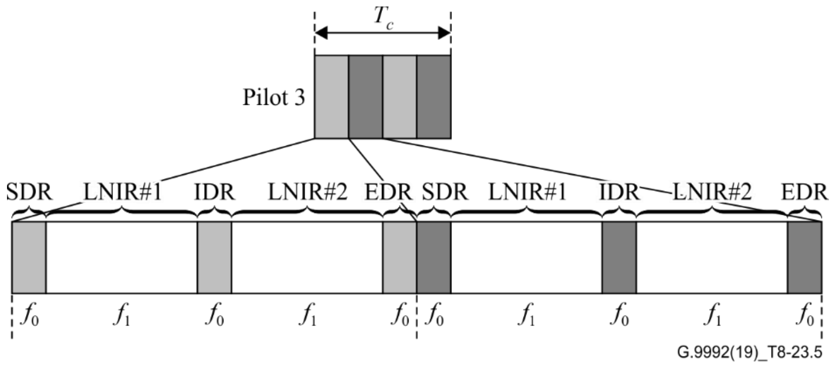
Number of Ports (N)	Port ID	Pilot symbol
	TX port #2	
$N_2 = 3$	TX port #1	
	TX port #2	
	TX port #3	

Table 8-23 – Waveform diagram of pilot symbols in UPPM-based MIMO transmission

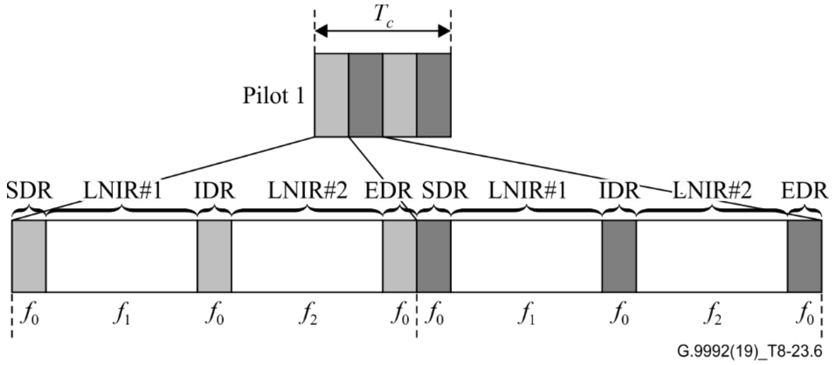
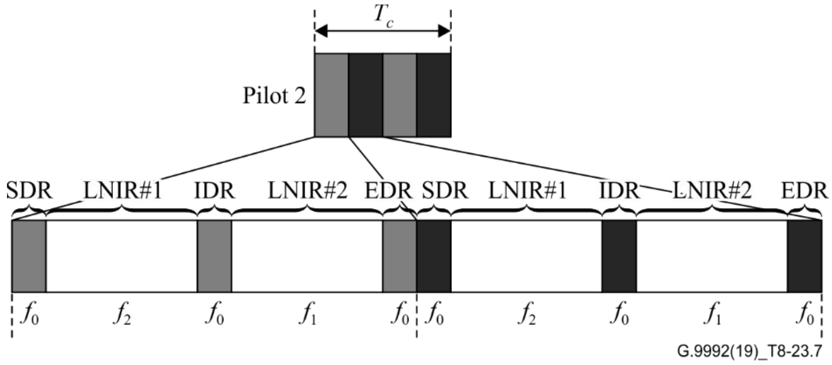
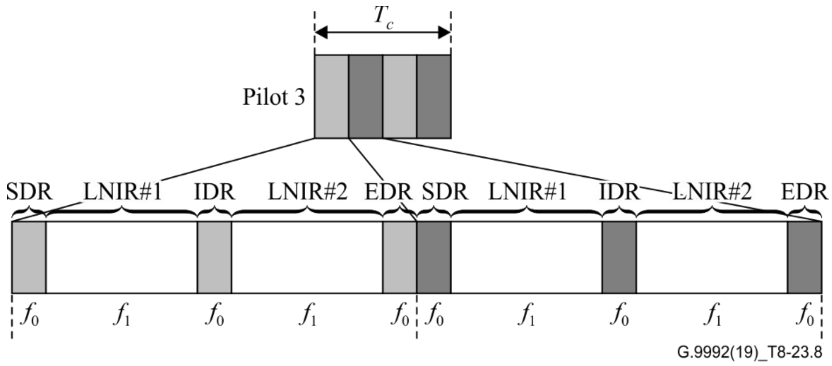
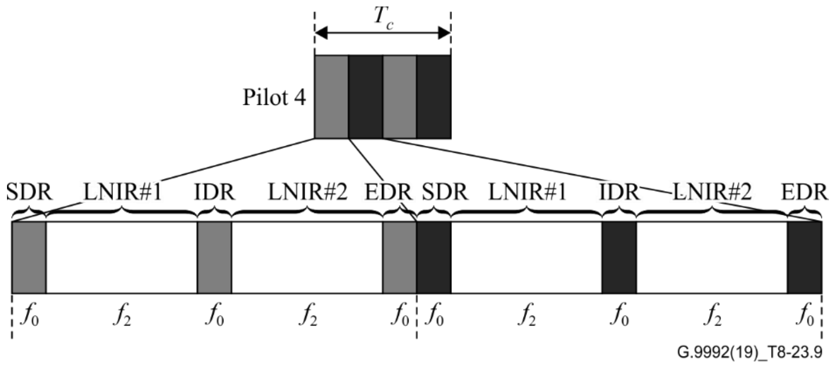
<table>
<tr><th>Number of Ports (N)</th><th>Port ID</th><th>Pilot symbol</th></tr>
<tr><td rowspan="4">$N_2 = 4$</td><td>TX port #1</td><td>
</td></tr>
<tr><td>TX port #2</td><td>
</td></tr>
<tr><td>TX port #3</td><td>
</td></tr>
<tr><td>TX port #4</td><td>
</td></tr>
</table>

Table 8-24 shows the related attributes and parameters for each section of different cases in accordance to Table 8-23. All frequencies given in Table 8-24 shall follow the following restrictions: $f_0 > 3/T_e'$, 200Hz $< f_1 < 2/T_e'$, 200Hz $< f_2 < 2/T_e'$, and $f_1 < f_2$. All time durations shall follow the following restrictions: if $N_2 = 2$, $2 \times T_{ppm} + T_{lnir} = T_s = T_c/2k$, else if $N_2 = 3$ or $N_2 = 4$, $3 \times T_{ppm} + T_{lnir1} + T_{lnir2} = T_s = T_c/2k$. The time duration of SDR and IDR and EDR are the same equals to T_{ppm}. If $N_2 = 2$, T_{lnir} is the duration of LNIR#1. Else if $N_2 = 3$ or 4, T_{lnir1} and T_{lnir2} are the duration of LNIR#1 and LNIR#2, respectively. The number of PWM pulses in each region shall be an integer.

Note that f_1 and f_2 can be any different frequencies as long as they could ensure that the total number of PWM pulses within the same period of T_{lnir} or T_{lnir1} or T_{lnir2} are different.

If the receiver records two parallel signals, when $N_2 = 2$ (there is only one LNIR in the whole segment), the receiver could determine that the transmitter has two TX ports and know the port number of each TX port. Similarly, when $N_2 = 3$ or 4, due to the unique preamble waveform, the receiver could also determine the total number of TX ports as well as their corresponding port number.

Table 8-24 – Specific value of pilot symbols in UPPM-based MIMO transmission

TX port total number	**Segment**	**Parameter**	**SDR**	**LNIR#1**	**IDR**	**LNIR#2**	**EDR**
$N_2 = 2$	TX port #1 odd-indexed segment	PWM frequency	f_0	f_1	N/A	N/A	f_0
		region duration	T_{ppm}	T_{lnir}	N/A	N/A	T_{ppm}
		PWM DC	D%	D%	N/A	N/A	D%
	TX port #1 even-indexed segment	PWM frequency	f_0	f_1	N/A	N/A	f_0
		region duration	T_{ppm}	T_{lnir}	N/A	N/A	T_{ppm}
		PWM DC	1-D%	1-D%	N/A	N/A	1-D%
	TX port #2 odd-indexed segment	PWM frequency	f_0	f_2	N/A	N/A	f_0
		region duration	T_{ppm}	T_{lnir}	N/A	N/A	T_{ppm}
		PWM DC	D%	D%	N/A	N/A	D%
	TX port #2 even-indexed segment	PWM frequency	f_0	f_2	N/A	N/A	f_0
		region duration	T_{ppm}	T_{lnir}	N/A	N/A	T_{ppm}
		PWM DC	1-D%	1-D%	N/A	N/A	1-D%
$N_2 = 3$	TX port #1 odd-indexed segment	PWM frequency	f_0	f_1	f_0	f_0	f_0
		region duration	T_{ppm}	T_{lnir1}	T_{ppm}	T_{lnir2}	T_{ppm}
		PWM DC	D%	D%	D%	D%	D%
	TX port #1 even-indexed segment	PWM frequency	f_0	f_1	f_0	f_0	f_0
		region duration	T_{ppm}	T_{lnir1}	T_{ppm}	T_{lnir2}	T_{ppm}
		PWM DC	1-D%	1-D%	1-D%	1-D%	1-D%

Table 8-24 – Specific value of pilot symbols in UPPM-based MIMO transmission

TX port total number	Segment	Parameter	SDR	LNIR#1	IDR	LNIR#2	EDR
	TX port #2 odd-indexed segment	PWM frequency	f_0	f_0	f_0	f_1	f_0
		region duration	T_{ppm}	T_{lnir1}	T_{ppm}	T_{lnir2}	T_{ppm}
		PWM DC	D%	D%	D%	D%	D%
	TX port #2 even-indexed segment	PWM frequency	f_0	f_0	f_0	f_1	f_0
		region duration	T_{ppm}	T_{lnir1}	T_{ppm}	T_{lnir2}	T_{ppm}
		PWM DC	1-D%	1-D%	1-D%	1-D%	1-D%
	TX port #3 odd-indexed segment	PWM frequency	f_0	f_1	f_0	f_1	f_0
		region duration	T_{ppm}	T_{lnir1}	T_{ppm}	T_{lnir2}	T_{ppm}
		PWM DC	D%	D%	D%	D%	D%
	TX port #3 even-indexed segment	PWM frequency	f_0	f_1	f_0	f_1	f_0
		region duration	T_{ppm}	T_{lnir1}	T_{ppm}	T_{lnir2}	T_{ppm}
		PWM DC	1-D%	1-D%	1-D%	1-D%	1-D%
$N_2 = 4$	TX port #1 odd-indexed segment	PWM frequency	f_0	f_1	f_0	f_2	f_0
		region duration	T_{ppm}	T_{lnir1}	T_{ppm}	T_{lnir2}	T_{ppm}
		PWM DC	D%	D%	D%	D%	D%
	TX port #1 even-indexed segment	PWM frequency	f_0	f_1	f_0	f_2	f_0
		region duration	T_{ppm}	T_{lnir1}	T_{ppm}	T_{lnir2}	T_{ppm}
		PWM DC	1-D%	1-D%	1-D%	1-D%	1-D%
	TX port #2 odd-indexed segment	PWM frequency	f_0	f_2	f_0	f_1	f_0
		region duration	T_{ppm}	T_{lnir1}	T_{ppm}	T_{lnir2}	T_{ppm}
		PWM DC	D%	D%	D%	D%	D%
	TX port #2 even-indexed segment	PWM frequency	f_0	f_2	f_0	f_1	f_0
		region duration	T_{ppm}	T_{lnir1}	T_{ppm}	T_{lnir2}	T_{ppm}
		PWM DC	1-D%	1-D%	1-D%	1-D%	1-D%

Table 8-24 – Specific value of pilot symbols in UPPM-based MIMO transmission

TX port total number	Segment	Parameter	SDR	LNIR#1	IDR	LNIR#2	EDR
	TX port #3 odd-indexed segment	PWM frequency	f_0	f_1	f_0	f_1	f_0
		region duration	T_{ppm}	T_{lnir1}	T_{ppm}	T_{lnir2}	T_{ppm}
		PWM DC	D%	D%	D%	D%	D%
	TX port #3 even-indexed segment	PWM frequency	f_0	f_1	f_0	f_1	f_0
		region duration	T_{ppm}	T_{lnir1}	T_{ppm}	T_{lnir2}	T_{ppm}
		PWM DC	1-D%	1-D%	1-D%	1-D%	1-D%
	TX port #4 odd-indexed segment	PWM frequency	f_0	f_2	f_0	f_2	f_0
		region duration	T_{ppm}	T_{lnir1}	T_{ppm}	T_{lnir2}	T_{ppm}
		PWM DC	D%	D%	D%	D%	D%
	TX port #4 even-indexed segment	PWM frequency	f_0	f_2	f_0	f_2	f_0
		region duration	T_{ppm}	T_{lnir1}	T_{ppm}	T_{lnir2}	T_{ppm}
		PWM DC	1-D%	1-D%	1-D%	1-D%	1-D%

8.3.5 PSD mask specifications

See clause 8.1.5.

8.3.6 Electrical specifications

8.3.6.1 Transmit clock tolerance

See clause 8.1.6.1.

8.3.7 Transmitter EVM requirements

See clause 8.1.7.

8.3.8 Termination impedance

See clause 8.1.8.

8.3.9 Total transmit power

See clause 8.1.9.

8.4 Control parameters

Table 8-25 – Parameters for PCS, PMA, PMD

Parameter	Description	Value
m	Modulation order of UPWM	2, 3, 4, 6, 8, 12, 16, 23, 32
b	The number of bits in a UPWM symbol frame	1, 2, 3, 4, 5
N_{sf}	N_{sf} UPWM symbol frames shall be obtained for a TX PHY frame after segmentation process	$N_{sf} \geq 1$, integer
N_{sf1}	$2N_{sf1} + 2$ UPPM symbol frames shall be obtained for a TX PHY frame after segmentation process	$N_{sf1} \geq 0$, integer
N_{ppm}	The number PPM symbols within a valid data waveform	$N_{ppm} \geq 2$, integer
f_c	Camera's frame rate	120 fps
T_e	Exposure duration for UPWM	1/2000s – 1/1000s
T_e'	Exposure duration for UPWM and UPPM	1/30000s – 1/15000s
T_s	The duration of a segment of PWM waveform	≤ 5ms
T_p	The duration of a basic PWM cycle of a UPWM symbol	$\leq T_e/5$
k	An integer to make sure T_s is less than 5 ms $T_s = T_c/(2k)$	$1/(240\ T_s)$
T_c	The duration of a UPWM symbol T_c is the reciprocal of the camera's frame rate f_c	1/120 s
T_{appm}	The duration of the basic PWM cycle in the first section of start delimiter of a UPPM preamble	$< T_e'/3$
T_{ppm}	The duration of the basic PPM cycle in the second section of start delimiter of a UPPM preamble or the duration of the basic PPM cycle of the valid data region of a UPPM waveform segment W_{i1} or W_{i2}	$\leq T_e/5$
W	The number of segments in pilot symbol (UPPM-based MIMO streams)	$2k$
f_0	Frequency of SDR, IDR, EDR	$f_0 > 3/T_e'$
f_1	One frequency of LNIR	200 Hz $< f_1 < 2/T_e'$, and $f_1 < f_2$
f_2	One frequency of LNIR	200 Hz $< f_2 < 2/T_e'$, and $f_1 < f_2$
T_{lnir}	The duration of LNIR	if $N_2 = 2$, $2 \times T_{ppm} + T_{lnir} = T_s = T_c/2k$, else if $N_2 = 3$ or $N_2 = 4$, $3 \times T_{ppm} + T_{lnir1} + T_{lnir2} = T_s = T_c/2k$
T_{lnir1}	The duration of LNIR#1	if $N_2 = 2$, $2 \times T_{ppm} + T_{lnir} = T_s = T_c/2k$, else if $N_2 = 3$ or $N_2 = 4$, $3 \times T_{ppm} + T_{lnir1} + T_{lnir2} = T_s = T_c/2k$

Table 8-25 – Parameters for PCS, PMA, PMD

Parameter	Description	Value
T_{lnir2}	The duration of LNIR#2	if $N_2 = 2$, $2 \times T_{ppm} + T_{lnir} = T_s = T_c/2k$, else if $N_2 = 3$ or $N_2 = 4$, $3 \times T_{ppm} + T_{lnir1} + T_{lnir2} = T_s = T_c/2k$

9 Data link layer specification

9.1 Functional model of DLL and frame formats

The functional model of the DLL is presented in Figure 9-1. The A-interface and PMI are respectively, two demarcation reference points between the AE and DLL and between the DLL and PHY. Internal reference points x1 and x2 respectively, show logical separation between the APC and LLC and between the LLC and MAC.

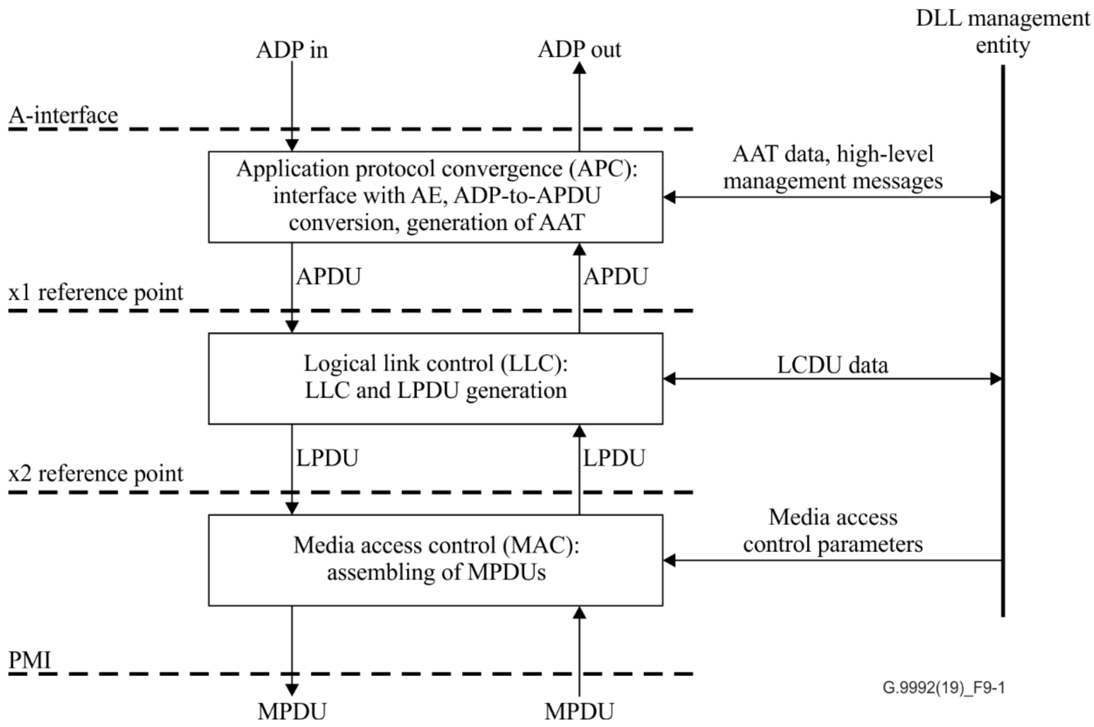


Figure 9-1 – Functional model of the DLL

In the transmit direction, application data primitives (ADPs) enter the DLL from the AE via the A-interface. Every incoming ADP set meets the format defined by the particular application protocol. For an Ethernet type AE, the ADP set has one of the standard Ethernet formats, as presented in Annex A (Ethernet APC). Each incoming ADP set is converted by the APC into application protocol data units (APDUs), which includes all parts of the ADP intended for communication to the destination node(s). The APC is responsible for forwarding APDUs to peers APCs.

The APC transfers APDUs to the LLC via the x1 reference point which is application independent. The LLC also receives from the DLL management entity, sets of management data primitives for LLC control frames which are mapped into link control data units (LCDU). The LLC is responsible for establishing the exchange of LCDUs (management frames) between peer LLCs.

In the LLC, the incoming APDU and LCDU are mapped into LLC frames. Each LLC frame is treated as an LLC protocol data units (LPDU) and then passed to the MAC via the x2 reference point.

The MAC is responsible for concatenating LPDUs into MPDUs and then conveying these MPDUs to the PHY via the PMI.

In the receive direction, MPDUs from the PHY enter via the PMI. The MAC disassembles the received MPDUs into LPDUs which are passed over the x2 reference point to the LLC. The LLC recovers the original APDUs and LCDUs from the received LPDUs, and conveys them to the APC and the LLC management entity, respectively. In the APC, the ADPs are recovered from the received APDUs and conveyed to the AE.

NOTE – No assumptions should be made on the partitioning of APC, LLC, and MAC in particular implementations; x1 and x2 are reference points and serve exclusively for the convenience of system definition.

9.1.1 Application protocol convergence sublayer

The functional model of the application protocol convergence (APC) is presented in Figure 9-2. It is intended to describe in more detail the APC functional block presented in Figure 9-1.

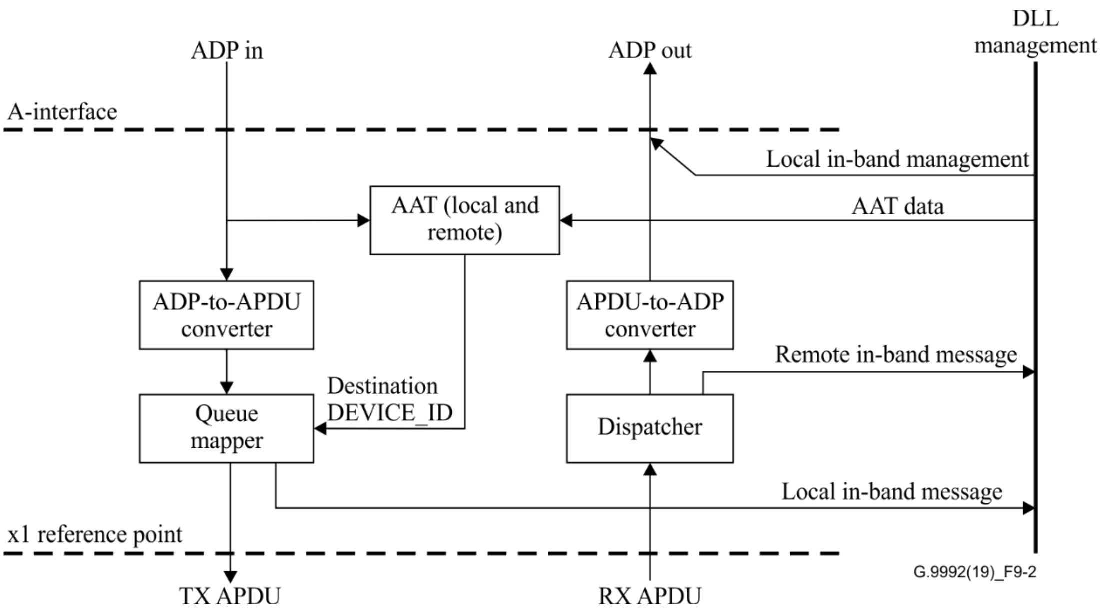


Figure 9-2 – Functional model of the APC

In the transmit direction, the incoming ADP data unit is converted into an APDU as defined in Annex A. The queue mapper maps APDUs into queues depending on their destination DEVICE_ID. After mapping, each APDU is sent to the LLC via the x1 reference point.

The data units of the in-band management messages arriving across the A-interface and addressed to the local node are directed to the DLL management entity ("Local in-band management", at the bottom of Figure 9-2). The in-band management messages generated by DLL management entity for the remote AE are converted to APDUs, and sent across the x1 reference point ("Remote in-band management" at the top of Figure 9-2).

In the receive direction, the APDUs incoming via the x1 reference point are converted back into the ADP set of the corresponding application protocol.

If addressed to the node, APDUs carrying in-band management messages from the remote AE are dispatched to the DLL management entity ("Remote in-band management" at the bottom of Figure 9-2). If addressed to the local AE, APDUs carrying in-band management messages from the remote AE are converted to a standard ADP and passed to A-interface. The in-band management messages (e.g., responses) generated by DLL management entity for the local AE are sent to the AE across the A-interface as standard sets of data unit primitives ("Local in-band management" at the top of Figure 9-2).

The local address association table (LAAT) contains in its first entry the MAC address of the node itself (i.e., REGID) and, in the rest of the table, the MAC addresses of the clients associated with the node. This data is collected from the incoming ADP data units. LAAT data is passed to the DLL management entity for network management purposes (see clause 8.5.3).

The remote address association table (RAAT) stores MAC addresses of other nodes in the domain.

The address association table (AAT) is formed by the aggregation of LAAT and RAAT.

9.1.2 Logical link control sublayer

The functional model of the LLC is presented in Figure 9-3. It is intended to describe in more detail the LLC functional block presented in Figure 9-1.

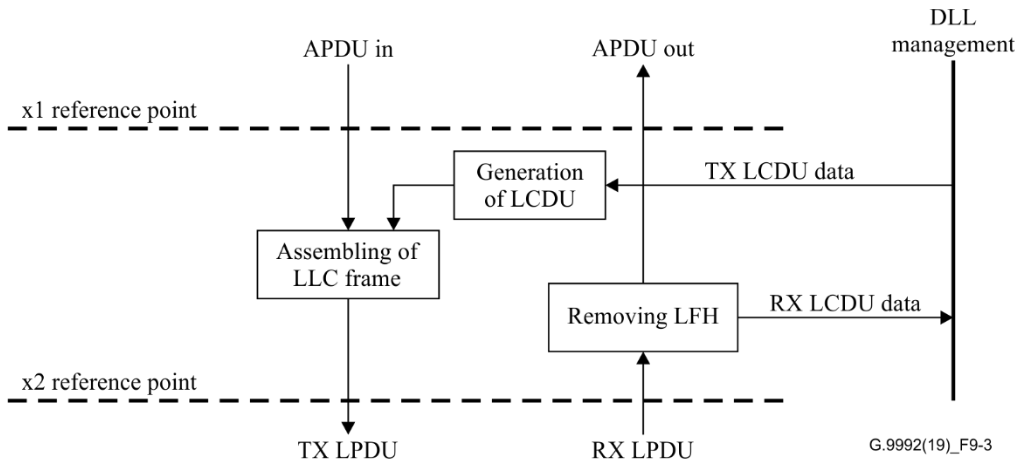


Figure 9-3 – Functional model of LLC

In the transmit direction, an LLC frame is formed from each APDU entering via the x1 reference point. Each LLC frame is treated as an LPDU.

The LCDU carries management data and has a format as defined in clause 9.1.2.1.3.

In the receive direction, the LPDUs disassembled from the incoming MPDU in the MAC and enter the LLC via the x2 reference point. The LLC then recovers the LLC frames from the received LPDUs. The payloads of the recovered LLC frames are passed to the APC via an x1 reference point, if they were carrying an APDU or to the DLL management, if they were carrying an LCDU.

9.1.2.1 LLC frame format

The LLC frame is formed from either an APDU or an LCDU, with a format as described in Figure 9-4.

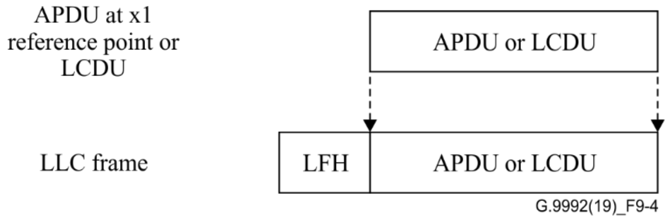


Figure 9-4 – LLC frame format

9.1.2.1.1 LLC frame header

The LLC frame header (LFH) shall be composed of the fields described in Table 9-1. The LFH is variable in length. Octet 0 shall be passed to the MAC first.

Table 9-1 – LFH fields format

Field	Octet	Bits	Definition
LLCFT	0 and 1	[2:0]	LLC frame type
FLEN		[15:3]	LLC frame body length in bytes
OriginatingNode	2	[7:0]	DEVICE_ID of the node that created the LLC frame
DestinationNode	3	[7:0]	Destination identifier that indicates the node(s) where the LLC frame is finally destined.

9.1.2.1.1.1 LLC frame type (LLCFT)

The LLCFT field is a 4-bit field that indicates the type of APDU that makes up the LLC frame. It is formatted as a 3-bit unsigned integer. Table 9-2 lists the valid LLC frame types.

Table 9-2 – LLC frame types

LLC frame type	Value
Padding frame	0
Management frame (LCDU)	1
Data frame (APDU)	2
Reserved	3-7

9.1.2.1.1.2 Frame length

The frame length (FLEN) field indicates the length in bytes of the frame contained within the LLC frame. This is the actual length of the LLC frame excluding the LFH. It is formatted as a 13-bit unsigned integer.

9.1.2.1.1.3 OriginatingNode

The OriginatingNode field carries the DEVICE_ID of the node that originated the LLC frame. For unidirectional broadcasting mode, the OriginatingNode field shall be set to 1, which indicates the DEVICE_ID of the domain master.

9.1.2.1.1.4 DestinationNode

The DestinationNode field indicates one or more nodes where the LLC frame is finally destined. It shall be set to BROADCAST_ID by the originating node.

9.1.2.1.2 LCDU frame format

The LCDU frame format, including the size of the fields, shall be as presented in Figure 9-5.

	LSB MSB
6 octets	Destination (MAC address)
6 octets	Source (MAC address)
2 octets	EtherType ($22E3_{16}$)
6 to 1500 octets	LCDU payload
	PAD
4 octets	FCS

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Figure 9-5 – LCDU format

The LCDU is identified at the destination node by its source/destination MAC address. The EtherType field is intended to identify the management message. The content of the EtherType field shall be $22E3_{16}$.

The PAD field shall complete the total length of LCDU to its minimum value of 64 bytes. The PAD field, if present, shall be set to zero.

The frame check sequence (FCS) shall be computed over all LCDU fields, from the first bit (LSB) of the destination MAC address field to the last bit (MSB) of the PAD using the standard IEEE 802.3 Ethernet 32-bit FCS computation algorithm. The FCS field shall not be included when MIC is used in the LLC frame encapsulating the LCDU.

Bits of LCDU shall be transmitted starting from the first octet of the destination MAC address.

The encapsulation of LCDUs into LLC frames is described in Figure 9-6.

NOTE – The format of the LCDU payload is for further study.

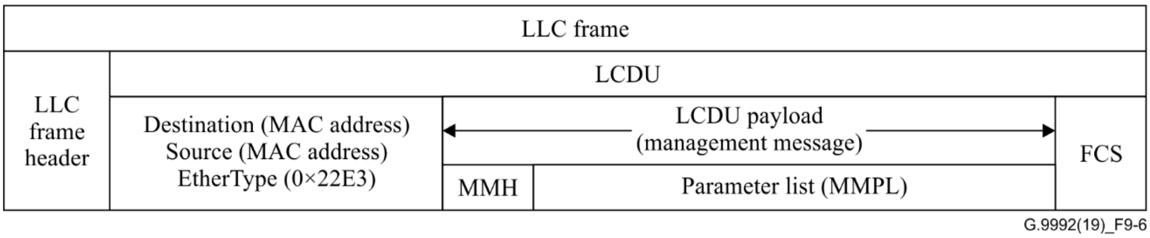

Figure 9-6 – Encapsulation of an LCDU into an LLC frame

9.1.2.1.3 APDU frame format

APDU frame format are presented in Annex A.

9.1.3 Medium access control sublayer

The functional model of the MAC is presented in Figure 9-7. It is intended to describe in more detail the MAC functional block presented in Figure 9-1.

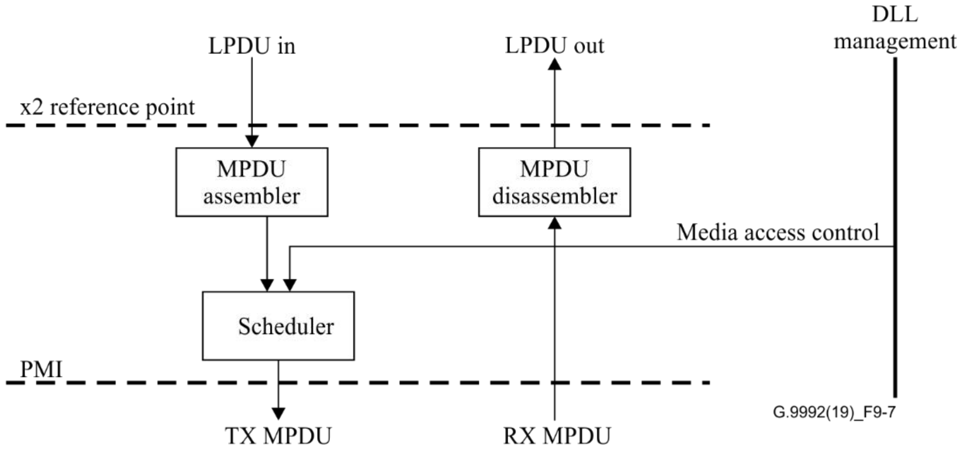

Figure 9-7– Functional model of MAC

In the transmit direction, MPDUs are assembled from LPDUs passed over the x2 reference point. The MPDU is then passed to the PHY across the PMI. The octet 0 of the LPH of the LPDU#1 of the MPDU (see Figure 9-8) shall be passed to the PHY first.

In the receive direction, the incoming MPDU is disassembled and the resulting LPDUs are passed to the LLC over the x2 reference point.

9.1.3.1 Assembling of MPDUs

The process of assembling an MPDU from one or more LPDUs is presented in Figure 9-8.

To form the MPDU, LPDUs are concatenated by the MAC in the same order as received across the x2 reference point

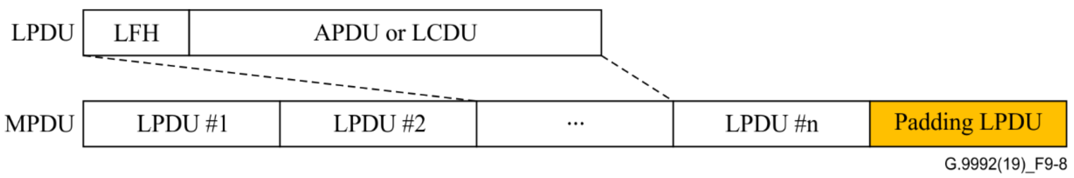

Figure 9-8 – Assembling of an MPDU from LPDUs

Padding LPDUs, if present, shall be placed at the end of the MPDU, see Figure 9-8, and shall be indicated as "padding frame" in the LLC frame header (see clause 9.1.2.1.1.1).

9.2 Addressing scheme

9.2.1 Node identifier

The following two node identification parameters shall be used:

– DEVICE_ID;

– BROADCAST_ID.

The DEVICE_ID shall be represented by an 8-bit unsigned integer with valid values in the range from zero to 250 as presented in Table 9-3. When a node decides to start a new domain by becoming its domain master, it shall have an assigned DEVICE_ID, which shall be 1. For unidirectional broadcasting mode, all the endpoint node shall set the DEVICE_ID to the default DEVICE_ID. A BROADCAST_ID is a DEVICE_ID with a fixed value of 255 and shall be used for broadcast transmission only.

Table 9-3 – Definition and valid values of node identification parameters

Parameter	Valid values	Description
DEVICE_ID	0	The default DEVICE_ID
	1	ID reserved for the domain master
	2 to 254	Reserved by ITU-T
BROADCAST_ID	255	A special value of DEVICE_ID reserved for broadcast

9.2.2 Address association table

Each node can have one or more applications associated with its AE (above its A-interface). Each application is identified by a unique 6-octet MAC address. Each node shall maintain the full list of MAC addresses associated with applications above its A-interface as well as its own MAC address. This list is referred to as an LAAT.

NOTE 1 – The list of MAC addresses associated with applications above its A-interface for a node can be populated by learning, or directly programmed by the DLL management entity.

Each node shall also maintain the list of MAC addresses associated with the AEs of other nodes in the domain and the MAC addresses of those nodes. This list is referred to as an RAAT.

The AAT is formed by the aggregation of the LAAT and the RAAT.

NOTE 2 – The routing of ADPs is for further study.

Annex A

Application protocol convergence sublayer

(This annex forms an integral part of this Recommendation.)

The application protocol convergence (APC) specific sublayer maps the primitives of the application protocol used by the application entity (AE) into the native protocol of the data link layer. It is the responsibility of the APC to convert incoming data units of the particular application protocol used by the AE into application protocol data units (APDUs) and map them onto the queues.

By default, APC shall support Ethernet, while other protocols can also be supported.

The description of APC in this annex is partitioned into a data plane and a management plane. The data plane part specifies converging of the AE data units into APDUs and back. The functional model of the data plane is presented in Figures 9-1 and 9-2. The part dealing with management plane specifies APC primitives and protocols related to APC peer-to-peer management.

A.1 Ethernet APC

The Ethernet APC (EAPC) is intended to operate with an Ethernet AE which supports IEEE bridging and switching protocols such as [IEEE 802.1D], [IEEE 802.1Q], [IEEE 802.1ad] (QinQ). Inter-domain bridging and bridging to alien domains implemented by the AE are beyond the scope of this Recommendation. The APC converts the standard set of primitives (at the MAC SAP, in terms of [IEEE 802.3], and those defined as internal sublayer services in terms of [IEEE 802.1]) at the A-interface into an APDU, which is further communicated through the domain to the peer APC. The APC shall accommodate the differences in primitive sets of different versions of [IEEE 802.3] and [IEEE 802.1] by substituting default values, as described in clause A.1.1.

A.1.1 Frame conversion

The incoming set of primitives (AIF_DATA.REQ) and the outgoing set of primitives (AIF_DATA.IND) at the A-interface of EAPC represent a sequence of Ethernet frames, each defined as a set of IEEE 802.1 primitives of M_UNITDATA.request and M_UNITDATA.indication, respectively, Table A.1.

Table A.1 – A-interface primitives description

AIF_DATA.REQ (AE → EAPC)	**AIF_DATA.IND (EAPC → AE)**
M_UNITDATA.request (frame_type, destination_address, source_address, mac_service_data_unit, user_priority, access_priority, frame_check_sequence)	M_UNITDATA.indication (frame_type, destination_address, source_address, mac_service_data_unit, user_priority, frame_check_sequence)

All unit-signal primitives specified in Table A.1 shall be interpreted in terms of clause 6.4 of [IEEE 802.1D]. Note that primitives frame_type, user_priority, access_priority, and frame_check_sequence, may not be provided by the AE, and primitives frame_type and user_priority may not be requested by the AE.

NOTE 1 – Clause 6.5.1 of [IEEE 802.1D] suggests that the "access priority" primitive be ignored and the frame_type primitive be set to user_data_type for IEEE 802.3 MAC frames.

NOTE 2 – The M_UNITDATA.request description in [IEEE 802.1Q] differs from that in [IEEE 802.1D] as it omits the frame_type and access_priority parameters. The frame_type is not required in [IEEE 802.1Q] as the receipt of a frame other than a user data frame does not cause a data indication, nor are such frames transmitted by the medium independent bridge functions. The mapping of M_UNITDATA.request to particular access methods specified in [IEEE 802.1Q] includes derivation of the access_priority parameter (for those media that require it) from the user_priority parameter.

NOTE 3 – The EM_UNITDATA.request and EM_UNITDATA.indication description in [IEEE 802.1ad] includes more quality of service related primitives, such as drop_eligible and others. These primitives, similarly to those defined in clause 6.6.1 of [IEEE 802.1Q] should be accommodated in the corresponding tags fields of the APDU as described in Table A.1.

If the frame_check_sequence primitive is provided by the AE, the incoming M_UNITDATA.request primitives (described in Table A.1 for AIF_DATA.REQ) shall be verified to be error free by computing their frame check sequence (FCS) as defined in clause 6.5.1 of [IEEE 802.1D]. If the computed FCS does not match the received value of the frame_check_sequence, the incoming primitive shall be discarded. If the frame_check_sequence primitive is not provided by the AE, the APC shall compute the FCS of the incoming M_UNITDATA.request primitives as defined in clause 3.28 of [IEEE 802.3].

Error-free primitives described in Table A.1 for AIF_DATA.REQ shall be converted into the APDU format presented in Figure A.1. The same APDU format shall be used for in-band management messages sourced by the local DLL management entity for the remote AE.

6 octets	Destination address
6 octets	Source address
2 octets	MAC client length/EtherType
Application dependent	Service data unit (APDU payload)
4 octets	Frame check sequence (FCS)

Figure A.1 – APDU format (TX and RX)

All fields shall have the same content as the corresponding fields of the MAC frame defined in [IEEE 802.3].

When sending a broadcast in-band management message (e.g., message addressed to all ITU-T G.9992 nodes), the EtherType tag shall be set to 22E316.

Bits of APDU shall be transmitted starting from the first octet of the destination address. The least significant bit of each octet shall be transmitted first. The most significant octet of each field shall be transmitted first.

The order of outgoing APDUs at the x1 reference point associated with a particular destination shall be the same as the order of incoming unit-data of the same destination.

The M_UNITDATA.indication primitives shall be derived from the APDUs received from the LLC across the x1 reference point as defined in clause 6.4.1 of [IEEE 802.1D], with the following additional rules:

– The frame_check_sequence primitive, if FCS is not a part of APDU, it shall be computed as defined in clause 3.28 of [IEEE 802.3].
– The frame_check_sequence primitive, if FCS is a part of APDU, it shall be verified as defined in clause 6.5.1 of [IEEE 802.1D]. APDUs that did not pass verification shall be discarded.

The same rules shall also be used to derive the M_UNITDATA.indication primitives for the in-band management messages sourced by the DLL management entity for the local AE.

The payload of in-band management data units generated by the DLL management entity shall follow the link control data unit (LCDU) payload format defined in clause 9.1.2.1.2.

A.1.2 Management plane

The management plane of the EAPC is for further study.

A.2 Other types of APC

Other types of APC are for further study.

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