I n t e r n a t i o n a l   T e l e c o m m u n i c a t i o n   U n i o n

ITU-T

TELECOMMUNICATION
STANDARDIZATION SECTOR
OF ITU

G.8261/Y.1361

Amendment 1
(07/2010)

SERIES G: TRANSMISSION SYSTEMS AND MEDIA, DIGITAL SYSTEMS AND NETWORKS

Packet over Transport aspects – Quality and availability targets

SERIES Y: GLOBAL INFORMATION INFRASTRUCTURE, INTERNET PROTOCOL ASPECTS AND NEXT-GENERATION NETWORKS

Internet protocol aspects – Transport

Timing and synchronization aspects in packet networks

Amendment 1: Network jitter limits for the synchronous Ethernet equipment clock interface and other clarifications

Recommendation ITU-T G.8261/Y.1361 (2008) – Amendment 1

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Recommendation ITU-T G.8261/Y.1361

Timing and synchronization aspects in packet networks

Amendment 1

Network jitter limits for the synchronous Ethernet equipment clock interface and other clarifications

Summary

Amendment 1 to Recommendation ITU-T G.8261/Y.1361:

– aligns the Recommendation to the new ITU-T G.826x document structure by moving the definitions into ITU-T G.8260;
– defines the EEC interface network jitter limits;
– clarifies some aspects related to reduced synchronous Ethernet function and to the EEC network limits;
– clarifies several aspects related to Appendix VI, *Measurement guidelines for packet-based methods*.

History

Edition	Recommendation	Approval	Study Group
1.0	ITU-T G.8261/Y.1361	2006-05-22	15
1.1	ITU-T G.8261/Y.1361 (2006) Cor. 1	2006-12-14	15
2.0	ITU-T G.8261/Y.1361	2008-04-29	15
2.1	ITU-T G.8261/Y.1361 (2008) Amend. 1	2010-07-29	15

FOREWORD

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The World Telecommunication Standardization Assembly (WTSA), which meets every four years, establishes the topics for study by the ITU-T study groups which, in turn, produce Recommendations on these topics.

The approval of ITU-T Recommendations is covered by the procedure laid down in WTSA Resolution 1.

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NOTE

In this Recommendation, the expression "Administration" is used for conciseness to indicate both a telecommunication administration and a recognized operating agency.

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As of the date of approval of this Recommendation, ITU had received notice of intellectual property, protected by patents, which may be required to implement this Recommendation. However, implementers are cautioned that this may not represent the latest information and are therefore strongly urged to consult the TSB patent database at http://www.itu.int/ITU-T/ipr/.

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Recommendation ITU-T G.8261/Y.1361

Timing and synchronization aspects in packet networks

Amendment 1

Network jitter limits for the synchronous Ethernet equipment clock interface and other clarifications

1) Clause 2 – References

Add the following references:

[ITU-T G.8260] Recommendation ITU-T G.8260 (2010), *Definitions and terminology for synchronization in packet networks*.

[ITU-T G.8265] Recommendation ITU-T G.8265/Y.1365 (2010), *Architecture and requirements for packet based frequency delivery*.

2) Clause 3 – Definitions

a) *Add the following definitions in clause 3.1:*

packet-based method: See [ITU-T G.8260].

packet-based method without timing support from the network: See [ITU-T G.8260].

packet-based method with timing support from the network: See [ITU-T G.8260].

b) *Replace:*

packet network timing function (PNT-F): The set of functions within the IWF that supports the synchronization network clock domain (see Figure B.2). This includes the function to recover and distribute the timing carried by the synchronization network. The PNT-F clocks may be part of the IWF or may be part of any other network element in the packet network.

When the PNT-Fs are part of the IWF they may support the CES IWF and/or change the layer over which timing is carried (i.e., from packet to physical layer and vice versa).

with:

packet network timing function (PNT-F): See [ITU-T G.8260].

c) *Replace*

adaptive clock recovery: Clock recovery technique that does not require the support of a network-wide synchronization signal to regenerate the timing. In this case the timing recovery process is based on the (inter-)arrival time of the packets (e.g., timestamps or CES packets). The information carried by the packets could be used to support this operation. Two-way or one-way protocols can be used.

with:

adaptive clock recovery: See [ITU-T G.8260].

3) Clause 9 – Network limits

a) *Add the following note after the first sentence of clause 9.2.1:*

NOTE – These limits are generally applicable at all points in the synchronization network. In some application cases, mainly in the access network, it might be possible to recover timing from an Ethernet signal that is generating jitter and wander according to the tolerance characteristics of the connected equipment (see Appendix IV for examples of relevant applications). The usage of an Ethernet link that does not comply with the limits defined in this clause is under the operator responsibility.

b) *Add the following text at the end of clause 9.2.2.1:*

Further examples of network limits specifically applicable to the wireless applications are described in clause IV.2.3.

c) *Replace Table 7 with the following tables:*

Table 7 – EEC interface network jitter limits

Interface	Reference	
2 048 kbit/s	See ITU-T G.823, clause 6.1: Network limits for output jitter at synchronization interfaces, SEC requirements	(Note 1)
2 048 kHz		
1 544 kbit/s	See ITU-T G.824, clause 6.1: Network limits for jitter	
STM-n	See ITU-T G.825, clause 5.1: Network limits for jitter	
Ethernet (synchronous Ethernet)	See Table 7a	(Note 2)
NOTE 1 – Jitter limits are taken from ITU-T G.823, ITU-T G.824 and ITU-T G.825 in order to allow proper interoperability with SEC based synchronization networks and combined EEC-SEC functions. NOTE 2 – In a chain of n ($n \leq 20$) connected EECs, the accumulated network jitter has to be low enough to allow all involved EECs to meet the output jitter specification at their synchronization outputs (e.g., 2048 kHz, 2048 kbit/s, 1544 kbit/s). See Figure 16 showing EECs in a chain; see also Annex D.		

Table 7a – Maximum permissible jitter at synchronous Ethernet network interfaces

Interface	Measurement bandwidth, –3 dB frequencies	Peak-to-peak amplitude (UIpp)
1 G (Notes 1, 2, 4)	2.5 kHz to 10 MHz	1.5
10 G (Notes 1, 3, 4)	20 kHz to 80 MHz	1.5
NOTE 1 – There is no specific high band jitter requirement for synchronous Ethernet. The relevant IEEE 802.3 jitter requirements shall be met in addition to the specific synchronous Ethernet wideband jitter requirements specified in this table. NOTE 2 – 1 G includes 1000BASE-KX, -SX, -LX; multi-lane interfaces are for further study. NOTE 3 – 10 G includes 10GBASE-SR/LR/ER, 10GBASE-LRM, 10GBASE-SW/LW/EW; multi-lane interfaces are for further study. NOTE 4 – 1 G: 1 UI = 0.8 ns 10 G (10GBASE-SR/LR/ER,-LRM): 1 UI = 96.97 ps 10 G (10GBASE-SW/LW/EW): 1 UI = 100.47 ps		

4) Clause 12 – Results and consequences of the different synchronization methods over packet network reference models

a) *Add the following paragraph at the beginning of clause 12.2.2:*

[ITU-T G.8265] describes the general architecture of frequency distribution using packet-based methods.

b) *Replace the reference to ITU-T Y.1540 with a reference to ITU-T G.8260 in Note 1 of clause 12.2.2:*

NOTE 1 – The terms packet delay and packet delay variation (PDV) used in this Recommendation are based on definitions provided in ~~[ITU-T Y.1540]~~[ITU-T G.8260].

5) Annex A – Proposed network architecture for synchronous Ethernet

Add the following text and tables after Table A.1:

In addition to a synchronous Ethernet port that is capable of both transmitting and receiving timing, it is possible to consider ports that provide a reduced synchronous Ethernet function. Reduced synchronous Ethernet functionality means the ability to support synchronization in a single direction only. There are two possible types of reduced synchronous Ethernet interfaces:

1) Synchronous Ethernet transmit only port: Such a port performs all synchronous Ethernet transmit functions, i.e., transmits QL messages over ESMC, and transmits the physical EEC clock via the Ethernet line.

2) Synchronous Ethernet receive only port: Such a port performs all synchronous Ethernet receive functions, i.e., receives and processes QL messages over ESMC and recovers the physical Ethernet line clock, providing it as a synchronization candidate.

The use of nodes with reduced synchronous Ethernet functionality has to be carefully considered in the synchronization network planning. Such nodes are expected to be used at the end of a synchronization chain.

Table A.1a – Synchronous Ethernet reduced functionality with QL enabled

Interface type	Operation mode	QL process	ESMC process
Synchronous Ethernet reduced functionality (QL enabled)	Synchronous mode (Tx only)	Active (Tx side only)	Tx side: Yes Rx side: Optional
	Synchronous mode (Rx only)	Active (Rx side only)	Rx side: Yes Tx side: Optional

Table A.1b – Synchronous Ethernet reduced functionality with QL disabled

Interface type	Operation mode	QL process	ESMC process
Synchronous Ethernet reduced functionality (QL disabled)	Synchronous mode (Tx only)	Inactive	Optional
	Synchronous mode (Rx only)	Inactive	Optional

6) Appendix IV – Applications and use cases

a) *Modify the following paragraph in clause IV.1 as follows:*

Frequency synchronization relates to the alignment of clocks in frequency, a process that is also referred to as syntonization. Phase synchronization and time synchronization are defined in [ITU-T G.8260]. ~~Phase synchronization implies that the two clocks are aligned in phase, a process that also referred to as relative time synchronization. Time synchronization is also referred to as time-of-day synchronization or wall-clock synchronization where the clocks in question are traceable to a common, universal, time-base such as UTC. Note that if two clocks are synchronized in time/phase then they are also synchronized in frequency~~. For some applications frequency synchronization may be adequate; for others a combination of frequency and time/phase may be required. For some applications, the source of time/timing may be specified, and for others the source could be any one of a set of (master) clocks.

b) *Add the following text after the first paragraph in clause IV.2.3 (Remarks):*

In general, on the long term, the reference timing signal may be allowed to drift *n* ppb provided that this is sufficiently below the maximum allowed deviation (i.e., *n* ppb << 50 ppb << 100 ppb, or << 250 ppb for the different cases). This would result in a tolerance MTIE mask where the limits on the short term are set by the ITU-T G.823 and G.824 traffic mask and on the long term by a *n* ppb line (where *n* shall be below the applicable requirement on the radio interface).

NOTE – It has been reported that there are cases of base stations that are less tolerant to wander on the short term than what is specified by ITU-T G.823 and G.824 traffic masks.

7) Appendix VI – Measurement guidelines for packet-based methods

a) *Add the following text at the end of clause VI.2:*

The traffic inserted into the packet switched network in some of the test cases (such as 2, 3, 13 and 14) may lead to very low frequency variation on the timing information carried by the timing packets. In this case, in order to attenuate, filter or suppress such low frequency effects the CES slave, PSC-A or PEC-S may require low frequency filtering capability.

b) *Add the following note in the Traffic model definition before Note 2 in clause VI.2:*

NOTE 1A – Different interpretations on how the traffic bursts are generated in the following network traffic models have been proposed. The test result may depend on the specific interpretation that has been adopted.

c) *Update the first sentence of the note in clause VI.2.2 to read:*

"NOTE – Traffic Model 1 is based on the typical traffic characteristics of wireless access networks that are based on the first generations of mobile technologies (e.g., GSM, WCDMA 3GPP releases up to Rel 4). ..."

d) *Update Test Case 17 in clause VI.5.2.7 as follows:*

VI.5.2.7 Test Case 17

Test Case 17 models routing changes caused by failures in the network.

Test Case 17 must use the following network conditions:

- Change the number of switches between the DUTs, causing a step change in packet network delay. The packets to load the network must use Network Traffic Model 1 as defined in clause VI.2.1:
  - Update the test set up in Figure VI.10 adding a cable from switch in position "n" to switch in position "n+2" (Figure VI.13 shows an example where n=1 and switch 2 is bypassed). In this way the traffic is re-routed (in both directions) to bypass one switch in the traffic path. This shall be done either using a fibre spool or adding an impairment box able to simulate different cable lengths (10 µs and 200 µs can be simulated as

typical examples). The configuration shall be done so that the traffic flow under test is routed directly from switch in position "n" via the new link to switch in position "n+2".

– Start with 40% of network disturbance load in the forward direction and 30% load in the reverse direction.

– After a stabilization period according to Appendix II, disconnect the cable from switch "n" to switch "n+2", so that traffic under test will then be forced to go through switch in position "n+1" (Figure VI.14 shows an example where n=1, the cable from switch 1 to switch 3 is removed, and the connection to switch 2 is restored in order for the traffic to go through switch 2).

– Allow a stabilization period according to Appendix II for the clock recovery process to stabilize, and then reconnect the link that was disconnected in order to restore the traffic on the original path.

• Repeat the test in order to create a larger phase step:

  – Update the test set up in Figure VI.10 adding a cable from switch in position "n" to switch in position "n+4". In this way the traffic is re-routed (in both directions) to bypass three switches in the traffic path. This shall be done either using a fibre spool or adding an impairment box able to simulate different cable lengths (10 µs and 200 µs can be simulated as typical examples). The configuration shall be done so that the traffic flow under test is routed directly from switch in position "n" via the new link to switch in position "n+4".

  – Apply 40% of network disturbance load in the forward direction and 30% load in the reverse direction.

  – After a stabilization period according to Appendix II, disconnect the cable from switch "n" to switch "n+4" (so that traffic under test will then be forced to go through switch in position "n+1").

  – Allow a stabilization period according to Appendix II for the clock recovery process to stabilize, and then reconnect the link that was disconnected in order to restore the traffic on the original path.

• Repeat the test using the Network Traffic Model 2 as defined in clause VI.2.2 to load the network.

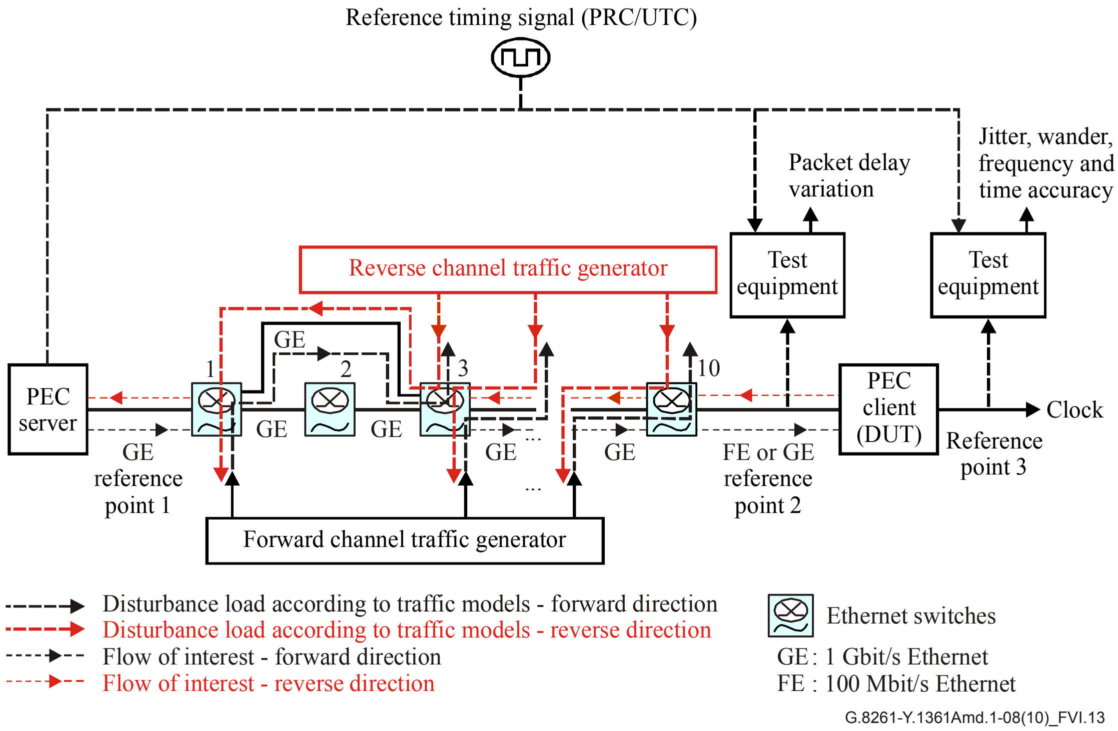

Figure VI.13 – Details of Test Case 17

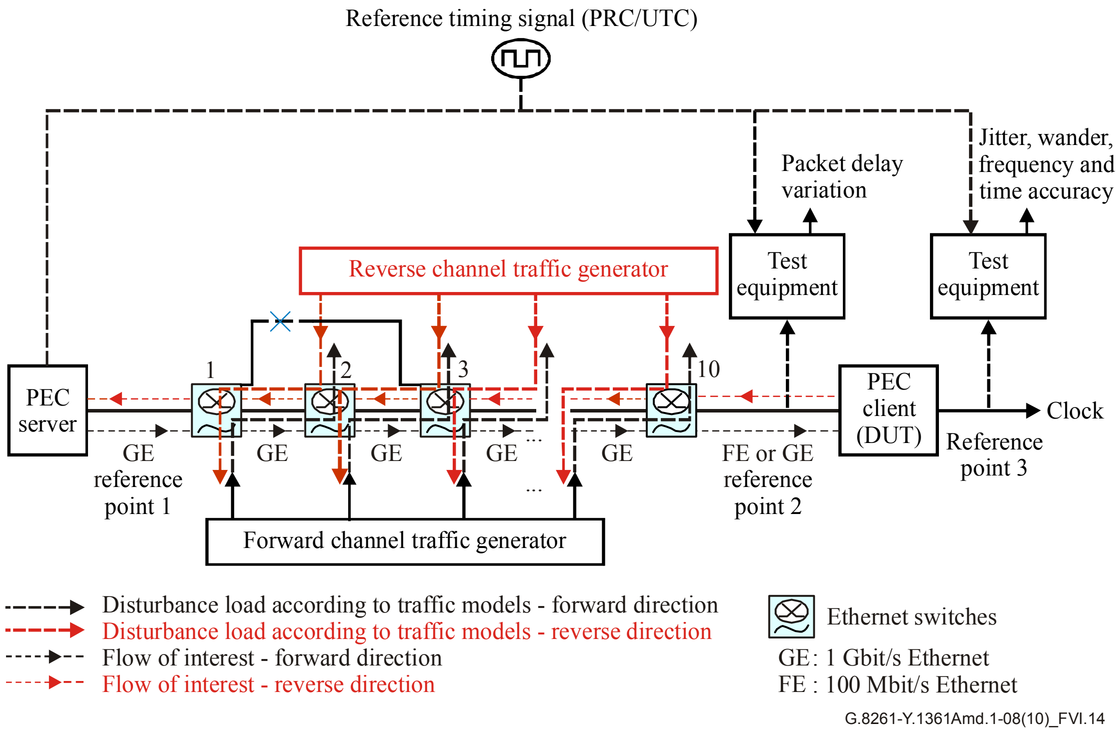

Figure VI.14 – Details of Test Case 17

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