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SERIES G: TRANSMISSION SYSTEMS AND MEDIA, DIGITAL SYSTEMS AND NETWORKS

Digital terminal equipments – Principal characteristics of multiplexing equipment for the synchronous digital hierarchy

Synchronization layer functions

Recommendation ITU-T G.781

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Recommendation ITU-T G.781

Synchronization layer functions

Summary

Recommendation ITU-T G.781 defines the atomic functions that are part of the two synchronization layers, the synchronization distribution (SD) layer and the network synchronization (NS) layer. It also defines some atomic functions, part of the transport layer, which are related to synchronization.

These functions describe the synchronization of SDH NEs and how SDH NEs are involved in Network Synchronization.

The specifications in this Recommendation are the superset of functionality of three regional standards bodies. Care should be taken when selecting from this Recommendation.

Not every atomic function defined in this Recommendation is required for every application. Different subsets of atomic functions may be assembled in different ways according to the combination rules given in Recommendation ITU-T G.783 to provide a variety of different capabilities. Network operators and equipment suppliers may choose which functions must be implemented for each application.

Source

Recommendation ITU-T G.781 was approved on 22 September 2008 by ITU-T Study Group 15 (2005-2008) under Recommendation ITU-T A.8 procedure.

FOREWORD

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The World Telecommunication Standardization Assembly (WTSA), which meets every four years, establishes the topics for study by the ITU-T study groups which, in turn, produce Recommendations on these topics.

The approval of ITU-T Recommendations is covered by the procedure laid down in WTSA Resolution 1.

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Synchronization layer functions

1 Scope

This Recommendation specifies a library of basic synchronization distribution building blocks, referred to as "atomic functions" and a set of rules by which they are combined in order to describe a digital transmission equipment's synchronization functionality. The library defined in this Recommendation forms part of the set of libraries defined furthermore in Recommendations [ITU-T G.783], [b-ITU-T G.705], [b-ITU-T G.798], [b-ITU-T G.8021] and [b-ITU-T G.8121]. The library comprises the functional building blocks needed to completely specify the generic functional structure of the ITU-T digital transmission hierarchy. Equipment that is compliant with these Recommendations should be describable as an interconnection of a subset of these functional blocks contained within these Recommendations. The interconnection of these blocks should obey the combination rules given in [ITU-T G.806]. The generic functionality is described in [ITU-T G.806].

The specifications in this Recommendation are the superset of functionality of three regional standards bodies. When different processing within a single atomic function is required to support the specific regional processing, this is identified by means of options I, II and III processing. "Option I" applies to networks optimized for the 2048 kbit/s hierarchy. "Option II" applies to networks optimized for the 1544 kbit/s hierarchy that include the rates 1544 kbit/s, 6312 kbit/s and 44 736 kbit/s. "Option III" applies to networks optimized for the 1544 kbit/s hierarchy that include the rates 1544 kbit/s, 6312 kbit/s, 33 064 kbit/s, 44 736 kbit/s and 97 728 kbit/s.

As a general rule, this Recommendation does not specify the atomic functions that are specific to PRC ([ITU-T G.811]) and SSU ([ITU-T G.812]) clock equipment; the SSM selection algorithm specified in this Recommendation is only generally applicable to SEC ([ITU-T G.813] and [ITU-T G.8262]) clock equipment. However, strictly for option II networks, there are some specific topologies listed containing both SEC and SSU clock equipment, for which the application of the SSM selection algorithm is described. The general case of using the SSM selection algorithm simultaneously in SSU and SEC clock equipment is for further study for all options.

2 References

The following ITU-T Recommendations and other references contain provisions which, through reference in this text, constitute provisions of this Recommendation. At the time of publication, the editions indicated were valid. All Recommendations and other references are subject to revision; users of this Recommendation are therefore encouraged to investigate the possibility of applying the most recent edition of the Recommendations and other references listed below. A list of the currently valid ITU-T Recommendations is regularly published. The reference to a document within this Recommendation does not give it, as a stand-alone document, the status of a Recommendation.

[ITU-T G.703] Recommendation ITU-T G.703 (2001), *Physical/electrical characteristics of hierarchical digital interfaces*.
<http://www.itu.int/rec/T-REC-G.703>

[ITU-T G.704] Recommendation ITU-T G.704 (1998), *Synchronous frame structures used at 1544, 6312, 2048, 8448 and 44 736 kbit/s hierarchical levels*.
<http://www.itu.int/rec/T-REC-G.704>

[ITU-T G.706] Recommendation ITU-T G.706 (1991), *Frame alignment and cyclic redundancy check (CRC) procedures relating to basic frame structures defined in Recommendation G.704*.
<http://www.itu.int/rec/T-REC-G.706>

[ITU-T G.707] Recommendation ITU-T G.707/Y.1322 (2007), *Network node interface for the synchronous digital hierarchy (SDH)*.
<http://www.itu.int/rec/T-REC-G.707>

[ITU-T G.775] Recommendation ITU-T G.775 (1998), *Loss of Signal (LOS), Alarm Indication Signal (AIS) and Remote Defect Indication (RDI) defect detection and clearance criteria for PDH signals*.
<http://www.itu.int/rec/T-REC-G.775>

[ITU-T G.783] Recommendation ITU-T G.783 (1997), *Characteristics of synchronous digital hierarchy (SDH) equipment functional blocks*.
<http://www.itu.int/rec/T-REC-G.783>

[ITU-T G.803] Recommendation ITU-T G.803 (2000), *Architecture of transport networks based on the synchronous digital hierarchy (SDH)*.
<http://www.itu.int/rec/T-REC-G.803>

[ITU-T G.806] Recommendation ITU-T G.806 (2006), *Characteristics of transport equipment – Description methodology and generic functionality*.
<http://www.itu.int/rec/T-REC-G.806>

[ITU-T G.810] Recommendation ITU-T G.810 (1996), *Definitions and terminology for synchronization networks*.
<http://www.itu.int/rec/T-REC-G.810>

[ITU-T G.811] Recommendation ITU-T G.811 (1997), *Timing characteristics of primary reference clocks*.
<http://www.itu.int/rec/T-REC-G.811>

[ITU-T G.812] Recommendation ITU-T G.812 (2004), *Timing requirements of slave clocks suitable for use as node clocks in synchronization networks*.
<http://www.itu.int/rec/T-REC-G.812>

[ITU-T G.813] Recommendation ITU-T G.813 (2003), *Timing characteristics of SDH equipment slave clocks (SEC)*.
<http://www.itu.int/rec/T-REC-G.813>

[ITU-T G.8261] Recommendation ITU-T G.8261/Y.1361 (2008), *Timing and synchronization aspects in packet networks*.
<http://www.itu.int/rec/T-REC-G.8261>

[ITU-T G.8262] Recommendation ITU-T G.8262/Y.1362 (2007), *Timing characteristics of synchronous Ethernet equipment slave clock (EEC)*.
<http://www.itu.int/rec/T-REC-G.8262>

[ITU-T G.8264] Recommendation ITU-T G.8264/Y.1364 (2008), *Distribution of timing information through packet networks*.
<http://www.itu.int/rec/T-REC-G.8264>

3 Terms and definitions

This Recommendation defines the following terms:

3.1 timing loop: This is a network condition where a slave clock providing synchronization becomes locked to its own timing signal. It is generally created when the slave clock timing information is looped back to its own input, either directly or via other network equipments. Timing loops should be prevented in networks by careful network design.

3.2 QL_minimum: QL_minimum is a configurable parameter used in the squelching of clock output signals. If the quality level of the signal used to derive the output falls below QL_minimum then the output will be squelched (cut-off or set to AIS).

3.3 clock-source quality-level: The clock-source quality-level of a SEC or SASE is defined as the grade of clock to which it is ultimately traceable, i.e., the grade of clock to which it is synchronized directly or indirectly via a chain of SECs and SASEs, however long this chain of clocks is. For example, the clock-source quality-level may be a primary reference clock complying with [ITU-T G.811], or it may be a slave clock in holdover-mode, complying with [ITU-T G.812], or a [ITU-T G.813] or [ITU-T G.8262] clock in holdover or free-run.

The clock-source quality-level is essentially, therefore, an indication only of the long-term accuracy of the NE clock.

3.4 station clock: This is a node clock as defined in [ITU-T G.810].

The functional definitions are given in [ITU-T G.783].

The symbols and diagrammatic conventions are given in [ITU-T G.783].

3.5 squelch: An action that cuts off (i.e., shuts down) an output signal. For some signals (e.g., 2 Mbit/s), squelching may be realized by means of inserting AIS instead of shutting down the signal.

3.6 synchronous equipment clock: A generic term representing both the SDH equipment clock ([ITU-T G.813]) and the ethernet equipment clock ([ITU-T G.8262]).

4 Abbreviations and acronyms

This Recommendation uses the following abbreviations and acronyms:

AI	Adapted Information
AIS	Alarm Indication Signal
AP	Access Point
BITS	Building Integrated Timing Supply
CI	Characteristic Information
CK	Clock signal (timing information)
CLR	Clear
CP	Connection Point
CS	Clock Source (timing information)
CSid	Clock Source identifier
DL	Data Link
DNU	Do Not Use
DUS	Do not Use for Sync
ES1	Electrical Section, level 1
ESF	Extended SuperFrame
ESMC	Ethernet Synchronization Messaging Channel
EXTCMD	EXTernal COMmand messaging channel
FS	Frame Start (timing information)

FSw	Forced Switch
HO	Hold-Off time
HO	HoldOver mode
ID	IDentifier
INVx	INValid x
LC	Layer Clock
LO	Locked mode
LO	LockOut
LOS	Loss Of Signal
LSB	Least Significant Bit
LTI	Loss of Timing Information
MA	Maintenance and Adaptation
MFP	MultiFrame Present
MFS	MultiFrame Start
MI	Management Information
MON	Monitored
MS	Multiplex Section
MSB	Most Significant Bit
MSw	Manual Switch
MTIE	Maximum Time Interval Error
NE	Network Element
NS	Network Synchronization
NSUPP	Not SUPPorted
OSn	Optical Section layer (STM-n)
P12s	2048 kbit/s PDH path layer with synchronous 125 µs frame structure according to [ITU-T G.704]
P31s	34 368 kbit/s PDH path layer with synchronous 125 µs frame structure according to [b-ITU-T G.832]
P4s	139 264 kbit/s PDH path layer with synchronous 125 µs frame structure according to [b-ITU-T G.832]
PDH	Plesiochronous Digital Hierarchy
PRC	Primary Reference Clock
PRS	Primary Reference Source
QL	Quality Level
RES	REServed for network synchronization use
RI	Remote Information
RSn	Regenerator Section layer STM-n

SASE	Stand Alone Synchronization Equipment
SD	Synchronization Distribution
SDH	Synchronous Digital Hierarchy
SDL	Specification and Description Language
SEC	Synchronous Equipment Clock
SF	Signal Fail
Sk	Sink
SMC	SONET Minimum Clock
So	Source
SQLCH	Squelch
SSF	Server Signal Fail
SSM	Synchronization Status Message
SSU	Synchronization Supply Unit
SSU-A	primary level SSU
SSU-B	secondary level SSU
ST2	STratum 2
ST3	STratum 3
ST3E	STratum 3 Enhanced
ST4	STratum 4
STM-N	Synchronous Transport Module, level N
STU	Synchronization Traceability Unknown
TCP	Termination Connection Point
TDEV	Time DEViation
TI	Timing Information
TL	Transport Layer
TM	Timing Marker
TNC	Transit Node Clock
TSF	Trail Signal Fail
TT	Trail Termination
UNC	UNConnected
UNK	UNKnown
VC-n	Virtual Container, level n
WTR	Wait To Restore

5 Synchronization principles

5.1 Network synchronization

Synchronization network architecture is specified in [ITU-T G.803].

Synchronization information is transmitted through the network via synchronization network connections. These synchronization network connections can transport different synchronization levels. Each synchronization network connection is provided by one or more synchronization link connection(s), each supported by a synchronized PDH trail, SDH multiplex section trail or IEEE 802.3 physical media trail.

Some of these synchronized PDH trail, SDH multiplex section trail, or IEEE 802.3 physical media trail signals contain a communication channel, the synchronization status message (SSM), the timing marker (TM) or the ethernet synchronization message channel (ESMC) transporting a quality level identifier. This quality level identifier can be used to select the highest synchronization level incoming reference signal from a set of nominated synchronization references available at the network element.

Synchronization network connections are unidirectional and generally point-to-multipoint. [ITU-T G.803] specifies a master-slave synchronization technique for synchronizing SDH networks and [ITU-T G.8261] specifies it for packet transport networks. Figures 1 to 4 illustrate the synchronization network connection model.

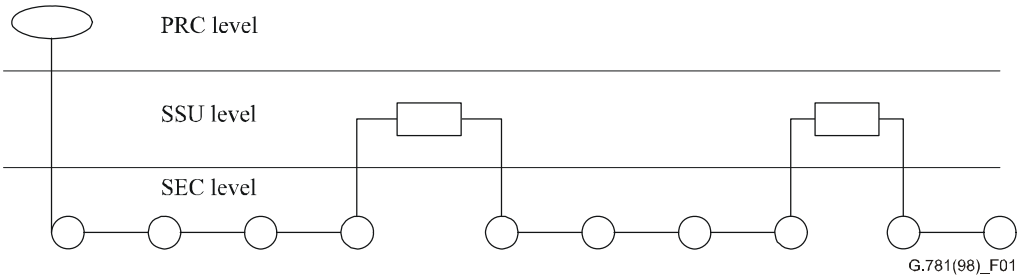


Figure 1 – General representation of a synchronization network

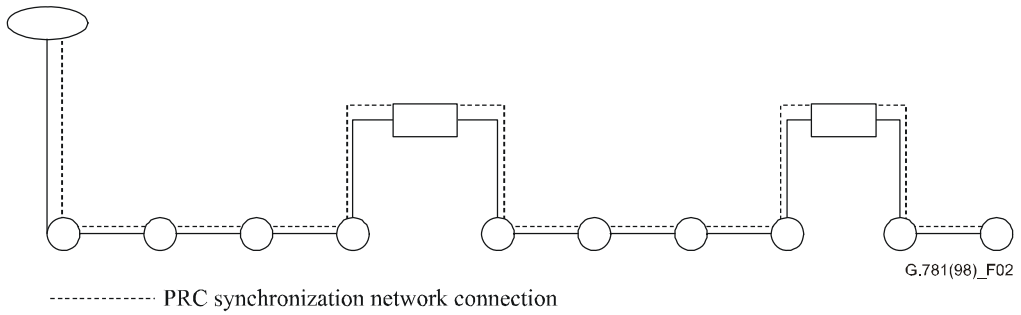


Figure 2 – Representation of the PRC network connection

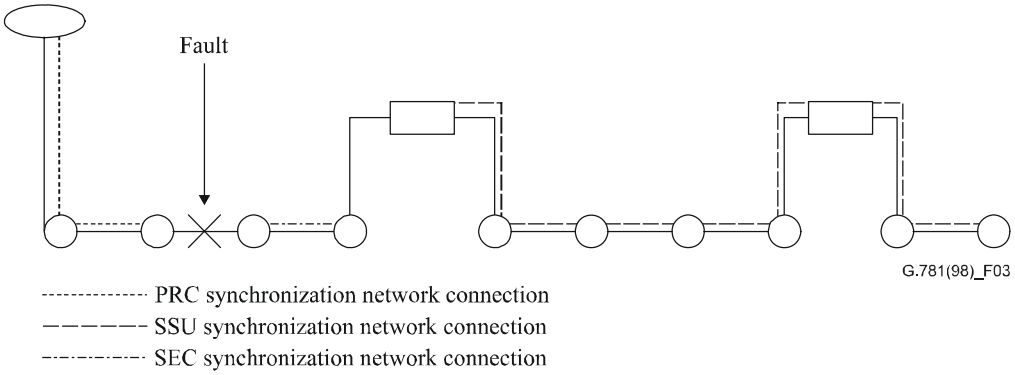


Figure 3 – Representation of the synchronization network connection in case of failure

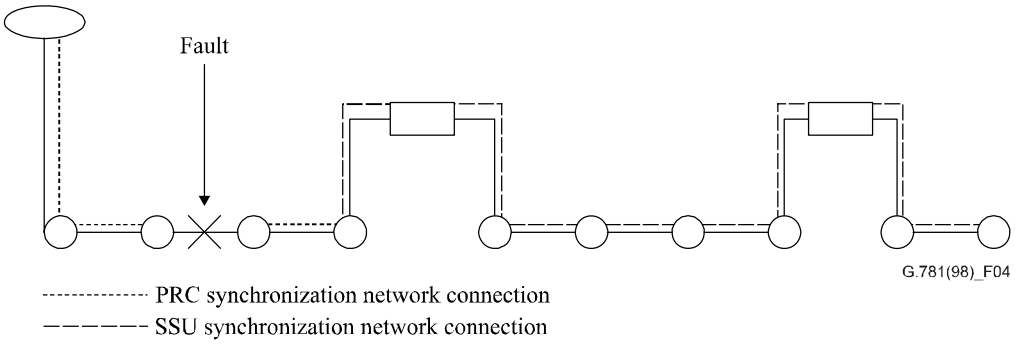


Figure 4 – Example of restoration of the synchronization

5.2 Synchronization distribution trails

Synchronization distribution trails transport timing between two adjacent equipments.

From a synchronization view point, adjacent network elements are those network elements that are interconnected via section signals. Between two such adjacent network elements (NEs), a unidirectional synchronization distribution trail exists.

An **SD trail** starts at the input of the SD_TT_So function and ends at the output of the SD_TT_Sk function.

An **SD link connection** transports synchronization timing information between two adjacent connection points (CPs) of the NS_C function.

An **NS network connection** transports synchronization timing information over a series of synchronization link connection (see Figure 5).

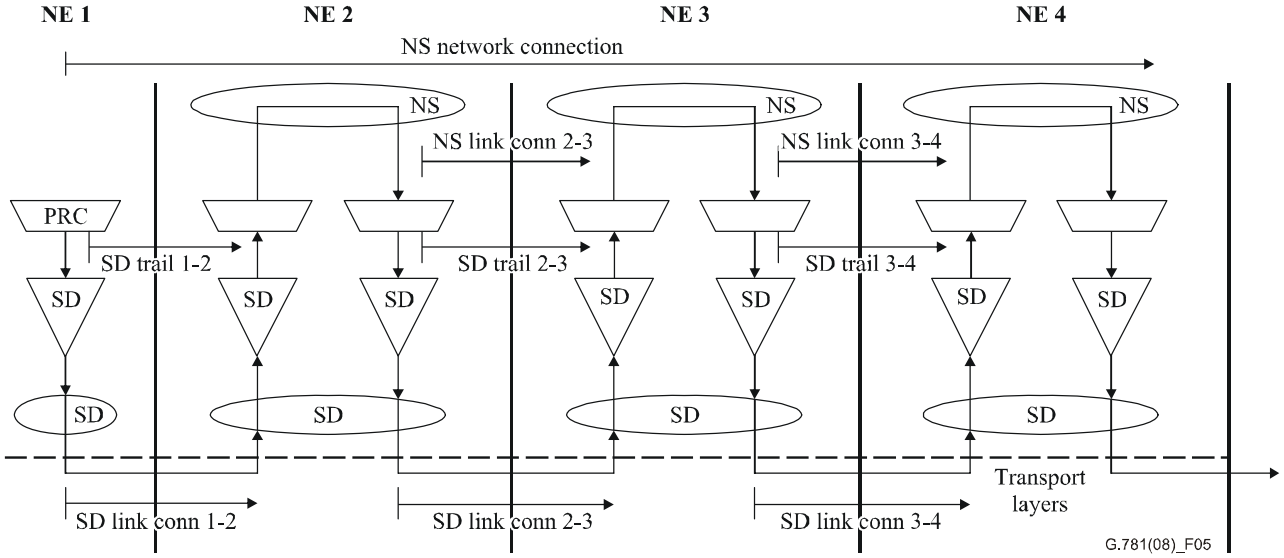


Figure 5 – Example of series of synchronization distribution network connection transporting PRC quality timing reference information

5.3 Synchronization interfaces

Synchronization trails can be carried through the network by a number of interfaces. Currently, the following signals are defined for such transport (refer also to Figures I.1 to I.4):

5.3.1 Overview

5.3.1.1 Option I synchronization networking

– Without traffic:
  - 2048 kHz (T12);
  - 2048 kbit/s (E12+P12s).

– With traffic:
  - 9 953 280 kbit/s (OS64+RS64+MS64);
  - 2 488 320 kbit/s (OS16+RS16+MS16);
  - 622 080 kbit/s (OS4+RS4+MS4);
  - 155 520 kbit/s (OS1 (or ES1)+RS1+MS1);
  - 139 264 kbit/s (E4+P4s);
  - 34 368 kbit/s (E31+P31s);
  - 2048 kbit/s (E12+P12s);
  - 100 000 kbit/s (ETY2[+ETH]);
  - 1 000 000 kbit/s (ETY3[+ETH]);
  - 10 000 000 kbit/s (ETY4[+ETH]).

NOTE – The ETYn synchronization interfaces are full duplex ones with continuous bit stream, as specified in [ITU-T G.8262].

5.3.1.2 Option II synchronization networking

– Without traffic:
  - 64 kHz (T01);
  - 1544 kbit/s (E11+P11s).

– With traffic:
  - 9 953 280 kbit/s (OS64+RS64+MS64);
  - 2 488 320 kbit/s (OS16+RS16+MS16);
  - 622 080 kbit/s (OS4+RS4+MS4);
  - 155 520 kbit/s (OS1 (or ES1)+RS1+MS1);
  - 1544 kbit/s (E11+P11s);
  - 100 000 kbit/s (ETY2[+ETH]);
  - 1 000 000 kbit/s (ETY3[+ETH]);
  - 10 000 000 kbit/s (ETY4[+ETH]).

NOTE – The ETYn synchronization interfaces are full duplex ones with continuous bit stream, as specified in [ITU-T G.8262].

5.3.1.3 Option III synchronization networking

– Without traffic:
  - 64 kHz (T02) [from SASE/BITS to NE];
  - 6312 kHz (T21) [from NE to SASE/BITS].

– With traffic:
  - 9 953 280 kbit/s (OS64+RS64+MS64);
  - 2 488 320 kbit/s (OS16+RS16+MS16);
  - 622 080 kbit/s (OS4+RS4+MS4);
  - 155 520 kbit/s (OS1 (or ES1)+RS1+MS1);
  - 100 000 kbit/s (ETY2[+ETH]);
  - 1 000 000 kbit/s (ETY3[+ETH]);
  - 10 000 000 kbit/s (ETY4[+ETH]).

NOTE – The ETYn synchronization interfaces are full duplex ones with continuous bit stream, as specified in [ITU-T G.8262]

5.3.2 STM-N

The STM-N transport signals carry (in addition to the payload) reference timing information and an indication of the quality level of the source generating this timing information, via the synchronization status message (SSM) as defined in [ITU-T G.707].

NOTE – Old equipment may not be able to support SSM via their STM-N interfaces.

5.3.3 2 Mbit/s

The 2 Mbit/s transport signals may carry (in addition to the payload) reference timing information.

The 2 Mbit/s timing reference signals (without payload) carry reference timing information to specific synchronization ports.

Both signals can carry an indication of the quality level of the source generating the timing information via the SSM as specified in [ITU-T G.704].

NOTE 1 – Old equipment may not be able to support SSM on their 2 Mbit/s interfaces.

NOTE 2 – The 2 Mbit/s timing reference signal can be connected to either a SASE/BITS or another NE. The SSM specifications in this version of this Recommendation include the interconnect between two NEs. The SSM processing with respect to the interface between NE and SASE is for further study.

5.3.4 2 MHz

Synchronization can be carried through 2 MHz signals to specific synchronization ports (so-called station clock ports). This signal does not carry an indication of the quality level of the source generating the timing information.

NOTE – The 2 MHz timing reference signal can be connected to either a SASE/BITS or another NE.

5.3.5 34 Mbit/s and 140 Mbit/s with 125 μs frame structure

34 Mbit/s and 140 Mbit/s signals with 125 μs frame structure as defined in [b-ITU-T G.832] carry a full 4-bit SSM code.

NOTE – For interworking with equipments compliant with the initial edition of [b-ITU-T G.832], new equipments should be able to be configured to recognize and generate the timing marker which is located in bit 8 of the MA (maintenance and adaptation) byte: the timing marker is set to "0" to indicate that the timing source is traceable to a primary reference clock (PRC), and is otherwise set to "1".

5.3.6 1.5 Mbit/s

The 1.5 Mbit/s transport signals may carry (in addition to the payload) reference timing information.

The 1.5 Mbit/s timing reference signals (without payload) carry reference timing information to specific synchronization ports.

Both signals can carry an indication of the quality level of the source generating the timing information via the SSM transported within the 1544 kbit/s signal's extended super frame (ESF) data link (DL) as specified in [ITU-T G.704].

NOTE 1 – The format of the data link messages in ESF frame format is "0xxx xxx0 1111 1111", transmitted right-most bit first. The 6 bits denoted "xxx xxx" contain the actual message; some of these messages are reserved for synchronization messaging. It takes 32 frames (i.e., 4 ms) to transmit all 16 bits of a complete DL word. Note that [ITU-T G.704] presents the data link messages in reverse order "1111 1111 0xxx xxx0".

NOTE 2 – Old equipment may not be able to support SSM on their 1.5 Mbit/s interfaces.

5.3.7 64 kHz

Within option II networks, synchronization can be carried through 64 kHz (T01) interface signals (see clause 4.2.2 of [ITU-T G.703] composite timing signal) to specific synchronization input ports (so-called station clock ports). This signal does not carry an indication of the quality level of the source generating the timing information.

Within option III networks, synchronization can be carried through 64 kHz (T02) interface signals (see Appendix II of [ITU-T G.703] composite timing signal) from the SASE to specific synchronization input ports (so-called station clock ports) on an NE. This signal does not carry an indication of the quality level of the source generating the timing information.

5.3.8 6312 kHz

Within option III networks, synchronization can be carried through 6312 kHz signals (see Appendix II of [ITU-T G.703]) from specific synchronization output ports (so-called station clock ports) on an NE to inputs of the SASE. This signal does not carry an indication of the quality level of the source generating the timing information.

5.3.9 100 Mbit/s, 1 Gbit/s, 10 Gbit/s

The IEEE 802.3 transport signals may carry (in addition to the payload) reference timing information, and an indication of the quality level of the source generating this timing information, via the synchronization status message (SSM) as defined in [ITU-T G.8264].

NOTE 1 – Equipment developed prior to this first revision of this Recommendation may not be able to carry reference timing information and/or support SSM via its IEEE 802.3 interfaces.

NOTE 2 – It is possible that equipment is equipped with both non-synchronous and synchronous IEEE 802.3 interfaces as defined in [ITU-T G.8264]. Non-synchronous IEEE 802.3 interfaces are excluded from the synchronization distribution process.

5.4 Clock-source quality-level

5.4.1 Clock-source quality-level definitions

SDH and packet transport networks throughout the world are based on different synchronization philosophies. Those differences are identified in this Recommendation as three options: I, II and III.

5.4.1.1 Option I synchronization networking

The following clock-source quality-levels are defined in the synchronization process of option I networks, corresponding to 4 levels of synchronization quality ([ITU-T G.803]).

QL-PRC: This synchronization trail transports a timing quality generated by a primary reference clock that is defined in [ITU-T G.811].

QL-SSU-A: This synchronization trail transports a timing quality generated by a type I or V slave clock that is defined in [ITU-T G.812].

QL-SSU-B: This synchronization trail transports a timing quality generated by a type VI slave clock that is defined in [ITU-T G.812].

QL-SEC: This synchronization trail transports a timing quality generated by a synchronous equipment clock (SEC) that is defined in [ITU-T G.813] or [ITU-T G.8262], option I.

QL-DNU: This signal should not be used for synchronization.

NOTE – The "unknown" quality level was defined to characterize the quality of an existing network. This QL is no longer supported by the SSM algorithm in option I networks. Instead, a synchronization reference input port which receives a signal without SSM can be provisioned to assume a quality level for that received signal (see clause 5.4.3).

5.4.1.2 Option II synchronization networking

Clock-source quality-levels of option II networks have been expanded from 7 levels to 9 levels. The 7 quality level set is referred to as first generation, and the new 9 quality level set is referred to as second generation. First generation quality levels are a subset of second generation quality levels.

The following clock-source quality-levels are defined in the synchronization selection process of an option II network corresponding to second generation quality levels.

QL-PRS: PRS traceable ([ITU-T G.811]).

QL-STU: Synchronized – Traceability unknown.

QL-ST2: Traceable to stratum 2 ([ITU-T G.812], type II).

QL-TNC: Traceable to transit node clock ([ITU-T G.812], type V).

QL-ST3E: Traceable to stratum 3E ([ITU-T G.812], type III).

QL-ST3: Traceable to stratum 3 ([ITU-T G.812], type IV).

QL-SMC: Traceable to SONET clock self timed ([ITU-T G.813] or [ITU-T G.8262], option II).

QL-ST4: Traceable to stratum 4 freerun (only applicable to 1.5 Mbit/s signals).

QL-PROV: Provisionable by the network operator.

QL-DUS: This signal should not be used for synchronization.

First generation quality levels do not define QL-ST3E and QL-TNC as separate quality levels and QL-PROV was identified as QL-RES.

5.4.1.3 Option III synchronization networking

The following clock-source quality-levels are defined in the synchronization process of an option III SDH network corresponding to 2 levels of synchronization quality.

QL-UNK: This synchronization trail transports a timing quality generated by an unknown clock source. It is at least of quality SSU.

QL-SEC: This synchronization trail transports a timing quality generated by a synchronous equipment clock (SEC) that is defined in [ITU-T G.813] or [ITU-T G.8262], option I.

NOTE – The use of other quality levels is for further study.

5.4.1.4 Squelching

The first purpose of the "squelch" function is to prevent transmission of a timing signal with a quality that is lower than the quality of the clock in the receiving network element or SASE. It is also used for the prevention of timing loops (see clause 5.13).

5.4.2 Hierarchy of clock-source quality-levels (QL) or (CS_QL)

The following tables define the QL hierarchy.

5.4.2.1 Option I synchronization networking

Table 1 – Hierarchy of quality levels in option I synchronization networks

Quality level	Order
QL-PRC	Highest
QL-SSU-A	|
QL-SSU-B	|
QL-SEC	|
QL-DNU	|
QL-INVx, QL-FAILED, QL-UNC, QL-NSUPP	Lowest

The quality levels QL-INVx, QL-FAILED, QL-UNC and QL-NSUPP are internal QLs inside the NE and are never generated at an output port.

QL-INVx is generated by the XX/SD_A_Sk function if an unallocated SSM value is received, where x represents the binary value of this SSM.

QL-NSUPP is generated by the XX/SD_A_Sk function when the function is not supporting the SSM (TM) processing.

QL-FAILED is generated by the SD_TT_Sk function when the terminated SD trail is in the signal fail state.

QL-UNC is generated by the SD_C or NS_C function when the output signal is not connected to an input, but instead to the internal unconnected signal generator.

5.4.2.2 Option II synchronization networking

Table 2 – Hierarchy of quality levels in option II synchronization networks

Quality level	Order
QL-PRS	Highest
QL-STU	|
QL-ST2	|
QL-TNC (Note)	|
QL-ST3E (Note)	|
QL-ST3	|
QL-SMC	|
QL-ST4	|
QL-PROV (default position)	|
QL-DUS	|
QL-INVx, QL-FAILED, QL-UNC, QL-NSUPP	Lowest
NOTE – QL-TNC and QL-ST3E are not defined for first generation synchronization networking (refer to clause 5.4.1.2) and QL-PROV was identified as QL-RES.	

The quality levels QL-INVx, QL-FAILED, QL-UNC and QL-NSUPP are internal QLs inside the NE and are never generated at an output port.

QL-INVx is generated by the XX/SD_A_Sk function if an unallocated SSM value is received, where x represents the binary value of this SSM.

QL-NSUPP is generated by the XX/SD_A_Sk function when the function is not supporting the SSM (TM) processing.

QL-FAILED is generated by the SD_TT_Sk function when the terminated SD trail is in the signal fail state.

QL-UNC is generated by the SD_C or NS_C function when the output signal is not connected to an input, but instead to the internal unconnected signal generator.

The quality level QL-PROV is provisionable by the network operator and may take different order positions. The default position for QL-PROV is as shown in Table 2.

5.4.2.3 Option III synchronization networking

Table 3 – Hierarchy of quality levels in option III synchronization networks

Quality level	Order
QL-UNK	Highest
QL-SEC	|
QL-INVx, QL-FAILED, QL-UNC, QL-NSUPP	Lowest

The quality levels QL-INVx, QL-FAILED, QL-UNC and QL-NSUPP are internal QLs inside the NE and are never generated at an output port.

QL-INVx is generated by the XX/SD_A_Sk function if an unallocated SSM value is received, where x represents the binary value of this SSM.

QL-NSUPP is generated by the XX/SD_A_Sk function when the function is not supporting the SSM (TM) processing.

QL-FAILED is generated by the SD_TT_Sk function when the terminated SD trail is in the signal fail state.

QL-UNC is generated by the SD_C or NS_C function when the output signal is not connected to an input, but instead to the internal unconnected signal generator.

5.4.3 Forcing and defaulting of clock-source quality-levels

For synchronization source signals/interfaces not supporting SSM transport/processing, it is possible in option I networks to force the quality level to a fixed provisioned value. This allows using these signals/interfaces as synchronization sources in an automatic reference selection process operating in QL-enabled mode.

Forcing of quality levels is used for new equipment operating in QL-enabled mode in order to:

– interwork with old equipment not supporting SSM/TM generation;

– interwork with new equipment operating in QL-disabled mode;

– select interfaces not supporting SSM/TM processing;

– select signals for which SSM/TM is not defined (e.g., 2 MHz).

In option II and III networks, synchronization input ports assume a default QL-STU/QL-UNK for synchronization source signals not supporting SSM.

5.4.3.1 Option I synchronization networking

The quality level of the input signal (STM-N, 2 Mbit/s, 2 MHz, 34 Mbit/s, 140 Mbit/s) can be forced to either QL-PRC, QL-SSU-A, QL-SSU-B or QL-SEC.

5.4.3.2 Option II synchronization networking

QL-STU is the default quality level for signals from equipment not supporting or not enabled for SSM in option II.

NOTE – 1544 kbit/s signals transport the SSM as a specific message within the data link (see [ITU-T G.704]). When a timing input port does not receive any SSM message, it defaults to QL-STU.

5.4.3.3 Option III synchronization networking

QL-UNK is the default quality level for 64 kHz station clock input signals.

5.4.4 Application of quality level "Unknown"

5.4.4.1 Option I synchronization networking

Option I synchronization networks do not support the unknown quality level. Instead, the network operator is required to force the quality level to one of the four quality levels: PRC, SSU-A, SSU-B or SEC. Engineering rules for this selection are for further study.

NOTE 1 – Equipment built according to the initial STM-N signal specification in which the S1 byte was still a Z1 byte with no defined value, may output any of the 16 codes within what is now bits 5 to 8 of byte S1.

NOTE 2 – Engineering rules for the forcing of quality levels in option I networks could be the following: if the reference signal is sourced by an SASE or NE with SSU-A clock, the forced QL should be QL-SSU-A; if the reference signal is sourced by an NE with SSU-B clock, the forced QL should be QL-SSU-B; if the reference signal is sourced by an NE with a SEC clock, the forced QL should be QL-SEC.

5.4.4.2 Option II synchronization networking

Quality level "unknown" (QL-STU) is intended to be used in option II applications where SSM functionality is not supported by all synchronization equipment. Without SSM capabilities, it is impossible for synchronization equipment to communicate its quality level. Consequently, the

QL-STU message is used in applications where equipment with SSM functionality is timed from a reference without an SSM. The QL-STU message indicates that the equipment is locked to a reference (i.e., it is not in holdover) but the quality of the source is not known.

Typically, this QL-STU quality level is assumed to apply to signals at an NE's station clock input port (connected to a BITS). 1.5 Mbit/s signals into the clock input ports default to STU if SSMs are not supported by the BITS. STM-N signals into the NE contain SSM code "0000" and are interpreted as QL-STU if SSMs are not supported by the STM-N output port in the previous NE.

When the input signal with forced QL-STU is selected as the synchronization reference, the output signals supporting SSM will indicate QL-STU in their SSM bits. Network elements supporting SSM processing will accept incoming QL-STU indications as one of the normal quality level indications.

The clock-source quality-level of a signal with QL-STU indication is assumed to be equal or less than PRS and better than or equal to ST2 (clause 5.4.2).

5.4.4.3 Option III synchronization networking

In the case of option III applications, an NE's clock is usually locked to PRC or SSU clock. Consequently, the quality level of the NE's clock signal is usually better than SSU. However, if there is an SEC, which has the possibility to become free-running and holdover state in a synchronization network connection, it is necessary to ensure the clock quality.

Quality level "unknown" (QL-UNK) message indicates that the equipment is locked to a reference (i.e., it is not in holdover) but the quality of the source is not known. Typically, this QL-UNK quality level is assumed to apply to 64 kHz signals at an NE's station clock input port (connected to an SASE). The quality of the source will then be at least SSU.

When the input signal with QL-UNK is selected as synchronization reference, the output signals supporting SSM will indicate QL-UNK in their SSM bits. Network elements supporting SSM processing will accept incoming QL-UNK indications as one of the normal quality level indications. The clock-source-quality level of a signal with QL-UNK indication is assumed to be equal or less than PRC and better than or equal to SSU.

If the clock-source quality-level is lower than QL-UNK at the clock input port of the NE in the upper synchronization layer, quality level "synchronous equipment clock" (QL-SEC) shall be transmitted from an NE in the upper synchronization layer to an NE in the lower synchronization layer. When the NE in the lower synchronization layer receives the QL-SEC, the NE in the lower synchronization layer squelches the output to the SSU to avoid the clock quality level degradation in other lower synchronization layers. The clock-source quality-level of a signal with QL-SEC indication means that its quality level is lower than SSU.

NOTE – Engineering rules for the forcing of quality levels in option III networks are for further study.

5.4.5 Application of quality level "provisioned"

The quality level QL-PROV defined for option II networks is provisionable to a QL order chosen by the operator.

5.5 Synchronization status messages (SSMs) and timing marker (TM) channels

The following signals have a four-bit SSM channel defined:

– STM-N (N = 1, 4, 16): bits 5 to 8 of the byte S1 (called SSMB, synchronization status message byte) of the multiplex section overhead as defined in [ITU-T G.707].

– 2 Mbit/s octet structured according to [ITU-T G.704]: bits S_{ax1} to S_{ax4} (x = 4, 5, 6, 7 or 8) of TS0.

– 1.5 Mbit/s octet structured according to clause 2.1 of [ITU-T G.704].

– 34 Mbit/s as defined in [b-ITU-T G.832]: bit 8 of MA byte with a 4-frame multiframe.

– 140 Mbit/s as defined in [b-ITU-T G.832]: bit 8 of MA byte with a 4-frame multiframe.

– 100 Mbit/s, 1 Gbit/s, 10 Gbit/s as defined in [b-IEEE 802.3]: 4-bit SSM field in the SSM PDU as defined in [ITU-T G.8264].

The following signals may have a one bit TM channel:

– 34 Mbit/s with a 125 µs frame structure as defined in [b-ITU-T G.832]: bit 8 of byte MA.

– 140 Mbit/s with a 125 µs frame structure as defined in [b-ITU-T G.832]: bit 8 of byte MA.

5.5.1 SSM and TM message sets

5.5.1.1 Option I synchronization networking

Five SSM codes are defined to represent clock source QL as listed below:

– code 0010 (quality PRC) means that the source of the trail is a PRC clock ([ITU-T G.811]);

– code 0100 (quality SSU-A), means that the source of the trail is a type I or V SSU clock [ITU-T G.812];

– code 1000 (quality SSU-B), means that the source of the trail is a type VI SSU clock ([ITU-T G.812]);

– code 1011 (quality SEC), means that the source of the trail is an SEC clock ([ITU-T G.813] or [ITU-T G.8262], option I);

– code 1111 (quality DNU), means that the signal carrying this SSM shall not be used for synchronization because a timing loop situation could result if it is used.

Two TM codes are defined in [b-ITU-T G.832]:

– code 0 (quality PRC), means that the source of the trail is a PRC clock ([ITU-T G.811]);

– code 1 (quality less_than_PRC), means that the source of the trail is not a PRC clock.

5.5.1.2 Option II synchronization networking

Nine SSM codes are defined to represent clock source QL as listed below on STM-N signals:

– code 0001 (quality PRS) means that the source of the trail is a PRS clock ([ITU-T G.811]);

– code 0000 (quality STU) means that the signal does not carry the QL message of the source of the trail;

– code 0111 (quality ST2), means that the source of the trail is a stratum 2 clock ([ITU-T G.812], type II);

– code 0100 (quality TNC), means that the source of the trail is a transit node clock ([ITU-T G.812], type V);

– code 1101 (quality ST3E), means that the source of the trail is a stratum 3E clock ([ITU-T G.812], type III);

– code 1010 (quality ST3), means that the source of the trail is a stratum 3 clock ([ITU-T G.812], type IV);

– code 1100 (quality SMC), means that the source of the trail is a SONET/Ethernet self-timed clock ([ITU-T G.813] or [ITU-T G.8262], option II);

– code 1110 (quality PROV), is provisionable by the network operator;

– code 1111 (quality DUS), means that the signal carrying this SSM shall not be used for synchronization because a timing loop situation could result if it is used.

NOTE 1 – Code 1101 and code 0100 are not recognized by equipment supporting only first generation SSM and are treated as invalid (see clause 5.4.1.2), code 1110 is identified as QL-RES.

Ten SSM codes are defined to represent clock source QL as listed below on 1544 kbit/s signals:

– code $04FF_H$ (quality PRS) means that the source of the trail is a PRS clock ([ITU-T G.811]);

– code $08FF_H$ (quality unknown) means that the source of the trail is unknown;

– code $0CFF_H$ (quality ST2) means that the source of the trail is a stratum 2 clock ([ITU-T G.812], type II);

– code $78FF_H$ (quality TNC) means that the source of the trail is a transit node clock ([ITU-T G.812], type V);

– code $7CFF_H$ (quality ST3E) means that the source of the trail is a stratum 3E clock ([ITU-T G.812, type III);

– code $10FF_H$ (quality ST3) means that the source of the trail is a stratum 3 clock ([ITU-T G.812, type IV);

– code $22FF_H$ (quality SMC) means that the source of the trail is a SONET/Ethernet self-timed clock ([ITU-T G.813] or [ITU-T G.8262], option II);

– code $28FF_H$ (quality ST4) means that the source of the trail is a stratum 4 clock;

– code $40FF_H$ (quality PROV) is provisionable by the network operator;

– code $30FF_H$ (quality DUS) means that the signal carrying this SSM shall not be used for synchronization because a timing loop situation could result if it is used.

NOTE 2 – Code $78FF_H$ and code $7CFF_H$ are not recognized by equipment supporting only second generation SSM and are treated as invalid (refer to clause 5.4.1.2), code $40FF_H$ is identified as QL-RES.

5.5.1.3 Option III synchronization networking

Two SSM codes are defined to represent clock source QL as listed below:

– code 0000 (quality unknown) means that the source of the trail is unknown;

– code 1011 (quality SEC) means that the source of the trail is an SEC clock ([ITU-T G.813] or [ITU-T G.8262], option I).

5.5.2 SSM and TM code word generation

The SSM can be viewed as an application-specific data communication channel with a limited message set. The message that shall be generated and inserted depends on the applied quality level indication that is input to the adaptation source function. The following tables present the relation between the existing set of QLs and SSM codes for the three options.

It is possible to disable the SSM generation and insert "1111". An application for this could be, e.g., at network boundaries where timing information should not be forwarded to the other network.

5.5.2.1 Option I synchronization networking

Table 4 – Quality level set and coding in synchronization status message in option I synchronization networks

Quality level (QL)	SSM usage	SSM coding [MSB..LSB]
QL-PRC	Enabled	0010
QL-SSU-A	Enabled	0100
QL-SSU-B	Enabled	1000
QL-SEC	Enabled	1011
QL-DNU	Enabled	1111
–	Disabled	1111

The TM can be viewed as an application-specific data communication channel with a limited message set. The message that shall be generated and inserted depends on the applied quality level indication that is input to the adaptation source function. The following table presents the relation between the existing set of QLs and TM codes.

Table 5 – Quality level set and coding in timing marker in option I synchronization networks

Quality Level (QL)	TM usage	TM coding
QL-PRC	Enabled	0
QL-SSU-A	Enabled	1
QL-SSU-B	Enabled	1
QL-SEC	Enabled	1
QL-DNU	Enabled	1
–	Disabled	1

At network boundaries, it should be possible to prevent synchronization information passing the interface. This can be achieved by disabling the SSM (TM) usage.

5.5.2.2 Option II synchronization networking

In order to provide stable interoperability between equipment supporting first generation and equipment supporting second generation quality levels, Table 6 defines the SSM coding for both "second generation output connected to a second generation input", and for "second generation output connected to first generation input".

This translation table is for newer equipment supporting second generation quality level definitions only. Message translation is provided on a per port basis as a provisionable option. This allows for equipment supporting second generation messaging to simultaneously pass valid SSMs to both second generation and first generation equipment.

The shaded fields in Table 6 identify the quality levels that require translation in order to be understood by first generation equipment: QL-TNC and QL-ST3E are translated into QL-ST3 messages, QL-PROV SSM code is interpreted as QL-RES by first generation equipment.

Table 6 – Quality level set and coding in synchronization status message in option II synchronization networks

Quality level (QL)	SSM usage	Second generation SSM		First generation SSM	
		SSM coding [MSB..LSB] in STM-N signal (BINARY)	SSM coding [MSB..LSB] in 1544 kbit/s signal with ESF (HEX)	SSM coding [MSB..LSB] in STM-N signal (BINARY)	SSM coding [MSB..LSB] in 1544 kbit/s signal with ESF (HEX)
QL-PRS	Enabled	0001	04FF	0001	04FF
QL-STU	Enabled	0000	08FF	0000	08FF
QL-ST2	Enabled	0111	0CFF	0111	0CFF
QL-TNC	Enabled	0100	78FF	1010[c)]	10FF[c)]
QL-ST3E	Enabled	1101	7CFF	1010[c)]	10FF[c)]

Table 6 – Quality level set and coding in synchronization status message in option II synchronization networks

Quality level (QL)	SSM usage	Second generation SSM		First generation SSM	
		SSM coding [MSB..LSB] in STM-N signal (BINARY)	SSM coding [MSB..LSB] in 1544 kbit/s signal with ESF (HEX)	SSM coding [MSB..LSB] in STM-N signal (BINARY)	SSM coding [MSB..LSB] in 1544 kbit/s signal with ESF (HEX)
QL-ST3	Enabled	1010	10FF	1010	10FF
QL-SMC	Enabled	1100	22FF	1100	22FF
QL-ST4	Enabled	–	28FF	–	28FF
QL-PROV	Enabled	1110	40FF	1110[a), b), c)]	40FF[a), b), c)]
QL-DUS	Enabled	1111	30FF	1111	30FF
–	Disabled	1111	08FF	1111	08FF

a) The assignment of the GEN1 message "reserved for network synchronization use (QL-RES)" needs to be done on a network-wide basis.

b) In a given network, the GEN1 message "reserved for network synchronization use (QL-RES)" can only reflect a single GEN2 message assignment.

c) The translation of the TNC or stratum 3E message to the reserved for network synchronization use (RES) message, is a user-definable option. In this case, the quality level of the RES message is between 3 and 4. In this way, GEN1 equipment that supports a TNC or stratum 3E quality clock can always receive traceable timing of an equal or better quality level which would then maintain the hierarchical distribution of timing. Because of the nature of the RES message, all NEs in the network need to be provisioned to recognize the RES message as TNC or stratum 3E. The RES message may only reflect one unique message on a network-wide basis.

At network boundaries, it shall be possible to prevent synchronization information passing the interface. This can be achieved by disabling the SSM usage, or by provisioning output signals to have QL-STU or QL-DUS.

The application of the QL-PROV message is at the discretion of the network operator.

5.5.2.3 Option III synchronization networking

Table 7 – Quality level set and coding in synchronization status message in option III synchronization networks

Quality level (QL)	SSM coding [MSB..LSB]
QL-UNK	0000
QL-SEC	1011

5.5.3 SSM and TM code word interpretation

At the receive side, the received SSM bits are to be validated by a persistency check and then interpreted to determine the QL.

5.5.3.1 Option I synchronization networking

Table 8 – Interpretation of synchronization status message codes in option I synchronization networks

SSM code [MSB..LSB]	QL interpretation
0000	QL-INV0
0001	QL-INV1
0010	QL-PRC
0011	QL-INV3
0100	QL-SSU-A
0101	QL-INV5
0110	QL-INV6
0111	QL-INV7
1000	QL-SSU-B
1001	QL-INV9
1010	QL-INV10
1011	QL-SEC
1100	QL-INV12
1101	QL-INV13
1110	QL-INV14
1111	QL-DNU

Table 9 – Interpretation of timing marker codes

TM code	QL interpretation
0	QL-PRC
1	QL-DNU

5.5.3.2 Option II synchronization networking

Table 10 – Interpretation of synchronization status message codes in STM-N signals in option II synchronization networks

SSM code [MSB..LSB] in STM-N signals	QL interpretation
0000	QL-STU
0001	QL-PRS
0010	QL-INV2
0011	QL-INV3
0100	QL-TNC
0101	QL-INV5
0110	QL-INV6
0111	QL-ST2

Table 10 – Interpretation of synchronization status message codes in STM-N signals in option II synchronization networks

SSM code [MSB..LSB] in STM-N signals	QL interpretation
1000	QL-INV8
1001	QL-INV9
1010	QL-ST3
1011	QL-INV11
1100	QL-SMC
1101	QL-ST3E
1110	QL-PROV
1111	QL-DUS
NOTE – First generation quality level equipment will not receive SSM codes 0100 (QL-TNC) or 1101 (QL-ST3E); output ports of second generation quality level equipment will be provisioned in this case to output 1010 (QL-ST3) instead [or 1110 (QL-PROV)]. Refer to clause 5.5.2.2.	

Table 11 – Interpretation of synchronization status message codes in 1544 kbit/s signals in option II synchronization networks

SSM code in 1544 kbit/s signals		QL interpretation
0xxx xxx0 1111 1111	HEX	
000 010	04FF	QL-PRS
000 100	08FF	QL-STU
000 110	0CFF	QL-ST2
111 100	78FF	QL-TNC
111 110	7CFF	QL-ST3E
001 000	10FF	QL-ST3
010 001	22FF	QL-SMC
010 100	28FF	QL-ST4
011 000	30FF	QL-DUS
100 000	40FF	QL-PROV
Other (see Note 1)	Other (see Note 1)	QL-INV
NOTE 1 – Other codes, not related to synchronization, are defined in Table 2 of [ITU-T G.704]. NOTE 2 – [ITU-T G.704] presents the data link messages in reverse order "1111 1111 0xxx xxx0". NOTE 3 – First generation quality level equipment will not receive SSM codes 111 100 (QL-TNC) or 111 110 (QL-ST3E); output ports of second generation quality level equipment will be provisioned in this case to output 001 000 (QL-ST3) instead [or 100 000 (QL-RES)]. Refer to clause 5.5.2.2.		

5.5.3.3 Option III synchronization networking

Table 12 – Interpretation of synchronization status message codes in option III synchronization networks

SSM code [MSB..LSB]	QL interpretation
0000	QL-UNK
0001	QL-INV1
0010	QL-INV2
0011	QL-INV3
0100	QL-INV4
0101	QL-INV5
0110	QL-INV6
0111	QL-INV7
1000	QL-INV8
1001	QL-INV9
1010	QL-INV10
1011	QL-SEC
1100	QL-INV12
1101	QL-INV13
1110	QL-INV14
1111	QL-INV15

5.6 Selection process

The process of selecting a synchronization source from the set of physical ports is performed in three steps, plus one for use of the station clock output:

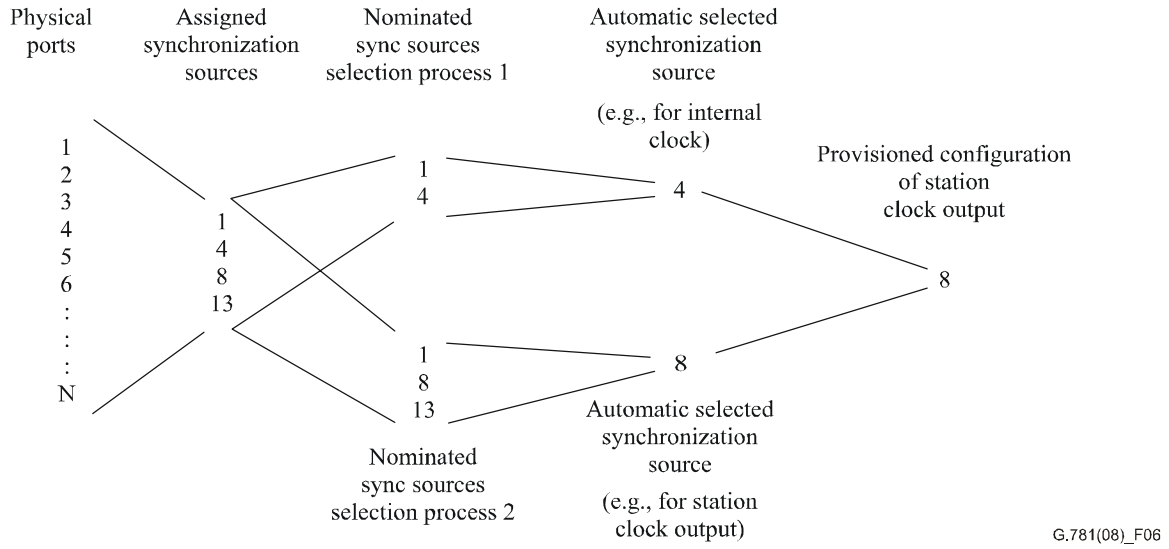


Figure 6 – Visualization of the synchronization source selection process(es)

1) *Assignment of a physical port to be a synchronization source*: Select a (limited) set of interface signals (from the total set of interfaces) to act as synchronization sources.

This is performed in the SD_C function by means of adding matrix connections between a group of inputs (connected to the server layer) and outputs (connected to the SD_TT_Sk functions).

2) *Nomination of a synchronization source for an automatic selection process*: Select a (sub)set of the synchronization sources to contribute to a selection process.

   This is performed in the NS_C function by means of assigning a priority to the synchronization source (see clause 5.10).

3) *Automatic selection process*: Selects the "best" synchronization source of the set from nominated sources according to the selection algorithm (see clause 5.12).

   The next step is required only for use of the station clock output:

4) *Configuration of the station clock output selector*: The selector is normally configured to allow the selected line synchronization source to be outputted to the SSU via the station clock output. An operator command allows the selection of the internal clock to be outputted, if required. This selection is only dependant on the operator command and not on the status of the selected signal.

NOTE – The specifications in this Recommendation allow a selection to be made between any set of synchronization interface signals input to a network element, independent of the actual synchronization network architecture deployed in the network. It is the network operator's responsibility to ensure that timing loops are not created.

5.7 Signal fail

Signal fail for a synchronization source is activated in case of defects detected in the server layers. In addition, an unconnected synchronization signal has also signal fail active in order to allow correct processing in the QL-disabled mode. Inclusion of specific synchronization failures (e.g., exceeded frequency deviation, exceeded wander limits), as signal fail criteria for SSU, are for further study.

In order to avoid reactions on short pulses or intermittent signal fail information, the signal fail information is passed through hold-off and wait to restore processes before it is considered by the selection process.

NOTE 1 – The delay of the signal fail information is only performed for the information passed to the selection process. The signal fail information for the main data path to the output of the NS_C function is not delayed.

In QL-enabled mode, the QL of a synchronization source with active signal fail is set to QL-FAILED. The selection process will react to this QL value instead of the signal fail signal in this mode.

NOTE 2 – Due to different persistence times for defect detection and the SSM acceptance process, a defect leading to signal fail could also result in a change of the QL value shortly before signal fail is activated. The implementation has to ensure that the selection process does not select a new synchronization source based on this intermediate QL value.

5.8 Hold-off time

The hold-off time ensures that short activation of signal fail are not passed to the selection process.

In QL-disabled mode, signal fail shall be active for the hold-off time before it is passed to the selection process.

In QL-enabled mode, a QL value of QL-FAILED shall exist for the hold-off time before it is passed to the selection process. In the meantime, the previous QL value is passed to the selection process.

NOTE – Other QL values than QL-FAILED will be passed to the selection process immediately.

Separate hold-off timers are used for each input to a selection process (nominated source).

The hold-off time is fixed in the range of 300 ms to 1800 ms.

5.9 Wait to restore time

The wait to restore time ensures that a previous failed synchronization source is only again considered as available by the selection process if it is fault-free for a certain time.

In QL-disabled mode, after deactivation of signal fail, it shall be false for the wait to restore time before signal fail false is passed to the selection process. In the meantime, signal fail true is passed to the selection process.

In QL-enabled mode, after a change of the quality level from QL-FAILED to any other value, the quality value shall be different from QL-FAILED for the wait to restore time before the new QL value is passed to the selection process. In the meantime, the quality level QL-FAILED is passed to the selection process.

Separate wait to restore timers are used for each input to a selection process (nominated source).

The wait to restore time is configurable in the range of 0 to 12 minutes in steps of 1 minute for all inputs of a selection process in common. The default value is 5 minutes.

Each wait to restore timer can be cleared with a separate clear command. If a wait to restore timer is cleared, the new QL value (in QL-enabled mode), or signal fail value (in QL-disabled mode), is immediately passed to the selection process.

5.10 Synchronization source priorities

In order to define a preferred network synchronization flow, priority values are allocated to assigned synchronization sources within a network element (see Table 13).

Different priorities reflect a preference of one synchronization source over the other. Equal synchronization source priorities reflect that no preference exists between the synchronization sources. Within the group of synchronization sources with equal priorities, the selection process has a non-revertive behaviour.

A priority of "dis" (disabled) identifies that this assigned synchronization source is not nominated for the selection process.

Table 13 – Priority order

Priority value	Order
1	Highest
2	|
3	|
:	|
K	|
dis, undef	Lowest
NOTE – The priority value is not numerically ordered. The following relation is present: "1" > "2" > "3" > .. >"K" > "undef", "dis".	

The priority value "undef" is associated with the unconnected signal of the NS_C function and is not configurable from the outside.

NOTE – The assigning of equal priorities to synchronization sources, in order to allow for non-revertive operation, does not allow for a pre-defined initialization state of known synchronization configuration following failure of a higher priority source.

5.11 External commands

Several external commands are available to the user (e.g., for maintenance purposes). These commands are independent and have different impacts on the selection processes.

5.11.1 External commands per nominated synchronization source

It is possible to temporarily remove a timing source as available synchronization source for the selection process.

This is controlled by the lockout commands. Lockout commands are accepted for nominated synchronization sources (synchronization sources that are not disabled) of each selection process.

The lockout status of a disabled synchronization source is "off".

NOTE – A locked out source is still nominated to the selection process and retains its synchronization source priority.

5.11.1.1 Set_Lockout#p command

The Set_Lockout#p command sets the lockout state of input p to "on". This causes this input to be no longer considered available by the selection process.

5.11.1.2 Clear_Lockout#p command

The Clear_Lockout#p command sets the lockout state of input p to "off". This causes this input to be considered available again by the selection process.

5.11.2 External commands per selection process

The activation and deactivation of external commands associated with the synchronization selection process are defined below. Furthermore, only one of these external commands is active at a time, per the selection process.

5.11.2.1 Clear command

A clear (CLR) command clears the forced switch and manual switch commands.

5.11.2.2 Forced switch #p command

A forced switch (FSw) to #p command can be used to override the currently selected synchronization source, assuming the synchronization source #p is enabled and not locked out.

The forced switch overrides the manual switch, and a subsequent forced switch pre-empts the previous forced switch.

If the source selected by the forced switch command (#p) is disabled or locked out, the forced switch command is automatically rejected.

The forced switch command can be cleared by the "clear" command.

NOTE – A forced switch command to a synchronization source #p that is in the SF state or has a QL of DNU in QL enabled mode will result in the network element entering holdover.

5.11.2.3 Manual switch #p command

A manual switch (MSw) to #p command selects the synchronization source #p, assuming it is enabled, not locked out, not in signal fail condition, and has a QL better than DNU in QL-enabled mode. Furthermore, in QL-enabled mode, a manual switch can be performed only to a source which has the highest available QL. As such, these conditions have the effect that manual switching can only be used to override the assigned synchronization source priorities.

A manual switch request overrides a previous manual switch request.

If the source selected by the manual switch command (#p) is disabled, locked out, in signal fail or has a QL of DNU or lower than one of the other source signals, the manual switch command is automatically rejected.

The manual switch command can be cleared by the "clear" command.

5.12 Automatic reference selection process

One or more reference selection processes operate independently to select the reference signal for the internal clock and, where present, the station clock output(s). However, the SD connection function delivering SD_CI to the station clock output atomic functions (see Figure 15) is only operated by operator command and not by an automatic process.

The selection process(es) can work in two distinct modes: QL-enabled and QL-disabled. If multiple selection processes are present in a network element, all processes work in the same mode.

The following is a brief description of the automatic reference selection process. The specific details (SDL diagrams) are defined in Annex A.

5.12.1 QL-enabled mode

In QL-enabled mode, the following parameters contribute to the selection process:

– quality level;

– signal fail via QL-FAILED;

– priority;

– external commands.

If no overriding external commands are active, the algorithm selects the reference with the highest quality level that is not experiencing a signal fail condition. If multiple inputs have the same highest quality level, the input with the highest priority is selected. For the case that multiple inputs have the same highest priority and quality level, the current existing selected reference is maintained if it belongs to this group, otherwise an arbitrary reference from this group is selected.

If no input could be selected, the function outputs the unconnected signal.

5.12.2 QL-disabled mode

In QL-disabled mode, the following parameters contribute to the selection process:

– signal fail;

– priority;

– external commands.

If no overriding external commands are active, the algorithm selects the reference with the highest priority that is not experiencing a signal fail condition. For the case that multiple inputs have the same highest priority, the current existing selected reference is maintained if it belongs to this group, otherwise an arbitrary reference from this group is selected.

If no input could be selected, the function outputs the unconnected signal.

5.13 Timing loop prevention

Synchronization network architectures should be designed such that timing loops will not occur under fault-free or failure conditions (refer to [ITU-T G.803]). Synchronization network architectures can be designed such that NE or SASE A will time NE or SASE B, and NE or SASE B will *never* time NE or SASE A. In cases where such rigorous synchronization network architecture is not viable, special timing loop prevention techniques should be used within network elements and SASEs that will open the potential loop. Some of these are described hereafter.

5.13.1 Station clock input used as a source for station clock output

This Recommendation allows the use of the station clock input as a source for the station clock output, either directly or via the SEC. When this functionality is present in a network element, the operator should be aware that this functionality is intended for timing quality monitoring purposes and that its use for other purposes could result in timing loops being created (see Figure 7). If a timing loop could be created, the operator should prevent it by a reconfiguration of the synchronization architecture.

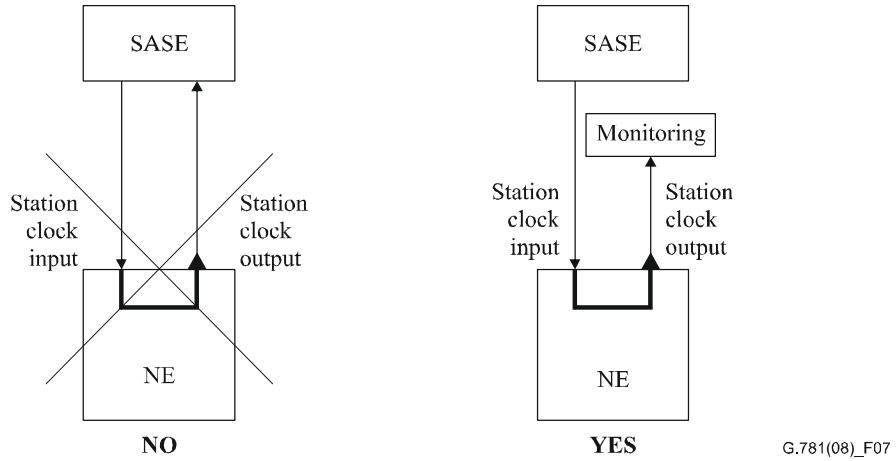


Figure 7 – Station clock output derived from station clock input

5.13.2 Between NEs with SEC type clocks

The master-slave synchronization over several NEs with multiple possible synchronization inputs for protection of synchronization, as defined in [ITU-T G.803], could lead to timing loops between NEs. To avoid timing loops, an NE should insert an SSM/TM value of DNU in the direction of the NE, which is used as the actual synchronization source for the NE clock (SEC).

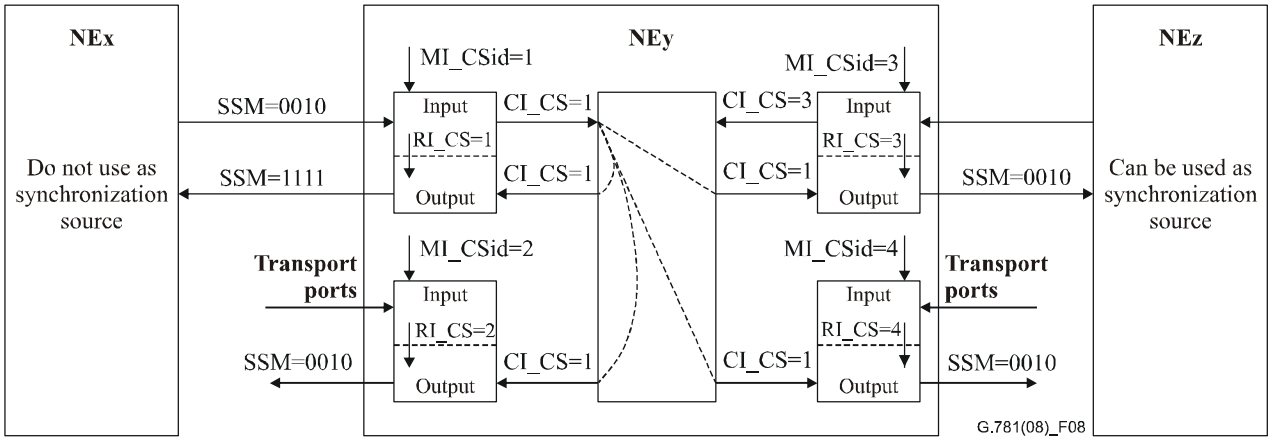


Figure 8 – Automatic DNU generation in an NE with SEC timing

The clock source identifier CSid has been introduced to support the above feature as shown on Figure 8. To each transport and station clock input port, a unique CSid is assigned (MI_CSid). This ID is processed in the synchronization layers together with the clock and quality level of the port. The CSid of the selected source for the SEC is distributed to all output ports. If a transport output port receives the same CSid as its associated input port (signalled via RI_CS) via the synchronization distribution layer (SD_CI_CS), the outgoing SSM/TM is set to DNU.

NOTE – The above principle may be extended to generate DNUs on groups, "bundles", of ports, which are known to have the same timing source. A provisional agreement is that processing of DNU generation on all the ports of the "bundle", when any one of them has been selected as the reference source, does not require additional information between the atomic functions. Use of an identical CS within the "bundle" has been considered but this is left for further study.

5.13.3 Between NEs with an SEC clock and an NE or SASE/BITS with an SSU/ST2 clock and only one link

NOTE 1 – As stated in clause 1, the application of the SSM message algorithm is not recommended in SSUs and between SECs and SSUs since this would, in a general sense, result in using SSMs over a whole operator domain. Given the current uncertainties in the specification of the SSM algorithm in synchronization networks with mixed SSU and SEC clock equipment, this cannot be recommended as a general rule. Interworking between SEC and SSU clock equipment is assumed to take place over interfaces that do not support SSM transport (see clause 5.13.3.1). An exception can be made for certain specific topologies in option II networks (see clause 5.13.3.2). The general case remains for further study.

NOTE 2 – "One link" refers to the logical connection between NE and SASE/BITS. One (logical) link may be realized by multiple physical connections (e.g., for availability reasons), each carrying the same clock information.

An NE can be interconnected with an SASE/BITS via its (64 kbit/s and 6 MHz, 2 MHz, 2 Mbit/s, 1.5 Mbit/s) station clock input and output ports. If the SASE/BITS is used as the actual synchronization source for the NE clock, the mechanism defined in clause 5.13.2 above has to be extended to support automatic DNU insertion also for this case.

It is not possible to detect that the SASE/BITS has selected the station clock output port of the NE as the actual clock source, but several conditions exist that indicate that the station clock output port is not used as the clock source by the SASE/BITS.

If an NE is connected to a SASE/BITS, remote information is exchanged between the normally unidirectional station clock input and output ports connected to the same SASE/BITS. The remote information transfers the CSid (CI_CS = RI_CS) and, in addition in case of QL enabled mode, the QL (CI_QL = RI_QL) of the clock signal selected for the station clock output to the station clock input. The user has to enable this feature by activating the remote indication connection between the station clock ports.

5.13.3.1 QL/SSM processing not supported between SASE/BITS and NE

If QL/SSM processing is not supported by the SASE/BITS, station clock ports or NE, a squelched/AIS station clock output port is the only criteria that indicates that the output port is not used as the clock source by the SASE/BITS. As long as the station clock output is not squelched (for 2 and 6 MHz station clock ports) or set to AIS (for 2 Mbit/s station clock ports), it is assumed that the SASE/BITS selects the station clock output of the NE as the reference clock. The station clock input port uses, in this case, the remote CSid (from the station clock output) as CSid for the clock signal to the selection process (RI_CS = CI_CS) instead of its own CSid (MI_CSid). This will result in DNU insertion in the traffic output port associated with the traffic input port used as source for the station clock (see Figure 9). If the station clock output is squelched or set to AIS, the remote CSid is replaced by the own CSid (MI_CSid) and the automatic DNU insertion in the traffic output port associated with the traffic input port used as source for the station clock is removed (see Figure 10).

There are still conditions in which the SASE/BITS does not select the station clock output of the NE as the synchronization source, but the automatic DNU insertion is still performed, e.g., if the SASE/BITS selects another source if the station clock output is still transmitting valid timing information (see Figure 11).

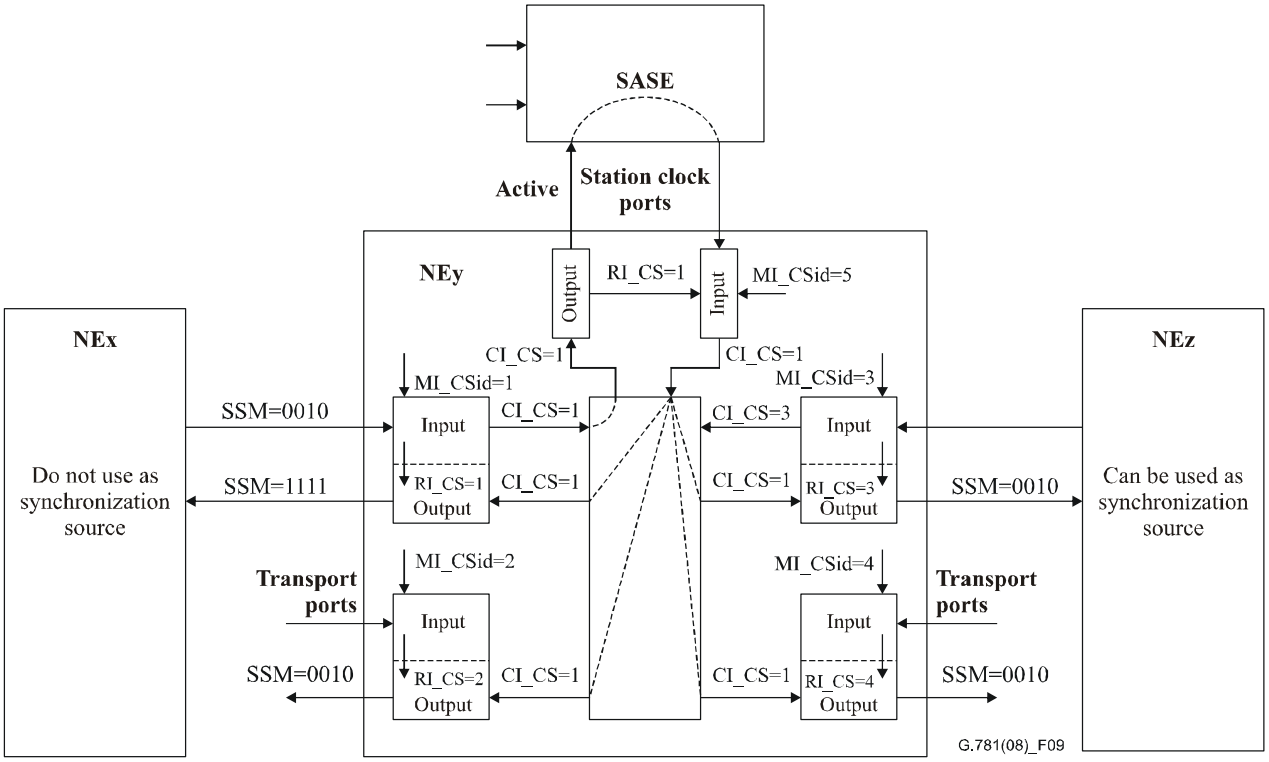


Figure 9 – Automatic DNU generation in an NE with SASE/BITS timing (SSM/QL not supported)

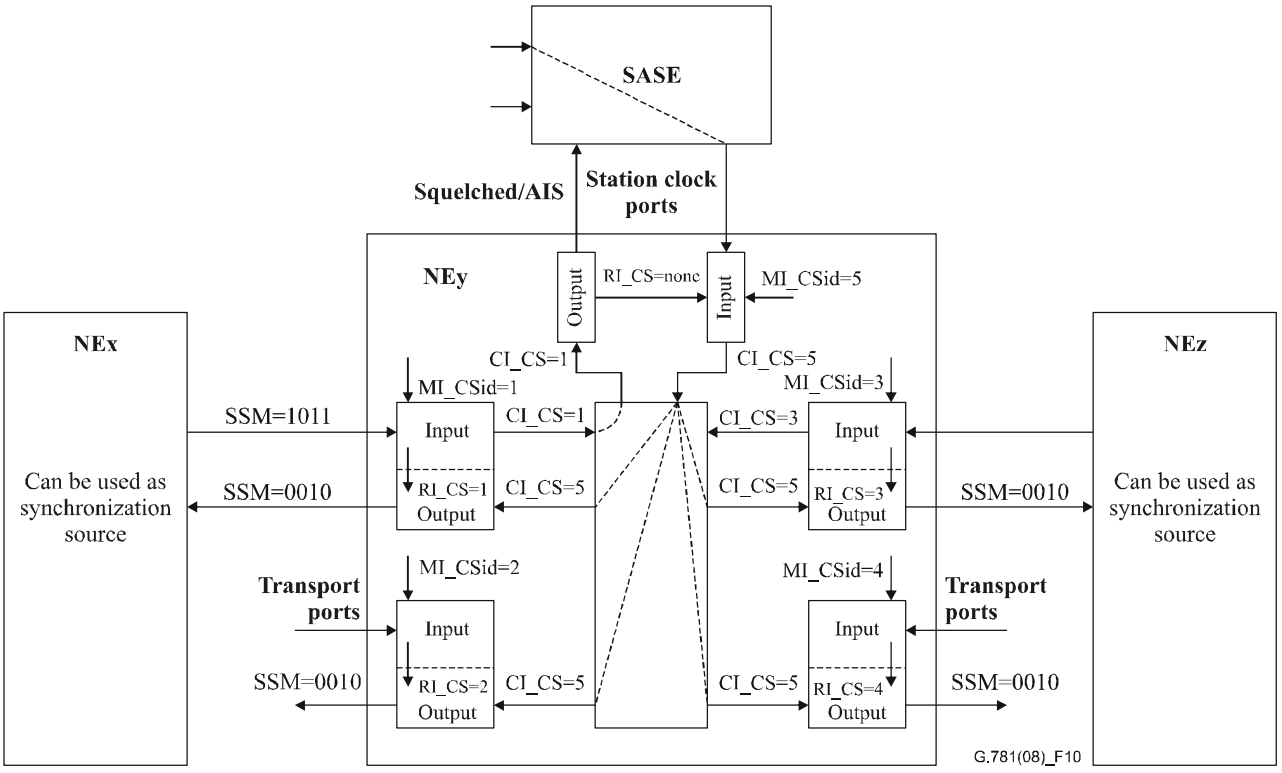


Figure 10 – Removal of automatic DNU generation in an NE with SASE/BITS timing (SSM/QL not supported)

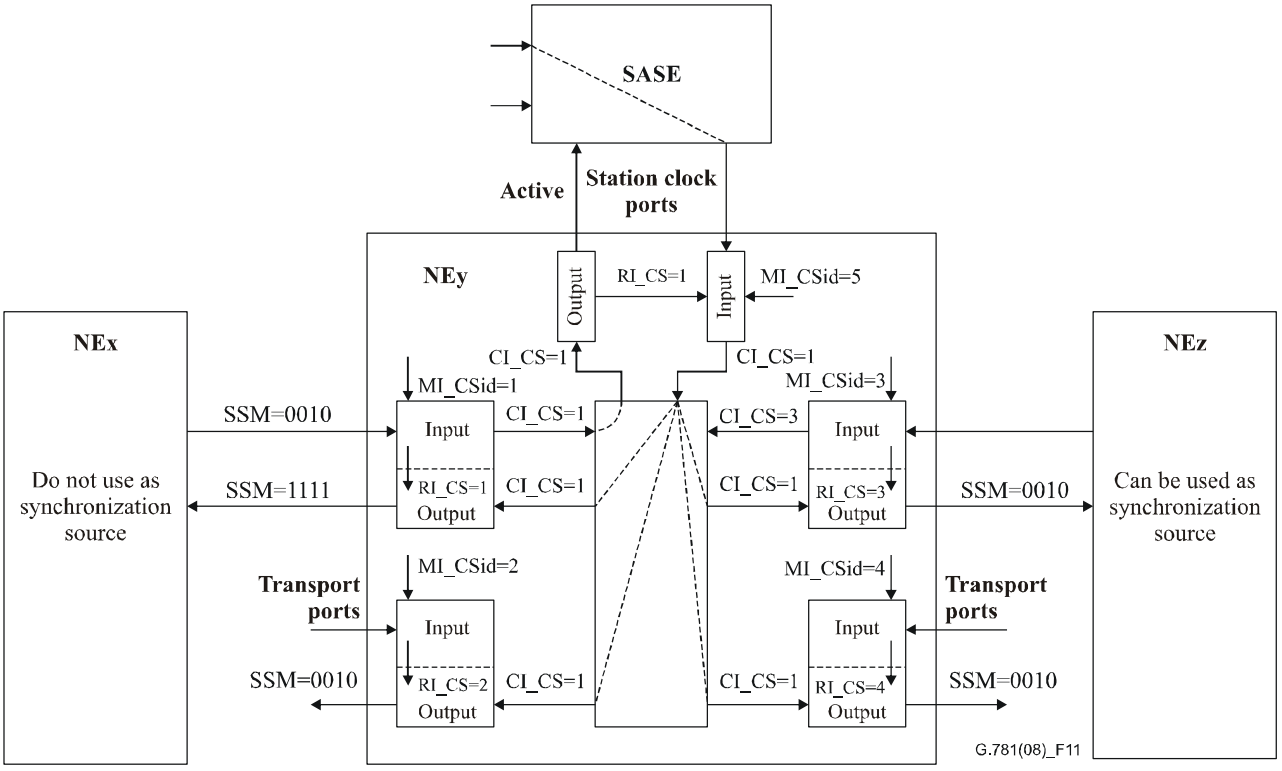


Figure 11 – Limitation of automatic DNU generation in an NE with SASE/BITS timing (SSM/QL not supported)

5.13.3.2 QL/SSM processing supported between SASE/BITS and NE (option II)

For the following specific topologies, and only within option II networks, the usage of SSMs in SSUs, and on the interface between SSUs and SECs, is recommended:

– A single ring consisting of SEC-based equipment, with collocated SSUs that filter the timing signal in some or all of the ring nodes. At present, it is recommended that SSMs should not be exchanged with the rest of the network.

  • In this application, the frequency derived from the SDH line and the SSM (i.e., the value indicated by the S1 byte) needs to be transferred from the SDH line to the SASE. In this case, the SDH NE is externally timed and must translate the SSM received from the SASE to the S1 bytes on SDH lines that are transmitted from that NE.

  • Field trials of preliminary SSM implementations have confirmed that mode switching (i.e., switching between externally timed and line timed operation) may lead to network instability and should not be used. Subsequent trials also indicate that appropriate and desirable synchronization switching is achieved using SSMs when mode switching is not used. These trials have also indicated some sensitivity to SSM processing delay times both in the NE and in the SASE.

  • Careful synchronization engineering remains mandatory to avoid potential timing loops or instabilities in the SSM algorithm.

– A linear chain consisting of SEC-based equipment with collocated SSUs that filter the timing signal in some or all of the nodes. At present, it is recommended that SSMs should not be exchanged with the rest of the network.

For option I and III networks these exceptions do not apply.

If QL/SSM processing is supported by the SASE/BITS and all other involved components (NE, station clock ports), different SSM values at the output and input station clock ports indicate

that the output port is not used as the clock source by the SASE/BITS. As long as the transmitted QL at the station clock output and the received QL at the station clock input of the NE are identical, it is assumed that the SASE/BITS selects the station clock output of the NE as the reference clock. The station clock input port uses, in this case, the remote CSid (from the station clock output) as CSid for the clock signal to the selection process (RI_CS = CI_CS) instead of its own CSid (MI_CSid). This will result in DNU insertion in the traffic output port associated with the traffic input port used as the source for the station clock (see Figure 12). If the transmitted and received QL are no longer identical, the remote CSid is replaced by the own CSid (MI_CSid) and the automatic DNU insertion in the traffic output port associated with the traffic input port used as the source for the station clock, is removed (see Figure 13). There are still conditions in which the SASE/BITS does not select the station clock output of the NE as the synchronization source, but the automatic DNU insertion is still performed, e.g., if the SASE/BITS selects another source with the same QL as the station clock output of the NE (see Figure 14).

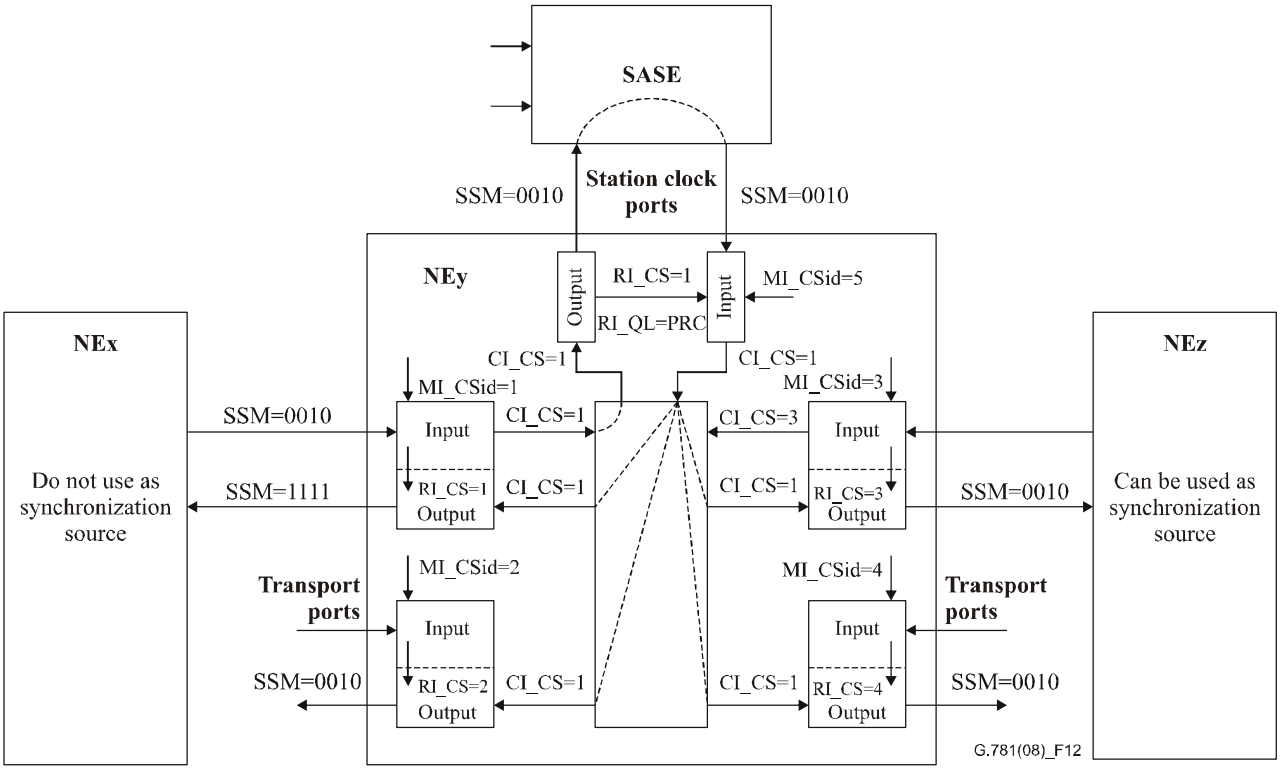


Figure 12 – Automatic DNU generation in an NE with SASE/BITS timing (SSM/QL supported)

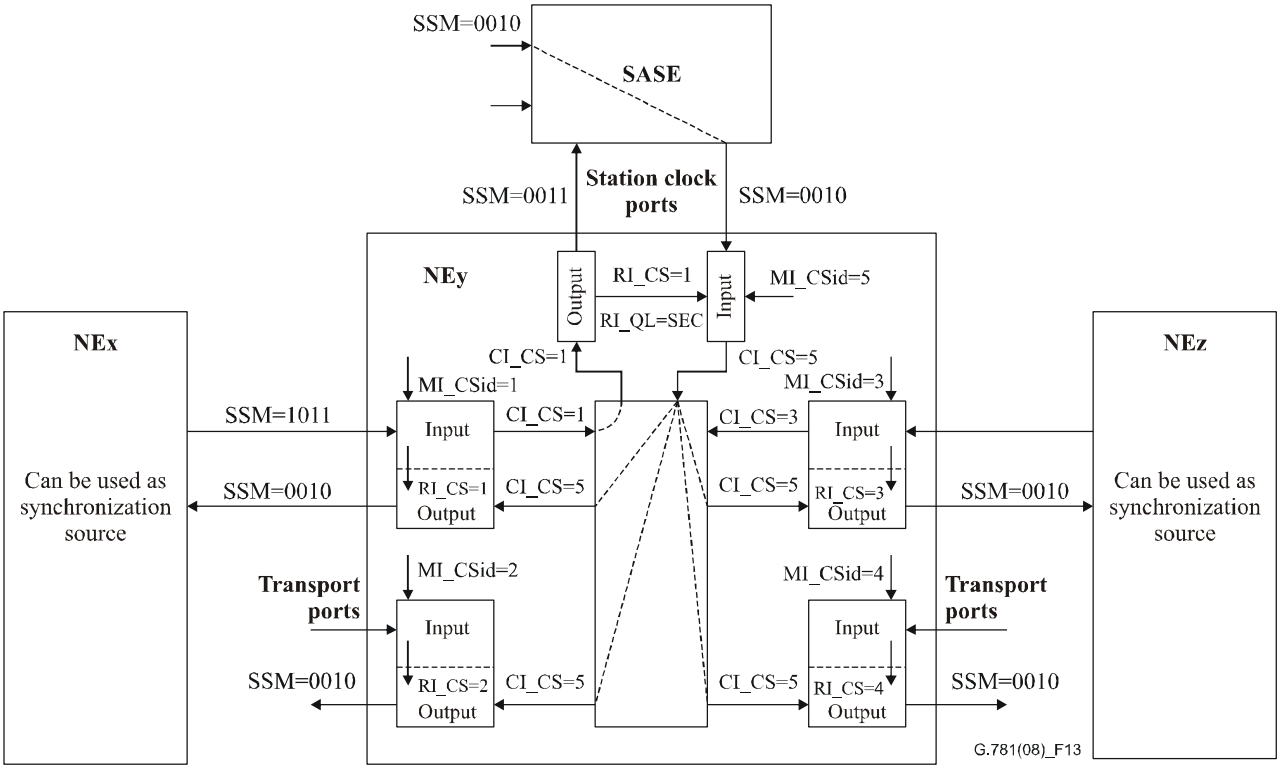


Figure 13 – Removal of automatic DNU generation in an NE with SASE/BITS timing (SSM/QL supported)

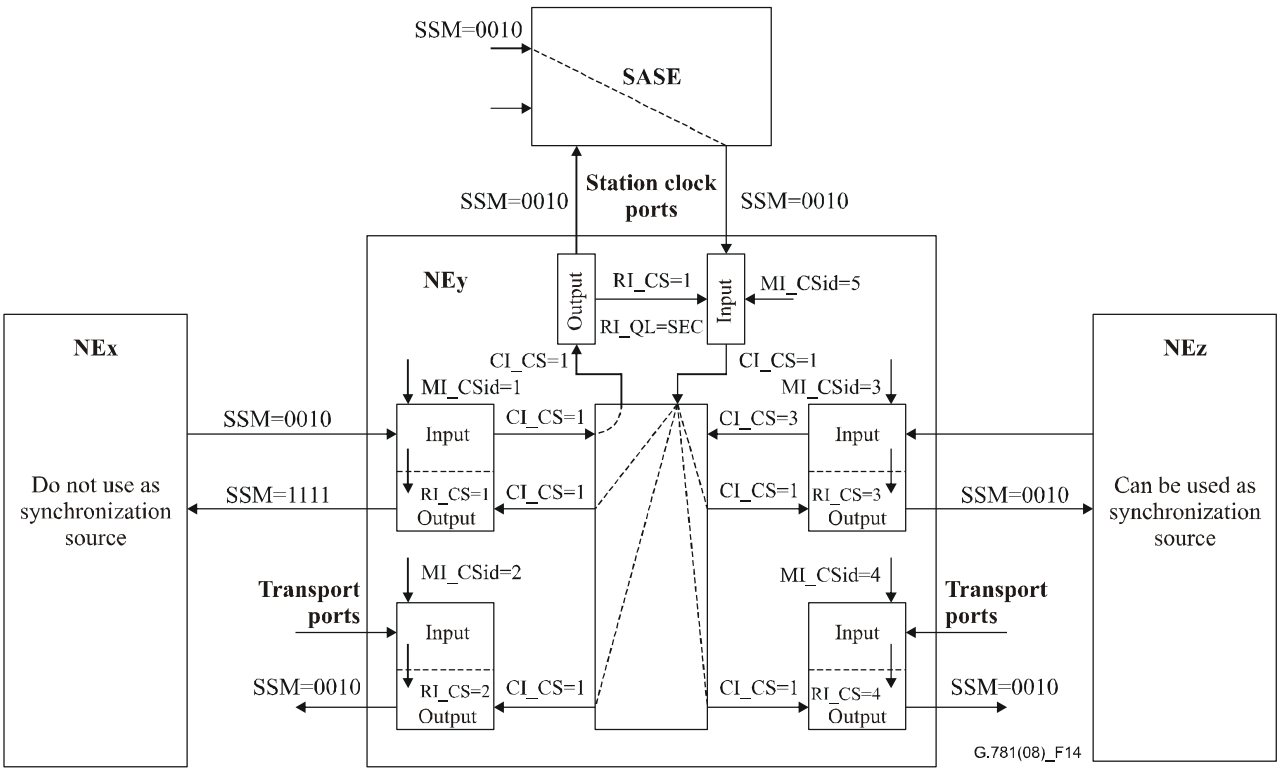


Figure 14 – Limitation of automatic DNU generation in an NE with SASE/BITS timing (SSM/QL supported)

5.13.4 Between NEs with an SEC clock and an NE or SASE/BITS with an SSU clock and several links

NOTE – "Several links" refers to the logical connections from an NE to an SASE/BITS. Each link carries information from a different clock.

A generalization of the timing loop prevention mechanism described in clause 5.13.3, applicable when NE and SASE/BITS are interconnected by several independent links, is for further study.

The necessity to support multiple independent links from an NE to an SASE in option I and option III SDH and packet transport network elements is for further study. SDH and packet transport network elements deployed in option II networks are required to support a minimum of two independent links from an NE to a BITS (see Figure 15).

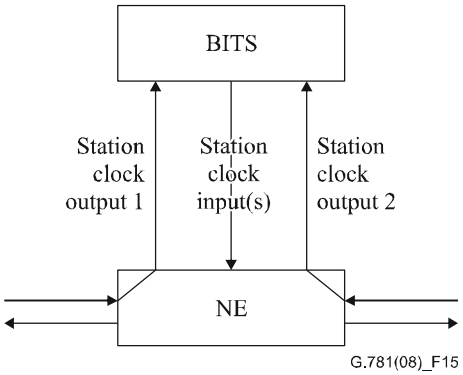


Figure 15 – Example of multiple independent links from NE to BITS

5.14 Delay times for NEs with SEC/ST3/SIC

5.14.1 Delay times for NEs with SEC in option I and III synchronization networks

The following delay times are caused by the atomic functions which perform the selection of the input synchronization reference. Three delays are defined:

– Holdover message delay T_{HM}

  This delay applies when the SEC shall enter holdover because of loss of signal of the input reference and lack of any other available reference. When this event occurs, the SEC goes immediately into holdover but changes the output SSM to the holdover code after a delay which has been defined to be between 500 ms and 2000 ms.

– Non-switching message delay T_{NSM}

  This delay applies when the QL of the selected synchronization source changes but no switchover to another source is performed. The outgoing SSM/TM follows this change at the input within a time defined to be less than 200 ms.

– Switching message delay T_{SM}

  This delay applies when a new synchronization source is selected. The output SSM change, if any, is done after a delay that has been defined to be between 180 ms and 500 ms.

NOTE 1 – The CS signal is used in the SD/NS-XXX_S_So function to detect that a new synchronization source has been selected.

A full description of these times is in Appendix III.

Change of the synchronization direction within a chain of 20 SECs

The above delay times allow the reversal of the synchronization flow in a chain of 20 NEs with SEC timing within 15.6 seconds. The change of the synchronization direction through 20 SECs requires 39 steps, as shown below:

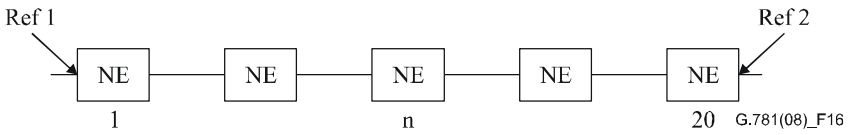


Figure 16 – Linear chain of SECs

NOTE 2 – The interfaces between the NEs in Figure 16 might be a combination of STM-N and synchronous ethernet interfaces.

Step	Action
1	Ref. 1 disappears from the first NE of the chain, NE 1 goes into holdover mode and transmits a new SSM. (T_{HM} 2 s maximum)
2 to 19	NE n (n = 2,3,..,19) transmits the new SSM without switch of reference to NE n. (T_{NSM} 200 ms maximum)
20	NE 20 switches to Ref. 2. (T_{SM} 500 ms maximum)
21 to 39	NE n (n = 19,18,..,1) changes to sync received from NE n+1. (T_{SM} 500 ms maximum)

This leads to a maximum restoration time of 15.6 seconds (T_{HM} + 18 T_{NSM} + 20 T_{SM}).

5.14.2 Delay times for NEs with ST3/SMC in option II synchronization networks

For further study.

5.15 Delay times for NEs with SSU/ST2 or for SASE/BITS

For further study.

5.16 Synchronization layer functions

The atomic functions which are involved in the transport of synchronization within the NE are shown in Figure 17.

This figure shows two synchronization layers plus the transport layer:

a) Synchronization distribution layer: This layer terminates and adapts the synchronization trails to the network synchronization layer and performs a pre-selection of candidate input ports.

b) Network synchronization layer: This layer performs the selection of a timing reference.

c) Transport layer: This layer provides the synchronization-related SD_CI information.

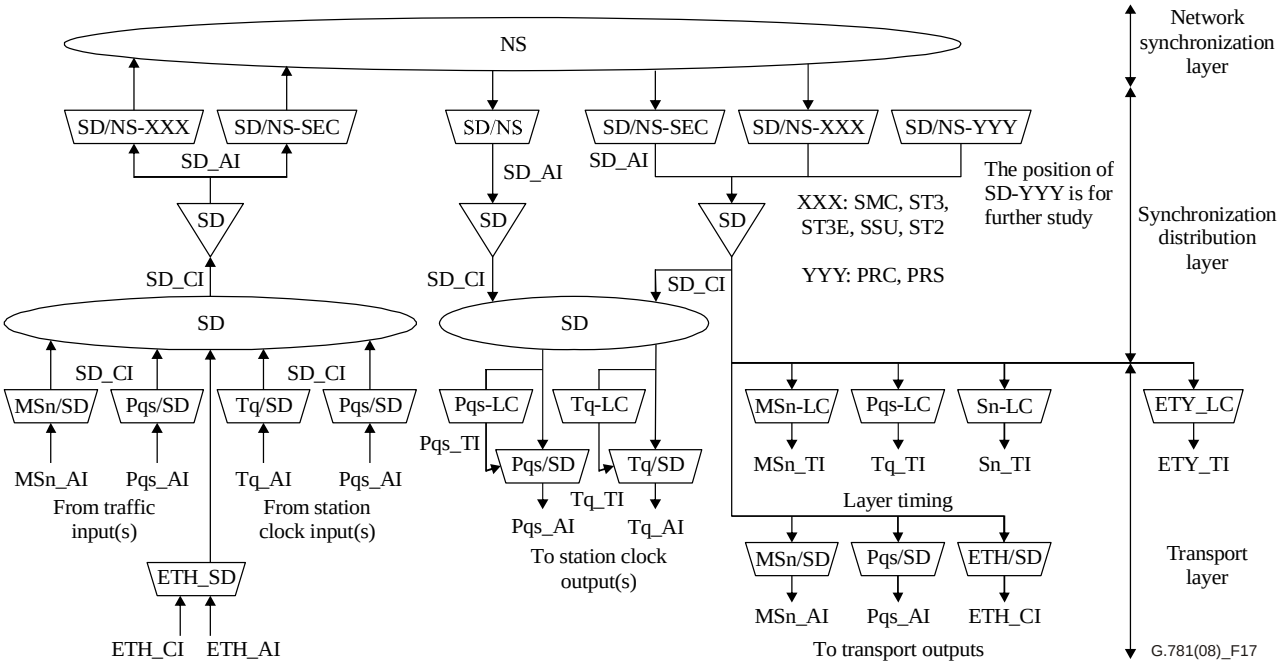


Figure 17 – Synchronization distribution and network synchronization layer atomic functions

Table 14 – Place holder

5.17 Overview of the processes performed within the atomic functions

A list of the synchronization atomic functions and a short description of their functionality is given in Table 15. For a more detailed description see clauses 6 to 9.

Table 15 – Functional overview of atomic functions

Atomic function	Functionality
XX-LC_A_So	Generation of the layer timing.
XX/SD_A_Sk	Access to reference clock. SSM(TM) acceptance and extraction of QL. Generate QL-NotSupported if signal does not support SSM. Generation of CS.
XX/SD_A_So	Insertion of QL into SSM(TM). Generate QL-DNU or squelch to prevent timing loops.
SD_C	Preselection of transport interfaces as possible synchronization sources. Selection of sources for the station clock outputs.
SD_TT_Sk	Report of QL to management. Manual insertion of a fixed QL value.
SD_TT_So	None.
SD/NS-SEC_A_Sk	None.
SD/NS-SSU_A_Sk	For further study.

Table 15 – Functional overview of atomic functions

Atomic function	Functionality
SD/NS_A_So	Generation of the clock for the station clock outputs from the selected synchronization reference.
SD/NS-SEC_A_So	Generation of holdover, locked and freerun modes timings. Generation of the NE clock (SEC type), locked to the selected synchronization reference.
SD/NS-XXX_A_So	Generation of the NE clock (XXX: SMC, ST3, ST3E, SSU, ST2 type) locked to the selected synchronization reference. The functionality and the position are for further study.
SD/NS-YYY_A_So	Generation of the NE clock (YYY: PRC, PRS type). The functionality and the position are for further study.
NS_C	Selection of synchronization reference sources.

5.18 Interworking between option I, II and III synchronization networks

Interworking between option I and II, option I and III and option II and III synchronization networks is not required.

6 Synchronization distribution layer atomic functions

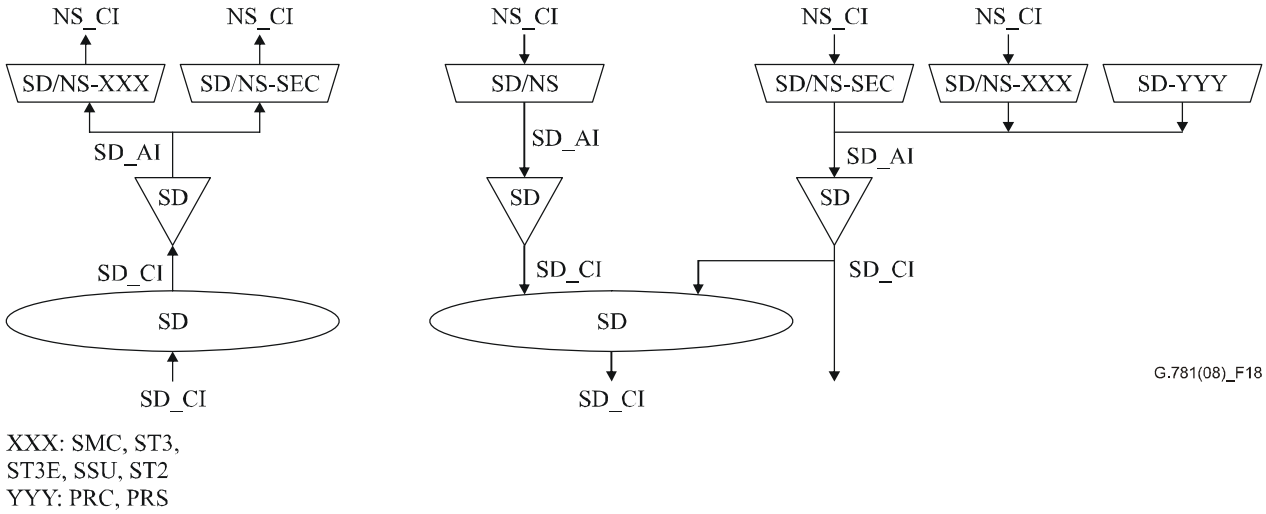


Figure 18 – Synchronization distribution layer atomic functions

SD layer CP

The CI at this point is a clock signal with associated server signal fail, quality level and clock source identifier.

SD layer AP

The AI at this point is a clock signal with associated trail signal fail, quality level and clock source identifier.

6.1 SD connection function (SD_C)

Symbol:

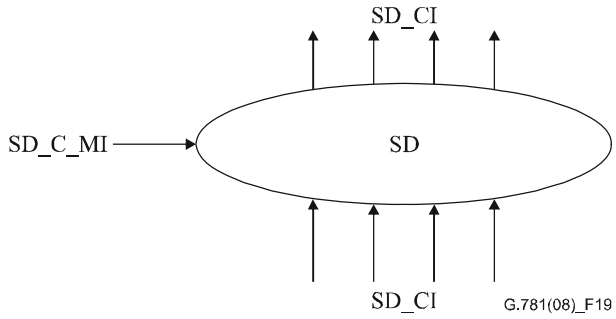


Figure 19 – SD_C symbol

Interfaces:

Table 16 – SD_C input and output signals

Input(s)	Output(s)
Per SD_CI, n x for the function: SD_CI_CK SD_CI_QL SD_CI_SSF SD_CI_CS Per input output connection point SD_C_MI_ConnectionPortIds	Per SD_CI, m x for the function: SD_CI_CK SD_CI_QL SD_CI_SSF SD_CI_CS

Processes:

In the SD_C function, SD layer characteristic information is routed between input (termination) connection points [(T)CPs] and output (T)CPs by means of matrix connections.

NOTE 1 – Neither the number of input/output signals to the connection function, nor the connectivity is specified in this Recommendation. That is a property of individual network elements.

Routing: The function shall be able to connect a specific input with a specific output by means of establishing a matrix connection between the specified input and output. It shall be able to remove an established matrix connection.

NOTE 2 – Broadcast connections are handled as separate connections to the same input CP.

Unconnected SD signal generation: The function shall generate an unconnected SD signal, specified as: SSF true, CS value none, QL value QL-UNC and undefined clock.

NOTE 3 – The unconnected signal is a logical signal defined for the purpose of this formal specification; it is not observable at any of the network element transport interfaces.

Defects: None.

Consequent actions:

If an output of this function is not connected to one of its inputs, the function shall connect the unconnected SD signal to the output.

Defect correlations: None.

Performance monitoring: None.

6.2 SD trail termination functions

6.2.1 SD trail termination source function (SD_TT_So)

Symbol:

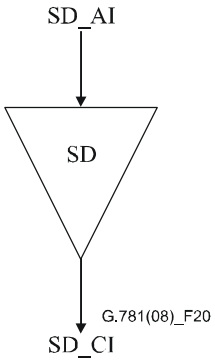


Figure 20 – SD_TT_So symbol

Interfaces:

Table 17 – SD_TT_So input and output signals

Input(s)	Output(s)
SD_AI_CK SD_AI_QL SD_AI_CS SD_AI_TSF	SD_CI_CK SD_CI_QL SD_CI_CS SD_CI_SSF

Processes:

Output SD_CI_CK is derived from and locked to SD_AI_CK.

Defects: None.

Consequent actions:

ASSF ← AI_TSF

Defect correlations: None.

Performance monitoring: None.

6.2.2 SD trail termination sink function (SD_TT_Sk)

Symbol:

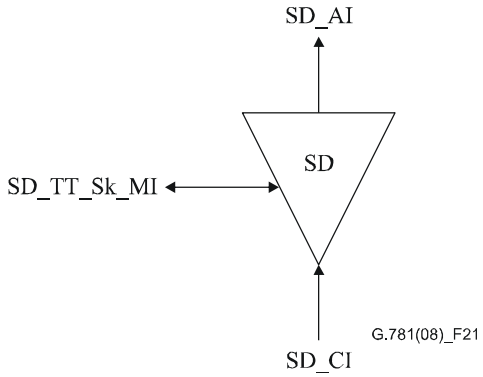


Figure 21 – SD_TT_Sk symbol

Interfaces:

Table 18 – SD_TT_Sk input and output signals

Input(s)	Output(s)
SD_CI_CK	SD_AI_CK
SD_CI_QL	SD_AI_QL
SD_CI_SSF	SD_AI_TSF
SD_CI_CS	SD_AI_CS
SD_TT_Sk_MI_QLoverwrite	SD_TT_Sk_MI_cSSF
SD_TT_Sk_MI_QLfixedValue	SD_TT_Sk_MI_QL
SD_TT_Sk_MI_QLmode	
SD_TT_Sk_MI_Tpmode	
SD_TT_Sk_MI_SSF_Reported	

Processes:

This function terminates a synchronization trail transmitted via one of the synchronization information's transport layers, processes and reports the incoming quality. It can operate in QL-enabled mode and QL-disabled mode.

QL-disabled mode:

In QL-disabled mode, the function shall report the status of the trail (MI_cSSF).

QL-enabled mode:

In QL-enabled mode, the function shall report the status of the trail (MI_cSSF) and the incoming quality level value (CI_QL) via MI_QL.

In QL-enabled mode, AI_CS=CI_CS, in pass through and overwrite operations.

The function shall support the ability to pass through or overwrite the incoming quality level information.

Pass through:

The quality level output (AI_QL) shall be related to the quality level input (CI_QL) signal as specified in clause 5 and Tables 19-21.

Overwrite:

For option I, the quality level output (AI_QL) is a fixed value provisioned via MI_QLfixedValue. The selection between pass through and overwrite mode shall be controlled via MI_QLoverwrite. The default value of MI_QLoverwrite shall be FALSE. The default for MI_QLfixedValue shall be QL-DNU.

For options II and III, overwrite is not defined.

Table 19 – Conversion of quality levels for option I synchronization networks

CI_QL	MI_QLoverwrite	CI_SSF	AI_QL
QL-INV0	False	False	QL-INV
QL-INV1	False	False	QL-INV
QL-PRC	False	False	QL-PRC
QL-INV3	False	False	QL-INV
QL-SSU-A	False	False	QL-SSU-A
QL-INV5	False	False	QL-INV
QL-INV6	False	False	QL-INV
QL-INV7	False	False	QL-INV
QL-SSU-B	False	False	QL-SSU-B
QL-INV9	False	False	QL-INV
QL-INV10	False	False	QL-INV
QL-SEC	False	False	QL-SEC
QL-INV12	False	False	QL-INV
QL-INV13	False	False	QL-INV
QL-INV14	False	False	QL-INV
QL-DNU	False	False	QL-DNU
QL-NSUPP	False	False	QL-NSUPP
QL-UNC	False	True	QL-FAILED
All	True	False	MI_QLfixedValue
All	x	True	QL-FAILED

Table 20 – Conversion of quality levels for option II synchronization networks

CI_QL	CI_SSF	AI_QL
QL-STU	False	QL-STU
QL-PRS	False	QL-PRS
QL-INV2	False	QL-INV
QL-INV3	False	QL-INV
QL-TNC	False	QL-TNC
QL-INV5	False	QL-INV
QL-INV6	False	QL-INV
QL-ST2	False	QL-ST2

Table 20 – Conversion of quality levels for option II synchronization networks

CI_QL	CI_SSF	AI_QL
QL-INV8	False	QL-INV
QL-INV9	False	QL-INV
QL-ST3	False	QL-ST3
QL-INV11	False	QL-INV
QL-SMC	False	QL-SMC
QL-ST3E	False	QL-ST3E
QL-PROV	False	QL-PROV
QL-DUS	False	QL-DUS
QL-DUS	False	QL-NSUPP
QL-UNC	True	QL-FAILED
All	True	QL-FAILED

Table 21 – Conversion of quality levels for option III synchronization networks

CI_QL	CI_SSF	AI_QL
QL-UNK	False	QL-UNK
QL-INV1	False	QL-INV
QL-INV2	False	QL-INV
QL-INV3	False	QL-INV
QL-INV4	False	QL-INV
QL-INV5	False	QL-INV
QL-INV6	False	QL-INV
QL-INV7	False	QL-INV
QL-INV8	False	QL-INV
QL-INV9	False	QL-INV
QL-INV10	False	QL-INV
QL-SEC	False	QL-SEC
QL-INV12	False	QL-INV
QL-INV13	False	QL-INV
QL-INV14	False	QL-INV
QL-INV15	False	QL-INV
QL-NSUPP	False	QL-NSUPP
QL-UNC	True	QL-FAILED
All	True	QL-FAILED

Defects: None.

Consequent actions:

aTSF ← CI_SSF

Defect correlations:

cSSF ← MON and CI_SSF and SSF_Reported

Performance monitoring: None.

6.3 SD adaptation functions

6.3.1 SD layer to NS layer SEC quality adaptation source function (SD/NS-SEC-A_So)

Symbol:

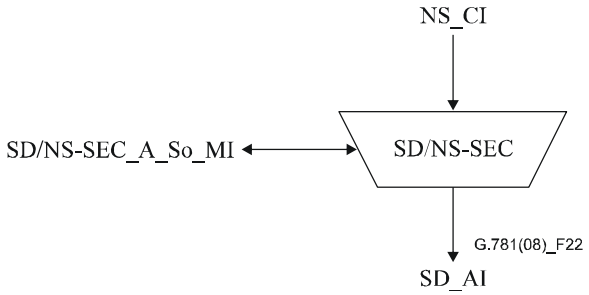


Figure 22 – SD/NS-SEC_A_So symbol

Interfaces:

Table 22 – SD/NS-SEC_A_So input and output signals

Input(s)	Output(s)
NS_CI_CK NS_CI_QL NS_CI_SSF NS_CI_CS SD/NS-SEC_A_So_MI_CkOperation SD/NS-SEC_A_So_MI_QLMode	SD_AI_CK SD_AI_QL SD_AI_CS SD/NS-SEC_A_So_MI_CkMode SD/NS-SEC_A_So_MI_cLTI

Processes:

This function generates a SEC type system clock as defined in [ITU-T G.803] and specified in [ITU-T G.813] or [ITU-T G.8262]. The function shall operate in QL-enabled or QL-disabled mode as selected by MI_QLMode.

The function shall support three types of operation:

– forced free-running operation working in the freerun mode;

– forced holdover operation, working in the holdover mode;

– normal operation, working in the locked or holdover mode depending on the input signals.

These three types of operation are activated by user management input (CkOperation) while modes, defined in [ITU-T G.810], are automatically activated by the status of input signals. Figure 23 shows the relationship between types of operation and modes.

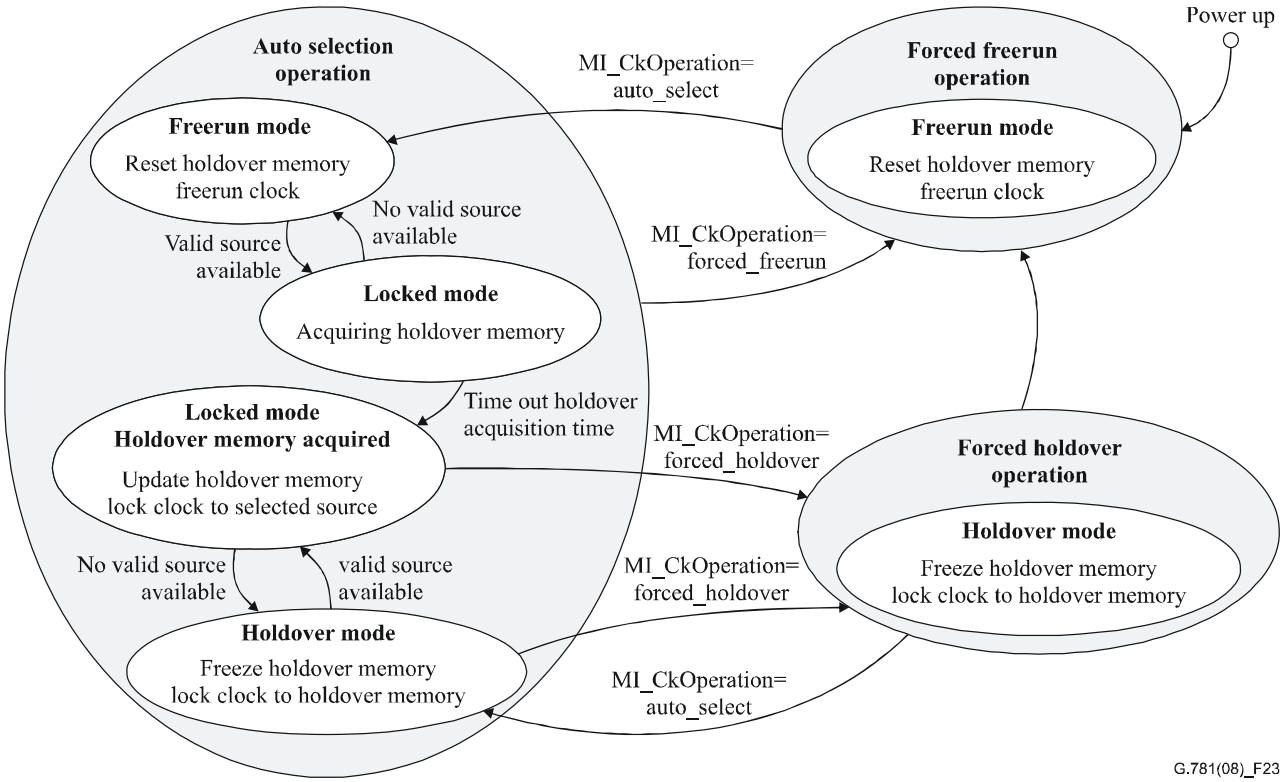


Figure 23 – Operational types

Bandwidth, transients, pull in and pull out ranges, noise, input and output jitter for locked mode operation, holdover accuracy and output phase deviation for holdover mode operation, frequency accuracy, transients, noise and output jitter for freerun mode operation shall be as specified in [ITU-T G.813] or [ITU-T G.8262].

Forced free-running operation:

This type of operation is activated by a management command, the function is in freerun mode:

– Clock generation:

  The outgoing clock (AI_CK) is not defined by an incoming reference or stored incoming reference data in the holdover memory. The holdover memory is reset to a default value.

– QL processing (in QL-enabled mode):

  The outgoing QL of the free-running mode is QL-SEC.

– CS processing:

  The outgoing CS of the free-running mode is "none".

Forced holdover operation:

This type of operation is activated by a management command, the function is in holdover mode.

– Clock generation:

  The outgoing clock (AI_CK) is defined by stored reference data in the holdover memory.

– QL processing (in QL-enabled mode):

  The outgoing QL of the holdover mode is QL-SEC.

– CS processing:

  The outgoing CS of the holdover mode is "none".

Auto selection operation:

This type of operation is activated by a management command. The auto selection operation works according to four modes: freerun, locked-acquiring holdover, locked-holdover acquired and holdover:

– Freerun mode: The freerun mode conforms to the freerun mode defined above. It is essentially a temporary mode until a valid source is available.

– Locked mode, acquiring holdover: This is a temporary mode, when coming from freerun, to acquire holdover memory. It behaves as specified below.

  As shown on Figure 23, some time is required before the holdover memory is acquired.

– Locked mode, holdover acquired: This is a steady state mode, entered when holdover memory is acquired. It behaves as specified below.

– Holdover mode: The holdover mode conforms to the holdover mode defined above. The holdover memory is no longer updated by the incoming reference clock.

The selection between the modes is done automatically depending on the quality of the incoming reference signal and the selected QL mode:

– QL-enabled mode:

  The locked mode is selected if the incoming reference is not in the signal fail state (SSF = false) and the quality level of the incoming reference is better than or equal to QL-SEC.

  The holdover mode is selected without delay when the incoming reference goes into the signal fail state (SSF = true) or the quality level of the incoming signal is lower than QL-SEC.

  The holdover mode is left when both the signal fail clears (SSF = false) and the quality level of the incoming signal is equal to or better than QL-SEC.

– QL-disabled mode:

  The locked mode is selected if the incoming reference is not in the signal fail state (SSF = false).

  The holdover mode is selected when the incoming reference goes into the signal fail state (SSF = true).

The actual selected mode is reported to the management (MI_CkMode).

– Clock generation:

  In freerun mode, the outgoing clock (AI_CK) is generated as specified under forced free-running operation.

  In the locked mode, the outgoing clock (AI_CK) is locked to the incoming reference clock (CI_CK) and the holdover memory is constantly updated with this reference clock.

  In holdover mode, the outgoing clock (AI_CK) is generated as specified under forced holdover operation.

– QL processing (in QL-enabled mode):

  If the function is in the locked mode, the outgoing QL follows the incoming QL.

  In case of a change of the selected synchronization source (which is detected by a change of the incoming CS), the outgoing QL shall be set to the new incoming QL after the settling time, t_s, to allow the internal oscillator to adjust to a possible frequency change.

  If the incoming QL changes without a change of the selected synchronization source (no change of the CI_CS), the outgoing QL shall follow without settling time.

If the function is in the holdover mode, the outgoing QL shall be set to QL-SEC as soon as the incoming CS value is "none" or if the incoming QL is too low (NS_CI_QL<"QL-SEC").

After leaving the holdover mode, the outgoing QL shall be set to the new incoming QL after the settling time, t_s.

The settling time, t_s, shall be in the range of 180 ms to 300 ms.

– CS processing:

Normally, the outgoing CS shall follow the incoming CS immediately.

If the function is in the holdover mode due to a too low QL value of the selected source (NS_CI_QL<"QL-SEC"), the outgoing CS shall be set to "none".

Defects:

The function shall detect a loss of timing inputs (dLTI) if an unconnected signal is present at its connection point (no input selected in NS_C) or if the input signal is failed (CI_SSF active). The defect is raised if CI_SSF = "true" or CI_CS = "none" for at least X seconds. The defect is cleared if CI_SSF = "false" and CI_CS ≠ "none" for at least Y seconds. The values of X and Y are for further study.

Consequent actions: None.

Defect correlation:

cLTI ← dLTI

Performance monitoring: None.

6.3.2 SD layer to NS layer SEC quality adaptation sink function (SD/NS-SEC_A_Sk)

Symbol:

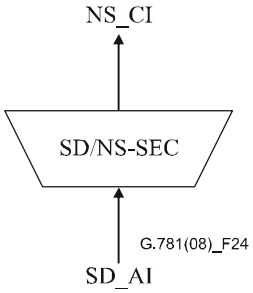


Figure 24 – SD/NS-SEC_A_Sk symbol

Interfaces:

Table 23 – SD/NS-SEC_A_Sk input and output signals

Input(s)	Output(s)
SD_AI_CK SD_AI_QL SD_AI_TSF SD_AI_CS	NS_CI_CK NS_CI_QL NS_CI_SSF NS_CI_CS

Processes:

This function connects input with output only. Currently, no processes are defined within this function.

Defects: None.

Consequent actions:

ASSF ← AI_TSF

Defect correlation: None.

Performance monitoring: None.

6.3.3 SD layer to NS layer SMC quality adaptation source function (SD/NS-SMC_A_So)

This function is for further study.

6.3.4 SD layer to NS layer SMC quality adaptation sink function (SD/NS-SMC_A_Sk)

This function is for further study.

6.3.5 SD layer to NS layer ST3 quality adaptation source function (SD/NS-ST3_A_So)

This function is for further study.

6.3.6 SD layer to NS layer ST3 quality adaptation sink function (SD/NS-ST3_A_Sk)

This function is for further study.

6.3.7 SD layer to NS layer ST3E quality adaptation source function (SD/NS-ST3E_A_So)

This function is for further study.

6.3.8 SD layer to NS layer ST3E quality adaptation sink function (SD/NS-ST3E_A_Sk)

This function is for further study.

6.3.9 SD layer to NS layer SSU quality adaptation source function (SD/NS-SSU_A_So)

This function is for further study.

6.3.10 SD layer to NS layer SSU quality adaptation sink function (SD/NS-SSU_A_Sk)

This function is for further study.

6.3.11 SD layer to NS layer ST2 quality adaptation source function (SD/NS-ST2_A_So)

This function is for further study.

6.3.12 SD layer to NS layer ST2 quality adaptation sink function (SD/NS-ST2_A_Sk)

This function is for further study.

6.3.13 SD layer to NS layer PRC quality adaptation source function (SD/NS-PRC_A_So)

This function is for further study.

6.3.14 SD layer to NS layer PRS quality adaptation source function (SD/NS-PRS_A_So)

This function is for further study.

6.3.15 SD layer to NS layer adaptation source function (SD/NS_A_So)

Symbol:

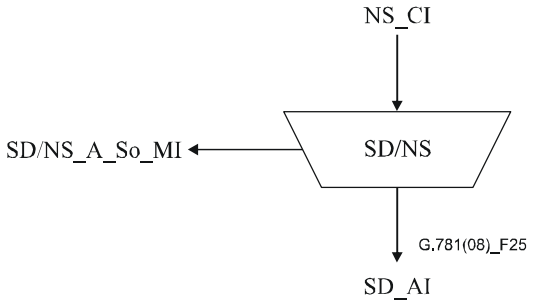


Figure 25 – SD/NS_A_So symbol

Interfaces:

Table 24 – SD/NS_A_So input and output signals

Input(s)	Output(s)
NS_CI_CK NS_CI_QL NS_CI_SSF NS_CI_CS	SD_AI_CK SD_AI_QL SD_AI_CS SD_AI_TSF SD/NS_A_So_MI_cLTI

Processes:

This function produces the station output clock process.

Wander limitation: The wander at the output of this function shall be within the MTIE mask specified in [ITU-T G.813] or [ITU-T G.8262].

NOTE – There might be a need for an AIS generator, this is for further study.

Defects:

The function shall detect a loss of timing inputs (dLTI) if an unconnected signal is present at its connection point (no input selected in NS_C) or if the input signal is failed (CI_SSF active). The defect is raised if CI_SSF = "true" or CI_CS = "none" for at least X seconds. The defect is cleared if CI_SSF = "false" and CI_CS ≠ "none" for at least Y seconds. The values of X and Y are for further study.

Consequent actions:

aTSF ← CI_SSF

Defect correlation:

cLTI ← dLTI

Performance monitoring: None.

7 Network synchronization layer atomic functions

Within this layer, the same connection function is used for one or two independent selection processes which may have independent inputs:

– a single selection of an input reference for the NE synchronization distribution;

– a single or no selection of an input reference for the station clock output.

The use of several independent selection processes for this station clock output is for further study.

These two processes shall work in the same QL mode.

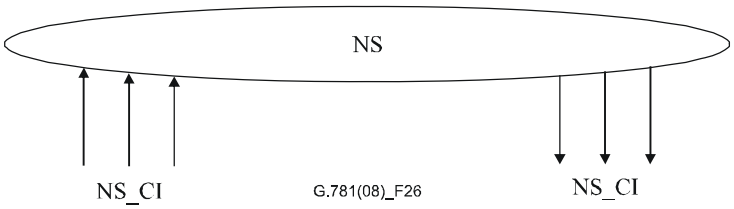


Figure 26 – Network synchronization layer atomic functions

NS layer CP

The CI at this point is a clock signal with associated server signal fail, quality level and clock source identifier.

7.1 NS_connection functions (NS_C)

Symbol:

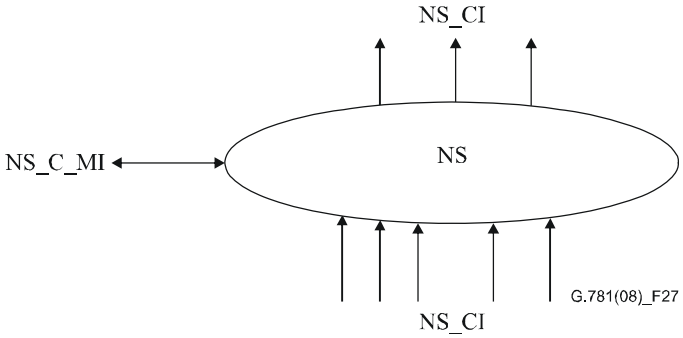


Figure 27 – NS_C symbol

Interfaces:

Table 25 – NS_C input and output signals

Input(s)	Output(s)
Per input:	Per output:
NS_CI_CK NS_CI_SSF NS_CI_QL NS_CI_CS	NS_CI_CK NS_CI_QL NS_CI_SSF NS_CI_CS
Per function:	
NS_C_MI_QLmode NS_C_MI_OptII_QL-PROV_Priority	
Per selector:	Per selector:
NS_C_MI_WTR NS_C_MI_EXTCMD	NS_C_MI_SelectedInput NS_C_MI_Reject_Request
Per input of a selector:	Per input of a selector:
NS_C_MI_priority NS_C_MI_CLR_WTR NS_C_MI_Set_lockout NS_C_MI_Clr_Lockout	NS_C_MI_State

Processes:

This function performs one or more independent selection processes. Each selection process selects a synchronization source out of the nominated set of synchronization source inputs determined by the selection algorithm.

The function can operate in QL-enabled or QL-disabled mode, as defined by MI_QLmode.

NOTE 1 – The number of input signals to the connection process and the number of connection processes in the function are not specified in this Recommendation. That is a property of individual network elements. Examples are presented in Appendix II.

Automatic reference selection process:

The function shall perform the automatic reference selection process as defined in clause 5.6 and Annex A.

External commands:

The function shall support the use of external commands as defined in clause 5.11.

Priority:

The function shall support the use of synchronization source priorities as defined in clause 5.10.

Hold-off time:

The function shall support a hold-off timer per input of a selection process (nominated source) as defined in clause 5.8.

Wait to restore time:

The function shall support a wait to restore timer per input of a selection process (nominated source) as defined in clause 5.9.

Via MI_CLR_WTR the WTR timer can be cleared before the WTR time is expired.

Signal fail extension:

For each input to a selection process, the signal fail information to the selector is a combination (OR function) of the incoming signal fail information (CI_SSF) and the signal fail information delayed by the WTR and hold-off process. Detailed information is provided in Figure A.1.

SF[m] = CI_SF[m] or WTR/HO[CI_SF[m]]

Status report:

The state of each input to a selection process (available, failed, WTR) shall be reported via MI_State.

The actual selected source of a selection process shall be reported via MI_SelectedInput.

Unconnected NS signal generator:

The function shall generate an unconnected NS signal. The unconnected NS signal has a undefined clock, a quality level of QL-UNC, a CS value of "none" and signal fail true.

NOTE 2 – This signal is a logical signal defined for the purpose of this Recommendation; it is not observable as such at any of the network element's interfaces.

Defects: None.

Consequent actions:

If an output of this function is not connected to one of its inputs, the function shall connect the unconnected NS signal to the output.

Defect correlations: None.

Performance monitoring: For further study.

8 Transport layer to SD layer atomic functions

8.1 STM-n multiplex section adaptation functions

8.1.1 STM-N multiplex section to SD adaptation source (MSn/SD_A_So)

Symbol:

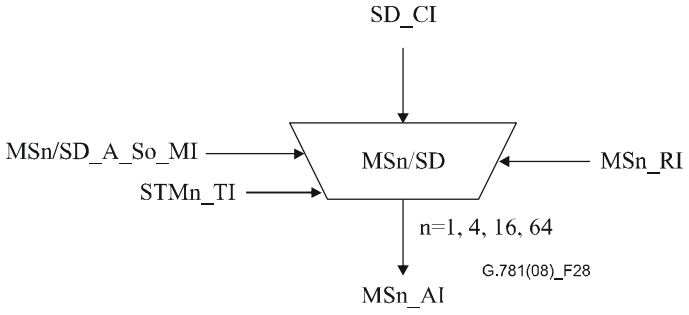


Figure 28 – MSn/SD_A_So symbol

Interfaces:

Table 26 – MSn/SD_A_So input and output signals

Input(s)	Output(s)
SD_CI_QL SD_CI_CS STMn_TI_CK STMn_TI_FS MSn_RI_CS MSn/SD_A_So_MI_SSMdis MSn/SD_A_So_MI_QLmode MSn/SD_A_So_MI_OptII_QLGEN MSn/SD_A_So_MI_OptII_QLRES	MSn_AI_D

Processes:

This function converts the CI_QL into the 4-bit SSM code (bits 5 to 8 of byte S1), as defined in [ITU-T G.707].

The SSM message that shall be generated and inserted depends on the applied quality level indication that is input to the adaptation source function (CI_QL). Tables 27 to 29 present the relationship between the existing set of QLs and the output SSM.

Table 27 – Quality level set coding into synchronization status message (SSM) in option I synchronization networks

Quality level (CI_QL)	SSM coding [MSB..LSB]
QL-PRC	0010
QL-SSU-A	0100
QL-SSU-B	1000
QL-SEC	1011

Table 28 – Quality level set coding into synchronization status message (SSM) in option II synchronization networks

Quality level (CI_QL)	SSM coding [MSB..LSB] MI_OptII_QLGEN=GEN2	SSM coding [MSB..LSB] MI_OptII_QLGEN=GEN1
QL-PRS	0001	0001
QL-STU	0000	0000
QL-ST2	0111	0111
QL-TNC	0100	1010 (Note)
QL-ST3E	1101	1010 (Note)
QL-ST3	1010	1010
QL-SMC	1100	1100
QL-PROV	1110	1110
NOTE – Instead of code "1010", the operator could choose to generate code "1110" (MI_OptII_QLRES is true). Refer to clause 5.5.2.2.		

Table 29 – Quality level set coding into synchronization status message (SSM) in option III synchronization networks

Quality level (CI_QL)	SSM coding [MSB..LSB]
QL-UNK	0000
QL-SEC	1011

QLmode: In the case where the function operates in QL-disabled mode (MI_QLmode = dis), the transmitted SSM code shall be forced to the "1111" pattern.

Timing loop prevention: If RI_CS equals CI_CS, the transmitted SSM shall be forced to the "1111" pattern to prevent a timing loop condition to occur. (See clause 5.13.)

SSM usage: The function supports the capability to prevent synchronization quality information from passing the interface (see clause 5.5.2). In the case where MI_SSMdis is true, the function shall force the SSM to the "1111" pattern.

S1[5-8]: Bits 5 through 8 (bit 5 as MSB) of byte S1 shall transport the 4-bit SSM code.

Defects: None.

Consequent actions:

```
if (MI_QLmode == dis)
then    S1[5-8] = 1111
else    if (RI_CS == CI_CS) or (SSMdis == true)
        then  S1[5-8] = 1111
        else  S1[5-8] = SSM[CI_QL]
        fi
fi
```

Defect correlations: None.

Performance monitoring: None.

8.1.2 STM-N multiplex section to SD adaptation sink (MSn/SD_A_Sk)

Symbol:

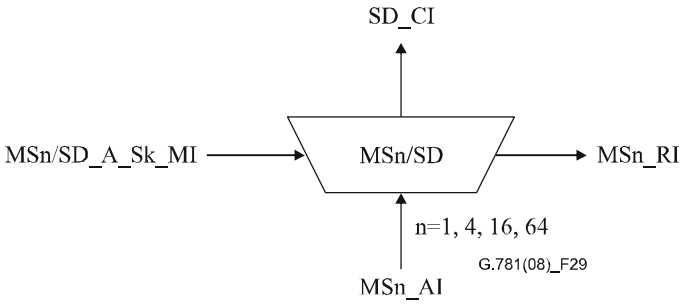


Figure 29 – MSn/SD_A_Sk symbol

Interfaces:

Table 30 – MSn/SD_A_Sk input and output signals

Input(s)	Output(s)
MSn_AI_D MSn_AI_CK MSn_AI_FS MSn_AI_TSF MSn/SD_A_Sk_MI_SSMsupp MSn/SD_A_Sk_MI_CSid MSn/SD_A_Sk_MI_QLmode	SD_CI_CK SD_CI_SSF SD_CI_CS SD_CI_QL MSn_RI_CS

Processes:

This function extracts and accepts the 4-bit synchronization status message (SSM), transmitted via bits 5 to 8 of byte S1 as defined in [ITU-T G.707]. It supplies the timing signal, recovered by the physical section layer, to the synchronization distribution layer.

S1[5-8]: In QL-enabled mode, and if SSMsupp is true, bits 5 to 8 of byte S1 shall be recovered.

For options I and III, the recovered bits 5 to 8 of byte S1 shall be accepted if the same code is present in three consecutive frames.

For option II, a received SSM code is accepted after receiving, in at least 8 consecutive samples (not necessarily consecutive frames), an identical (new) value. The sampling rate must be such that a new value can be validated within 1 second (assuming no bit errors). If no validated SSM is detected for a period greater than 10 seconds, the value "1111" shall be assumed. At least once per 10 seconds, the evaluation of the received SSM shall be restarted.

The accepted code shall be converted to a quality level QL[SSM] as specified in Table 8 (option I), Table 10 (option II), Table 12 (option III) and output via CI_QL.

QLmode: In the case where the function operates in QL-disabled mode (MI_QLmode = dis), the received SSM code shall be ignored and the CI_QL shall be forced to the QL-NSUPP.

SSM support: In the case where MI_SSMsupp is false, the received SSM bit in the S1 byte should not be interpreted as a valid QL value and the CI_QL shall be forced to the QL-NSUPP.

Clock source identifier: The function shall insert the clock source identifier received via MI_CSid into CI_CS and RI_CS to support timing loop prevention as described in clause 5.13.

Defects: None.

Consequent actions:

aSSF ← AI_TSF

if (MI_QLmode == disabled) or (MI_SSMsupp == false)

then CI_QL = QL-NSUPP

else CI_QL = QL[SSM]

fi

Defect correlations: None.

Performance monitoring: None.

8.2 Pqs adaptation functions

8.2.1 Pqs to SD adaptation source (Pqs/SD_A_So)

Symbol:

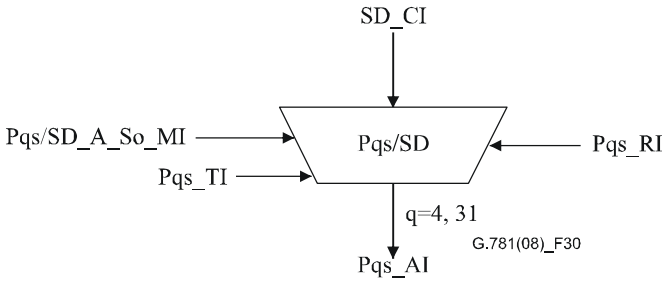


Figure 30 – Pqs/SD_A_So symbol

Interfaces:

Table 31 – Pqs/SD_A_So input and output signals

Input(s)	Output(s)
SD_CI_QL SD_CI_CS Pqs_TI_CK Pqs_TI_FS Pqs_TI_MFS Pqs_RI_CS Pqs/SD_A_So_MI_TMmode Pqs/SD_A_So_MI_SSMdis Pqs/SD_A_So_MI_QLmode	Pqs_AI_D

Processes:

This function converts the CI_QL and CI_SSF information into the 4-bit SSM code (multiframed bit 8 of byte MA), or into the 1-bit TM code, as defined in [b-ITU-T G.832]. This is controlled by MI_TMmode.

TMmode: In the case where TMmode is disabled, the function shall generate the SSM code. In the case where TMmode is enabled, the function shall generate the TM code.

MA[6-7]: If TMmode is disabled, the value of the multiframe indicator bits shall be set as specified by [b-ITU-T G.832], 500 µs TU multiframe sequence, and aligned with Pqs_TI_MFS. Such a multiframe indicator is available for SSM processing. If TMmode is enabled, the multiframe indicator is not required for this mode of operation.

Figure 31 – Multiframe indicator bits in byte MA

The SSM or TM message that shall be generated and inserted depends on the applied quality level indication that is input to the adaptation source function (CI_QL). Table 32 presents the relation between the existing set of QLs and the output SSM and TM codes.

NOTE – There may be another parallel adaptation function, e.g., Pqs/TUG_A_So that also generates a multiframe sequence. The equipment should take care that the multiframe sequences generated are the same from all adaptation functions involved.

MA[8], MA[8][1-4]: In the case where TMmode is disabled, bit 8 of byte MA in a four-frame multiframe (first frame as MSB) shall transport the 4-bit SSM code. In the case where TMmode is enabled, bit 8 of byte MA shall transport the 1-bit TM code.

Table 32 – Quality level set coding into synchronization status message and timing marker

Quality level (CI_QL)	SSM coding [MSB..LSB]	TM coding
QL-PRC	0010	0
QL-SSU-A	0100	1
QL-SSU-B	1000	1
QL-SEC	1011	1

QLmode: In the case where the function operates in QL-disabled mode (MI_QLmode = dis), the transmitted SSM code shall be forced to the "1111" pattern, while the transmitted TM code shall be forced to the "1" pattern.

Timing loop prevention: If RI_CS equals CI_CS, the transmitted SSM[TM] shall be forced to the "1111" ["1"] pattern to prevent a timing loop condition from occurring. See clause 5.13.

SSM/TM usage: The function supports the capability to prevent synchronization quality information from passing the interface (see clause 5.5.2). In the case where MI_SSMdis is true, the function shall force the SSM[TM] to the "1111" ["1"] pattern.

Defects: None.

Consequent actions:

```
if (MI_TMmode == dis)
then    if (MI_QLmode == dis)
        then   MA[8][1-4] = 1111
        else   if (RI_CS == CI_CS) or (SSMdis == true)
        then   MA[8][1-4] = 1111
        else   MA[8][1-4] = SSM[CI_QL]
             fi
        fi
else    if (MI_QLmode == dis)
        then   MA[8] = 1
        else   if (RI_CS == CI_CS) or (SSMdis == true)
        then   MA[8] = 1
        else   MA[8] = TM[CI_QL]
        fi
        fi
fi
```

Defect correlations: None.

Performance monitoring: None.

8.2.2 Pqs to SD adaptation sink (Pqs/SD_A_Sk)

Symbol:

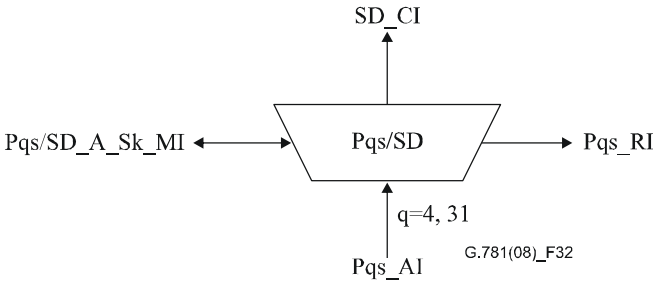


Figure 32 – Pqs/SD_A_Sk symbol

Interfaces:

Table 33 – Pqs/SD_A_Sk input and output signals

Input(s)	Output(s)
Pqs_AI_D Pqs_AI_CK Pqs_AI_FS Pqs_AI_TSF Pqs/SD_A_Sk_MI_TMmode Pqs/SD_A_Sk_MI_QLmode Pqs/SD_A_Sk_MI_SSMsupp Pqs/SD_A_Sk_MI_CSid	SD_CI_CK SD_CI_SSF SD_CI_CS SD_CI_QL Pqs_RI_CS Pqs/SD_A_Sk_MI_cLOM

Processes:

This function extracts and accepts the 4-bit synchronization status message (SSM), transmitted via the multiframed bit 8 of byte MA, or the 1-bit timing marker (TM), transmitted via bit 8 of byte MA as defined in [b-ITU-T G.832]. It supplies the timing signal, recovered by the physical section layer, to the synchronization distribution layer.

TMmode: In the case where TMmode is disabled, the function shall interpret bit 8 of byte MA as the SSM code. In the case where TMmode is enabled, the function shall interpret bit 8 of byte MA as the TM code.

MA[6-7]: In QL-enabled mode, and if TMmode is disabled and if SSMsupp is true, the function shall recover the 500 µs (multi)frame start phase performing multi-frame alignment on bits 6 and 7 of byte MA. Out-of-multiframe (OOM) shall be assumed once an error is detected in the MA bit 6 and 7 sequence. Multiframe alignment shall be assumed to be recovered, and the in-multiframe (IM) state shall be entered, when an error-free MA sequence is found in four consecutive Pqs frames.

MA[8][1-4]: In QL-enabled mode, and if TMmode is disabled and SSMsupp is true, bit 8 of byte MA in a four frame multiframe (first frame as MSB) shall be recovered and accepted if the same code is present in three consecutive 4-bit multiframes. The accepted code shall be converted to a quality level QL[SSM] as specified in Table 8 (option I) and output via CI_QL.

MA[8]: In QL-enabled mode, and if TMmode is enabled and SSMsupp is true, bit 8 of byte MA shall be recovered and accepted if the same code is present in three consecutive frames. The accepted code shall be converted to a quality level QL[TM] as specified in Table 9 and output via CI_QL.

QLmode: In the case where the function operates in QL-disabled mode (MI_QLmode = dis), the received SSM or TM code shall be ignored and the CI_QL shall be forced to the QL-NSUPP.

SSM/TM support: In the case where MI_SSMsupp is false, the received SSM or TM code shall be ignored and the CI_QL shall be forced to the QL-NSUPP.

Clock source identifier: The function shall insert the clock source identifier received via MI_CSid into CI_CS and RI_CS to support timing loop prevention as described in clause 5.13.

Defects:

If the multiframe alignment process is in the OOM state, and the MA[6-7] multiframe is not recovered within X ms, a dLOM defect shall be declared. Once in a dLOM state, this state shall be exited when the multiframe is recovered (multiframe alignment process enters the IM state). X shall be a value in the range 1 ms to 5 ms. X is not configurable. dLOM shall be cleared when QLmode is disabled, or SSMsupp is false, or TMmode is enabled.

Consequent actions:

```
aSSF    ←  dLOM or AI_TSF
    if (MI_QLmode == disabled) or (MI_SSMsupp == false)
    then    CI_QL = QL-NSUPP
    else    if (MI_TMmode == disabled)
            then    CI_QL = QL[SSM]
            else    CI_QL = QL[TM]
            fi
    fi
```

Defect correlations:

```
cLOM  ←  dMFP and (not AI_TSF)
```

NOTE – There may be another parallel adaptation function, e.g., Pqs/TUG_A_sk that also generates cLOM. The EMF should take care that fLOM is reported only once.

Performance monitoring: None.

8.3 P12s layer adaptation functions

8.3.1 P12s layer adaptation source functions

Two types of P12s/SD_A_So functions are defined:

– type 1 for a 2 Mbit/s station clock output supporting SSM: P12s/SD-sc-1_A_So;

– type 2 for a 2 Mbit/s station clock output not supporting SSM: P12s/SD-sc-2_A_So.

Other types are for further study.

8.3.1.1 Type 1 P12s to SD adaptation source for station clock output supporting SSM (P12s/SD-sc-1_A_So)

Symbol:

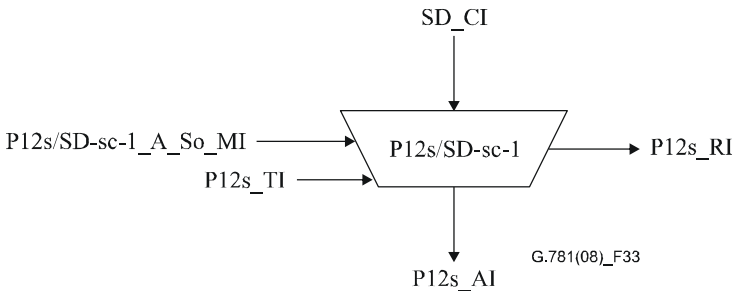


Figure 33 – P12s/SD-sc-1_A_So symbol

Interfaces:

Table 34 – P12s/SD-sc-1_A_So input and output signals

Input(s)	Output(s)
SD_CI_QL SD_CI_CS SD_CI_SSF P12s_TI_CK P12s_TI_FS P12s_TI_MFS P12s/SD-sc-1_A_So_MI_SelSaSSM P12s/SD-sc-1_A_So_MI_QLmode P12s/SD-sc-1_A_So_MI_SSMsupp P12s/SD-sc-1_A_So_MI_QLminimum	P12s_AI_D P12s_AI_CK P12s_AI_FS P12s_AI_MFS P12s_AI_AISinsert P12s_RI_CS

Processes:

This function converts the CI_QL and CI_SSF information into the 4-bit SSM code transmitted in one of the five S_a bits, as defined in [ITU-T G.704], and an AISinsert control signal.

The SSM message that shall be generated and inserted depends on the applied quality level indication that is input to the adaptation source function (CI_QL). Table 35 presents the relationship between the existing set of QLs and the output SSM codes.

Table 35 – Quality level set coding into synchronization status message in option I synchronization network

Quality level (CI_QL)	SSM coding [MSB..LSB]
QL-PRC	0010
QL-SSU-A	0100
QL-SSU-B	1000
QL-SEC	1011
QL-UNC	1111

QLmode: In the case where the function operates in QL-disabled mode (MI_QLmode = dis), the transmitted SSM code shall be forced to the "1111" pattern and AI_AISinsert shall be used to signal that no synchronization source is available.

S_{ax}: The 4-bit SSM code shall be inserted in one of the S_a bits (S_{ax}, x = 4 to 8) as selected via MI_SelSaSSM. The 4-bit SSM code shall be transported in alignment with the CRC-4 submultiframe.

Interworking: For interworking with old equipment not supporting SSM processing, AIS insertion can be used instead of SSM insertion to pass synchronization quality information via the interface. In the case where MI_SSMsupp is true, the function shall force the SSM to the "1111" pattern and AI_AISinsert shall be used to signal that no synchronization source is available or CI_QL is below MI_QLminimum.

Clock source identifier and quality level: The function shall insert the clock source identifier received via CI_CS into RI_CS to support timing loop prevention as described under consequent actions (see clause 5.13).

Defects: None.

Consequent actions:

```
if (MI_QLmode == dis)
then    Sax[1-4] = 1111
        if (CI_SSF == true)
        then  AI_AISinsert = true
              RI_CS = none
        else  AI_AISinsert = false
              RI_CS = CI_CS
        fi
else    if (MI_SSMsupp == true)
        then  Sax[1-4] = 1111
              if (CI_SSF == true) or (CI_QL<MI_QLminimum)
              then    AI_AISinsert = true
                      RI_CS = none
              else    AI_AISinsert = false
                      RI_CS = CI_CS
              fi
        else  AI_AISinsert = false
              if (CI_SSF == true)
              then    Sax[1-4] = 1111
                      RI_CS = none
              else    Sax[1-4] = SSM[CI_QL]
                      RI_CS = CI_CS
              fi
        fi
fi
```

Defect correlations: None.

Performance monitoring: None.

8.3.1.2 Type 2 P12s to SD adaptation source for station clock output port not supporting SSM (P12s/SD-sc-2_A_So)

Symbol:

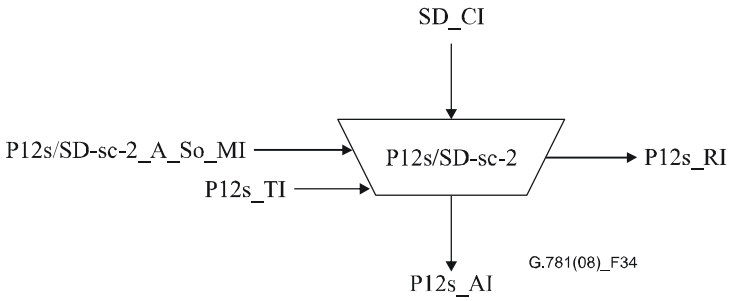


Figure 34 – P12s/SD-sc-2_A_So symbol

Interfaces:

Table 36 – P12s/SD-sc-2_A_So input and output signals

Input(s)	Output(s)
SD_CI_QL SD_CI_CS SD_CI_SSF P12s_TI_CK P12s_TI_FS P12s_TI_MFS P12s/SD-sc-2_A_So_MI_QLminimum P12s/SD-sc-2_A_So_MI_QLmode	P12s_AI_CK P12s_AI_FS P12s_AI_MFS P12s_AI_AISinsert P12s_RI_CS

Processes:

This function converts the CI_QL and CI_SSF information into an AISinsert control signal.

QLmode: In the case where the function operates in QL-disabled mode (MI_QLmode = dis), AI_AISinsert shall be activated if CI_SSF is true. In the case of QL-enabled mode, AI_AISinsert shall be activated if CI_SSF is true or CI_QL is below MI_QLminimum.

Clock source identifier and quality level: The function shall insert the clock source identifier received via CI_CS into RI_CS to support timing loop prevention as described under consequent actions (see also clause 5.13).

Defects: None.

Consequent actions:

```
if (MI_QLmode == dis)
then    if (CI_SSF == true)
        then  AI_AISinsert = true
              RI_CS = none
        else  AI_AISinsert = false
              RI_CS = CI_CS
        fi
```

```
else    if (CI_SSF == true) or (CI_QL < MI_QLminimum)
        then  AI_AISinsert = true
              RI_CS = none
        else  AI_AISinsert = false
              RI_CS = CI_CS
        fi
fi
```

Defect correlations: None.

Performance monitoring: None.

8.3.2 P12s layer adaptation sink functions

Two types of P12s/SD_A_Sk functions are defined:

– type 1 for a 2 Mbit/s traffic input port: P12s/SD-tf_A_Sk;

– type 2 for a 2 Mbit/s station clock input port: P12s/SD-sc_A_Sk.

8.3.2.1 Type 1 P12s to SD adaptation sink for traffic input port (P12s/SD-tf_A_Sk)

Symbol:

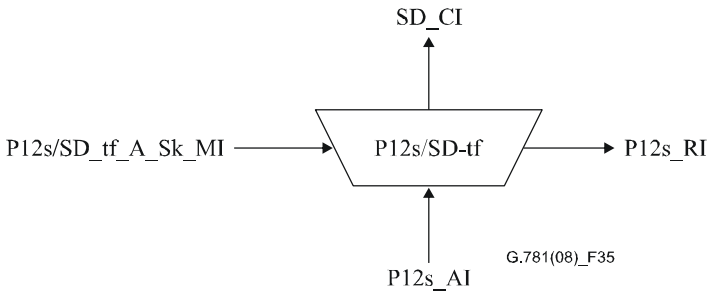


Figure 35 – P12s/SD-tf_A_Sk symbol

Interfaces:

Table 37 – P12s/SD-tf_A_Sk input and output signals

Input(s)	Output(s)
P12s_AI_D P12s_AI_CK P12s_AI_FS P12s_AI_TSF P12s_AI_MFS P12s_AI_MFP P12s/SD-tf_A_Sk_MI_SSMsupp P12s/SD-tf_A_Sk_MI_SelSaSSM P12s/SD-tf_A_Sk_MI_QLmode P12s/SD-tf_A_Sk_MI_CSid	SD_CI_CK SD_CI_SSF SD_CI_CS SD_CI_QL P12s_RI_CS (for further study)

Processes:

This function extracts and accepts the 4-bit synchronization status message (SSM), transmitted via one of the S_a bits as defined in [ITU-T G.704]. It supplies the timing signal, recovered by the physical section layer, to the synchronization distribution layer.

S_{ax}[1-4]: In QL-enabled mode, and if SSMsupp is true, bits S_{ax}[1] to S_{ax}[4] (x = MI_SelSaSSM is a value in the set [4, 5, 6, 7, 8]) shall be recovered and accepted if the same code is present in three consecutive frames. The accepted code shall be converted to a quality level QL[SSM] as specified in Table 8 (option I) and output via CI_QL.

QLmode: In the case where the function operates in QL-disabled mode (MI_QLmode = dis), the received SSM code shall be ignored and the CI_QL shall be forced to the QL-NSUPP.

SSM support: In the case where MI_SSMsupp is false, the received SSM code shall be ignored and the CI_QL shall be forced to the QL-NSUPP.

Clock source identifier: The function shall insert the clock source identifier received via MI_CSid into CI_CS to support timing loop prevention as described in clause 5.13. RI_CS generation is for further study.

Defects: None.

Consequent actions:

aSSF ← AI_TSF or (AI_ MFP==false and QLmode==enabled and SSMsupp==true)
if (MI_QLmode == disabled) or (MI_SSMsupp == false)
then CI_QL = QL-NSUPP
else CI_QL = QL[SSM]
fi

Defect correlations: None

Performance monitoring: None.

8.3.2.2 Type 2 P12s to SD adaptation sink for station clock input port (P12s/SD-sc_A_Sk)

Symbol:

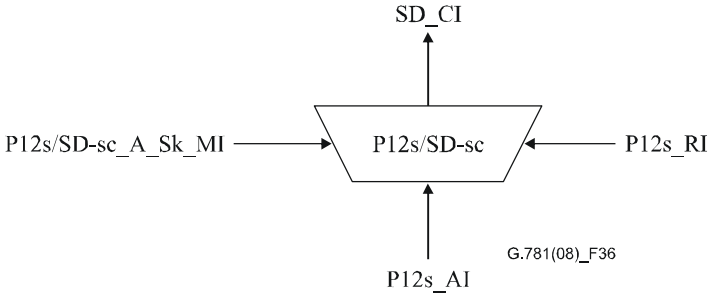


Figure 36 – P12s/SD-sc_A_Sk symbol

Interfaces:

Table 38 – P12s/SD-sc_A_Sk input and output signals

Input(s)	Output(s)
P12s_AI_D P12s_AI_CK P12s_AI_FS P12s_AI_TSF P12s_AI_MFS P12s_AI_MFP P12s_RI_CS P12s/SD-sc_A_Sk_MI_SSMsupp P12s/SD-sc_A_Sk_MI_SelSaSSM P12s/SD-sc_A_Sk_MI_CSid P12s/SD-sc_A_Sk_MI_QLmode	SD_CI_CK SD_CI_SSF SD_CI_CS SD_CI_QL

Processes:

This function extracts and accepts the 4-bit synchronization status message (SSM), transmitted via one of the S_a bits as defined in [ITU-T G.704]. It supplies the timing signal, recovered by the physical section layer, to the synchronization distribution layer.

S_{ax}: In QL-enabled mode, and if SSMsupp is true, bits $S_{ax}[1]$ to $S_{ax}[4]$ (x = MI_SelSaSSM is a value in the set [4, 5, 6, 7, 8]) shall be recovered and accepted if the same code is present in three consecutive frames. The accepted code shall be converted to a quality level QL[SSM] as specified in Table 8 and output via CI_QL.

QLmode: In the case where the function operates in QL-disabled mode (MI_QLmode = dis), the received SSM code shall be ignored and the CI_QL shall be forced to the QL-NSUPP.

SSM support: In the case where MI_SSMsupp is false, the received SSM code shall be ignored and the CI_QL shall be forced to the QL-NSUPP.

Clock source identifier: The function shall process the clock source identifier received via RI_CS to support timing loop prevention (see clause 5.13). The function shall determine the value of the CI_CS output signal as follows:

```
if (RI_CS == none)
then    CI_CS = MI_CSid
else    CI_CS = RI_CS
fi
```

Defects: None.

Consequent actions:

```
aSSF    ←  AI_TSF or (AI_MFP==false and QLmode==enabled and SSMsupp==true)
    if (MI_QLmode == disabled) or (MI_SSMsupp == false)
    then    CI_QL = QL-NSUPP
    else    CI_QL = QL[SSM]
    fi
```

Defect correlations: None

Performance monitoring: None.

8.4 T12 layer adaptation functions

8.4.1 T12 to SD adaptation source (T12/SD_A_So)

Symbol:

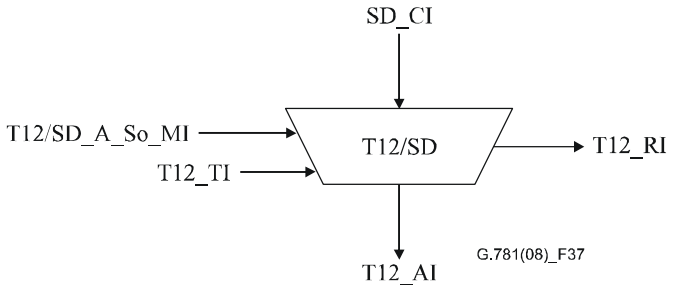


Figure 37 – T12/SD_A_So symbol

Interfaces:

Table 39 – T12/SD_A_So input and output signals

Input(s)	Output(s)
SD_CI_QL SD_CI_CS SD_CI_SSF T12_TI_CK T12/SD_A_So_MI_QLminimum T12/SD_A_So_MI_QLmode	T12_AI_CK T12_AI_SQLCH T12_RI_CS

Processes:

This function converts the CI_QL and CI_SSF information into an SQLCH control signal.

QLmode: In the case where the function operates in QL-disabled mode (MI_QLmode = dis), AI_SQLCH shall be activated if CI_SSF is true. In the case of QL-enabled mode, AI_SQLCH shall be activated if CI_SSF is true or CI_QL is below MI_QLminimum.

Clock source identifier and quality level: The function shall insert the clock source identifier received via CI_CS into RI_CS to support timing loop prevention as described under consequent actions (see clause 5.13).

Defects: None.

Consequent actions:

```
if (MI_QLmode == dis)
then    if (CI_SSF == true)
        then   AI_SQLCH = true
               RI_CS = none
        else   AI_SQLCH = false
               RI_CS = CI_CS
        fi
else    if (CI_SSF == true) or (CI_QL < MI_QLminimum)
        then   AI_SQLCH = true
```

RI_CS = none
else AI_SQLCH = false
RI_CS = CI_CS
fi
fi

Defect correlations: None.

Performance monitoring: None.

8.4.2 T12 to SD adaptation sink (T12/SD_A_Sk)

Symbol:

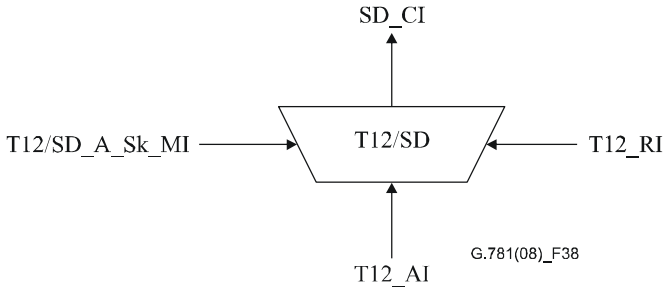


Figure 38 – T12/SD_A_Sk symbol

Interfaces:

Table 40 – T12/SD_A_Sk input and output signals

Input(s)	Output(s)
T12_AI_CK T12_AI_TSF T12_RI_CS T12/SD_A_Sk_MI_Csid	SD_CI_CK SD_CI_SSF SD_CI_CS SD_CI_QL

Processes:

This function adapts the 2048 kHz timing information from an external reference to equipment-specific timing characteristic information. This function regenerates the received clock signal and supplies the recovered timing signal to the synchronization distribution layer.

Regeneration: The function shall output a valid clock signal when any combination of the following signal conditions exists at the input:

– an input electrical amplitude level with any value in the range specified by [ITU-T G.703];

– jitter modulation applied to the input signal with any value defined in [ITU-T G.813] or [ITU-T G.8262];

– the input signal frequency has any value in the range 2048 kHz ± 50 ppm.

NOTE – The frequency and jitter/wander tolerance is further constrained by the requirements of the client (SD) layer. For example, in the MS SDH layer, the frequency offset should not exceed 4.6 ppm.

SSM support: CI_QL shall be forced to the QL-NSUPP.

Clock source identifier: The function shall process the clock source identifier received via RI_CS to support timing loop prevention (see clause 5.13). The function shall determine the value of the CI_CS output signal as follows:

if (RI_CS == none)
then CI_CS = MI_CSid
else CI_CS = RI_CS
fi

Defects: None.

Consequent actions:

aSSF ← AI_TSF

Defect correlations: None

Performance monitoring: None.

8.5 P11s layer adaptation functions

8.5.1 P11s to SD adaptation source (P11s/SD_A_So)

For further study.

8.5.2 P11s to SD adaptation sink (P11s/SD_A_Sk)

For further study.

8.6 T01 layer adaptation functions

8.6.1 T01 to SD adaptation source (T01/SD_A_So)

Symbol:

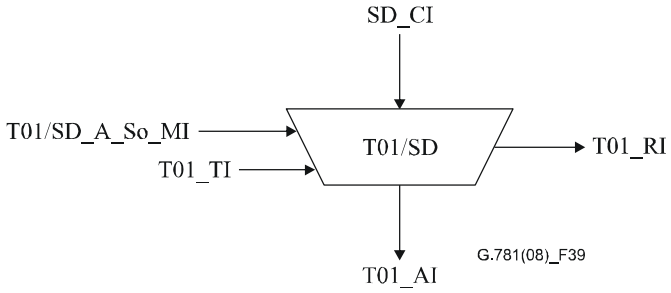


Figure 39 – T01/SD_A_So symbol

Interfaces:

Table 41 – T01/SD_A_So input and output signals

Input(s)	Output(s)
SD_CI_QL SD_CI_CS SD_CI_SSF T01_TI_CK T01/SD_A_So_MI_QLminimum T01/SD_A_So_MI_QLmode	T01_AI_CK T01_AI_SQLCH T01_RI_CS

Processes:

This function converts the CI_QL and CI_SSF information into an SQLCH control signal.

QLmode: In the case where the function operates in QL-disabled mode (MI_QLmode = dis), AI_SQLCH shall be activated if CI_SSF is true. In the case of QL-enabled mode, AI_SQLCH shall be activated if CI_SSF is true or CI_QL is below MI_QLminimum.

Clock source identifier and quality level: The function shall insert the clock source identifier received via CI_CS into RI_CS to support timing loop prevention as described under consequent actions (see clause 5.13).

Defects: None.

Consequent actions:

```
if (MI_QLmode == dis)
then    if (CI_SSF == true)
        then  AI_SQLCH = true
              RI_CS = none
        else  AI_SQLCH = false
              RI_CS = CI_CS
        fi
else    if (CI_SSF == true) or (CI_QL < MI_QLminimum)
        then  AI_SQLCH = true
              RI_CS = none
        else  AI_SQLCH = false
              RI_CS = CI_CS
        fi
fi
```

Defect correlations: None.

Performance monitoring: None.

8.6.2 T01 to SD adaptation sink (T01/SD_A_Sk)

Symbol:

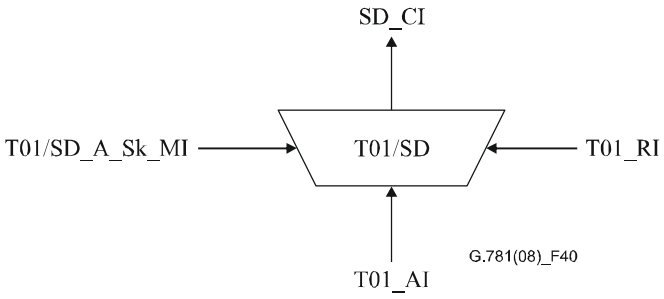


Figure 40 – T01/SD_A_Sk symbol

Interfaces:

Table 42 – T01/SD_A_Sk input and output signals

Input(s)	Output(s)
T01_AI_CK T01_AI_TSF T01_RI_CS T01/SD_A_Sk_MI_Csid	SD_CI_CK SD_CI_SSF SD_CI_CS SD_CI_QL

Processes:

This function adapts the 64 kHz T01 timing information from an external reference to equipment-specific timing characteristic information. This function regenerates the received clock signal and supplies the recovered timing signal to the synchronization distribution layer.

Regeneration: The function shall output a valid clock signal when any combination of the following signal conditions exists at the input:

– an input electrical amplitude level with any value in the range specified by [ITU-T G.703];

– jitter modulation applied to the input signal with any value defined in [ITU-T G.813] or [ITU-T G.8262];

– the input signal frequency has any value in the range 64 kHz ± *TBD* ppm.

NOTE – The frequency and jitter/wander tolerance is further constrained by the requirements of the client (SD) layer.

SSM support: CI_QL shall be forced to the QL-UNK.

Clock source identifier: The function shall process the clock source identifier received via RI_CS to support timing loop prevention (see clause 5.13). The function shall determine the value of the CI_CS output signal as follows:

```
if (RI_CS == none)
then    CI_CS = MI_CSid
else    CI_CS = RI_CS
fi
```

Defects: None.

Consequent actions:

aSSF ← AI_TSF

Defect correlations: None

Performance monitoring: None.

8.7 T02 layer adaptation functions

8.7.1 T02 to SD adaptation source (T02/SD_A_So)

For further study.

8.7.2 T02 to SD adaptation sink (T02/SD_A_Sk)

Symbol:

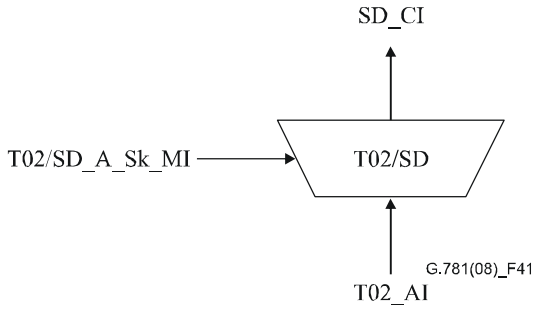


Figure 41 – T02/SD_A_Sk symbol

Interfaces:

Table 43 – T02/SD_A_Sk input and output signals

Input(s)	Output(s)
T02_AI_CK T02_AI_TSF T02/SD_A_Sk_MI_CSid	SD_CI_CK SD_CI_SSF SD_CI_CS SD_CI_QL

Processes:

This function adapts the 64 kHz T02 timing information from an external reference to equipment-specific timing characteristic information. This function regenerates the received clock signal and supplies the recovered timing signal to the synchronization distribution layer.

Regeneration: The function shall output a valid clock signal when any combination of the following signal conditions exists at the input:

– an input electrical amplitude level with any value in the range specified by [ITU-T G.703];

– jitter modulation applied to the input signal with value *TBD*;

– the input signal frequency has any value in the range 64 kHz ± *TBD* ppm.

NOTE – The frequency and jitter/wander tolerance is further constrained by the requirements of the client (SD) layer.

SSM support: CI_QL shall be forced to the QL-UNK.

Clock source identifier: The function shall assign MI_CSid to CI_CS.

Defects: None.

Consequent actions:

aSSF ← AI_TSF

Defect correlations: None

Performance monitoring: None.

8.8 T21 layer adaptation functions

8.8.1 T21 to SD adaptation source (T21/SD_A_So)

Symbol:

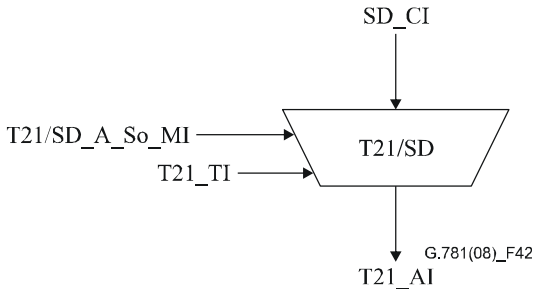


Figure 42 – T21/SD_A_So symbol

Interfaces:

Table 44 – T21/SD_A_So input and output signals

Input(s)	Output(s)
SD_CI_QL SD_CI_CS SD_CI_SSF T21_TI_CK T21/SD_A_So_MI_QLminimum T21/SD_A_So_MI_QLmode	T21_AI_CK T21_AI_SQLCH

Processes:

This function converts the CI_QL and CI_SSF information into an SQLCH control signal.

QLmode: In the case where the function operates in QL-disabled mode (MI_QLmode = dis), AI_SQLCH shall be activated if CI_SSF is true. In the case of QL-enabled mode, AI_SQLCH shall be activated if CI_SSF is true or CI_QL is below MI_QLminimum.

Defects: None.

Consequent actions:

```
if (MI_QLmode == dis)
then    if (CI_SSF == true)
        then   AI_SQLCH = true
        else   AI_SQLCH = false
        fi
else    if (CI_SSF == true) or (CI_QL < MI_QLminimum)
        then   AI_SQLCH = true
        else   AI_SQLCH = false
        fi
fi
```

Defect correlations: None.

Performance monitoring: None.

8.8.2 T21 to SD adaptation sink (T21/SD_A_Sk)

For further study.

8.9 ETH layer adaptation functions

8.9.1 ETH to SD adaptation source (ETH/SD_A_So)

Symbol:

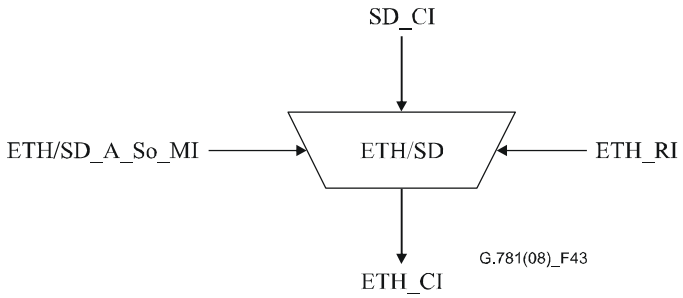


Figure 43 – ETH/SD_A_So symbol

Interfaces:

Table 45 – ETH/SD_A_So input and output signals

Input(s)	Output(s)
SD_CI_QL SD_CI_CS ETH_RI_CS ETH/SD_A_So_MI_SSMdis ETH/SD_A_So_MI_QLmode ETH/SD_A_So_MI_OptII_QLGEN ETH/SD_A_So_MI_OptII_QLRES	ETH_CI_ESMC

Processes:

This function converts the CI_QL into the 4-bit SSM code, as defined in [ITU-T G.707], and insert it in the SSM field in the CI_ESMC. The ESMC carries event and information messages, as defined in [ITU-T G.8264].

The SSM message that shall be generated and inserted depends on the applied quality level indication that is input to the adaptation source function (CI_QL). Tables 27 to 29 present the relationship between the existing set of QLs and the output SSM.

QLmode: This function operates in the QL-enabled mode.

Timing loop prevention: If RI_CS equals CI_CS, the transmitted SSM shall be forced to the "1111" pattern to prevent a timing loop condition to occur (see clause 5.13).

SSM usage: The function supports the capability to prevent synchronization quality information to pass the interface (see clause 5.5.2). In the case where MI_SSMdis is true, no ESMC is activated, i.e., neither event nor information ESMC PDU messages are generated.

SSM: The SSM field in the SSM PDU shall transport the 4-bit SSM code.

The ESSM message channel, specified in [ITU-T G.8264], defines 2 types of messages, event and information ones. The generation of an event-based message is triggered by a change of the SSM

code, SD_CI_QL value, within the delay times (T_{HM}, T_{NSM}, T_{SM}) specified in clause 5.14. The information messages are generated with a periodicity of one second.

Defects: None.

Consequent actions:

```
if (MI_SSMdis == true)
then no message is generated
else if (MI_QLmode == dis)
    then S1[5-8] = 1111
    elseif (RI_CS == CI_CS)
        then SSM = 1111
        else  SSM = SSM[CI_QL]
        fi
    fi
fi
```

Defect correlations: None.

Performance monitoring: None.

8.9.2 ETH to SD adaptation sink (ETH/SD_A_Sk)

Symbol:

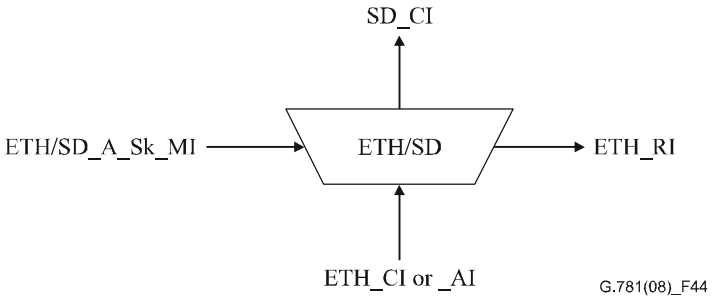


Figure 44 – ETH/SD_A_Sk symbol

Interfaces:

Table 46 – ETH/SD_A_Sk input and output signals

Input(s)	Output(s)
ETH_CI_ESMC ETH_CI_CK ETH_CI_SSF ETH_AI_TSF ETH/SD_A_Sk_MI_SSMsupp ETH/SD_A_Sk_MI_CSid ETH/SD_A_Sk_MI_QLmode	SD_CI_CK SD_CI_SSF SD_CI_CS SD_CI_QL ETH_RI_CS

Processes:

This function extracts and accepts the 4-bit synchronization status messages (SSMs) that are transmitted in the SSM event-based and information messages carried by the ESMC, as defined in [ITU-T G.8264].

SSM: For all options, the recovered SSM bits are accepted immediately if no CI_SSF or AI_TSF condition applies.

The accepted code shall be converted to a quality level QL[SSM] as specified in Table 8 (option I), Table 10 (option II), Table 12 (option III) and output via CI_QL. The SD_CI_QL output is generated with the SSM extracted from both event-based and information messages.

QLmode: In the case where the function operates in QL-disabled mode (MI_QLmode = dis), the received SSM code shall be ignored and the CI_QL shall be forced to the QL-NSUPP.

SSM support: In the case where MI_SSMsupp is false, the received SSM extracted from the CI_ESMC should not be interpreted as a valid QL value and the CI_QL shall be forced to the QL-NSUPP.

Clock source identifier: The function shall insert the clock source identifier received via MI_CSid into CI_CS and RI_CS to support timing loop prevention as described in clause 5.13.

Defects:

dLOESMC: If no valid ESMC PDU is received during 5 seconds, a loss of ESMC (LOESMC) defect is detected. The LOESMC defect is cleared on receipt of the first ESMC PDU.

Consequent actions:

aSSF ← CI_SSF or AI_TSF or dLOESMC

if (MI_QLmode == disabled) or (MI_SSMsupp == false)

then CI_QL = QL-NSUPP

else CI_QL = QL[SSM]

fi

Defect correlations:

cLOESMC ← dLOESMC and (not CI_SSF)

Performance monitoring: None.

9 Equipment clock to transport layers clock adaptation functions

9.1 STM-N layer

9.1.1 STM-N layer clock adaptation source (MSn-LC_A_So)

Symbol:

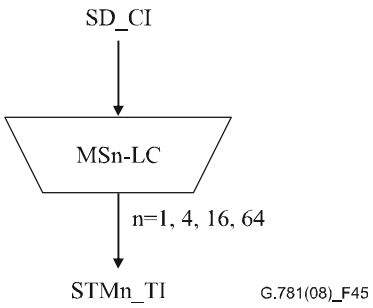


Figure 45 – MSn-LC_A_So symbol

Interfaces:

Table 47 – MSn-LC_A_So input and output signals

Input(s)	Output(s)
SD_CI_CK	STMn_TI_CK STMn_TI_FS

Processes:

This function performs the STM-N clock and frame start signal generation locked to the network element clock signal SD_CI_CK, to time the adaptation source functions in this layer (and its server layers).

Clock generation: The function shall generate the clock (bit) reference signal STMn_TI_CK for the STM-N signal. The STMn_TI_CK frequency shall be 155 520 kHz (N=1), 622 080 kHz (N=4), 2 488 320 kHz (N=16), 9 953 280 kHz (N=64) locked to the input signal SD_CI_CK.

Jitter limiter: The function shall process the signal such that, in the absence of input jitter at the synchronization interface, the intrinsic jitter at the STM-N output interface shall be as specified in [ITU-T G.813] or [ITU-T G.8262] for optical interfaces, and [ITU-T G.783] for STM-1 electrical interface.

Frame start signal generation: The function shall generate the frame start reference signal STMn_TI_FS for the STM-N signal. The STMn_TI_FS signal shall be active once per 19 440 (N=1), 77 760 (N=4), 311 040 (N=16), 1 244 160 (N=64) clock cycles.

Defects: None.

Consequent actions: None.

Defect correlations: None.

Performance monitoring: None.

9.2 VC layers

9.2.1 VC-n layer clock adaptation source (Sn-LC_A_So)

Symbol:

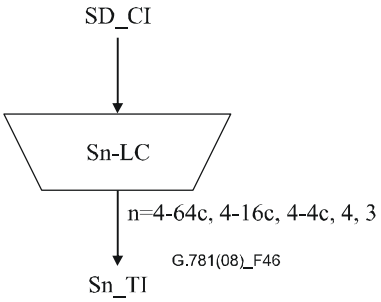


Figure 46 – Sn-LC_A_So symbol

Interfaces:

Table 48 – Sn-LC_A_So input and output signals

Input(s)	Output(s)
SD_CI_CK	Sn_TI_CK Sn_TI_FS Sn_TI_MFS

Processes:

This function performs the VC-n (n=4-64c, 4-16c, 4-4c, 4, 3) clock and frame start signal generation locked to the network element clock signal SD_CI_CK to time the adaptation source and connection functions in this layer.

Clock generation: The function shall generate the clock (bit) reference signal Sn_TI_CK for the VC-n signal. The Sn_TI_CK frequency shall be 9 621 504 kHz (n=4-64c), 2 405 376 kHz (n=4-16c), 601 344 kHz (n=4-4c), 150 336 kHz (n=4), 48 960 kHz (n=3), locked to the input signal SD_CI_CK.

Jitter limiter: For further study.

Frame start signal generation: The function shall generate the frame start reference signal Sn_TI_FS for the VC-n signal. The Sn_TI_FS signal shall be active once per 1 202 688 (n=4-64c), 300 672 (n=4-16c), 75 168 (n=4-4c), 18 792 (n=4), 6120 (n=3) clock cycles, and the multiframe reference Sn_TI_MFS shall be active once every 4 frames.

Defects: None.

Consequent actions: None.

Defect correlations: None.

Performance monitoring: None.

9.2.2 VC-m layer clock adaptation source (Sm-LC_A_So)

Symbol:

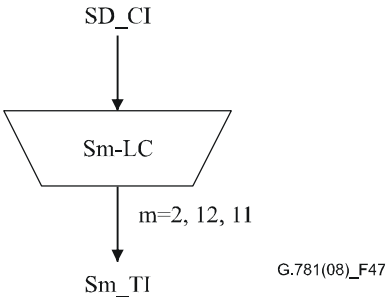


Figure 47 – Sm-LC_A_So symbol

Interfaces:

Table 49 – Sm-LC_A_So input and output signals

Input(s)	Output(s)
SD_CI_CK	Sm_TI_CK Sm_TI_FS

Processes:

This function performs the VC-m (m=2, 12, 11) clock and frame start signal generation locked to the network element clock signal SD_CI_CK to time the adaptation source and connection functions in this layer.

Clock generation: The function shall generate the clock (bit) reference signal Sm_TI_CK for the VC-m signal. The Sm_TI_CK frequency shall be 6848 kHz (m=2), 2240 kHz (m=12), 1664 kHz (m=11), locked to the input signal SD_CI_CK.

Jitter limiter: For further study.

Frame start signal generation: The function shall generate the frame start reference signal Sm_TI_FS for the VC-m signal. The Sm_TI_FS signal shall be active once per 856 (m=2), 280 (m=12), 208 (m=11) clock cycles.

Defects: None.

Consequent actions: None.

Defect correlations: None.

Performance monitoring: None.

9.3 Pxx layers

9.3.1 Pqs layer clock adaptation source (Pqs-LC_A_So)

Symbol:

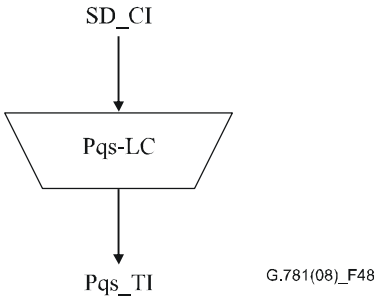


Figure 48 – Pqs-LC_A_So symbol

Interfaces:

Table 50 – Pqs-LC_A_So input and output signals

Input(s)	Output(s)
SD_CI_CK	Pqs_TI_CK Pqs_TI_FS Pqs_TI_MFS

Processes:

This function performs the Pqs (q=4, 31) clock and frame start signal generation locked to the network element clock signal SD_CI_CK to time the adaptation source functions in this layer.

Clock generation: The function shall generate the clock (bit) reference signal Pqs_TI_CK for the Pqs signal. The Pqs_TI_CK frequency shall be 139 264 kHz (q=4), 34 368 kHz (q=31) locked to the input signal SD_CI_CK.

Jitter limiter: For further study.

Frame start signal generation: The function shall generate the frame start reference signal Pqs_TI_FS for the Pqs signal. The Pqs_TI_FS signal shall be active once per 17 408 (q=4), 4296 (q=31) clock cycles. Pqs_TI_MFS shall be active once every 4 frames.

Defects: None.

Consequent actions: None.

Defect correlations: None.

Performance monitoring: None.

9.3.2 P12s layer clock adaptation source (P12s-LC_A_So)

Symbol:

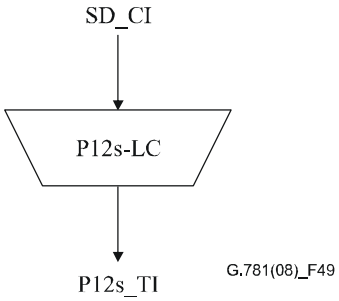


Figure 49 – P12s-LC_A_So symbol

Interfaces:

Table 51 – P12s-LC_A_So input and output signals

Input(s)	Output(s)
SD_CI_CK	P12s_TI_CK P12s_TI_FS P12s_TI_MFS

Processes:

This function performs the P12s clock and frame start signal generation locked to the clock signal SD_CI_CK to time the adaptation source functions in this layer.

Clock generation: The function shall generate the clock (bit) reference signal P12s_TI_CK for the P12s signal. The P12s_TI_CK frequency shall be 2048 kHz locked to the input signal SD_CI_CK.

NOTE – If an SD_CI_SSF is present at the input of the function, it is also present at the input of P12s/SD and an AIS is generated by P12_TT.

Jitter limiter: The function shall process the signal such that, in the absence input jitter at the sychronization interface, the intrinsic jitter at the E12 output interface is compatible with [ITU-T G.813] or [ITU-T G.8262].

Frame start signal generation: The function shall generate the frame start reference signal P12s_TI_FS for the P12s signal. The P12s_TI_FS signal shall be active once per 256 clock cycles and P12s_TI_MFS once every 16 frames.

Defects: None.

Consequent actions: None.

Defect correlations: None.

Performance monitoring: None.

9.3.3 P11s layer clock adaptation source (P11s-LC_A_So)

For further study.

9.4 T12 layer

9.4.1 T12 layer clock adaptation source (T12-LC_A_So)

Symbol:

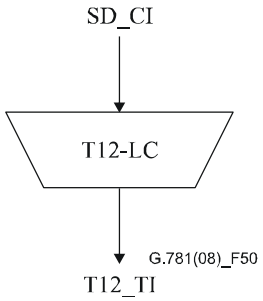


Figure 50 – T12-LC_A_So symbol

Interfaces:

Table 52 – T12-LC_A_So input and output signals

Input(s)	Output(s)
SD_CI_CK	T12_TI_CK

Processes:

This function performs the T12 clock signal generation locked to the clock signal SD_CI_CK to time the adaptation source functions T12/SD_A_So.

Clock generation: The function shall generate the clock reference signal T12_TI_CK for the 2048 kHz signal. The T12_TI_CK frequency shall be 2048 kHz locked to the input signal SD_CI_CK.

NOTE – If an SD_CI_SSF is present at the input of the function, it is also present at the input of T12s/SD and a squelch action is activated.

Jitter limiter: The function shall process the signal such that, in the absence of input jitter at the synchronization interface, the intrinsic jitter at the 2048 kHz output interface is compatible with [ITU-T G.813] or [ITU-T G.8262].

Defects: None.

Consequent actions: None.

Defect correlations: None.

Performance monitoring: None.

9.5 T01 layer

9.5.1 T01 layer clock adaptation source (T01-LC_A_So)

For further study.

9.6 T02 layer

9.6.1 T02 layer clock adaptation source (T02-LC_A_So)

For further study.

9.7 T21 layer

9.7.1 T21 layer clock adaptation source (T21-LC_A_So)

Symbol:

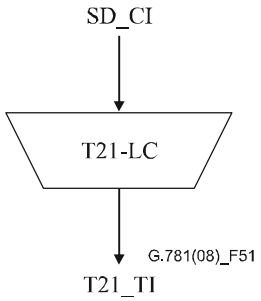


Figure 51 – T21-LC_A_So symbol

Interfaces:

Table 53 – T21-LC_A_So input and output signals

Input(s)	Output(s)
SD_CI_CK	T21_TI_CK

Processes:

This function performs the T21 clock signal generation locked to the clock signal SD_CI_CK to time the adaptation source functions T21/SD_A_So.

Clock generation: The function shall generate the clock reference signal T21_TI_CK for the 6312 kHz signal. The T21_TI_CK frequency shall be 6312 kHz locked to the input signal SD_CI_CK.

NOTE – If an SD_CI_SSF is present at the input of the function, it is also present at the input of T21/SD and a squelch action is activated.

Jitter limiter: For further study.

Defects: None.

Consequent actions: None.

Defect correlations: None.

Performance monitoring: None.

9.8 ETYn layer

9.8.1 ETYn layer clock adaptation source (ETYn-LC_A_So)

Symbol:

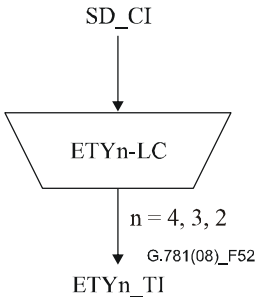


Figure 52 – ETYn-LC_A_So symbol

Interfaces:

Table 54 – ETY-LC_A_So input and output signals

Input(s)	Output(s)
SD_CI_CK	ETYn_TI_CK

Processes:

This function performs the ETYn (n=4, 3, 2) clock signal generation locked to the network element clock signal SD_CI_CK, to time the adaptation source functions in this layer.

Clock generation: The function shall generate the clock (bit) reference signal ETYn_TI_CK for the ETYn signal. The ETYn_TI_CK frequency shall be 10 000 000 kHz (k=4), 1 000 000 kHz (k=3), 100 000 kHz (m=2) locked to the input signal SD_CI_CK.

NOTE – The ETY_TI_CK signal provides the reference clock to the ETY/ETH adaptation source function. Several processes within this adaptation source function operate on this clock. The line encoding process in this adaptation source function generates the line clock using the ETY_CI_CK as input signal.

Jitter limiter: For further study.

Defects: None.

Consequent actions: None.

Defect correlations: None.

Performance monitoring: None.

10 T12 section layer functions

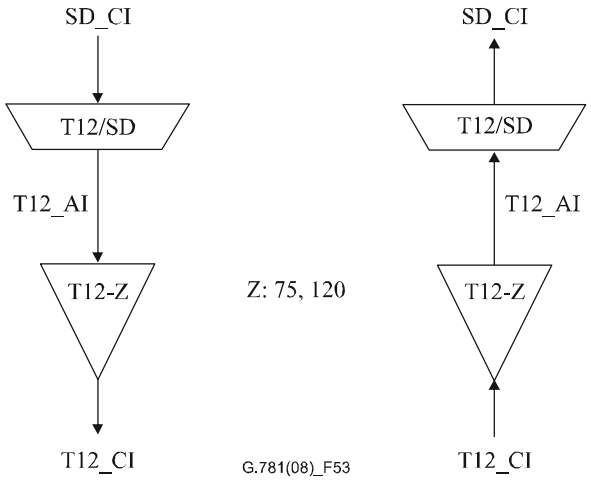


Figure 53 – T12 section atomic functions

T12 layer CP

The characteristic information T12_CI of the intra-station electrical layer CP is an electrical 2048 kHz signal of defined amplitude, frequency and pulse shape specified by clause 13 of [ITU-T G.703].

T12 layer AP

The information passing across the T12/SD AP is a 2048 kHz synchronization signal.

10.1 T12 connection function T12_C

Not applicable.

10.2 T12 trail termination functions

10.2.1 T12 trail termination source (T12-Z_TT_So)

NOTE – Z (Ω) will be one value out of the set: {75, 120} (Ω).

Symbol:

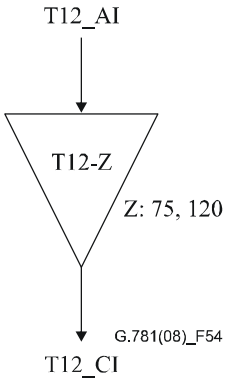


Figure 54 – T12-Z_TT_So symbol

Interfaces:

Table 55 – T12-Z_TT_So input and output signals

Input(s)	Output(s)
T12_AI_CK T12_AI_SQLCH	T12_CI_CK

Processes:

This function generates the electrical 2048 kHz signal used for transmission of synchronization signals to an external equipment on a plesiochronous intra-station section specified by clause 13 of [ITU-T G.703].

Pulse shape: The function shall meet the requirement specified by [ITU-T G.703].

Maximum peak voltage: The function shall meet the requirement specified by [ITU-T G.703].

Minimum peak voltage: The function shall meet the requirement specified by [ITU-T G.703].

Pair in each direction: The function shall meet the requirement specified by [ITU-T G.703].

Defects: None.

Consequent actions:

On activation of T12_AI_SQLCH, the function shall shut down the output within 250 µs; on clearing of T12_AI_SQLCH, the function shall output a normal signal within 250 µs.

Defect correlations: None.

Performance monitoring: None.

10.2.2 T12 trail termination sink (T12-Z_TT_Sk)

NOTE 1 – Z (Ω) will be one value out of the set: {75, 120} (Ω).

Symbol:

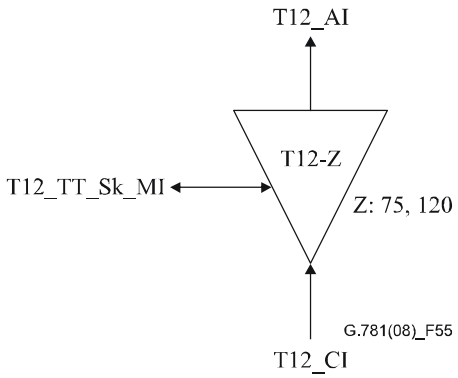


Figure 55 – T12-Z_TT_Sk symbol

Interfaces:

Table 56 – T12-Z_TT_Sk input and output signals

Input(s)	Output(s)
T12_CI_CK T12_TT_Sk_MI_PortMode	T12_AI_CK T12_AI_TSF T12_TT_Sk_MI_cLOS

Processes:

This function recovers the electrical 2048 kHz signal used for transmission of synchronization signals from an external equipment on a plesiochronous intra-station section specified by clause 13 of [ITU-T G.703].

Input return loss: The function shall meet the requirement specified by [ITU-T G.703].

Port mode: The function shall have a port mode as specified in clause 6.1 of [ITU-T G.806].

NOTE 2 – The AUTO state of the port mode process is optional.

Defects:

The function shall detect 2048 kHz loss of signal defect (dLOS) as defined for the 2048 kbit/s dLOS specification in [ITU-T G.775].

Consequent actions:

aTSF ← dLOS

Defect correlations:

cLOS ← MON and dLOS

Performance monitoring: None.

11 T01 section layer functions

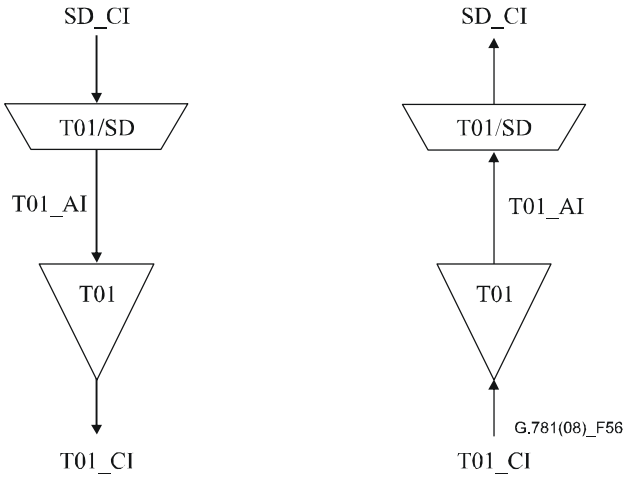


Figure 56 – T01 section atomic functions

T01 layer CP

The characteristic information T01_CI of the intra-station electrical layer CP is an electrical 64 kHz composite timing signal of defined amplitude, frequency and pulse shape specified by clause 4.2.2 of [ITU-T G.703].

T01 layer AP

The information passing across the T01/SD AP is a 64 kHz synchronization signal.

11.1 T01 connection function T01_C

Not applicable.

11.2 T01 trail termination functions

11.2.1 T01 trail termination source (T01_TT_So)

Symbol:

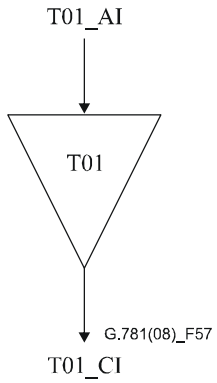


Figure 57 – T01_TT_So symbol

Interfaces:

Table 57 – T01_TT_So input and output signals

Input(s)	Output(s)
T01_AI_CK T01_AI_SQLCH	T01_CI_CK

Processes:

This function generates the electrical 64 kHz composite timing signal used for transmission of synchronization signals to an external equipment on a plesiochronous intra-station section specified by clause 4.2.2 of [ITU-T G.703].

Pulse shape: The function shall meet the requirement specified by [ITU-T G.703].

Maximum peak voltage: The function shall meet the requirement specified by [ITU-T G.703].

Minimum peak voltage: The function shall meet the requirement specified by [ITU-T G.703].

Pair in each direction: The function shall meet the requirement specified by [ITU-T G.703].

Defects: None.

Consequent actions:

On activation of T01_AI_SQLCH, the function shall shut down the output within 250 µs; on clearing of T01_AI_SQLCH, the function shall output a normal signal within 250 µs.

Defect correlations: None.

Performance monitoring: None.

11.2.2 T01 trail termination sink (T01_TT_Sk)

Symbol:

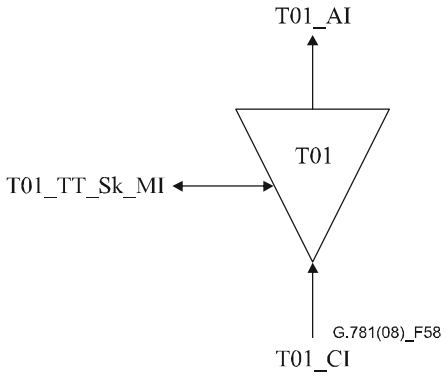


Figure 58 – T01_TT_Sk symbol

Interfaces:

Table 58 – T01_TT_Sk input and output signals

Input(s)	Output(s)
T01_CI_CK T01_TT_Sk_MI_PortMode	T01_AI_CK T01_AI_TSF T01_TT_Sk_MI_cLOS

Processes:

This function recovers the electrical 64 kHz composite timing signal used for transmission of synchronization signals from an external equipment on a plesiochronous intra-station section specified by clause 4.2.2 of [ITU-T G.703].

Port Mode: The function shall have a port mode as specified in clause 6.1 of [ITU-T G.806].

NOTE – The AUTO state of the port mode process is optional.

Defects:

The function shall detect 64 kHz loss of signal defect (dLOS) as defined for the 64 kbit/s dLOS specification in [ITU-T G.775].

Consequent actions:

aTSF ← dLOS

Defect correlations:

cLOS ← MON and dLOS

Performance monitoring: None.

12 T02 section layer functions

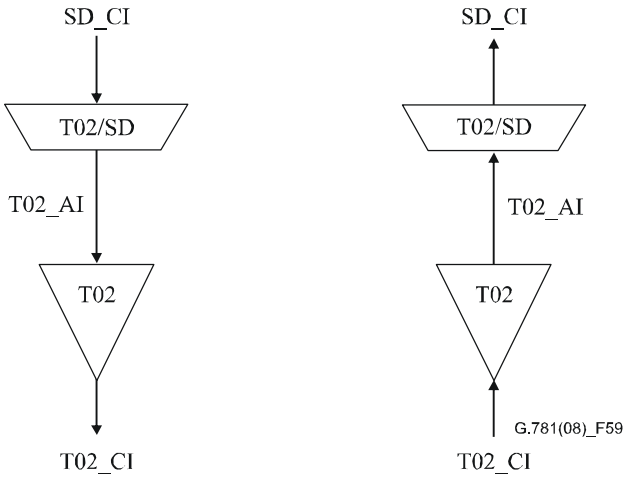


Figure 59 – T02 section atomic functions

T02 layer CP

The characteristic information T02_CI of the intra-station electrical layer CP is an electrical 64 kHz composite timing signal of defined amplitude, frequency and pulse shape specified by Appendix II of [ITU-T G.703].

T02 layer AP

The information passing across the T02/SD AP is a 64 kHz synchronization signal.

12.1 T02 connection function T02_C

Not applicable.

12.2 T02 trail termination functions

12.2.1 T02 trail termination source (T02_TT_So)

For further study.

12.2.2 T02 trail termination sink (T02_TT_Sk)

Symbol:

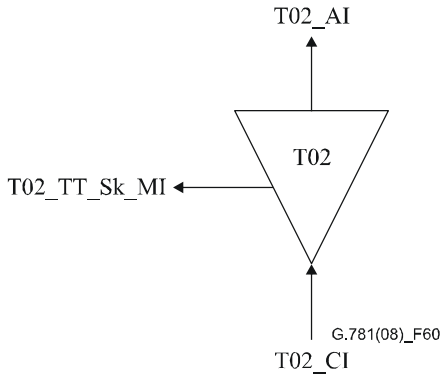


Figure 60 – T02_TT_Sk symbol

Interfaces:

Table 59 – T02_TT_Sk input and output signals

Input(s)	Output(s)
T02_CI_CK	T02_AI_CK T02_AI_TSF T02_TT_Sk_MI_cLOS

Processes:

This function recovers the electrical 64 kHz composite timing signal used for transmission of synchronization signals from an external equipment on a plesiochronous intra-station section specified by Appendix II of [ITU-T G.703].

Defects:

The function shall detect 64 kHz loss of signal defect (dLOS) as defined in Appendix II of [ITU-T G.703].

Consequent actions:

aTSF ← dLOS

Defect correlations:

cLOS ← MON and dLOS

Performance monitoring: None.

13 T21 section layer functions

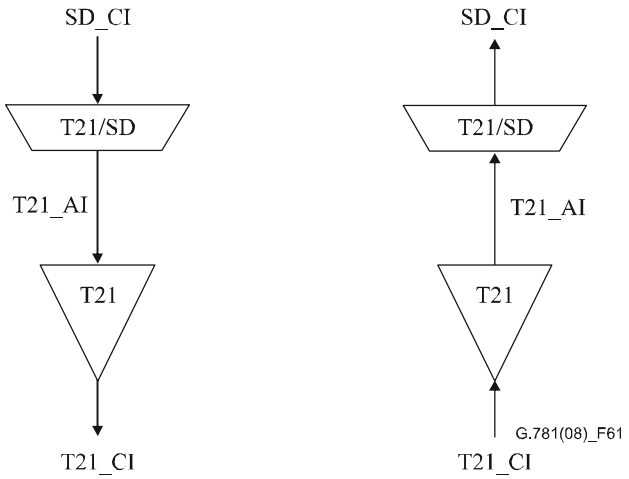


Figure 61 – T21 section atomic functions

T21 layer CP

The characteristic information T21_CI of the intra-station electrical layer CP is an electrical 6312 kHz clock signal of defined amplitude, frequency and pulse shape specified by Appendix II of [ITU-T G.703].

T21 layer AP

The information passing across the T21/SD AP is a 6312 kHz synchronization signal.

13.1 T21 connection function T21_C

Not applicable.

13.2 T21 trail termination functions

13.2.1 T21 trail termination source (T21_TT_So)

Symbol:

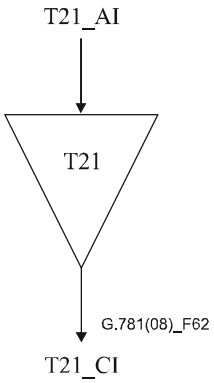


Figure 62 – T21_TT_So symbol

Interfaces:

Table 60 – T21_TT_So input and output signals

Input(s)	Output(s)
T21_AI_CK T21_AI_SQLCH	T21_CI_CK

Processes:

This function generates the electrical 6312 kHz clock signal used for transmission of synchronization signals to an external equipment on a plesiochronous intra-station section specified by Appendix II of [ITU-T G.703].

Pulse shape: The function shall meet the requirement specified by [ITU-T G.703].

Maximum peak voltage: The function shall meet the requirement specified by [ITU-T G.703].

Minimum peak voltage: The function shall meet the requirement specified by [ITU-T G.703].

Pair in each direction: The function shall meet the requirement specified by [ITU-T G.703].

Defects: None.

Consequent actions:

On activation of T21_AI_SQLCH, the function shall shut down the output; on clearing of T21_AI_SQLCH, the function shall output a normal signal.

Defect correlations: None.

Performance monitoring: None.

13.2.2 T21 trail termination sink (T21_TT_Sk)

For further study.

Annex A

Synchronization selection process

(This annex forms an integral part of this Recommendation)

This annex specifies the detailed operation of the automatic synchronization reference selection process located in the NS_C function. Refer to clause 5 for an introduction to this process.

A selection process needs the quality level (NS_CI_QL) and signal fail (NS_CI_SSF) information from each input (i.e., each SD_TT_Sk and SD/NS_A_Sk combination; the pair is henceforth called a "timing source") after it has passed through a hold-off/wait to restore process (HO/WtR).

Via the management interface it receives the priority (which includes disabling) of each timing source and its lock-out status. Switch requests (clear, manual, forced) and requests to change the mode of operation between QL-enabled and QL-disabled also come in through the management interface.

The output of the selection control process is the currently selected input ("select q") and its QL. The currently selected input is reported towards the management interface. In addition, rejection messages are sent towards the management interface. Figure A.1 shows the interfaces between the selection control process and its environment.

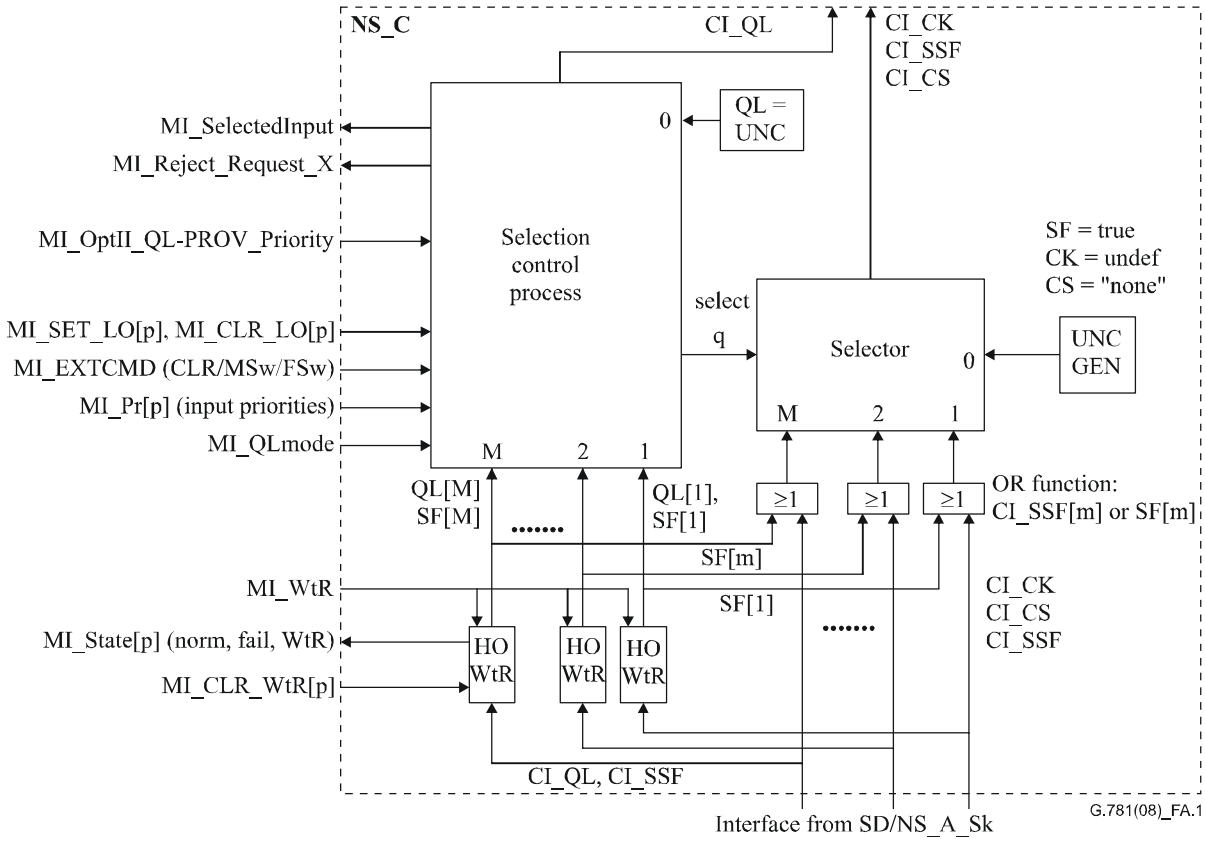


Figure A.1 – Environment of selection control process

The selector supports M inputs (1 to M) and one output. In addition, the selector has a M+1th input, the null (0) input connected to an "unconnect" signal generator process.

Unconnect signal: A signal where CI_CK is undefined, CI_SSF is true and CI_CS is "none".

In the SDL diagrams that describe the selection process, there are six states which correspond to the two modes of operation [QL-mode enabled (1) and QL-mode disabled (2)] and, within each of these modes, three "maintenance" states: no request active (A), manual switch active (B) and forced switch active (C). For each of these six states, the reaction to all possible input variations are given.

In the SDL diagrams "report q" is MI_selected input information and QL_out equals CI_CL, as defined in Figure A.1.

Table A.1 – Notational conventions and parameters used in the SDL diagrams

Parameter	Abbreviation	Values (high to low)/Explanation
Quality level [input] *) The position of QL-PROV in the QL order in option II networks may be changed via MI_OptII_QL-PROV_Priority.	QL[p]	Option I: PRC, SSU-A, SSU-B, SEC, DNU, INV, FAILED, undef(ined)
		Option II: PRS, STU, ST2, TNC, ST3E, ST3, SMC, ST4, PROV*, DUS, INV, FAILED, undef(ined)
		Option III: UNK, SEC, INV, FAILED, undef(ined)
Quality level [0]	QL[0]	UNConnected
Priority [input]	Pr[p]	1, 2, ..., K, dis(abled)
Priority [0]	Pr[0]	Undef(ined)
Signal fail [input]	SF[p]	False, true
Signal fail [0]	SF[0]	True
Lock out status [input]	LO[p]	On, off
Lock out status [0]	LO[0]	Off
Input	p	1, 2, ..., M
Selected input	q	0,1, 2, ..., M
Number of timing sources	M	
Number of different priorities	K	K = M
	:=	Assignment symbol
	==	Equality test symbol
	<=	Less or equal test symbol
NOTE – The QLs DNU and DUS are represented as DNU in the following figures.		

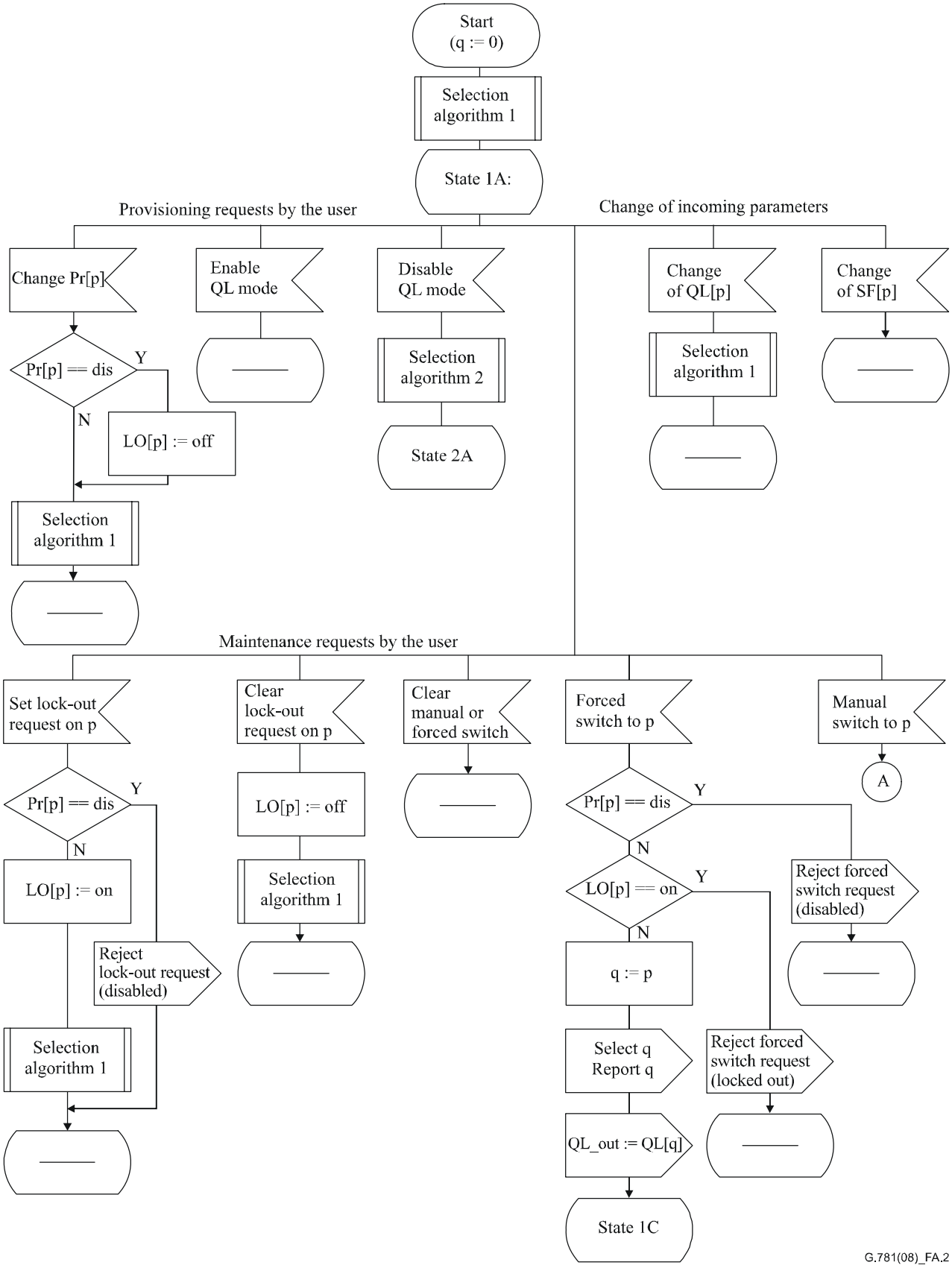


Figure A.2 – QL-enabled mode, no active switch request (state 1A)

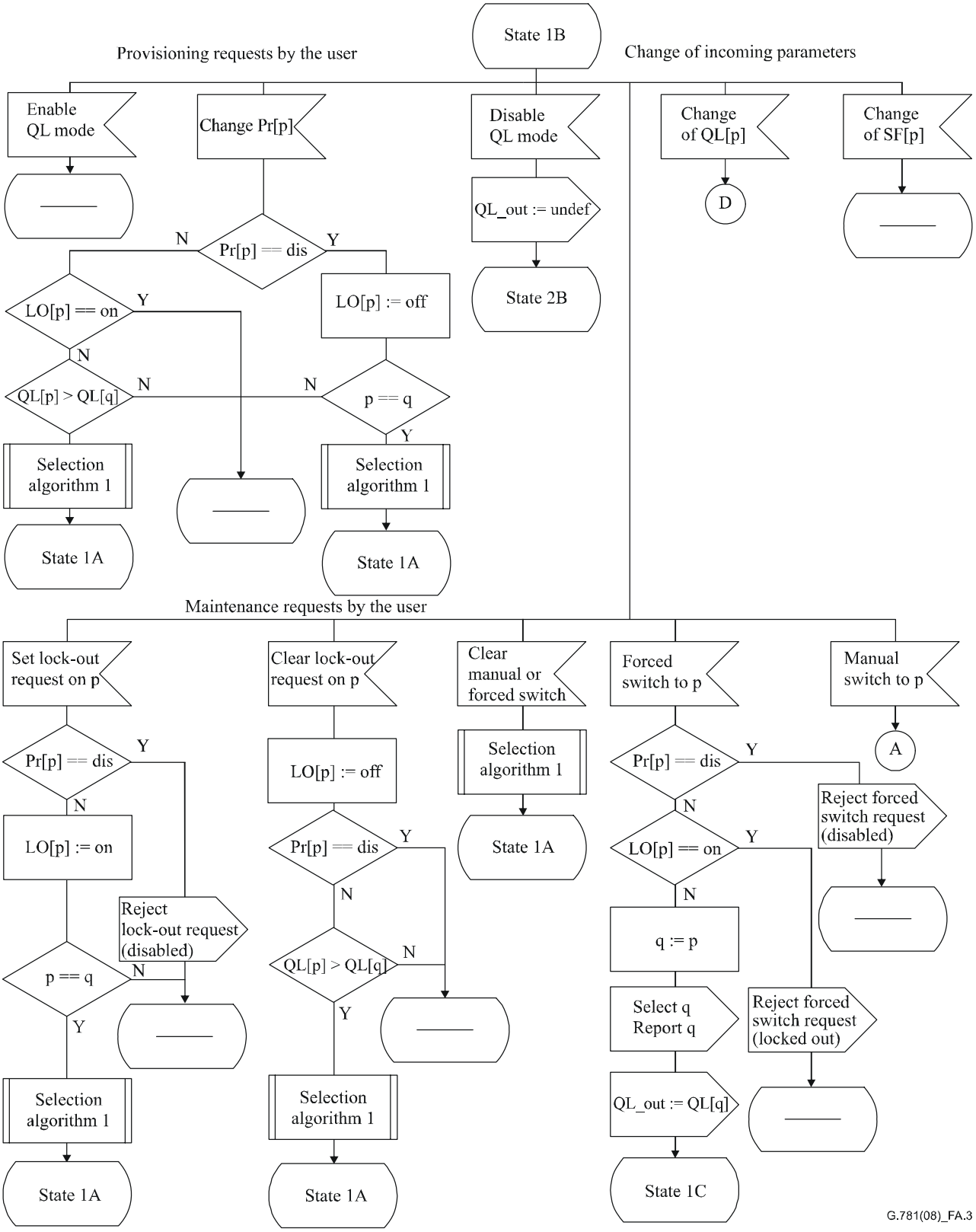


Figure A.3 – QL-enabled mode, active manual switch request (state 1B)

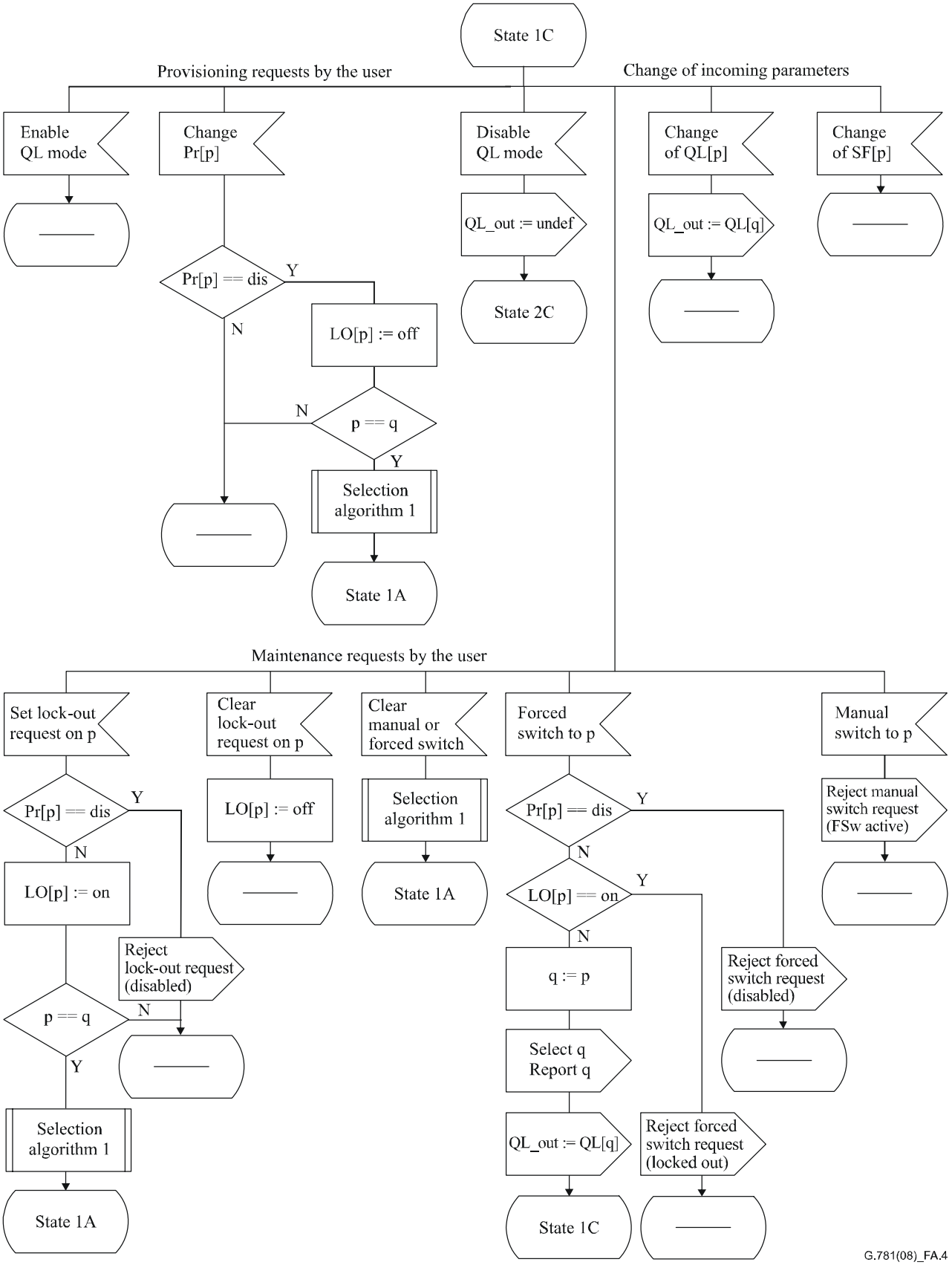


Figure A.4 – QL-enabled mode, active forced switch (state 1C)

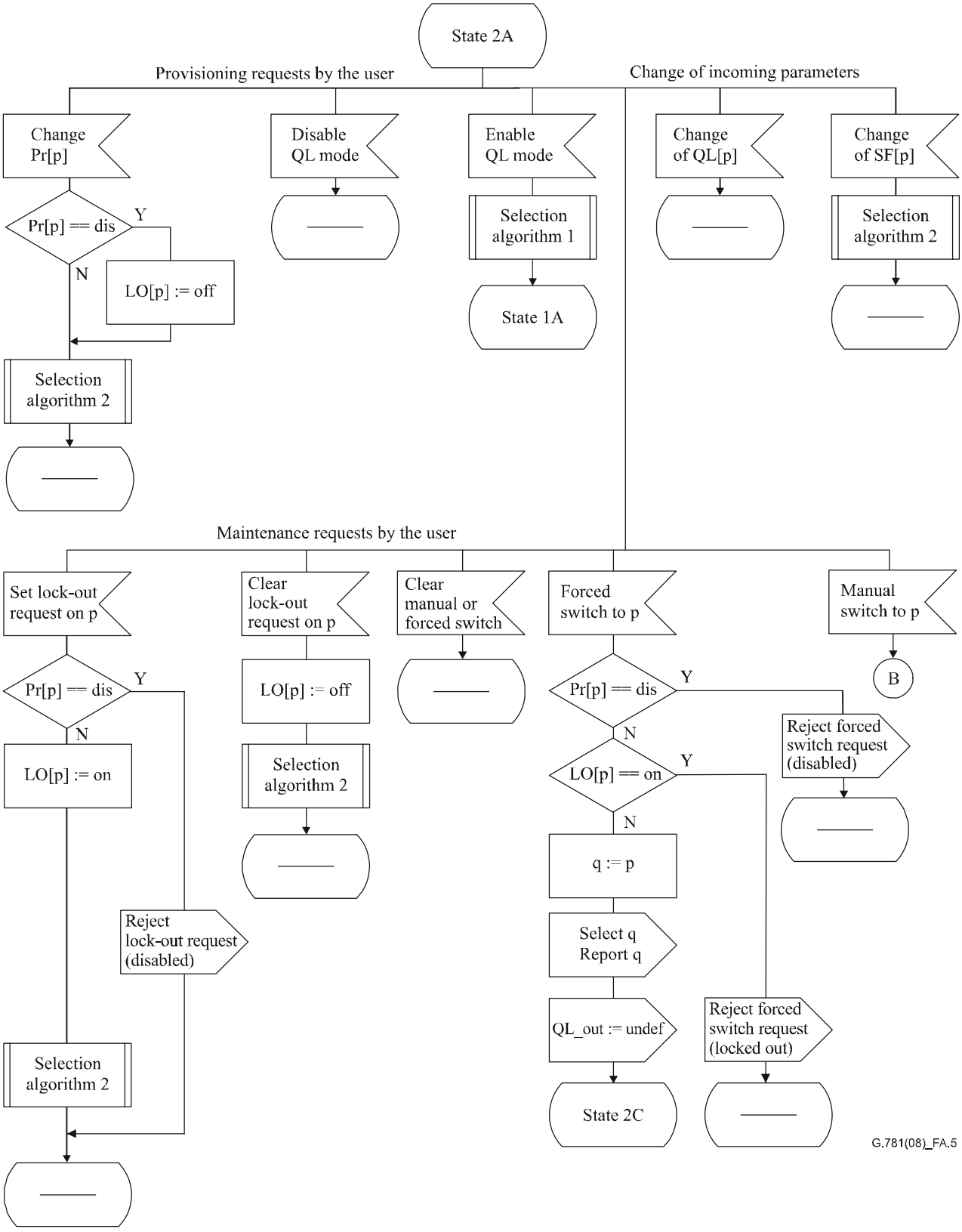


Figure A.5 – QL-disabled mode, no external switch request active (state 2A)

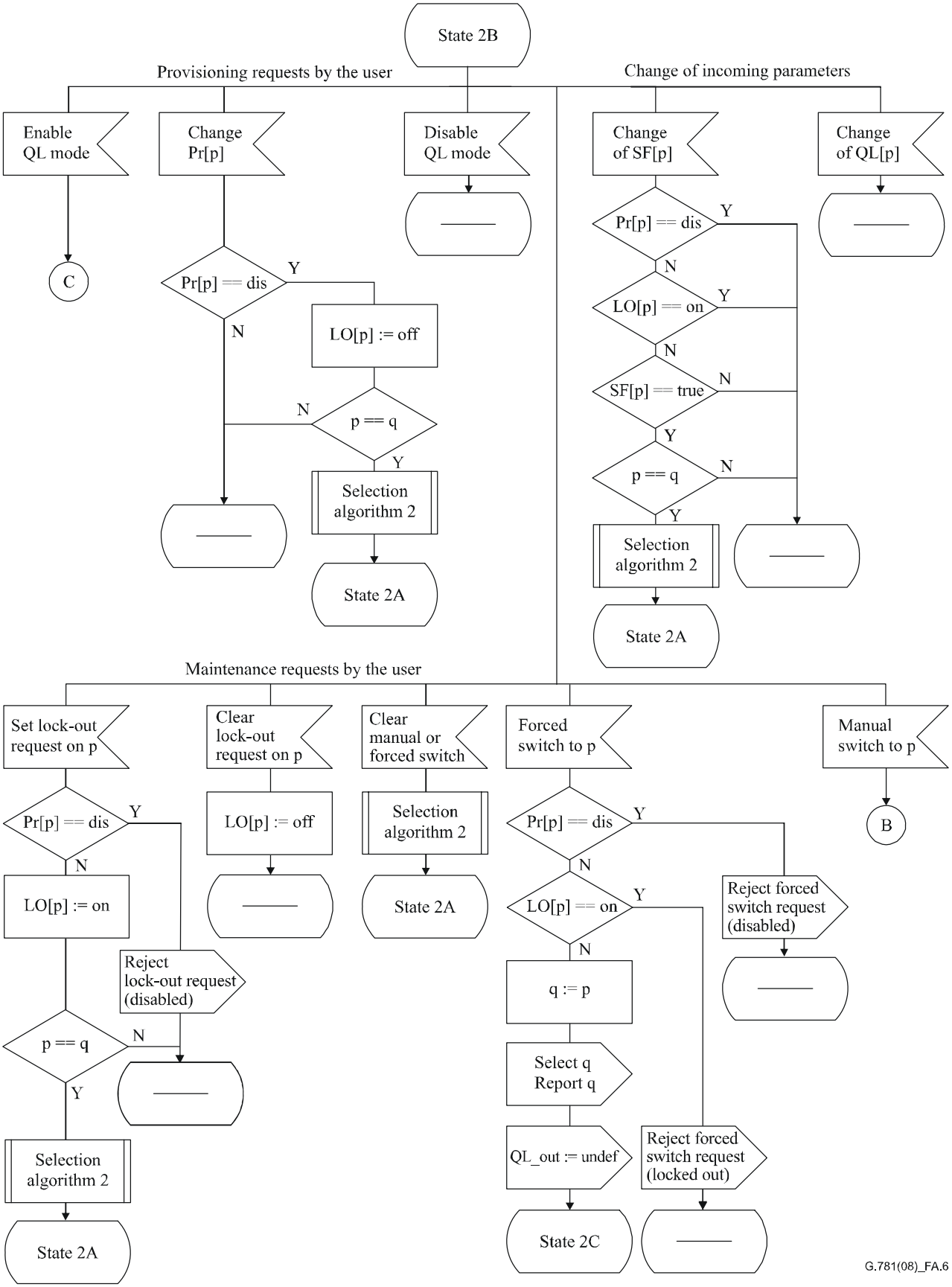


Figure A.6 – QL-disabled mode, active manual switch request (state 2B)

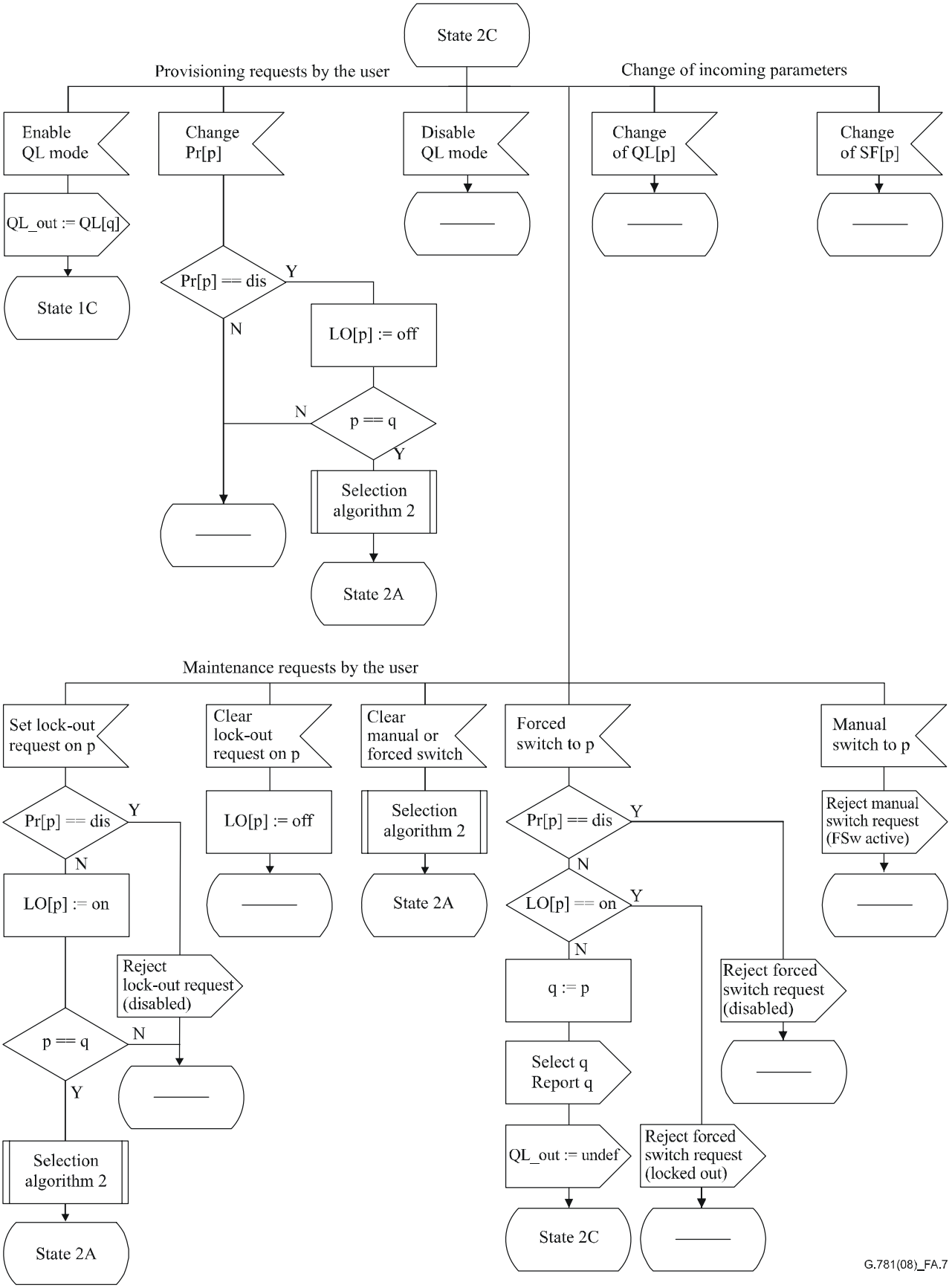


Figure A.7 – QL-disabled mode, active forced switch request (state 2C)

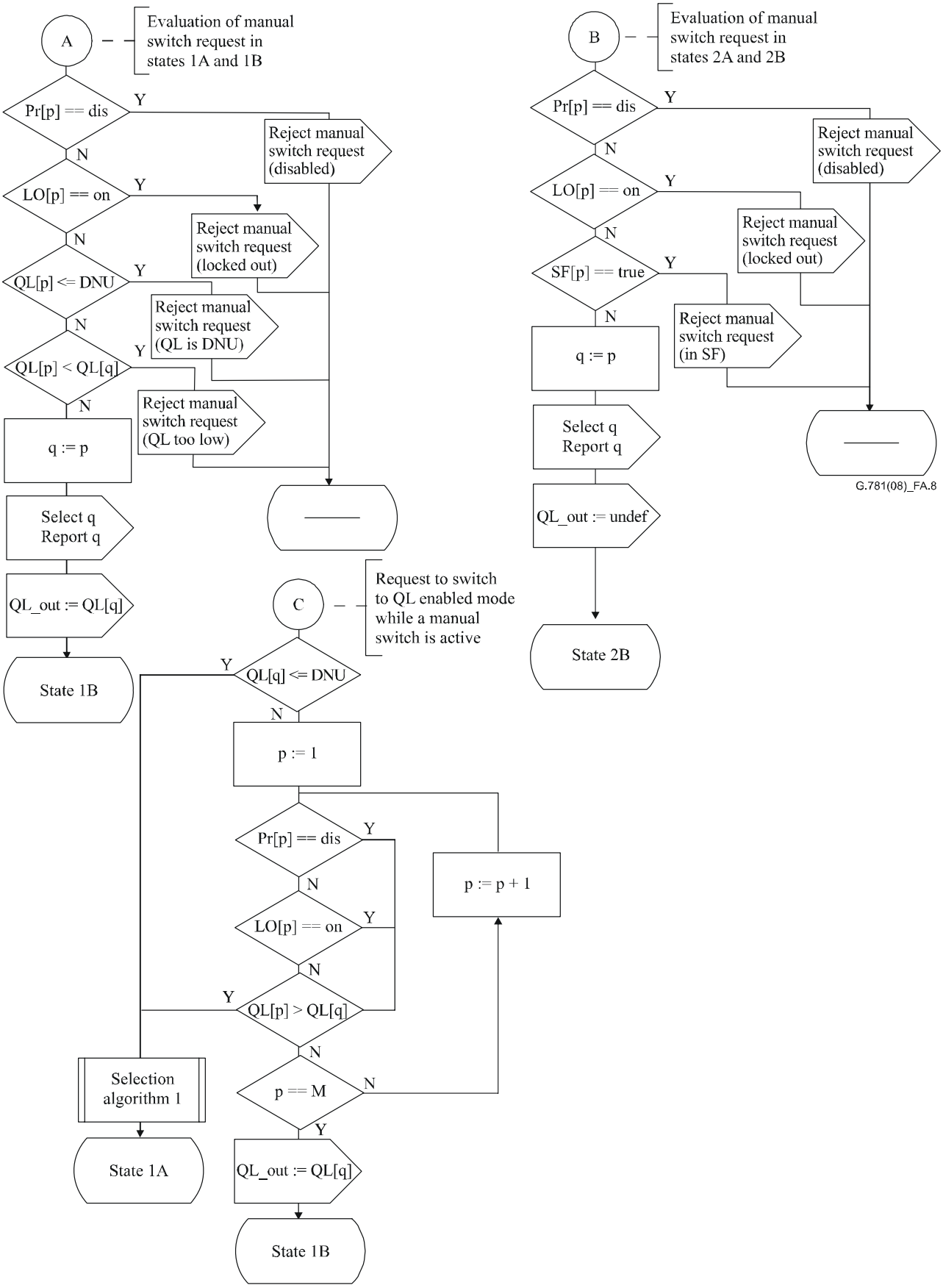


Figure A.8 – Continuations of previous states

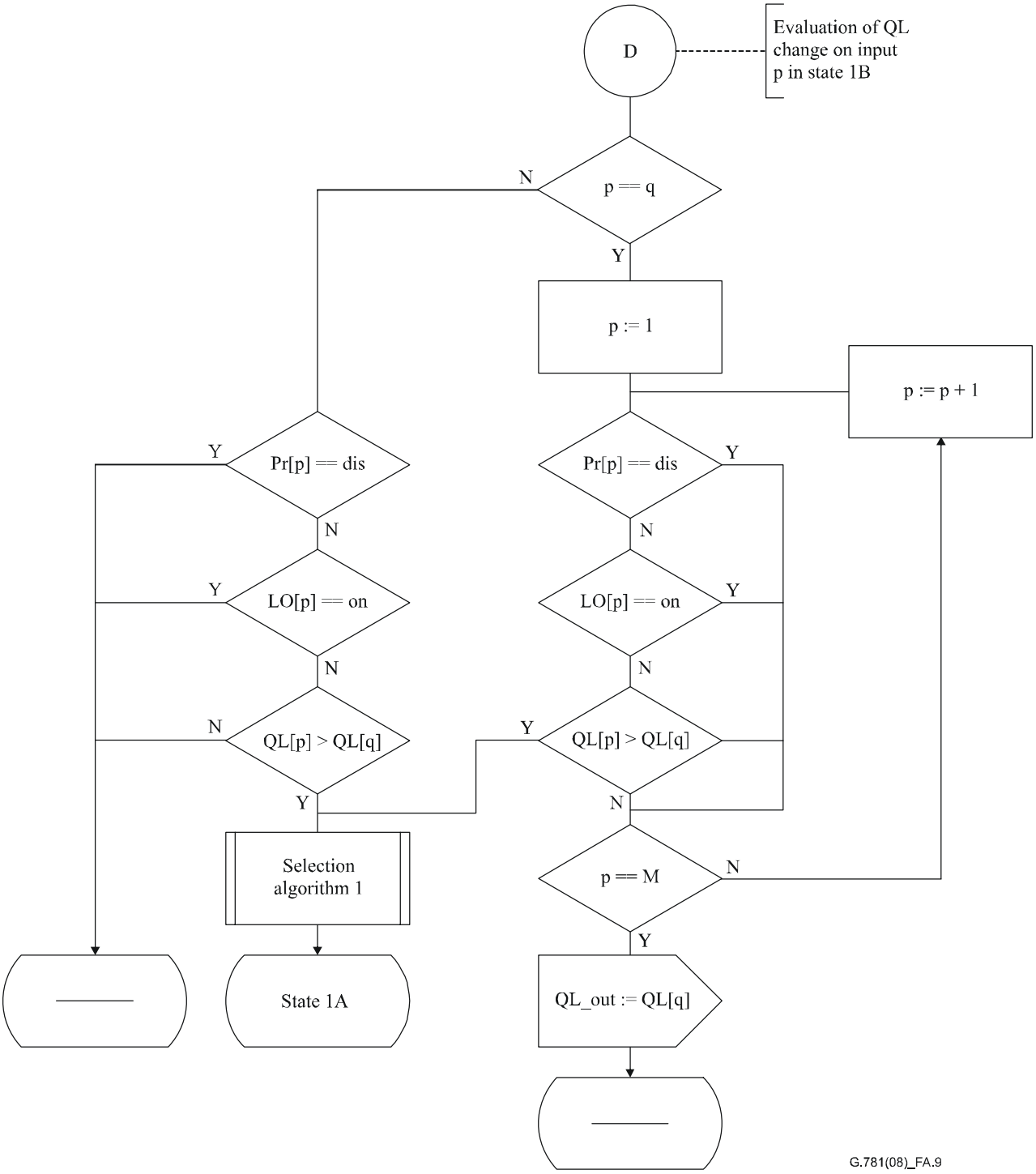


Figure A.9 – Continuations of previous states

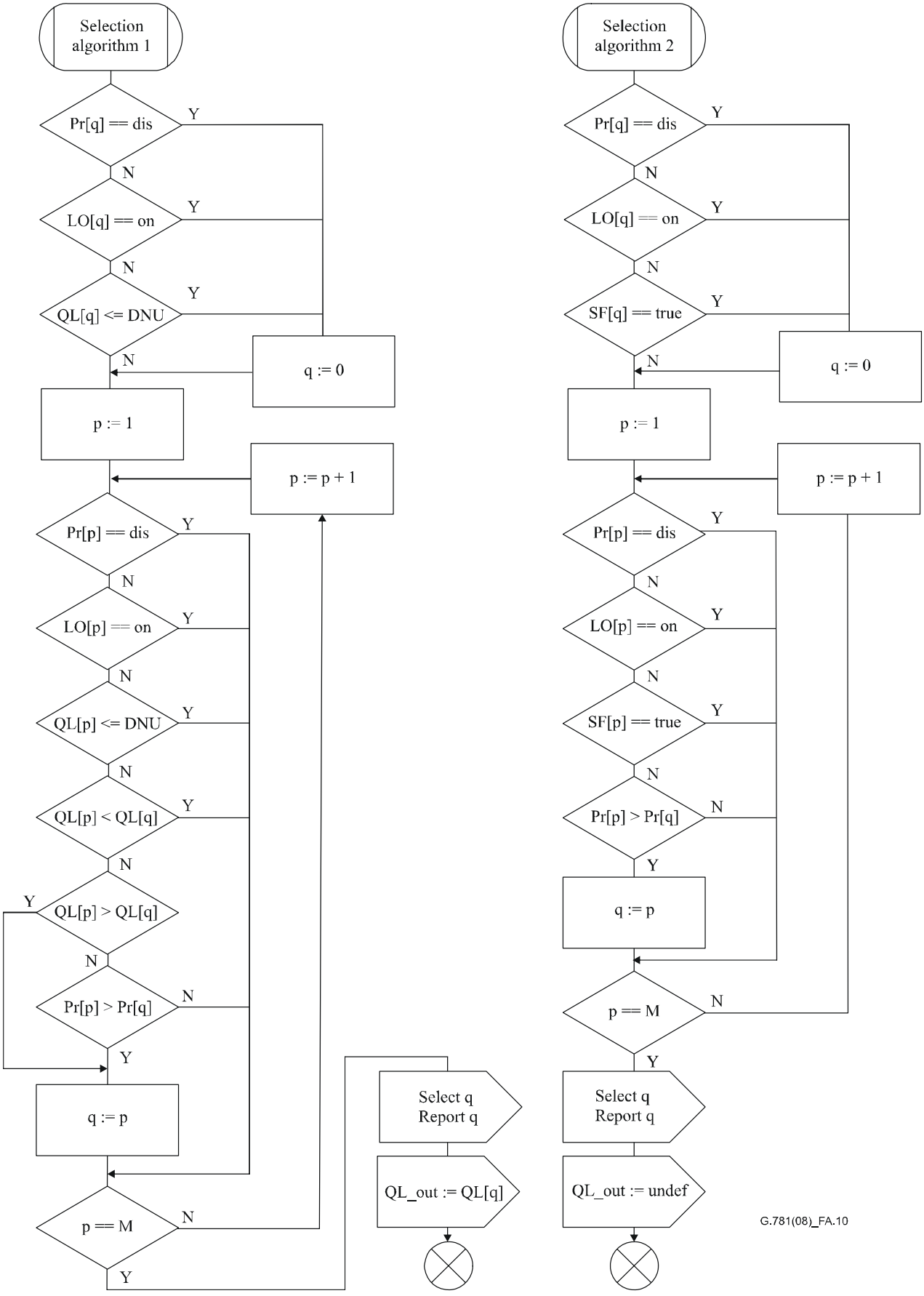


Figure A.10 – Synchronization selection algorithms for QL mode enabled (1) and QL mode disabled (2)

Appendix I

Transport layer models for synchronization information

(This appendix does not form an integral part of this Recommendation)

This appendix (Figures I.1 to I.4) shows the interfaces (sink and source), between NNI and SD_CP, that are able to transport synchronization information using the atomic functions described in [ITU-T G.783], [b-ITU-T G.705], [b-ITU-T G.8021].

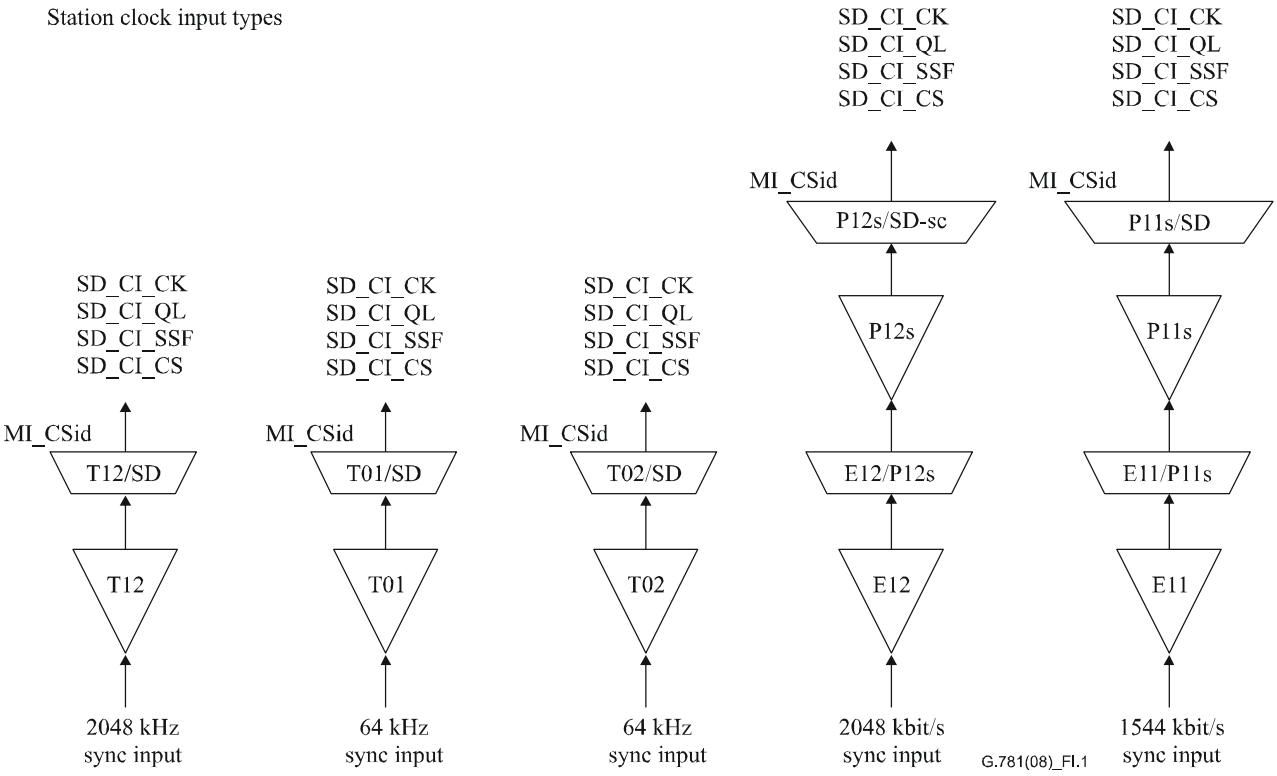


Figure I.1 – Synchronization transport port models: Station clock inputs

Station clock output types

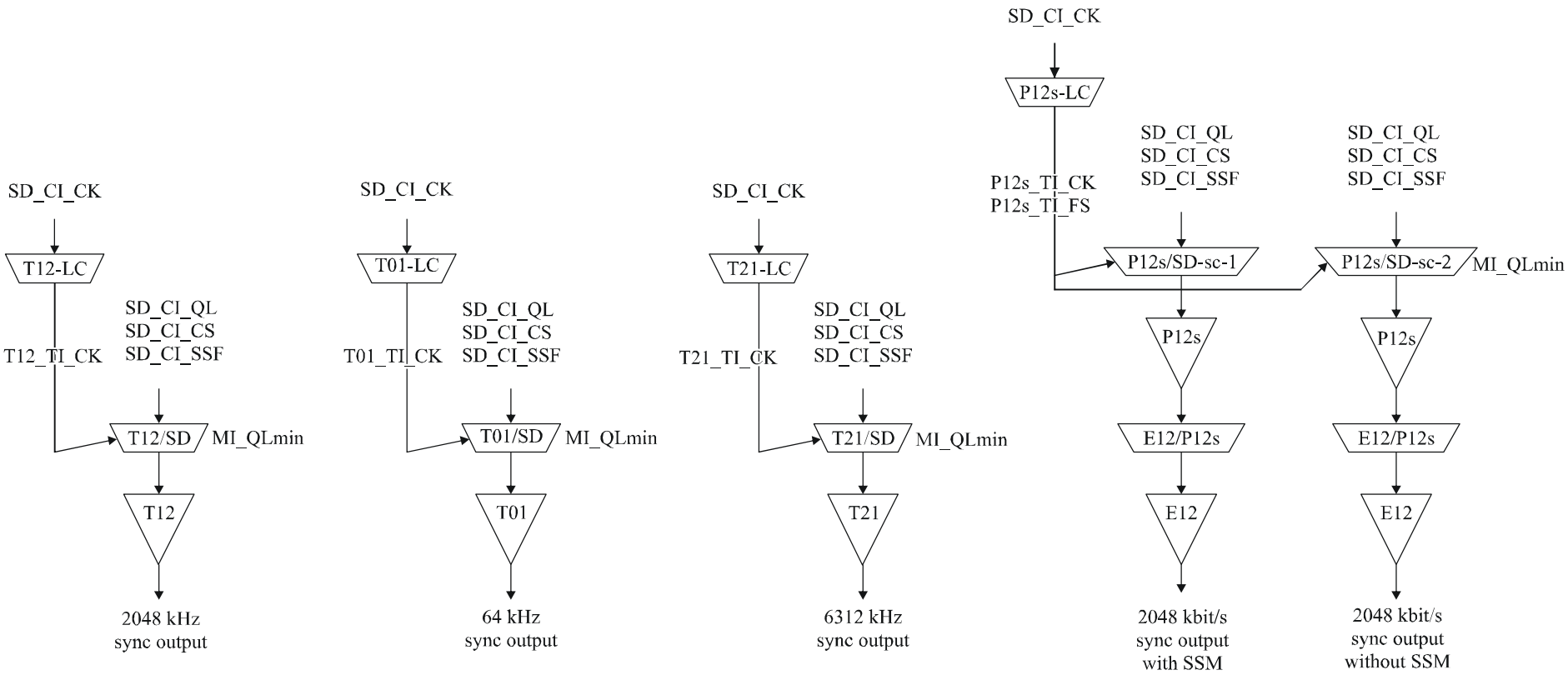


Figure I.2 – Synchronization transport port models: Station clock outputs

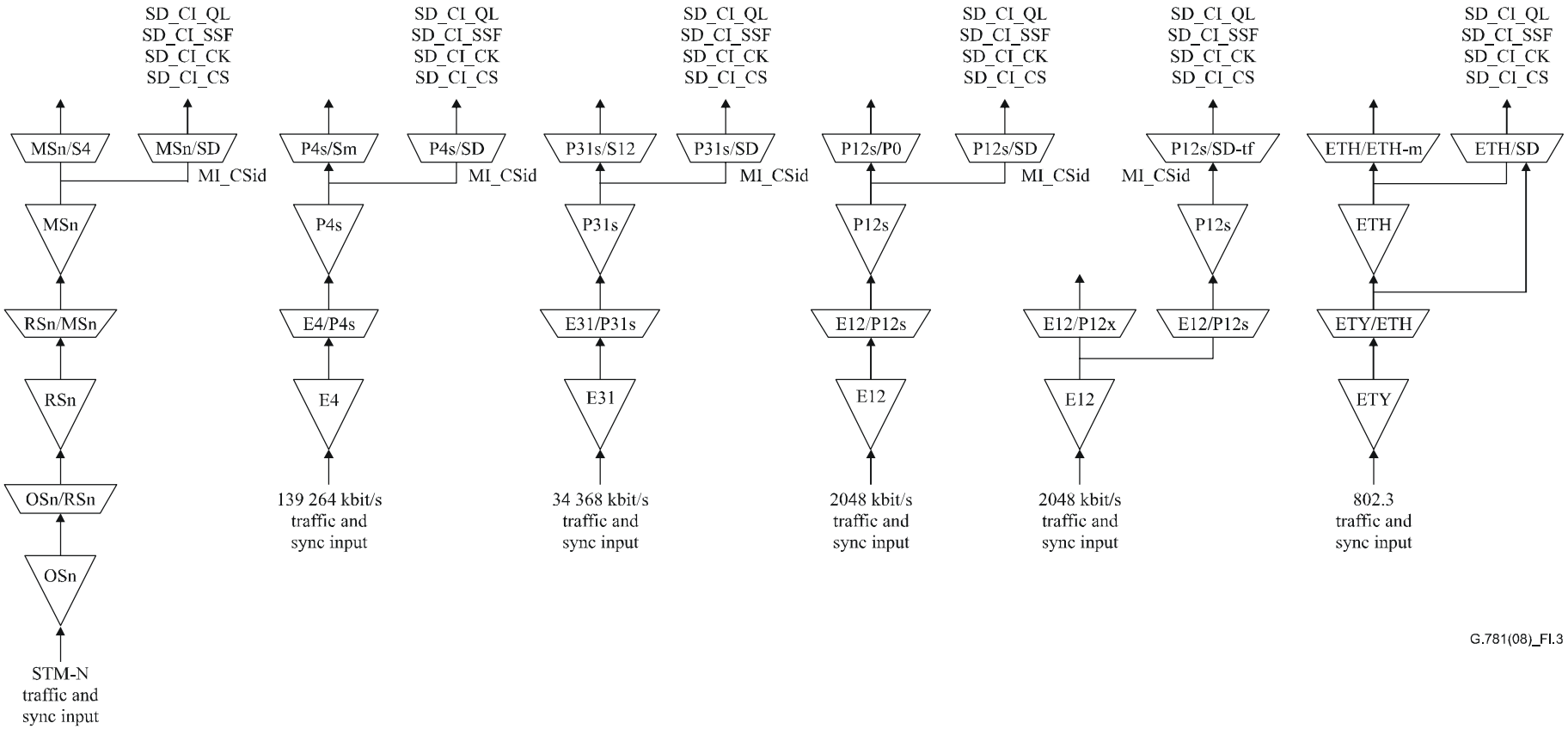


Figure I.3 – Synchronization transport port models: Traffic (line and tributary) inputs

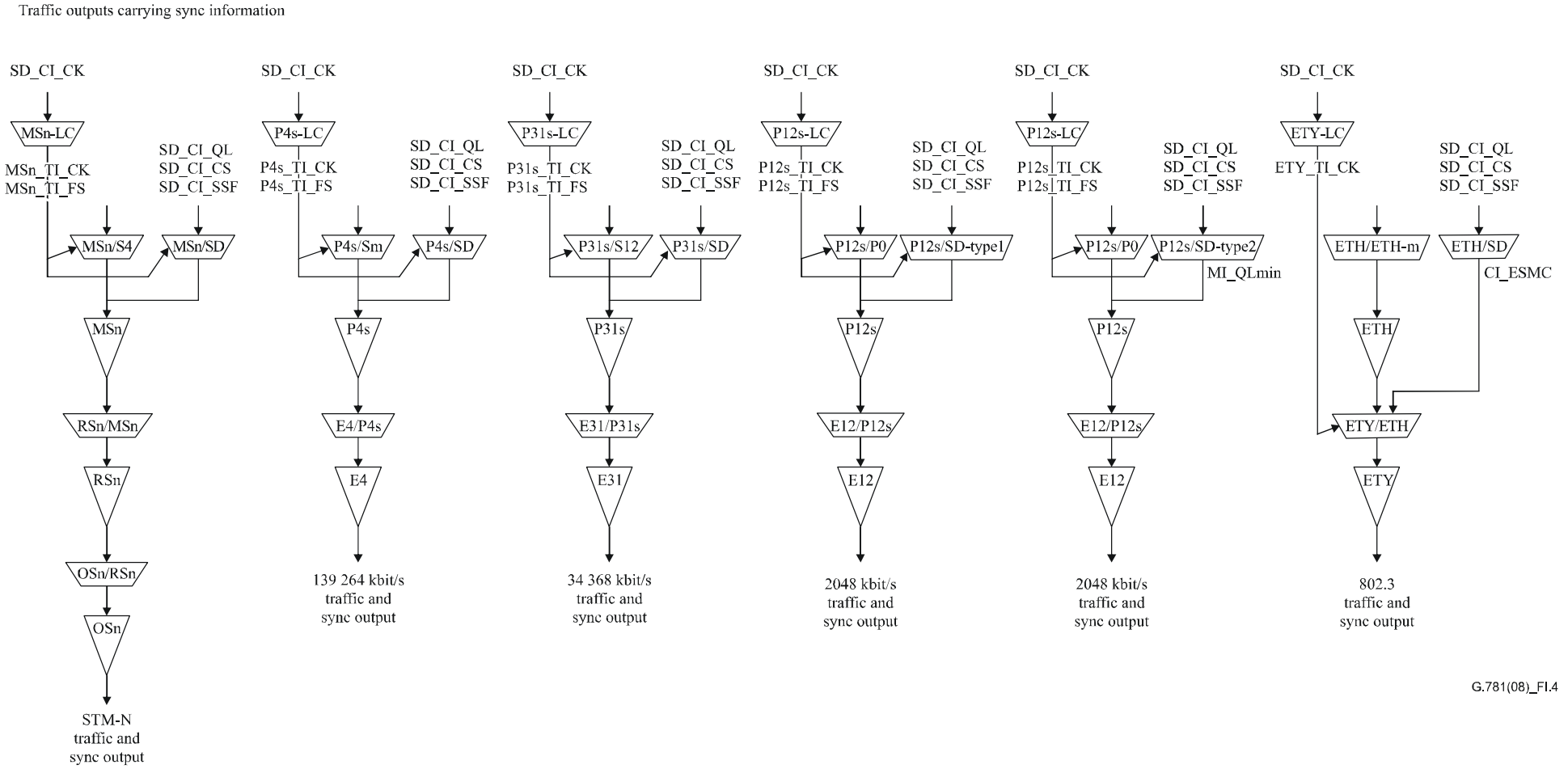


Figure I.4 – Synchronization transport port models: Traffic (line and tributary) outputs

Appendix II

Examples of synchronization functionality in the NE

(This appendix does not form an integral part of this Recommendation)

II.1 Examples of synchronization functionality in the NE for option I networks

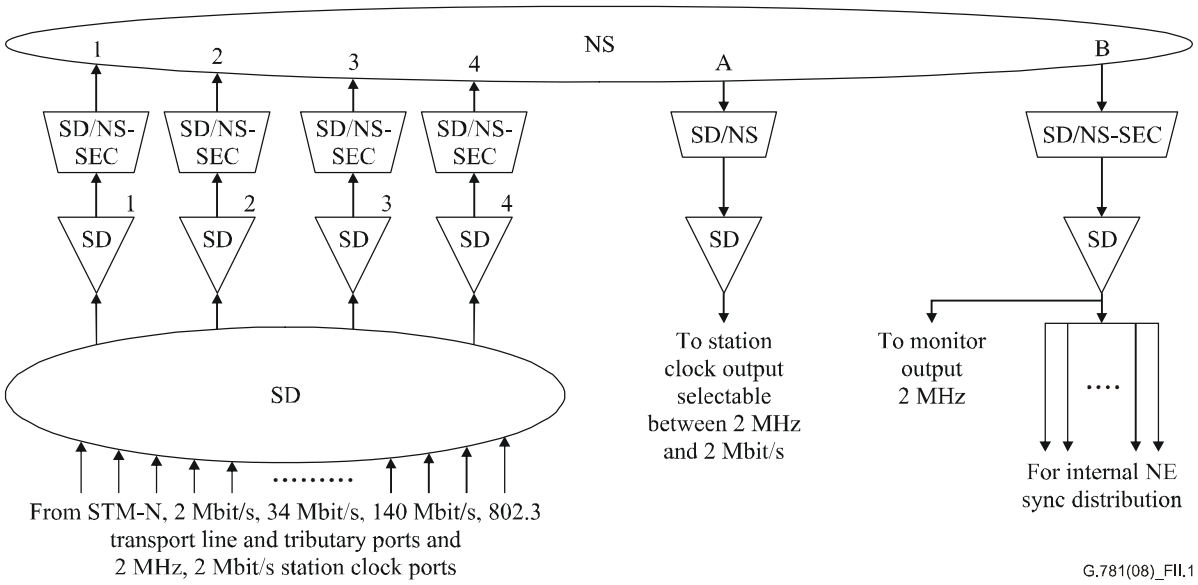


Figure II.1 – Example 1 of a network element's synchronization distribution layer functional model

Figure II.1 presents an example of the SD layer functionality within a network element providing SEC quality timing. The NE in the example offers four timing ports that can be connected to the transport ports carrying synchronization information, selected from the set of line and tributary transport ports and/or station clock ports within the NE.

Output B of NS_C function may use all four input signals to select the best synchronization reference input signal. Output A should exclude input signals derived from station clock ports if output A is connected to the source of the station clock input signal (see clause 5.13.1); otherwise, output A may select from all four input signals. Both outputs select independently of each other an input out of the set of configured inputs for that particular output.

NOTE 1 – The correct provisioning is a responsibility of the user of the equipment.

The signal at output B of NS_C is connected to the system clock process (NS/SD-SEC_A_So). When it meets certain criteria it is used as a reference signal for the system clock process. Otherwise, the clock process will enter holdover.

The output signal of the system clock process is used to time the atomic functions inside the network element. In addition, it is output also via the station clock output dedicated to monitoring the internal clock signal.

The signal at output A of NS_C is connected to the station clock output.

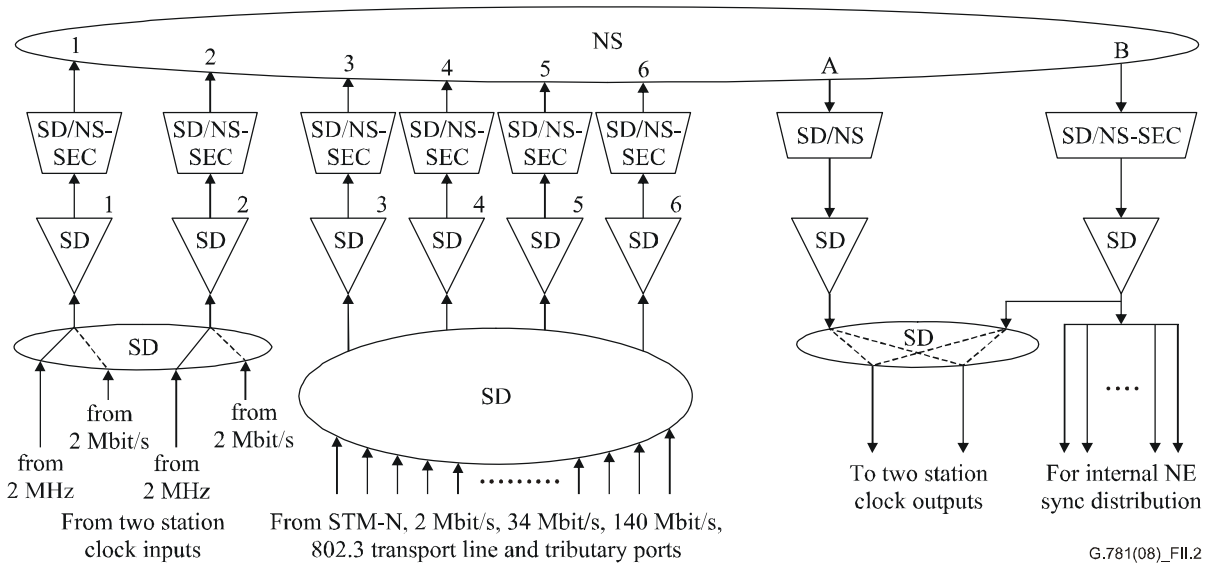


Figure II.2 – Example 2 of a network element's synchronization distribution layer functional model

Figure II.2 presents a second example of the SD layer functionality within a network element providing SEC quality timing. The NE in the example offers two station clock timing ports, each of them being either of the type 2 MHz or 2 Mbit/s. These station clock based synchronization reference input signals can both be connected to a timing port (SD_TT_Sk #1, #2).

Furthermore, the NE offers four timing ports that can be connected to a number of transport ports carrying synchronization information, selected from the set of line and tributary transport ports within the NE. Signals from timing ports within the range #3 to #6 that are not connected to a transport port will be disconnected in the NS_C function.

Output B of NS_C function may use all six input signals to select the best synchronization reference input signal. Output A should exclude input signals #1 and #2. Both outputs select independently of each other an input out of the set of configured inputs for that particular output.

The signal at output B of NS_C is connected to the system clock process (NS/SD-SEC_A_So). When it meets certain criteria, it is used as a reference signal for the system clock process. Otherwise, the clock process will enter holdover.

The output signal of the system clock process is used to time the atomic functions inside the network element. As an option, it can also be output via one or both station clock outputs. The latter to support monitoring of the internal clock signal, or to provide a synchronization signal to, e.g., a small synchronous network element that is the last in the chain.

The signal at output A of NS_C is connected to the station clock output selector (SD_C). Depending on the application in the network, station clock outputs #1 and #2 can operate as a protection pair both sourced by the same input of SD_C, or as two independent outputs sourced by the same or different input signals (as appropriate for the application).

NOTE 2 – Figure II.2 presents two instances of SD_C functions (the first connected to SD_TT_Sk functions #1 and #2 and the second connected to SD_TT_Sk functions #3 to #6) to reflect explicitly the supported connectivity in the network element. The station clock input signals can be connected to timing ports 1, and 2 and not to timing ports 3 to 6. Similarly, the line and tributary input signals can be connected to timing ports 3 to 6, and not to timing ports 1 and 2.

II.2 Examples of synchronization functionality in the NE for option II networks

For further study.

II.3 Examples of synchronization functionality in the NE for option III networks

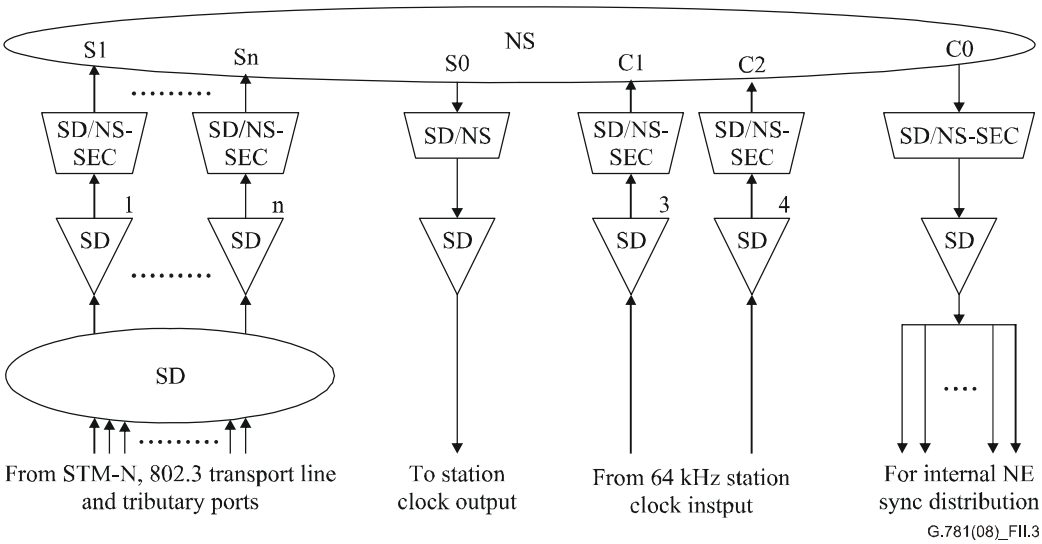


Figure II.3 – Example of a network element's synchronization distribution layer functional model for option III network

Figure II.3 presents a third example of the SD layer functionality within a network element operating in an option III network.

In option III, the output C0 of NS_C function should use only two input signals derived from station clock ports (#C1 or #C2) to select the best synchronization reference input signal, and should not use input signals derived from each transport port.

The signal at output C0 of NS_C is connected to the system clock process (NS/SD-SEC_A_So). When it meets certain criteria, it is used as a reference signal for the system clock process. The output signal of the system clock process is used to time atomic functions inside the network element.

Output S0 of NS_C may use all of the input signals that are offered from transport ports (from #S1 to #Sn) to select the synchronization reference signal. The selection process to output S0 in NS_C function is only provided by the operator.

The signal at output S0 of NS_C is connected to the station clock output.

Appendix III

Delay time allocation for option I and III networks

(This appendix does not form an integral part of this Recommendation)

III.1 Delay and processing times for the synchronization selection process

The following delay and processing times are defined for an SEC using the QL-enabled mode for the reference selection process in Option I and III networks. They are based on a ring configuration with 20 NEs. Delay and processing times for other applications (e.g., SSU) are for further study.

Three delay time values are defined for the synchronization selection process of the SEC. These are the non-switching message delay T_{NSM}, the switching message delay T_{SM} and the holdover message delay T_{HM}. These times are measurable at the interfaces of the NE.

These delay times are caused by internal delay and processing times of the synchronization distribution atomic functions. The hold-off time t_h and processing time t_p are part of the reference selection process of the NS_C function. The settling time t_s is part of the SD/NS-SEC_A_So function. For a detailed description, see clause 6.

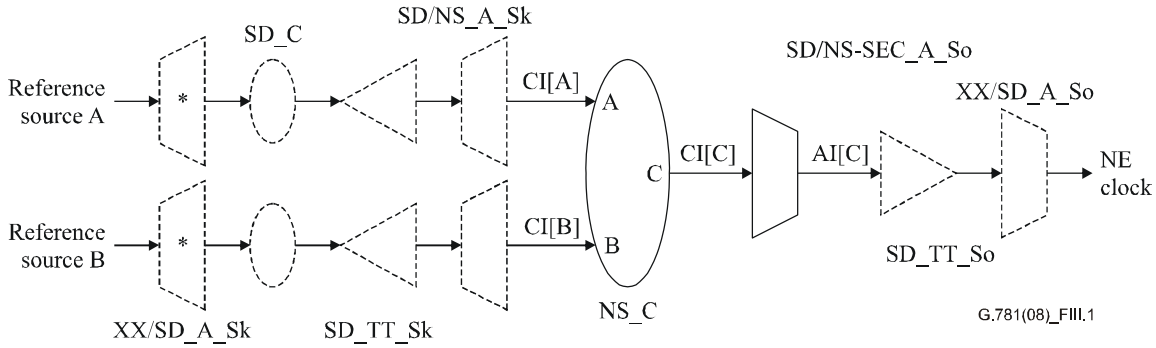


Figure III.1 – Example configuration for clock selection

The timing diagrams in the following description are based on a configuration with two clock reference sources as shown in Figure III.1.

The dotted functions in the figure do not contribute to delay and processing times. The persistence check for SSM acceptance in the XX/SD_A_Sk functions is also not considered in the following as it is small compared to the overall time.

III.2 Non-switching message delay T_{NSM}

This delay applies when the QL of the selected reference signal changes and the sync source is maintained. T_{NSM} defines the maximum time between the change of the input QL and the change of the output QL (Figure III.2).

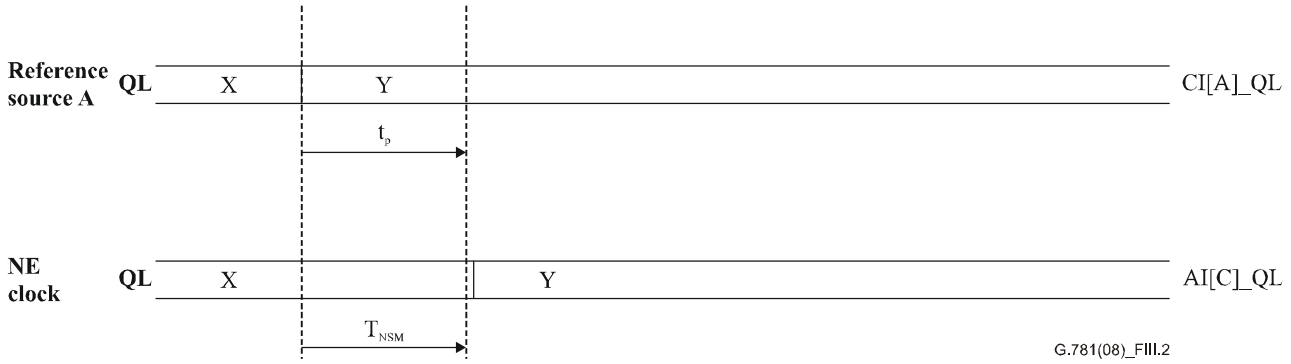


Figure III.2 – T_{NSM}

T_{NSM} is due to the processing time t_p of the reference selection process in the NS_C function.

A maximum value of 200 ms is defined for T_{NSM}.

$T_{NSM} = t_p$ = 0 ms to 200 ms.

III.3 Switching message delay T_{SM}

This delay applies if a switch over to another reference source is performed with a different QL value. T_{SM} defines the time between the triggering of the new selection (e.g., change of the QL of a reference, external command, etc.) and the change of the QL at the output (Figure III.3).

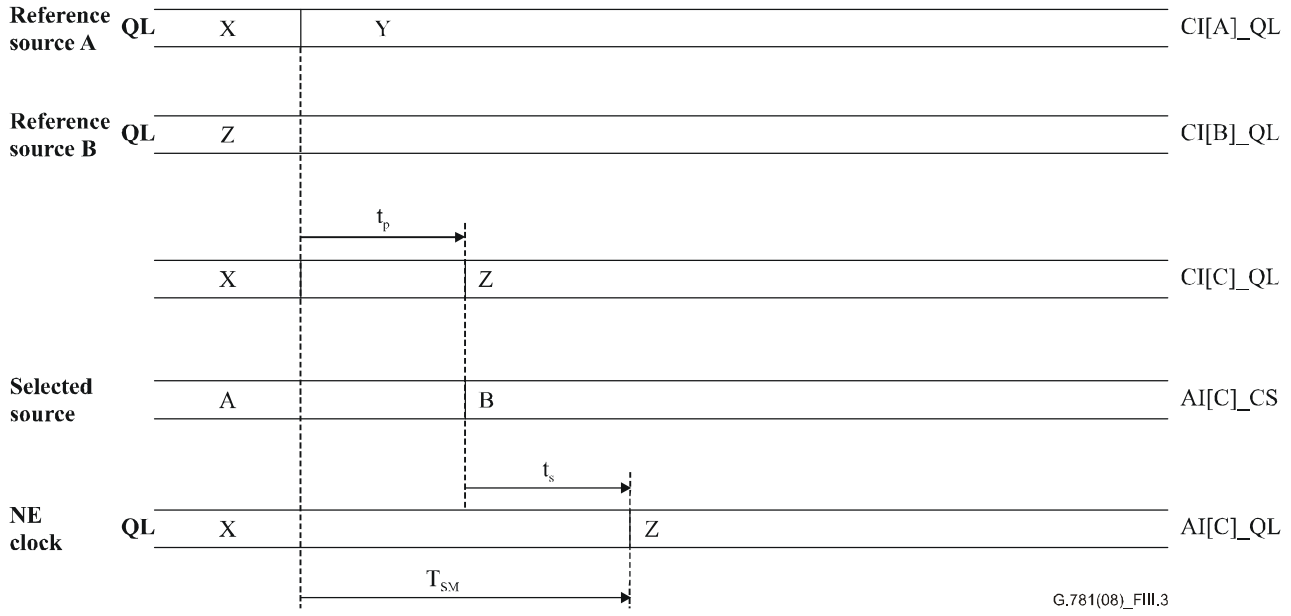


Figure III.3 – T_{SM}

T_{SM} is due to the processing time t_p of the selection process in the NS_C function and the settling time t_s of the oscillator in the SD/NS-SEC_A_So function.

A range of 180 ms to 500 ms is defined for T_{SM}.

$T_{SM} = (t_p + t_s)$ = 180 ms to 500 ms.

III.4 Holdover message delay T_{HM}

This delay applies when the SEC should enter a holdover mode due to a failure condition of the selected sync source and the unavailability of any other synchronization source. When this event occurs, the SEC goes immediately into holdover mode. The outgoing QL changes to QL_SEC after the time T_{HM} (Figure III.4).

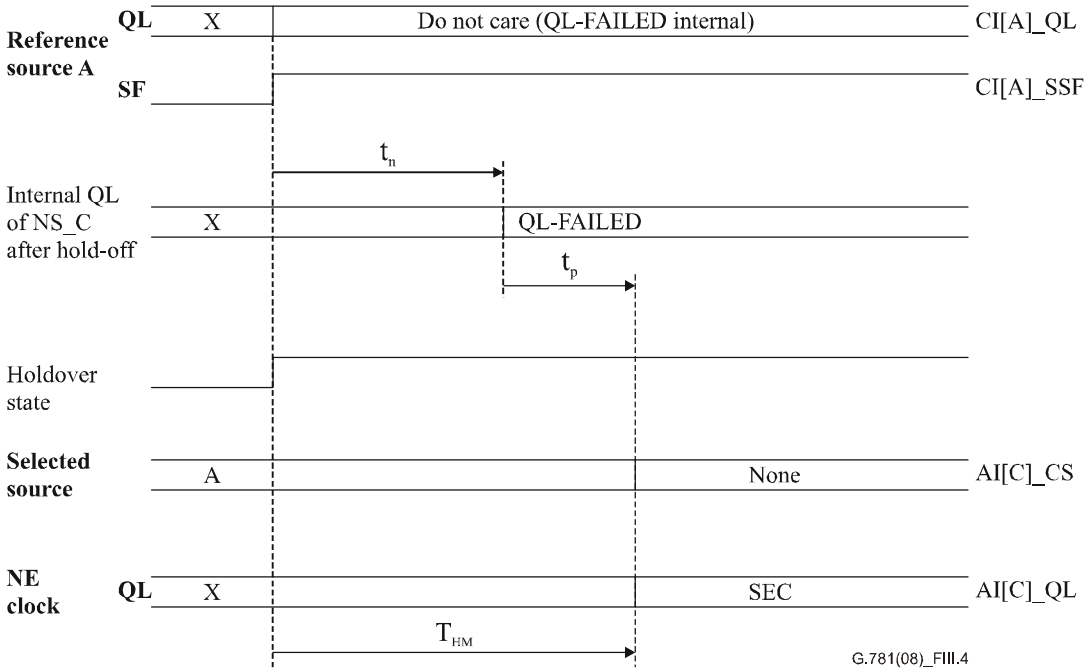


Figure III.4 – T_{HM}

NOTE – The internal QL of NS_C after hold-off characterizes a signal located between the WTR block and the selection control process box defined in Figure A.1.

T_{HM} is due to the QL-FAILED (SSF) hold-off time t_h and the processing time t_p of the selection process in the NS_C function.

A range of 300 ms to 2000 ms is defined for T_{HM}.

$T_{HM} = t_h + t_p$ = 300 ms to 2000 ms.

III.5 Wait to restore time T_{WTR}

The wait to restore time applies when a synchronization source signal recovers from a failure condition. This signal comes available only for the selection process after signal fail is cleared at least for the time T_{WTR} (Figure III.5).

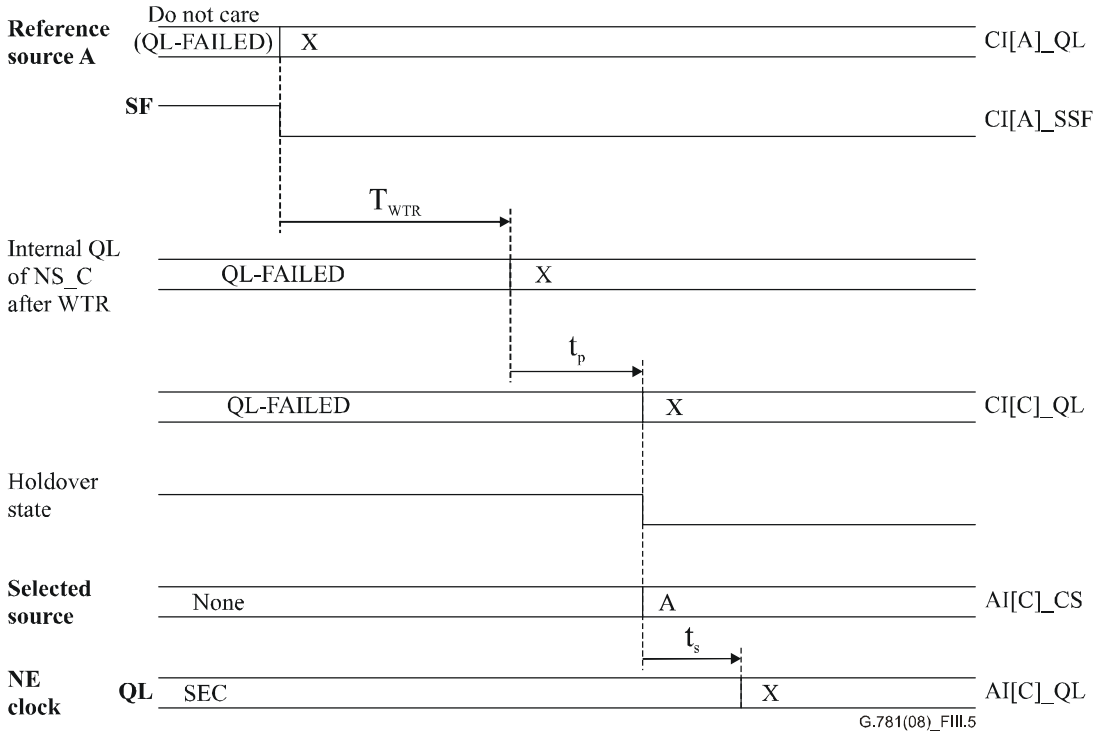


Figure III.5 – T_{WTR}

NOTE – The internal QL of NS_C after WTR characterizes a signal located between the WTR block and the selection control process box defined in Figure A.1.

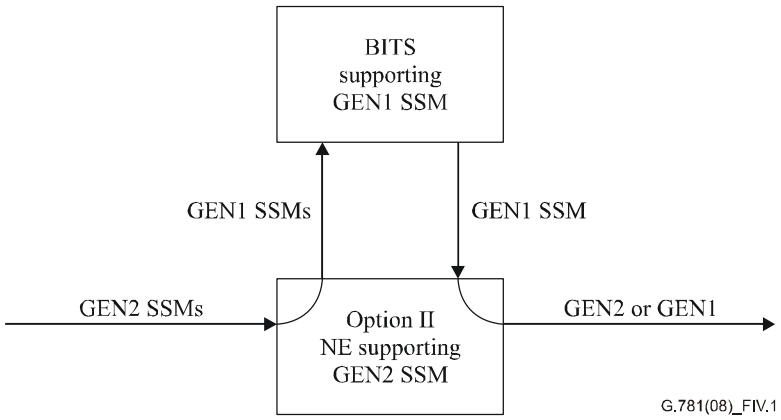
T_{WTR} is implemented in the NS_C function. The definition of WTR is in clause 4.

Appendix IV

Interworking of option II equipment supporting second generation SSM and first generation SSM using a translation function

(This appendix does not form an integral part of this Recommendation)

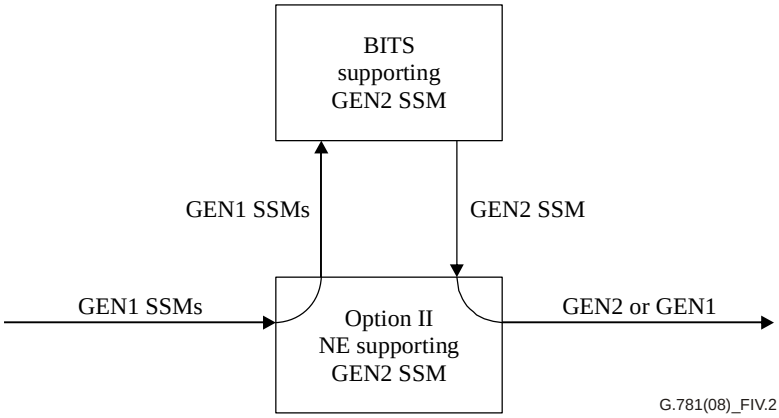
Translation between second generation (GEN2) and first generation (GEN1) SSM is necessary to ensure interoperability. Both the number of quality levels and the quality level definitions differ between GEN2 and GEN1. However, the GEN1 SSMs are a subset of GEN2. The translation function is a provisionable option on a per-port basis (both STM-N and 1544 kbit/s station clock) in equipment supporting GEN2 SSM to provide acceptable SSM to equipment supporting GEN1 SSM. Figures IV.1 and IV.2 show examples of message flows between equipment supporting GEN2 and GEN1 SSM. In Figure IV.1 a NE supporting GEN2 SSM is co-located with a BITS supporting GEN1 SSM. In this case, the 1544 kbit/s station clock output port of the NE is provisioned to provide the translation from GEN2 to GEN1 SSM.



* Message output depends on SSM message requirement of downstream equipment or co-located SASE.

Figure IV.1 – Example of SSM translation between an option II NE (GEN2) and a BITS (GEN1)

In Figure IV.2, an SDH option II NE is co-located with a BITS supporting GEN2 SSM. In this case, the NE receives GEN1 SSM. In this case, there is no need for any translation provisioning and the 1544 kbit/s station clock output just passes the received SSM to the BITS.



* Message output depends on SSM message requirement of downstream equipment or co-located SASE.

Figure IV.2 – Example of SSM translation between an option II NE (GEN2) and a BITS (GEN2)

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