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SERIES K: PROTECTION AGAINST INTERFERENCE

Surge protective component application guide – High frequency signal isolation transformers

Recommendation ITU-T K.126

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Surge protective component application guide – High frequency signal isolation transformers

Summary

Failures of Ethernet local area network (LAN) ports have been attributed to the use of inappropriate surge protective devices (SPDs), lack of insulation coordination and inappropriate wiring, which causes the failure of transformers, associated wiring, components and connectors. Recommendation ITU-T K.126 discusses isolation transformer parameters and how they influence the equipment common-mode and differential-mode surge performance. Access to the full text of Recommendation ITU-T K.95 is necessary to fully understand this Recommendation.

History

Edition	Recommendation	Approval	Study Group	Unique ID*
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Keywords

Characteristics, common-mode surge, differential-mode surge, Ethernet, high frequency, isolation transformer, power over Ethernet, PoE, ratings, surge protective device, SPD.

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* To access the Recommendation, type the URL http://handle.itu.int/ in the address field of your web browser, followed by the Recommendation's unique ID. For example, http://handle.itu.int/11.1002/1000/11830-en.

FOREWORD

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1 Scope

The [b-ITU-T K.96] application overview guide and other ITU-T component specific guide Recommendations cover surge protective components (SPCs) used in power and telecom surge protective devices (SPDs) and equipment ports. This application guide on high frequency signal isolation transformer technology SPCs covers:

- component construction;
- characteristics;
- ratings;
- application examples.

2 References

The following ITU-T Recommendations and other references contain provisions which, through reference in this text, constitute provisions of this Recommendation. At the time of publication, the editions indicated were valid. All Recommendations and other references are subject to revision; users of this Recommendation are therefore encouraged to investigate the possibility of applying the most recent edition of the Recommendations and other references listed below. A list of the currently valid ITU-T Recommendations is regularly published. The reference to a document within this Recommendation does not give it, as a stand-alone document, the status of a Recommendation.

[ITU-T K.95] Recommendation ITU-T K.95 (2016), *Surge parameters of isolating transformers used in telecommunication devices and equipment*.

3 Definitions

3.1 Terms defined elsewhere

This Recommendation uses the following terms defined elsewhere:

3.1.1 clearance [b-IEC/TR 60664-2-1]: Shortest distance in air between two conductive parts.

3.1.2 common-mode surge [ITU-T K.95]: Surge appearing equally on all conductors of a group at a given location.

NOTE 1 – The reference point for common-mode surge voltage measurement can be a chassis terminal, or a local earth/ground point.

NOTE 2 –Also known as longitudinal surge or asymmetrical surge.

3.1.3 creepage distance [b-IEC/TR 60664-2-1]: Shortest distance along the surface of a solid insulating material between two conductive parts.

3.1.4 designation of an impulse shape [b-IEC 60099-4]: Combination of two numbers, the first representing the virtual front time (T1) and the second the virtual time to half-value on the tail (T2).

NOTE 1 – It is written as T1/T2, both in microseconds, the sign "/" having no mathematical meaning.

NOTE 2 – Some standards use alternative designations such as A/B or T1 × T2.

NOTE 3 – Combination wave generators have both voltage and current impulse designations given separated by a hyphen e.g., 1.2/50-8/20.

NOTE 4 – Waveshapes defined as maximum front time and minimum time to half value are expressed as <T1/>T2.

3.1.5 differential-mode surge [ITU-T K.95]: Surge occurring between any two conductors or two groups of conductors at a given location.

NOTE 1 –The surge source may be floating, without a reference point or connected to reference point, such as a chassis terminal, or a local earth/ground point.

NOTE 2 – Also known as metallic surge or transverse surge or symmetrical surge or normal surge.

3.1.6 electric screen [b-IEC 60050-151]: Screen of conductive material intended to reduce the penetration of an electric field into a given region.

3.1.7 impulse withstand voltage [b-IEC/TR 60664-2-1]: Highest peak value of impulse voltage of prescribed form and polarity which does not cause breakdown of insulation under specified conditions.

3.1.8 insulation coordination [b-IEC/TR 60664-2-1]: Mutual correlation of insulation characteristics of electrical equipment taking into account the expected micro-environment and other influencing stresses.

3.1.9 insulation resistance [b-IEC 62631-1]: Resistance under specified conditions between two conductive bodies separated by the insulating material.

3.1.10 isolating transformer [b-IEC 60065]: Transformer with protective separation between the input and output windings.

3.1.11 rated impulse voltage [b-IEC/TR 60664-2-1]: Impulse withstand voltage value assigned by the manufacturer to the equipment or to a part of it, characterizing the specified withstand capability of its insulation against transient overvoltages.

3.1.12 rated winding d.c. [ITU-T K.95]: Maximum winding current that will not cause the winding conductor temperature to exceed a specified increase above the ambient temperature.

3.1.13 surge [ITU-T K.95]: Temporary disturbance on the conductors of an electrical service caused by an electrical event not related to the service.

3.1.14 virtual front time; T1: The front time T1 of a voltage impulse is 1/0.6 times the interval T between the instants when the impulse is 30% and 90% of the peak value [b-IEC 60060-1]. The front time T1 of a surge current impulse is 1.25 times the interval T between the instants when the impulse is 10% and 90% of the peak value [b-IEC 62475].

NOTE – Some standards use the 10% and 90% front time measurement for the voltage impulse.

3.1.15 virtual origin; O1: For the impulse voltage waveform, it is the instant at which a straight line drawn through the 30% and 90% amplitude values crosses the time axis [b-IEC 60060-1]. For the impulse current waveform, it is the instant at which a straight line drawn through the 10% and 90% amplitude values crosses the time axis [b-IEC 60060-1].

3.1.16 virtual time to half-value; T2 [b-IEC 60060-1][b-IEC 62475]: Interval of time between the instant of virtual origin O1 and the instant when the voltage or current has decreased to half the peak value.

3.1.17 withstand voltage [b-IEC/TR 60664-2-1]: Voltage to be applied to a specimen under prescribed test conditions which does not cause breakdown and/or flashover of a satisfactory specimen.

3.2 Terms defined in this Recommendation

None.

4 Abbreviations and acronyms

This Recommendation uses the following abbreviations and acronyms:

DMM	Digital multimeter
GDT	Gas Discharge Tube
IR	Insulation Resistance
LAN	Local Area Network
LIT	Lightning Isolation Transformer
PoE	Power over Ethernet
POTS	Plain Old Telephone System
RJ45	Registered Jack 45
SPC	Surge Protective Component
SPD	Surge Protective Device

5 Conventions

This Recommendation uses the following:

[b-IEC 60617] Type 1 symbols to represent the different transformer configurations.

Figure 5-1 shows the symbol for a two-winding transformer.

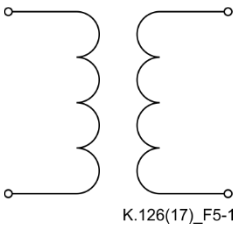


Figure 5-1 – Symbol for a two-winding transformer

Figure 5-2 shows the symbol for a two-winding transformer with instantaneous voltage polarity indicators.

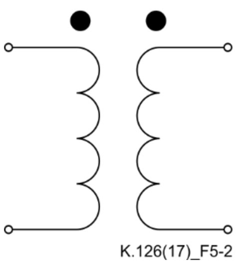


Figure 5-2 – Symbol for a two-winding transformer with polarity indication

Figure 5-3 shows the symbol for a two-winding transformer with an electric screen between the windings.

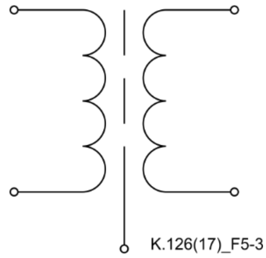


Figure 5-3 – Symbol for a two-winding transformer with electric screen

Figure 5-4 shows the symbol for a transformer with centre-tapped windings. When testing is done with shorted windings, the centre tap is also connected to that winding shorting link, other testing is done without any connection to the centre tap terminal.

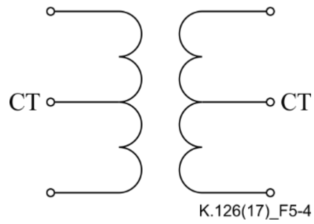


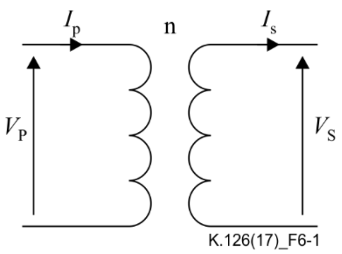
Figure 5-4 – Transformer with centre-tapped windings

6 Component construction

6.1 Transformer basics

The ideal transformer transforms the primary winding voltage, V_P, to a secondary winding voltage of V_S. The relationship is $V_S = V_P/n$, where n is the primary to secondary turns ratio.

Similarly the primary winding current, I_P, transforms to a secondary winding current of I_S. The relationship is $I_S = I_P*n$. The transformer is 100 % efficient with a primary power of V_P*I_P and a secondary power of $V_S*I_S = (V_P/n)*(I_P*n) = V_P*I_P$. The transformer winding inductance is considered to be high enough that it does not adversely affect the circuit operation. Figure 6-1 shows the ideal transformer.



V_P Primary winding voltage
I_P Primary winding current
V_S Secondary winding voltage
I_S Secondary winding current
n Transformer primary to secondary turns ratio

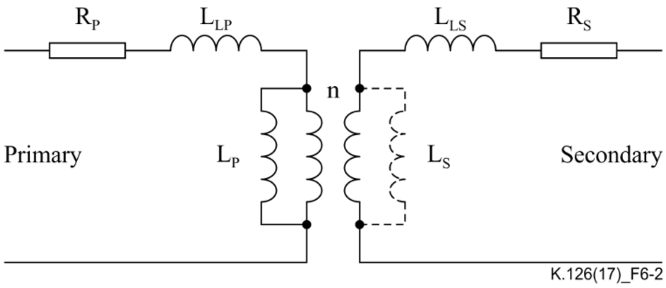
Figure 6-1 – Ideal transformer

6.2 Transformer parasitics

The primary winding and secondary winding will not be perfectly coupled and the non-coupled inductance is called leakage inductance. Circuit-wise winding leakage inductance can be emulated by adding a series inductor, L_{LP}, to the primary winding and adding a series inductor, L_{LS}, to the secondary winding. (In circuit simulation, an alternative is to make the winding coupling factor, k, less than one.)

Neither will the windings have zero resistance. Winding resistance is emulated by adding a series resistor, R_P, to the primary winding and a series resistor, R_S, to the secondary winding.

The primary winding will not have infinite inductance and is represented by the inductor, L_P, which transforms to a secondary inductor of $L_S = L_P/n^2$. Inductor, L_P, is effectively in parallel with the primary winding of the ideal transformer. Figure 6-2 shows the equivalent circuit with the parasitics. Example values are shown in Table 1.



L_P	Primary winding self-inductance component	L_S	Secondary winding self-inductance component
L_{LP}	Primary winding leakage inductance component	L_{LS}	Secondary winding leakage inductance component
R_P	Primary winding resistance component	R_S	Secondary winding resistance component
n	Transformer primary to secondary turns ratio		

Figure 6-2 – Ideal transformer with winding leakage inductance, winding resistance and the actual primary self-inductance added

6.3 Transformer core saturation

Without a core, the primary and secondary windings have a low inductance and poor coupling. Figure 6-3 shows how the two windings are effectively independent. Current through a winding creates a widely dispersed magnetic flux, Φ, in and around the winding, see Figure 6-3.

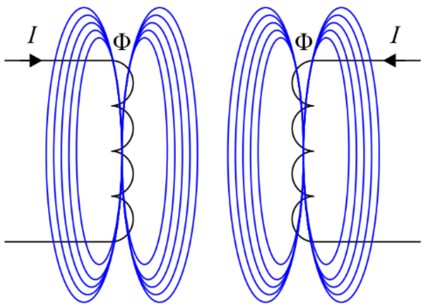


Figure 6-3 – Transformer winding flux without a core in place

When the windings are on a magnetic core, the flux is strongly constrained to the core resulting in a good coupling between the windings and a higher winding inductance value, see Figure 6-4.

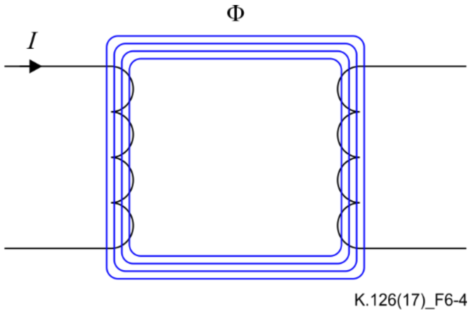


Figure 6-4 – Transformer winding flux with a core in place

The general magnetic formula for winding inductance is L = N*Φ/I_{MAG}, where N is the number of turns of the winding, Φ is the winding flux and I_{MAG} is the winding magnetizing current. The inductance L is proportional to the flux to current ratio, Φ/I_{MAG}. The winding without a core has a constant Φ/I_{MAG} slope and the inductance value will be constant too, see Figure 6-5. The winding with a core has a high initial Φ/I_{MAG} slope that decreases rapidly in the winding saturation current, I_{MAGSAT}, region and stabilizes to a low slope thereafter. The resultant inductance versus current characteristic will show a high initial inductance value, which decreases in the I_{MAGSAT} region and stabilizes to a low value, as shown in Figure 6-5.

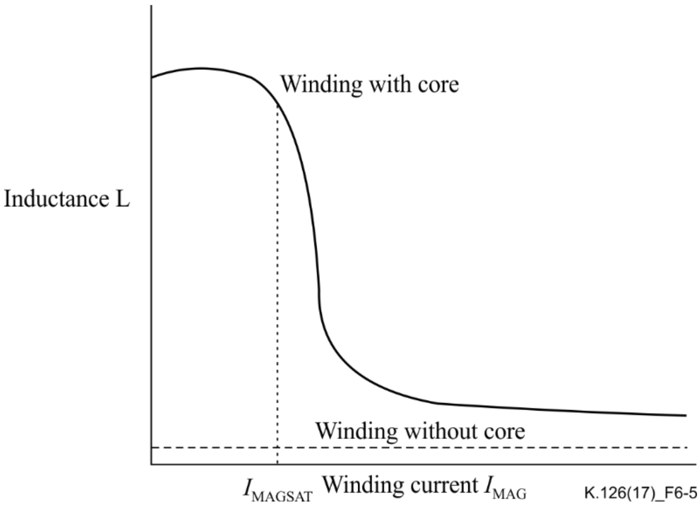


Figure 6-5 – Winding inductance, *L*, versus winding magnetizing current I_{MAG}

Although the saturation "knee" in the Figure 6-5 characteristic exists over a range of current, under fast-rising current surge conditions the inductance change accelerates the transition through the I_{MAGSAT} region. This rapid transition makes it easy to determine when core saturation occurs, see Figure 9-10.

Once the transformer core has saturated, the secondary circuit can be represented as a series circuit consisting of the secondary saturated winding inductance component, L_{SSAT}, carrying the peak secondary current just prior to saturation, I_{SM}, the secondary leakage inductance component, L_{LS} and the secondary winding resistance component, R_S.

6.4 High frequency signal transformers

Soft ferrites are often used for the cores of high frequency transformers. In depth details of soft ferrites and transformers using them can be found in [b-Snelling, 1988] and [b-Snelling, 1983].

To reduce the leakage inductance to a negligible level, the primary and secondary wires are often wound together on the core. This is called bifilar winding, which is defined as a set of two coils whose turns consist of two contiguous conductors isolated from one another. As the wires are in contact with each other, the wire insulation coating must be able to withstand the rated impulse voltage. The closeness of the two winding conductors increases the inter-winding capacitance and a value of about 25 pF is typical.

Power over Ethernet (PoE) requires a primary winding centre-tap from which to extract the DC (direct current) power. Transformers for this purpose are often quadfilar wound, i.e., four wires are wrapped together, then wound on to the core. Pairs of windings can then be connected in series to give two centre-tapped windings as shown in Figure 6-6.

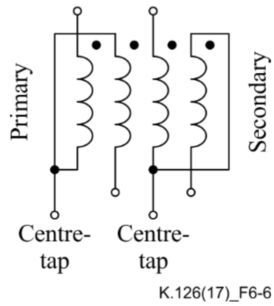


Figure 6-6 – Quadfilar wound centre-tapped primary and secondary windings

Often common-mode chokes and Ethernet transformers are supplied as a complete assembly. Circuit examples of these are shown in Figure 6-7. Such assemblies combined with a registered jack 45 (RJ45) are also available, although some of these combined units have been found to have creepage and clearance problems [b-Ardley].

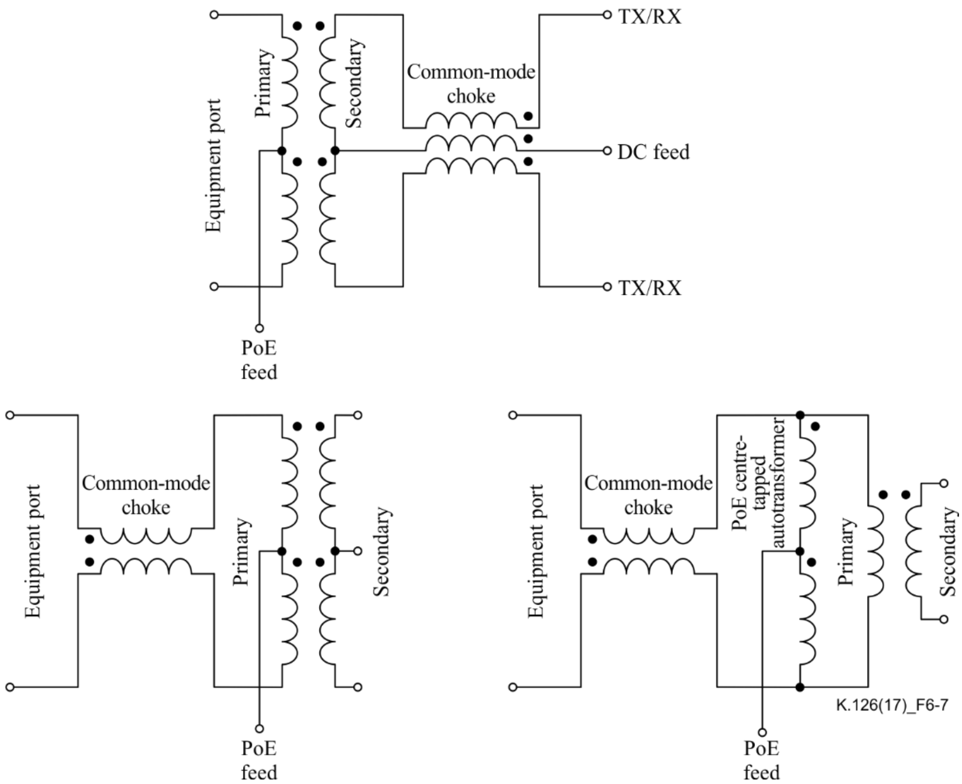


Figure 6-7 – Magnetic assembly circuits

Figure 6-8 illustrates a wound component assembly, the unpotted view showing four quadfilar wound Ethernet transformers with their smaller four bifilar wound common-mode chokes.

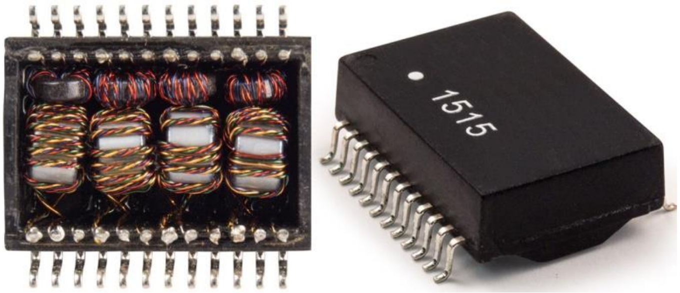


Figure 6-8 – Unpotted and potted magnetic assembly for one Ethernet port

(Figure 6-8 is reproduced with permission from Bourns, Inc.)

7 Characteristics

7.1 Measurement

[ITU-T K.95] defines the test circuits and measurement procedures for the transformer parameters discussed in this clause.

7.2 Inter-winding capacitance

The value of the inter-winding capacitance value determines the level of capacitive current that flows into the secondary circuit as a result of primary voltage, d*V*/d*t*. [ITU-T K.95] uses the circuit shown in Figure 7-1 to measure the total primary winding to secondary winding capacitance component, $C_{P\text{-}S}$. For the purposes of circuit modelling, 50% of $C_{P–S}$, can be considered as connected between the winding starts and the remaining 50% of $C_{P–S}$, can be considered as connected between the winding ends.

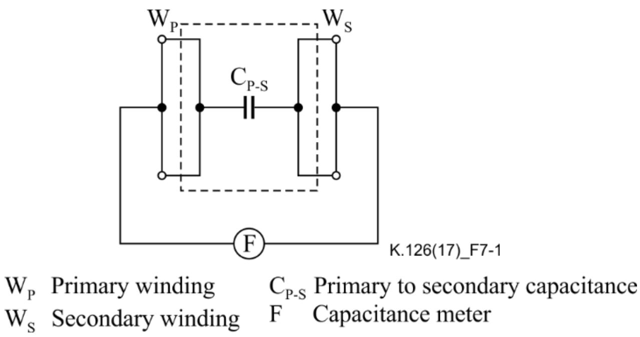
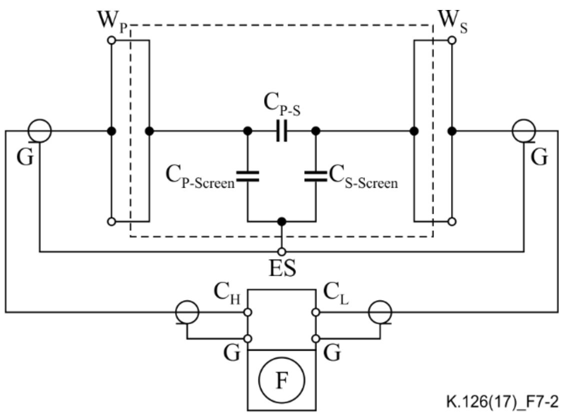


Figure 7-1 – Test circuit to measure the transformer inter-winding capacitance

If the transformer has an electric screen between the primary and secondary windings, three capacitances need to be considered, the residual inter-winding capacitance component, $C_{P–S}$, the primary to screen capacitance component, $C_{P–Screen}$ and the secondary winding to screen capacitance component, $C_{S–Screen}$. [ITU-T K.95] uses the circuit shown in Figure 7-2 to measure these three capacitance values.



W_P	Primary winding	$C_{P-Screen}$	Primary to screen capacitance
W_S	Secondary winding	$C_{S-Screen}$	Secondary to screen capacitance
ES	Electric screen	C_{P-S}	Primary to secondary residual capacitance
C_H	Capacitance measurement connection Hi	G	Guard connection (coaxial cables screen)
C_L	Capacitance measurement connection Lo	F	Guarded measurement capacitance bridge

Figure 7-2 – Test circuit to measure the inter-winding capacitance of a transformer with an electric screen

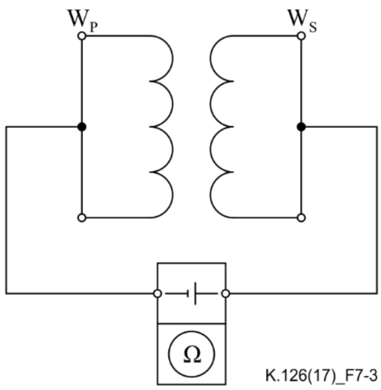
The values of $C_{P-Screen}$ and $C_{S-Screen}$ can be measured by making the following connection changes in Figure 7-2:

– For $C_{P-Screen}$ measurement, connect C_H to W^P, connect C_L to ES, and connect G to W_S.

– For $C_{S-Screen}$ measurement, connect C_H to W_S, connect C_L to ES, and connect G to W_P.

7.3 Insulation resistance

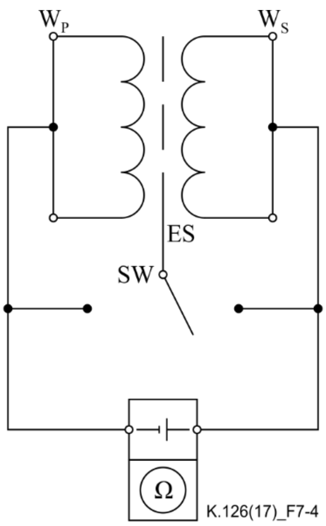
[b-IEEE 802.3] requires that the Ethernet port insulation resistance (IR) at 500 V d.c. be 2 MΩ or greater. [ITU-T K.95] uses the circuit shown in Figure 7-3 to measure the IR of a transformer. Both the primary winding, W_P, and secondary winding, W_S, are short-circuited. The IR is measured between the two short circuits.



W_P	Primary winding	Ω	IR meter with defined dc bias
W_S	Secondary winding		

Figure 7-3 – Test circuit to measure the insulation resistance of a transformer

If the transformer has an electric screen between the primary and secondary windings, three IRs need to be considered, primary winding to screen, secondary winding to screen and primary to secondary. [ITU-T K.95] uses the circuit shown in Figure 7-4 to measure the IR to screen values.

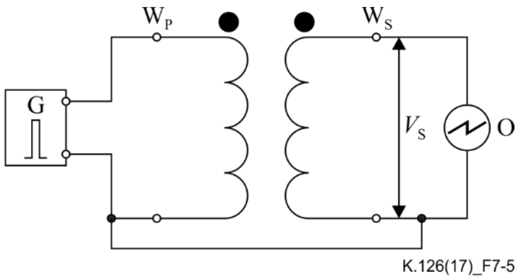


W_P Primary winding
W_S Secondary winding
ES Electric screen
Ω IR meter with defined dc bias
SW Two position selector switch

Figure 7-4 – Test circuit to measure the insulation resistance of a transformer with an electric screen

7.4 Core saturation voltage–time value

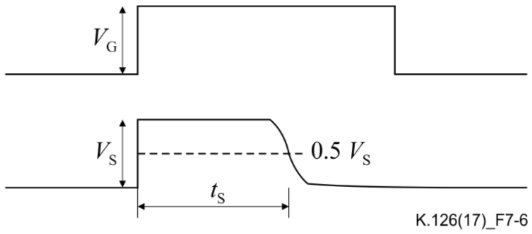
The value of the voltage–time integral, normally expressed in volt-seconds V·s, determines when the transformer core goes into saturation. [ITU-T K.95] uses the circuit shown in Figure 7-5 to measure the secondary voltage–time let-through.



W_P Primary winding
W_S Secondary winding
V_S Peak secondary winding voltage
G Pulse generator, 50 Ω source impedance
O Oscilloscope monitoring V_S

Figure 7-5 – Test circuit to measure the transformer voltage–time product

Figure 7-6 shows the generator open-circuit output voltage and the resultant secondary winding voltage. Core saturation is shown by the secondary winding voltage pulse being truncated, having a shorter duration, t_S, than the generator pulse. The transformer voltage–time product is given by $V_S t_S$, expressed in microvolt seconds. How to use the volt second parameter is given in clause 9.4.4.

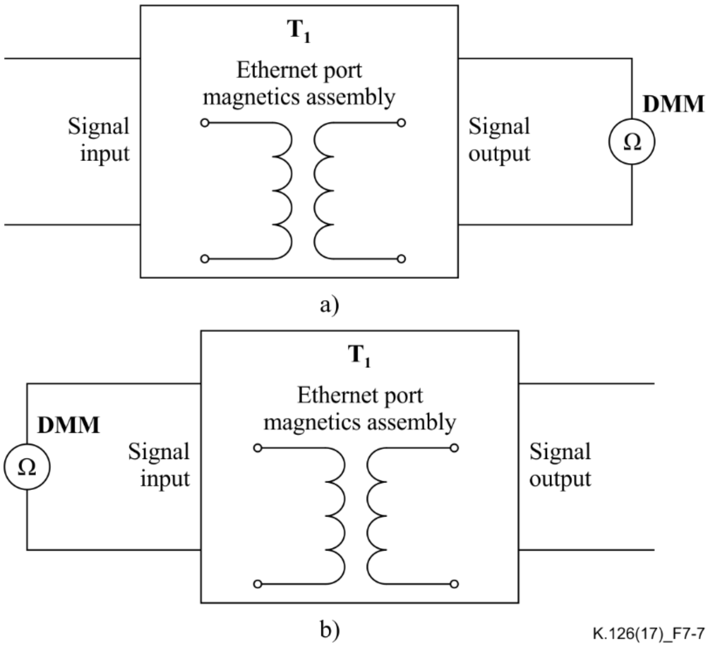


V_G Open-circuit pulse generator peak voltage t_S Secondary winding voltage time above 50% V_S
V_S Secondary winding peak voltage

Figure 7-6 – Generator and transformer secondary voltage waveforms

7.5 Winding resistance

The value of the primary winding resistance component, R_P, is important for PoE applications, since it represents a loss in delivered power. Generally the primary resistance balance of the two halves of a centre-tapped winding is within 5% and unlikely to cause a net d.c. flux in the transformer core that would substantially reduce the primary inductance value under PoE conditions. If surge protection is applied to the primary winding, the value of R_P is a factor in surge coordination. The value of secondary winding resistance component, R_S, needs to be taken into account for differential-mode surge conditions. [ITU-T K.95] uses the circuit shown in Figure 7-7 to measure winding resistance.

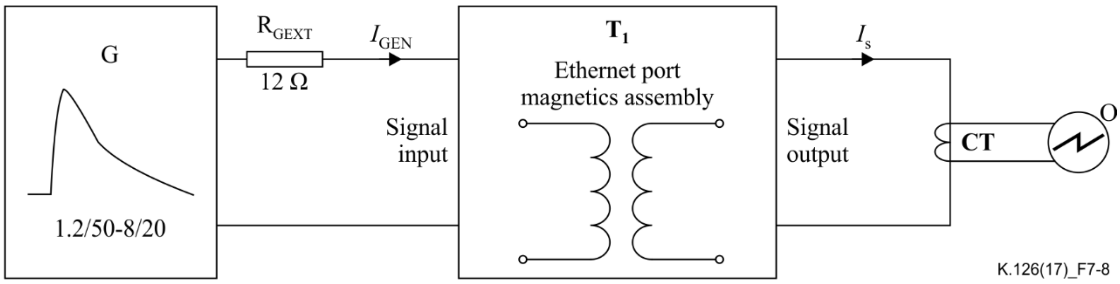


T_1 Transformer or Ethernet port magnetics assembly incorporating transformer DMM Digital multimeter or equivalent for measuring resistance

Figure 7-7 – Resistance measurement of a) secondary winding and b) primary winding

7.6 Saturated core secondary winding inductance

The value of the secondary winding saturated-core inductance component, $L_{S(SAT)}$, together with the peak secondary current at transformer core saturation determine the secondary winding surge energy after core saturation. The value of $L_{S(SAT)}$ is derived from a current decay time measurement and the secondary winding resistance component, R_S. [ITU-T K.95] uses the circuit shown in Figure 7-8 to measure the shorted secondary winding current decay time, $\tau_{L/R}$, for a 37% reduction in amplitude. The value of $L_{S(SAT)}$ is the calculated as $\tau_{L/R}$*R_S.



T_1 Transformer or Ethernet port magnetics assembly incorporating transformer
CT Current transformer or current probe
I_S Secondary winding short-circuit current
I_{GEN} Primary winding current from the generator
G 1.2/50-8/20 combinaison wave surge generator
O Oscilloscope or equivalent recording secondary current, I_S
R_{GEXT} Generator external series resistor

Figure 7-8 – Test circuit for measuring secondary short-circuit current under surge conditions

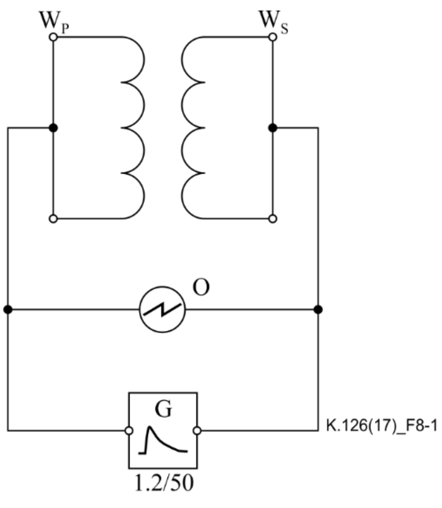
8 Ratings

8.1 Verification

[ITU-T K.95] defines the test circuits and rating verification procedures for the transformer parameters discussed in this clause.

8.2 Rated impulse voltage

The common-mode rated impulse voltage value should be greater than or at least equal to the expected electrical environment. [ITU-T K.95] uses the circuit shown in Figure 8-1 to verify the transformer common-mode rated impulse voltage. After the rated impulse voltage test, the transformer has a further IR test (7.3) to check for any insulation degradation.

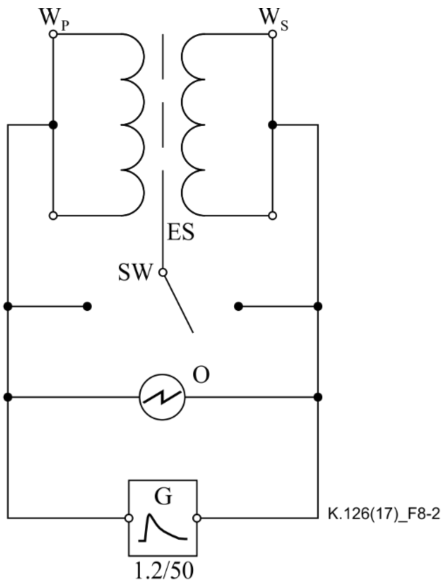


W_P Primary winding
W_S Secondary winding
G 1.2/50 surge generator
O Oscilloscope or equivalent monitoring impulse voltage

Figure 8-1 – Transformer rated impulse voltage test circuit

If the transformer has an electric screen between the primary and secondary windings, two rated impulse voltage test are performed; primary winding to screen and secondary winding to screen. [ITU-T K.95] uses the circuit shown in Figure 8-2 for these rated impulse voltage verifications.

After the rated impulse voltage tests, the transformer has further IR tests (5.3) to check for any insulation degradation.

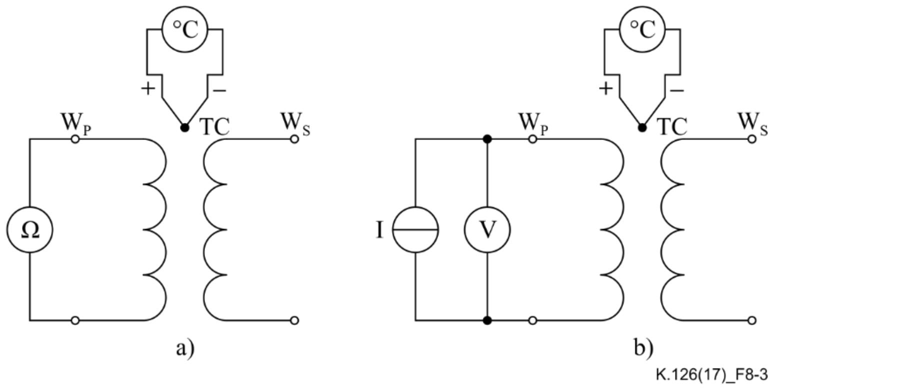


W_P Primary winding
W_S Secondary winding
ES Electric screen
G 1.2/50 surge generator
O Oscilloscope or equivalent monitoring impulse voltage
SW Two position selector switch

Figure 8-2 – Rated impulse voltage test circuit for a transformer with an electric screen

8.3 Rated winding d.c.

This parameter is only relevant under extreme conditions, such as a standard that demands a differential mode power cross test. [ITU-T K.95] uses the circuit shown in Figure 8-3 to verify that the transformer temperature rise is not excessive when conducting the rated value of d.c. Circuit a) measures the pre-test values of winding resistance and circuit b) measures the winding voltage at the rated d.c. and the local ambient temperature of the transformer after thermal equilibrium is reached.



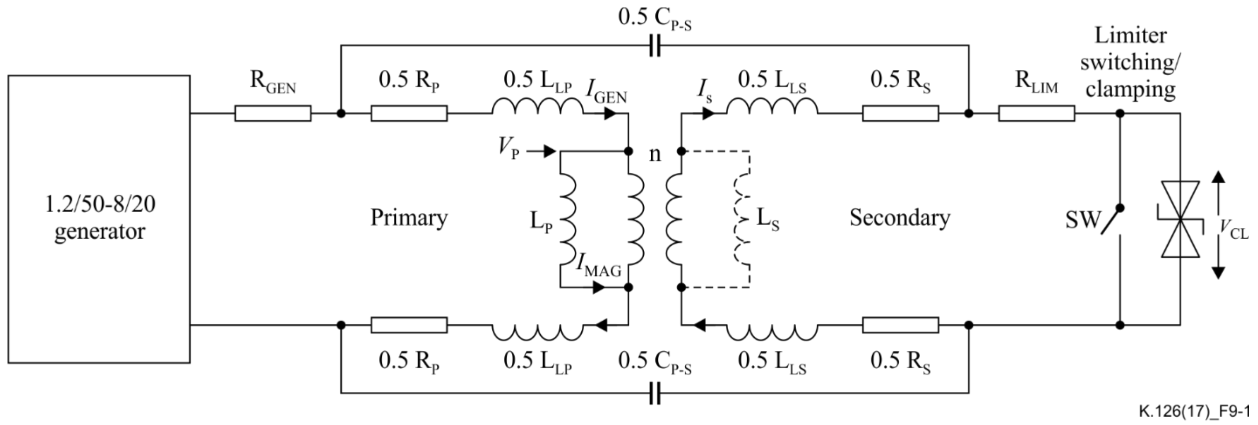
W_P Primary winding
W_S Secondary winding
TC Thermocouple, placed 10 mm ±2 mm from the transformer for sensing the local ambient temperature
°C Meter measuring the local ambient temperature
Ω Ohm meter to measure winding resistance
I Current source set to the winding rated dc, I_{DC}
V Voltmeter to measure winding voltage, V_W

Figure 8-3 – Winding conductor temperature rise test circuit

9 Application examples

9.1 Transformer example

To explain the role of the various isolating transformer parameters, the equivalent circuit shown in Figure 9-1 is used. There are some compromises in the model, such as lumped values for distributed parameters and the nodes to which the equivalent winding capacitances connect.



R_p	Primary winding resistance	R_S	Secondary winding resistance
L_{LP}	Primary leakage inductance	L_{LS}	Secondary leakage inductance
R_{GEN}	Series resistance from generator	R_{LIM}	Series resistance to limiter
V_P	Primary voltage	SW	Switching voltage limiter
C_{P-S}	Inter-winding capacitance	V_{CL}	Clamping limiter voltage
I_{GEN}	Generator current	L_S	Secondary inductance
I_{MAG}	Magnetising current	n	Transformer turns ratio
L_P	Primary magnetising inductance		

Figure 9-1 – Transformer circuit model

Typical values for transformer parameters are given in Table 1.

Table 1 – Typical Figure 9-1 PoE transformer parameter values

Component symbol	Value	Component symbol	Value
R_p	0.9 Ω max. (100 Base-T) 1.4 Ω max. (1000 Base-T)	R_S	0.9 Ω max. (100 Base-T) 1.4 Ω max. (1000 Base-T)
L_{LP}	0.25 µH max.	L_{LS}	0.25 µH max.
L_P	350 µH min. at 8 mA d.c. (100 Base-T) 80 µH min. at 28 mA d.c. (1000 Base-T)	L_S	Similar to L_P
$C_{P–S}$	25 pF typ.	n	1:1

9.2 Common-mode surge

9.2.1 Capacitive surge current

The d*v*/d*t* wavefront of a common-mode voltage surge creates the highest capacitive current, i, as the voltage is changing at its fastest rate ($dv/dt = i/C$). For a typical surge waveform, [b-Maytum, 1994] estimated that the initial rate of rise was three times that of the average given by the peak open-circuit voltage value divided by the front time.

Figure 9-2 shows two situations: normal differential signal conditions; and common-mode surge conditions. The capacitive loops are: the primary to secondary capacitance loops (0.5 $C_{P–S}$); and the

Smith termination network loop [b-Smith] (C_S and C_{PoE}). The extra C_{PoE} capacitor is necessary in PoE designs to block the DC powering voltage of the signal pairs. The peak Smith termination charging current will be less than $C_S \times (dv/dt)_{MAX}$, as the current step is modified to an exponential rise by the $R_S \times C_S$ time constant. Some designs do not use a Smith termination circuit for reasons given in [b-Ardley].

Under normal differential signal conditions, capacitive currents are negligible as there is no common mode signal to drive Smith termination current or any net primary to secondary inter-winding current.

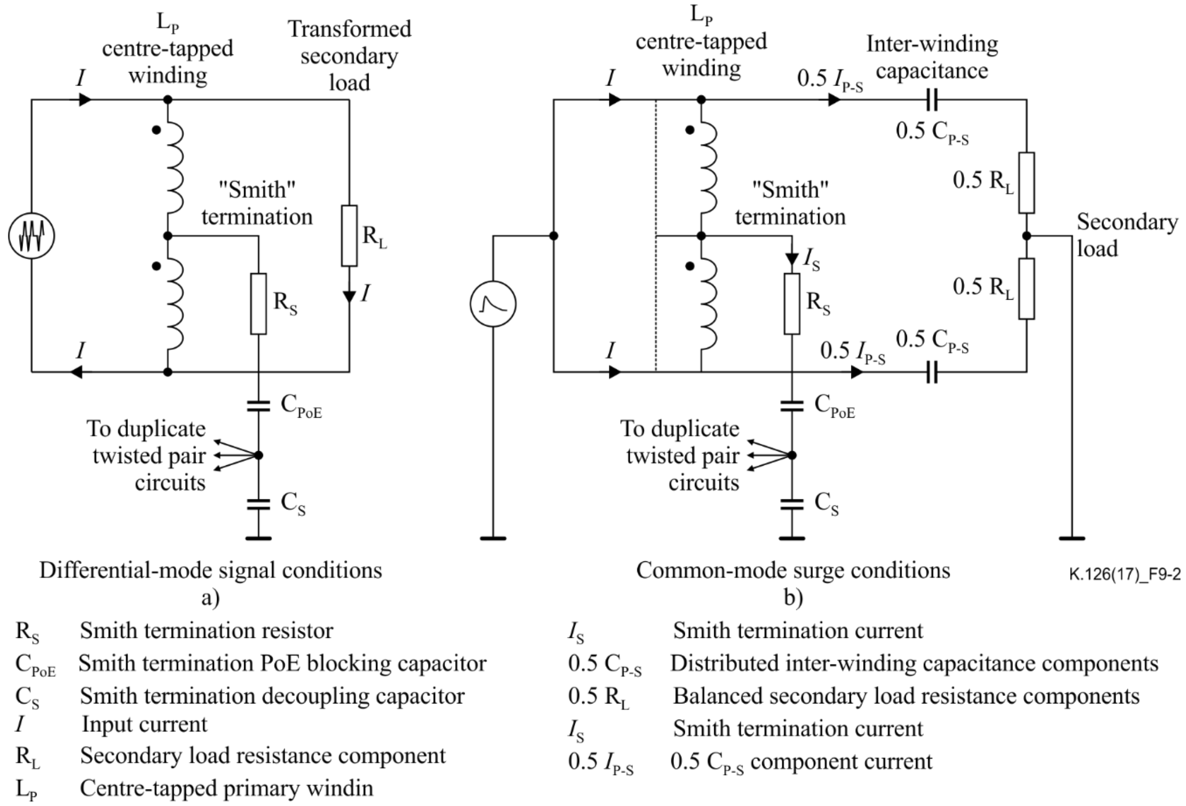


Figure 9-2 – Smith circuit capacitive currents

Under common-mode surge conditions, there will be Smith termination and inter-winding capacitive currents. The typical recommended values for the Smith termination components are; $R_S = 75\ \Omega$, $C_{POE} = 10$ nF 200 V and $C_S = 1$ nF 2 kV. As the impulse test voltage used in [b-IEEE 802.3] is 2.4 kV, the design approach must be that a 2 kV rated capacitor can withstand a temporary overvoltage to 2.4 kV.

Under differential signal conditions, with one signal polarity applied to one end of the centre-tapped primary winding and the opposite signal polarity applied to the other winding end, the primary has high impedance. Under common-mode surge conditions, when both ends of the centre-tapped primary winding have the same polarity applied, there is core flux cancellation making the winding essentially air-cored [b-Pulse]. In this state, the primary winding has negligible impedance and effectively shorts the winding ends and the centre-tap together. This means the common-mode surge voltage from both wires of the signal twisted pair are directly applied to the Smith termination circuit.

Figures 9-3 and 9-4 show the Smith termination overall voltage, V_S, capacitor C_S voltage, V_{CS}, and current, I_S, for a surge delivered by a 1.2/50–8/20 generator charged to 2.5 kV for two twisted pairs and for all four twisted pairs. In the two pair case, with charging via two resistors, the current in one resistor peaks at about 1.9 A. In the four pair case, with charging via four resistors, the current in one resistor peaks at about 1.0 A. Surge measurements made in [b-Chaudhry] show that at surge levels approaching the enhanced level (6 kV), the higher charging currents and the consequent resistive energy tend to cause failure of the termination resistors. The selected resistor energy ratings and capacitor voltage ratings need to be adequate for the chosen electrical surge environment.

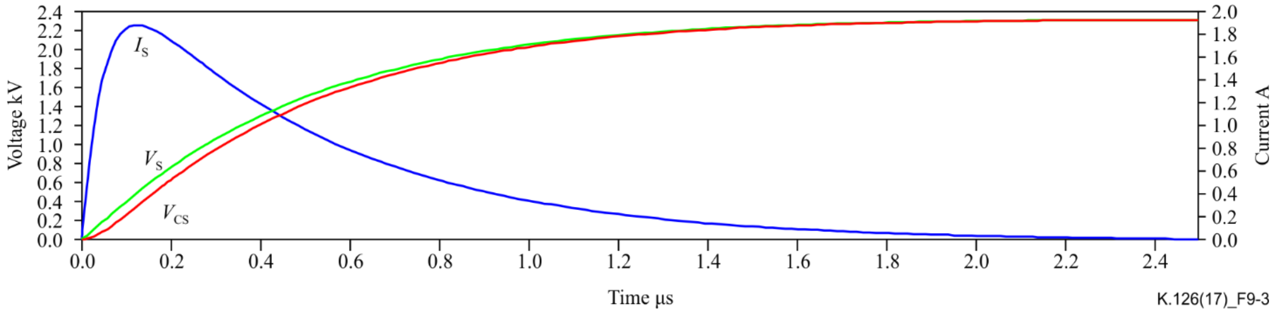


Figure 9-3 – Smith termination voltages and current with two pairs connected

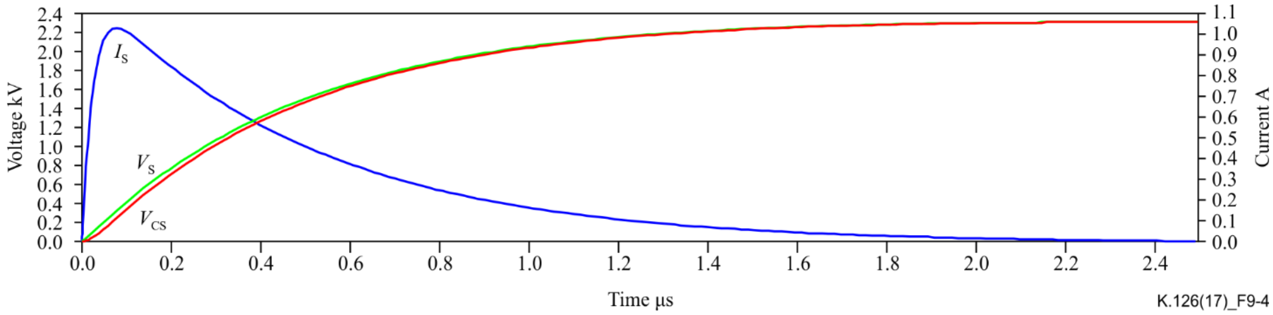


Figure 9-4 – Smith termination voltages and current with four pairs connected

Under common-mode surge conditions, the inter-winding primary–secondary capacitance is charged and discharged. The example equivalent inter-winding capacitance is 10 pF between the primary and the secondary winding starts, together with a second 10 pF between the primary and the secondary winding finishes, see Figure 9-2. Figure 9-5 shows the 10 pF capacitor surge voltage, V_{SURGE}, and current, $0.5I_{P-S}$, for a surge delivered by a 1.2/50–8/20 generator charged to 2.5 kV. The resultant peak capacitive current is just under 50 mA. At the 6 kV enhanced test level, the capacitor current is about 120 mA. This level is not a significant secondary circuit stress, as the current levels caused by differential-mode surges are considerably higher.

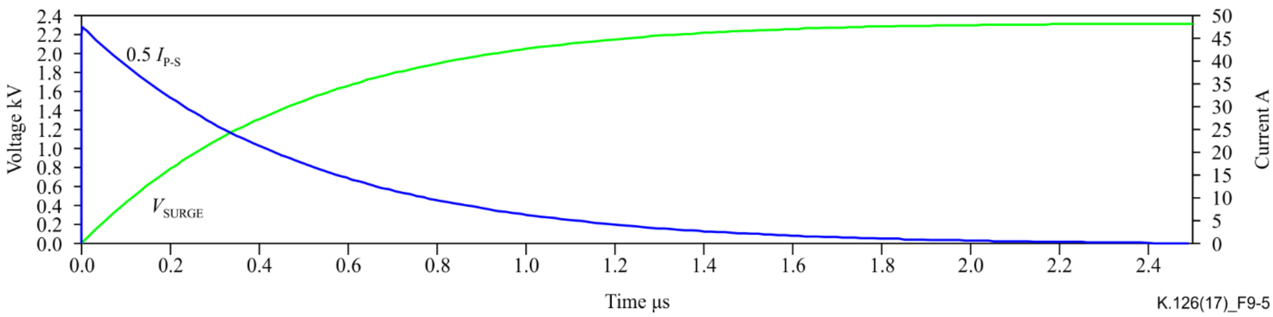


Figure 9-5 – Secondary capacitive current for a 10 pF inter-winding capacitance

9.2.2 Switching voltage limiter discharge current

If a switching voltage limiting function is present by the use of either an external SPD or SPCs in the equipment port, the switching action causes a rapid voltage change, much faster than that which occurs on the surge front. Assuming the SPD and the equipment port meet the IR requirements of 7.3, the rapid voltage decrease is likely to occur at voltages in excess of 700 V.

Figure 9-6 shows the Smith termination current, I_S, for a surge delivered by a 1.2/50–8/20 generator charged to 2.5 kV for two twisted pairs with an 800 V switching voltage limiter on one pair. The peak charging current is 1.9 A as in Figure 9-3, but the discharging current is higher, approaching –7 A.

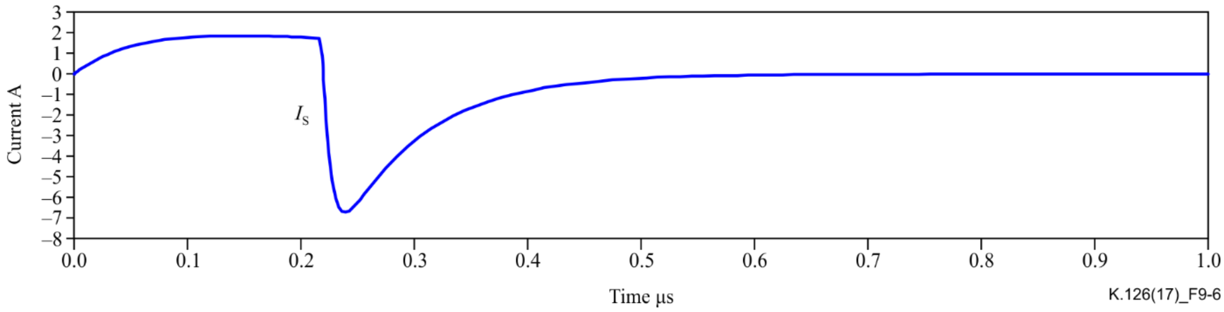


Figure 9-6 – Smith termination discharge current caused by an 800 V switching voltage limiter

Figure 9-7 shows the 10 pF inter-winding capacitor surge voltage, V_{SURGE}, and current, $I_{P–S}/2$, for a surge delivered by a 1.2/50–8/20 generator charged to 2.5 kV with a connected 800 V switching voltage limiter. The resultant peak charging current is just under 50 mA as in Figure 9-5, but the discharging current is higher, reaching a peak of −4.5 A. In practice, the peak current and duration of the discharge current will depend on the switching waveform of the voltage limiter.

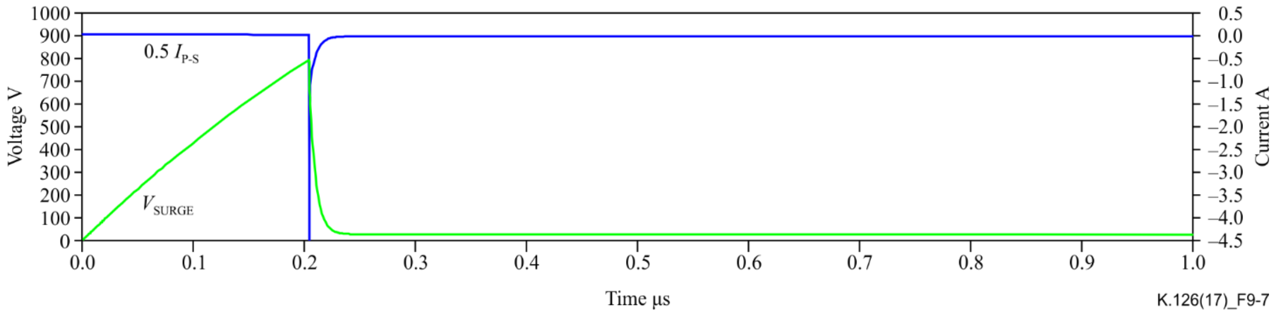


Figure 9-7 – Inter-winding capacitance discharge current caused by an 800 V switching voltage limiter

The operation of a switching voltage limiter effectively shorts the cable conductors to the local functional bonding point and this can nearly double the peak voltage level on the equipment at the other end of the cable [b-Maytum, 2011]. A double voltage result is the same as that caused by the termination mismatch mechanism of an isolating power transformer reflecting the surge waveform back down the line (see Chapter 9 of [b-Hileman]). In addition, asynchronous voltage switching can convert common-mode surges into differential mode surges.

The most elegant approach with the fewest consequences for Ethernet port design is to avoid the need for common-mode switching voltage limiters by using an isolating transformer with a withstand voltage rating greater than or equal to that of the expected electrical environment.

9.3 DC insulation resistance

[b-IEEE 802.3] requires that the Ethernet port IR at 500 V d.c. be 2 MΩ or greater. The test circuits are shown in 7.3. The 500 V d.c. test voltage has two implications.

- Any common-mode voltage limiter must have an operating threshold above 500 V, otherwise the port will fail the IR test.
- The 500 V d.c. test level is higher than the peak voltage of 120 V and 230 V a.c. mains voltages, meaning that a single contact power cross can be withstood without current flow.

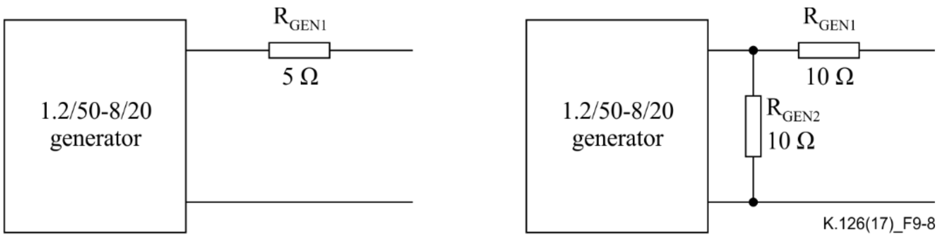
The risk of getting a differential two contact power cross is highly unlikely, making such a test meaningless. Unfortunately many standards still apply old plain old telephone system (POTS) testing techniques to Ethernet ports, resulting in increased costs and probably no field benefits.

9.4 Differential-mode primary winding surge

9.4.1 Impulse generator configuration

For Ethernet, ITU-T has standardized on the 1.2/50–8/20 generator. In the open circuit mode, it produces the 1.2/50 voltage impulse use for testing insulation [b-IEC 60060-1]. In terms of a common-mode current delivered to a low-impedance port, it has been found that a series resistor of 5 Ω gives a typical I^2t value of 12 A^2s, which is of the same order of magnitude as the value needed to cause observed field failures of fuses (rated at 15 A^2s) and printed wiring tracks.

The [b-ITU-T K.117] Ethernet common-mode generator configuration is shown in Figure 9-8 a). If a differential-mode surge is created by breakdown or voltage limiter operation at one cable end twisted pair and the same happens at the other end of the cable, the surge current is shared between the two conductors of the twisted pair. In this case, the differential surge current into the port will be half the common-mode surge current. Figure 9-8 b) shows how this is implemented using the common-mode generator voltage settings. Half the generator output current is taken by the shunt resistor R_{GEN2} (10 Ω) and the other half of the generator current is applied to the equipment port via series resistor R_{GEN1} (10 Ω). Together the two resistors form a generator load of 5 Ω, making the surge current waveshape the same for common-mode and differential-mode surges.



a) Common-mode impulse generator configuration

b) Differential-mode impulse generator configuration

Figure 9-8 – Common-mode and differential-mode impulse generator configurations

9.4.2 Saturating core transformer surge conditions

Under differential surge conditions, see Figure 9-10, a saturating core signal transformer has a secondary winding surge let-through current, I_S, that is typically triangular and can be described by three surge waveform parameters of front, peak and decay as follows:

– Waveform **front** due to transformer linear surge current transfer from primary winding to secondary winding, the current ratio being set by the transformer's primary to secondary turn's ratio, n.

– Waveform **peak** determined by the transformer core saturation event setting the peak secondary current, the event time being set by the transformer's volt–second (V·s) value for core saturation.

– Waveform **decay** due to the saturated core secondary winding stored energy dump, the current waveform of which is set by the transformer saturated core winding inductance, the secondary leakage inductance, the peak secondary current, the secondary winding resistance and the secondary load impedance.

Figure 9-9 shows an example waveform with the three waveform parameters indicated.

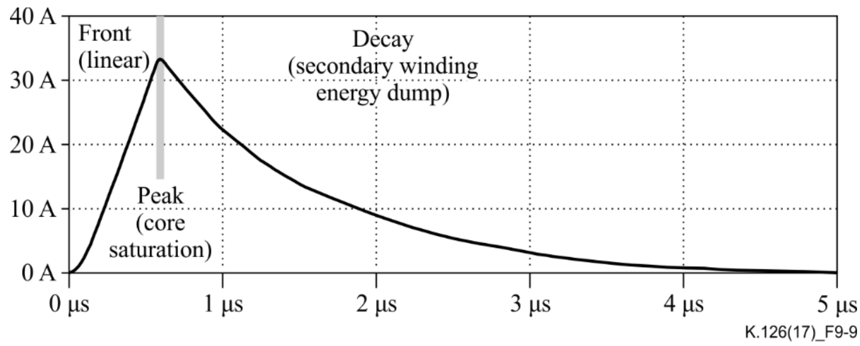
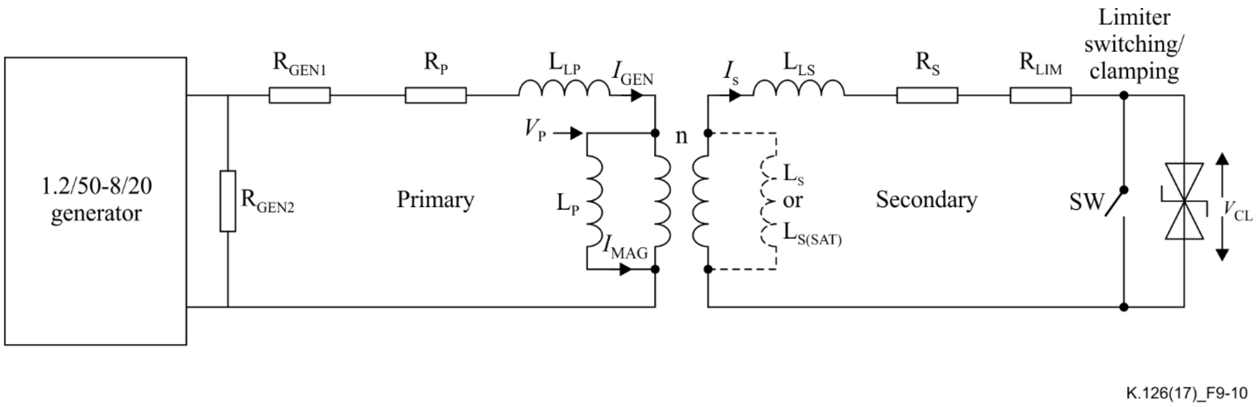


Figure 9-9 – Example waveform of transformer secondary winding differential surge let-through current



R_p	Primary winding resistance	R_S	Secondary winding resistance
L_{LP}	Primary leakage inductance	L_{LS}	Secondary leakage inductance
R_{GEN}	Series resistance from generator	R_{LIM}	Series resistance to limiter
V_P	Primary voltage	SW	Switching voltage limiter
$C_{P\text{-}S}$	Inter-winding capacitance	V_{CL}	Clamping limiter voltage
I_{GEN}	Generator current	L_S	Secondary inductance
I_{MAG}	Magnetising current	n	Transformer turns ratio
L_P	Primary magnetising inductance	$L_{S(SAT)}$	Saturated core secondary inductance

Figure 9-10 – Effective secondary circuit for differential surge

9.4.3 Secondary current front

During this period, the transformer operates in a linear mode, transforming the generator current in the primary to secondary winding current. The intrinsic secondary circuit voltage is the sum of the inductive voltage due to the rising current in the leakage inductance, any voltage limiter threshold voltage and the resistive voltages across the secondary resistance, the external secondary resistance and the effective limiter characteristic resistance.

9.4.4 Secondary current peak

The transformer action effectively ends when the transformer core saturates as shown by the primary magnetizing current, I_{MAG}, dramatically increasing when the transformer volt-second value has been reached, see Figure 9-11.

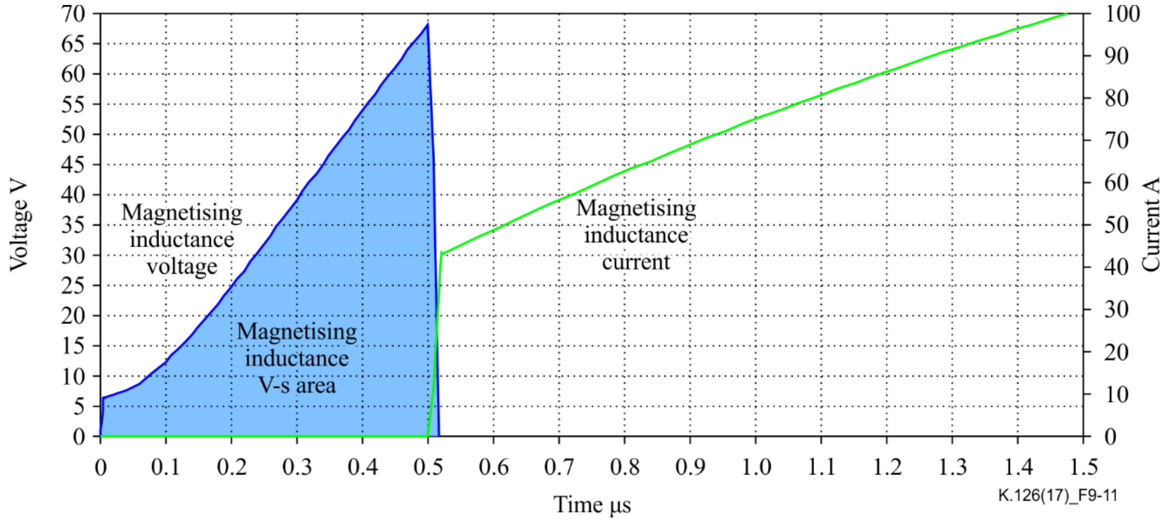
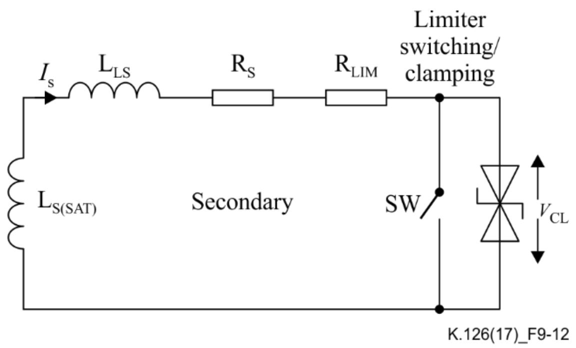


Figure 9-11 – Transformer primary magnetizing inductance voltage and current

The peak secondary current, $I_{S(PEAK)}$ at saturation will be roughly the surge generator dI/dt multiplied by the time to reach core saturation, about 0.5 µs in this example.

9.4.5 Secondary current decay

During the waveform decay period, when the saturated core decouples the primary and secondary windings and the effective secondary circuit becomes the transformer saturated core winding inductance, $L_{S(SAT)}$, the established secondary current, $I_{S(PEAK)}$, the secondary winding resistance, R_S, the limiter series resistance, R_{LIM}, and the switching or clamping limiter threshold voltage and characteristic resistance are as shown in Figure 9-12. The stored energy of $0.5[L_{S(SAT)} + L_{LS})]I_{S(PEAK)}{}^2$ is discharged into the described circuit loop.



R_S	Secondary winding resistance component	$L_{S(SAT)}$	Saturated core secondary inductance component
R_{LIM}	Series resistance to limiter component	L_{LS}	Secondary leakage inductance component
SW	Switching voltage limiter	V_{CL}	Clamping limiter voltage
I_S	Secondary current		

Figure 9-12 – Secondary current decay circuit after core saturation

There are two factors controlling the current decay rate: the ratio of the inductive components to the resistive components (L/R); and the threshold voltage of the voltage limiter (V_{CL}/L).

9.4.6 Basic and enhanced test levels

Figure 9-13 shows an example of the different secondary currents at the ITU-T basic (2.5 kV) and enhanced (6 kV) levels.

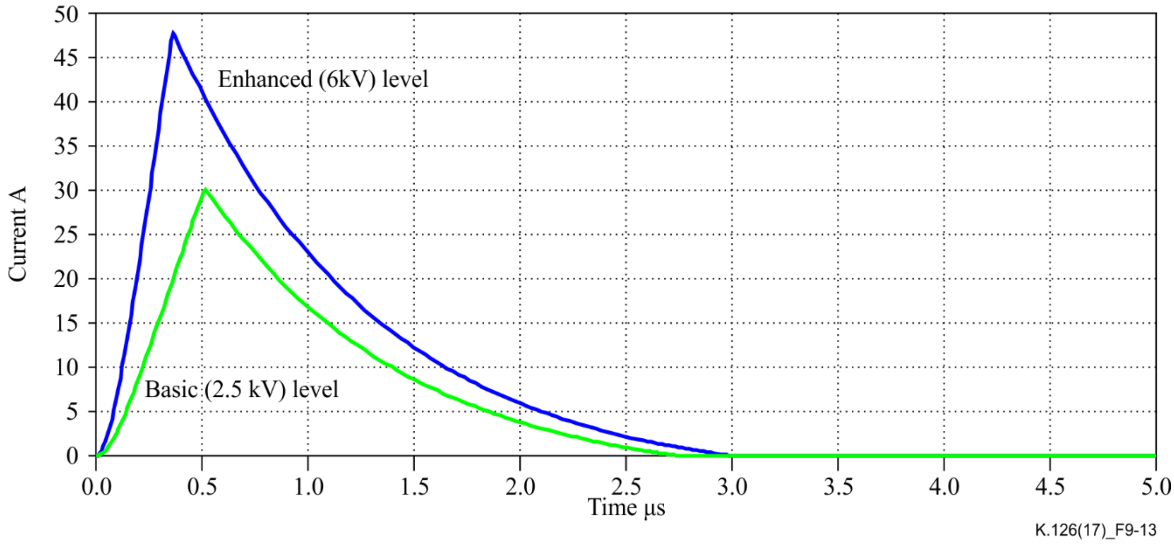


Figure 9-13 – Basic and enhanced secondary current levels

It is perhaps not intuitive that increasing the test voltage by 6/2.5 = 2.4 times only increases the peak secondary current by 47.5/30 = 1.6 times. The reason for this is that the transformer volt second parameter is fixed and this means that the peak current to generator voltage relationship is like a square root law $(6/2.5)^{0.5} = 1.55$. The bulk of the energy deposited in the voltage limiter comes from the decay period and the secondary protection components should be selected accordingly.

9.4.7 Alternative impulse generators

[b-GR-1089] and [b-ATIS-0600036], originating from the USA, offer a <2/>10[1] as an alternative to the 1.2/50–8/20 generator. The open-circuit generator voltages are set at 800 V, which is lower than the ITU-T 2.5 kV (basic) and 6 kV (enhanced) levels, and these lower voltage levels will increase the generator and equipment interaction. To make both generators produce the same short circuit current of 100 A at the 800 V setting, a 6 Ω series resistor is placed in the 1.2/50–8/20 generator output.

The circuit generator, I_{GEN}, and secondary, I_S, currents of the <2/>10 and 1.2/50–8/20 configurations are shown in Figure 9-14.

1 The waveshape designator normally quotes the nominal wavefront time and nominal time to half value. Where the waveshape quotes the maximum front time and the minimum time to half value the < and > symbols are used before the times. For more information on this type of waveshape see [b-ITU-T K.96].

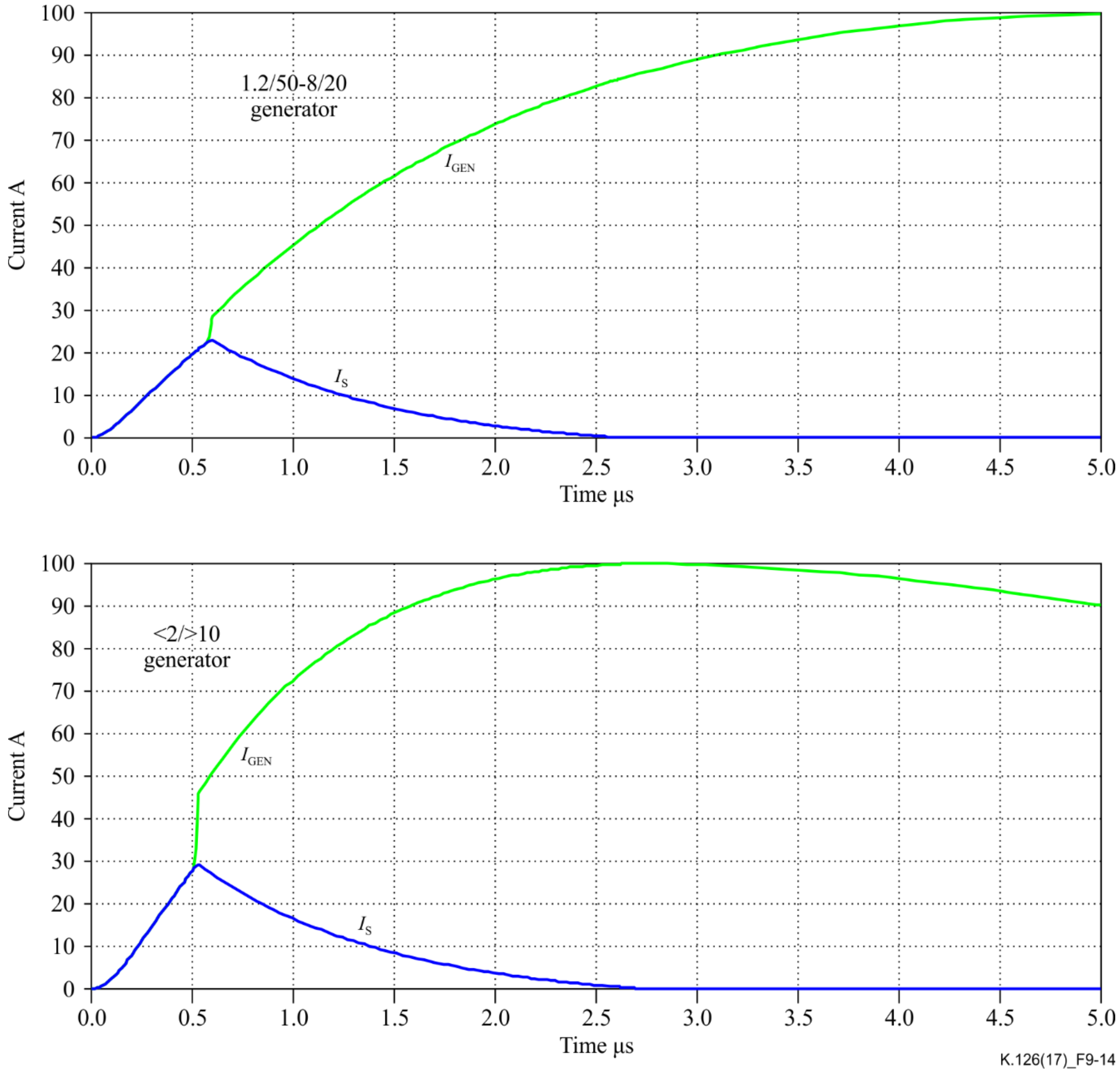


Figure 9-14 – Generator (green trace) and secondary (blue trace) currents for 1.2/50–8/20 and <2/>10 generators

There are three obvious differences in the waveforms:

– The 1.2/50–8/20 generator current has a slower rate of rise.

– The 1.2/50–8/20 generator current has a smaller current step at core saturation due to its higher output impedance.

– The <2/>10 secondary peak current is higher due to its faster rate of rise.

The <2/>10 generator secondary circuit stress is the highest. The two generator stresses can be equalized by raising the 1.2/50–8/20 generator open-circuit voltage to about 1 200 V because the resultant initial d*I*/d*t* of the front then equals that of the <2/>10 generator. Figure 9-15 shows in detail the difference in the secondary currents and, for comparison, the ITU-T basic level secondary current. It shows that the secondary currents of the <2/>10 and ITU-T basic are very similar and the 1.2/50–8/20 peak secondary current is some 6 A lower. In selecting a generator for the differential testing of a transformer primary winding, the key parameter is the front initial d*I*/d*t*.

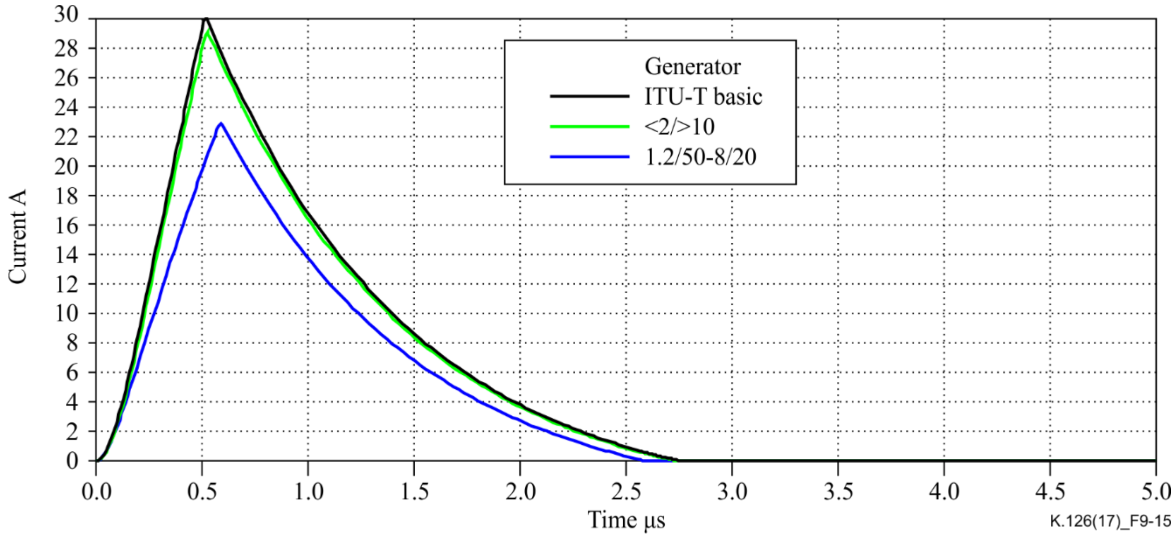


Figure 9-15 – Comparison of secondary currents from three different configurations

9.5 Rated impulse voltage

The common-mode rated impulse voltage value should be greater than or at least equal to the expected electrical environment. Often it is not realized that to guarantee the rated impulse voltage value the component must be capable of withstanding a substantially higher voltage value.

Table 2 lists the preferred values for the transformer insulation rated impulse voltage together with the corresponding impulse withstand test voltage. To verify that the insulation rated impulse voltage is at least its specified value, the applied impulse withstand test voltage must be higher. The ratio of impulse withstand to rated impulse voltage used in Table 2 is 1.17 for voltages less than 4 kV and 1.23 for voltages of 4 kV and above in accordance with [b-IEC 60664-1] and [b-IEC/TR 60664-2-1].

Table 2 – Impulse withstand test voltage for rated impulse voltage

Rated impulse voltage (kV)	Impulse withstand voltage[a] (kV)
2.4 (see Note)	2.8
2.5	2.92
6	7.39
12	14.8
15	18.5
25	30.8

NOTE – The transformer impulse withstand voltage corresponding to the 1.2/50, 2.4 kV rated impulse voltage used for the equipment port test of [b-IEEE 802.3] is 2.8 kV.

[a] The 1.2/50 peak voltage amplitude tolerance shall be ±5% in accordance with [b-IEC/TR 60664-2-1].

To satisfy [b-IEEE 802.3], the rated impulse voltage should be at least 2.4 kV or preferably 2.5 kV. This requirement will meet basic Ethernet port needs. In more severe electrical environments, such as home networking, an enhanced 6 kV rated impulse value is recommended. In special cases, values of 12 kV and above may be necessary.

9.6 Rated winding d.c.

Generally, the primary resistance value, represented by R_P, and, for centre-tapped primaries, the resistive matching of the two primary halves, is of more interest than the winding current capability. The primary resistance represents a power loss for PoE applications, as the d.c. powering current flows through the transformer primary or in some cases a centre-tapped choke. The resistive match is important to avoid a net d.c. flux in the core, which can change the winding inductance.

As pointed out in clause 8.3, rated current is only needed in extreme circumstances. The only other reason to specify this parameter is to match standardized wire current ratings. For example, at the time of writing, specifying a maximum wire current of 0.75 A d.c. per conductor at 60 °C is under consideration,[2] which would result in a centre-tap rated current of 1.5 A d.c.

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[2] In Draft International Standard IEC 60364-7-716, *Low-Voltage electrical installations – Part 7-716: Requirements for special installations or locations – DC power distribution over Information Technology Cable Infrastructure*.

Annex A

Use of isolating transformers for a.c. power and signal applications

(This annex forms an integral part of this Recommendation.)

For mitigation measures of lightning surge, there are some methods such as appropriate earthing and bonding, addition of SPD and isolation. Lightning isolation transformers (LITs) are components for isolation mitigation measure. This Annex shows the mitigation measures by isolation of surges and the application methods for LITs to improve resistibility against overvoltage at the design step.

A.1 Application of LITs to equipment that requires isolation

The surge mitigation measure for equipment that requires to be isolated is to prevent surges from entering with LITs and not SPDs.

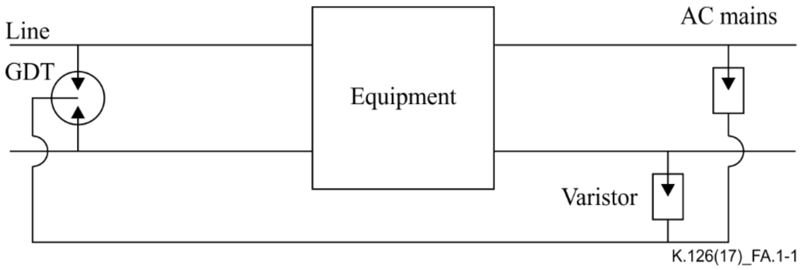

Figure A.1-1 – Surge mitigation measure with SPDs

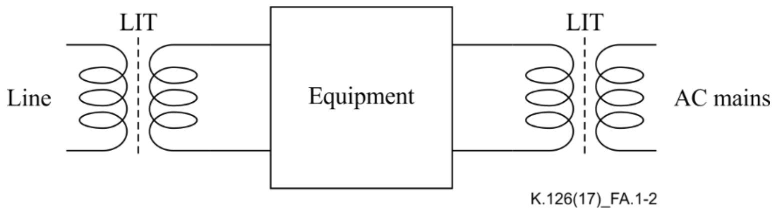

Figure A.1-2 – Surge mitigation measure with LITs

A.2 Application of LITs on communication line for high-speed signal transmission

When SPDs as surge mitigation measure apply to high speed signal transmission such as Ethernet, it may cause the decrease of LCL and the increase of transmission loss. In such cases, the use of LIT is recommended to prevent surges from entering.

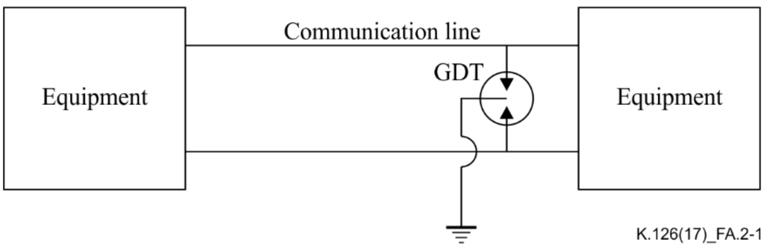

Figure A.2-1 – Surge mitigation measure with SPDs

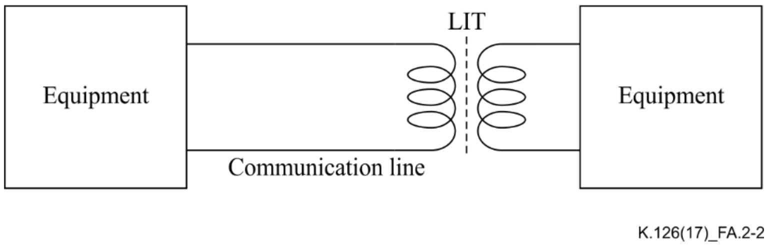

Figure A.2-2 – Surge mitigation measures with LITs

A.3 LITs for equipment with low resistibility

The operating voltage and speed are important for SPDs used for the equipment with low resistibility. When the operating voltage cannot be set lower, the insertion of resistors on transmission lines makes SPD operate efficiently. However, they cause the increase of transmission loss. LITs realize surge mitigation without influence on signal transmission by considering signal characteristics.

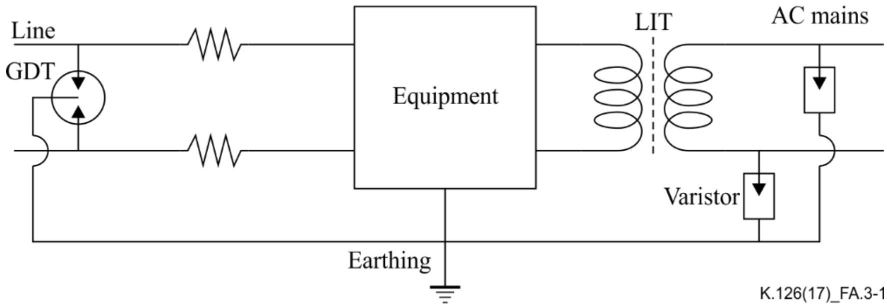

Figure A.3-1 – Example of surge protection coordination with resistors

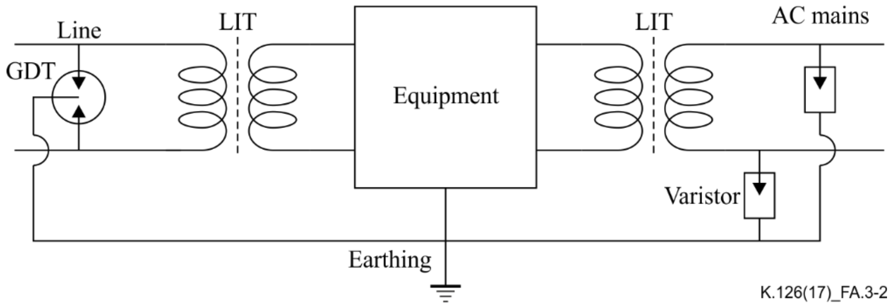

Figure A.3-2 – Surge mitigation measure with LITs

Bibliography

[b-ITU-T K.96] Recommendation ITU-T K.96 (2014), *Surge protective components: Overview of surge mitigation functions and technologies.*

[b-ITU-T K.117] Recommendation ITU-T K117 (2016), *Primary protector parameters for the surge protection of equipment Ethernet ports.*

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