International Telecommunication Union

ITU-T G.8262/Y.1362

TELECOMMUNICATION
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Amendment 2

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Recommendation ITU-T G.8262/Y.1362

Timing characteristics of a synchronous Ethernet equipment slave clock (EEC)

Amendment 2

Summary

Amendment 2 to Recommendation ITU-T G.8262/Y.1362 adds Appendix III "List of Ethernet interfaces applicable to synchronous Ethernet". It also clarifies a sentence in clause 9.1.1.

History

Edition	Recommendation	Approval	Study Group
1.0	ITU-T G.8262/Y.1362	2007-08-13	15
1.1	ITU-T G.8262/Y.1362 (2007) Amend. 1	2008-04-29	15
1.2	ITU-T G.8262/Y.1362 (2007) Amend. 2	2010-01-13	15

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In some areas of information technology which fall within ITU-T's purview, the necessary standards are prepared on a collaborative basis with ISO and IEC.

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Recommendation ITU-T G.8262/Y.1362

Timing characteristics of a synchronous Ethernet equipment slave clock (EEC)

Amendment 2

1 Clause 9.1.1

Change the following paragraph in clause 9.1.1 from:

"While suitable test signals that check conformance to the mask in Figure 6 are being studied, test signals with a sinusoidal phase variation can be used, according to the levels in Table 8."

To:

"Suitable test signals that check conformance to the mask in Figure 6 are being studied. Test signals with a sinusoidal phase variation can be used, according to the levels in Table 8, to check conformance to the mask in Figure 5."

2 Appendix III

Add Appendix III "List of Ethernet interfaces applicable to synchronous Ethernet" comprising the following text:

Appendix III

List of Ethernet interfaces applicable to synchronous Ethernet

(This appendix does not form an integral part of this Recommendation)

A list of all Ethernet interfaces listed in [IEEE 802.3] published in 2008 is provided in Table III.1. It specifies the Ethernet interfaces which are valid for synchronous Ethernet operation. Other interfaces may exist; the list of interfaces is not exhaustive and might be updated.

The following considerations have been taken into consideration for the generation of this list.

CSMA/CD

The IEEE 802.3-2008 specifies two operating modes: half-duplex and full-duplex modes.

The original Ethernet interfaces were developed for a single medium that was shared between multiple end stations using the CSMA/CD mechanism. Most interfaces use separate media (or separate carriers) for bidirectional communication between two end stations. The use of half-duplex operation on such bidirectional, point-to-point media serves to mimic the behaviour of legacy shared media operation. In all cases, there is no difference in PHY behaviour between half-duplex and full-duplex modes. The half-duplex functionality is controlled by the media access control sublayer (MAC) and only affects packet transport at layer 2 and above.

Interfaces titled CSMA/CD may be used for the purposes of synchronous Ethernet in all cases where the media is point-to-point.

Constant signal

The interface must permanently transport a signal.

This signal must be coded so that there is a guarantee of transitions so that the clock can be recovered. This is achieved by the 64B/66B encoding in some 10G interfaces; DSQ-128 (2 x 2 pair, PAM-16) signalling for 10G over twisted pair copper; 8B/10B encoding in some 1G interfaces and 10G over 4 channels of fibre or copper; 4D-PAM-5 encoding for 1G over twisted pair copper interfaces; 4B/5B encoding for some 100M interfaces; and MLT-3 for 100M over twisted pair copper interfaces.

All IEEE 802.3 point-to-point PHYs that operate at speed of 100 Mbit/s or greater use constant signalling.

Master/slave

Some bidirectional interfaces are designed to have one side, designated as the clock master, acting as the clock generator, the other side as the slave, which is forced to recover the clock.

Such a configuration will only support unidirectional synchronous Ethernet. Such conditions can be announced under supervision of the Ethernet synchronization message channel (ESMC) process, as defined in [ITU-T G.8264] where synchronous Ethernet reduced interfaces are introduced. For such interfaces, the master/slave resolution should be forced by station management as defined by the appropriate clause in [IEEE 802.3], in accordance with the synchronization network architecture. ESMC reduced interface status should be synchronized with master/slave status.

Two examples of master/slave clock operation are 1000BASE-T and 10GBASE-T.

Auto-negotiation

The auto-negotiation mechanism defined for some sets of PHYs is used to find the highest mutually supported mode of operation for two partners at link start-up time. The algorithm will always favour a higher speed compared to a lower speed and full-duplex to half-duplex. Because the negotiation happens at link start-up, it should be compatible with synchronous Ethernet but may not be compatible with the synchronization distribution plan. Note that the negotiation is an option for some PHY types and the supported PHY speed and duplex may be forced by management.

Note that there are some cases where auto-negotiation could appear during operation, e.g., during an upgrade. Auto-negotiation must not have any impact on rates and clocks to be compatible with synchronous Ethernet.

Physical loopback

All physical loopback functionalities specified on full-duplex links that interrupt the link for test/check "in-service" are not compatible with synchronous Ethernet. Thus, they should be only allowed during the link set-up.

Point-to-multipoint

Some PHY interfaces are designed for point-to-multipoint operation over passive optical networks. Such links use intermittent signalling for the upstream direction but may be suitable for unidirectional synchronous Ethernet.

Miscellaneous

Some of the older PHY types are rarely used and need not be considered, for example two PHY types are defined for use over DSL.

Implementation issues

Some interfaces transmit signals over parallel cables or fibres. These interfaces use one clock source for all physical lanes, but the recovered clock (and reference point for timestamping) may vary depending on the definition of multi-lane operation. It is not clear at this point whether further definition will be required for the operation of synchronous Ethernet over these interfaces.

Based on the above considerations, Table III.1 lists the PHY interfaces specified by [IEEE 802.3] and designates which ones may be considered for synchronous Ethernet compatibility, which should not be considered and which may be unidirectional only.

Table III.1 – List of Ethernet interfaces eligible to synchronous Ethernet

PHY	Description	IEEE 802.3 clause	Coding	Synchronous Ethernet capable
10BASE2	10 Mbit/s coaxial	10	Manchester, intermittent	No
10BASE5	*10 Mbit/s coaxial*	*8*	*Manchester, intermittent*	No (Note 1)
10BASE-F	10 Mbit/s fibre	15	NRZ, intermittent	No
10BASE-FP	*10 Mbit/s fibre, star*	*16*	*NRZ, intermittent*	No (Note 1)
10BASE-T	10 Mbit/s TP copper	14	Manchester, intermittent	No
100BASE-BX10	100 Mbit/s bidi fibre	58, 66	4B/5B	Yes
100BASE-FX	100 Mbit/s fibre	24, 26	4B/5B	Yes
100BASE-LX10	100 Mbit/s fibre	58, 66	4B/5B	Yes
100BASE-T2	*100 Mbit/s TP copper*	*32*	*PAM-5*	No (Note 1)
100BASE-T4	*100 Mbit/s TP copper*	*23*	*8B6T*	No (Note 1)
100BASE-TX	100 Mbit/s TP copper	24, 25	MLT-3	Yes
1000BASE-BX10	1 Gbit/s bidi fibre	59, 66	8B/10B	Yes
1000BASE-CX	1 Gbit/s twinax	39	8B/10B	Yes
1000BASE-KX	1 Gbit/s backplane	70	8B/10B	Yes
1000BASE-LX	1 Gbit/s fibre	38	8B/10B	Yes
1000BASE-PX	1 Gbit/s PON	38	8B/10B	Unidirectional
1000BASE-SX	1 Gbit/s fibre	38	8B/10B	Yes
1000BASE-T	1 Gbit/s TP copper	40	4D-PAM5	Unidirectional
10BROAD36	*10 Mbit/s coax*	*11*	*BPSK*	No (Note 1)
10GBASE-CX4	10 Gbit/s 4x twinax	54	8B/10B	Yes
10GBASE-ER	10 Gbit/s fibre	49, 52	64B/66B	Yes
10GBASE-EW	10 Gbit/s fibre	50, 52	64B/66B	Yes
10GBASE-KR	10 Gbit/s backplane	72	64B/66B	Yes

Table III.1 – List of Ethernet interfaces eligible to synchronous Ethernet

PHY	Description	IEEE 802.3 clause	Coding	Synchronous Ethernet capable
10GBASE-KX4	10 Gbit/s 4x backplane	71	8B/10B	Yes
10GBASE-LR	10 Gbit/s fibre	49, 52	64B/66B	Yes
10GBASE-LRM	10 Gbit/s fibre	68	64B/66B	Yes
10GBASE-LW	10 Gbit/s fibre	50, 52	64B/66B	Yes
10GBASE-LX4	10 Gbit/s 4λ fibre	50, 52	8B/10B	Yes
10GBASE-SR	10 Gbit/s fibre	49, 52	64B/66B	Yes
10GBASE-SW	10 Gbit/s fibre	50, 52	64B/66B	Yes
10GBASE-T	10 Gbit/s TP copper	55	DSQ-128	Yes (Note 2)
10PASS-TS	>10 Mbit/s DSL	61, 62	DMT	No
1BASE-5	*1 Mbit/s TP copper*	*12*	*Manchester*	No (Note 1)
2BASE-TL	>2 Mbit/s DSL	61, 63	PAM	No
10/1GBASE-PR	10 Gbit/s/1 Gbit/s PON	76	64B/66B / 8B/10B	Unidirectional
10GBASE-PR	10 Gbit/s PON	76	64B/66B	Unidirectional
40GBASE-KR4	40 Gbit/s 4x backplane	84	64B/66B	Yes
40GBASE-CR4	40 Gbit/s 4x twinax	85	64B/66B	Yes
40GBASE-SR4	40 Gbit/s 4x fibre	86	64B/66B	Yes
40GBASE-LR4	40 Gbit/s 4λ fibre	87	64B/66B	Yes
100GBASE-CR10	100 Gbit/s 10x twinax	85	64B/66B	Yes
100GBASE-SR10	100 Gbit/s 10x fibre	86	64B/66B	Yes
100GBASE-LR4	100 Gbit/s 4λ fibre	88	64B/66B	Yes
100GBASE-ER4	100 Gbit/s 4λ fibre	88	64B/66B	Yes

NOTE 1 – These rows (highlighted in italics) are deprecated.

NOTE 2 – 10GBASE-T may support dual master or master/slave clocking (i.e., unidirectional synchronous Ethernet).

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