International Telecommunication Union

ITU-T

TELECOMMUNICATION
STANDARDIZATION SECTOR
OF ITU

G.8251

(09/2010)

SERIES G: TRANSMISSION SYSTEMS AND MEDIA, DIGITAL SYSTEMS AND NETWORKS

Packet over Transport aspects – Quality and availability targets

The control of jitter and wander within the optical transport network (OTN)

Recommendation ITU-T G.8251

ITU-T G-SERIES RECOMMENDATIONS

TRANSMISSION SYSTEMS AND MEDIA, DIGITAL SYSTEMS AND NETWORKS

INTERNATIONAL TELEPHONE CONNECTIONS AND CIRCUITS	G.100–G.199
GENERAL CHARACTERISTICS COMMON TO ALL ANALOGUE CARRIER-TRANSMISSION SYSTEMS	G.200–G.299
INDIVIDUAL CHARACTERISTICS OF INTERNATIONAL CARRIER TELEPHONE SYSTEMS ON METALLIC LINES	G.300–G.399
GENERAL CHARACTERISTICS OF INTERNATIONAL CARRIER TELEPHONE SYSTEMS ON RADIO-RELAY OR SATELLITE LINKS AND INTERCONNECTION WITH METALLIC LINES	G.400–G.449
COORDINATION OF RADIOTELEPHONY AND LINE TELEPHONY	G.450–G.499
TRANSMISSION MEDIA AND OPTICAL SYSTEMS CHARACTERISTICS	G.600–G.699
DIGITAL TERMINAL EQUIPMENTS	G.700–G.799
DIGITAL NETWORKS	G.800–G.899
DIGITAL SECTIONS AND DIGITAL LINE SYSTEM	G.900–G.999
MULTIMEDIA QUALITY OF SERVICE AND PERFORMANCE – GENERIC AND USER-RELATED ASPECTS	G.1000–G.1999
TRANSMISSION MEDIA CHARACTERISTICS	G.6000–G.6999
DATA OVER TRANSPORT – GENERIC ASPECTS	G.7000–G.7999
PACKET OVER TRANSPORT ASPECTS	G.8000–G.8999
Ethernet over Transport aspects	G.8000–G.8099
MPLS over Transport aspects	G.8100–G.8199
Quality and availability targets	**G.8200–G.8299**
Service Management	G.8600–G.8699
ACCESS NETWORKS	G.9000–G.9999

For further details, please refer to the list of ITU-T Recommendations.

Recommendation ITU-T G.8251

The control of jitter and wander within the optical transport network (OTN)

Summary

Recommendation ITU-T G.8251 specifies the maximum network limits of jitter and wander that shall not be exceeded and the minimum equipment tolerance to jitter and wander that shall be provided at any relevant interfaces which are based on the optical transport network (OTN).

The requirements for the jitter and wander characteristics that are specified in this Recommendation must be adhered to in order to ensure interoperability of equipment produced by different manufacturers and a satisfactory network performance.

History

Edition	Recommendation	Approval	Study Group
1.0	ITU-T G.8251	2001-11-29	15
1.1	ITU-T G.8251 (2001) Cor. 1	2002-06-13	15
1.2	ITU-T G.8251 (2001) Amend. 1	2002-06-13	15
1.3	ITU-T G.8251 (2001) Cor. 2	2008-05-22	15
1.4	ITU-T G.8251 (2001) Amend.2	2010-01-13	15
2.0	ITU-T G.8251	2010-09-22	15

FOREWORD

The International Telecommunication Union (ITU) is the United Nations specialized agency in the field of telecommunications, information and communication technologies (ICTs). The ITU Telecommunication Standardization Sector (ITU-T) is a permanent organ of ITU. ITU-T is responsible for studying technical, operating and tariff questions and issuing Recommendations on them with a view to standardizing telecommunications on a worldwide basis.

The World Telecommunication Standardization Assembly (WTSA), which meets every four years, establishes the topics for study by the ITU-T study groups which, in turn, produce Recommendations on these topics.

The approval of ITU-T Recommendations is covered by the procedure laid down in WTSA Resolution 1.

In some areas of information technology which fall within ITU-T's purview, the necessary standards are prepared on a collaborative basis with ISO and IEC.

NOTE

In this Recommendation, the expression "Administration" is used for conciseness to indicate both a telecommunication administration and a recognized operating agency.

Compliance with this Recommendation is voluntary. However, the Recommendation may contain certain mandatory provisions (to ensure, e.g., interoperability or applicability) and compliance with the Recommendation is achieved when all of these mandatory provisions are met. The words "shall" or some other obligatory language such as "must" and the negative equivalents are used to express requirements. The use of such words does not suggest that compliance with the Recommendation is required of any party.

INTELLECTUAL PROPERTY RIGHTS

ITU draws attention to the possibility that the practice or implementation of this Recommendation may involve the use of a claimed Intellectual Property Right. ITU takes no position concerning the evidence, validity or applicability of claimed Intellectual Property Rights, whether asserted by ITU members or others outside of the Recommendation development process.

As of the date of approval of this Recommendation, ITU had not received notice of intellectual property, protected by patents, which may be required to implement this Recommendation. However, implementers are cautioned that this may not represent the latest information and are therefore strongly urged to consult the TSB patent database at http://www.itu.int/ITU-T/ipr/.

Table of Contents

		Page
1	Scope	1
2	References	2
3	Definitions	3
4	Abbreviations and acronyms	3
5	Network limits for the maximum output jitter and wander at an OTUk interface	5
	5.1 Network limits for jitter	5
	5.2 Network limits for wander	6
6	Jitter and wander tolerance of network interfaces	6
	6.1 Jitter and wander tolerance of OTN interfaces	6
	6.2 Jitter and wander tolerance of client interfaces	11
Annex A – Specification of the ODUk clock (ODC)		13
	A.1 Scope	13
	A.2 Applications	17
	A.3 Frequency accuracy	17
	A.4 Pull-in and pull-out ranges	17
	A.5 Noise generation	18
	A.6 Noise tolerance	22
	A.7 Jitter transfer	22
	A.8 Transient response	24
Appendix I – Relationship between network interface jitter requirements and input jitter tolerance		26
	I.1 Network interface jitter requirements	26
	I.2 Input jitter tolerance of network equipment	27
Appendix II – Effect of OTN on the distribution of synchronization via STM-N and synchronous Ethernet clients		29
	II.1 Introduction	29
	II.2 Provisional synchronization reference chain	29
	II.3 Synchronization network limit	30
	II.4 Variable channel memory	31
	II.5 Maximum buffer hysteresis	31
Appendix III – Hypothetical reference model (HRM) for 3R regenerator jitter accumulation		33
Appendix IV – 3R regenerator jitter accumulation analyses		34
	IV.1 Introduction	34
	IV.2 Model 1	34
	IV.3 Model 2	55
	IV.4 Jitter generation of regenerators using parallel serial conversion	56

Page

Appendix V – Additional background on demapper (ODCp) phase error and demapper wideband jitter generation requirements 58
V.1 Introduction 58
V.2 Demapper phase error 58
V.3 Demapper wideband jitter generation due to gaps produced by fixed overhead in OTUk frame 60
Appendix VI – OTN atomic functions 63
VI.1 Introduction 63
Appendix VII – Hypothetical reference models (HRMs) for CBRx (SDH and synchronous Ethernet client) and ODUj[/i] payload jitter and short-term wander accumulation 65
VII.1 Introduction 65
VII.2 OTN hypothetical reference models 65
VII.3 Impact of the insertion of OTN islands in the ITU-T G.803 synchronization reference chain 67
Appendix VIII – CBRx and ODUj[/i] payload jitter and short-term wander accumulation analyses 70
VIII.1 Introduction 70
VIII.2 Simulation model 70
VIII.3 Jitter and short-term wander simulation results 77
Bibliography 113

Introduction

In an optical transport network (OTN), jitter and wander accumulate on transmission paths according to the jitter and wander generation and transfer characteristics of each respective equipment interconnected. This equipment may be, for example, 3R regenerators, client mappers, and client demappers/desynchronizers.

An excessive amount of jitter and wander can adversely affect both digital (e.g., by generation of bit errors, frame slips and other abnormalities) and analogue baseband signals (e.g., by unwanted phase modulation of the transmitted signal). The consequences of such impairment will, in general, depend on the particular service that is being carried and the terminating or adaptation equipment involved.

It is therefore necessary to set limits on the maximum magnitude of jitter and wander, and the corresponding minimum jitter and wander tolerance at network interfaces, in order to guarantee a proper quality of the transmitted signals and a proper design of the equipment.

These network limits are independent of the particular service that is being carried.

Recommendation ITU-T G.8251

The control of jitter and wander within the optical transport network (OTN)

1 Scope

The scope of this Recommendation is to define the parameters and the relevant limits that satisfactorily control the amount of jitter and wander present at the OTN network-node interface (NNI).

OTN network interfaces, to which this Recommendation is applicable, are defined in terms of bit rates and frame structures in [ITU-T G.709]; the relevant equipment characteristics are described in [ITU-T G.798] and the optical characteristics in [ITU-T G.959.1] or [ITU-T G.693]. Additional information regarding the architecture of the OTN is found in [ITU-T G.872].

The network limits given in clause 5, OTN interface tolerance specifications given in clause 6.1, and OTN equipment interface specifications given in Annex A apply at or refer to the OTUk interface. The relevant bit rates for these specifications are the OTUk bit rates. Note that some of the other requirements in this Recommendation, e.g., the demapper clock (ODCp), asynchronous mapper clock (ODCa), and bit-synchronous mapper clock (ODCb) requirements in Annex A, apply to other interfaces and other bit rates (i.e., the demapper resides in the sink adaptation function between the ODUkP and CBR, ODUj[/i] or ODUkP/ODUj_A client, while the asynchronous and bit-synchronous mapper clocks reside in the source adaptation function between the ODUkP and client). In this Recommendation the term 'clock', when used in ODU clock (ODC), refers to a frequency source. Note that this Recommendation contains requirements for both non-OTN CBRx clients mapped into ODUk and ODUj[/i] clients multiplexed into ODUk (k > j).

The OTN physical layer is not required to transport network synchronization. More precisely, neither the ODUk nor any layers below it are required to transport synchronization. Network synchronization distribution is a function of the client layer, e.g., SDH.

[ITU-T G.825] specifies the jitter and wander requirements for SDH clients, and any SDH signal (which must meet [ITU-T G.825]) is suitable for providing synchronization (see [ITU-T G.803]). SDH clients must meet [ITU-T G.825] requirements for both asynchronous and bit-synchronous mappings.

[ITU-T G.8261] specifies the jitter and wander requirements of synchronous Ethernet for providing synchronization (see Annex D of [ITU-T G.8261]). Synchronous Ethernet clients must meet [ITU-T G.8261] requirements for both GMP and bit-synchronous mappings.

Jitter and wander requirements for SDH networks are specified in [ITU-T G.825]. Jitter and wander requirements for PDH and synchronization networks are specified in [ITU-T G.823], for networks based on the first level bit rate of 2048 kbit/s, and in [ITU-T G.824] for networks based on the first-level bit rate of 1544 kbit/s.

The jitter and wander control philosophy is based on the need:

– to recommend a maximum network limit that should not be exceeded at any relevant OTN NNI;

– to recommend a consistent framework for the specification of individual digital equipment (i.e., jitter and wander transfer, tolerance and generation requirements);

– to provide sufficient information and guidelines for organizations to measure and study jitter and wander accumulation in any network configuration.

Note that there may exist hybrid network element (NE) types that contain SDH, Ethernet, and/or OTN atomic functions. For such hybrid NEs, it may not be possible to access the respective ports to make measurements to verify compliance with the requirements in this Recommendation. Measurements to verify compliance for hybrid NE types is outside the scope of this Recommendation.

2 References

The following ITU-T Recommendations and other references contain provisions which, through reference in this text, constitute provisions of this Recommendation. At the time of publication, the editions indicated were valid. All Recommendations and other references are subject to revision; users of this Recommendation are therefore encouraged to investigate the possibility of applying the most recent edition of the Recommendations and other references listed below. A list of the currently valid ITU-T Recommendations is regularly published. The reference to a document within this Recommendation does not give it, as a stand-alone document, the status of a Recommendation.

[ITU-T G.693] Recommendation ITU-T G.693 (2006), *Optical interfaces for intra-office systems*.

[ITU-T G.707] Recommendation ITU-T G.707/Y.1322 (2000), *Network node interface for the synchronous digital hierarchy (SDH)*.

[ITU-T G.709] Recommendation ITU-T G.709/Y.1331 (2009), *Interfaces for the optical transport network (OTN), including its Amendment 1 (2010)*.

[ITU-T G.783] Recommendation ITU-T G.783 (2006), *Characteristics of synchronous digital hierarchy (SDH) equipment functional blocks, including its amendments*.

[ITU-T G.798] Recommendation ITU-T G.798 (2010), *Characteristics of optical transport network hierarchy equipment functional blocks*.

[ITU-T G.803] Recommendation ITU-T G.803 (2000), *Architecture of transport networks based on the synchronous digital hierarchy (SDH)*.

[ITU-T G.810] Recommendation ITU-T G.810 (1996), *Definitions and terminology for synchronization networks*.

[ITU-T G.811] Recommendation ITU-T G.811 (1997), *Timing characteristics of primary reference clocks*.

[ITU-T G.813] Recommendation ITU-T G.813 (2003), *Timing characteristics of SDH equipment slave clocks (SEC)*.

[ITU-T G.823] Recommendation ITU-T G.823 (2000), *The control of jitter and wander within digital networks which are based on the 2048 kbit/s hierarchy*.

[ITU-T G.824] Recommendation ITU-T G.824 (2000), *The control of jitter and wander within digital networks which are based on the 1544 kbit/s hierarchy*.

[ITU-T G.825] Recommendation ITU-T G.825 (2000), *The control of jitter and wander within digital networks which are based on the synchronous digital hierarchy (SDH), including its Amendment 1 (2008)*.

[ITU-T G.872] Recommendation ITU-T G.872 (2001), *Architecture of optical transport networks*.

[ITU-T G.959.1] Recommendation ITU-T G.959.1 (2009), *Optical transport network physical layer interfaces*.

[ITU-T G.8261] Recommendation ITU-T G.8261/Y.1361 (2008), *Timing and synchronization aspects in packet networks.*

[IEEE 802.3] IEEE Std. 802.3-2008, *Information Technology – Local and Metropolitan Area Networks – Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications*.

[IEEE 802.3ba] IEEE Std. 802.3ba-2010, *Information Technology – Local and Metropolitan Area Networks – Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications – Amendment 4: Media Access Control Parameters, Physical Layers and Management Parameters for 40 Gb/s and 100 Gb/s Operation*.

3 Definitions

The terms and definitions used in this Recommendation that pertain to timing and jitter are contained in [ITU-T G.810] and [ITU-T G.825]. The terms and definitions used in this Recommendation that pertain to the OTN are contained in [ITU-T G.709], [ITU-T G.798] and [ITU-T G.872]. The terms and definitions used in this Recommendation that pertain to SDH are contained in [ITU-T G.707], [ITU-T G.783] and [ITU-T G.803].

4 Abbreviations and acronyms

This Recommendation uses the following abbreviations:

3R Reamplification, Reshaping, and Retiming

A Adaptation

AI Adapted Information

AIS Alarm Indication Signal

AMP Asynchronous Mapping Procedure

AP Access Point

CBR Constant Bit Rate

CI Characteristic Information

CK Clock

CP Connection Point

D Data

EEC synchronous Ethernet Equipment Clock

FC-x Fibre Channel of rate x

FEC Forward Error Correction

GMP Generic Mapping Procedure

HRM Hypothetical Reference Model

MC Master Clock

MTIE Maximum Time Interval Error

NE	Network Element
NNI	Network-Node Interface
OA	Optical Amplifier
OCh	Optical Channel with full functionality
OChr	Optical Channel with reduced functionality
OCI	Open Connection Indication
ODC	ODUk Clock
ODCx	ODUk Clock of type "x", where x is "a", "b", "r", or "p"
ODU	Optical channel Data Unit
ODUk	Optical channel Data Unit-k
ODUkP	ODUk Path
ODUkT	ODUk Tandem connection
OTL	Optical channel Transport Lane
OMS	Optical Multiplex Section
OPSM	Optical Physical Section Multilane
OPU	Optical channel Payload Unit
OPUk	Optical channel Payload Unit-k
OTM	Optical Transport Module
OTN	Optical Transport Network
OTS	Optical Transmission Section
OTU	Optical channel Transport Unit
OTUk	completely standardized Optical channel Transport Unit-k
PDH	Plesiochronous Digital Hierarchy
PI	Proportional plus Integral
PLL	Phase-Locked Loop
PMD	Polarization Mode Dispersion
ppm	parts per million
PRBS	Pseudo-Random Binary Sequence
PRC	Primary Reference Clock
PSD	Power Spectral Density
rms	root mean square
RS	Reed-Solomon
SDH	Synchronous Digital Hierarchy
SEC	SDH Equipment Clock
Sk	Sink

So	Source
SSU	Synchronization Supply Unit
STM	Synchronous Transport Module
STM-N	Synchronous Transport Module – level N
TCP	Termination Connection Point
TDEV	Time Deviation
TVAR	Time Variance
UI	Unit Interval
UIpp	Unit Interval peak-to-peak
UTC	Coordinated Universal Time
VCO	Voltage-Controlled Oscillator
WFM	White Frequency Modulation
WPM	White Phase Modulation

5 Network limits for the maximum output jitter and wander at an OTUk interface

The jitter and wander limits given in this clause are the maximum permissible levels at OTUk interfaces within an OTN. The OTUk interface is just below the OCh/OTUk adaptation function in Figure 1-3 of [ITU-T G.798]. One example of this interface is the input to a 3R regenerator (sink) or output from a 3R regenerator (source).

NOTE – The OTUk is precisely defined in [ITU-T G.709]; essentially, it is the digital signal that is mapped into the Optical Channel (OCh). The OTUk bit rate is essentially the line rate associated with the OCh and respective wavelength that the OCh is assigned to. The OTUk bit rates are given in Table 7-1 of [ITU-T G.709], and are equal to the inverses of the bit periods given in Table 5.1-1.

5.1 Network limits for jitter

Table 5.1-1 gives the maximum permissible levels of jitter at OTUk interfaces. Jitter as measured over a 60-second interval shall not exceed the limits given in Table 5.1-1, when using the specified measurement filters. The limits shall be met for all operating conditions and regardless of the amount of equipment preceding the interface. In general, these network limits are compatible with the minimum tolerance to jitter that all equipment input ports are required to provide. Guidelines for the derivation of the parameters values of Table 5.1-1 are given in Appendix I.

There is a close relationship between network limits and input tolerance such that the jitter measurement filter cut-off frequencies used in Table 5.1-1 have the same values as the jitter tolerance mask corner frequencies used in clause 6.1. Appendix I provides further information about this relationship.

The high-pass measurement filters of Table 5.1-1 have a first-order characteristic and a roll-off of 20 dB/decade. The low-pass measurement filters for OTU1, OTU2, and OTU3 have a maximally-flat, Butterworth characteristic and a roll-off of –60 dB/decade.

Table 5.1-1 – Maximum permissible jitter at OTUk interfaces

Interface	Measurement bandwidth, –3 dB frequencies (Hz)	Peak-to-peak amplitude (UIpp)
OTU1	5 k to 20 M	1.5
	1 M to 20 M	0.15
OTU2	20 k to 80 M	1.5
	4 M to 80 M	0.15
OTU3	20 k to 320 M	6.0
	16 M to 320 M	0.18
OTL3.4 (OTU3 Multilane) per lane	FFS	FFS
	4 M measured up to fourth-order Bessel-Thomson filter defined in clause 87.8.9 of [IEEE 802.3ba]	Each lane according to clause 87.7.2, Table 87-8, and clause 87.8.11 of [IEEE 802.3ba]
OTL4.4 (OTU4 Multilane) per lane	FFS	FFS
	10 M measured up to fourth-order Bessel-Thomson filter defined in clause 88.8.8 of [IEEE 802.3ba]	Each lane according to clause 88.8.10, Table 88-13 of [IEEE 802.3ba]

NOTE – OTU1 $1\ \text{UI} = \frac{238}{(255)(2.48832)}\text{ns} = 375.1\,\text{ps}$

OTU2 $1\ \text{UI} = \frac{237}{(255)(9.95328)}\text{ns} = 93.38\,\text{ps}$

OTU3 $1\ \text{UI} = \frac{236}{(255)(39.81312)}\text{ns} = 23.25\,\text{ps}$

OTL3.4 $1\ \text{UI} = \frac{4\times 236}{(255)(39.81312)}\text{ns} = 92.98\,\text{ps}$ per lane

OTL4.4 $1\ \text{UI} = \frac{4\times 227}{(255)(99.5328)}\text{ns} = 35.77\,\text{ps}$ per lane

5.2 Network limits for wander

OTUk interfaces are not synchronization interfaces. None of the ODUk clocks are significant sources of wander. There is no need for specification of network wander limits.

6 Jitter and wander tolerance of network interfaces

6.1 Jitter and wander tolerance of OTN interfaces

This clause specifies the jitter and wander tolerance for OTUk input ports. This is the minimum jitter and wander that must be tolerated at the input to the OCh/OTUk_A_Sk and OPSM/OTUk_A_Sk atomic function. This represents, for example, the jitter and wander tolerance for a 3R regenerator. The input ports of all equipment must be capable of accommodating levels of jitter and wander up to at least the minimum limits defined in clauses 6.1.1, 6.1.2, 6.1.3, and 6.1.4 in order to ensure that, in general, any equipment can be connected to any appropriate interface within a network.

NOTE 1 – As stated above, both the jitter and wander tolerance requirements apply at the OTUk input port, which is the input to the OCh/OTUk_A_Sk or the OPSM/OTUk_A_Sk atomic function. However, while the requirements apply at this interface, they are not all driven by this atomic function. For example, the high-band jitter tolerance requirement (i.e., the tolerance above the highest frequency breakpoint, which is 1 MHz for OTU1, 4 MHz for OTU2 and OTL3.4 lane of the OTU3 Multilane, 16 MHz for OTU3, and 10 MHz for an OTL4.4 lane of the OTU4 Multilane) is driven by the wideband clock recovery circuit in the OCh/OTUk_A_Sk atomic function; however, the wideband jitter tolerance requirement (i.e., the tolerance between 5 kHz and 100 kHz for OTU1 and between 20 kHz and 400 kHz for OTU2 and OTU3) is driven by the ODCr in the OTUk/ODUk_A_So and OTUk/ODUk_A_Sk atomic functions.

The jitter and wander tolerance of an OTUk interface indicates the minimum level of phase noise that the input port shall accommodate whilst:

- not causing any alarms;
- not causing any slips or loss of lock in the clock recovery phase-locked loop; and
- not causing any bit errors in excess of those allowed by an equivalent 1 dB optical power penalty.

The limit of tolerable input jitter is measured by the 1 dB optical power penalty method as follows:

The optical input power is reduced until a BER of 10^{-10} is reached. Then, the power is increased by 1 dB and jitter is applied to the input signal. The amount of jitter that results in BER of 10^{-10} is the limit of tolerable input jitter. If the system uses FEC, this shall be disabled for the measurement when using an external bit error detector. Alternatively, BER may be measured by leaving the FEC enabled and counting the number of corrected bit errors per unit time.

NOTE 2 – This definition is subject to further study, taking into account the effects of, e.g., optical amplifiers (OA), polarization mode dispersion (PMD), and forward error correction (FEC).

All OTUk input ports of equipment shall be able to tolerate an OCh_AI_D signal that has:

a) optical characteristics of [ITU-T G.959.1] or [ITU-T G.693],

b) a frequency offset (relative to the nominal value) within the range defined in clause A.3, and

c) a sinusoidal phase deviation having an amplitude-frequency relationship, defined in the following clauses, which indicates the appropriate limits for the different interfaces.

In principle, these requirements shall be met regardless of the information content of the digital signal. However, for test purposes, the content of the signal with jitter and wander modulation should be a structured test sequence as defined in [ITU-T G.709].

For convenience of testing, the required tolerance is defined in terms of the peak-to-peak amplitude and frequency of sinusoidal jitter which modulates a digital test pattern. It is important to recognize that this test condition is not, in itself, intended to be representative of the type of jitter found in practice in a network.

Guidance on the measurement set-up for input jitter and wander tolerance is provided in Appendix III of [ITU-T G.823].

Requirements for jitter and wander tolerance for each OTUk rate are given in the following subclauses. These requirements specify the minimum levels of jitter that must be accommodated at an OTUk interface.

6.1.1 OTU1 jitter and wander tolerance

The level of sinusoidal jitter that must be accommodated by OTU1 interfaces is specified in Table 6.1-1 and illustrated in Figure 6.1-1. A phase-locked loop with corner frequency greater than or equal to 5 kHz that can tolerate jitter and wander indicated by the 20 dB/decade sloped portion of

the mask between 500 Hz and 5 kHz will also tolerate jitter and wander indicated by an extension of this sloped region to lower frequencies, because such jitter and wander is within the bandwidth of the phase-locked loop. OTU1 interfaces must tolerate this jitter and wander but, for practical reasons, it is not required to measure them below 500 Hz.

Table 6.1-1 – OTU1 input sinusoidal jitter tolerance limit

Frequency *f* (Hz)	**Peak-to-peak amplitude (UIpp)**
$500 < f \leq 5$ k	$7500\ f^{-1}$
5 k $< f \leq 100$ k	1.5
100 k $< f \leq 1$ M	$1.5 \times 10^{5} f^{-1}$
1 M $< f \leq 20$ M	0.15

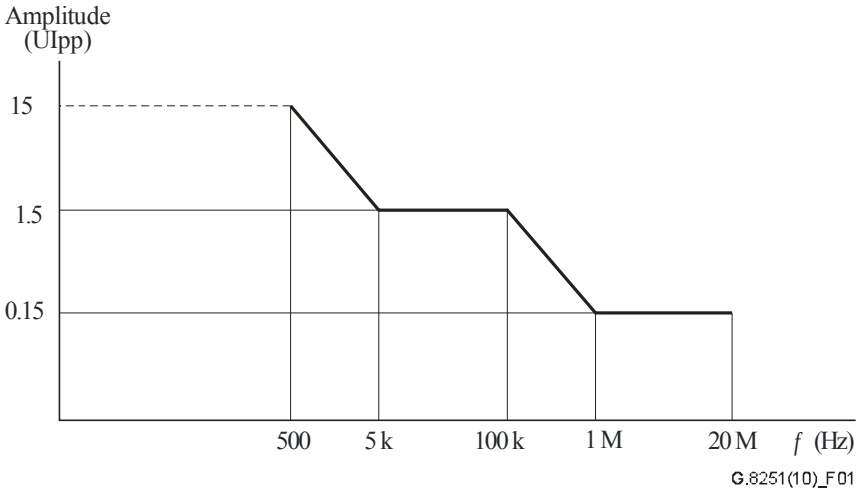


Figure 6.1-1 – OTU1 input sinusoidal jitter tolerance limit

6.1.2 OTU2 jitter and wander tolerance

The level of sinusoidal jitter that must be accommodated by OTU2 interfaces is specified in Table 6.1-2 and illustrated in Figure 6.1-2. A phase-locked loop with corner frequency greater than or equal to 20 kHz that can tolerate jitter and wander indicated by the 20 dB/decade sloped portion of the mask between 2 kHz and 20 kHz will also tolerate jitter and wander indicated by an extension of this sloped region to lower frequencies, because such jitter and wander is within the bandwidth of the phase-locked loop. OTU2 interfaces must tolerate this jitter and wander but, for practical reasons, it is not required to measure them below 2 kHz.

Table 6.1-2 – OTU2 input sinusoidal jitter tolerance limit

Frequency *f* (Hz)	**Peak-to-peak amplitude (UIpp)**
2 k $< f \leq 20$ k	$3.0 \times 10^{4}\ f^{-1}$
20 k $< f \leq 400$ k	1.5
400 k $< f \leq 4$ M	$6.0 \times 10^{5}\ f^{-1}$
4 M $< f \leq 80$ M	0.15

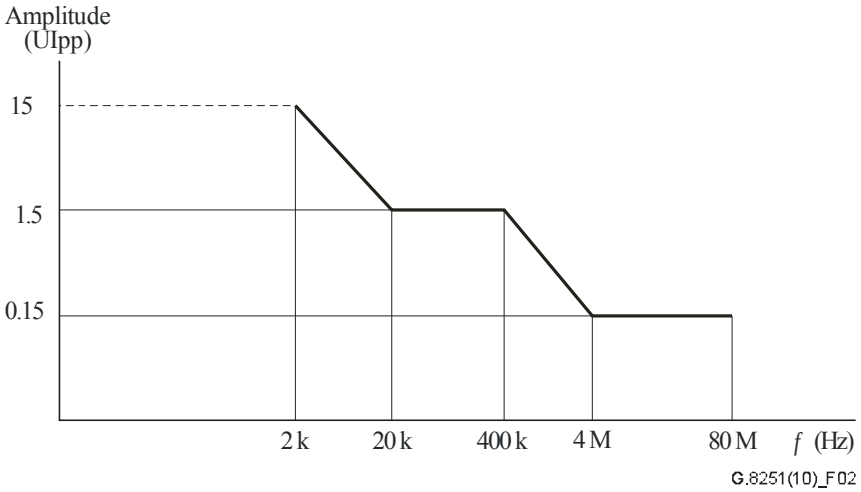


Figure 6.1-2 – OTU2 input sinusoidal jitter tolerance limit

6.1.3 OTU3 jitter and wander tolerance

The level of sinusoidal jitter that must be accommodated by OTU3 interfaces is specified in Table 6.1-3 and illustrated in Figure 6.1-3. A phase-locked loop with corner frequency greater than or equal to 20 kHz that can tolerate jitter and wander indicated by the 20 dB/decade sloped portion of the mask between 8 kHz and 20 kHz will also tolerate jitter and wander indicated by an extension of this sloped region to lower frequencies, because such jitter and wander is within the bandwidth of the phase-locked loop. OTU3 interfaces must tolerate this jitter and wander but, for practical reasons, it is not required to measure it below 8 kHz.

Table 6.1-3 – OTU3 input sinusoidal jitter tolerance limit

Frequency *f* (Hz)	**Peak-to-peak amplitude (UIpp)**
8 k < *f* ≤ 20 k	$1.2 \times 10^5 f^{-1}$
20 k < *f* ≤ 480 k	6.0
480 k < *f* ≤ 16 M	$2.88 \times 10^6 f^{-1}$ UI
16 M < *f* ≤ 320 M	0.18

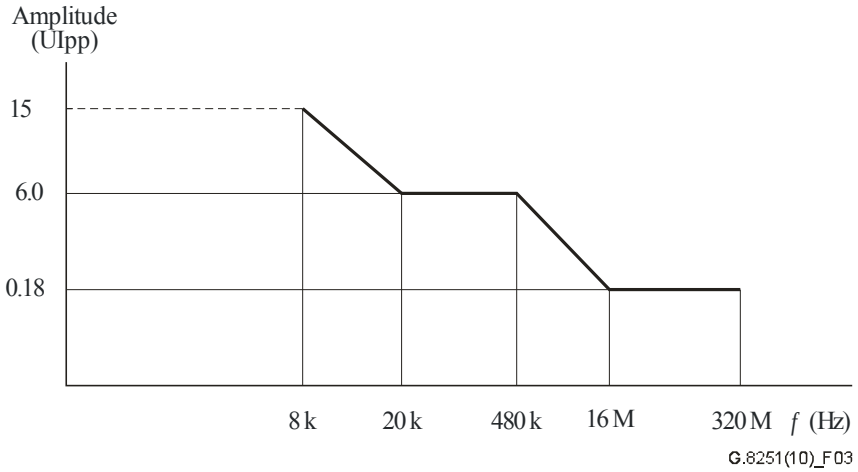


Figure 6.1-3 – OTU3 input sinusoidal jitter tolerance limit

The jitter tolerance of the OTU3 multilane interface is given in Table 6.1-4 and illustrated in Figure 6.1-4.

Table 6.1-4 – OTL3.4 per lane input sinusoidal jitter tolerance limit

Frequency *f* (Hz)	**Peak-to-peak amplitude (UIpp)**
FFS	FFS
FFS	FFS
FFS	FFS
4 M < *f* ≤ measured up to fourth-order Bessel-Thomson filter defined in [IEEE 802.3ba], clause 87.8.9.	Each lane according to clause 87.7.2, Table 87-8, and clause 87.8.11 of [IEEE 802.3ba]

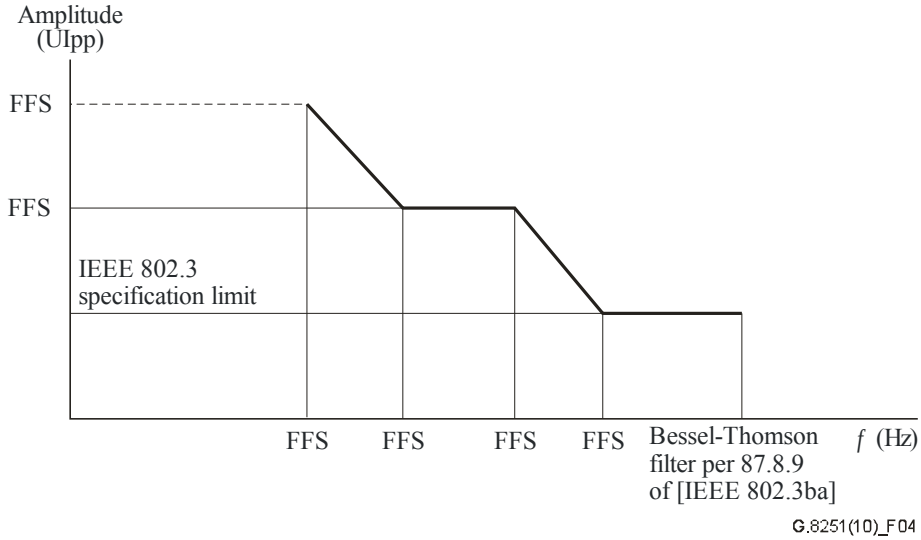


Figure 6.1-4 – OTL3.4 per lane input sinusoidal jitter tolerance limit

6.1.4 OTU4 jitter and wander tolerance

The level of jitter that must be accommodated by the OTU4 multilane interface is given in Table 6.1-5 and illustrated in Figure 6.1-5.

Table 6.1-5 – OTL4.4 per lane input sinusoidal jitter tolerance limit

Frequency *f* (Hz)	**Peak-to-peak amplitude (UIpp)**
FFS	FFS
FFS	FFS
FFS	FFS
10 M < *f* ≤ measured up to fourth-order Bessel-Thomson filter defined in clause 88.8.8 of [IEEE 802.3ba]	Each lane according to clause 88.7.2, Table 88-8 and clause 88.8.10 of [IEEE 802.3ba]

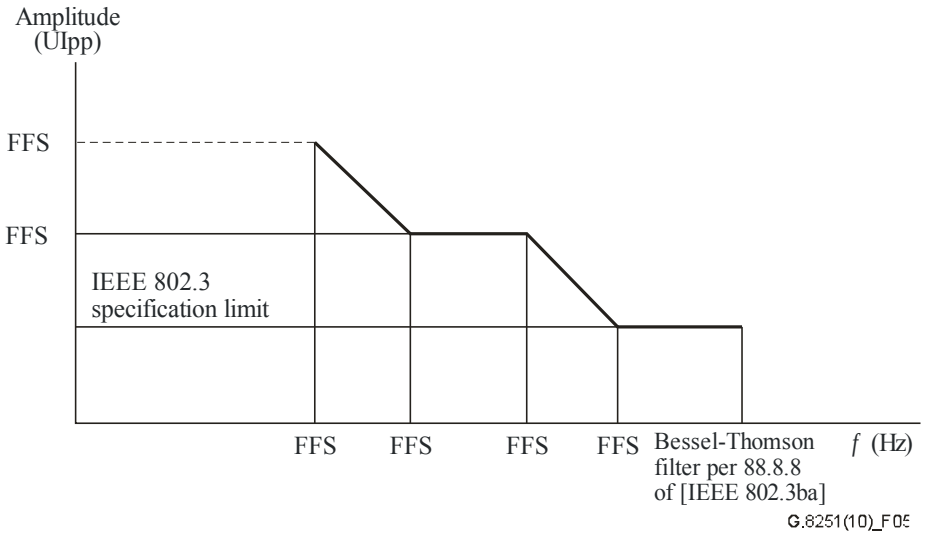


Figure 6.1-5 – OTL4.4 per lane input sinusoidal jitter tolerance limit

6.2 Jitter and wander tolerance of client interfaces

Jitter and wander tolerance requirements and network limits for CBR0G155, CBR0G622, CBR2G5, CBR10G, and CBR40G are derived from the corresponding requirements for STM-1, STM-4, STM-16, STM-64 and STM-256 signals, respectively, given in [ITU-T G.825].

STM input ports, i.e., the input to the ODUkP/CBRx-a_A_So and ODUkP/CBRx-b_A_So atomic functions, must tolerate jitter and wander levels specified in [ITU-T G.825]. Guidelines for measuring the input jitter and wander tolerance of equipment input interfaces are given in Appendix III of [ITU-T G.823].

For input ports to the ODU0P-to-Client adaptation function (ODU0P/CBRx_A, 0 < x ≤ 1G25), the specification of the particular clients applies. Jitter and wander tolerance requirements and network limits for 1GE are derived from the corresponding requirements for (transcoded) 1GE signals, given in [IEEE 802.3]. For SDH rates, the [ITU-T G.825] specifications apply; for native Ethernet, the [IEEE 802.3] specifications apply (clock tolerance of 100 ppm).

The 10GE signals shall support the 10G Ethernet specifications in [IEEE 802.3].

For 40G and 100G Ethernet to be transported over ODU3 and ODU4, respectively, the jitter as defined in [IEEE 802.3ba] is applicable on the multilane client port.

The FC-x (x = 100, 200, 400, 800, and 1200) signals shall support the fibre channel specifications of [b-ANSI 352] and [b-ANSI 364].

Annex A

Specification of the ODUk clock (ODC)

(This annex forms an integral part of this Recommendation)

A.1 Scope

This annex contains the requirements for the ODUk clock (ODC). Here, the term 'clock' refers to a clock filtering and/or generating circuit. Four ODC types are defined, for different applications (see clause A.2):

1) ODCa for asynchronous mapping (AMP or GMP) of constant bit rate (CBR) clients (e.g., generic CBRx client, RS client, etc.) and variable bit rate (VBR) clients (e.g., VP client, GFP client, etc.) into ODUk, asynchronous multiplexing of ODUj[/i] (AMP mapping into 2.5G timeslots) or ODUj (mapping into 1.25G timeslots) clients into ODUk (k > j), generation of Test/NULL signals, and AIS and OCI generation;
2) ODCb for bit-synchronous mapping of CBRx clients into ODUk;
3) ODCr for 3R regeneration of the ODUk signal; and
4) ODCp for demapping of constant bit rate (CBR) clients and demultiplexing of ODUj[/i] or ODUj clients from ODUk (k > j).

The ODCa and ODCb generate the timing signal for the ODUk and OTUk signals produced by an OTN network element. The ODCr generates the timing signal for the OTUk produced by a 3R regenerator. The ODCp generates the timing signal for a demapped CBRx client signal or demultiplexed ODUj[/i] or ODUj signal.

The four ODC types, the atomic functions they reside in, and their applicable requirements, are summarized in Table A.1-1. The requirements are described in more detail in the clauses that follow.

Table A.1-1 – Summary of ODUk clock (ODC) types

	ODCa (Note 4)	ODCb (Note 4)	ODCr	ODCp (Note 4)
Atomic function	ODUkP/CBRx-a_A_So ODUkP/GFP_A_So ODUkP/NULL_A_So ODUkP/PRBS_A_So ODUkP/RSn-a_A_So ODUkP/VP_A_So ODUkP/ODU[i]j_A_So ODUkP/ODUj_A_So ODUkP/ODUi[j]_A_Sk (AIS clock) OTUk/ODUk_A_Sk (AIS clock) OTUkV/ODUk_A_Sk (AIS clock) ODUk_C (OCI clock)	ODUkP/CBRx-b_A_So ODUkP/RSn-b_A_So	OTUk/ODUk_A_So and OTUk/ODUk_A_Sk (i.e., the clocks of these atomic functions are concentrated in a single ODCr; see [ITU-T G.798])	ODUkP/CBRx_A_Sk ODUkP/ODU[i]j_A_Sk ODUkP/ODUj_A_Sk
Frequency accuracy	±20 ppm	±20 ppm for ODUk (k = 0, 1, 2, 3, 4) ±20 ppm for CBRx (x = 2G5, 10G, 40G) ±100 ppm for ODU2e, ODUflex, 10GE, and FC-x (x = 100, 200, 400, 800, 1200)	±20 ppm	±20 ppm for ODUk (k= 0, 1, 2, 3, 4) ±20 ppm for CBRx (x = 0G155, 0G622, 2G5, 10G, 40G) ±100 ppm for 1GE, 10GE, 40GE, 100GE, FC-x, ODUflex, and ODU2e
Free-run mode supported	Yes	Yes	Yes	Yes
Locked mode supported	No	Yes	Yes	Yes
Holdover mode supported	No	No	No	No
Pull-in range	NA	±20 ppm (SDH clients) ±100 ppm (Ethernet and FC-x (x = 100, 200, 400, 800, 1200) clients)	±20 ppm	±20 ppm (SDH clients) ±100 ppm (Ethernet and FC-x (x = 100, 200, 400, 800, 1200) clients)

Table A.1-1 – Summary of ODUk clock (ODC) types

	ODCa (Note 4)	ODCb (Note 4)	ODCr	ODCp (Note 4)
Pull-out range	NA	±20 ppm (SDH clients) ±100 ppm (Ethernet and FC-x (x = 400, 800, 1200) clients)	±20 ppm	±20 ppm (SDH clients) ±100 ppm (Ethernet and FC-x (x = 100, 200, 400, 800, 1200) clients)
Jitter generation	Table A.5-1	Table A.5-1	Table A.5-1	Table A.5-2
Wander generation	NA	NA (Note 1)	NA	NA (Note 2)
Jitter tolerance	NA	[ITU-T G.825] for SDH clients [IEEE 802.3] for Ethernet clients	Table 6.1-1, Figure 6.1-1 (OTU1) Table 6.1-2, Figure 6.1-2 (OTU2) Table 6.1-3, Figure 6.1-3 (OTU3) Table 6.1-4, Figure 6.1-4 (OTU3/ OTL3.4) Table 6.1-5, Figure 6.1-5 (OTU4/ OTL4.4)	Table 6.1-1, Figure 6.1-1 (OTU1) Table 6.1-2, Figure 6.1-2 (OTU2) Table 6.1-3, Figure 6.1-3 (OTU3) Table 6.1-4, Figure 6.1-4 (OTU3/OTL3.4) [IEEE 802.3] for Ethernet clients
Wander tolerance	NA	[ITU-T G.825]	Clause 6.1	Clause 6.1

Table A.1-1 – Summary of ODUk clock (ODC) types

	ODCa (Note 4)	ODCb (Note 4)	ODCr	ODCp (Note 4)
Jitter transfer	NA	Maximum bandwidth: ODU0: 0.5 kHz ODU1: 1 kHz ODU2: 4 kHz ODU2e: 4 kHz ODU3: 16 kHz ODUflex: FFS Maximum gain peaking: 0.1 dB for ODU0, 1, 2, 2e, and 3 FFS for ODUflex (see Table A.7-1 and Figure A.7-1)	Maximum bandwidth: OTU1: 250 kHz OTU2: 1000 kHz OTU3: 4000 kHz OTU4: 10000 kHz Maximum gain peaking: 0.1 dB for OTU1, 2, 3 and 4 (see Table A.7-2 and Figure A.7-1)	Maximum bandwidth: 300 Hz for ODUk (k=0, 1, 2, 2e, 3, flex) 300 Hz for CBRx (x = 0G155, 0G622, 2G5, 10G, 40G), 10GE, 40GE, 100GE, FC-x (x =100, 200, 400, 800, 1200) 100 Hz for 1GE Maximum gain peaking: 0.1 dB (see clause A.7.3)
Output when input signal is lost	AIS (CBRx client) OTUk: no frame hit OTUk frequency unchanged	AIS (CBRx client) Local Fault (Ethernet and FC-x (x = 100, 200, 400, 800, 1200) clients) OTUk: no frame hit OTUk initial frequency change ≤ 9 ppm (See clause A.8)	AIS (OTUk) OTUk: frame hit allowed Temporary OTUk frequency offset > 20 ppm allowed	AIS (CBRx client), AIS (ODUj[/i] client) Frequency offset ≤ 20 ppm Local Fault (Ethernet and FC-x (x = 100, 200, 400, 800, 1200) clients) Frequency offset ≤ 100 ppm

NA No requirement because not applicable

NOTE 1 – The wander generation of ODCb is expected to be negligible compared to the wander on the input CBR (e.g., SDH) client signal, because the ODCb bandwidth is relatively wideband.

NOTE 2 – The intrinsic wander generation of the ODCp is negligible compared to the wander generated by the demapping process.

NOTE 3 – To achieve the compliance of STM-1 and STM-4 signals mapped with GMP into ODU0 with SDH jitter wander specification in addition to the ODCp clock filtering, the use of one bit additional phase information as specified in [ITU-T G.709] and [ITU-T G.798] is required.

NOTE 4 – An ODCa, ODCb, or ODCp for one client is not required to support another client simultaneously.

The output timing signals at the lower layers are derived from the ODUkP_AI_CK (i.e., from the ODCa, ODCb, or ODCr output) by frequency multiplication. For example, the OTUk timing signal is the OTUk_AI_CK, which is output from the OTUk/ODUk_A_So atomic function (see clause 13.3.1.1 of [ITU-T G.798]). This signal is derived from the ODUk_CI_CK (characteristic information of the ODUk; this signal has the same frequency as the ODUkP_AI_CK) via frequency multiplication by 255/239. The OTUk_AI_CK provides the timing input to the OCh/OTUk_A_So and OPSM/OTUk_A atomic functions, whose output is the OCh data signal (OCh_AI_D).

NOTE – In the case of asynchronous mapping or multiplexing, there is no requirement for a single master clock, i.e., single ODCa, in OTN equipment. Within OTN equipment there may be multiple, independent ODCa clocks for each outgoing wavelength (i.e., for the source of each OCh, OTUk, and ODUk). In the case of bit-synchronous mapping, 3R regeneration, and demapping there cannot be a single master clock for multiple OCh's, i.e., an ODCb, ODCr, or ODCp supplies timing for a single ODUk, OTUk, or CBR client, respectively.

A.2 Applications

The ODCa and ODCb are used for the mapping of payload to the ODUk signal; the ODCr is used for the 3R regeneration; the ODCp is used in the CBR demapper and ODU[i]j demultiplexer.

The ODCa, used for asynchronous mapping (AMP and GMP) and ODU[i]j multiplexing, is free running and the bit rate offset is accommodated by appropriately controlled stuffing. The ODCa is also the AIS and OCI clock.

The ODCb, used for bit-synchronous mapping, is locked to the bit rate of the incoming payload signal and the bit rate offset is accommodated by a fixed stuff pattern. The synchronous operation is continued even if the received payload contents is AIS. If the incoming signal fails, the ODC enters the free-run condition.

The ODCr, used for 3R regeneration, is locked to the bit rate of the incoming OCh_AP signal (including AIS). If the incoming signal fails, the ODC enters the free-run condition.

The ODCp, used for the CBR demapper and the ODU[i]j demultiplexer, is locked to the bit rate of the gapped OPUk clock (i.e., the timing of the signal that results from taking the OPUk payload and applying the justification control). If the incoming signal fails, the ODCp enters a free-run condition.

A.3 Frequency accuracy

Under free-running conditions, the output frequency accuracy of ODCa and ODCp shall not be worse than 20 ppm with respect to a reference traceable to an [ITU-T G.811] clock. Under free-running conditions, the output frequency accuracy of ODCb shall not be worse than 100 ppm for 1GE, 10GE, 40GE, 100GE, and FC-x clients and ODU2e, and shall not be worse than 20 ppm for all other respective clients and ODUs (see Table A.1-1). Under free-running conditions, the output frequency accuracy of ODCp shall not be worse than 100 ppm for 1GE, 10GE, 40GE, 100GE, and FC-x clients and ODU2e, and shall not be worse than 20 ppm for all other respective clients and ODUs (see Table A.1-1).

A.4 Pull-in and pull-out ranges

A.4.1 Pull-in range

The minimum pull-in range of ODCb, ODCr, and ODCp shall be ±100 ppm for 1GE, 10GE, 40GE, 100GE, and FC-x clients and ODU2e, and ±20 ppm for all other clients and ODUs (see Table A.1-1), whatever the internal oscillator frequency offset may be. There is no requirement for the pull-in range of ODCa because it is free-running.

A.4.2 Pull-out range

The minimum pull-out range of ODCb, ODCr, and ODCp shall be ±100 ppm for 1GE, 10GE, 40GE, 100GE, and FC-x clients and ODU2e, and ±20 ppm for all other clients and ODUs (see Table A.1-1), whatever the internal oscillator frequency offset may be. There is no requirement for the pull-out range of ODCa because it is free-running.

A.5 Noise generation

This clause limits the output jitter and wander for each applicable clock type, in the absence of any input jitter or wander. Note that the respective input and output signals depend on the clock type, because the different clock types are located in different atomic functions.

A.5.1 Jitter generation

A.5.1.1 ODCa, ODCb, and ODCr jitter generation

In the absence of input jitter, jitter of the ODCa and ODCb output, i.e., the ODUkP_AI_CK signal, shall not exceed the values specified in Table A.5-1 when measured over a 60-second interval with the measurement filters specified in that table. Since ODCa is free-running, there is no input jitter by definition. For ODCb, it is the input client signal that is jitter-free.

NOTE 1 – The ODU2e has a ±100 ppm clock tolerance aligned to the 10G Ethernet client, but the ODU2e jitter generation requirements are identical to ODU2 and enable transport of synchronous Ethernet.

Table A.5-1 – ODCa, ODCb, and ODCr jitter generation requirements

Interface	Measurement bandwidth, –3 dB frequencies (Hz)	Peak-to-peak amplitude (UIpp) (Note 2)
ODU0	2.5 k to 10 M	0.3
	0.5 M to 10 M	0.1
ODU1, OTU1	5 k to 20 M	0.3
	1 M to 20 M	0.1
ODU2, OTU2	20 k to 80 M	0.3
	4 M to 80 M	0.1
ODU2e	20 k to 80 M	0.3
	4 M to 80 M	0.1
ODU3, OTU3	20 k to 320 M	1.2 (Note 1)
	16 M to 320 M	0.14
OTL3.4	FFS	FFS
	4 M measured up to fourth-order Bessel-Thomson filter defined in clause 87.8.9 of [IEEE 802.3ba]	Each lane as defined in clause 87.7.1, Table 87-7, and clause 87.8.9 of [IEEE 802.3ba]
OTL4.4	FFS	FFS
	10 M to fourth-order Bessel-Thomson filter defined in clause 88.8.8 of [IEEE 802.3ba]	Each lane as defined in clause 88.7.1, Table 88-7, and clause 88.8.8 of [IEEE 802.3ba]

Table A.5-1 – ODCa, ODCb, and ODCr jitter generation requirements

Interface	Measurement bandwidth, –3 dB frequencies (Hz)	Peak-to-peak amplitude (UIpp) (Note 2)
ODUflex	FFS	FFS

NOTE 1 – See clause IV.4 for additional information.

NOTE 2 –

ODU0 $1UI = \frac{1}{1.24416}[\text{ns}] = 803.8\,\text{ps}$

ODU1 $1UI = \frac{238}{(239)(2.48832)}[\text{ns}] = 400.2\,\text{ps}$

ODU2 $1UI = \frac{237}{(239)(9.95328)}[\text{ns}] = 99.63\,\text{ps}$

ODU3 $1UI = \frac{236}{(239)(39.81312)}[\text{ns}] = 24.80\,\text{ps}$

OTU1 $1\text{ UI} = \frac{238}{(255)(2.48832)}\text{ns} = 375.1\,\text{ps}$

OTU2 $1\text{ UI} = \frac{237}{(255)(9.95328)}\text{ns} = 93.38\,\text{ps}$

OTU3 $1\text{ UI} = \frac{236}{(255)(39.81312)}\text{ns} = 23.25\,\text{ps}$

OTL3.4 $1\text{ UI} = \frac{4 \times 236}{(255)(39.81312)}\text{ns} = 92.98\,\text{ps per lane}$

OTL4.4 $1\text{ UI} = \frac{4 \times 227}{(255)(99.5328)}\text{ns} = 35.77\,\text{ps per lane}$

In the absence of input jitter to a 3R regenerator (i.e., to the OCh/OTUk_A_Sk atomic function), the output jitter on the clock information in the OCh_AI_D signal output from the OCh/OTUk_A_So atomic function shall not exceed the values specified in Table A.5-1 when measured over a 60-second interval with the measurement filters specified in that table. The signal that must be free of input jitter when this measurement is made is the OCh_AI_D signal input to the corresponding OCh/OTUk_A_Sk atomic function. Specifically, it is the clock information in this signal that must have no input jitter.

NOTE 2 – This is actually a requirement for the jitter generation of a 3R regenerator; it constrains the total jitter generation in all the atomic functions from OCh/OTUk_A_Sk to OCh/OTUk_A_So (inclusive) or OPSM/OTUk_A_Sk to OPSM/OTUk_A_So (inclusive). The ODCr is included in this, as it resides in the OTUk/ODUk_A_So and OTUk/ODUk_A_Sk atomic functions (i.e., the clocks of these atomic functions are concentrated in a single ODCr; see [ITU-T G.798]).

A.5.1.2 ODCp jitter generation

In the absence of input jitter, jitter of the ODCp output, i.e., the CBR/RS_CI_CK signal or the ODUj[/i]_CI_Ck or ODUj_CI_Ck signal, shall not exceed the values specified in Table A.5-2 when measured over a 60-second interval with the measurement filters specified in that table. Note that the output is at the CBRx/RSn_CP interface, the ODUj[/i]_CP interface, or the ODUj_CP interface. The requirements shall be met when the input frequency of the CBRx/ODUj[/i] or the CBRx/ODUj client is constant within the limits –20 ppm to +20 ppm from the nominal frequency and when the

input frequency of the 10GE/ODU2e, 40GE or 100GE client is constant within the limits –100 ppm to +100 ppm from the nominal frequency.

NOTE – The CBR_CP and ODUk[/i]_CP are internal to a network element, and are therefore generally not accessible to testing. Compliance with the requirement may be verified by varying the frequency of the CBRx/ODUj[/i], CBRx/ODUj or 10GE/ODU2e client input at the OS_CP or OCh_CP within the limits –20 ppm to +20 ppm or –100 ppm to +100 ppm, respectively, from nominal frequency and verifying that, for jitter-free input, the jitter on the demapped client output of the ODCp is within the limits specified in Table A.5-2.

One purpose of the ODCp wideband jitter generation requirements is to ensure that the gaps due to fixed overhead in the OTUk frame will not cause excessive output jitter. Additional information on this is provided in clause V.3.

Table A.5-2 – ODCp jitter generation requirements

Interface	**Measurement bandwidth, –3 dB frequencies (Hz)**	**Peak-to-peak amplitude (UIpp) (Note 3)**
CBR0G155	0.5 k to 1.3 M	1.0
	65 k to 1.3 M	0.1
CBR0G622	1 k to 5 M	1.0
	250 k to 5 M	0.1
1GE	2.52 k to 10 M	1.0
	0.673 M to f_4 (Note 1)	TP2, according to clause 38.5, Table 38-10 of [IEEE 802.3]
ODU0	2.5 k to 10 M	1.0
	0.673 M to 10 M	0.1
CBR2G5, ODU1	5 k to 20 M	1.0
	1 M to 20 M	0.1
CBR10G, ODU2	20 k to 80 M	1.0
	4 M to 80 M	0.1
10GE, ODU2e	20 k to 80 M	1.0
	4 M to f_4 (Note 2)	Transmit eye mask, defined in clause 52.7.1, Table 52-16 of [IEEE 802.3]
CBR40G, ODU3	80 k to 320 M	1.0
	16 M to 320 M	0.14
40GE, ODU3 Multilane	FFS	FFS
	4 M measured up to fourth-order Bessel-Thomson filter defined in clause 87.8.9 of [IEEE 802.3ba]	Each lane as defined in clause 87.7.1, Table 87-7, and clause 87.8.9 of [IEEE 802.3ba]

Table A.5-2 – ODCp jitter generation requirements

Interface	Measurement bandwidth, –3 dB frequencies (Hz)	Peak-to-peak amplitude (UIpp) (Note 3)
100GE	FFS	FFS
	10 M to fourth-order Bessel-Thomson filter defined in clause 88.8.8 of [IEEE 802.3ba]	Each lane as defined in clause 88.7.1, Table 88-7, and clause 88.8.8 of [IEEE 802.3ba]
ODUflex and its CBRx clients	FFS	FFS

NOTE 1 – f_4 = bandwidth of fourth-order Bessel-Thomson filter defined in clause 38.6.5 of [IEEE 802.3].
NOTE 2 – f_4 = bandwidth of fourth-order Bessel-Thomson filter defined in clause 52.9.7 of [IEEE 802.3].

NOTE 3 – 1GE $1\text{UI} = \frac{1}{1.25}$ [ns] = 800 ps

CBR2G5 $1\text{ UI} = \frac{1}{2.48832}$ [ns] = 401.9 ps

CBR10G $1\text{UI} = \frac{1}{9.95328}$ [ns] = 100.5 ps

CBR40G $1\text{ UI} = \frac{1}{39.81312}$ [ns] = 25.12 ps

ODU0 $1UI = \frac{1}{1.24416}[\text{ns}] = 803.8\,\text{ps}$

ODU1 $1\text{ UI} = \frac{238}{(239)(2.48832)}$ [ns] = 400.2 ps

ODU2 $1\text{ UI} = \frac{237}{(239)(9.95328)}$ [ns] = 99.63 ps

ODU2e $1\text{ UI} = \frac{237}{(239)(10.31250)}$ [ns] = 97.78 ps

ODU3 $1\text{ UI} = \frac{236}{(239)(39.81312)}$ [ns] = 25.43 ps

ODU3 (Multilane) $1\text{ UI} = \frac{236\times 4}{(239)(39.81312)}$ [ns] = 99.21 ps

ODU4 (Multilane) $1\text{ UI} = \frac{227\times 4}{(239)(99.53280)}$ [ns] = 38.17 ps

A.5.2 Wander generation

There are no wander generation requirements for ODCa, ODCb, ODCr, and ODCp. For ODCb, any intrinsic wander generation is expected to be negligible compared to the wander on the input CBR (e.g., SDH) client signal, because the ODCb bandwidth is relatively wideband. The intrinsic wander generation of the ODCp is negligible compared to the wander generated by the demapping process.

A.6 Noise tolerance

This clause specifies the jitter and wander tolerance of ODCb, ODCr, and ODCp. There are no jitter and wander tolerance requirements for ODCa because ODCa is free-running.

ODCb must satisfy the same jitter and wander tolerance requirements as CBR2G5, CBR10G, CBR40G, 1GE, 10GE, 40GE, 100GE, or FC-x client interfaces (the input to the ODUkP/CBRx-b_A_So atomic function). These requirements are given in clause 6.2, which references [ITU-T G.825] and the Ethernet specifications in [IEEE 802.3].

Note that the ODCb is contained in the ODUkP/CBRx-b_A_So atomic function.

ODCr and ODCp must satisfy the same jitter and wander tolerance requirements as OTUk input ports (the input to the OCh/OTUk_A_Sk atomic function). These requirements are given in clause 6.1 and its subclauses. Note that the ODCr is contained in the OTUk/ODUk_A_So and OTUk/ODUk_A_Sk atomic functions, and the ODCp is contained in the ODUkP/CBRx_A_Sk atomic function.

A.7 Jitter transfer

This clause specifies the jitter transfer of ODCb, ODCr, and ODCp. There are no jitter transfer requirements for ODCa because ODCa is free-running.

A.7.1 Jitter transfer for ODCb

The jitter transfer function for ODCb is defined as the ratio of the output sinusoidal jitter amplitude to input sinusoidal jitter amplitude, as a function of frequency. The ODCb input is the CBRx_CI_CK signal at the ODUkP/CBRx-b_A_So atomic function. The ODCb output is the CBRx_AI_CK signal at the ODUkP/CBRx-b_A_Sk atomic function.

The jitter transfer function of ODCb shall be under the curve given in Figure A.7-1 when input sinusoidal jitter up to the respective masks referenced in clause A.6 is applied. The parameters of Figure A.7-1 are given in Table A.7-1. Note that the parameter f_C may be considered the maximum bandwidth of the ODCb, and the parameter P the maximum gain peaking of the ODCb. The jitter transfer limit is specified between frequencies of f_L and f_H. The jitter transfer limit is not specified for frequencies higher than f_H nor lower than f_L.

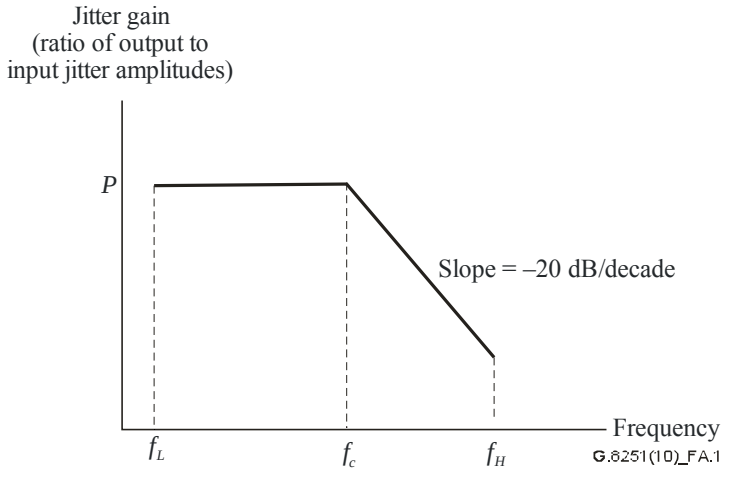


Figure A.7-1 – ODCb jitter transfer

Table A.7-1 – ODCb jitter transfer requirement

ODUk level	f_L (Hz)	f_C (kHz)	f_H (kHz)	P (dB)	Input mask
ODU1	10	1	100	0.1	Clause A.6
ODU2	40	4	400	0.1	Clause A.6
ODU2e	40	4	400	0.1	Clause A.6
ODU3	160	16	1600	0.1	Clause A.6
ODUflex	FFS	FFS	FFS	FFS	FFS

A.7.2 Jitter transfer for ODCr

The jitter transfer requirements for ODCr are, essentially, the transfer requirements for a 3R regenerator. While the 3R regenerator encompasses all the atomic functions between the OCh/OTUk_A_Sk adaptation function and OCh/OTUk_A_So adaptation function, and includes the wideband clock recovery circuit in the OCh/OTUk_A_Sk, the ODCr (contained in the OTUk/ODUk_A_So and OTUk/ODUk_A_Sk atomic functions) bandwidth is, in practice, significantly narrower than any of the other bandwidths present in the regenerator and therefore determines the transfer characteristics. Because the ODCr bandwidth is much larger than 10 Hz (i.e., the upper limit of the wander region), the regenerators transfer wander without attenuation; there are no explicit wander transfer requirements.

The jitter transfer function of a 3R regenerator is defined as the ratio of the output sinusoidal jitter amplitude to input sinusoidal jitter amplitude, as a function of frequency. The 3R regenerator input is the OCh_AI_D signal at the OCh/OTUk_A_Sk atomic function. The 3R regenerator output is the OCh_AI_D signal at the OCh/OTUk_A_So atomic function. Note that the jitter transfer is not associated with a single atomic function; rather, it is associated with all the atomic functions between and including the OCh/OTUk adaptation sink and source functions. Normally, at least part of the 3R regeneration function must occur in the OCh/OTUk_A_Sk function because a clock must be recovered. However, the jitter transfer and jitter tolerance requirements imply the presence of a second, narrower bandwidth phase-locked loop; this phase-locked loop is in the ODCr, contained in the OTUk/ODUk_A_So and OTUk/ODUk_A_Sk atomic functions.

The jitter transfer function of a 3R regenerator shall be under the curve given in Figure A.7-1 when input sinusoidal jitter up to the masks of Figures 6.1-1, 6.1-2, 6.1-3, and 6.1-5 and for OTU1, OTU2, OTU3, and, OTU4 respectively, is applied. The parameters of Figure A.7-1 are given in Table A.7-2. Note that the parameter f_C may be considered the maximum bandwidth of the 3R regenerator, and the parameter P the maximum gain peaking of the 3R regenerator. The jitter transfer limit is specified between frequencies of f_L and f_H. The jitter transfer limit is not specified for frequencies higher than f_H nor lower than f_L.

Table A.7-2 – ODCr jitter transfer requirement

OTUk level	f_L (kHz)	f_C (kHz)	f_H (MHz)	P (dB)	Input mask
OTU1	2.5	250	20	0.1	Figure 6.1-1, Table 6.1-1
OTU2	10	1000	80	0.1	Figure 6.1-2, Table 6.1-2
OTU3	40	4000	320	0.1	Figure 6.1-3, Table 6.1-3
OTU4	100	10000	800	0.1	Figure 6.1-5, Table 6.1-5, (values per lane)

A.7.3 Jitter transfer for ODCp

The jitter transfer requirements for ODCp are, essentially, the transfer requirements for a CBR (e.g., SDH) demapper (i.e., a desynchronizer) or ODU[i]j demultiplexer. The demapper function, including the ODCp, is contained in the ODUkP/CBRx_A_Sk and ODUkP/RSn_A_Sk atomic functions. The demultiplexer functions, including the ODCp, are contained in the ODUkP/ODU[i]j_A_Sk atomic function. The ODCp performs filtering, which is necessary to control the mapping/demapping jitter and wander accumulation over multiple OTN islands.

The 3 dB bandwidth of the desynchronizer shall not exceed 300 Hz for:

– ODUk (k=0, 1, 2, 2e, 3, flex);

– CBRx (x = 0G155, 0G622, 2G5, 10G, 40G);

– 10GE, 40GE, 100GE;

– FC-x (x = 100, 200, 400, 800, 1200).

The 3 dB bandwidth of the desynchronizer shall not exceed 100 Hz for 1GE.

The maximum gain peaking of the desynchronizer shall be 0.1 dB. These requirements apply to all ODUk rates. Additional information, on demapper phase error, is given in Appendix V.

A.8 Transient response

When a CBR client signal is lost and AIS is inserted, or when the CBR client is restored and AIS is removed, the ODUk and OTUk timing must be maintained. This requirement is met automatically for asynchronous mappings because the ODCa is free-running and therefore independent of the client signal clock. However for bit-synchronous mapping, the ODCb takes its timing from the client. Specifically, the client signal timing is recovered by the clock recovery circuit that resides in the OS/CBR_A_Sk atomic function; the output of this clock recovery circuit is input to the ODCb (see Appendix VI for a summary of the atomic functions). Loss of the client signal results in the ODCb either entering free-run or switching to a free-running AIS clock or Ethernet local fault clock; restoration of the client signal results in the ODCb switching from free-run condition or from a free-running AIS clock to an independent client-signal clock. In addition, there may be a short period between the instant the client input to the clock recovery circuit is lost and the detection of this loss; during this period, the clock recovery circuit output may be off frequency and still be input to the ODCb. In all these cases, [ITU-T G.798] requires that the ODUk clock shall stay within its limits and no frame phase discontinuity shall be introduced. The maximum possible frequency difference between a ±20 ppm CBRx (e.g., SDH) client and free-running ODCb or free-running AIS clock is 40 ppm (because the largest possible offset for each signal is ±20 ppm). The maximum possible frequency difference between a ±100 ppm 1GE, 10GE, 40GE, 100GE or FC-x client and free-running replacement signal (local fault) clock is 200 ppm.

The above requirements mean that the ODCb must adequately filter a frequency step whose size is the maximum possible frequency difference, as indicated above, between the client and either AIS clock or replacement signal (local fault) clock, such that downstream equipment in the OTN, i.e., 3R regenerators, can tolerate the resulting filtered phase transient. Specifically, this means that the phase transient shall not cause buffer overflow in an ODCr that meets the jitter and wander tolerance requirements of clause 6.2. In addition, the ODCb must adequately filter the clock recovery circuit output during the short period between the loss of the client input to the clock recovery circuit and the removal of the clock recovery circuit output from the ODCb input.

If:

1) the clock recovery circuit in the OS/CBR_A_So atomic function loses its input and/or the ODCb loses its input and either enters free-run or switches to an AIS clock; or

2) the ODCb recovers from AIS to the output of the clock recovery circuit,

the ODCb output shall meet the following requirements:

a) Any initial frequency step shall not exceed 9 ppm.

b) Any frequency drift rate following the initial frequency step shall not exceed 200 ppm/s.

c) The total change in frequency shall not exceed the maximum possible frequency difference between the client signal and either the AIS clock or the replacement signal (local fault) clock.

Then, the ODCb is allowed to lose synchronization for a period up to 600 ms.

NOTE – An ODCb, for one client is not required to support another client simultaneously.

Appendix I

Relationship between network interface jitter requirements and input jitter tolerance

(This appendix does not form an integral part of this Recommendation)

I.1 Network interface jitter requirements

For all OTUk bit rates, two network limits are specified in Table 5.1-1: one for a wideband measurement filter and one for a high-band measurement filter. The general form of this specification is shown in Table I.1-1 and is applicable to all OTUk rates.

Table I.1-1 – General form for OTUk interface jitter requirements

Measurement filter	Measurement bandwidth	Peak-to-peak amplitude (UIpp)
Wideband	f_1 to f_4	A_2
High-band	f_3 to f_4	A_1

At any OTUk interface, the following output jitter specifications must be met:

1) Timing jitter as measured over a 60-second interval with a band pass filter with a lower cut-off frequency f_1 and a minimum upper cut-off frequency f_4 shall not exceed A_2 unit intervals (UI) peak-to-peak.

2) Timing jitter as measured over a 60-second interval with a band pass filter with a lower cut-off frequency f_3 and a minimum upper cut-off frequency f_4 shall not exceed A_1 unit intervals (UI) peak-to-peak.

The roll off at lower cut-off frequency, f_1 and f_3, shall be 20 dB/decade. The roll off at the upper cut-off frequency, f_4, shall be –60 dB/decade.

The value of f_1 reflects the narrowest timing circuit cut-off frequency expected in a line system. The timing circuit may time a regenerator's output signal and could be implemented as a phase-locked loop (PLL). Jitter at frequencies higher than the bandwidth of this PLL will be partially absorbed by the PLL's buffer. The portion not absorbed could cause transmission errors due to buffer spill. Jitter at frequencies lower than this bandwidth will simply pass through without affecting transmission performance. The value of f_1 therefore represents the narrowest bandwidth that might be used in this output timing circuit. The value of f_3 is related to the bandwidth of input timing acquisition circuitry. Jitter at frequencies higher than this bandwidth will constitute alignment jitter and will cause an optical power penalty due to its effect on the eye pattern. This high frequency jitter must therefore be limited to the same degree that equipment specifications limit optical power penalty through jitter tolerance.

The value of f_4 reflects reasonable measurement limitations and is specified to establish minimum measurement bandwidth requirements. f_4 is chosen to include all expected, significant alignment jitter. A value between one and two decades beyond the widest expected 3R regenerator 3 dB bandwidth (cut-off frequency) was chosen (see clause A.7.2).

The values of A_1 and A_2 are directly related to input sinusoidal jitter tolerance. These parameters have built-in margin and are reasonably conservative because:

1) sinusoidal jitter represents worst-case jitter with respect to input jitter tolerance; and

2) accumulated OTN line (OTUk) jitter will not be sinusoidal (instead, it will be noisy).

I.2 Input jitter tolerance of network equipment

The general form of the weighting filters used for measuring output jitter at a network interface given in Table I.1-1 are reproduced here in Figure I.2-1. The filter responses are given in Equations (I.2-1) and (I.2-2).

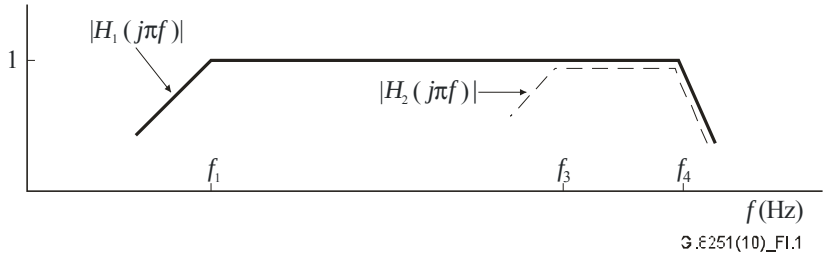


Figure I.2-1 – Weighting filters for measuring network interface output jitter

$$H_1(s) = \frac{s}{s+\omega_1} \cdot \frac{\omega_4^3}{s^3 + 2\omega_4 s^2 + 2\omega_4^2 s + \omega_4^3}$$
$$|H_1(2\pi jf)|^2 = \frac{f^2}{f^2 + f_1^2} \cdot \frac{f_4^6}{f^6 + f_4^6} \quad \text{(I.2-1)}$$

$$H_2(s) = \frac{s}{s+\omega_3} \cdot \frac{\omega_4^3}{s^3 + 2\omega_4 s^2 + 2\omega_4^2 s + \omega_4^3}$$
$$|H_2(2\pi jf)|^2 = \frac{f^2}{f^2 + f_3^2} \cdot \frac{f_4^6}{f^6 + f_4^6} \quad \text{(I.2-2)}$$

where:

$$\omega_1 = 2\pi f_1 \qquad \omega_3 = 2\pi f_3 \qquad \omega_4 = 2\pi f_4$$

The first term of the function $H_1(s)$ represents the phase error transfer function $H_e(s)$ of some PLL, and its amplitude of A_2 = 1.5 UIpp represents its phase error tolerance.

Then the corresponding input phase tolerance of the PLL is given by:

$$A_{tol1} = \frac{A_2}{|H_1(j2\pi f)|} \quad \text{(I.2-3)}$$

Similarly, the input phase tolerance corresponding to $H_2(s)$ and its amplitude of A_1 = 0.15 UIpp is given by:

$$A_{tol2} = \frac{A_1}{|H_2(j2\pi f)|} \quad \text{(I.2-4)}$$

These sinusoidal jitter tolerance masks are illustrated in Figure I.2-2. If unweighted sinusoidal jitter at a network interface satisfies both of these masks, it also satisfies (i.e., lies below) a single mask that is the lower of the two masks for each frequency. Such a combined mask is shown as a dashed curve in Figure I.2-3.

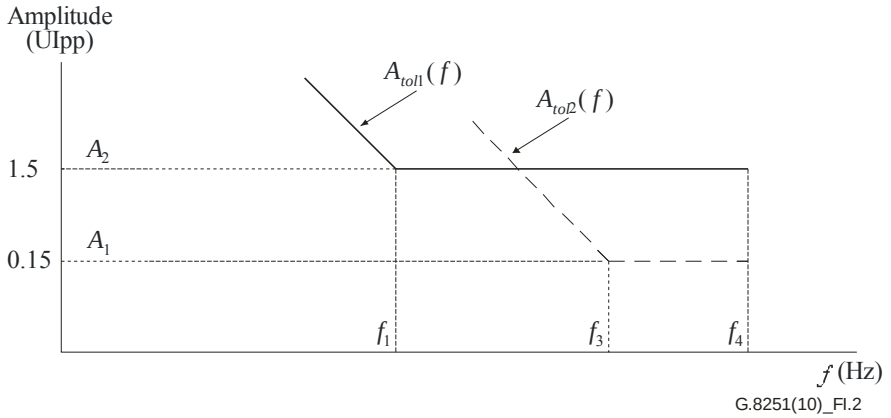


Figure I.2-2 – Upper bounds on sinusoidal jitter amplitude

Figure I.2-3 compares this combined mask with the OTU1 input jitter sinusoidal tolerance mask. They are the same in the range 500 Hz < f < 20 MHz.

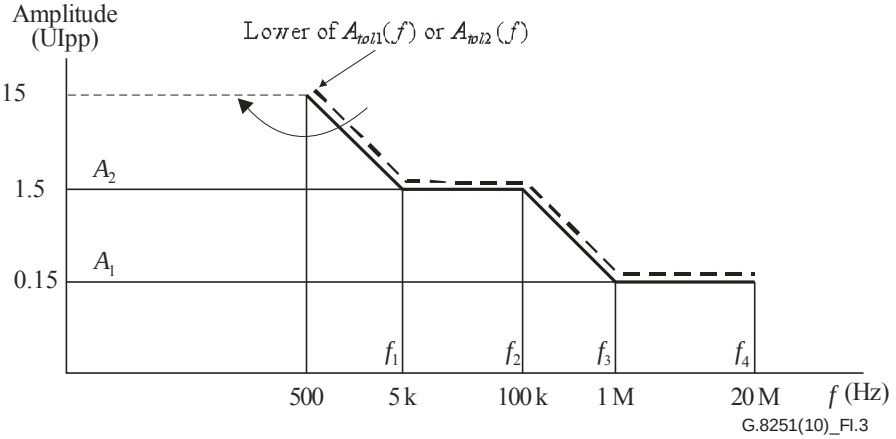


Figure I.2-3 – Upper bound on sinusoidal output jitter at an OTU1 interface [lower of $A_{tol1}(f)$ or $A_{tol2}(f)$] compared with input jitter/wander tolerance mask

Appendix II

Effect of OTN on the distribution of synchronization via STM-N and synchronous Ethernet clients

(This appendix does not form an integral part of this Recommendation)

II.1 Introduction

As stated in clause 1 (Scope) and in clause 5.2, the OTN physical layer will not be used to transport synchronization. The current standard for the transportation of synchronization over SDH or synchronous Ethernet is adequate. However, the introduction of the optical transport network (OTN) changes the position of an STM-N or synchronous Ethernet signal in the sense that it can now be a client signal within the OTN layer network. This might affect the synchronization network architecture, since the STM-N or synchronous Ethernet signal is currently used as a carrier for synchronization information (next to its payload-carrying capacity). This appendix analyses possible effects on the synchronization network of long-term wander (i.e., over time scales on the order of one day) associated with the introduction of the OTN layer. Appendix VII describes hypothetical reference models (HRMs) used to analyse the jitter and short-term wander associated with the introduction of the OTN layer. Appendix VII also provides a summary description of simulations based on the HRMs and an adapted ITU-T G.803 synchronization reference chain. Appendix VIII provides more detailed description of the simulation model used for OTN client payload jitter and wander accumulation, and describes some of the simulation results.

II.2 Provisional synchronization reference chain

To analyse the effect of the introduction of the OTN on the synchronization distribution network, the synchronization reference chain from [ITU-T G.803] has been provisionally adapted. The original reference chain contains 1 PRC, 10 SSUs and 60 SECs/EECs, under the condition that not more than 20 SECs/EECs are concatenated between any pair of SSUs. The provisionally adapted reference model has still 1 PRC and 10 SSUs, but the inter-SSU connections are now presumed to be over the OTN network. At the end of the chain there are 20 SECs/EECs (see Figure II.2-1).

NOTE – A more detailed analysis is done in Appendix VII and the correct reference chain is shown in Figure VII.3-2.

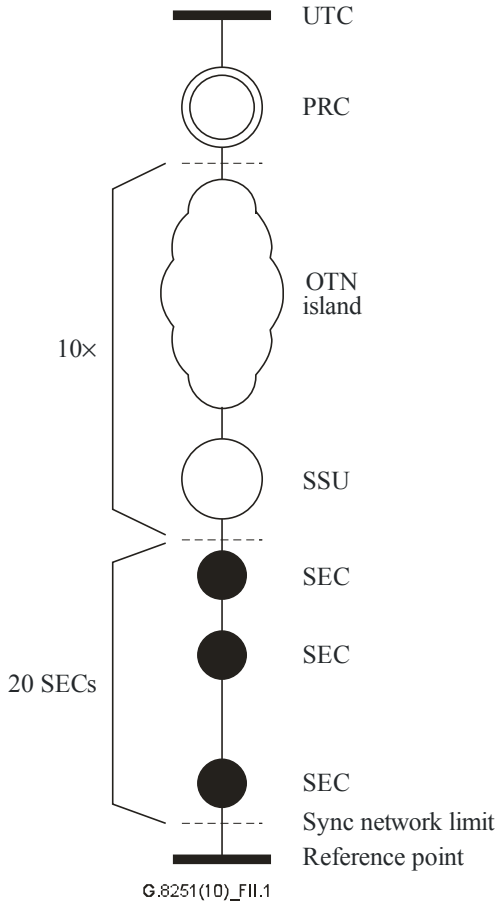


Figure II.2-1 – Adapted synchronization reference chain (provisional). For a synchronous Ethernet client, the SECs are replaced by EECs

The OTN island in this model has to be understood as a conglomerate of OTN equipment that performs mapping of an STM-N into its corresponding ODUk, multiple NEs that perform (de)multiplexing and cross-connecting of ODUks and transport over optical channels (including optical multiplexing and cross-connecting), and finally demapping of the STM-N.

The composition of each OTN island in the provisional model is assumed to consist of 1 OTN network element that performs the mapping operation and nine other OTN network elements that perform multiplexing operations of ODUks.

In fact, the distribution of the OTN islands over the adapted synchronization reference model is not important for the long-term wander accumulation. In the model there is one OTN island between each SSU pair, but another distribution is also allowed. For example, five inter-SSU connections may have two OTN islands each while the other interconnections make use of the STM-N physical layer. Also, the number of multiplexing/mapping network elements may be freely re-divided over the OTN islands, to create some "large" and some "small" OTN islands.

II.3 Synchronization network limit

The network limit that is valid at the end of the synchronization reference chain, as defined in [ITU-T G.803], allows for 5 µs of wander over 24 hours for Option 1 (see [ITU-T G.823]) and 1.86 µs over 24 hours for Option 2 (see [ITU-T G.824]). It was agreed that in the adapted synchronization reference chain, 10% of the Option 1 budget should be adequate for the combined effect of the OTN islands, i.e., 500 ns (or ~78 bytes at 1.25 Gbit/s).

Since there are 10 OTN islands in the synchronization reference chain, each with 10 mapper/multiplexer NEs (all assumed to work at the 1.25 Gbit/s rate which represents the worst

case), there are 100 of those NEs altogether in the reference chain. Hence, each OTN network element of such type can be allowed 5 ns (or 0.78 bytes at 1.25 Gbit/s) contribution to the long-term wander build-up.

II.4 Variable channel memory

Generically, one can state that the maximum amount of wander that can be accumulated on a path through a network depends on the maximum amount of propagation delay variation through the network. Propagation delay variations can be caused by elastic buffers that are used in mapping and multiplexing operations. But they can also be caused by fibres, of which the exact propagation delay depends, for example, on temperature. In general, the variable part of the amount of memory in the channel will determine the maximum possible wander. If the propagation delay is $\tau_o \pm \Delta\tau$, the maximum peak-to-peak wander is $2 \cdot \Delta\tau$. (See Figure II.4-1.)

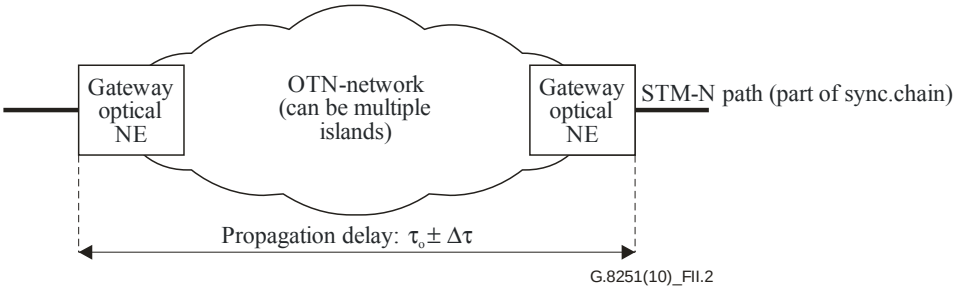


Figure II.4-1 – Variable channel delay

Whether or not the upper wander limit will actually be reached in practical networks depends on a number of factors. The performance of the synchronization of the network is one factor (e.g., this is the main reason why SDH networks require synchronous operation), another factor is the actual design of the elastic buffers. To compute the likelihood of exceeding certain amounts of wander over a certain amount of time with a certain probability requires extensive simulation work, which captures the important details of the elasticstore-related processes and the exact network reference model. The disadvantage of this approach is that it is generally not easy to perform these simulations over long time intervals (e.g., on the order of one day) for networks that deviate in some aspects from the reference model. For this reason, a worst-case approach, based on maximum channel memory variation, has been chosen for the evaluation of long-term wander.

II.5 Maximum buffer hysteresis

If each OTN network element is allowed to contribute 5 ns to long-term wander accumulation, the resulting maximum buffer hysteresis is approximately 6.22 UI = 0.778 bytes for ODU0, 12.5 UI = 1.5625 bytes for ODU1, 50 UI = 6.25 bytes for ODU2, and 200 UI = 25 bytes for ODU3. Because implementations are often more convenient if they can work with whole numbers of bytes, the ODU0 value is increased to the nearest whole number of bytes, i.e., 1 byte. The ODU1 value is set to 2 times this, or 2 bytes, the ODU2 value is set to 8 times this, or 8 bytes, and the ODU3 value is set to 32 times this, or 32 bytes. In units of phase time, the buffer hysteresis is approximately 6.4 ns. The total long-term wander budget for the Figure II.2-1 synchronization reference chain (100 OTN network elements) becomes 640 ns.

[ITU-T G.798] specifies that the maximum allowed buffer hysteresis in alignment functions for mapping and multiplexing operations[1], be restricted to 1 byte for STM-1, STM-4, 1000BASE-X, and FC-100 (these clients are all mapped to ODU0), 2 bytes for STM-16, FC-200, and IB-2G, 8 bytes for STM-64 and IB-8G, 32 bytes for STM-256 and 40GBASE-R, and 80 bytes for 100GBASE-R, per OTN NE[2, 3].

The above requirement for elastic store hysteresis per OTN network element should be applied to each possible route of the respective OTN client or its ODUk envelope through any OTN network element that performs mapping or multiplexing. In case multiple independent paths exist, the requirement should hold for each of these paths individually.

Another assumption made in this appendix is that OTN network elements that do not perform any multiplexing or mapping do not contain elastic buffers and thus do not contribute to the long-term wander accumulation.

---

1 Although desynchronizers and demultiplexers contain elastic stores, these elastic stores do not contribute to the long-term wander accumulation, since the very slow phase variations do not affect the buffer fill.

2 It is assumed that in case both mapping and multiplexing functions are performed on a single STM-N through an OTN NE, these can be realized with a single alignment operation.

3 Note that this differs from the approach in [ITU-T G.783], where for SDH pointer processors a minimum, instead of a maximum, amount of buffer hysteresis is prescribed. This is based on the objective of SDH to minimize the number of pointer adjustment events in the network.

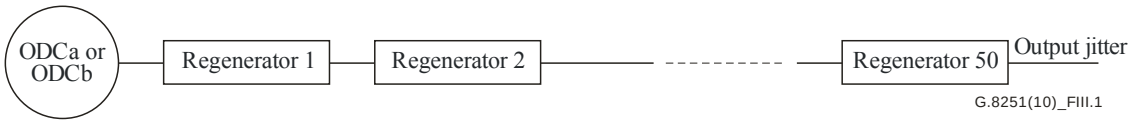
Appendix III

Hypothetical reference model (HRM) for 3R regenerator jitter accumulation

(This appendix does not form an integral part of this Recommendation)

This appendix describes the hypothetical reference model (HRM) used to obtain the 3R regenerator jitter transfer requirements in clause A.7.2 and the ODCa, ODCb, and ODCr jitter generation requirements in clause A.5.1.1. These requirements, together with the HRM, are consistent with the jitter network limits (at an OTUk interface) in clause 5.1 and the jitter tolerance requirements in clauses 6.1.1 to 6.1.3. The details of the 3R regenerator jitter accumulation analyses leading the above requirements and the HRM are given in Appendix IV.

The HRM for 3R regenerator jitter accumulation is given in Figure III.1-1. The HRM consists of 50 cascaded regenerators, each assumed to meet the jitter generation and transfer requirements of clauses A.5.1.1 and A.7.2, respectively. The 50 3R regenerators are preceded by an ODCa or ODCb, which is assumed to meet the jitter generation requirements of clause A.5.1.1. The 50 3R regenerators and ODCa or ODCb, together with the desynchronizer at the demapper, comprise one OTN island. For the case of bit-synchronous mapping, the ODCb is assumed to meet the noise transfer requirement of clause A.7.1. Under these conditions, the output jitter at the end of the chain of 50 3R regenerators is expected to be within the jitter network limits of Table 5.1-1 (see clause 5.1) and the jitter tolerance masks of Figures 6.1-1 to 6.1-3 (Tables 6.1-1 to 6.1-3; see clauses 6.1.1, 6.1.2, and 6.1.3, respectively). Note that, for the case of bit-synchronous mapping, it is not necessary to consider jitter accumulation over multiple OTN islands because the jitter accumulation at the egress of an island is effectively filtered by the desynchronizer.



NOTE – For the case of asynchronous mapping, the optical transmission section clock has no input (and therefore no jitter on the input). For the case of bit-synchronous mapping, any jitter accumulation in the previous island is filtered by the desynchronizer of that island.

Figure III.1-1 – HRM for 3R regenerator jitter accumulation

Note that other than stating that the 3R regenerators meet the jitter generation requirements of clause A.5.1.1, no detail is given here on precisely where in each regenerator the noise is generated. For the purposes here, it is simply stated that each regenerator meets clause A.5.1.1 jitter generation requirements in the absence of input jitter. Details of this for two jitter accumulation analyses are given in Appendix IV.

Appendix IV

3R regenerator jitter accumulation analyses

(This appendix does not form an integral part of this Recommendation)

IV.1 Introduction

This appendix describes the details of 3R regenerator jitter accumulation analyses that led to the jitter generation requirements of clause A.5.1, the jitter transfer requirements of clause A.7, and the HRM of Appendix III. Two different models were used in respective analyses that were performed independently; however, the models were similar and led to the same results.

Both models were implemented in the frequency domain. Each noise source was modelled via a power spectral density (PSD), which was passed through appropriate filters representing the regenerators. In the first model, the details of the regenerator PLLs were modelled with noise introduced in various components. In the second model, the noise was modelled via a PSD with an appropriate shape at the regenerator output, and the overall regenerator transfer characteristic (from input to output) was modelled separately. The noise levels were adjusted in both models such that the jitter generation requirements would be satisfied. Jitter generation and output jitter were evaluated using the appropriate measurement filters, which were also modelled with frequency domain transfer functions. The frequency domain models most conveniently produce mean-square jitter as the area under the PSD, and root-mean-square (rms) jitter as the square root of this. Peak-to-peak jitter over 60 s was assumed to be equal to 10 times the rms jitter.[4]

IV.2 Model 1

The regenerator is modelled as a second-order phase-locked loop (PLL) with first-order, proportional-plus-integral (PI) loop filter. Three separate noise sources are assumed to be present, representing phase detector noise, voltage-controlled oscillator (VCO) noise, and thermal noise in the optical receiver just prior to the PLL input. The model is developed for both systematic and random jitter accumulation cases; however, results are given only for random jitter accumulation cases. Jitter accumulation over 3R regenerators is approximately random because the buffer fills in the narrow-band phase-locked loops of the successive regenerators (i.e., in the successive ODCrs) are uncorrelated with each other. This is because it is the pattern-dependent jitter that can accumulate systematically, and the pattern-dependent jitter is produced by the clock recovery process in the wideband phase-locked loops. The lack of correlation in the ODCr buffer fills means that read clock pulses with pattern-dependent jitter will time different outgoing bits in successive 3R regenerators. This results in the pattern-dependent jitter in successive regenerators also being uncorrelated.

---

[4] In defining peak-to-peak jitter or, more generally, the peak-to-peak of any random process, both a measurement interval and a respective quantile (or percentile) should be specified. This is because, if the peak-to-peak measurement is repeated a sufficient number of times (always over the same measurement interval), a distribution of values will be obtained. Here, the measurement interval is taken to be 60 s. The quantile is not specified, but is assumed to be a convenient value consistent with a peak-to-peak to rms ratio of 10. This quantile is expected to be greater than 0.99. If the regenerators can be modelled as linear systems and the noise distribution is Gaussian, then the precise ratio of peak-to-peak to rms jitter is unimportant as long as the generation and output jitter specifications are expressed either both in terms of peak-to-peak jitter or both in terms of rms jitter.

The following subclauses present the details of the model and give results for selected cases. To minimize the number of simulation cases that must be run, the model is developed in dimensionless form. Two sets of results are given:

1) equivalent 3 dB bandwidth of 8 MHz for the OTU2 case, which is equivalent to the [ITU-T G.783] requirement for STM-64 regenerators; and

2) equivalent 3 dB bandwidth of 1 MHz for the OTU2 case, which is the requirement adopted for this Recommendation in clause 6.1.3.

The results show that the narrower bandwidth here was necessary in order to meet the jitter network limits of Table 5.1-1.

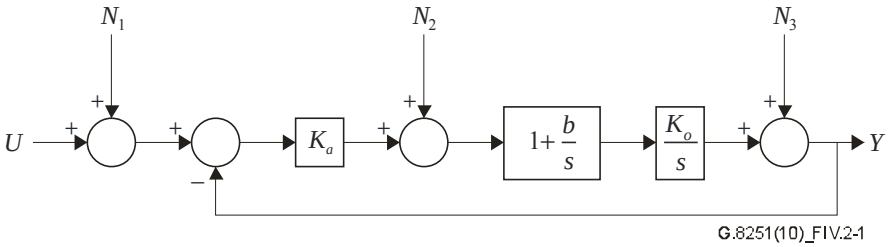


Figure IV.2-1 – Regenerator model

IV.2.1 Model details

The frequency domain analysis follows the methods used in [b-Varma] and [b-Trischitta]. The 3R regenerator model is shown in Figure IV.2-1. This is a linear model for a phase-locked loop (PLL). The phase detector gain is K_a, an active loop filter is assumed with transfer function $1+b/s$, and the VCO gain is K_o. $Y(s)$, $U(s)$, $N_1(s)$, $N_2(s)$, and $N_3(s)$, are the Laplace transforms (more precisely, the square root of the respective PSD) of the output, input, optical receiver noise, phase detector noise, and VCO noise, respectively. Then, the transfer functions may be written as follows:

$$\frac{Y(s)}{N_1(s)}=\frac{Y(s)}{U(s)}\equiv H(s)=\frac{\frac{K_aK_o}{s}\left(1+\frac{b}{s}\right)}{1+\frac{K_aK_o}{s}\left(1+\frac{b}{s}\right)}=\frac{K_aK_os+K_aK_ob}{s^2+K_aK_os+K_aK_ob} \tag{IV.2-1}$$

$$=\frac{2\varsigma\omega_n s+\omega_n^2}{s^2+2\varsigma\omega_n s+\omega_n^2}$$

$$\frac{Y(s)}{N_2(s)}=\frac{1}{K_a}H(s) \tag{IV.2-2}$$

$$\frac{Y(s)}{N_3(s)}=\frac{1}{1+\frac{K_aK_o}{s}\left(1+\frac{b}{s}\right)}=\frac{s^2}{s^2+K_aK_os+K_aK_ob} \tag{IV.2-3}$$

$$=\frac{s^2}{s^2+2\varsigma\omega_n s+\omega_n^2}=1-H(s)$$

where the undamped natural frequency and damping ration are:

$$\omega_n = \sqrt{K_a K_o b}$$
$$\varsigma = \frac{1}{2}\sqrt{\frac{K_a K_o}{b}} \tag{IV.2-4}$$

Since it will be assumed that both N_1 and N_2 are white noise, or white phase modulation (WPM), it will be convenient to combine these into a single equivalent noise source. This may be done as follows:

$$\begin{aligned} Y(s) &= H(s)U(s) + H(s)N_1(s) + H(s)N_2(s)/K_a + [1 - H(s)]N_3(s) \\ &= H(s)U(s) + H(s)N_{12}(s) + H_e(s)N_3(s) \end{aligned} \tag{IV.2-5}$$

where the equivalent noise source N_{12} is given by:

$$N_{12}(s) = N_1(s) + N_2(s)/K_a \tag{IV.2-6}$$

and the usual notation is used for the phase error transfer function:

$$H_e(s) \equiv 1 - H(s) \tag{IV.2-7}$$

A chain of N 3R regenerators is modelled by assuming that the output of the jth regenerator is the input to the (j+1)st regenerator, and that the input to the first regenerator in the chain is zero (i.e., the first regenerator is, in essence, a clock and has noise generation but no input jitter). In the following analysis, the cases of systematic and random jitter accumulation are considered separately, using the methodology of [b-Varma] and [b-Trischitta]. First, consider the random jitter accumulation case. Here, it is assumed that the corresponding noise sources in all the regenerators have the same magnitude, i.e., the same PSD, but are uncorrelated. The relation between the PSD of the input and output of a single regenerator is, using Equation (IV.2-5), and setting $s = j\omega$ in the transfer function to obtain the frequency response:

$$S_Y(\omega) = |H(j\omega)|^2 S_U(\omega) + |H(j\omega)|^2 S_{12}(\omega) + |H_e(j\omega)|^2 S_3(\omega) \tag{IV.2-8}$$

where $S(\omega)$ with the respective subscript denotes the PSD for the input, output, or respective noise source. Then, for a chain of N 3R regenerators, the PSD of the output phase assuming random jitter accumulation is:

$$\begin{aligned} S_{Nr}(\omega) &= \sum_{j=1}^{N} |H(j\omega)|^{2j} S_{12}(\omega) + \sum_{j=1}^{N} |H_e(j\omega)|^2 |H(j\omega)|^{2j-2} S_3(\omega) \\ &= \frac{|H(jw)|^2 \left[1 - |H(j\omega)|^{2N}\right]}{1 - |H(j\omega)|^2} S_{12}(\omega) + \frac{|H_e(j\omega)|^2 \left[1 - |H(j\omega)|^{2N}\right]}{1 - |H(j\omega)|^2} S_3(\omega) \end{aligned} \tag{IV.2-9}$$

For the case of systematic jitter accumulation, it is assumed that the corresponding noise sources in the successive regenerators are perfectly correlated, i.e., the N_{12} noise sources in the successive regenerators are perfectly correlated with each other, and the N_3 noise sources in the successive regenerators are perfectly correlated with each other. However, it is assumed that an N_{12} noise source and an N_3 noise source are uncorrelated. Then, for a chain of N 3R regenerators, the output phase Y_N at the end of the chain is:

$$\begin{aligned} Y_N(s) &= \sum_{j=1}^{N} H^j(s) N_{12}(s) + \sum_{j=1}^{N} H^{j-1}(s) H_e(s) N_3(s) \\ &= \frac{H(s)\left[1-H^N(s)\right]}{1-H(s)} N_{12}(s) + \frac{H_e(s)\left[1-H^N(s)\right]}{1-H(s)} S_3(s) \end{aligned} \tag{IV.2-10}$$

Then the PSD of the output is related to the noise source PSDs by:

$$S_{Ns}(\omega) = \left|H(j\omega)\right|^2 \left|\frac{1-H^N(j\omega)}{1-H(j\omega)}\right|^2 S_{12}(\omega) + \left|H_e(j\omega)\right|^2 \left|\frac{1-H^N(j\omega)}{1-H(j\omega)}\right|^2 S_3(\omega) \tag{IV.2-11}$$

The mean square phase at the output of the chain of 3R regenerators is given by the integral of the PSD of Equation (IV.2-9) or (IV.2-11) over all frequencies (from minus infinity to plus infinity). Since the PSD is symmetric about zero, it is convenient to use the one-sided PSD and integrate from zero to infinity. In addition, it is convenient to use the frequency *f* in Hz rather than ω in rad/s. The usual convention is to define the one-sided PSD as follows:

$$W(f) \equiv 4\pi S(2\pi f) \tag{IV.2-12}$$

With this definition, the mean square is equal to the integral of *W*(*f*) from zero to infinity. Then, Equation (IV.2-9) for random jitter accumulation becomes:

$$W_{Nr}(f) = \frac{\left|H(j2\pi f)\right|^2 \left(1-\left|H(j2\pi f)\right|^{2N}\right)}{1-\left|H(j2\pi f)\right|^2} W_{12}(f) + \frac{\left|H_e(j2\pi f)\right|^2 \left(1-\left|H(j2\pi f)\right|^{2N}\right)}{1-\left|H(j2\pi f)\right|^2} W_3(f) \tag{IV.2-13}$$

Equation (IV.2-11) for systematic jitter accumulation becomes:

$$W_{Ns}(f) = \left|H(j2\pi f)\right|^2 \left|\frac{1-H^N(j2\pi f)}{1-H(j2\pi f)}\right|^2 W_{12}(f) + \left|H_e(j2\pi f)\right|^2 \left|\frac{1-H^N(j2\pi f)}{1-H(j2\pi f)}\right|^2 W_3(f) \tag{IV.2-14}$$

Note that Equations (IV.2-13) and (IV.2-14) are the one-sided PSDs for the output phase noise. To obtain the PSDs for output jitter, these equations must be multiplied by the frequency responses of the appropriate jitter measurement filters. The jitter measurement filter consists of a first order high-pass filter followed by a third-order maximally-flat low-pass filter. The frequency response is given by:

$$\left|H_{meas}(j2\pi f)\right|^2 = \frac{f^2}{f^2 + f_{HP}^2} \times \frac{f_{LP}^6}{f^6 + f_{LP}^6} \tag{IV.2-15}$$

The cut-off frequencies f_{HP} and f_{LP} depend on the respective rate and whether the jitter is high-band or wideband. The specific values are given in Table 5.1-1.

Next, Equations (IV.2-13) and (IV.2-14) are rewritten using a dimensionless form of $H(j2\pi f)$. Following [b-Varma], define:

$$x = \frac{\omega}{\omega_n} = \frac{f}{f_n} \tag{IV.2-16}$$

Then the frequency responses $H(j\omega)$ and $H_e(j\omega)$ may be written (by dividing the numerator and denominator of Equations (IV.2-1) and (IV.2-3) by ω_n^2):

$$H(x) = \frac{2\zeta jx + 1}{-x^2 + 2\zeta jx + 1} \tag{IV.2-17}$$

$$H_e(x) = \frac{-x^2}{-x^2 + 2\zeta j x + 1} \tag{IV.2-18}$$

In addition, Equation (IV.2-15) for the jitter measurement filter becomes:

$$H_{meas}(x) = \frac{x^2}{x^2 + (f_{HP}/f_n)^2} \times \frac{(f_{LP}/f_n)^6}{f^6 + (f_{LP}/f_n)^6} \tag{IV.2-19}$$

Then Equations (IV.2-13) and (IV.2-14) become:

$$W_{Nr}(x) = \frac{|H(x)|^2\left(1 - |H(x)|^{2N}\right)}{1 - |H(x)|^2} W_{12}(x) + \frac{|H_e(x)|^2\left(1 - |H(x)|^{2N}\right)}{1 - |H(x)|^2} W_3(x) \tag{IV.2-20}$$

$$W_{Ns}(x) = |H(x)|^2 \left|\frac{1 - H^N(x)}{1 - H(x)}\right|^2 W_{12}(x) + |H_e(x)|^2 \left|\frac{1 - H^N(x)}{1 - H(x)}\right|^2 W_3(x) \tag{IV.2-21}$$

(Equations (IV.2-17) to (IV.2-21) are slightly imprecise in the notation because the same symbols for the functions *H* and *W* are used when expressed in terms of *x* rather than *f*; to be more precise, new symbols should have been defined, but this would have been cumbersome.)

The advantage of the dimensionless forms of Equations (IV.2-17) to (IV.2-21) is that the dependence on the undamped natural frequency or, in essence, the regenerator bandwidth, is gone. The regenerator frequency responses in Equations (IV.2-17) and (IV.2-18) depend only on damping ratio, or, equivalently, on gain peaking. The jitter measurement filter frequency response in Equation (IV.2-19) depends only on the ratio of the high-pass and low-pass filter cut-off frequencies to the regenerator undamped natural frequency or, equivalently, bandwidth. These ratios are the same for the different OTUk rates as long as the values scale with rate; since the gain peaking requirement is also the same for all the rates (0.1 dB), this means that the PSDs may be evaluated once for a given set of ratios, rather than once for each rate.

Finally, the mean square phase and jitter are equal to the appropriate PSD integrated over *f* from 0 to infinity:

$$\sigma^2 = \int_0^\infty W(f)df = f_n \int_0^\infty W(x)dx \tag{IV.2-22}$$

In other words, to obtain the mean square phase or jitter we integrate the dimensionless PSD and multiply by the undamped natural frequency for the respective rate. In addition, and this is most important, it means that the ratio of the mean-square or rms phase or jitter for *N* regenerators to that for one regenerator is independent of the undamped natural frequency and, for the cases here, is the same for all OTUk (because the jitter measurement filter bandwidths and regenerator bandwidths are in the same ratios for all OTUk). This means that the simulations only need to be done once for each set of frequency ratios, rather than once for each value of k and each set of frequency ratios, which reduces the amount of simulation by a factor of 3.

In the examples here, the noise source N_{12} is modelled as white noise:

$$W_{12}(f) = W_{0,12} \tag{IV.2-23}$$

In addition, the noise source N_3 represents VCO noise. A model for this is given in [b-Wolaver] and [b-Leeson]. The VCO PSD is primarily white noise above a frequency f_b, and WFM below f_b:

$$W_3(f) = W_{0,3}\left(1 + \left(\frac{f_b}{f}\right)^2\right) \tag{IV.2-24}$$

Equation (IV.2-24) is shown schematically in Figure IV.2-2 (the figure is intended to be a log-log plot; the actual curve would be 3 dB above the breakpoint at frequency f_b). The frequency f_b is given by:

$$f_b = \frac{f_0}{2Q} \tag{IV.2-25}$$

where f_0 is the line rate (oscillator frequency) and Q is the quality factor. Inserting Equation (IV.2-25) into Equation (IV.2-24) and dividing numerator and denominator by f_n so that the result may be written in terms of the dimensionless parameter x:

$$W_3(x) = W_{0,3}\left(1 + \left[\frac{(f_0 / f_n)}{2Qx}\right]^2\right) \tag{IV.2-26}$$

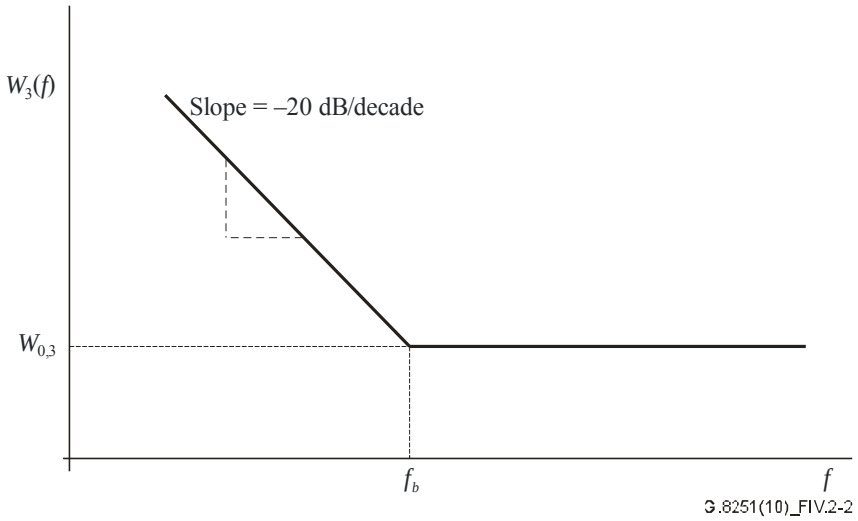


Figure IV.2-2 – Schematic of VCO power spectral density

In the examples in the next clause, the ratios of high-band and wideband jitter accumulation for N regenerators to the respective jitter for one regenerator, for the N_{12} noise source and for the N_3 noise source separately, are evaluated. This means that the PSD magnitude coefficients $W_{0,12}$ and $W_{0,3}$ cancel on taking the ratio. The results depend only on damping ratio (or, equivalently, gain peaking), ratio of jitter measurement filter cut-off frequencies to undamped natural frequency (or, equivalently, regenerator bandwidth), and, for the N_3 noise source, ratio of line rate to undamped natural frequency and VCO Q-factor. This may be expressed:

$$\frac{\sigma_{12,N}}{\sigma_{12,1}} = F_{12}(a_{LP}, a_{HP}, \varsigma) \tag{IV.2-27}$$

$$\frac{\sigma_{3,N}}{\sigma_{3,1}} = F_3(a_{LP}, a_{HP}, \varsigma, a_0, Q) \tag{IV.2-28}$$

where:

$$a_{HP} = \frac{f_{HP}}{f_n}$$
$$a_{LP} = \frac{f_{LP}}{f_n} \qquad \text{(IV.2-29)}$$
$$a_0 = \frac{f_0}{f_n}$$

The functions F_{12} and F_3 are different for the random and systematic cases; in addition, a_{HP} is different for high-band and wideband jitter. But, the functions and the quantities are the same for all three rates (for a given set of frequency ratios) because the various bandwidths are in the same ratios for all three rates.

The relation between undamped natural frequency and 3 dB bandwidth, and between gain peaking and damping ratio, are [see [b-Gardner] for Equation (IV.2-30) and [b-Wolaver] for Equation (IV.2-31)]:

$$f_{3dB} = f_n \left[2\varsigma^2 + 1 + \sqrt{\left(2\varsigma^2 + 1\right)^2 + 1} \right]^{1/2} \qquad \text{(IV.2-30)}$$

$$H_p = 1 + \frac{1}{4\varsigma^2} \qquad \text{(IV.2-31)}$$

The gain peaking, H_p, in Equation (IV.2-31), is a pure fraction (i.e., the gain peaking in dB is equal to 20 times the log to base 10 of $H_p - 1$ in Equation (IV.2-31)).

A C program was used to evaluate mean-square and rms high-band jitter and wideband jitter by numerical integration of the filtered PSD. PSDs were evaluated using a frequency step that was always taken to be less than 0.1 times the minimum bandwidth or cut-off frequency (i.e., less than 0.1 times the wideband jitter high-pass filter cut-off frequency). The extent of the PSD was always taken to be more than 10 times the maximum bandwidth or cut-off frequency (i.e., more than 10 times the low-pass jitter filter cut-off frequency). Note that the jitter measurement filter imposes a maximum bandwidth on the system; i.e., the PSD can be integrated to infinite frequency and the result will converge because of the jitter measurement low-pass filter (we truncate the integration at sufficiently high frequency that the contribution above that frequency is negligible, but not at such high frequency that the simulation time is prohibitive).

IV.2.2 Model results

Simulations were run for two sets of regenerator bandwidths, corresponding to SDH requirements in [ITU-T G.783] and OTN requirements in this Recommendation. The former have 3 dB bandwidths of 2 MHz, 8 MHz, and (by extrapolation) 32 MHz for STM-16, STM-64, and STM-256 respectively. These values were used for OTU1, OTU2, and OTU3, respectively. The latter have 3 dB bandwidths of 250 kHz, 1 MHz, 4 MHz for OTU1, OTU2, and OTU3, respectively. All the simulation cases assumed random jitter accumulation.

General parameters for each of the sets of cases are summarized in Table IV.2-1 (SDH bandwidth cases) and in Tables IV.2-2a and IV.2-2b (OTN bandwidth cases). For the requirements of this Recommendation, it was necessary to make separate runs for OTU3 wideband jitter accumulation. This is because the OTU3 wideband jitter high-pass measurement filter bandwidth is the same as that for OTU2 (i.e., it does not scale by a factor of 4 relative to OTU2, as the other parameters do). Parameters for the OTU1 and OTU2 simulation cases are given in Table IV.2-2a; parameters for the OTU3 simulation cases are given in Table IV.2-2b. The jitter measurement filter bandwidths are

taken from Table 5.1-1. Note that damping ratio and undamped natural frequency are related to gain peaking and 3 dB bandwidth by Equations (IV.2-30) and (IV.2-31).

Table IV.2-1 – General parameters for the simulation cases based on [ITU-T G.783] regenerator bandwidths (2 MHz, 8 MHz, 32 MHz, for OTU1, OTU2, and OTU3, respectively)

Parameter	Value
Gain peaking H_p	1.0115 (0.1 dB)
Damping ratio ζ	4.6465
$f_{HP,wideband} / f_{3dB}$	2.5×10^{-3}
$f_{HP,highband} / f_{3dB}$	0.5
f_{LP}/f_{3dB}	10
f_0 / f_{3dB}	1339
f_{3dB} / f_n	9.4006

Table IV.2-2a – General parameters for the simulation cases based on OTU1 and OTU2 regenerator bandwidths (250 kHz and 1 MHz for OTU1 and OTU2, respectively)

Parameter	Value
Gain peaking H_p	1.0115 (0.1 dB)
Damping ratio ζ	4.6465
$f_{HP,wideband} / f_{3dB}$	2.0×10^{-2}
$f_{HP,highband} / f_{3dB}$	4.0
f_{LP} / f_{3dB}	80
f_0 / f_{3dB}	10710
f_{3dB} / f_n	9.4006

Table IV.2-2b – General parameters for the simulation cases based on OTU3 regenerator bandwidths (4 MHz)

Parameter	Value
Gain peaking H_p	1.0115 (0.1 dB)
Damping ratio ζ	4.6465
$f_{HP,wideband} / f_{3dB}$	5.0×10^{-3}
$f_{HP,highband} / f_{3dB}$	4.0
f_{LP} / f_{3dB}	80
f_0 / f_{3dB}	10755
f_{3dB} / f_n	9.4006

For each set of bandwidths, results are presented for the following cases:

- low-pass filtered noise (e.g., in optical receiver, phase detector, etc.);
- high-pass filtered noise (e.g., in VCO):
  - only WPM (infinite Q);
  - WPM and WFM (Q = 535);
  - WPM and WFM (Q = 100);
  - WPM and WFM (Q = 30).

The three cases with finite Q factor correspond, for OTU2, to the cut-off frequency f_b between WFM and WPM equal to 10 MHz, 53.5 MHz, and 178 MHz. The cases are intended to represent a range of Q factor (the first value was chosen to correspond to a "round" number for cut-off frequency (for the OTU2 case)).

IV.2.2.1 Results for cases based on SDH regenerator bandwidths [ITU-T G.783]

Figures IV.2-3a and IV.2-3b show high-band and wideband jitter accumulation results for the case of low-pass filtered white noise and the case of high-pass filtered white (i.e., WPM only) noise, assuming random jitter accumulation. Figure IV.2-3a shows accumulation over up to 1000 3R regenerators, on a log-log scale. Figure IV.2-3b presents the results on a linear scale; the plot stops at 200 3R regenerators so that results for smaller numbers of regenerators are visible on the scale of the plot.

The results show that:

- wideband jitter accumulates more rapidly than high-band jitter;
- noise introduced via a low-pass filter accumulates more rapidly than noise introduced via a high-pass filter.

Regarding the second bullet item, the noise introduced via a high-pass filter hardly accumulates at all until the number of 3R regenerators reaches a few hundred. This lack of accumulation is due to the fact that most of the noise is above the bandwidth of the regenerator; noise introduced in one regenerator is heavily filtered by subsequent regenerators. Note, however, that there is no WFM in the VCO here. The rapid increase after the number of regenerators reaches several hundred is due to the gain peaking of the regenerators.

The results show that after 100 regenerators, wideband and high-band jitter have accumulated by factors of approximately 5.5 and 2.0, respectively, for low-pass model white noise, and by factors of less than 1.1 for high-pass model white noise. After 1000 regenerators, wideband and high-band jitter have accumulated by factors of approximately 21'000 and 2500, respectively, for low-pass model white noise, and by factors of approximately 400 and 45, respectively, for high-pass model white noise.

Figures IV.2-4a and IV.2-4b show high-band and wideband jitter accumulation results for the case of high-pass filtered noise with various amounts of WFM. The relative amount of WFM is indicated via the Q factor; as indicated above, the three cases correspond to cut-off frequencies of 10 MHz (Q = 535), 53.5 MHz (Q = 100), and 178 MHz (Q = 30) for the OTU2 rate (see Equation (IV.2-25)). A smaller Q indicates a larger relative amount of WFM; Equations (IV.2-24) and (IV.2-25) indicate that reducing Q by a factor increases the WFM component by that factor. As expected, jitter accumulation is larger for the cases with larger WFM component (smaller Q factor). The Q = 535 cases show jitter accumulation approaching about half the accumulation for the low-pass filtered noise case of Figures IV.2-3a and IV.2-3b. In contrast, the Q = 100 and Q = 30 cases show larger accumulation that is very close to that of the low-pass filtered noise case of Figures IV.2-3a and IV.2-3b, for both high-band and wideband jitter. This agreement between the low-pass and high-pass model results is due to the fact that, for this range of Q factor

(i.e., below 100) and for the ratios of regenerator to measurement filter bandwidths used here, the result of passing WFM through a high-pass filter gives similar noise to that of passing WPM through a low-pass filter.

Note also that the jitter accumulation for the Q = 100 and Q = 30 cases is very similar. This is because, for both of these cases, the frequency f_b is sufficiently above the regenerator bandwidth that the WFM contribution dominates. To see this, note that f_0/f_{3dB} is 1339 (Table IV.2-1), which is sufficiently large compared to the Q factor for these cases (30 and 100). Note that no claim is being made that absolute jitter accumulation is the same in both these cases; the results in Figures IV.2-4a and IV.2-4b are for relative jitter accumulation (jitter out of the jth regenerator divided by jitter out of the first regenerator, and it is this quantity that is the same for both cases).

The results so far show how rapidly high-band and wideband jitter accumulate for various noise models. However, it is also of interest to know whether, for a given model, the respective high-band or wideband jitter generation limit is more stringent. To determine this, the ratio of wideband to high-band jitter generation for a single regenerator, for each model is needed (assuming the same noise source for high-band and wideband jitter generation). The ratios are given in Table IV.2-3.

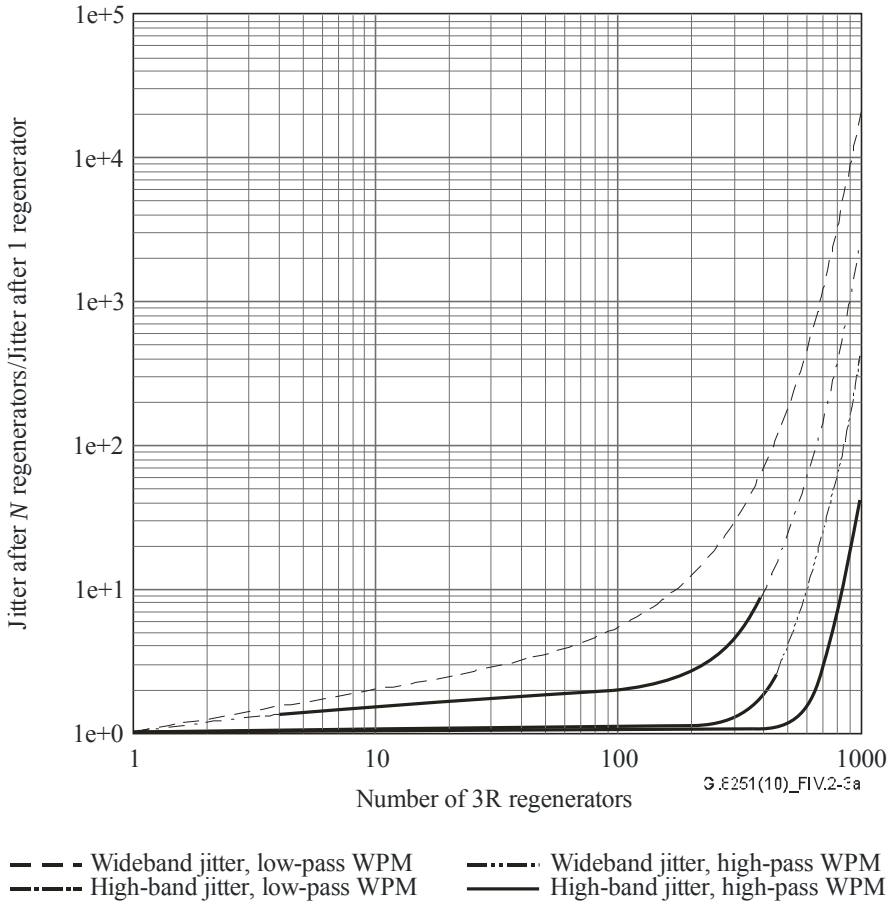
Table IV.2-3 – Ratio of wideband to high-band rms jitter generation, for one 3R regenerator (SDH 3 dB bandwidths)

Case	Ratio
Low-pass filtered noise	1.2500
High-pass filtered noise, no WFM	1.0136
High-pass filtered noise, with WFM (Q = 535)	1.0502
High-pass filtered noise, with WFM (Q = 100)	1.2078
High-pass filtered noise, with WFM (Q = 30)	1.2400

The ratios indicate that, for the high-pass noise models, wideband jitter generation is not appreciably larger than high-band jitter generation. Even for the low-pass noise model, the former is only 25% larger than the latter. These ratios are considerably less than the factor of 3 difference between the wideband and high-band jitter generation requirements (0.3 UIpp versus 0.1 UIpp for wideband and high-band, respectively; see Table A.5-1).

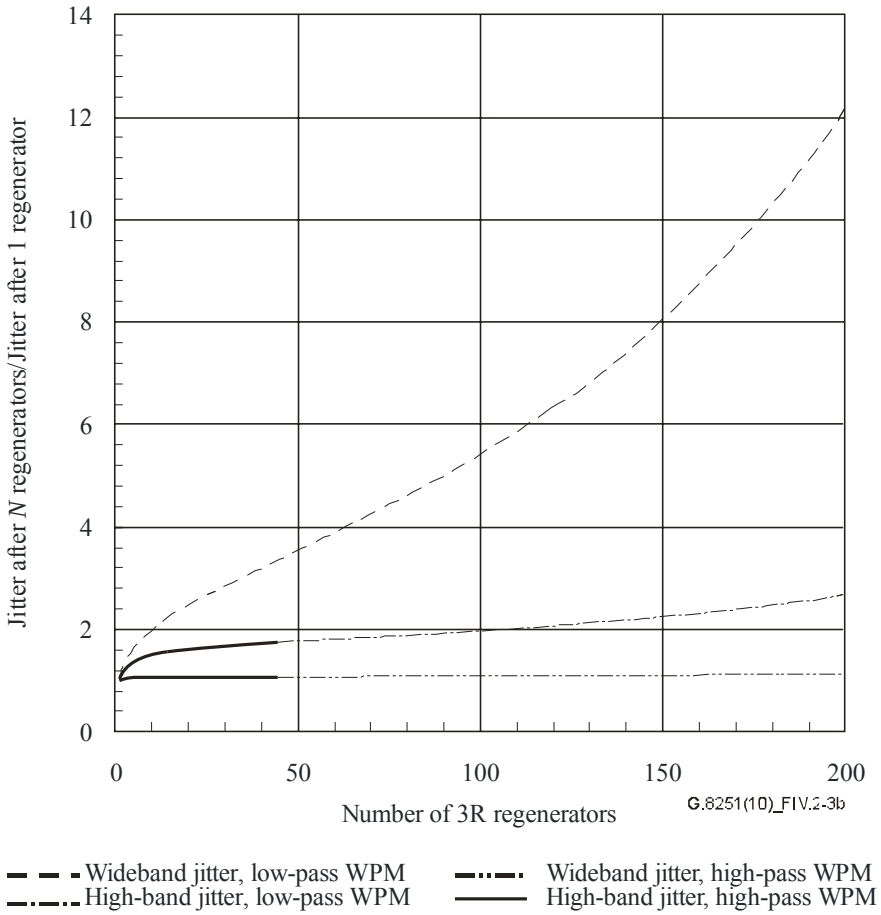
The results (Figures IV.2-3, IV.2-4, and Table IV.2-3) may now be used to assess whether the jitter network limits of Table 5.1-1 can be satisfied for a reference chain of 50 3R regenerators, assuming the regenerators satisfy the SDH requirements of [ITU-T G.783] (and the answer is that the network limits cannot be satisfied in this case). Figure IV.2-3b shows that, for low-pass WPM noise, the high-band jitter accumulation reaches a factor of 1.5 after approximately 10 regenerators, and is between 1.5 and 2.0 after 50 regenerators. Figure IV.2-4b shows that, for high-pass noise with Q = 30 or 100, the high-band jitter accumulation reaches a factor of 1.5 after approximately 10 and 15 regenerators, respectively, and is between 1.5 and 2.0 after 50 regenerators. Since the ratio of the high-band jitter network limit to high-band jitter generation requirement is 1.5 (i.e., 0.15/0.1), it is seen that a reference chain of regenerators, each of which meet the jitter generation requirements and has low or moderate Q factor, will not meet the jitter network limit. In fact, the network limit will be exceeded after approximately 10 or 11 regenerators. It is only in the high Q factor cases (Q = 535, or the high-pass WPM case, which corresponds to $Q \rightarrow \infty$) where the network limit can be met after 50 regenerators; for these cases there is almost no high-band jitter accumulation. Note that for the Q = 535 case, the wideband jitter accumulation after 50 regenerators is approximately a factor of 1.9. This meets the wideband jitter network limit, as the ratio of the network limit to generation requirement is 5 (i.e., 1.5/0.3).

In a case where both low-pass and high-pass (VCO) noise are present, it is, in principle, necessary to know the relative amount of each. This plus the simulation results that gave rise to Figures IV.2-3 and IV.2-4 could be used to construct similar curves for the combined case. However, the above results do show that if the *Q* factor is sufficiently small (i.e., less than approximately 100, and certainly for values around 30), the low-pass and high-pass noise models give similar results for relative jitter accumulation. For these cases, it is not necessary to perform separate simulations of high-pass and low-pass filtered noise, nor is it necessary to know the relative amount of each noise type; instead, it is necessary only to know the total noise generation (and regenerator bandwidth and gain peaking) to determine the jitter accumulation.



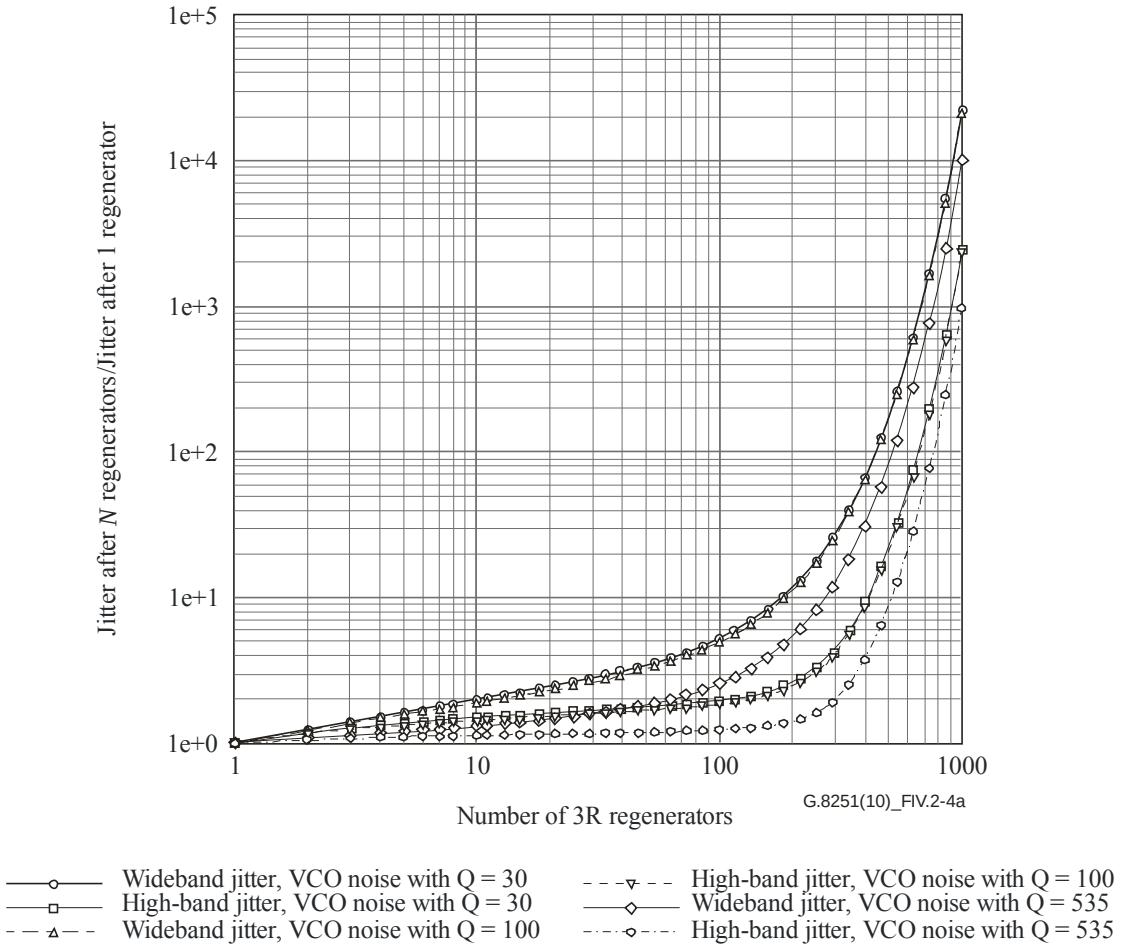
NOTE – Assumptions are: 3R regenerator bandwidths meet ITU-T G.783 (SDH) requirements, random jitter accumulation, no WFM in VCO (high-pass) noise cases. Log-log plot.

Figure IV.2-3a – Relative increase in jitter over *N* 3R regenerators



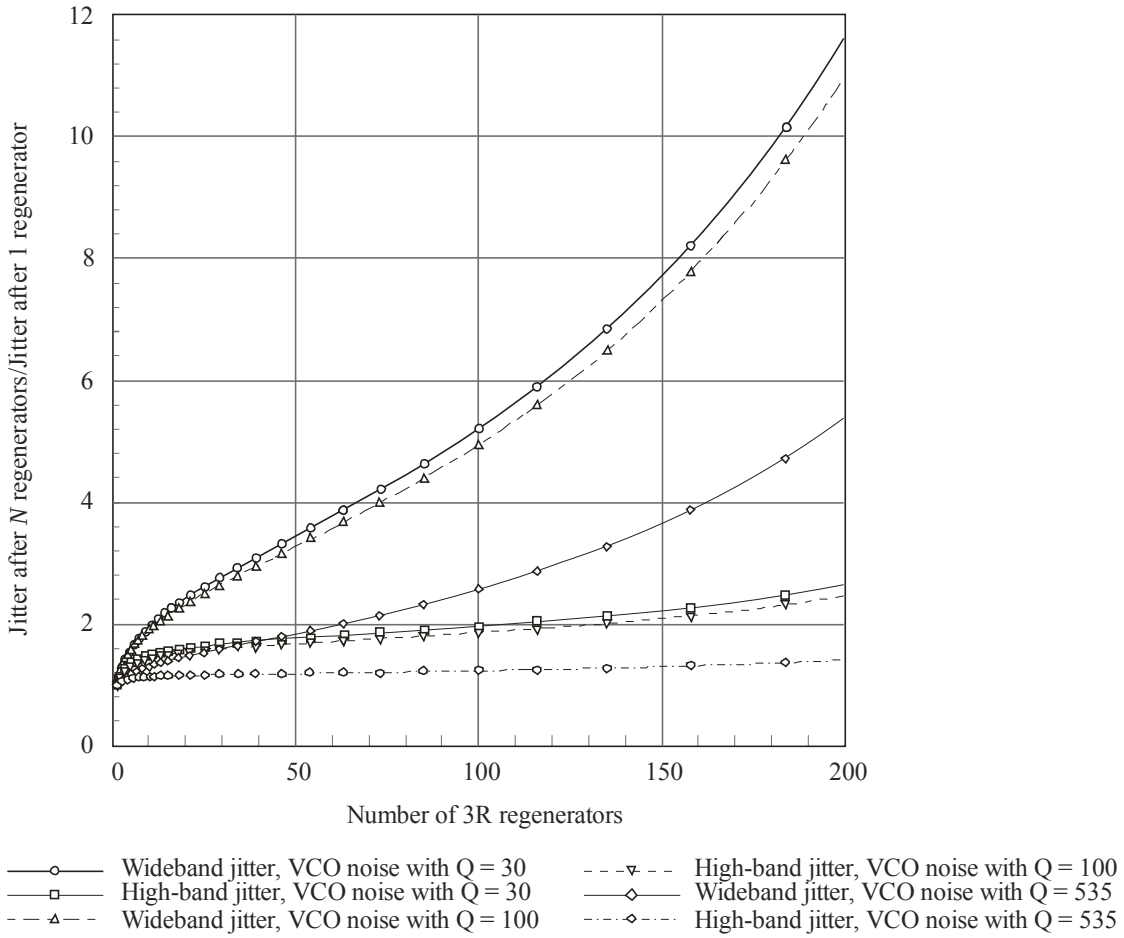
NOTE – Assumptions are: 3R regenerator bandwidths meet ITU-T G.783 (SDH) requirements, random jitter accumulation, no WFM in VCO (high-pass) noise cases. Linear plot.

Figure IV.2-3b – Relative increase in jitter over *N* 3R regenerators



NOTE – Assumptions are: 3R regenerator bandwidths meet ITU-T G.783 (SDH) requirements, random jitter accumulation, VCO (high-pass) noise with WFM and WPM and indicated *Q*-factor. Log-log plot.

Figure IV.2-4a – Relative increase in jitter over *N* 3R regenerators



NOTE – Assumptions are: 3R regenerator bandwidths meet ITU-T G.783 (SDH) requirements, random jitter accumulation, VCO (high-pass) noise with WFM and WPM and indicated *Q*-factor. Linear plot.

G.8251(10)_FIV.2-4b

Figure IV.2-4b – Relative increase in jitter over *N* 3R regenerators

IV.2.2.2 Results for cases based on OTN 3R regenerator bandwidths (in this Recommendation): High-band jitter for OTU1, OTU2, and OTU3; Wideband jitter for OTU1 and OTU2

Figures IV.2-5 and IV.2-6 (parts a and b for each figure) show wideband jitter results for OTU1 and OTU2 3R regenerators and high-band jitter results for OTU1, OTU2, and OTU3 3R regenerators. The 3 dB bandwidths are narrower than the corresponding SDH regenerator bandwidths by a factor of 8. Figures IV.2-5a and IV.2-5b show high-band and wideband jitter accumulation results for the case of low-pass filtered white noise and the case of high-pass filtered white (i.e., WPM only) noise, assuming random jitter accumulation. Figures IV.2-6a and IV.2-6b show high-band and wideband jitter accumulation results for the case of high-pass filtered noise with various amounts of WFM. As with the previous cases, based on SDH regenerator bandwidths, the relative amount of WFM is indicated via the *Q* factor; the *Q* factor values used here were the same as in the SDH cases (*Q* = 30, 100, 535). A smaller *Q* indicates a larger relative amount of WFM.

Table IV.2-4 shows the ratio of wideband to high-band jitter generation for a single regenerator, for each model (assuming the same noise source for high-band and wideband jitter generation). Comparing with the results in Table IV.2-3 for SDH bandwidths, it is seen that the ratio of wideband to high-band jitter accumulation is larger here. In addition, the degree to which this ratio is larger here is greater for cases where there is a larger portion of noise in the low frequency part of the spectrum. For the low-pass filtered noise case, this is due to the fact that more noise is filtered out in the high-band jitter measurement than in the wideband jitter measurement, and the relative

amount of noise remaining after filtering in the wideband measurement, relative to the high-band measurement, is larger as the regenerator bandwidth is made narrower. For high-pass filtered noise models, the effect is the same as in the low-pass filtered noise model as the *Q* factor decreases, because for smaller *Q* factor the noise generation at low frequencies looks more like the low-pass filtered noise model.

Table IV.2-4 – Ratio of wideband to high-band rms jitter generation, for one OTU1 or OTU2 3R regenerator (OTN 3 dB bandwidths from Table A.7-1)

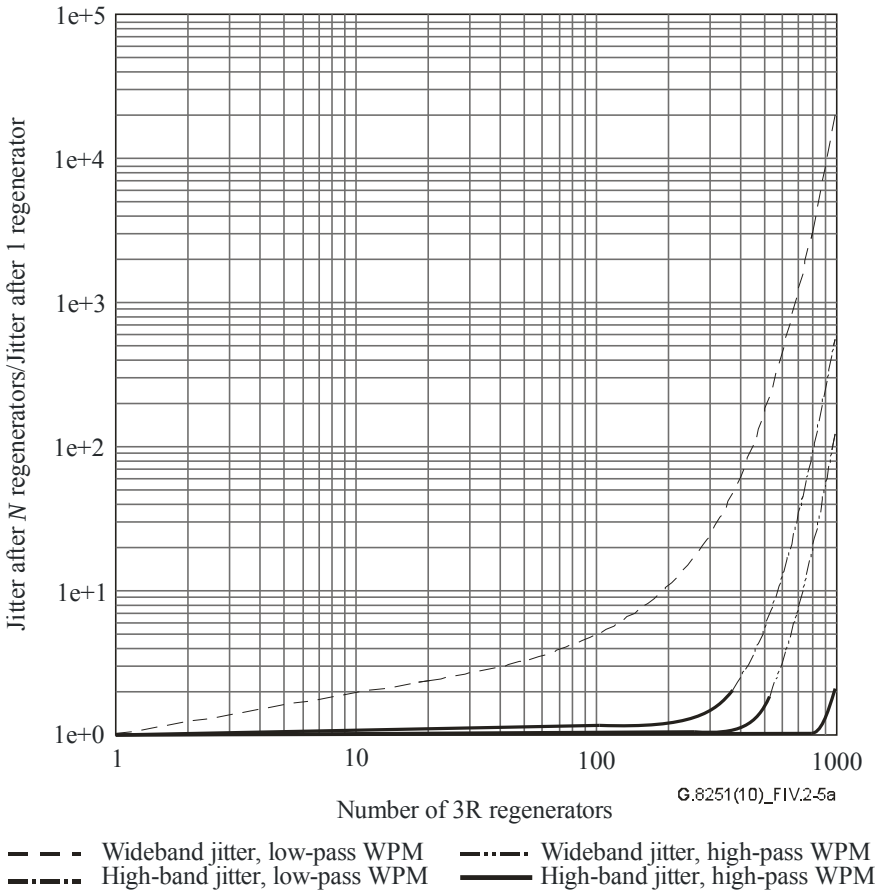
Case	Ratio
Low-pass filtered noise	2.2725
High-pass filtered noise, no WFM	1.0308
High-pass filtered noise, with WFM (*Q* = 535)	1.4862
High-pass filtered noise, with WFM (*Q* = 100)	2.1927
High-pass filtered noise, with WFM (*Q* = 30)	2.2605

The jitter accumulation results are qualitatively similar to those for the corresponding SDH cases, except that in general there is less jitter accumulation. For example, after 100 regenerators the wideband jitter accumulates by a factor of approximately 5 for the case of low-pass filtered noise (Figure IV.2-5b) and by factors of approximately 4.8, 4.8, and 4 for the case of high-pass filtered noise with *Q* = 30, 100, and 535, respectively. The corresponding jitter accumulation factors for the SDH regenerator bandwidth cases are 5.5, 5.2, 5, and 2.6, respectively. Note that the only one of these cases where there is less SDH jitter accumulation is the high-pass filtered noise with *Q* = 535 case. As in the SDH regenerator bandwidth cases, the jitter accumulation for the *Q* = 100 and *Q* = 30 cases is very similar.

The results (Figures IV.2-5 and IV.2-6, and Table IV.2-4) may now be used to assess whether the OTU1 and OTU2 jitter network limits of Table 5.1-1 can be satisfied for a reference chain of 50 3R regenerators, assuming the regenerators satisfy the OTN requirements of Table A.7-1 (and the answer is that the network limits can be satisfied in this case). Figure IV.2-5b shows that, for both low-pass and high-pass WPM noise, the high-band jitter accumulation remains very close to a factor of 1 up to 200 regenerators. Figure IV.2-6b shows that, for high-pass noise with *Q* = 30, 100, or 535, the high-band jitter accumulation also remains very close to a factor of 1 up to 200 regenerators. Since the ratio of the high-band jitter network limit to high-band jitter generation requirement is 1.5 (i.e., 0.15/0.1), it is seen that a reference chain of regenerators, each of which meet the jitter generation requirements, will meet the jitter network limit. The simulation results here show this for 200 regenerators; the high-band jitter network limit is certainly met for reference chains of 50 regenerators.

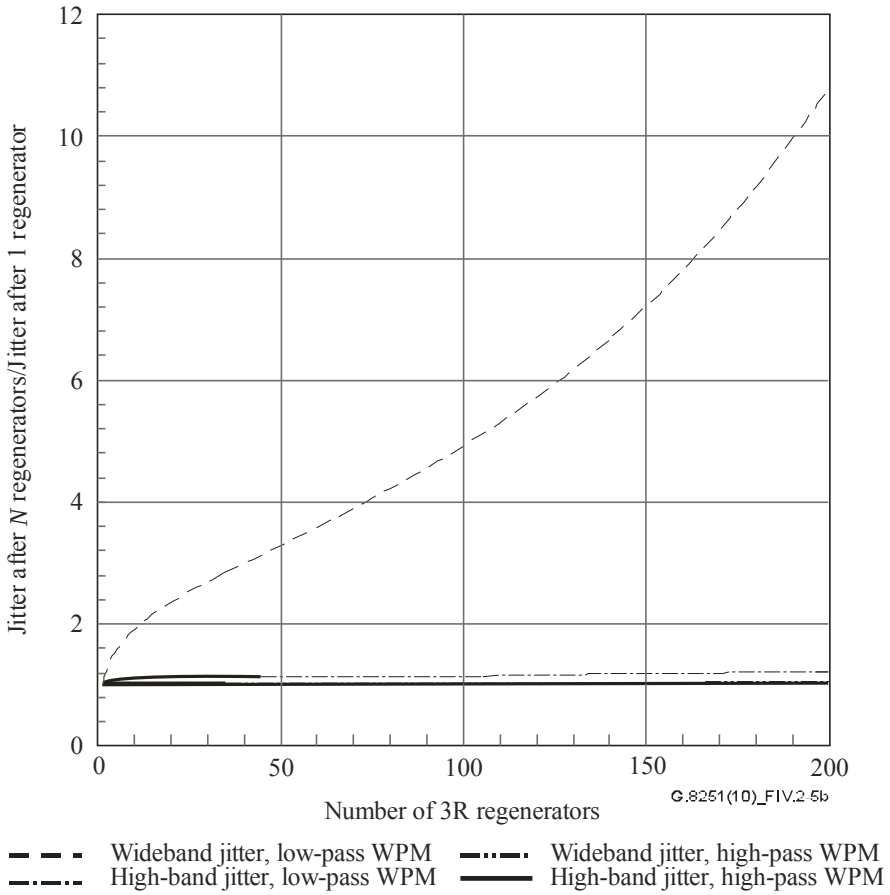
Table IV.2-4 indicates that the largest ratio of wideband to high-band jitter generation is approximately 2.27, which occurs for the low-pass filtered noise model. Since the ratio of the wideband to high-band jitter generation requirements is 3 (0.3/0.1), it is seen that a regenerator that meets the high-band jitter generation requirement will also meet the wideband jitter generation requirement.

Finally, Figures IV.2-5 and IV.2-6 show that the wideband jitter network limits are satisfied for a chain of 50 3R regenerators. The ratio of wideband jitter network limit to wideband jitter generation limit is 5 (1.5/0.3). Figure IV.2-5b shows that wideband jitter increases by factors of 5 and 1, after 100 regenerators, for low-pass filtered WPM and high-pass filtered WPM noise models, respectively. Figure IV.2-6b shows that wideband jitter increases by factors of 4.8, 4.8, and 4 after 100 regenerators, for high-pass filtered noise models with Q = 30, 100, and 535, respectively.



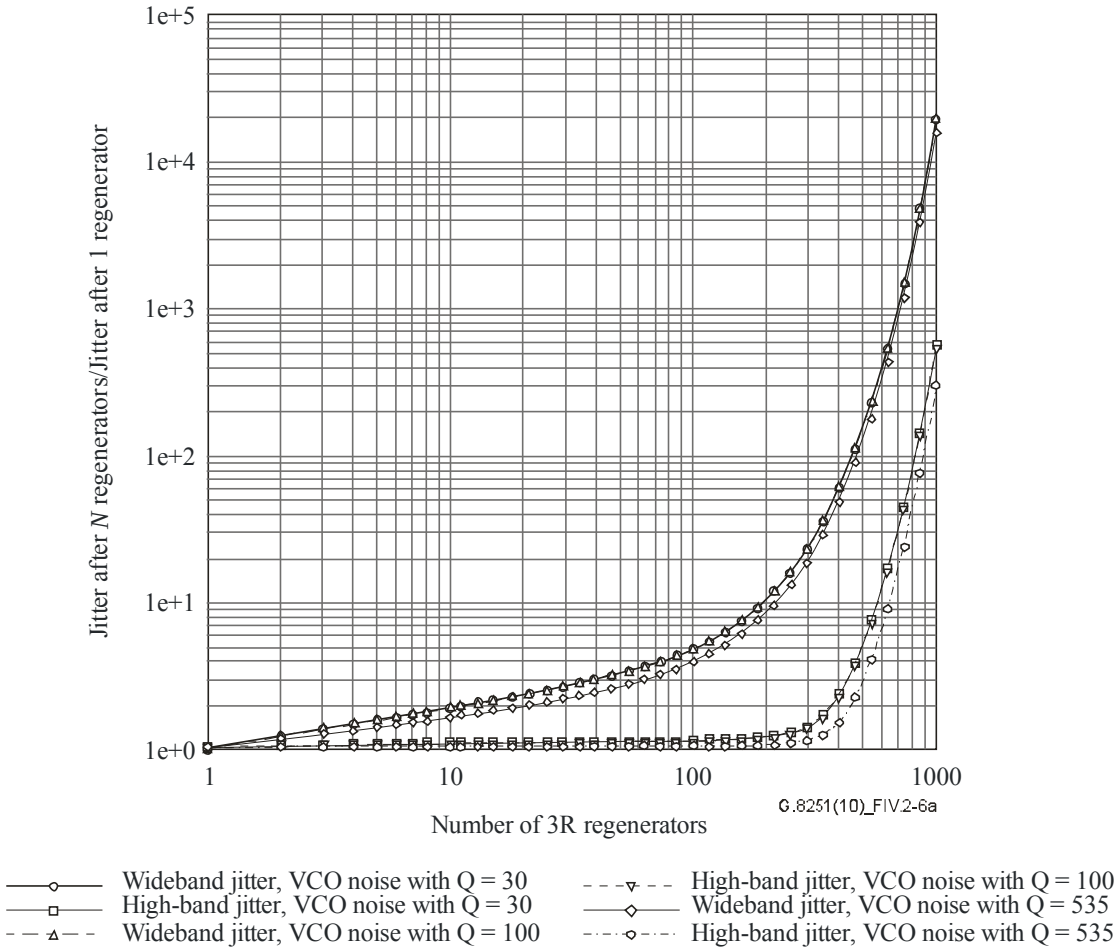
NOTE – Assumptions are: 3R regenerator bandwidths meet ITU-T G.8251 (OTN) requirements, random jitter accumulation, no WFM in VCO (high-pass) noise cases. Log-log plot.

Figure IV.2-5a – Relative increase in jitter over *N* 3R regenerators



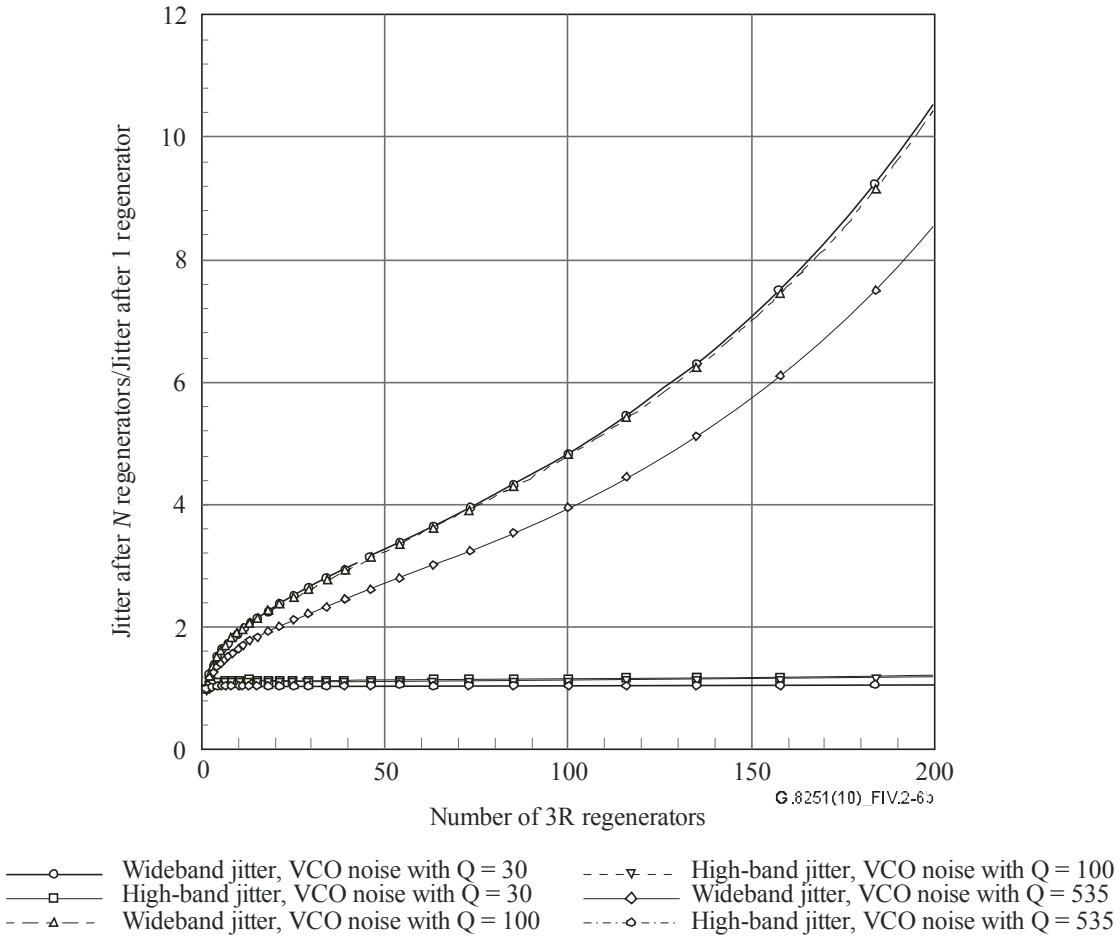
NOTE – Assumptions are: 3R regenerator bandwidths meet ITU-T G.8251 (OTN) requirements, random jitter accumulation, no WFM in VCO (high-pass) noise cases. Linear plot.

Figure IV.2-5b – Relative increase in jitter over *N* 3R regenerators



NOTE – Assumptions are: 3R regenerator bandwidths meet ITU-T G.8251 (OTN) requirements, random jitter accumulation, VCO (high-pass) noise with WFM and WPM and indicated *Q*-factor. Log-log plot.

Figure IV.2-6a – Relative increase in jitter over *N* 3R regenerators



NOTE – Assumptions are: 3R regenerator bandwidths meet ITU-T G.8251 (OTN) requirements, random jitter accumulation, VCO (high-pass) noise with WFM and WPM and indicated *Q*-factor. Linear plot.

Figure IV.2-6b – Relative increase in jitter over *N* 3R regenerators

IV.2.2.3 Results for cases based on OTN 3R regenerator bandwidths (in this Recommendation): Wideband jitter for OTU3

Figures IV.2-7a and IV.2-7b show results for OTU3 wideband jitter accumulation. Comparison with the results above for OTU1 and OTU2 shows almost no change (compare Figure IV.2-7a with the wideband jitter curves in Figures IV.2-5a and IV.2-6a; compare Figure IV.2-7b with the wideband jitter curves in Figures IV.2-5b and IV.2-6b). Table IV.2-4 gives the ratio of wideband to high-band rms jitter generation for a single 3R regenerator for OTU1 and OTU2. The corresponding results for OTU3, obtained from the new simulations, are given in Table IV.2-5 (with the results for OTU1 and OTU2 shown in parentheses for comparison). The results for OTU3 are also almost the same as the corresponding results for OTU1 and OTU2.

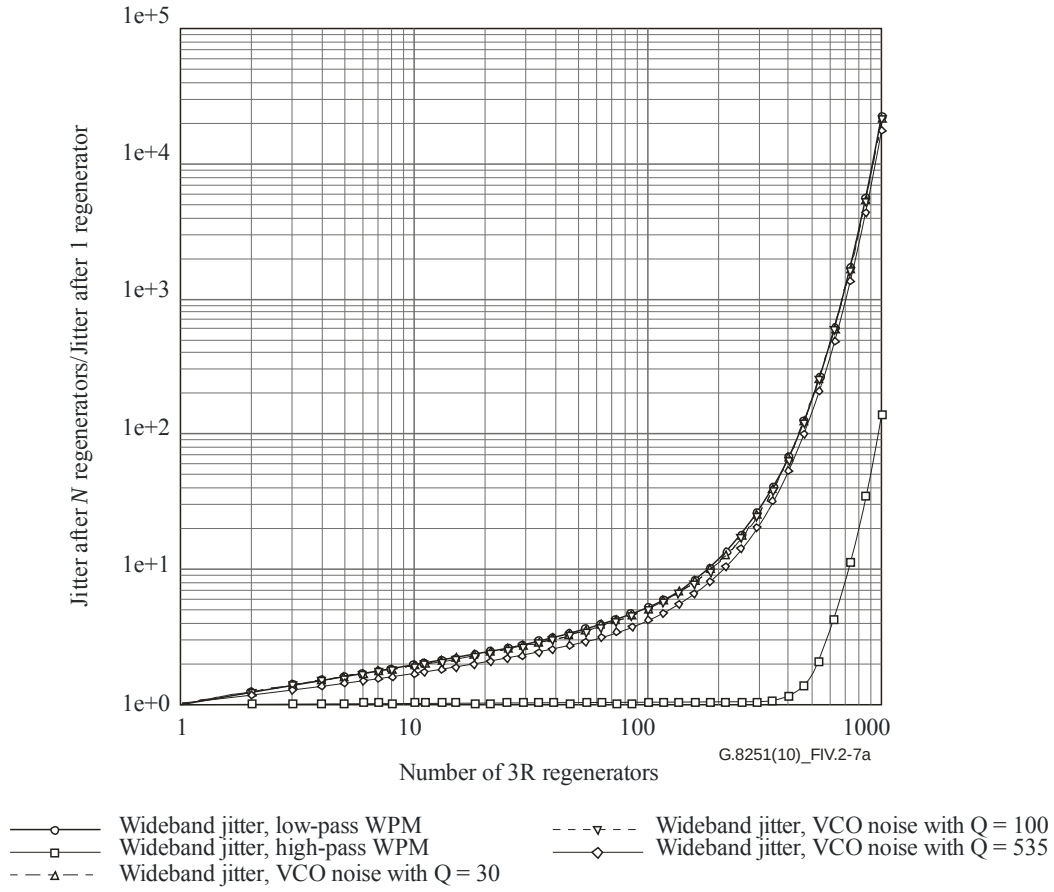
Table IV.2-5 – Ratio of wideband to high-band rms jitter generation, for one OTU3 3R regenerator (results for OTU1 and OTU2, from Table IV.2-4, shown in parentheses for comparison)

Case	Ratio
Low-pass filtered noise	2.2898 (compare to 2.2725)
High-pass filtered noise, no WFM	1.0308 (same)
High-pass filtered noise, with WFM (Q = 535)	1.4946 (compare to 1.4862)
High-pass filtered noise, with WFM (Q = 100)	2.2055 (compare to 2.1927)
High-pass filtered noise, with WFM (Q = 30)	2.2734 (compare to 2.2605)

The results may now be used to verify that the OTU3 jitter wideband jitter accumulation is acceptable. Table IV.2-5 shows that the worst ratio of wideband to high-band jitter generation (over all the noise models) is approximately 2.29 (versus 2.27 for OTU1 and OTU2). Since the ratio of the wideband to high-band jitter generation requirement is 12, it is seen that an OTU3 3R regenerator that meets the high-band jitter generation requirement will meet the wideband jitter generation requirement.

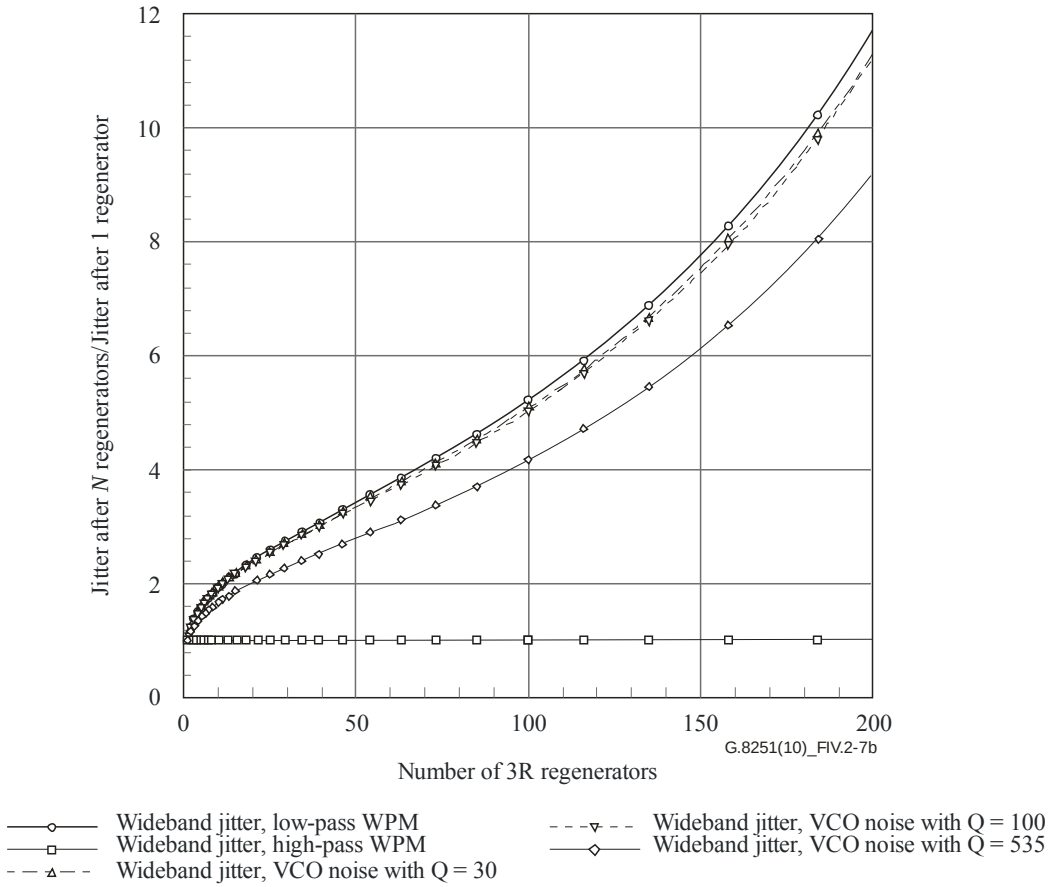
Finally, Figure IV.2-7b shows that the largest factor increase in wideband rms jitter after 100 regenerators, among all the noise models, is approximately 5.2, and occurs for low-pass filtered WPM. While this is larger than the ratio for wideband jitter network limit to wideband jitter generation of 5 (6.0/1.2), the network limit is still satisfied assuming the high-band jitter requirements are satisfied. This is because, based on the results in Table IV.2-5, meeting the high-band jitter generation of 0.1 UIpp means that the wideband jitter generation will only be 0.229 UIpp and not 1.2 UIpp. Therefore, the wideband jitter accumulation will be (5.2)(0.229) = 1.19 UIpp. In any case, note that this is for 100 regenerators; for 50 (as in Appendix III HRM) the wideband jitter increases by a factor of 3.4. This is well within the ratio of 5.

Therefore, the OTU3 wideband jitter generation requirements are consistent with the OTU3 jitter transfer bandwidth and Appendix III HRM.



NOTE – Assumptions are: 3R regenerator bandwidths meet ITU-T G.8251 (OTN) requirements; random jitter accumulation; noise models include: 1) low-pass filtered noise model, 2) VCO (high-pass filtered) noise model with no WFM, and 3) VCO (high-pass filtered) noise models with WFM and WPM and indicated *Q*-factor. Log-log plot.

Figure IV.2-7a – Relative increase in OTU3 wideband jitter over *N* 3R regenerators



NOTE – Assumptions are: 3R regenerator bandwidths meet ITU-T G.8251 (OTN) requirements; random jitter accumulation; noise models include: 1) low-pass filtered noise model, 2) VCO (high-pass filtered) noise model with no WFM, and 3) VCO (high-pass filtered) noise models with WFM and WPM and indicated *Q*-factor. Linear plot.

Figure IV.2-7b – Relative increase in OTU3 wideband jitter over *N* 3R regenerators

IV.3 Model 2

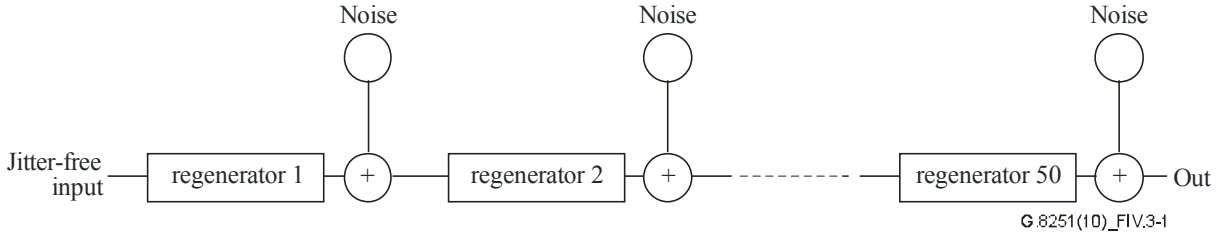


Figure IV.3-1 – Schematic of Model 2

IV.3.1 Introduction

A maximum number of 50 regenerators between mapping and subsequent demapping in an OTN island is assumed. A conservative approach in WDM systems using optical amplifiers and dispersion-compensating measures leads to a span of more than 300 km between two regeneration operations (total length of 15'000 km). The regenerator model used in previous work based on SDH regenerators is a second-order PLL which filters wideband noise. The wideband noise is assumed as pattern-dependent jitter with constant power spectral density. The 3 dB bandwidth of 8 MHz of the regenerator is the noise shaping filter. The value of the output jitter measured with a band pass filter (4 MHz to 80 MHz) is 0.01 UIrms. Details of the filter are described in [ITU-T G.825].

The same filtering as in [ITU-T G.825] is used here because of the similarity of the STM-64 regenerator and the OTU2 regenerator. The OTU2 bit rate is roughly 7.6% above that of the

STM-64. The maximum allowed jitter generation of a STM-64 regenerator in [ITU-T G.783] is given for two combinations of high-pass and low-pass filtering. The jitter value measured in the range between 4 MHz and 80 MHz should not exceed 0.1 UIpp. The value between 20 kHz and 80 MHz should not exceed 0.3 UIpp. This clearly means that roughly 90% of the total noise power could be concentrated in the range below 4 MHz.

Assuming an 8 MHz bandwidth and 0.1 dB gain peaking for such a regenerator would not allow to cascade it in a chain without exceeding the 0.15 UIpp jitter tolerance requirement in [ITU-T G.825]. The 0.15 UIpp requirement is the most important requirement. The 4 MHz high-pass filter actually simulates the alignment jitter of a clock recovery with an assumed 4 MHz bandwidth. This alignment jitter also describes the deviation of the sampling time from the static (jitter-free) sampling time inside the receive eye.

If a regenerator is used as in [ITU-T G.783], its bandwidth must be defined. The non-uniform noise distribution is the reason why the bandwidth of the regenerators must be reduced below the value of 8 MHz.

IV.3.2 Structure of the equivalent building blocks in the noise simulation

Each regenerator contains at its output a summation point where the intrinsic jitter is added. The noise spectrum is low-pass filtered white Gaussian noise. The regenerator jitter transfer function is modelled as a second order PLL with a gain peaking of 0.1 dB. The input of the regenerator must have a clock recovery PLL with corner frequency (i.e., 3 dB bandwidth) greater than 4 MHz (jitter acceptance) which adds some additional filtering to the jitter transfer function. This was not taken into account in the simulation because of the much larger bandwidth compared to the bandwidth of the dominant PLL.

This means that, for the simulation, the bandwidth of the regenerator is modelled only with the (dominant) transfer function of the PLL in the transmit part of the regenerator.

The spectral shaping of the noise source was chosen so that the total noise powers measured after the high-pass – low-pass filter combinations of 20 kHz/80 MHz and 4 MHz/80 MHz differ by a factor of 9. This corresponds to a factor of 3 in rms values and is equivalent to jitter values of 0.3 UIpp and 0.1 UIpp respectively. The noise source does not describe an absolute value. It is used as a normalized reference for the calculation of the accumulation.

The simulation shows that a bandwidth below 1.5 MHz is necessary in order to not exceed the 0.15 UIpp after 50 regenerator operations. Assuming some safety margin a value of 1 MHz is proposed.

The accumulated values for a chain of 50 regenerators with 1 MHz bandwidth, 0.1 dB gain peaking and the maximum allowed noise production according to the values in [ITU-T G.783] are:

– 0.122 UIpp in the upper frequency range;

– 0.815 UIpp in the frequency range from 20 kHz to 80 MHz.

The equivalent proposal for the bandwidth of an OTN regenerator carrying STM-16 client signals is 250 kHz.

IV.4 Jitter generation of regenerators using parallel serial conversion

Regenerators using only one PLL, i.e., the clock recovery, may have requirements which could be contradictory. They have to perform some filtering and their bandwidth has to be large enough to fulfil the jitter tolerance requirement.

The jitter tolerance requires a bandwidth which has to be above the frequency where the first 1/f slope starts. This could lead to a relatively high jitter generation exceeding the maximum allowed value. Generally speaking it is not the purpose of the clock recovery to minimize jitter.

Main requirements for the clock recovery in order to optimize the bit error performance are:

- keeping the sampling time for the data retiming flipflop independent of the clock frequency at the position of the optimum eye opening (e.g., by using an integrating control loop);
- following the phase modulation of the incoming signal without deviating too much from the ideal sampling time (i.e., jitter tolerance);
- generating a low intrinsic jitter in terms of peak-to-peak values which should not exceed a small portion of the usable eye opening.

  This last bullet point clearly does not contain any requirement regarding the spectral distribution of the intrinsic jitter.

Unlike the measurement of jitter using band-limiting filters, the jitter generated in the clock recovery has to be considered without any filtering because it describes the deviation of the ideal sampling time.

In the case of very high bit rates it could be a problem having a clock recovery which is optimized for error performance while not taking care of the output jitter.

The concept to overcome this difficulty is the use of a serial parallel conversion where the incoming signal normally is converted into bytes. This so-called deserializer often uses a structure of 16 parallel bits.

At this level, the frequency where the data processing can be done is reduced by a factor of 16. This allows the use of a phase-locked loop that performs a dejitterizer function with a reduced bandwidth. At the output of such a regenerator the only jitter is that of this PLL and the reasonably low jitter of the PLL performing the multiplexer function and multiplying the clock frequency by a factor of 16.

These concepts allow for higher values of low frequency intrinsic jitter because of the narrower bandwidth of the dejitterizer function. This function filters these phase noise components in regenerators to such a degree that the accumulation in chains, defined in the HRM of Appendix III, does not exceed the network limit.

An example of this is the maximum intrinsic jitter for OTU3 in Table A.5-1. This can be 1.2 UIpp in the low frequency range.

This value very clearly addresses the possible use of such a triple PLL concept because a value of 1.2 UIpp clearly is not allowed in a one-stage (only clock recovery) regenerator. As shown above, it would produce bit errors.

Appendix V

Additional background on demapper (ODCp) phase error and demapper wideband jitter generation requirements

(This appendix does not form an integral part of this Recommendation)

V.1 Introduction

Clause A.7.3 contains the jitter transfer requirements for the demapper clock, i.e., the ODCp. Clause V.2 provides additional information on demapper phase error.

Clause A.5.1.2 contains the jitter generation requirements for the ODCp. It is stated there that one purpose of the ODCp wideband jitter generation requirements is to ensure that the gaps due to fixed overhead in the OTUk frame will not cause excessive output jitter. The wideband jitter generation for ODCp is limited to 1.0 UIpp for STM-16, STM-64, and STM-256 demappers. Clause V.3 provides additional information and background on this requirement.

V.2 Demapper phase error

The demapper (i.e., desynchronizer) is modelled as a second order phase-locked loop (PLL) with 20 dB/decade roll-off. The model is the same as the 3R regenerator Model 1 described in clause IV.2 and illustrated in Figure IV.2-1; only the numerical values of the parameters are different. Referring to Figure IV.2-1 and Equation (IV.2-1), the transfer function for the desynchronizer is:

$$H(s)=\frac{K_aK_os+K_aK_ob}{s^2+K_aK_os+K_aK_ob} \tag{V.2-1}$$

where K_a is the phase detector gain, K_o is the VCO gain, and b is the integral time constant assuming a PI loop filter with transfer function $1+b/s$. The phase error transfer function, i.e., the transfer function between the PLL input and the difference between the PLL output and input, is given by Equation (IV.2-7):

$$H_e(s)\equiv 1-H(s)=\frac{s^2}{s^2+K_aK_os+K_aK_ob} \tag{V.2-2}$$

Combining the phase detector gain and VCO gain to obtain an overall proportional time constant τ_p:

$$\tau_p=\frac{1}{K_aK_o} \tag{V.2-3}$$

and defining the integral time constant $\tau_i = 1/b$, the phase error transfer function may be rewritten:

$$H_e(s)=\frac{s^2}{s^2+\frac{s}{\tau_p}+\frac{1}{\tau_p\tau_i}}=\frac{\tau_p\tau_is^2}{\tau_p\tau_is^2+\tau_is+1} \tag{V.2-4}$$

The phase error transfer function may also be written in the canonical form in terms of undamped natural frequency and damping ratio:

$$H_e(s)=\frac{s^2}{s^2+2\varsigma\omega_ns+\omega_n^2} \tag{V.2-5}$$

where:

$$\omega_n = \frac{1}{\sqrt{\tau_p \tau_i}}$$
$$\varsigma = \frac{1}{2}\sqrt{\frac{\tau_i}{\tau_p}} \qquad \text{(V.2-6)}$$

Finally, using Equations (IV.2-30) and (IV.2-31), the phase error transfer function may be rewritten in terms of the gain peaking and 3 dB bandwidth. For a sufficiently large damping ratio (certainly satisfied by damping ratios on the order of 4 or 5, which is the case here), Equation (IV.2-30) may be approximated by:

$$\omega_{3dB} \cong 2\varsigma\omega_n \qquad \text{(V.2-7)}$$

where ω_{3dB} is the 3 dB bandwidth expressed in rad/s. Then:

$$H_e(s) = \frac{s^2}{s^2 + \omega_{3dB} s + \varepsilon\omega_{3dB}^2} \qquad \text{(V.2-8)}$$

where the quantity ε is the fractional part of the gain peaking, i.e., see Equation (IV.2-31):

$$\varepsilon \equiv H_p - 1 = \frac{1}{4\varsigma^2} \qquad \text{(V.2-9)}$$

The quantity ε is approximately related to the gain peaking in dB by:

$$H_p(dB) = 20\log_{10}\left(1 + \frac{1}{4\varsigma^2}\right) \cong 8.6859\ln\left(1 + \frac{1}{4\varsigma^2}\right) \cong 8.6859\varepsilon \qquad \text{(V.2-10)}$$

Let the input to the ODCp PLL be a frequency drift D (the units of D are fractional frequency offset per second, i.e., s^{-1}). Then the input, expressed as a phase history $u(t)$ in unit intervals (UI), is (the notation $u(t)$, and $U(s)$ for its Laplace transform, are used for the input in clause V.2 and Figure IV.2-1):

$$u(t) = \frac{1}{2} D f_0 t^2 \qquad \text{(V.2-11)}$$

where f_0 is the input client frequency (i.e., frequency of the client signal at the mapper). The Laplace transform of the input is:

$$U(s) = \frac{D f_0}{s^3} \qquad \text{(V.2-12)}$$

The Laplace transform of the phase error is obtained by multiplying the phase error transfer function by the Laplace transform of the phase input; the result is:

$$E(s) \equiv H_e(s) U(s) = \frac{\tau_p \tau_i}{\tau_p \tau_i s^2 + \tau_i s + 1} \times \frac{D f_0}{s} \qquad \text{(V.2-13)}$$

Equation (V.2-13) has the same form as the transfer function for the step response of a damped oscillator; for damping ratio greater than 1 (which is the case here) the oscillator is overdamped and there is no overshoot. In this case, the maximum response, i.e., the maximum phase error, is equal to the steady-state phase error. This is given by:

$$E_{ss} \equiv \lim_{t \to \infty} e(t) = \lim_{s \to \infty} sE(s) = D f_0 \tau_p \tau_i \quad \text{(UI)} \qquad \text{(V.2-14)}$$

The units of the steady-state phase error in Equation (V.2-14) are UI. To obtain the result in units of time, this must be divided by the client frequency f_0:

$$E_{ss} = D\tau_p\tau_i \quad \text{(s)} \tag{V.2-15}$$

This may be rewritten in terms of 3 dB bandwidth and damping ratio using Equations (V.2-6) and (V.2-7):

$$E_{ss} = D\frac{4\varsigma^2}{\omega_{3dB}^2} = \frac{D\varsigma^2}{\pi^2 f_{3dB}^2} \quad \text{(s)} \tag{V.2-16}$$

Inserting $D = 10^{-8}$/s, $\zeta = 4.6465$ (which corresponds to 0.1 dB gain peaking; see Equation (IV.2-31)), and $f_{3dB} = 300$ Hz, the steady-state phase error is:

$$E_{ss} = \frac{(10^{-8}s^{-1})(4.6465)^2}{\pi^2(300\text{Hz})^2} = 2.43\times10^{-13}\text{s} = 0.243\text{ps} \tag{V.2-17}$$

In Equation (V.2-17), the 3 dB bandwidth and gain peaking just meet the requirements of clause A.7.3 (300 Hz and 0.1 dB, respectively). In practice, the bandwidth and gain peaking will be somewhat lower. It is seen from Equation (V.2-16) that decreasing the 3 dB bandwidth and gain peaking (i.e., increasing the damping ratio) will cause the steady-state phase error to increase. For example, if the 3 dB bandwidth is 150 Hz and the gain peaking is 0.5% (i.e., approximately 0.043 dB using Equation (V.2-10), which corresponds to a damping ratio of 7.07), the steady-state phase error is:

$$E_{ss} = \frac{(10^{-8}s^{-1})(7.07)^2}{\pi^2(150\text{Hz})^2} = 2.25\times10^{-12}\text{s} \cong 2.3\text{ps} \tag{V.2-18}$$

V.3 Demapper wideband jitter generation due to gaps produced by fixed overhead in OTUk frame

The jitter and wander transfer requirements for ODCp given in clause A.7.3 and Table A.1-1 ensure that the jitter due to the mapping and demapping of client signals into and out of OPUk, possibly multiple times, will be acceptable (i.e., will satisfy the respective network limits, which are given in [ITU-T G.825] for the case of SDH clients). The ODCp jitter generation requirements given in clause A.5.1.2 and Table A.5-2 ensure that any additional jitter produced by the ODCp will be within limits. An ODCp that does not generate any additional jitter and meets the transfer requirements of clause A.7.3, namely 3 dB bandwidth not exceeding 300 Hz and gain peaking not exceeding 0.1 dB, will meet the requirements of Table A.5-2. For example, the zero-to-peak wideband jitter due to a single justification when an STM-16 is demapped from an OPU1 is approximately 0.4 UIpp assuming a 300 Hz bandwidth, 0.1 dB gain peaking, and 5 kHz high-pass jitter measurement filter for wideband jitter. The peak-to-peak jitter is therefore twice this, or approximately 0.8 UIpp. This is within the 1.0 UIpp requirement of Table A.5-2.

The additional margin in the Table A.5-2 requirements allows for some ODCp jitter generation, while keeping total jitter accumulation acceptable. One possible source of ODCp jitter generation is the jitter due to the gaps caused by the fixed overhead in the OTUk frame. This jitter is considered in this clause, and it is shown that one method of reducing this jitter to a level that is negligible is via the addition of a suitable filter following the proportional-plus-integral filter in the ODCp phase-locked loop (PLL).

NOTE – This is not the only method for reducing this jitter; other, widely-used methods employ a virtual FIFO to smooth the gaps due to fixed overhead. In some of these methods, a clock whose rate is equal to the OPUk payload rate is derived from the OTUk clock; this derived clock is input to a desynchronizer phase-locked loop (PLL) that controls the reading of client data from the demapper FIFO. The PLL that produces

the OPUk payload clock from the OTUk clock filters the jitter due to fixed overhead gaps; the desynchronizer PLL filters the jitter due to justifications.

As in clause V.2, the demapper is modelled as a PLL using the model of Figure IV.2-1; however, now an additional filter $G(s)$ is inserted between the loop filter $(1+b/s)$ and VCO (K_o/s). The form of $G(s)$ will be specified later. The transfer function, $H(s)$, for the PLL is:

$$H(s)=\frac{\frac{K_aK_o}{s}\left(1+\frac{b}{s}\right)G(s)}{1+\frac{K_aK_o}{s}\left(1+\frac{b}{s}\right)G(s)}=\frac{(K_aK_os+K_aK_ob)G(s)}{s^2+(K_aK_os+K_aK_ob)G(s)} \qquad \text{(V.3-1)}$$

where K_a is the phase detector gain, K_o is the VCO gain, and b is the integral time constant assuming a PI loop filter with transfer function $1+b/s$. Defining the proportional time constant as in Equation (V.2-3), the integral time constant $\tau_i = 1/b$, the undamped natural frequency and damping ratio as in Equation (V.2-6), the 3 dB bandwidth as in Equation (V.2-7) (in units of rad/s), and the fractional part of the gain peaking as in Equation (V.2-9), the transfer function may be rewritten:

$$H(s)=\frac{(\omega_{3dB}s+\varepsilon\omega_{3dB}^2)G(s)}{s^2+(\omega_{3dB}s+\varepsilon\omega_{3dB}^2)G(s)} \qquad \text{(V.3-2)}$$

Setting $s = j\omega$ in Equation (V.3-2) to obtain the frequency response, dividing numerator and denominator by ω_{3dB}^2 and defining the dimensionless quantity $x = \omega/\omega_{3dB} = f/f_{3dB}$ (where $\omega = 2\pi f$ and $\omega_{3dB} = 2\pi f_{3dB}$), produces:

$$H(j\omega)=\frac{(jx+\varepsilon)G(j\omega)}{-x^2+(jx+\varepsilon)G(j\omega)} \qquad \text{(V.3-3)}$$

Each row of an OTUk, ODUk, and OPUk frame has 3808 bytes of OPUk payload and 272 bytes of OPUk, ODUk, and OTUk overhead (see [ITU-T G.709]). The 272 bytes of overhead gives rise to a gap of size (8)(272) UI = 2176 UI. This gap repeats with period equal to one-fourth the OTUk frame period (because the OTUk frame has 4 rows). The result is a sawtooth phase waveform with amplitude of 2176 UI and period equal to the OTUk frame period divided by 4. The worst case is OTU1 (i.e., STM-16 mapped into ODU1), because here the frame period is largest. The remainder of this clause will focus on this case. The resulting sawtooth period is 48.971 μs /4 = 12.243 μs. The frequency of the sawtooth is 81.68 kHz.

An approximate value for the magnitude of the frequency response may be obtained by noting that a Fourier decomposition of the sawtooth consists of a fundamental frequency of 81.68 kHz and harmonics. Since f_{3dB} = 300 Hz, the quantity x is of order 81680/300 = 272 or larger. The quantity ε, which is the fractional part of the gain peaking, is of order 0.1 dB/8.6859 = 0.012 (see Equation (V.2-10)). Then $x >> \varepsilon$. In addition, the filter $G(s)$ is a low-pass filter; its magnitude is never much greater than 1 (assuming small gain peaking) and much less than 1 for frequencies above its bandwidth. Finally, note that $x^2 = (272)^2 = 73980 >> x$. Then the magnitude of the frequency response given in Equation (V.3-3) may be approximated:

$$|H(j\omega)| \cong \frac{|G(j\omega)|}{x} \qquad \text{(V.3-4)}$$

Consider first the case where the filter $G(s)$ is not present, i.e., $G(s) = 1$. Then the PLL reduces the amplitude of each frequency component of the sawtooth by a factor x. An order of magnitude estimate of the jitter may be obtained by assuming the entire energy of the sawtooth is concentrated in the lowest harmonic and the amplitude is 2176 UIpp. The resulting jitter is

2176 UIpp / 272 = 8 UIpp. A more exact value of 6.3 UI was obtained via time-domain simulation using a sawtooth input. In any case, the jitter is far in excess of the 1.0 UIpp limit of Table A.5-2.

To reduce the jitter to an acceptable level, the filter $G(s)$ may be taken to be a third-order, low-pass filter with bandwidth of approximately 0.1 times the frequency of the sawtooth, i.e.,:

$$G(s)=\left(\frac{a}{s+a}\right)^3 \tag{V.3-5}$$

with $a = 2\pi f_a = 2\pi$ (8200 Hz). Then, again making the approximation that all the energy of the phase waveform is in the lowest harmonic with frequency of 81.68 kHz, the magnitude of the frequency response is approximately:

$$\left|G(j\omega)\right|=\left(\frac{f_a}{\sqrt{f^2+f_a^2}}\right)^3 \approx (0.1)^3 = 0.001 \tag{V.3-6}$$

The order of magnitude estimate of jitter is reduced to 8×10^{-3} UIpp = 8 mUIpp. A more exact value of 6.3×10^{-3} = 6.3 mUIpp was obtained via time-domain simulation using a sawtooth input. In any case, the jitter is now well within the 1.0 UIpp limit of Table A.5-2.

Appendix VI

OTN atomic functions

(This appendix does not form an integral part of this Recommendation)

VI.1 Introduction

Figure VI.1-1 summarizes the atomic functions used for OTN timing. Table A.1-1 indicates the relationships between the ODCa, ODCb, ODCr, and ODCp and these atomic functions.

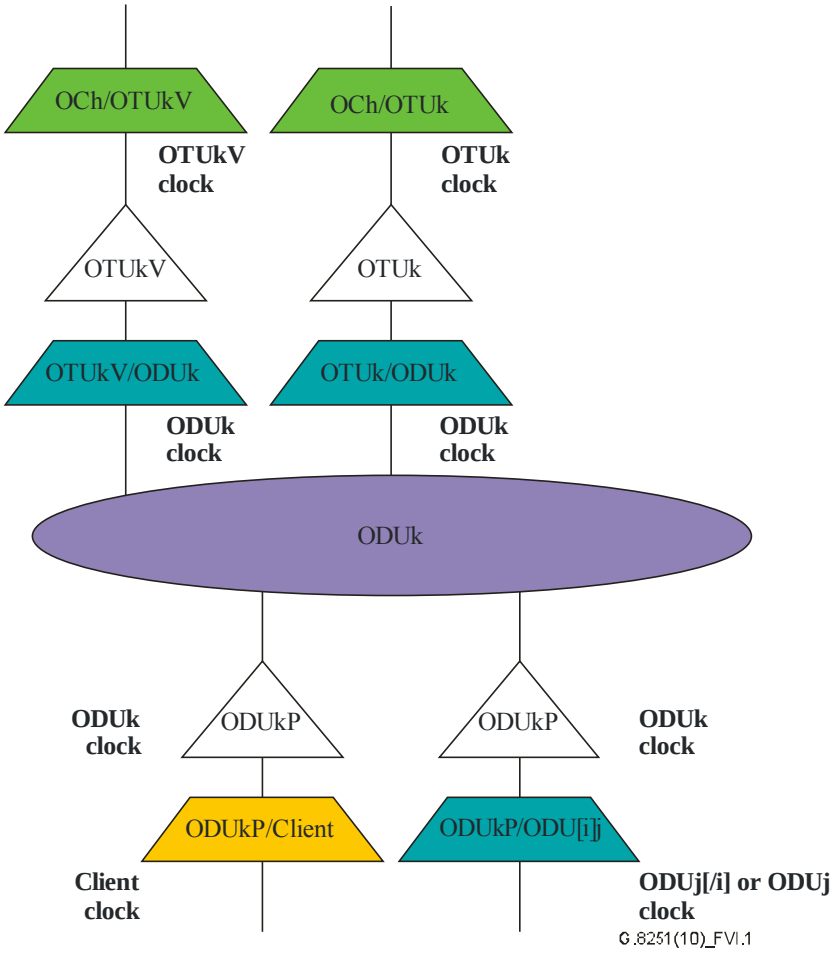


Figure VI.1-1 – Atomic functions used for OTN timing

OCh/OTUk_A_Sk: Clock recovery for the OTUk clock.

OTUk/ODUk_A_Sk: Generates ODUk clock from OTUk clock (239:255 ratio). In the case of OTUk defects including signal fail, AIS is generated with an AIS clock. The ODUk clock has to be within the limits even in case of a loss of signal.

OTUk/ODUk_A_So: Generates OTUk clock from ODUk clock (255:239 ratio). As the ODUk signal is always available no AIS clock is required. A switch between several ODUk signals with different clock phases and different frequencies shall not harm the OTUk clock.

OCh/OTUkV_A_Sk: Clock recovery for the OTUkV clock.

OTUkV/ODUk_A_Sk: Generates ODUk clock, either from the OTUkV clock with a fixed ratio (synchronous mapping) or based on the OTUkV clock and stuffing (asynchronous mapping).

OTUkV/ODUk_A_So: Generates OTUkV clock, either from the ODUk clock with a fixed ratio (synchronous mapping) or free running (asynchronous mapping) with stuffing of the ODUk into the OTUk.

ODUkP/Client_A_So: Generates ODUk clock, either free-running (asynchronous mapping) with stuffing of the client signal into the ODUk if necessary or from the client clock with a fixed ratio (synchronous mapping).

ODUkP/Client_A_Sk: Generates client clock based on the ODUk clock, and stuffing decisions if applicable.

ODUk_C: Generates free running ODUk clock for OCI.

ODUkP/ODU[i]j_A_So: Generates free-running ODUk clock. Stuffing of ODUj[/i] into ODUk.

ODUkP/ODU[i]j_A_Sk: Generates ODUj[/i] or ODUj clock based on ODUk clock and stuffing decision. AIS clock on incoming signal fail.

Appendix VII

Hypothetical reference models (HRMs) for CBRx (SDH and synchronous Ethernet client) and ODUj[/i] payload jitter and short-term wander accumulation

(This appendix does not form an integral part of this Recommendation)

VII.1 Introduction

This appendix describes the hypothetical reference models (HRM) used to obtain the ODCp (desynchronizer) jitter transfer requirements in clause A.7.3 and the ODCp jitter generation requirements in clause A.5.1.2. These requirements, together with the HRM, are consistent with the CBRx and synchronous Ethernet payload jitter network limits and jitter tolerance requirements, expressed by the requirements for SDH and synchronous Ethernet signals in [ITU-T G.825] and [ITU-T G.8261], respectively. These requirements are also consistent with the ODUj[/i] payload jitter network limits and jitter tolerance requirements, expressed by the requirements for OTUk signals in clauses 5.1 and 6.1.1 to 6.1.3. In addition, these requirements are consistent with the CBRx and synchronous Ethernet payload short-term wander MTIE and TDEV requirements. The MTIE requirements are given in Figure 8 of [ITU-T G.823] (CBRx requirement) and Figure 13 of [ITU-T G.8261] (synchronous Ethernet requirement) for Option 1, and in Figure 8 of [b-ATIS-0900101] (CBRx and synchronous Ethernet requirement) for Option 2. The TDEV requirements are given in Figure 9 of [ITU-T G.823] (CBRx requirement) and Figure 14 of [ITU-T G.8261] (synchronous Ethernet requirement) for Option 1, and in Figure 5 of [ITU-T G.824] (CBRx requirement) and Figure 15 of [ITU-T G.8261] (synchronous Ethernet requirement) for Option 2. The details of the payload jitter and short-term wander (TDEV) accumulation analyses leading to the above requirements and the HRMs are given in Appendix VIII, for the CBR2G5 and ODU1 cases (payload jitter analyses are given only for the latter).

VII.2 OTN hypothetical reference models

Appendix II describes an HRM for the transport of synchronization over OTN via SDH clients. That HRM contains a total of 100 mapping or multiplexing OTN network elements (and for each mapping or multiplexing network element there is a corresponding demapping or demultiplexing network element). The specific example of Figure II.2-1 has 10 "OTN islands", where each island[5] consists of one mapping/demapping and nine multiplexing/demultiplexing network elements and is separated from each adjacent island by an SSU. However, Appendix II is considered only with long-term wander accumulation, which depends mainly on total buffer storage of all the OTN network elements. In fact, the distribution of the mapping/demapping or multiplexing/demultiplexing elements is not important for long-term wander accumulation (this is effectively stated in clause II.2) and, in the worst case, there can be up to 100 mapping/demapping or multiplexing/demultiplexing elements between two adjacent SSUs or SECs. The total long-term wander accumulation is bounded by the total mapper or multiplexer buffer capacity of 100 network elements (wherever they are in the HRM). This consideration gave rise to the maximum buffer hysteresis requirements described in clause II.5 and specified in [ITU-T G.798].

While long-term wander accumulation can be bounded by the total buffer storage of all the network elements, jitter accumulation and short-term wander accumulation do depend more heavily on the distribution of the mapping/demapping and multiplexing/demultiplexing elements in the HRM. If there is no ODUk multiplexing, i.e., if there is only mapping and demapping of a CBRx payload,

[5] This use of the term "island" differs from other usage, where an island is taken to be a single mapper/demapper or multipexer/demultiplexer pair.

then the worst case is that of 100 mapping/demapping operations between adjacent SECs or SSUs. If there is ODUk multiplexing, then the worst case is still that of 100 mapping/demapping or multiplexing/demultiplexing operations between adjacent SECs or SSUs, but now one must also consider the relative numbers and placement of the CBRx to ODU1 mappings, ODU1 to ODU2 multiplexings, and ODU2 to ODU3 multiplexings.

Two initial HRMs were developed for the jitter and short-term wander accumulation studies described in Appendix VIII. These HRMs, denoted HRM 1 and HRM 2, respectively, are:

HRM 1: (CBR2G5→ODU1→CBR2G5) + (33 identical tandem of CBR2G5→ODU1→ODU2→ODU3→ODU2→ODU1→CBR2G5).

HRM 2: (33 CBR2G5→ODU1→ CBR2G5) + [CBR2G5→ODU1+ (33 ODU1→ODU2→ODU1) + {ODU1→ODU2 + (33 ODU2→ODU3→ODU2) + ODU2→ODU1} + ODU1→ CBR2G5].

These HRMs were chosen to:

1) bound the types of scenarios that occur in practice regarding the distribution of the higher levels of ODUk multiplexing within the OTN islands; and

2) bound the jitter and short-term wander accumulation that occurs in a network of OTN islands.

The HRMs were meant to be bounding scenarios, rather than to represent actual network configurations that will occur in practice. HRM 1 represents one extreme, where the higher levels of ODUk multiplexing (higher level ODUk islands) are distributed uniformly among the lower level ODUk islands. In HRM 1, each ODU1 island (OTN island where CBR2G5 is mapped into ODU1), except the first one, contains exactly one ODU2 island (island where ODU1 is multiplexed into ODU2), and each ODU2 island contains exactly one ODU3 island (OTN island where ODU2 is multiplexed into ODU3). HRM 2 represents the other extreme, where the higher levels of ODUk multiplexing are concentrated on one of the lower level ODUk islands. In HRM 2, all the ODU2 islands are concentrated in the final ODU1 island, and all the ODU3 islands are concentrated in the final ODU2 island.

The results in Appendix VIII show that these two HRMs bound the jitter accumulation and short-term wander accumulation, both on the CBRx payloads and ODUj[/i] payloads, that occur in a network of OTN islands.

Subsequent to the Appendix VIII analyses, additional payload jitter and short-term wander accumulation analyses were performed for STM-1 and 1 Gbit/s synchronous Ethernet clients (note that these analyses are not documented in Appendix VIII). These analyses were performed because these clients have nominal rates that are significantly less than the nominal rate of the CBR2G5 client considered in Appendix VIII. The lower rates mean that the corresponding unit intervals are larger, which can result in larger wander accumulation. In addition, the lower rates, and therefore the lower jitter high-pass measurement filter corner frequency, mean that it must be verified that the jitter accumulation is acceptable.

In adapting HRM 1 and HRM 2 to the STM-1 and 1 Gbit/s synchronous Ethernet clients, ODU1, ODU2, and ODU3 are replaced by ODU0, ODU1, and ODU2, respectively. This is because both the STM-1 and 1 Gbit/s synchronous Ethernet signals have nominal rates that are less than the OPU0 rate. However, HRM 2 would actually not occur in a real network, because the first 33 mappings/demappings would be client→ODU0→client, which implies transport via an OTU0. This cannot occur because there is no OTU0 defined. Therefore, a modification of HRM 2, designated HRM 2a, was developed:

HRM 2a: (33 client→ODU0→ODU1→ODU0→ client) + [client→ODU0→ODU1+ (33 ODU1→ODU2→ODU1) + ODU1→ODU0→ client].

HRM 2a was developed after a number of analyses had been performed using HRM 1 and HRM 2. However, comparison of results for selected HRM 2 cases with results for corresponding HRM 2a cases (i.e., for each pair of cases compared, the only difference was that one member of the pair used HRM 2 and the other member used HRM 2a; all other parameters were the same) indicated that the results were very similar.

VII.3 Impact of the insertion of OTN islands in the ITU-T G.803 synchronization reference chain

Initial short-term wander analyses performed for STM-1 and synchronous Ethernet clients, using HRM 1 and HRM 2 described above, indicated that the MTIE and TDEV accumulation were so close to the network limits that the effect of input noise should also be considered. Therefore, the ITU-T G.803 synchronization reference chain (Figure 8-5 of [ITU-T G.803]) was adapted for use with HRM 1 and HRM 2 for OTN. The ITU-T G.803 synchronization reference chain consists of a PRC, up to *K* SSUs, and up to *N* SECs (and/or EECs) between the PRC and first SSU, between successive SSUs, and following the final SSU. Clause 8.2.4 of [ITU-T G.803] indicates that for Option 1 networks, $K = 10$ and $N = 20$, with the additional constraint that the total number of SECs (and/or EECs) does not exceed 60. Clause 8.2.4 of [ITU-T G.803] indicates that these values of *K* and *N* apply only to Option 1 networks, and that for Option 2 networks the values are for further study.

In adapting the ITU-T G.803 synchronization reference chain, it was assumed that a network of OTN islands replaces at least 1 SEC/EEC in the ITU-T G.803 reference chain, and at least one SEC/EEC follows the OTN island. This means that the synchronization reference chain for determining OTN client input wander will contain 1 PRC, 10 SSUs, and 58 SECs/EECs, with the constraint that at most 20 SECs/EECs can be contiguous. In addition, the OTN client desynchronizer bandwidths are wider than SEC/EEC and SSU bandwidths, and the SEC/EEC bandwidths are wider than the Type I, II, or III SSU bandwidths. Given this, the worst case occurs when the SECs/EECs are as close to the end of the reference chain as possible, and the OTN islands follow the 58th SEC/EEC (and are then followed by 1 SEC/EEC). This means that the worst case occurs when 18 SECs/EECs follow the last SSU, 20 SECs/EECs are between the last and second-to-last SSUs, and 20 SECs/EECs are between the second-to-last and third-to-last SSUs. This worst-case reference chain is illustrated below in Figure VII.3-1.

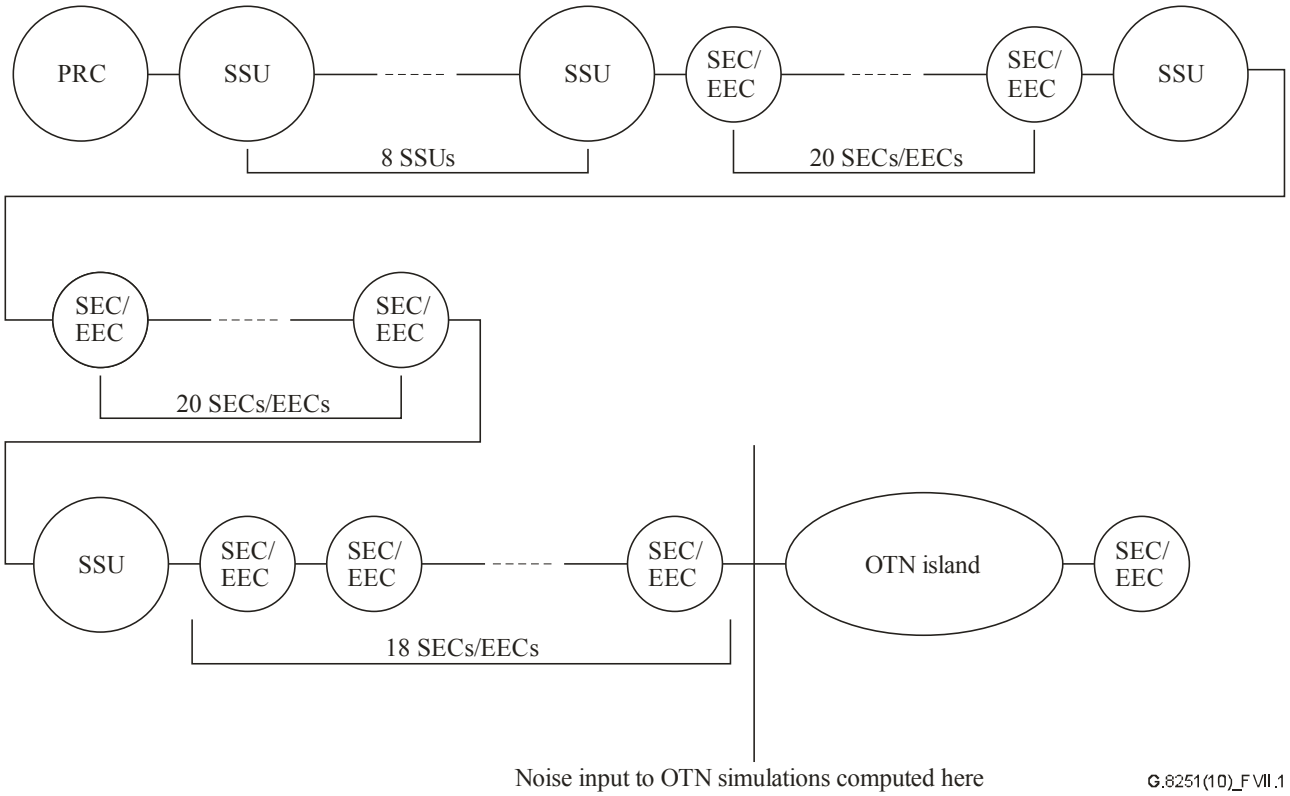


Figure VII.3-1 – Worst-case synchronization reference chain, for simulating input wander for OTN clients

In Figure VII.3-1, the "OTN island" is either HRM 1, HRM 2, or HRM 2a.[6] The synchronization reference chain that precedes the OTN island was used as the basis for wander accumulation simulations to obtain OTN client input wander for the simulation of client wander accumulation over the OTN island.

Note that the synchronization reference chain of Figure VII.3-1 is based on the number of SECs/EECs and SSUs, i.e., values of *K* and *N*, that [ITU-T G.803] indicates are applicable only to Option 1. However, [ITU-T G.803] indicates that values for Option 2 are for further study; therefore, Figure VII.3-1 was also used for Option 2 simulations.

Figure VII.3-1 was used only to determine client input wander, and not client input wideband jitter. STM-1 and 1 Gbit/s synchronous Ethernet client wideband jitter accumulation simulations assumed that input wideband jitter was the 1.5 UIpp network limit.

In the simulations, the synchronization chain of Figure VII.3-1 was used as a worst case, in the sense that a large OTN at the end of almost the full synchronization reference chain defined in [ITU-T G.803] was considered as the most conservative case. From this worst case, it is possible to ensure that other less challenging situations, such as the case of multiple smaller OTN islands distributed along the synchronization reference chain defined in [ITU-T G.803], will not lead to excessive jitter and wander accumulation.

Simulations have shown that, when using HRM 1, HRM 2, and HRM 2a for the large OTN island of Figure VII.3-1, the SDH and synchronous Ethernet client jitter and wander accumulation at the output of the OTN island are still compliant with the network limits specified in [ITU-T G.823],

[6] This use of the term "OTN island" is in the sense of Figure II.2-1, where an OTN island is a conglomerate of OTN equipment that performs mapping, (de)multiplexing and cross-connecting, and demapping.

[ITU-T G.824], and [ITU-T G.8261] (the former two are for Option 1 and Option 2 SDH clients, and the latter for synchronous Ethernet clients).

It is assumed (although it was not simulated) that the effect of the last SEC/EEC after the OTN island will not lead to the network limits specified in [ITU-T G.823], [ITU-T G.824], and [ITU-T G.8261] being exceeded, due to the additional filtering capabilities of this last clock. In addition, it is expected (although not simulated either) that if 19 SECs/EECs had been considered before the OTN island, instead of 18 SECs/EECs, the network limits specified in [ITU-T G.823], [ITU-T G.824], and [ITU-T G.8261] would still have been met (the simulation results were consistent with this conclusion).

Based on these observations, it is assumed that multiple OTN islands can be inserted between the SECs/EECs of the synchronization reference chain of [ITU-T G.803], without having to reduce the maximum number of SECs/EECs in tandem (i.e., 20) specified in [ITU-T G.803]. The insertion of multiple OTN islands should not lead to excessive jitter and wander accumulation, provided that the sum of the number of mapper/demapper pairs of all the OTN islands does not exceed the number in HRM 1, HRM 2, or HRM 2a (i.e., 100).[7] This is illustrated in Figure VII.3-2.

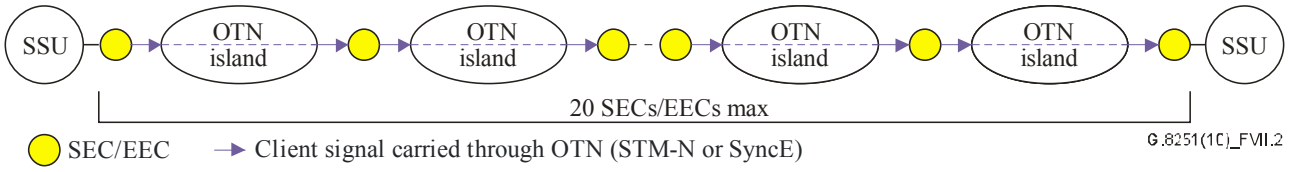


Figure VII.3-2 – Insertion of multiple OTN islands in the synchronization reference chain of [ITU-T G.803] (only the portion between 2 SSUs is shown here)

[7] Actually, the order of mapping/demapping operations in HRM 2 caused it to have 101 mapper/demapper pairs; however, the network limits were still met.

Appendix VIII

CBRx and ODUj[/i] payload jitter and short-term wander accumulation analyses

(This appendix does not form an integral part of this Recommendation)

VIII.1 Introduction

This appendix describes the details of the CBRx and ODUj[/i] payload jitter and short-term wander accumulation analyses that led to the ODCp jitter transfer requirements of clause A.7.3 and the HRM of Appendix VII. A time-domain simulation model for payload mapping jitter and wander and jitter and wander due to ODUk multiplexing was developed. The details of the simulator are described in clause VIII.2, and jitter and short-term wander simulation results are given in clause VIII.3. These analyses do not include the effects of any 3R regenerators between the mapper/multiplexer and demapper/demultiplexer. This jitter is of high frequency compared to the maximum ODCp bandwidth of 300 Hz, and is therefore easily filtered by the ODCp.

VIII.2 Simulation model

A time domain simulator was developed to evaluate phase and jitter accumulation over a network of OTN islands. The term OTN island denotes a mapping of a CBRx or ODUj[/i] client signal into an ODUkP, transport of the ODUkP with possible multiple multiplexing to ODUm (m > k) and subsequent demultiplexing, and demapping of the client from the ODUkP with a desynchronizer or demultiplexer of specified bandwidth and gain peaking. As indicated in the introduction, the effect of 3R regenerators is ignored because 3R regenerator jitter generation is of high frequency and easily filtered by the ODCp. It is assumed that this operation can be repeated a number of times; i.e., there may be multiple OTN islands. In addition, the operation is recursive in the sense that one OTN island may contain multiple, higher-level OTN islands. A schematic of the model is shown in Figure VIII.2-1[8].

The following subclauses describe the different portions of the model. These include:

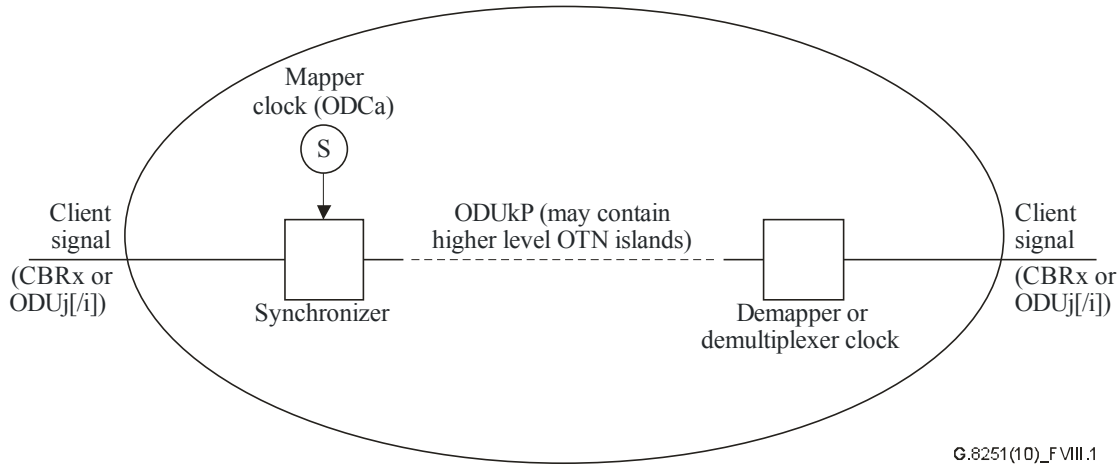
– first-order high-pass jitter measurement filter;

– second-order filter with gain peaking and 20 dB/decade roll-off (used in demapper (desynchronizer) and demultiplexer);

– +1/0/–1 byte justification scheme for CBRx mapper or +2/+1/0/–1 byte justification scheme for ODUj[/i] mapper, including the possibility of unequally-spaced justification opportunities when multiplexing ODU2 into ODU3;

– overall model (combining of mapper and demapper, and accumulation over multiple islands).

[8] Note that the use of the term "OTN island" here is different from the usage in Appendices II and VII. Here, an island is taken to be a single mapper/demapper or multiplexer/demultiplexer pair; therefore, an island here may contain one or more higher-level islands. In Appendices II and VII, an OTN island consists of the CBRx mapper/demapper and all multiplexing/demultiplexing pairs between the mapper and demapper.



NOTE – This OTN island may contain one or more higher level OTN islands.

Figure VIII.2-1 – Schematic of model for one OTN island

VIII.2.1 First-order, high-pass jitter measurement filter

This model is needed to evaluate jitter accumulated in the client signal at the egress of an OTN island. The input to the filter is the client phase accumulated up to that point; the output is the jitter. The filter is typically a first-order, high-pass filter whose 3 dB bandwidth depends on the particular client. For CBRx clients, the jitter measurement filter is specified in Table 1 of [ITU-T G.825]; for ODUj[/i] clients, the jitter measurement filter is specified in Table 5.1-1. Actually, the jitter measurement filter is a band-pass filter with both upper (low-pass) and lower (high-pass) cut-off frequencies depending on the particular rate (and increasing with increasing rate)[9]. However, the low-pass jitter measurement cut-off frequencies 20 MHz, 80 MHz, and 320 MHz for the approximately 2.5, 10, and 40 Gbit/s clients, respectively. It will turn out that these frequencies correspond to time constants that are small compared to the time step of the simulation. Therefore, it is unnecessary to model the low-pass portion of the jitter measurement filter. The high-pass portion of the jitter measurement filter depends on whether one is simulating wideband jitter or high-band jitter. The first-order, high-pass filter model covers both cases as long as the appropriate bandwidth is specified.

The transfer function for a first-order, high-pass filter, is:

$$H(s) = \frac{s}{s+a} = 1 - \frac{a}{s+a} \qquad \text{(VIII.2-1)}$$

where $a = 2\pi f_0$ and f_0 is the filter 3 dB cut-off frequency. One may obtain a discrete-time model by first obtaining a model for the low-pass filter represented by the $a/(s+a)$ term in Equation (VIII.2-1), and then subtracting the result from the input. A first-order, linear differential equation corresponding to the low-pass filter is:

$$\frac{dy}{dt} + ay(t) = au(t) \qquad \text{(VIII.2-2)}$$

[9] In addition, the low-pass portion of the jitter measurement filter has a 60 dB/decade rolloff and is maximally flat (Butterworth).

where $y(t)$ is the filter output and $u(t)$ is the filter input. Now, let T be the time step in the numerical implementation of this filter, with $t = 0$ the beginning of a time step and $t = T$ be the end of the time step. Then, the above may be converted to discrete-time form by multiplying by the integrating factor e^{at} and integrating from 0 to T. The result is:

$$e^{aT} y(T) - y(0) = \int_0^T a e^{at} u(t)\, dt \tag{VIII.2-3}$$

Finally, assume that the input $u(t)$ can be modelled as a constant equal to $u(0)$ over the time step from 0 to T. Then:

$$y(T) = e^{-aT} y(0) + (1 - e^{-aT}) u(0) \tag{VIII.2-4}$$

Equation (VIII.2-4) is the discrete-time model for the low-pass filter represented by the $a/(s + a)$ term in Equation (VIII.2-1). A discrete-time model for the high-pass filter is obtained by subtracting Equation (VIII.2-4) from $u(0)$. The result is:

$$y(T) = -e^{-aT} y(0) + e^{-aT} u(0) \tag{VIII.2-5}$$

Equation (VIII.2-5) is the discrete-time model for the high-pass jitter measurement filter.

VIII.2.2 Second-order, low-pass filter with gain peaking and 20 dB/decade roll-off

This model is needed for the CBRx demapper (desynchronizer) and the ODUj[/i] demultiplexer. The transfer function for a second-order, low-pass filter with 20 dB/decade roll-off is:

$$H(s) = \frac{2\varsigma\omega_n s + \omega_n^2}{s^2 + 2\varsigma\omega_n s + \omega_n^2} \tag{VIII.2-6}$$

where ω_n is the undamped natural frequency and ζ is the damping ratio. In the cases of interest here $\zeta > 1$, i.e., the system is overdamped. The damping ratio is related to the gain peaking by (see Equation (IV.2-31)):

$$H_p \approx 1 + \frac{1}{4\zeta^2} \tag{VIII.2-7}$$

where H_p is the gain peaking expressed as a pure gain (the gain peaking in dB is 20 $\log_{10} H_p$). The damping ratio and undamped natural frequency are related to the 3 dB bandwidth by (see Equation (IV.2-30)):

$$f_{3dB} = \frac{\omega_n}{2\pi}\left[2\zeta^2 + 1 + \sqrt{\left(2\zeta^2 + 1\right)^2 + 1}\right]^{1/2} \tag{VIII.2-8}$$

where f_{3dB} is the 3 dB bandwidth in Hz. Using Equations (VIII.2-7) and (VIII.2-8), the damping ratio and undamped natural frequency may be determined using the respective 3 dB bandwidth and gain peaking.

Equation (VIII.2-6) is equivalent to the following second-order, linear differential equation:

$$\frac{d^2 y}{dt^2} + 2\varsigma\omega_n \frac{dy}{dt} + \omega_n^2 y(t) = 2\varsigma\omega_n \frac{du}{dt} + \omega_n^2 u(t) \tag{VIII.2-9}$$

where, as in the previous clause, $y(t)$ is the filter output and $u(t)$ is the filter input. Equation (VIII.2-9) may be converted to a discrete time model using the standard state variable approach (see [b-Schultz]). Consider a second-order equation with the same left-hand side as Equation (VIII.2-9) but right-hand side equal to the input $u(t)$. For this equation, define state variables x_1 and x_2, where x_1 is equal to the output of this equation and x_2 is the derivative of the

output. The output $y(t)$ of Equation (VIII.2-9) is then easily obtained as a linear combination of x_1 and x_2 due to the linearity of Equation (VIII.2-9). The resulting equations, written in standard matrix notation, are:

$$\begin{aligned} \dot{x} &= Ax + Bu \\ y &= Cx \end{aligned} \qquad \text{(VIII.2-10)}$$

where:

$$A = \begin{bmatrix} 0 & 1 \\ -\omega_n^2 & -2\varsigma\omega_n \end{bmatrix} \qquad B = \begin{bmatrix} 0 \\ 1 \end{bmatrix} \qquad C = \begin{bmatrix} \omega_n^2 & 2\varsigma\omega_n \end{bmatrix}$$

Therefore, obtaining a discrete-time model for Equation (VIII.2-6) is equivalent to obtaining a discrete-time model for the first of Equation (VIII.2-10); the output y is easily obtained from the state **x** at a time step using the second of Equation (VIII.2-10).

The solution $\mathbf{x}(t)$ to the first of Equation (VIII.2-10) may be obtained in the same manner as the solution to the corresponding first-order equation, Equation (VIII.2-3). However, the integrating factor is now a matrix-exponential $e^{\mathbf{A}t}$. The matrix exponential is defined using the usual power series representation for e^x, and it can be shown to converge for all matrices whose entries are complex numbers (and therefore for all systems of interest here)[10]. The result, whereas before one integrates from 0 to T where T is the time step, is:

$$x(T) = e^{AT}x(0) + \int_0^T e^{A(T-t)}Bu(t)\,dt \qquad \text{(VIII.2-11)}$$

At this point, the derivation departs from the first-order analysis in that it is necessary to approximate the input $u(t)$ as a first-order expression in t in evaluating the integral in Equation (VIII.2-11), rather than a zeroth-order expression as was done in going from Equations (VIII.2-3) to (VIII.2-4). The reason for this is that the input to the desynchronizer filter is typically an "irregular" sawtooth-type function, i.e., the function, to lowest-order neglecting clock and regenerator noise, looks like a linear function of time with jumps occurring at stuffs. Since it is desired to eventually use a time step corresponding to the time between stuff opportunities or, at least, not much smaller than this (so that run times will be reasonable), a linear approximation in the integral is necessary to adequately represent the unfiltered phase (which is input to the desynchronizer filter). Note that one could, in principle, use higher-order approximations (the linear approximation is essentially a trapezoidal rule approximation).

A linear interpolation of the input $u(t)$ between 0 and T is:

$$u(t) \approx u(0) + \frac{u(T) - u(0)}{T}t \qquad \text{(VIII.2-12)}$$

Inserting Equation (VIII.2-12) into Equation (VIII.2-11) and integrating (and noting that matrix exponential functions may be integrated like ordinary exponential functions provided the order of non-commuting matrices (in this case **A** and **B**) is preserved) produces:

$$x(t) = e^{AT}x(0) + \left(e^{AT} - I\right)A^{-1}Bu(0) + \left(e^{AT} - I\right)A^{-2}B\frac{u(T) - u(0)}{T} - [u(T) - u(0)]A^{-1}B \qquad \text{(VIII.2-13)}$$

where **I** is the identity matrix (and is 2 × 2). Note that the first two terms of Equation (VIII.2-13) are what would arise from a zeroth-order approximation for the input; the final two terms arise from the linear term in the approximation.

---

[10] The proof of this is particularly simple for the case where the matrix **A** is diagonalizable.

To complete the discretization of Equation (VIII.2-10), an explicit expression for the matrix exponential $e^{\mathbf{At}}$ is needed. This may be obtained by noting that the Laplace transform of $e^{\mathbf{At}}$ is given by:

$$\mathsf{L}(e^{At}) = (sI - A)^{-1} \tag{VIII.2-14}$$

where L denotes the Laplace transform. The matrix exponential $e^{\mathbf{At}}$ may now be evaluated by calculating the inverse of the matrix $s\mathbf{I} - \mathbf{A}$ and then evaluating the inverse Laplace transform of each of the entries (it can be shown that the Laplace transform of a matrix exponential function is equal to the matrix of Laplace transforms of each of the entries). The result is:

$$e^{AT} = \begin{bmatrix} e^{-aT}\cosh bT + \frac{a}{b}e^{-aT}\sinh bT & \frac{1}{b}e^{-aT}\sinh bT \\ -\frac{a^2 - b^2}{b}e^{-aT}\sinh bT & e^{-aT}\cosh bT - \frac{a}{b}e^{-aT}\sinh bT \end{bmatrix} \tag{VIII.2-15}$$

where:

$$\begin{aligned} a &= \varsigma\omega_n \\ b &= \omega_n\sqrt{\varsigma^2 - 1} \\ a^2 - b^2 &= \omega_n^2 \end{aligned} \tag{VIII.2-16}$$

The discrete-time filter is given by Equations (VIII.2-13), (VIII.2-15), and the second of Equation (VIII.2-10). Given the state $\mathbf{x}(0)$ and input $u(0)$ at the beginning of a time step, Equations (VIII.2-13) and (VIII.2-15) are used to obtain the state $\mathbf{x}(T)$ at the end of the time step. The second of Equation (VIII.2-10) is then used to obtain the filter output $y(t)$.

VIII.2.3 Mapper/multiplexer model

A +1/0/–1 or +2/+1/0/–1 byte justification (stuffing) scheme is modelled for the mapper or multiplexer, respectively. To determine whether to do a positive justification at a justification opportunity, the buffer fill and total number of justifications up to that point are kept track of (separately for the mapper/multiplexer of each island). Let $\phi_r(t)$ be the read clock phase (in UI) at time t, $\phi_w(t)$ be the write clock phase (in UI) at time t, $B(t)$ the synchronizer buffer fill (in UI) at time t, B_0 the initial buffer fill (in UI) at time zero, $n_{stuff}(t)$ the algebraic sum of the byte justifications up to (but not including) time t, and U the number of unit intervals in one byte (i.e., 8). Then:

$$B(t) = \phi_w(t) - \phi_r(t) + B_0 + Un_{stuff}(t) \tag{VIII.2-17}$$

If $B(t)$ exceeds in the positive direction the upper mapper/multiplexer buffer threshold, a negative justification is performed[11]. In doing this, n_{stuff} is decremented by 1. Conversely, if $B(t)$ exceeds in the negative direction the lower mapper/multiplexer buffer threshold, a positive justification is performed. In doing this, n_{stuff} is incremented by 1. Note that n_{stuff} is needed to calculate the phase input to the desynchronizer (described shortly).

The write clock phase is equal to the phase output from the previous island at this level (i.e., if the current island is an ODUk island, this is the phase output from the previous ODUk island in the current chain) with any accumulated jitter from that island. The write clock phase for the first island in the current chain is equal to the client signal phase input to that island. If phase is measured with

[11] Here, the sign convention is used where the transmission of an additional byte, which occurs when $B(t)$ goes above the upper threshold, is referred to as a positive justification, and the transmission of one less byte, which occurs when $B(t)$ goes below the lower threshold, is referred to as a positive justification.

respect to the nominal client signal rate f_0 (in UI/s), which is input, and if the client is allowed to have a frequency offset y_{client} relative to this (in ppm), then the write clock phase for the first island in the current chain is:

$$\phi_{w,island\ 1}(t) = (1.0 \times 10^{-6}) U f_0 y_{client} t \quad \text{(VIII.2-18)}$$

The simulation model allows the client frequency offset to be set on input or chosen randomly from a uniform distribution between $\pm y_{client,max}$, where $y_{client,max}$ is set on input.

In calculating the read clock phase, server layer fixed overhead is neglected. In addition, in the multiplexing case the read clock refers only to the portion of the server payload available for the client in question (and not the portion used for other clients multiplexed with this one). Then, the client and server effective nominal rates are the same. However, the server clock (read clock) is allowed to have a frequency offset y_{clock} relative to its nominal rate. Then, the read clock phase is:

$$\phi_{read}(t) = (1.0 \times 10^{-6})\, f_0 y_{clock} t \quad \text{(VIII.2-19)}$$

The unfiltered phase input to the desynchronizer is equal to the read clock phase, plus the phase due to any multiplexing/demultiplexing of the server into higher level signals, plus the phase due to byte justifications:

$$\phi_{unfilt}(t) = \phi_{read}(t) - U n_{stuff}(t) + \phi_{mux/demux}(t) \quad \text{(VIII.2-20)}$$

Note that the term $Un_{stuff}(t)$, which accounts for the justifications, enters in Equations (VIII.2-17) and (VIII.2-20) with opposite signs. This is because the effect of a positive justification is one extra byte on the output and one less byte in the buffer, and vice versa for a negative justification.

The unfiltered phase given by Equation (VIII.2-20) is input to the desynchronizer model. This is a second order filter with gain peaking, as described in the previous clause. The time step chosen for this model will be discussed shortly.

To obtain the phase due to any multiplexing/demultiplexing of the server into higher level signals, $\phi_{mux/demux}$, consider first the simple case of CBR2G5 mapped into ODU1, which is then multiplexed (mapped) into ODU2, which is then multiplexed into ODU3. At the CBR2G5 to ODU1 mapper, the stuff decisions are based on the difference between the CBR2G5 clock and mapper clock. Therefore, these stuff decisions are independent of any jitter due to the ODU1 to ODU2 or ODU2 to ODU3 mappings. At the ODU1 to CBR2G5 demapper, the recovered ODU1 clock includes any jitter due to the ODU1 to ODU2 and ODU2 to ODU3 mappings; this phase is added to the phase due to the stuff decisions that were made at the CBR2G5 to ODU1 mapper, and the sum is filtered by the CBR2G5 desynchronizer. Next, looking at the recovered ODU1 clock at the ODU1 to CBR2G5 demapper, it can be argued analogously that this has jitter due to the ODU1 to ODU2 stuffing process at the ODU1 to ODU2 mapper, plus any ODU2 jitter due to its being mapped into ODU3. Both processes are filtered by the ODU2 to ODU1 desynchronizer (demultiplexer). Finally, the ODU2 recovered clock at the ODU2 to ODU1 demapper has jitter due to the ODU2 to ODU3 stuffing process; these stuffs are filtered by the ODU3 to ODU2 desynchronizer.

Therefore, each level of multiplexing may be treated independently of the levels below it (e.g., ODU1 multiplexing into ODU2 is independent of CBR2G5 into ODU1 multiplexing). The simulator must represent the order of the multiplexing operations, i.e., the layout of the islands (this is easy to do using the C language, for example). In any island, the stuff decisions are made based on the phase difference between the client and mapper clocks. Phase is accumulated within the island in going from the mapper to demapper if there are any higher levels of mapping/demapping. This phase is added to the phase due to the stuffs at the demapper, and the total is filtered by the desynchronizer. The whole process is implemented at each level.

Since the simulation is implemented in discrete time, it is desirable for the times of stuff opportunities to occur at integral numbers of time steps. However, achieving this is complicated by the fact that the times between stuff opportunities for the different levels of mapping are not integral multiples of each other. This is because the OTU1/ODU1/OPU1 frame time of 48.971 µs (see [ITU-T G.709]) is slightly more than 4 times the OTU2/ODU2/OPU2 frame time of 12.191 µs, which is slightly more than 4 times the OTU3/ODU3/OPU3 frame time of 3.035 µs. These frame times are not in exact ratios of 4 because, when multiplexing 4 ODUks into ODUm (m = k+1), each ODUk has its OPU and ODU overhead and, in addition, the ODUm has its OPU and ODU overhead. But, the main interest here is the effect of waiting-time jitter and short-term wander, i.e., the variable stuffs due to the stuff decisions at the mappers/multiplexers. The effect of the fixed overhead is of lesser interest; this overhead gives rise to high-frequency phase variation that is easily filtered by the desynchronizers. The mapping processes at all levels can be normalized to a common time base based on the OTU1/ODU1/OPU1 frame time by neglecting the ODU and OPU overhead (except for the actual stuffs). If this is done, it is then only necessary to adjust the maximum positive and negative frequency offsets (i.e., the allowable range of frequency offsets) for the ODU1, ODU2, and ODU3 mapper clocks such that the ranges of stuff ratios for mapping CBRx into ODU1, ODU1 into ODU2, and ODU2 into ODU3 come out correctly. These calculations may be done using the relations in Appendix I of [ITU-T G.709] (see Equation (I-3) of [ITU-T G.709]).

With the above approximation, the "effective" ODU2 frame time in the simulator becomes one-fourth the ODU1 frame time. An ODU1 multiplexed into an ODU2 gets a stuff opportunity every four ODU2 frames, and the time between stuff opportunities for this process is equal to that for the mapping of CBR2G5 into ODU1 (namely, the ODU1 frame time, or 48.971 µs). Similarly, the "effective" ODU3 frame time is one-fourth the "effective" ODU2 frame time. An ODU2 multiplexed into ODU3 gets four stuff opportunities every 16 ODU3 frames. Therefore, the basic time unit in the simulator must be chosen as the "effective" ODU3 frame time, which is 1/16 the ODU1 frame time, or (48.971)/(16) µs = 3.06069 µs. The time step of the simulation can be no larger than this, but may need to be smaller if any of the filters (desynchronizer or jitter measurement filters) have time constants that are shorter. If the time step needs to be smaller than the "effective" ODU3 frame time, it is taken to be an integral sub-multiple of this frame time. Specifically, the simulation time step is chosen to be the largest submultiple of the "effective" ODU3 frame time that is no more than 0.1 times the smallest filter time constant. Stuffs for mapping CBR2G5 into ODU1 and ODU1 into ODU2 are allowed every 16 of the basic ("effective") ODU3 frame times. Stuffs for mapping ODU2 into ODU3 are allowed every four out of 16 of these basic times.

In multiplexing ODU2 into ODU3, the stuff opportunities need not be equally-spaced. The mapping is described in detail in [ITU-T G.709]. When an ODU2 is multiplexed into an ODU3, the ODU2 gets four of every 16 stuff opportunities in 16 successive ODU3 frames. The other 12 stuff opportunities go to the other ODU1s and/or ODU2s being multiplexed. However, the specific four frames that a particular ODU2 gets may not be equally spaced, and most likely will not be if ODU1 to ODU3 multiplexing is allowed. This is because the ODU1 client only requires one stuff opportunity out of every 16 ODU3 frames. The ODU1 and ODU2 client connections will not necessarily be set up at the same time; therefore, there is no guarantee that, when an ODU2 connection is desired (and the bandwidth is available) that the four ODU3 frames that have stuff opportunities will be equally spaced. It is essential that the bandwidth be usable in cases where the stuff opportunities are not equally spaced. Therefore, the possibility of unequally-spaced stuff opportunities is modelled by associating with every island (mapper) an array of length 16. Each array element indicates whether a stuff is or is not allowed on that particular effective ODU3 frame out of each set of 16. For each island, the simulator initializes at the start of the run the particular (effective) ODU3 frames that correspond to stuff opportunities. The initialization may be done in one of three ways:

1) randomly chosen;

2) concentrated; and

3) equally-spaced.

If the stuff opportunities are randomly chosen, then each island will likely have stuff opportunities on different ODU3 frames (even for CBR2G5 into ODU1 or ODU1 into ODU2 mappings, for which there is one stuff opportunity every 16 "effective" ODU3 frames; the particular one will be different for each island).

VIII.2.4 Overall model

The models described in clauses VIII.2.1-VIII.2.3 were combined into an overall model for jitter and wander accumulation in a network of OTN islands. The client signal input to the first island is assumed to be unjittered, but may have a frequency offset from nominal (which may be chosen randomly within a range). The phase output, filtered by the demapper/demultiplexer, from each island is the input phase to the next island at the same level (the write clock for that island). The output of each island can also be separately input to a high-pass jitter measurement filter to evaluate jitter for that island. Both peak-to-peak and RMS (actually, standard deviation) of phase and jitter are calculated for the outputs of each island. These calculations are performed after an initial time interval has elapsed (specified on input) so that any initial transient may decay (this time may be determined from knowledge of the filter time constants and verified with an initial test run where sample waveforms are examined). In addition, it is possible to save all the phase (filtered and unfiltered) and jitter waveforms output from all the islands into files, though this is not normally done for runs with a large number of islands and appreciable simulation time as the disk storage requirements can be considerable.

The peak-to-peak phase and jitter are evaluated by saving at each time step, after the initialization period, the maximum and minimum phase and jitter samples up to that point. The standard deviation (RMS) is evaluated as the square root of the sample standard variance, which is given by (it is assumed in this calculation that the number of time steps is sufficiently large that the difference between the number of samples and the number of samples minus one (the number of degrees of freedom) can be neglected):

$$\sigma_\phi^2 = \frac{1}{n-n_0}\sum_{j=n_0+1}^{n}\phi^2(jT) - \left(\frac{1}{n-n_0}\sum_{j=n_0+1}^{n}\phi(jT)\right)^2 \qquad \text{(VIII.2-21)}$$

In Equation (VIII.2-21), $\phi(jT)$ is the phase or jitter at the *jth* time step, σ_ϕ^2 is the sample variance, n is the number of time steps, and n_0 is the number of time steps in the initialization period.

The simulation model requires a random number generator. For the simulation cases performed here, a random number generator based on a combination of a linear congruential and a shift register algorithm was used. The period of this generator is of order $(2^{32} - 1)(2^{48} - 1) = 1.2 \times 10^{24}$. In all cases, multiple independent replications were run by saving the state of the random number generator in a file and using this state to initialize the generator for the subsequent replication. The number of random samples, i.e., the number of invocations of the generator, was counted (using two 32-bit integer variables) so it could always be checked that the supply of random samples was not exhausted.

The simulation model was implemented in a C program.

VIII.3 Jitter and short-term wander simulation results

Simulations were run for each of the two HRMs documented in Appendix VII. It was indicated in the previous clause that the justification opportunities for the multiplexing of ODU2 into ODU3 need not be equally spaced. Three types of cases were considered:

- Stuff opportunities chosen randomly in each ODU2→ODU3 mapping.

- Stuff opportunities concentrated together for each ODU2→ODU3 mapping (i.e., in a set of 16 ODU3 frames, an ODU2 gets four stuff opportunities in a row, followed by 12 frames with no stuff opportunity).
- Stuff opportunities equally spaced (one every four ODU3 frames).

The first case is the most realistic, the second the most conservative, and the third the least conservative.

Next, a worst-case condition when using a positive/zero/negative justification scheme, for purposes of jitter and wander accumulation, can occur when the frequency offset between the client and mapper clocks is small but non-zero, and sufficiently small that the resulting stuff rate is small compared to the desynchronizer bandwidth. Therefore, the following two types of cases were considered:

- Client and mapper clocks free-running with frequency offsets within their required frequency tolerances (i.e., ±20 ppm, but adjusted to account for the fact that ODUk fixed overhead is neglected).
- Client and mapper clocks free-running with frequency offsets of ±0.05 ppm.

In the latter case, the maximum frequency offset between client and server is 0.1 ppm. For mapping CBR2G5 into ODU1 (and therefore approximately for ODU1 into ODU2) this gives rise to a maximum mean stuff rate of 31 Hz, which is well within the 300 Hz desynchronizer bandwidth. To show this, let y be the frequency offset between the client and OPU1 clocks (for a particular mapper), and f_0 be the nominal OPU1 rate. Then the rate at which excess phase (positive or negative) is accumulated is yf_0. Since the stuff unit is 1 byte, or 8 UI (positive or negative), the mean time between stuffs is approximately $8/yf_0$, and the mean rate of stuffs is $yf_0/8$. If the maximum frequency offset magnitude between client and OPU1 is $y_{\max}$ = 0.1 ppm, the maximum mean stuff rate is given by:

$$f_{stuff,\max} = (0.1\times10^{-6})(2.488320\times10^{9})/8 = 31\,\text{Hz} \qquad \text{(VIII.3-1)}$$

For mapping ODU2 into ODU3, in the best case the rate would be 4 times this, or 124 Hz, which is still within the 300 Hz desynchronizer bandwidth.

Then, considering that there are two HRMs, three sets of assumptions on stuff opportunities, and two sets of assumptions on clock accuracies, a total of 12 cases can be considered. These are summarized in Table VIII.3-1 (designated Cases 1-12).

Also indicated in Table VIII.3-1 is the number of independent replications of the simulation run for each case. If 300 independent replications are run, a good level of statistical confidence for the 95th percentile of a distribution can be obtained (i.e., if 300 independent samples of a population are placed in ascending order, a 99% confidence interval for the 95th percentile of the distribution for this population is given by the interval between the 275th and 294th samples (the 7th and 26th largest samples). This result follows from the fact that if the samples are selected independently and all have the same distribution, then reasonably tight confidence intervals for a percentile of the distribution are obtained from a binomial distribution (see [b-Papoulis] for details). However, due to constraints on computational resources, only Cases 9-12 had 300 replications completed. For the other cases, it is still possible to obtain 99% confidence intervals for the 95th percentile of the respective distribution; however, the intervals will be larger than those with 300 replications because the number of replications is smaller (see Table VIII.3-3).

Table VIII.3-1 – Summary of simulation cases

Simulation case	Hypothetical reference model	Stuff opportunities	Clock offsets	Number of independent replications of simulation
1	HRM 1	Randomly selected	Random within free-run accuracies	271
2	HRM 2	Randomly selected	Random within free-run accuracies	271
3	HRM 1	Randomly selected	Random within ±0.05 ppm	271
4	HRM 2	Randomly selected	Random within ±0.05 ppm	271
5	HRM 1	Concentrated	Random within free-run accuracies	191
6	HRM 2	Concentrated	Random within free-run accuracies	191
7	HRM 1	Concentrated	Random within ±0.05 ppm	255
8	HRM 2	Concentrated	Random within ±0.05 ppm	255
9	HRM 1	Equally spaced	Random within free-run accuracies	300
10	HRM 2	Equally spaced	Random within free-run accuracies	300
11	HRM 1	Equally spaced	Random within ±0.05 ppm	300
12	HRM 2	Equally spaced	Random within ±0.05 ppm	300

Table VIII.3-2 shows remaining parameters for the simulation cases. These are common to all the cases. Note that the initialization time indicated in Table VIII.3-2 is the time needed for initial transients to decay before beginning any peak-to-peak jitter or TDEV calculation.

Table VIII.3-2 – Parameters common to all simulation cases

Parameter	Value
Stuffing mechanism	+/–/0 byte stuffing
Desynchronizer/demultiplexer order	2nd order, with 20 dB/decade roll-off
Desynchronizer/demultiplexer 3 dB bandwidth	300 Hz
Desynchronizer/demultiplexer gain peaking	0.1 dB
Desynchronizer/demultiplexer damping ratio	4.6465 (corresponds to 0.1 dB gain peaking)
Mapper buffer initial conditions	Random
Time step	3.0607×10^{-6} s
Simulation time	31 s
Initialization time	1.0 s

VIII.3.1 Results for wideband jitter accumulation

Results are given in this clause for peak-to-peak wideband jitter accumulation for the CBR2G5 client and, for Model 2, the ODU1 client. The ODU1 jitter accumulation results in Model 2 are for

the final ODU1 island; here, the ODU1 is transported over 33 ODU2 islands followed by a single ODU2 island containing 33 ODU3 islands.

A 99% confidence interval for the 95th percentile is obtained for each case by ordering the peak-to-peak jitter results from smallest to largest. A 99% confidence interval for the 95th percentile of the distribution then falls between the samples whose indices (after ordering) are given in Table VIII.3-3. As indicated earlier, this result follows from the fact that the confidence intervals may be obtained from a binomial distribution; see [b-Papoulis] for more details (the same result is applied to obtaining confidence intervals for MTIE in clause II.5 of [ITU-T G.810]).

Table VIII.3-3 – Extent of 99% confidence interval for 95th percentile of a distribution, for various numbers of samples

Number of samples	Index of sample for lower end of 99% confidence interval	Index of sample for lower end of 99% confidence interval
300	275	294
271	248	266
255	234	251
191	174	189
NOTE – Samples are assumed to have been ordered from smallest to largest.		

VIII.3.1.1 CBR2G5 client wideband jitter accumulation results

Results for CBR2G5 client wideband jitter accumulation for Cases 1-12 are given in Figures VIII.3-1 through VIII.3-12, respectively. The accumulation is shown over 34 ODU1 islands (this is the number of ODU1 islands for each case; the remaining islands are ODU2 and ODU3 islands).

The first thing to note is that the peak-to-peak jitter accumulation is within the 1.5 UIpp network limit of [ITU-T G.825] in all cases. The worst case appears to be Case 7, where the largest upper extent of the peak-to-peak jitter (largest upper extent of the 99% confidence interval for the 95th percentile) is approximately 1.08 UIpp. Some general trends in the results are now discussed.

On examining first the Model 1 cases (Figures VIII.3-1, VIII.3-3, VIII.3-5, VIII.3-7, VIII.3-9, and VIII.3-11), note that the peak-to-peak jitter increases over the first few ODU1 islands, and then remains at a generally constant level for the remaining islands. There is some fluctuation around the generally constant level, but the amplitude of the fluctuation is less than the initial increase. Next, comparing the loose clock tolerance cases (Cases 1, 5, and 9, in Figures VIII.3-1, VIII.3-5 and VIII.3-9, respectively) with the tight clock tolerance cases (Cases 3, 7, and 11, in Figures VIII.3-3, VIII.3-7 and VIII.3-11, respectively), note that the peak-to-peak jitter is larger in the tight clock tolerance cases, and the amount of fluctuation is less. In addition, the increase to the roughly constant level occurs faster in the tight clock tolerance cases, in approximately 3 islands versus 4-10 islands in the loose clock tolerance cases (in these latter cases the fact that the increase is more gradual makes it more subjective in defining when the constant level is reached).

The jitter is larger in the tight clock tolerance cases because in these cases the stuffs are occurring at low enough frequency that they are filtered independently by the desynchronizer. In these cases, the maximum jitter occurs when jitter peaks at successive levels line up. This maximum value is approximately 1.22 UIpp, which may be obtained as follows. First, the zero-to-peak jitter due to a justification of 8 UI for the CBR2G5 to ODU1 mapping, filtered by a 300 Hz low-pass filter desynchronizer and a 5 kHz high-pass jitter measurement filter, is evaluated. Next, the zero-to-peak jitter due to a justification of 8 UI for the ODU1 to ODU2 mapping, filtered by two 300 Hz low-pass desynchronizers (ODU2 to ODU1 and ODU1 to CBR2G5) and a 5 kHz high-pass jitter measurement filter is evaluated. This result is added to the previous result, under the assumption that in the worst case the two peaks line up. The result for ODU2 to ODU3 mapping is obtained,

using three desynchronizer filters and recognizing that the UI here is approximately one-fourth that of the CBR2G5 UI. Finally, the entire result is multiplied by 2 to obtain peak-to-peak jitter from zero-to-peak jitter.

It appears that two islands are required in order to have a reasonable probability of obtaining this jitter (the peak-to-peak jitter is around 0.6 UI after 2 islands in Figures VIII.3-3, VIII.3-7 and VIII.3-11). A third island is required to get a jitter peak in the opposite direction. Even so, the theoretical maximum of 1.22 UIpp is not obtained; apparently there is always some overlap of the peaks in the positive and negative directions. In the loose clock tolerance cases (Figures VIII.3-1, VIII.3-5 and VIII.3-9), the maximum peak-to-peak jitter level is lower and there is more fluctuation. This is because, for these cases, the stuffs can occur at higher frequency and, when this frequency is of the same order as the desynchronizer bandwidth or larger, they interfere with each other.

Next, consider the effect of whether the ODU2 stuff opportunities are concentrated, random, or evenly spaced. In the tight clock tolerance cases (Figures VIII.3-3, VIII.3-7 and VIII.3-11), the maximum peak-to-peak jitter is similar in all three cases (1.08 UIpp for the concentrated stuff opportunities versus 1.06 UIpp for the other two cases). This is because the stuffs tend to be widely separated in these cases (i.e., by more than 16 ODU3 frames). In the loose clock tolerance cases there is slightly more dependence; the maximum peak-to-peak jitter in Case 9 (equally-spaced stuff opportunities, Figure VIII.3-9) is approximately 0.77 UIpp, versus 0.81 UIpp for the other two cases (Figures VIII.3-1 and VIII.3-5). In any case, the impact of the stuff opportunity spacing is small in all cases because it affects only the ODU2 to ODU3 mapping, for which the unit interval is only one-fourth as large as that for CBR2G5 to ODU1 or ODU1 to ODU2.

Next, consider the Model 2 cases (Figures VIII.3-2, VIII.3-4, VIII.3-6, VIII.3-8, VIII.3-10 and VIII.3-12), and note that for the initial ODU1 islands that do not contain any ODU2 or ODU3 islands (islands 1-33), the peak-to-peak jitter increases over the first few ODU1 islands and then stays roughly at this level, fluctuating. The behaviour is roughly analogous to the Model 1 cases, except that the steady-state level is less than in the Model 1 cases because it reflects only one level of mapping. There is also less fluctuation in the Model 2 cases compared to the corresponding Model 1 cases (i.e., comparing Cases 1 and 2, 3 and 4, 5 and 6, 7 and 8, 9 and 10, and 11 and 12). Then, the Model 2 cases all show an increase in jitter at the 34th ODU1 island. This is due to the higher levels of mapping in this island (33 ODU1 to ODU2 mapping/demappings, followed by an ODU2 island with 33 ODU3 islands). This increase in jitter in the final island brings the peak-to-peak jitter to approximately the level in the corresponding Model 1 case (it brings it to a slightly lower level in the tight clock tolerance cases and slightly higher level in the loose clock tolerance cases).

The results here indicate that, for consideration of CBR2G5 wideband jitter accumulation:

- the [ITU-T G.825] network limit of 1.5 UIpp is met;
- the peak-to-peak jitter accumulation increases relatively quickly to a maximum value and remains at this value; the ordering of the types of islands (i.e., ODU1, ODU2, and ODU3) is of secondary importance;
- there is little dependence on the locations of the stuff opportunities;
- the jitter accumulation is higher for smaller clock tolerances.

VIII.3.1.2 ODU1 client wideband jitter accumulation results

Results for ODU1 client wideband jitter accumulation for Cases 2, 4, 6, 8, 10, and 12 are given in Figures VIII.3-13 through VIII.3-18, respectively. The accumulation is shown over 33 ODU2 islands, which are numbered from 35 through 67 (this is the number of ODU2 islands in the final ODU1 island for each case; note that the final ODU2 island contains 33 ODU3 islands).

The peak-to-peak jitter accumulation is within the 1.5 UIpp network limit of 5.1 in all cases. The maximum peak-to-peak jitter is largest in the tight clock tolerance cases (Figures VIII.3-14, VIII.3-16, and VIII.3-18), where it reaches 0.84 UIpp.

The results are qualitatively similar to the results for CBR2G5 clients. The impact of the location of the stuff opportunities is small. The peak-to-peak jitter increases over the first few islands to a roughly constant level, about which it fluctuates for the remaining islands. The increase is faster and the fluctuations smaller for the tight clock tolerance cases compared to the loose clock tolerance cases. The overall jitter accumulation is larger for the tight clock tolerance cases. Finally, there is an increase in jitter in the final ODU2 island due to the ODU3 islands in this ODU2 island (the previous ODU2 islands do not contain any higher levels of multiplexing).

VIII.3.1.3 STM-16 client short-term wander (TDEV) accumulation results

Results are given in this clause for CBR2G5 client short-term wander accumulation over all the islands. The results are presented in the form of TDEV for the CBR2G5 client emerging from the final ODU1 island. TDEV is displayed for integration times ranging from 3.06 μs (the simulation time step) to approximately 10 s (one-third the total simulated time of 30 s following the 1 s initialization time; note that TDEV involves a second difference calculation, and therefore can be obtained for integration times up to one-third the extent of the data). Note that it is mainly integration times of 0.05 s or larger that are of interest, because TDEV characterizes wander.

For each value of integration time the square root of mean TVAR (mean taken over all the replications) and square root of standard deviation of TVAR (i.e., fourth root of variance of TVAR, taken over all the replications) is obtained. The former is a point estimate of the expected value of TDEV. The latter is an approximation to the standard deviation of TDEV. The 95th percentile of TVAR is approximated as the value 2 standard deviations from the mean TVAR, and the 95th percentile of TDEV is approximated as the square-root of this.

CBR2G5 TDEV results for Cases 1-12 are given in Figures VIII.3-19 to VIII.3-30, respectively. First, note that TDEV is within the 10 ns limit for SDH Option 2 and the 12 ns limit for SDH Option 1 (for the integration times less than 10 s, which are the ones of interest here; see [ITU-T G.813]). The maximum TDEV is approximately 1 ns in the loose clock tolerance cases, which occurs for integration time of approximately 0.01 s. The maximum TDEV is approximately 3 ns in the tight clock tolerance cases, which occurs for integration time of approximately 0.3 s. TDEV is larger in the tight clock tolerance cases for longer integration times, but larger in the loose clock tolerance cases for shorter integration times. This is most likely due to the fact that the phase variation in the loose clock tolerance cases has higher frequency.

VIII.3.1.4 Conclusions

The results above indicate that:

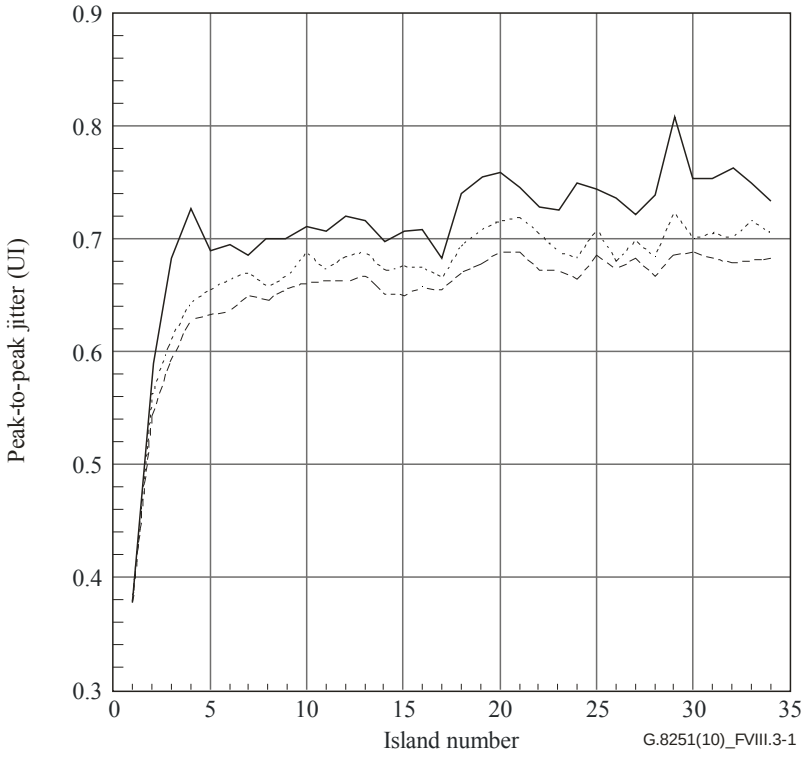
- the [ITU-T G.825] network limit of 1.5 UIpp is met for CBR2G5 clients;
- the network limit in this Recommendation of 1.5 UIpp is met for ODU1 clients;
- the maximum peak-to-peak jitter accumulation increases relatively quickly (over the initial islands) to a maximum value; the ordering of the island types (ODU1, ODU2, ODU3) is of secondary importance;
- there is little dependence on the locations of the stuff opportunities;
- the jitter accumulation is higher for smaller clock tolerances;
- the ITU-T G.813 wander TDEV limits of 10 ns for SDH Option 2 and 12 ns for SDH Option 1 is met for CBR2G5 clients.

The third bullet item is significant; it means that as long as the number of islands exceeds a sufficient number, it does not matter how many there are or what their order is, because the jitter accumulation saturates. In fact, the jitter accumulation saturates for all the CBR2G5 and ODU1

client cases here. This means that there is no need to consider more islands for the ODU1 multiplexing cases (the longest ODU1 client chain was 33 islands), because the jitter has already saturated.

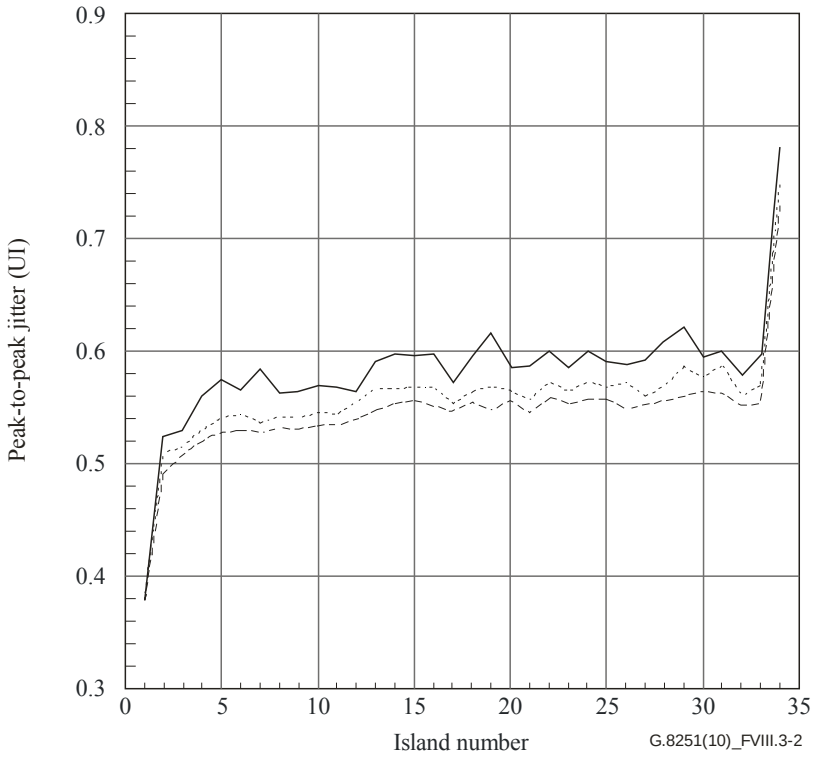
While jitter on ODU2 clients was not considered, this is expected to be similar to the mapping of STM-64 into ODU2. This is because the maximum justification rate is approximately the same for both cases. Jitter for such cases will be smaller than CBR2G5 into ODU1 mapping jitter due to the wider bandwidth jitter measurement high-pass filter.

The above simulation cases do not consider high-band jitter. This is because the high-band jitter measurement high-pass filter bandwidth exceeds the wideband high-pass filter bandwidth by a factor of approximately 200, while the high-band jitter network limit is less than the wideband jitter network limit by a factor of 10. The result is that the high-band jitter accumulation will be well below the network limit – by a factor of 20 or more (this result may be obtained by considering the jitter due to an isolated 8 UI justification).



NOTE – ODU1 islands numbered from 1 to 34.
300 Hz desynchronizer at all levels (with 0.1 dB gain peaking).
5 kHz jitter measurement filter.
Other assumptions in Tables VIII.3-1 and VIII.3-2.

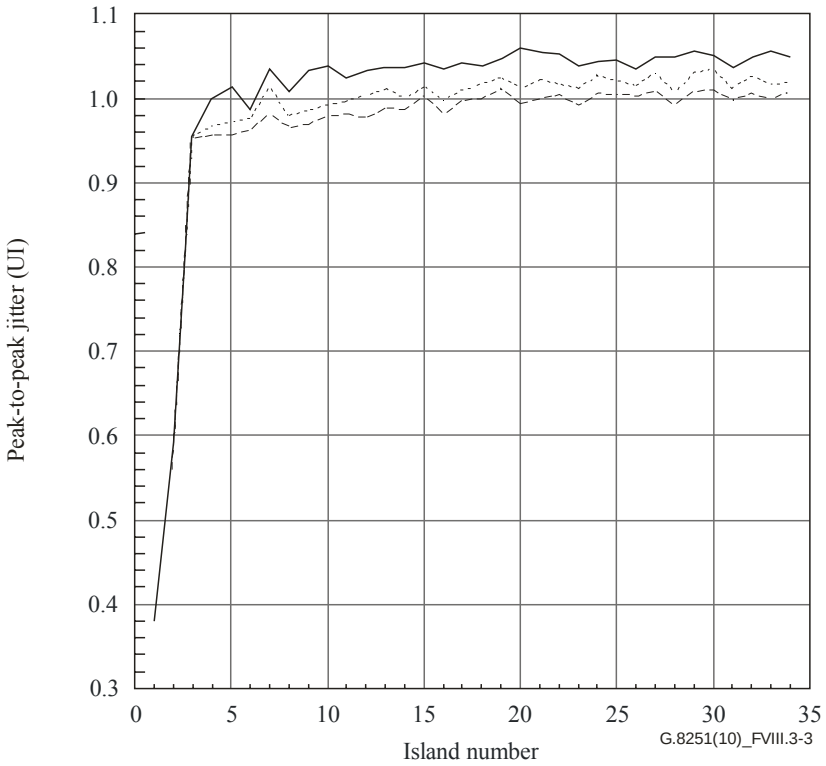
Figure VIII.3-1 – CBR2G5 client peak-to-peak wideband jitter results for Case 1 (Model 1)



—— 95th percentile, upper end of 99% confidence interval
····· 95th percentile, point estimate
– – – 95th percentile, lower end of 99% confidence interval

NOTE – ODU1 islands numbered from 1 to 34.
300 Hz desynchronizer at all levels (with 0.1 dB gain peaking).
5 kHz jitter measurement filter.
Other assumptions in Tables VIII.3-1 and VIII.3-2.

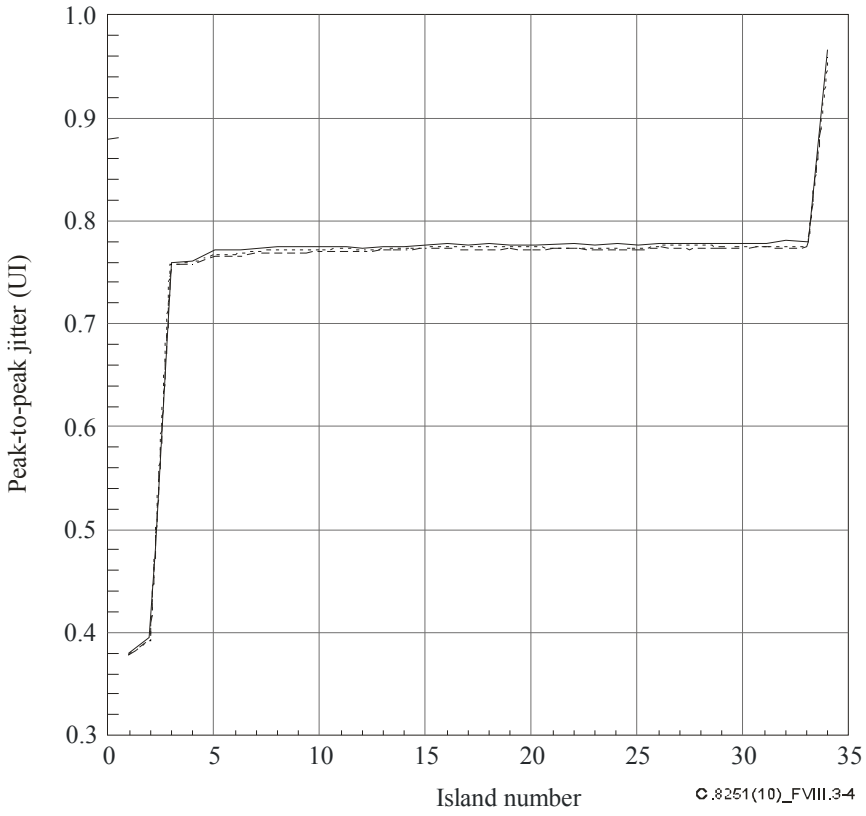
Figure VIII.3-2 – CBR2G5 client peak-to-peak wideband jitter results for Case 2 (Model 2)



—— 95th percentile, upper end of 99% confidence interval
····· 95th percentile, point estimate
– – – 95th percentile, lower end of 99% confidence interval

NOTE – ODU1 islands numbered from 1 to 34.
300 Hz desynchronizer at all levels (with 0.1 dB gain peaking).
5 kHz jitter measurement filter.
Other assumptions in Tables VIII.3-1 and VIII.3-2.

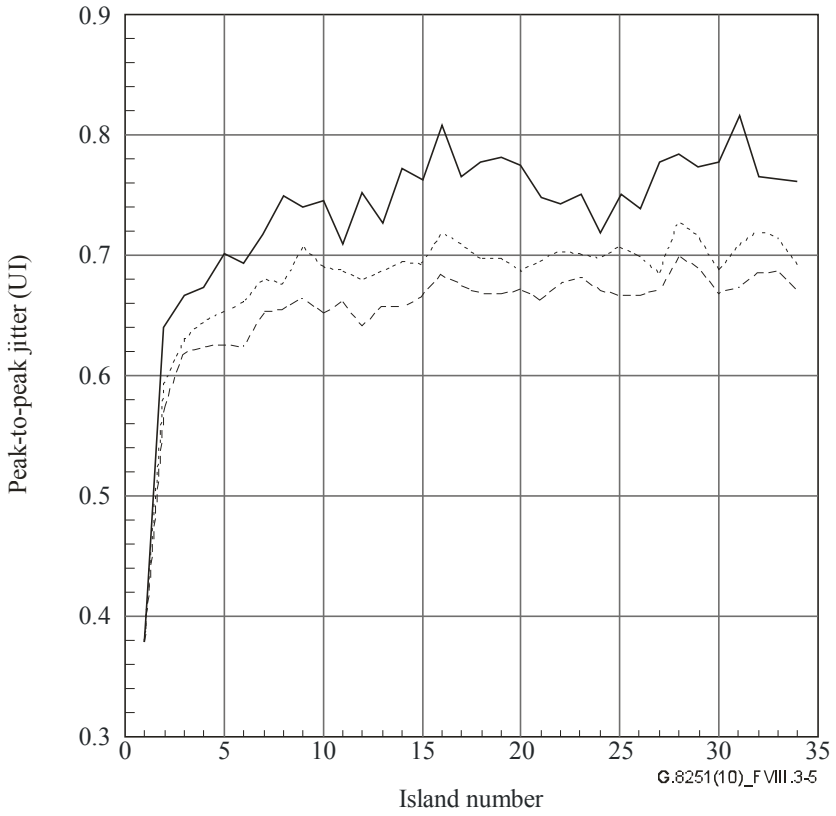
Figure VIII.3-3 – CBR2G5 client peak-to-peak wideband jitter results for Case 3 (Model 1)



—— 95th percentile, upper end of 99% confidence interval
----- 95th percentile, point estimate
– – – 95th percentile, lower end of 99% confidence interval

NOTE – ODU1 islands numbered from 1 to 34.
300 Hz desynchronizer at all levels (with 0.1 dB gain peaking).
5 kHz jitter measurement filter.
Other assumptions in Tables VIII.3-1 and VIII.3-2.

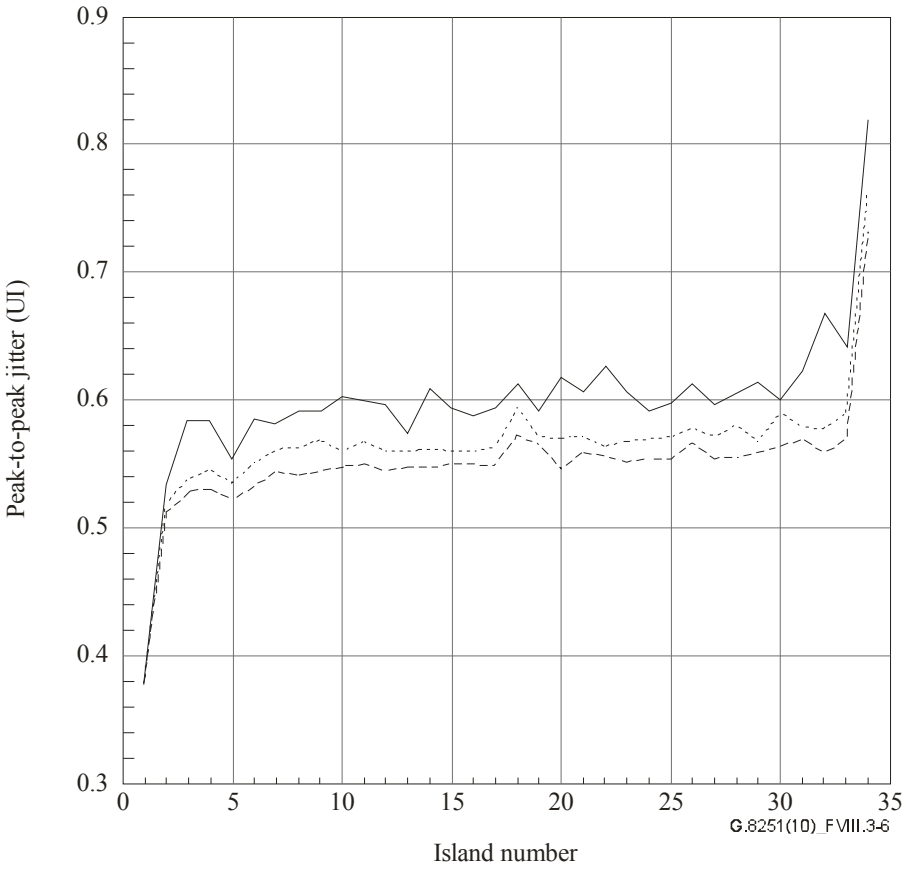
Figure VIII.3-4 – CBR2G5 client peak-to-peak wideband jitter results for Case 4 (Model 2)



—— 95th percentile, upper end of 99% confidence interval
----- 95th percentile, point estimate
– – – 95th percentile, lower end of 99% confidence interval

NOTE – ODU1 islands numbered from 1 to 34.
300 Hz desynchronizer at all levels (with 0.1 dB gain peaking).
5 kHz jitter measurement filter.
Other assumptions in Tables VIII.3-1 and VIII.3-2.

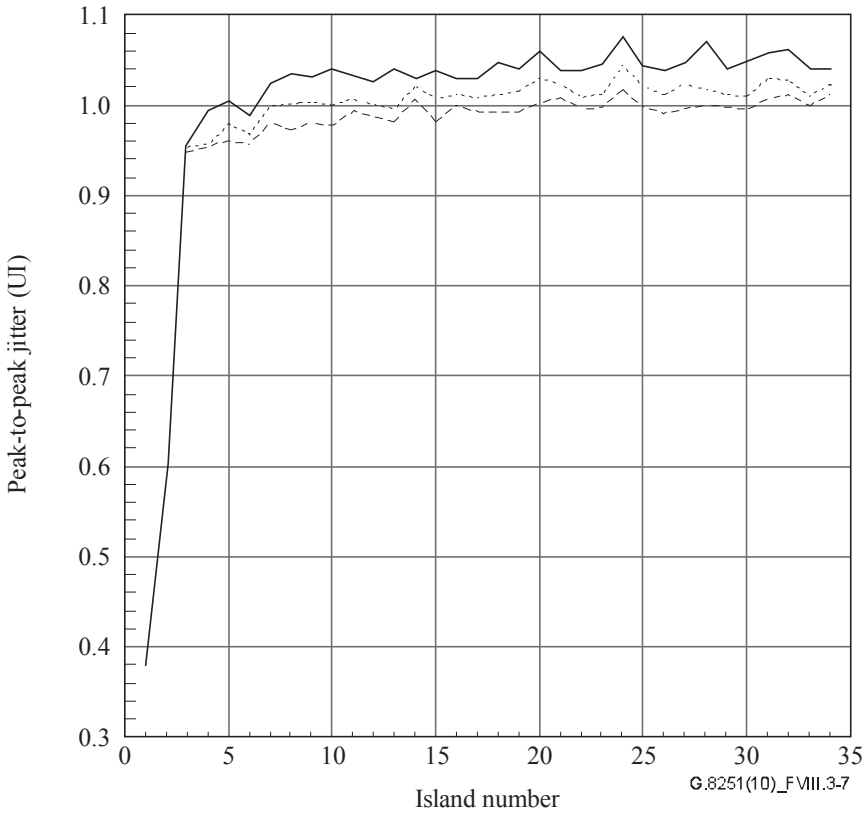
Figure VIII.3-5 – CBR2G5 client peak-to-peak wideband jitter results for Case 5 (Model 1)



—— 95th percentile, upper end of 99% confidence interval
····· 95th percentile, point estimate
– – – 95th percentile, lower end of 99% confidence interval

NOTE – ODU1 islands numbered from 1 to 34.
300 Hz desynchronizer at all levels (with 0.1 dB gain peaking).
5 kHz jitter measurement filter.
Other assumptions in Tables VIII.3-1 and VIII.3-2.

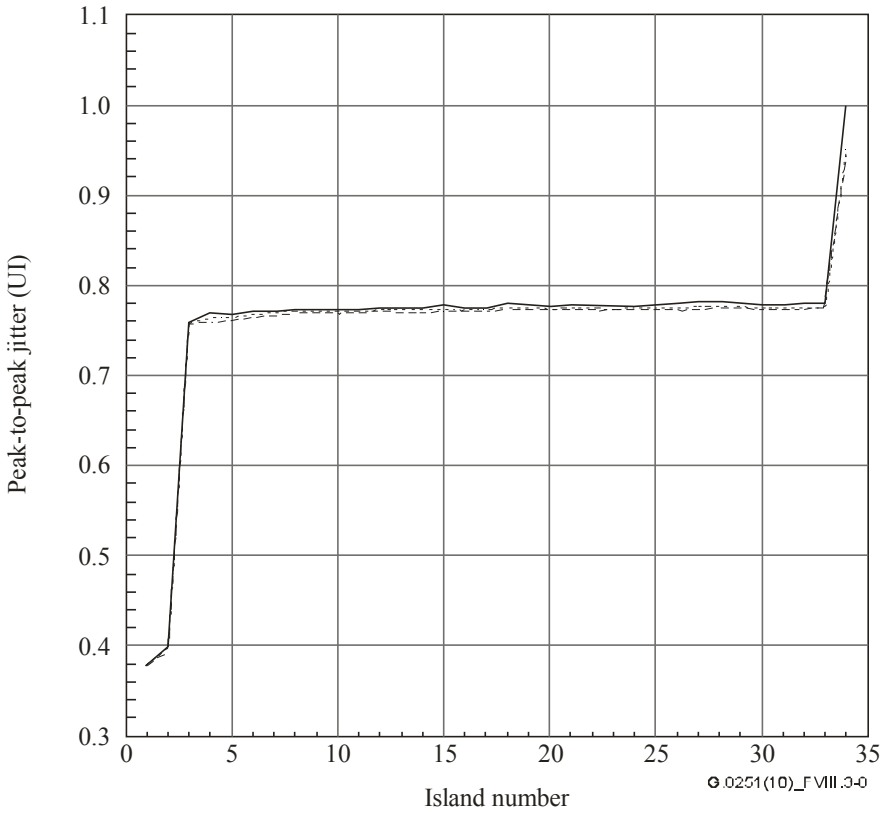
Figure VIII.3-6 – CBR2G5 client peak-to-peak wideband jitter results for Case 6 (Model 2)



—— 95th percentile, upper end of 99% confidence interval
----- 95th percentile, point estimate
– – – 95th percentile, lower end of 99% confidence interval

NOTE – ODU1 islands numbered from 1 to 34.
300 Hz desynchronizer at all levels (with 0.1 dB gain peaking).
5 kHz jitter measurement filter.
Other assumptions in Tables VIII.3-1 and VIII.3-2.

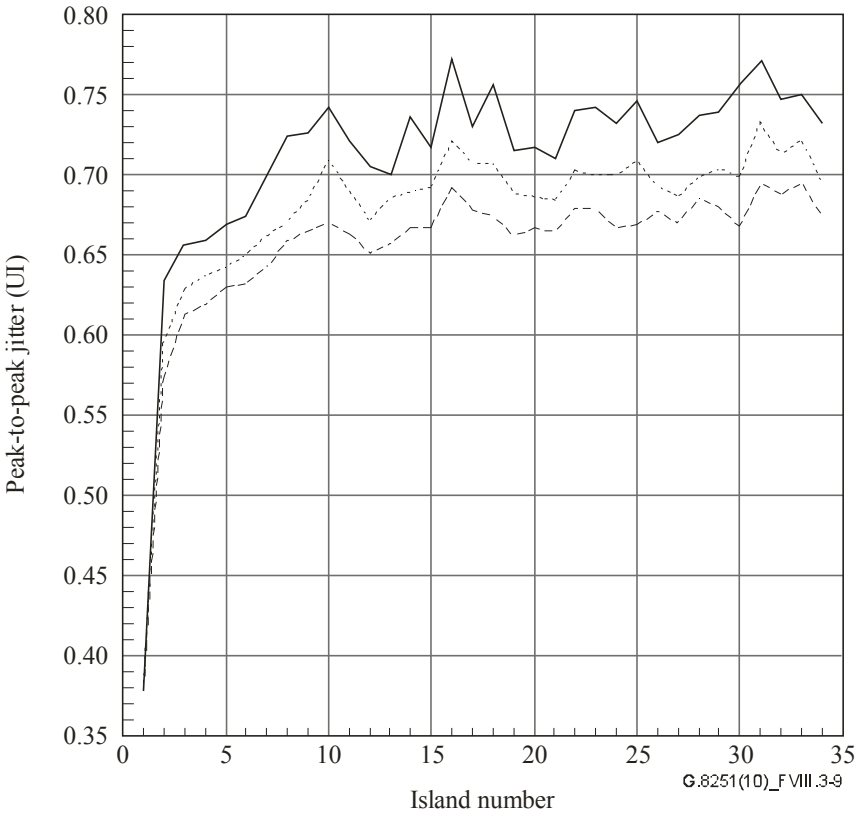
Figure VIII.3-7 – CBR2G5 client peak-to-peak wideband jitter results for Case 7 (Model 1)



—— 95th percentile, upper end of 99% confidence interval
----- 95th percentile, point estimate
– – – 95th percentile, lower end of 99% confidence interval

NOTE – ODU1 islands numbered from 1 to 34.
300 Hz desynchronizer at all levels (with 0.1 dB gain peaking).
5 kHz jitter measurement filter.
Other assumptions in Tables VIII.3-1 and VIII.3-2.

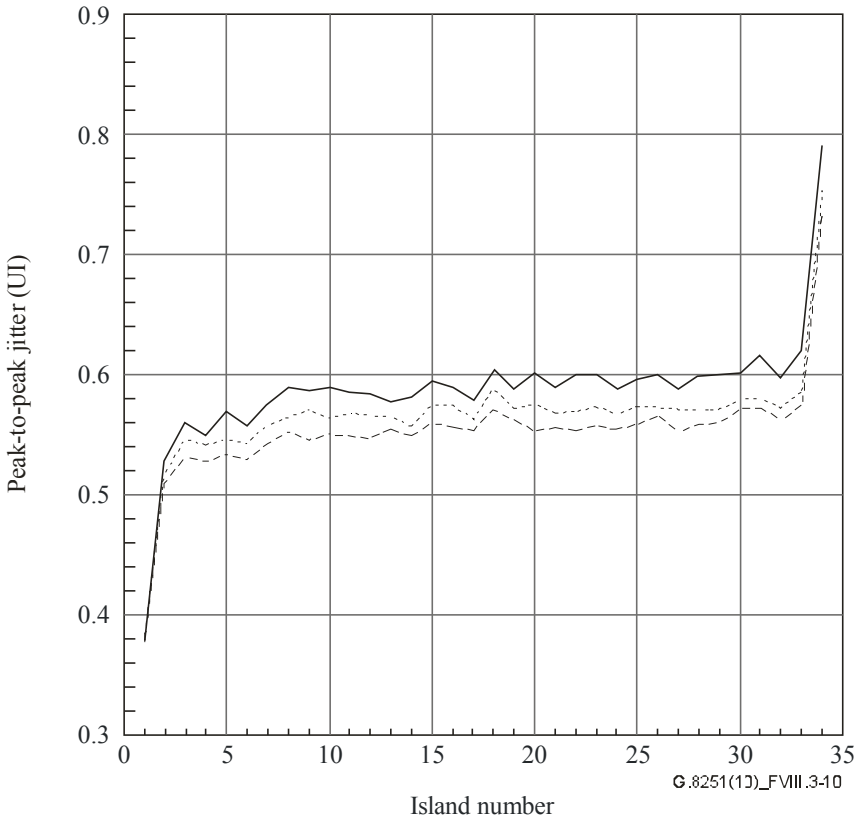
Figure VIII.3-8 – CBR2G5 client peak-to-peak wideband jitter results for Case 8 (Model 2)



—— 95th percentile, upper end of 99% confidence interval
----- 95th percentile, point estimate
– – – 95th percentile, lower end of 99% confidence interval

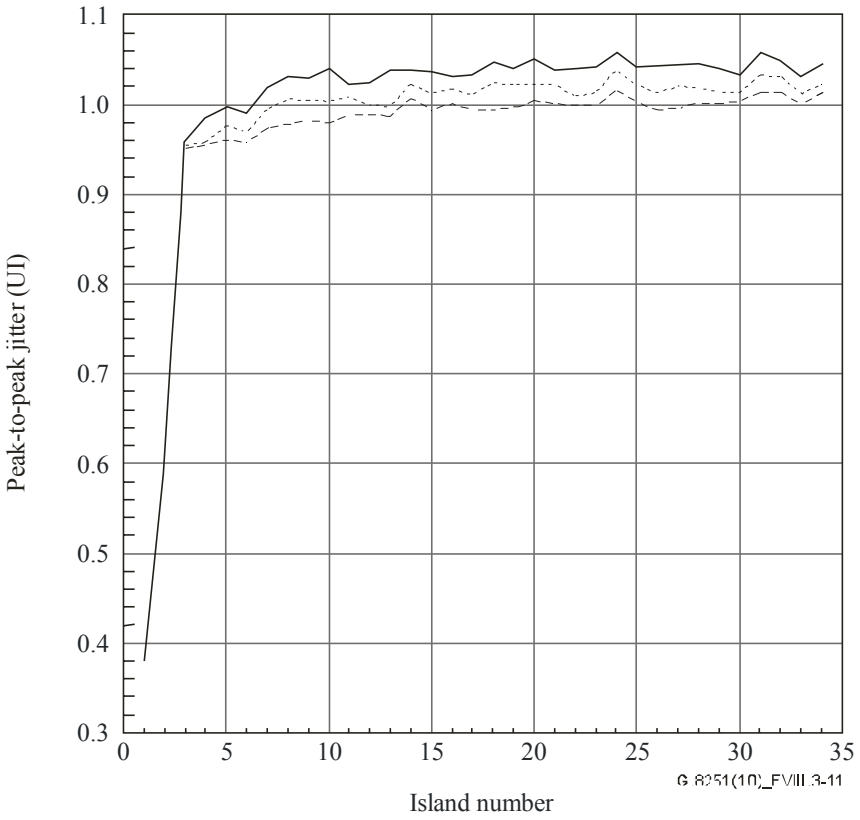
NOTE – ODU1 islands numbered from 1 to 34.
300 Hz desynchronizer at all levels (with 0.1 dB gain peaking).
5 kHz jitter measurement filter.
Other assumptions in Tables VIII.3-1 and VIII.3-2.

Figure VIII.3-9 – CBR2G5 client peak-to-peak wideband jitter results for Case 9 (Model 1)



NOTE – ODU1 islands numbered from 1 to 34.
300 Hz desynchronizer at all levels (with 0.1 dB gain peaking).
5 kHz jitter measurement filter.
Other assumptions in Tables VIII.3-1 and VIII.3-2.

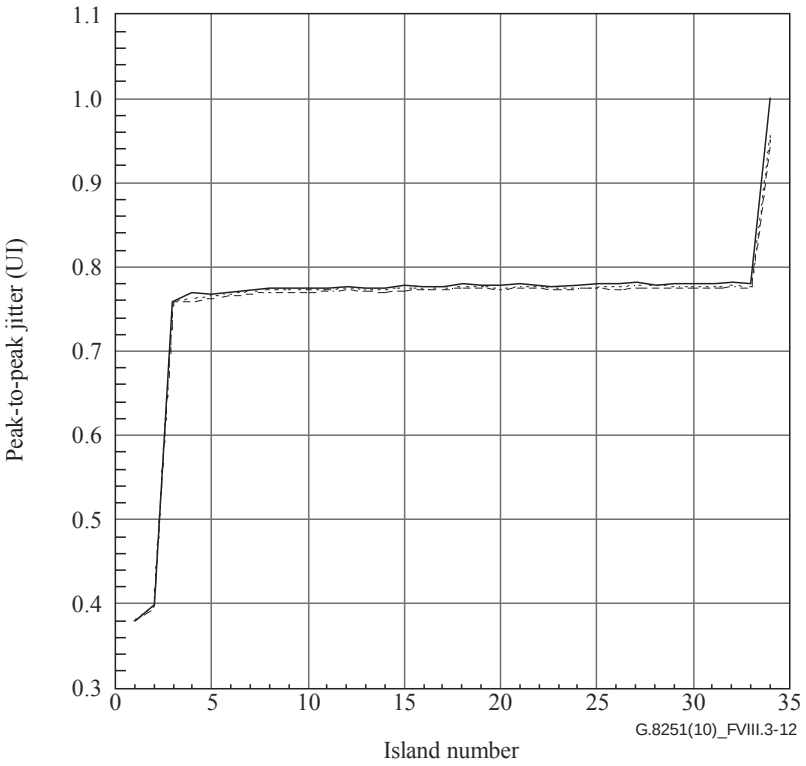
Figure VIII.3-10 – CBR2G5 client peak-to-peak wideband jitter results for Case 10 (Model 2)



—— 95th percentile, upper end of 99% confidence interval
····· 95th percentile, point estimate
– – – 95th percentile, lower end of 99% confidence interval

NOTE – ODU1 islands numbered from 1 to 34.
300 Hz desynchronizer at all levels (with 0.1 dB gain peaking)
5 kHz jitter measurement filter.
Other assumptions in Tables VIII.3-1 and VIII.3-2.

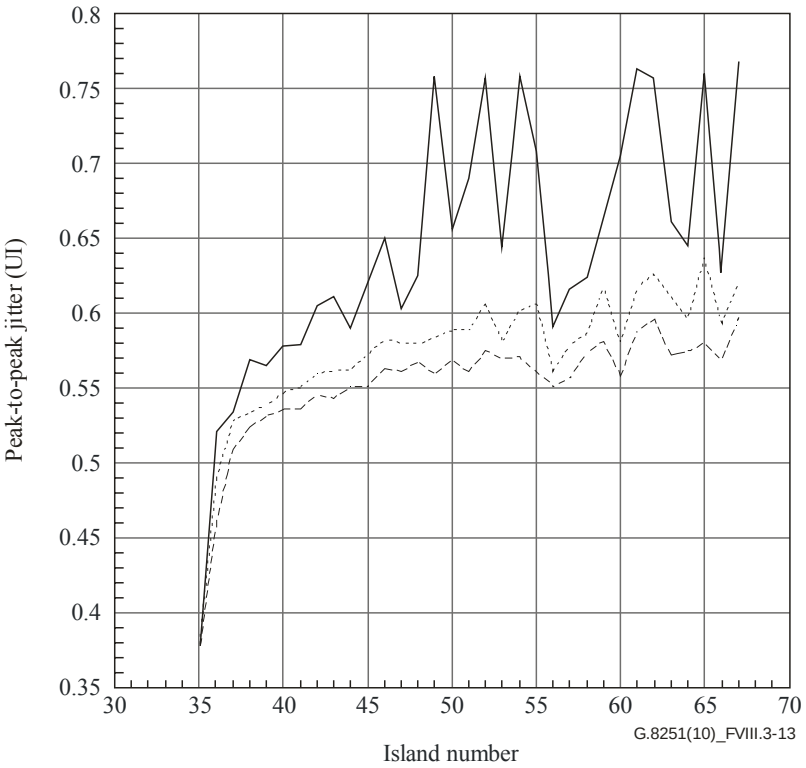
Figure VIII.3-11 – CBR2G5 client peak-to-peak wideband jitter results for Case 11 (Model 1)



—— 95th percentile, upper end of 99% confidence interval
····· 95th percentile, point estimate
– – – 95th percentile, lower end of 99% confidence interval

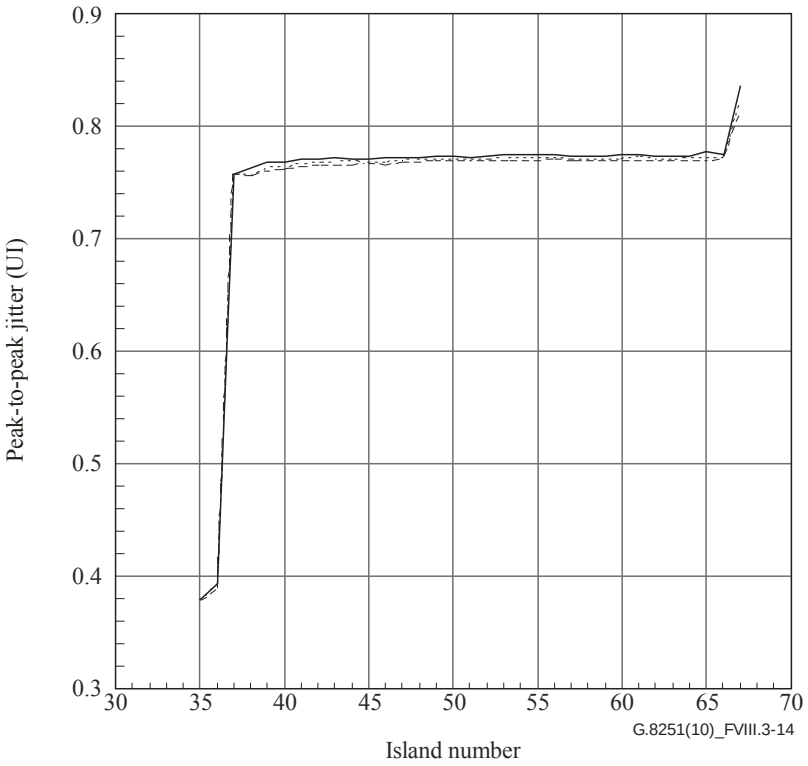
NOTE – ODU1 islands numbered from 1 to 34.
300 Hz desynchronizer at all levels (with 0.1 dB gain peaking).
5 kHz jitter measurement filter.
Other assumptions in Tables VIII.3-1 and VIII.3-2.

Figure VIII.3-12 – CBR2G5 client peak-to-peak wideband jitter results for Case 12 (Model 2)



NOTE – ODU2 islands numbered from 35 to 67.
300 Hz desynchronizer at all levels (with 0.1 dB gain peaking).
5 kHz jitter measurement filter.
Other assumptions in Tables VIII.3-1 and VIII.3-2.

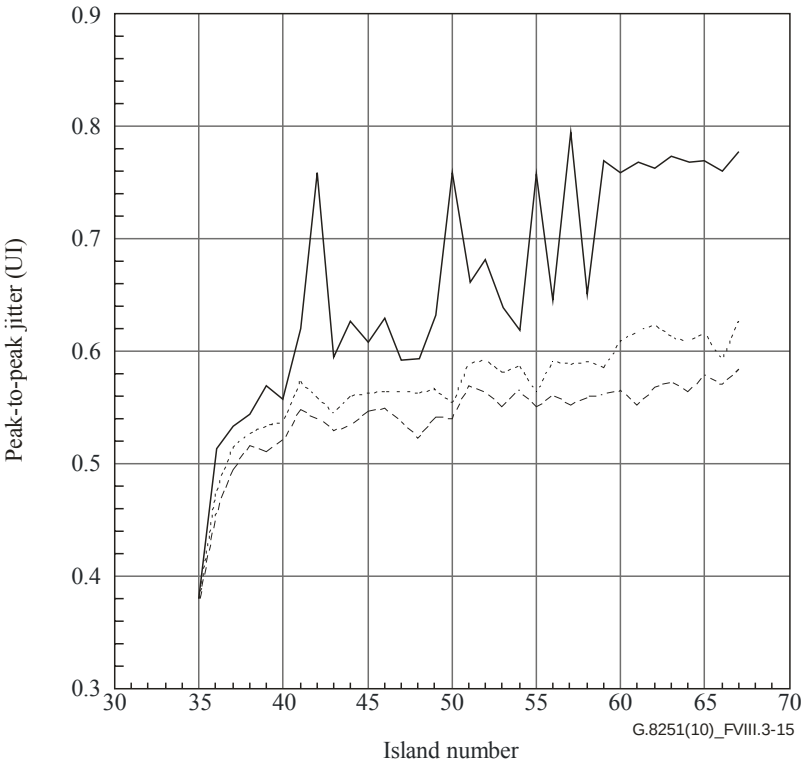
Figure VIII.3-13 – ODU1 client peak-to-peak wideband jitter results for Case 2 (Model 2)



—— 95th percentile, upper end of 99% confidence interval
····· 95th percentile, point estimate
– – – 95th percentile, lower end of 99% confidence interval

NOTE – ODU2 islands numbered from 35 to 67.
300 Hz desynchronizer at all levels (with 0.1 dB gain peaking).
5 kHz jitter measurement filter.
Other assumptions in Tables VIII.3-1 and VIII.3-2.

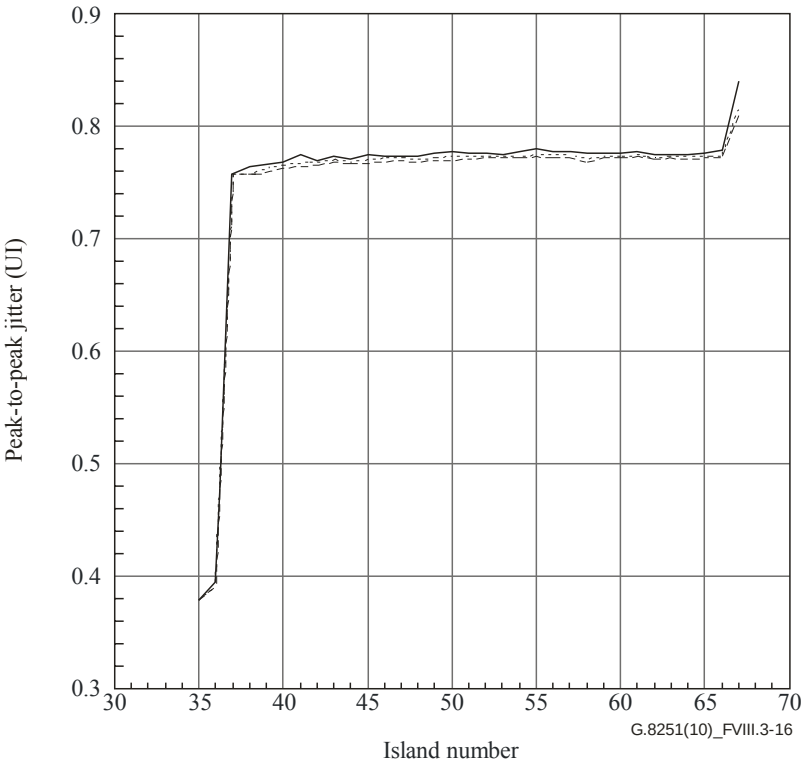
Figure VIII.3-14 – ODU1 client peak-to-peak wideband jitter results for Case 4 (Model 2)



—— 95th percentile, upper end of 99% confidence interval
····· 95th percentile, point estimate
– – – 95th percentile, lower end of 99% confidence interval

NOTE – ODU2 islands numbered from 35 to 67.
300 Hz desynchronizer at all levels (with 0.1 dB gain peaking).
5 kHz jitter measurement filter.
Other assumptions in Tables VIII.3-1 and VIII.3-2.

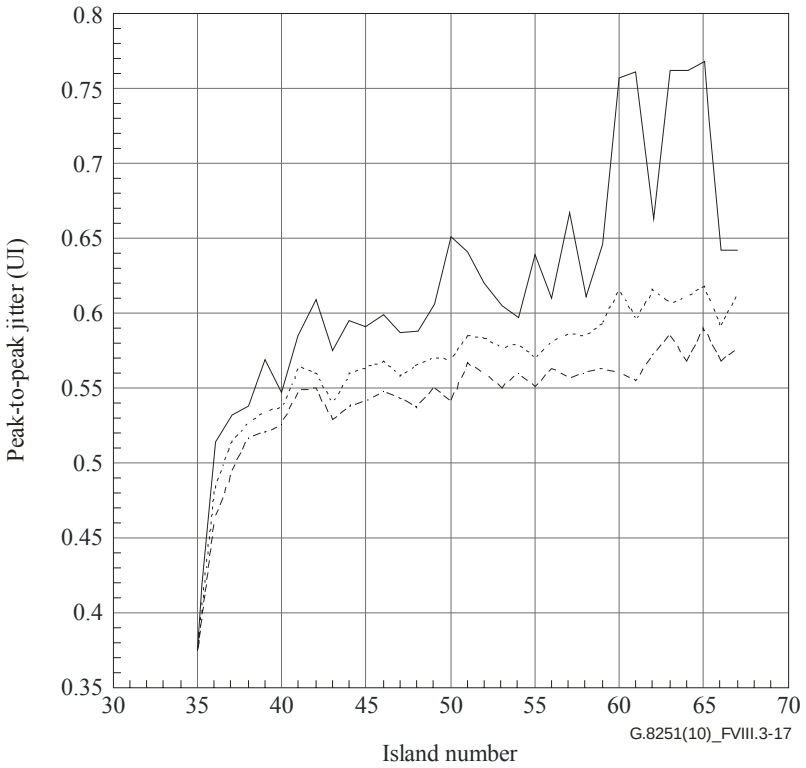
Figure VIII.3-15 – ODU1 client peak-to-peak wideband jitter results for Case 6 (Model 2)



—— 95th percentile, upper end of 99% confidence interval
····· 95th percentile, point estimate
– – – 95th percentile, lower end of 99% confidence interval

NOTE – ODU2 islands numbered from 35 to 67.
300 Hz desynchronizer at all levels (with 0.1 dB gain peaking).
5 kHz jitter measurement filter.
Other assumptions in Tables VIII.3-1 and VIII.3-2.

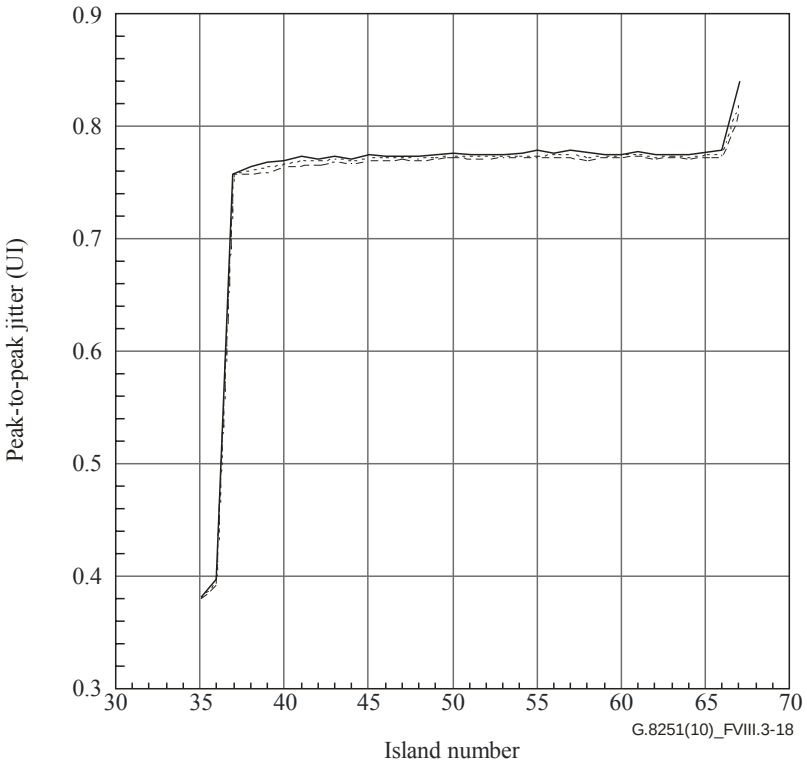
Figure VIII.3-16 – ODU1 client peak-to-peak wideband jitter results for Case 8 (Model 2)



—— 95th percentile, upper end of 99% confidence interval
····· 95th percentile, point estimate
– – – 95th percentile, lower end of 99% confidence interval

NOTE – ODU2 islands numbered from 35 to 67.
300 Hz desynchronizer at all levels (with 0.1 dB gain peaking).
5 kHz jitter measurement filter.
Other assumptions in Tables VIII.3-1 and VIII.3-2.

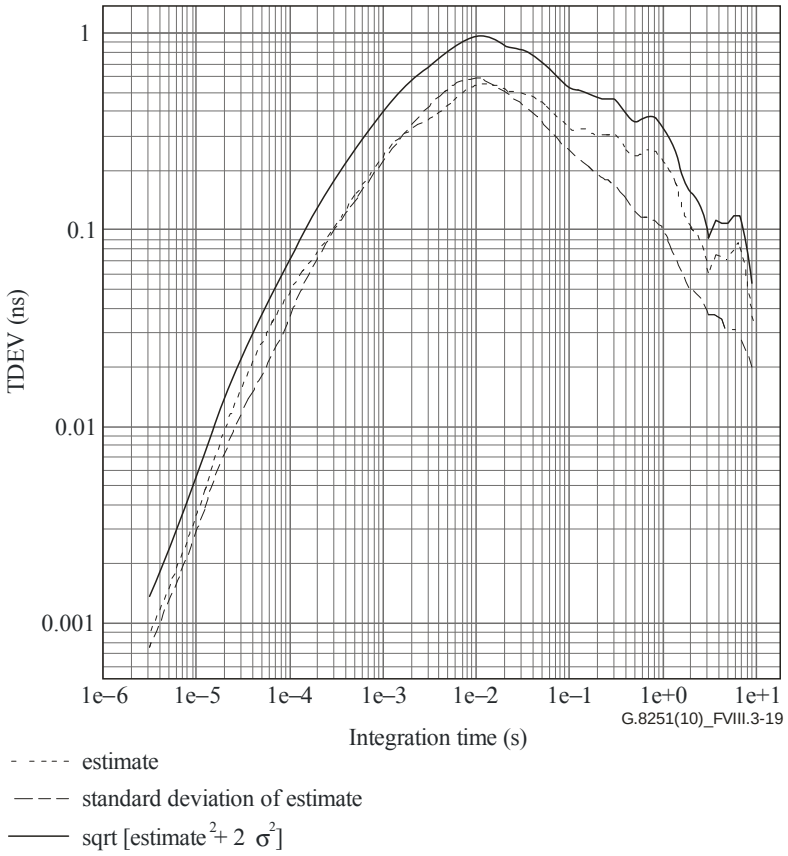
Figure VIII.3-17 – ODU1 client peak-to-peak wideband jitter results for Case 10 (Model 2)



—— 95th percentile, upper end of 99% confidence interval
····· 95th percentile, point estimate
– – – 95th percentile, lower end of 99% confidence interval

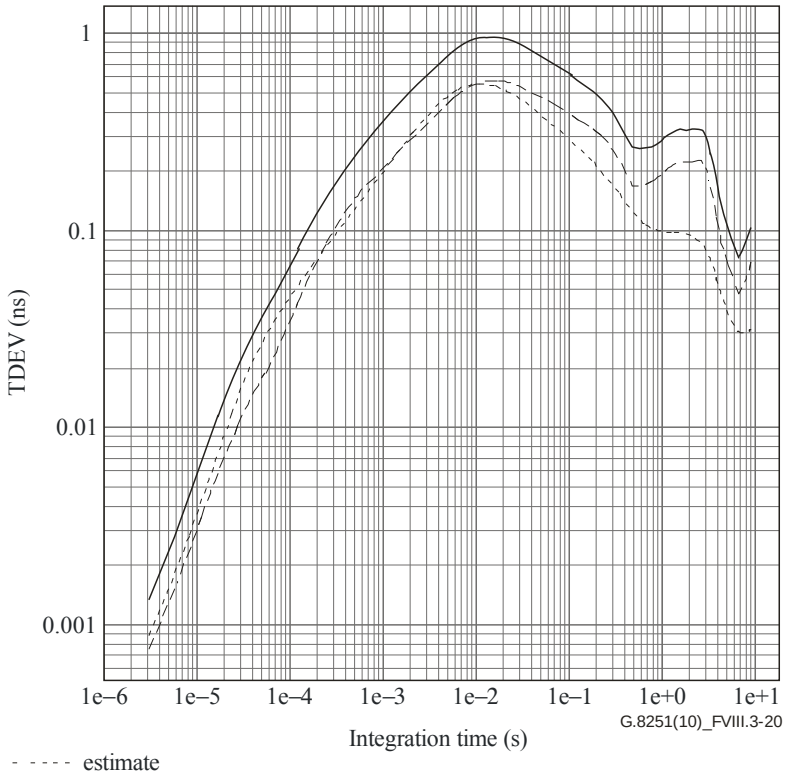
NOTE – ODU2 islands numbered from 35 to 67.
300 Hz desynchronizer at all levels (with 0.1 dB gain peaking).
5 kHz jitter measurement filter.
Other assumptions in Tables VIII.3-1 and VIII.3-2.

Figure VIII.3-18 – ODU1 client peak-to-peak wideband jitter results for Case 12 (Model 2)



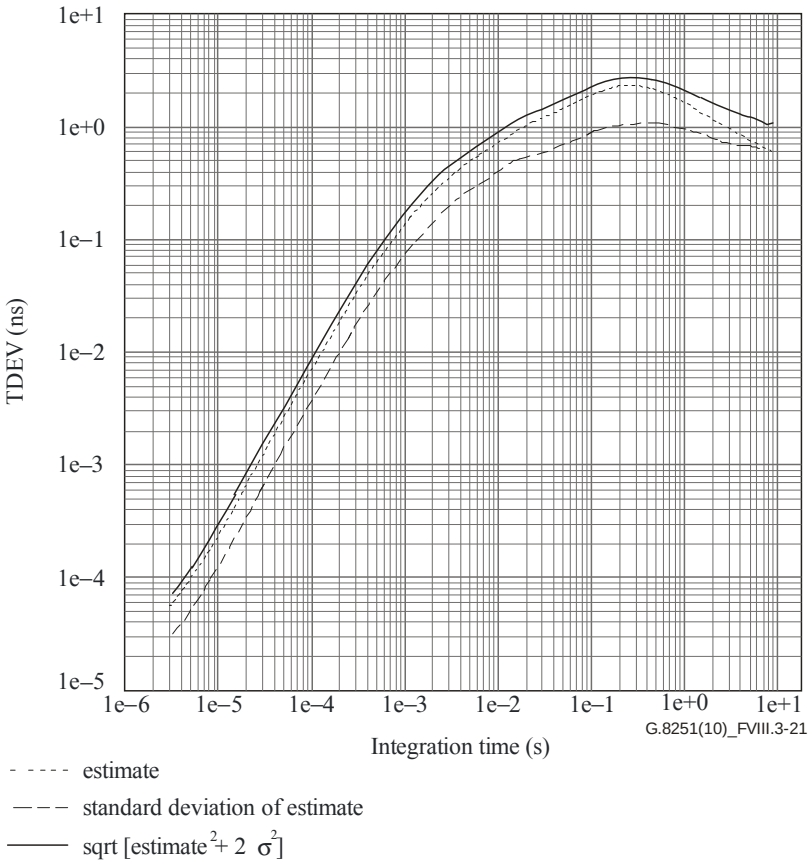
NOTE – ODU1 islands numbered from 1 to 34.
300 Hz desynchronizer at all levels (with 0.1 dB gain peaking).
Other assumptions in Tables VIII.3-1 and VIII.3-2.

Figure VIII.3-19 – CBR2G5 client short-term wander (TDEV) results for Case 1 (Model 1)



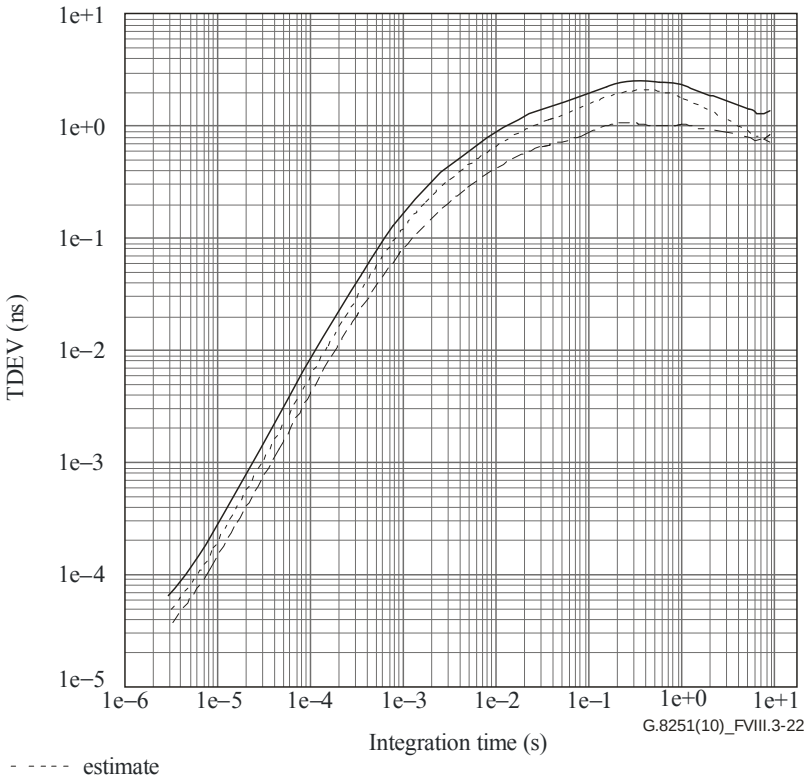
NOTE – ODU1 islands numbered from 1 to 34.
300 Hz desynchronizer at all levels (with 0.1 dB gain peaking).
Other assumptions in Tables VIII.3-1 and VIII.3-2.

Figure VIII.3-20 – CBR2G5 client short-term wander (TDEV) results for Case 2 (Model 2)



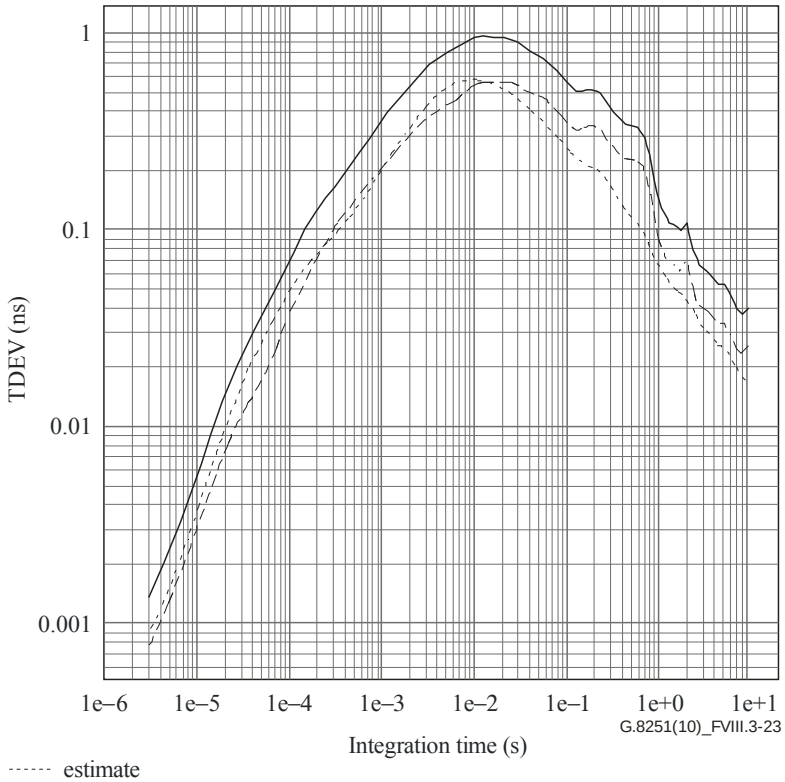
NOTE – ODU1 islands numbered from 1 to 34.
300 Hz desynchronizer at all levels (with 0.1 dB gain peaking).
Other assumptions in Tables VIII.3-1 and VIII.3-2.

Figure VIII.3-21 – CBR2G5 client short-term wander (TDEV) results for Case 3 (Model 1)



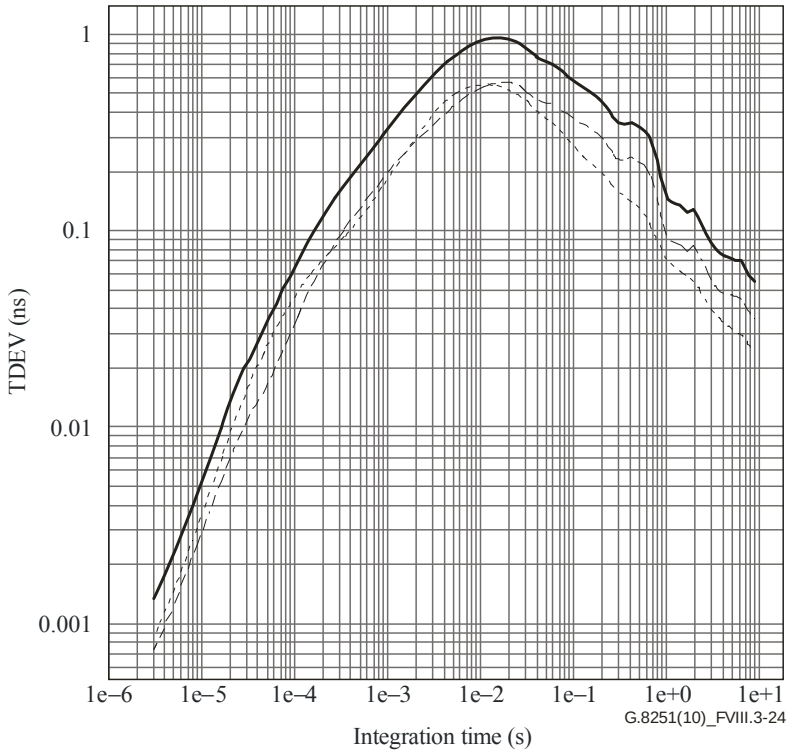
NOTE – ODU1 islands numbered from 1 to 34.
300 Hz desynchronizer at all levels (with 0.1 dB gain peaking).
Other assumptions in Tables VIII.3-1 and VIII.3-2.

Figure VIII.3-22 – CBR2G5 client short-term wander (TDEV) results for Case 4 (Model 2)



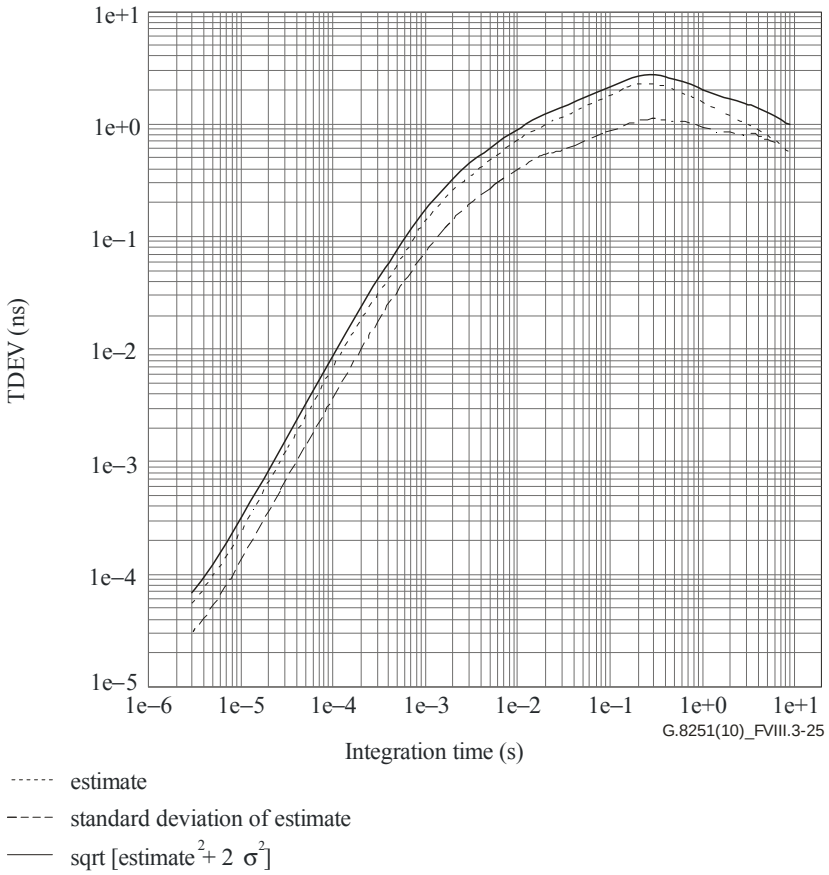
NOTE – ODU1 islands numbered from 1 to 34.
300 Hz desynchronizer at all levels (with 0.1 dB gain peaking).
Other assumptions in Tables VIII.3-1 and VIII.3-2.

Figure VIII.3-23 – CBR2G5 client short-term wander (TDEV) results for Case 5 (Model 1)



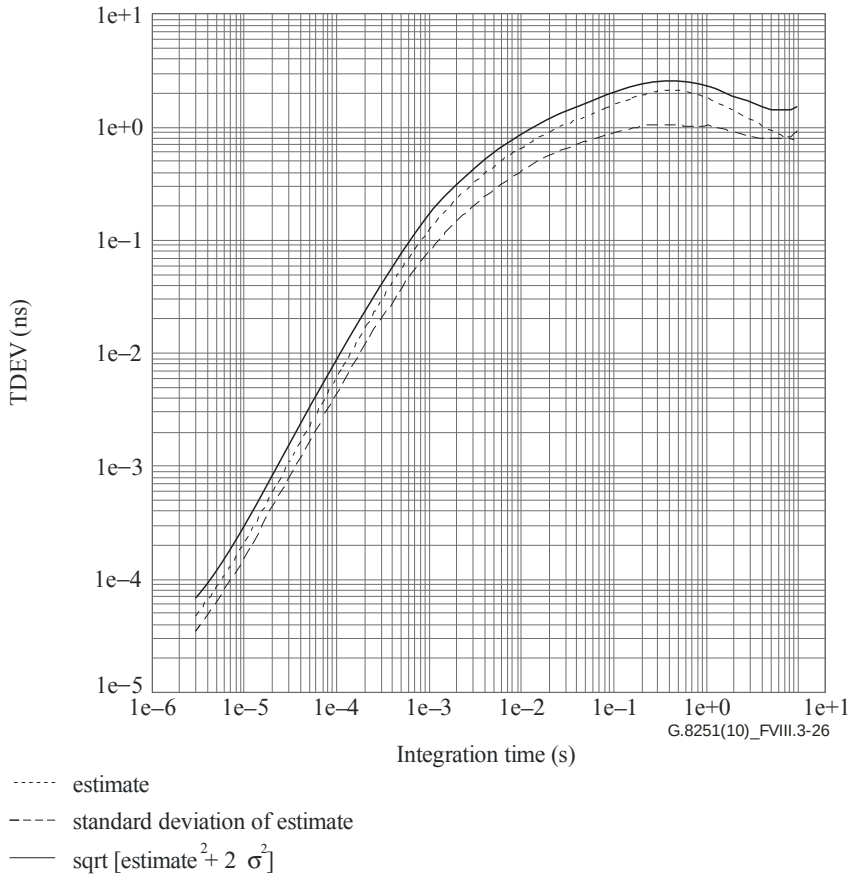
NOTE – ODU1 islands numbered from 1 to 34.
300 Hz desynchronizer at all levels (with 0.1 dB gain peaking).
Other assumptions in Tables VIII.3-1 and VIII.3-2.

Figure VIII.3-24 – CBR2G5 client short-term wander (TDEV) results for Case 6 (Model 2)



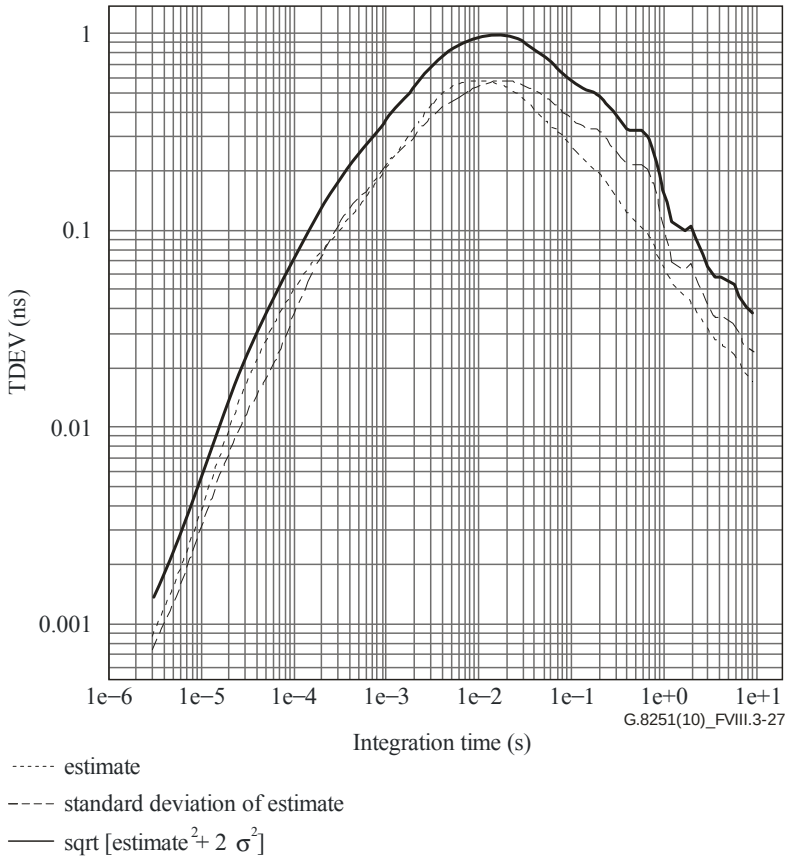
NOTE – ODU1 islands numbered from 1 to 34.
300 Hz desynchronizer at all levels (with 0.1 dB gain peaking).
Other assumptions in Tables VIII.3-1 and VIII.3-2.

Figure VIII.3-25 – CBR2G5 client short-term wander (TDEV) results for Case 7 (Model 1)



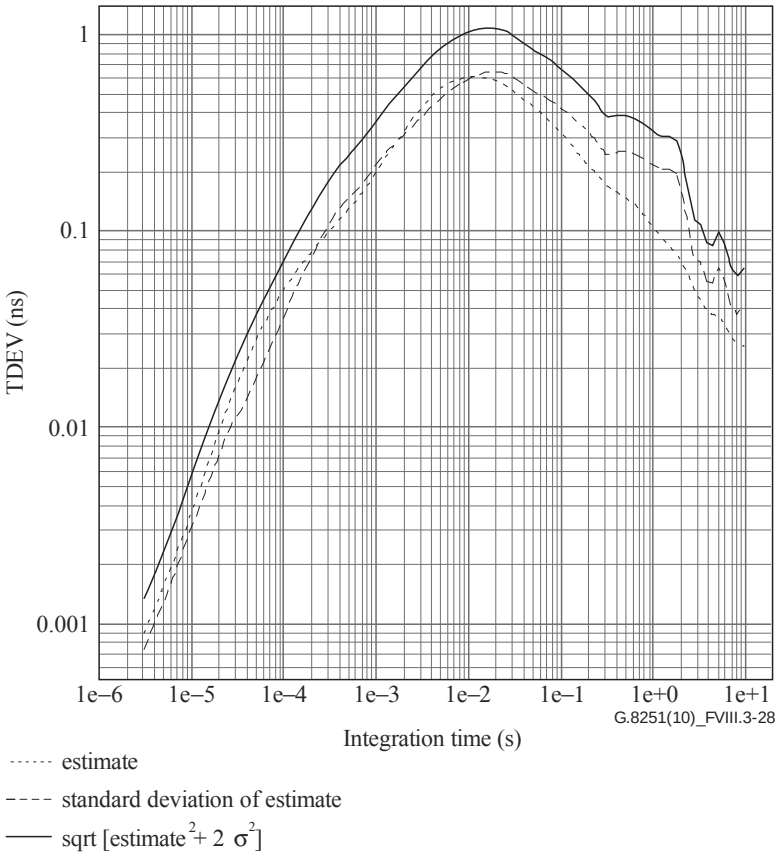
NOTE – ODU1 islands numbered from 1 to 34.
300 Hz desynchronizer at all levels (with 0.1 dB gain peaking).
Other assumptions in Tables VIII.3-1 and VIII.3-2.

Figure VIII.3-26 – CBR2G5 client short-term wander (TDEV) results for Case 8 (Model 2)



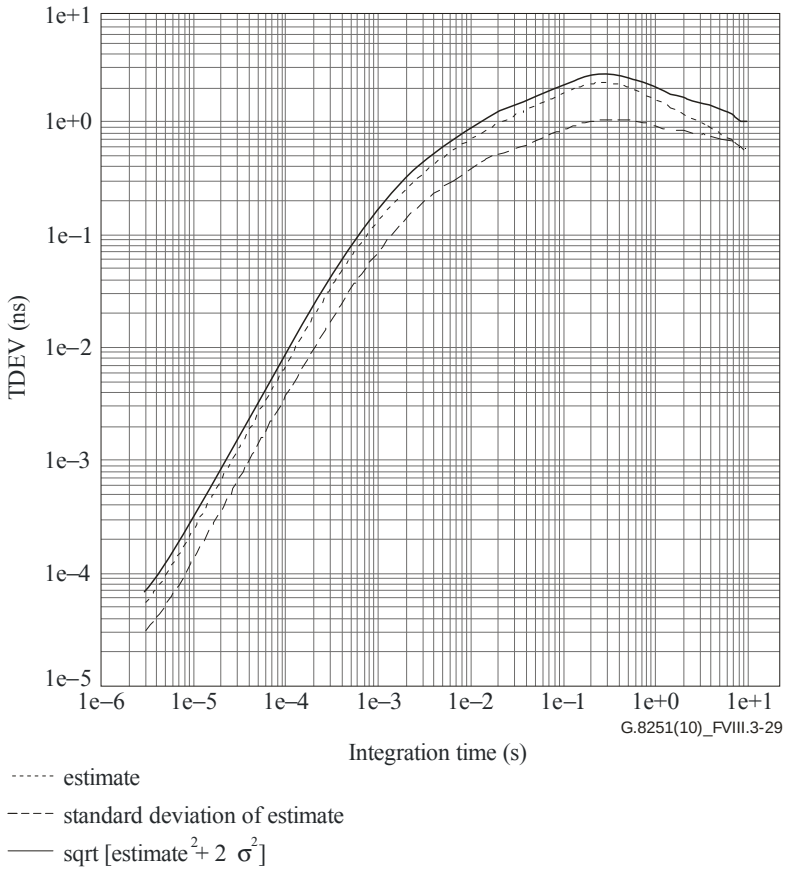
NOTE – ODU1 islands numbered from 1 to 34.
300 Hz desynchronizer at all levels (with 0.1 dB gain peaking).
Other assumptions in Tables VIII.3-1 and VIII.3-2.

Figure VIII.3-27 – CBR2G5 client short-term wander (TDEV) results for Case 9 (Model 1)



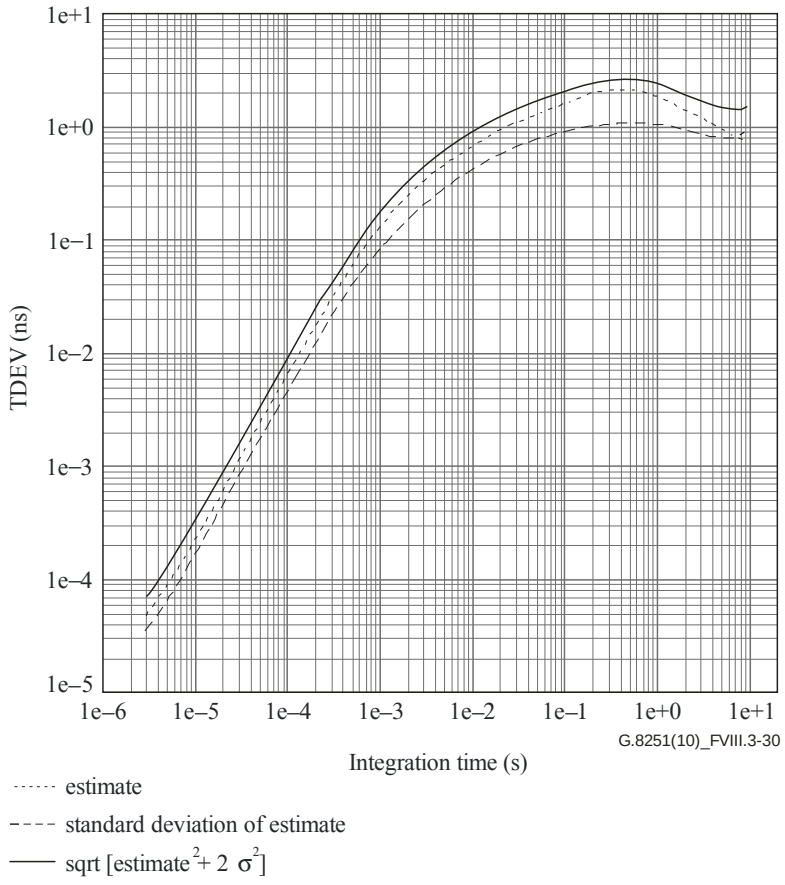
NOTE – ODU1 islands numbered from 1 to 34.
300 Hz desynchronizer at all levels (with 0.1 dB gain peaking).
Other assumptions in Tables VIII.3-1 and VIII.3-2.

Figure VIII.3-28 – CBR2G5 client short-term wander (TDEV) results for Case 10 (Model 2)



NOTE – ODU1 islands numbered from 1 to 34.
300 Hz desynchronizer at all levels (with 0.1 dB gain peaking).
Other assumptions in Tables VIII.3-1 and VIII.3-2.

Figure VIII.3-29 – CBR2G5 client short-term wander (TDEV) results for Case 11 (Model 1)



NOTE – ODU1 islands numbered from 1 to 34.
300 Hz desynchronizer at all levels (with 0.1 dB gain peaking).
Other assumptions in Tables VIII.3-1 and VIII.3-2.

Figure VIII.3-30 – CBR2G5 client short-term wander (TDEV) results for Case 12 (Model 2)

Bibliography

[b-ANSI 352] American National Standard for Information Technology – *Fibre Channel Physical Interfaces (FC – PI)*, ANSI INCITS 352 – 2002, December 1, 2002.

[b-ANSI 364] American National Standard for Information Technology – *Fibre Channel – 10 Gigabit (10GFC)*, ANSI INCITS 364-2003, November 6, 2003.

[b-ATIS 0900101] ATIS-0900101.2006 (Revision of T1.101/1999), *Synchronization Interface Standard*, American National Standard for Telecommunications, ATIS.

[b-Gardner] GARDNER, F.M., (1979), *Phaselock Techniques*, 2nd Edition, Wiley, New York.

[b-Leeson] LEESON, D.B., (1966), *A Simple Model of Feedback Oscillator Noise Spectrum*, Proc. IEEE, pp. 329-330, February.

[b-Papoulis] PAPOULIS, Athanasios, (1991), *Probability, Random Variables, and Stochastic Processes*, Third Edition, McGraw-Hill, p. 254 (Eq. (9-25)), New York.

[b-Schultz] SCHULTZ, Donald G., MELSA, James L., (1967), *State Functions and Linear Control Systems*, McGraw-Hill, New York.

[b-Trischitta] TRISCHITTA, P.R., and VARMA, E.L., (1989), *Jitter in Digital Transmission Systems,* Artech House, Norwood, MA.

[b-Varma] VARMA, E.L., WU, J. (1982), *Analysis of Jitter Accumulation in a Chain of Digital Regenerators*, Proceedings of IEEE Globecom, Vol. 2, p. 653-657.

[b-Wolaver] WOLAVER, D.H., (1991), *Phase-Locked Loop Circuit Design*, Prentice-Hall, Englewood Cliffs, NJ.

SERIES OF ITU-T RECOMMENDATIONS

Series A	Organization of the work of ITU-T
Series D	General tariff principles
Series E	Overall network operation, telephone service, service operation and human factors
Series F	Non-telephone telecommunication services
Series G	**Transmission systems and media, digital systems and networks**
Series H	Audiovisual and multimedia systems
Series I	Integrated services digital network
Series J	Cable networks and transmission of television, sound programme and other multimedia signals
Series K	Protection against interference
Series L	Construction, installation and protection of cables and other elements of outside plant
Series M	Telecommunication management, including TMN and network maintenance
Series N	Maintenance: international sound programme and television transmission circuits
Series O	Specifications of measuring equipment
Series P	Terminals and subjective and objective assessment methods
Series Q	Switching and signalling
Series R	Telegraph transmission
Series S	Telegraph services terminal equipment
Series T	Terminals for telematic services
Series U	Telegraph switching
Series V	Data communication over the telephone network
Series X	Data networks, open system communications and security
Series Y	Global information infrastructure, Internet protocol aspects and next-generation networks
Series Z	Languages and general software aspects for telecommunication systems

Printed in Switzerland
Geneva, 2011