INTERNATIONAL TELECOMMUNICATION UNION

ITU-T

TELECOMMUNICATION
STANDARDIZATION SECTOR
OF ITU

G.804

(02/98)

SERIES G: TRANSMISSION SYSTEMS AND MEDIA, DIGITAL SYSTEMS AND NETWORKS

Digital transmission systems – Digital networks – General aspects

---

ATM cell mapping into Plesiochronous Digital Hierarchy (PDH)

ITU-T Recommendation G.804

(Previously CCITT Recommendation)

ITU-T G-SERIES RECOMMENDATIONS

TRANSMISSION SYSTEMS AND MEDIA, DIGITAL SYSTEMS AND NETWORKS

INTERNATIONAL TELEPHONE CONNECTIONS AND CIRCUITS	G.100–G.199
TESTING EQUIPMENTS	
TRANSMISSION MEDIA CHARACTERISTICS	
General	G.600–G.609
Symmetric cable pairs	G.610–G.619
Land coaxial cable pairs	G.620–G.629
Submarine cables	G.630–G.649
Optical fibre cables	G.650–G.659
Characteristics of optical components and sub-systems	G.660–G.699
DIGITAL TRANSMISSION SYSTEMS	
TERMINAL EQUIPMENTS	G.700–G.799
General	G.700–G.709
Coding of analogue signals by pulse code modulation	G.710–G.719
Coding of analogue signals by methods other than PCM	G.720–G.729
Principal characteristics of primary multiplex equipment	G.730–G.739
Principal characteristics of second order multiplex equipment	G.740–G.749
Principal characteristics of higher order multiplex equipment	G.750–G.759
Principal characteristics of transcoder and digital multiplication equipment	G.760–G.769
Operations, administration and maintenance features of transmission equipment	G.770–G.779
Principal characteristics of multiplexing equipment for the synchronous digital hierarchy	G.780–G.789
Other terminal equipment	G.790–G.799
DIGITAL NETWORKS	G.800–G.899
General aspects	**G.800–G.809**
Design objectives for digital networks	G.810–G.819
Quality and availability targets	G.820–G.829
Network capabilities and functions	G.830–G.839
SDH network characteristics	G.840–G.849
Telecommunications management network	G.850–G.859
DIGITAL SECTIONS AND DIGITAL LINE SYSTEM	G.900–G.999
General	G.900–G.909
Parameters for optical fibre cable systems	G.910–G.919
Digital sections at hierarchical bit rates based on a bit rate of 2048 kbit/s	G.920–G.929
Digital line transmission systems on cable at non-hierarchical bit rates	G.930–G.939
Digital line systems provided by FDM transmission bearers	G.940–G.949
Digital line systems	G.950–G.959
Digital section and digital transmission systems for customer access to ISDN	G.960–G.969
Optical fibre submarine cable systems	G.970–G.979
Optical line systems for local and access networks	G.980–G.999

For further details, please refer to ITU-T List of Recommendations.

ITU-T RECOMMENDATION G.804

ATM CELL MAPPING INTO PLESIOCHRONOUS DIGITAL HIERARCHY (PDH)

Summary

This Recommendation provides the mapping to be used for the transport of ATM cells over PDHs at the various hierarchical bit rates defined in Recommendation G.702. These mappings cover both the 1544 kbit/s and 2048 kbit/s-based hierarchies and are used in conjunction with the frame structures defined in Recommendation G.832.

Source

ITU-T Recommendation G.804 was revised by ITU-T Study Group 15 (1997-2000) and was approved under the WTSC Resolution No. 1 procedure on the 10th of February 1998.

FOREWORD

ITU (International Telecommunication Union) is the United Nations Specialized Agency in the field of telecommunications. The ITU Telecommunication Standardization Sector (ITU-T) is a permanent organ of the ITU. The ITU-T is responsible for studying technical, operating and tariff questions and issuing Recommendations on them with a view to standardizing telecommunications on a worldwide basis.

The World Telecommunication Standardization Conference (WTSC), which meets every four years, establishes the topics for study by the ITU-T Study Groups which, in their turn, produce Recommendations on these topics.

The approval of Recommendations by the Members of the ITU-T is covered by the procedure laid down in WTSC Resolution No. 1.

In some areas of information technology which fall within ITU-T's purview, the necessary standards are prepared on a collaborative basis with ISO and IEC.

NOTE

In this Recommendation, the expression "Administration" is used for conciseness to indicate both a telecommunication administration and a recognized operating agency.

INTELLECTUAL PROPERTY RIGHTS

The ITU draws attention to the possibility that the practice or implementation of this Recommendation may involve the use of a claimed Intellectual Property Right. The ITU takes no position concerning the evidence, validity or applicability of claimed Intellectual Property Rights, whether asserted by ITU members or others outside of the Recommendation development process.

As of the date of approval of this Recommendation, the ITU had not received notice of intellectual property, protected by patents, which may be required to implement this Recommendation. However, implementors are cautioned that this may not represent the latest information and are therefore strongly urged to consult the TSB patent database.

CONTENTS

Recommendation G.804

ATM CELL MAPPING INTO PLESIOCHRONOUS DIGITAL HIERARCHY (PDH)

(Geneva, 1993; revised in 1998)

1 Introduction

This Recommendation identifies the way of transporting ATM cells over PDH networks at different hierarchical bit rates.

1.1 Scope

Existing transmission networks are based on Plesiochronous Digital Hierarchy (PDH) as defined in Recommendation G.702. ATM is considered as the suitable technique to support B-ISDN. The Synchronous Digital Hierarchy (SDH) will form the basis of transport of the ATM cells.

During the transition period, there are needs to transport ATM cells using existing PDH transmission networks. This Recommendation provides the mapping to be used for this transport of ATM cells on the different PDH bit rates for both 1544 and 2048 kbit/s hierarchies.

1.2 Abbreviations

This Recommendation uses the following abbreviations:

AIS	Alarm Indication Signal
ATM	Asynchronous Transfer Mode
BIP-8	Bit Interleaved Parity-8
B-ISDN	Broadband aspects of Integrated Services Digital Network
CRC	Cyclic Redundancy Check
FEAC	Far-End Alarm and Control
FEBE	Far-End Block Error
FERF	Far-End Receive Failure
HEC	Header Error Control
LCD	Loss of Cell Delineation
OAM	Operation, Administration and Maintenance
PDH	Plesiochronous Digital Hierarchy
PLCP	Physical Layer Convergence Protocol
POH	Path OverHead
POI	Path OverHead Identifier
RAI	Remote Alarm Indication
SDH	Synchronous Digital Hierarchy
TS	Time Slot

1.3 Definitions

This Recommendation defines the following terms:

1.3.1 idle cell: A cell which is inserted and extracted by the physical layer in order to adapt the cell flow rate at the boundary between the ATM layer and the physical layer to the available payload capacity of the transmission used.

1.3.2 valid cell: A cell whose header has no errors or has been modified by the cell Header Error Control (HEC) verification process.

1.3.3 nibble: A nibble is a group of four bits.

NOTE – The order of transmission of information in all diagrams in this Recommendation is first from left to right and then top to bottom. Within each byte the most significant bit is transmitted first. The most significant bit (bit 1) is illustrated at the left of all diagrams.

2 Mapping of ATM cells into 1544 kbit/s

2.1 Frame format

The multiframe structure for the 24-frame multiframe as described in Recommendation G.704 shall be used.

The ATM cell is mapped into bits 2 to 193 (i.e. time slots 1 to 24 described in Recommendation G.704) of the 1544 kbit/s frame with the octet structure of the cell aligned with the octet structure of the frame (see Figure 2-1).

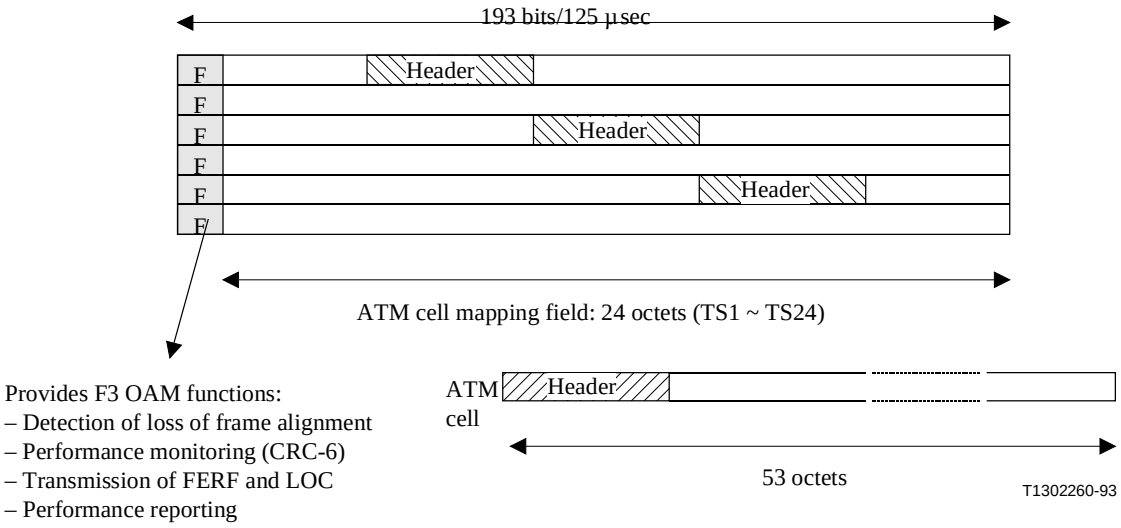

Figure 2-1/G.804 – Frame structure for 1544 kbit/s used to transport ATM cells

2.2 Cell rate adaptation

The cell rate adaptation to the payload capacity of the frames is performed by the insertion of idle cells, as described in Recommendation I.432.1, when valid cells are not available from the ATM layer.

2.3 Header Error Control (HEC) generation

The Header Error Control (HEC) value is generated and inserted in the specific field in compliance with Recommendation I.432.1.

2.4 Scrambling of the ATM cell payload (optional)

As an option, the ATM cell payload (48 bytes) can be scrambled before mapping into the 1544 kbit/s signal. If this option is used, then, the reverse operation, following termination of 1544 kbit/s signal, the ATM cell payload will be descrambled before being passed to ATM layer. The self-synchronizing scrambler with the generator polynomial $x^{43} + 1$, as described in Recommendation I.432.1, is used. If this option is not used, then no descrambling is done in the reverse operation.

2.5 Cell delineation

The cell delineation shall be performed using the Header Error Control (HEC) mechanism as defined in Recommendation I.432.1.

2.6 Cell header verification and extraction

The cell header verification shall be performed in compliance with Recommendation I.432.1. All physical layer cells shall be extracted and only valid cells are passed to the ATM layer.

2.7 Physical layer OAM

The error detection and performance reporting functions described in Recommendation G.704 are used. In addition, the Loss of Cell Delineation (LCD) is to be reported by a priority data link message. The specific 16-bit codeword is for further study.

3 Mapping of ATM cells into 2048 kbit/s

3.1 Frame format

The basic frame structure at 2048 kbit/s as described in Recommendation G.704 shall be used.

The ATM cell is mapped into bits 9 to 128 and bits 137 to 256 (i.e. time slots 1 to 15 and time slots 17 to 31 described in Recommendation G.704) of the 2048 kbit/s frame with the octet structure of the cell aligned with the octet structure of the frame (see Figure 3-1).

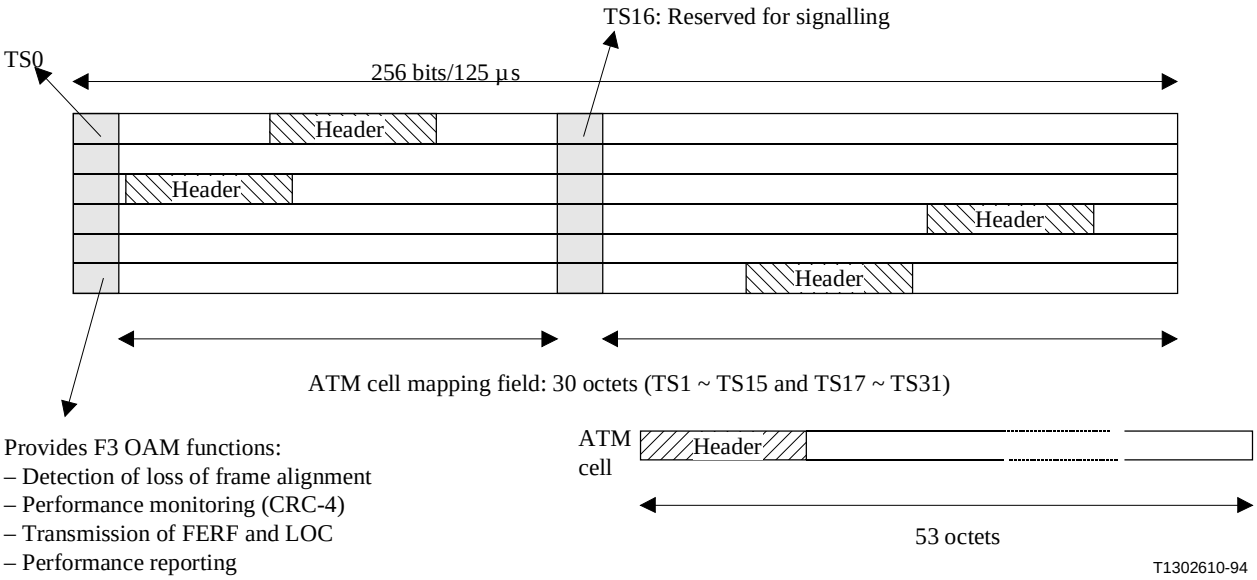

Figure 3-1/G.804 – Frame structure for 2048 kbit/s used to transport ATM cells

3.2 Cell rate adaptation

The cell rate adaptation to the payload capacity of the frames is performed by the insertion of idle cells, as described in Recommendation I.432.1, when valid cells are not available from the ATM layer.

3.3 Header Error Control (HEC) generation

The Header Error Control (HEC) value is generated and inserted in the specific field in compliance with Recommendation I.432.1.

3.4 Scrambling of the ATM cell payload

The ATM cell payload (48 bytes) shall be scrambled before mapping into the 2048 kbit/s signal. In the reverse operation, following termination of 2048 kbit/s signal, the ATM cell payload will be descrambled before being passed to the ATM layer. A self-synchronizing scrambler with the generator polynomial $x^{43} + 1$, as described in Recommendation I.432.1, shall be used. Cell payload field scrambling is required to provide security against false cell delineation and replication of the 2048 kbit/s frame alignment word.

3.5 Cell delineation

The cell delineation shall be performed using the Header Error Control (HEC) mechanism as defined in Recommendation I.432.1.

3.6 Cell header verification and extraction

The cell header verification shall be performed in compliance with Recommendation I.432.1. All the physical layer cells shall be extracted and only the valid cells are passed to the ATM layer.

3.7 Physical layer OAM

Overhead bits for physical layer OAM functionality are defined in Recommendation G.704.

4 Mapping of ATM cells into 6312 kbit/s

4.1 Frame format

The basic frame structure at 6312 kbit/s as described in Recommendation G.704 shall be used.

The ATM cell is mapped into bits 1 to 768 (i.e. time slots 1 to 96 described in Recommendation G.704) of the 6312 kbit/s frame with the octet structure of the cell aligned with the octet structure of the 6312 kbit/s frame. Bits 769 to 784 (time slots 97 and 98) are reserved for user communication channels and the last five bits (F-bits) are used for frame alignment and OAM (see Figure 4-1).

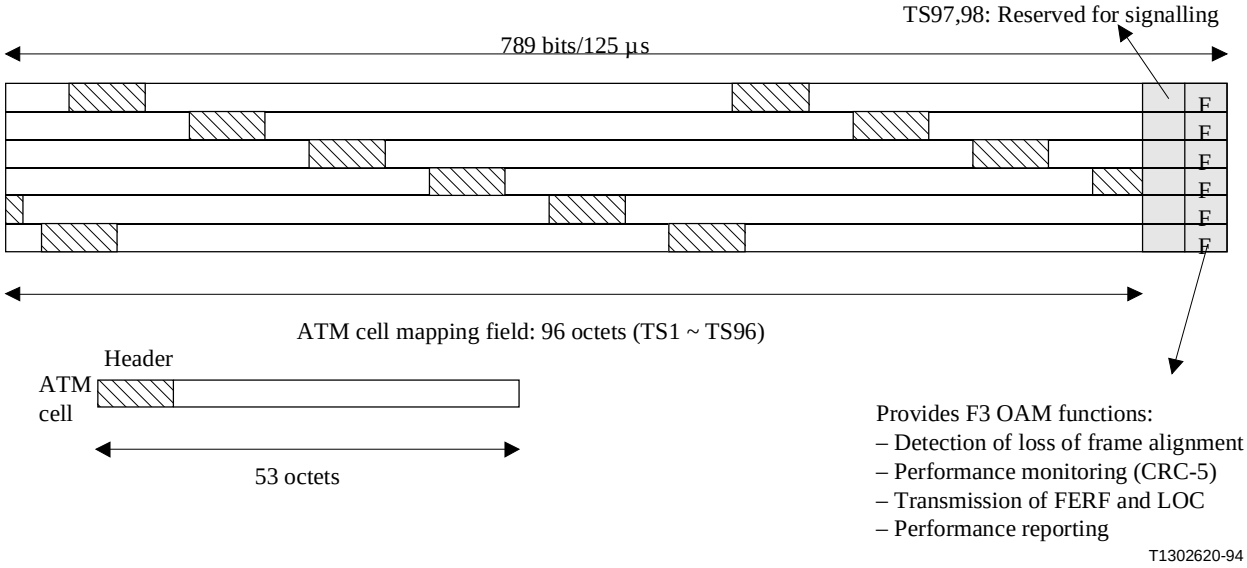

Figure 4-1/G.804 – Frame structure for 6312 kbit/s used to transport ATM cells

4.2 Cell rate adaptation

The cell rate adaptation to the payload capacity of the frames is performed by the insertion of idle cells, as described in Recommendation I.432.1, when valid cells are not available from the ATM layer.

4.3 Header Error Control (HEC) generation

The Header Error Control (HEC) value is generated and inserted in the specific field in compliance with Recommendation I.432.1.

4.4 Scrambling of the ATM cell payload

The ATM cell payload (48 bytes) shall be scrambled before mapping into the 6312 kbit/s signal. In the reverse operation, following termination of 6312 kbit/s signal, the ATM cell payload will be descrambled before being passed to the ATM layer. A self-synchronizing scrambler with the generator polynomial $x^{43} + 1$, as described in Recommendation I.432.1, shall be used. Cell payload field scrambling is required to provide security against false cell delineation and replication of the 6312 kbit/s frame alignment word.

4.5 Cell delineation

The cell delineation shall be performed using the Header Error Control (HEC) mechanism as defined in Recommendation I.432.1.

4.6 Cell header verification and extraction

The cell header verification shall be performed in compliance with Recommendation I.432.1. All the physical layer cells shall be extracted and only the valid cells are passed to the ATM layer.

4.7 Physical layer OAM

The error monitoring is performed by the CRC-5 procedure defined in Recommendation G.706. The transmission of the FERF is performed using the F-bits as described in Recommendation G.704. The FERF should also be used to indicate the LCD. The transmission of FEBE is for further study.

5 Mapping of ATM cells into 8448 kbit/s

For further study.

6 Mapping of ATM cells into 34 368 kbit/s

6.1 Frame format

The basic frame structure at 34 368 kbit/s as described in Recommendation G.832 shall be used.

The ATM cells are mapped into the 530 payload octets of the 34 368 kbit/s frame with the octet structure of the cell aligned with the octet structure of the frame (see Figure 6-1).

6.2 Cell rate adaptation

The cell rate adaptation to the payload capacity of the frames is performed by the insertion of idle cells, as described in Recommendation I.432.1, when valid cells are not available from the ATM layer.

6.3 Header Error Control (HEC)

The Header Error Control (HEC) value is generated and inserted in the specific field in compliance with Recommendation I.432.1.

6.4 Scrambling of the ATM cell payload

The ATM cell payload (48 bytes) shall be scrambled before mapping into the 34 368 kbit/s signal. In the reverse operation, following termination of 34 368 kbit/s signal, the ATM cell payload will be descrambled before being passed to the ATM layer. A self-synchronizing scrambler with the generator polynomial $x^{43} + 1$, as described in Recommendation I.432.1, shall be used. Cell payload field scrambling is required to provide security against false cell delineation and the replication of the 34 368 kbit/s frame alignment word.

6.5 Cell delineation

The cell delineation shall be performed using the HEC mechanism as defined in Recommendation I.432.1.

6.6 Cell header verification and extraction

The cell header verification shall be performed in compliance with Recommendation I.432.1. All physical layer cells shall be extracted and only valid cells are passed to the ATM layer.

6.7 Physical layer OAM

Overhead bytes for physical layer OAM functionality are defined in Recommendation G.832.

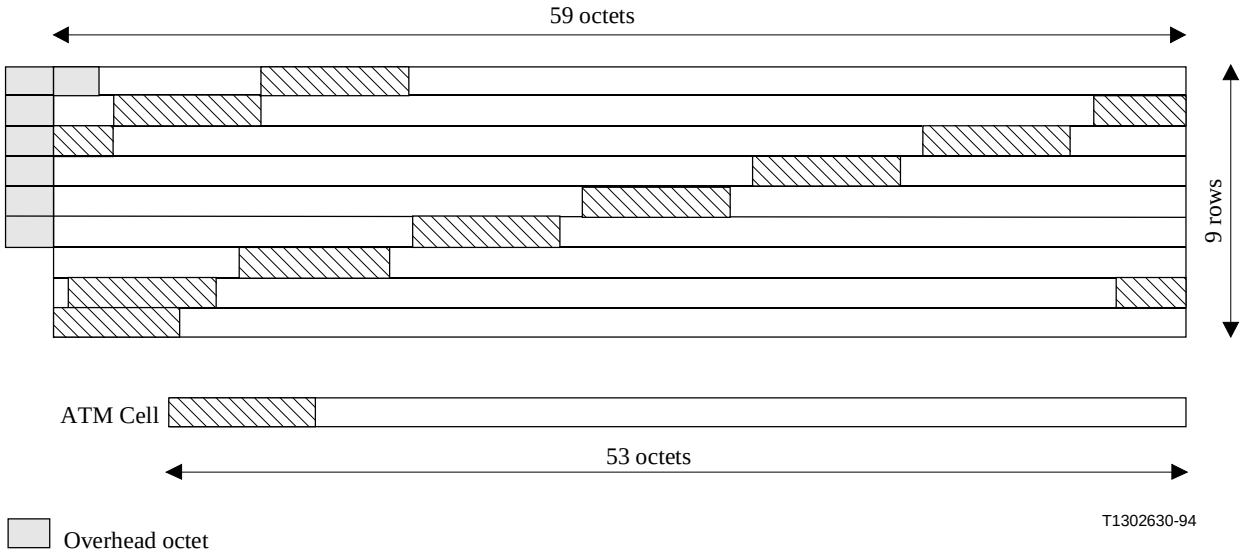

Figure 6-1/G.804 – Frame structure for 34 368 kbit/s used to transport ATM cells

7 Mapping of ATM cells into 44 736 kbit/s

7.1 Frame format

The multiframe format at 44 736 kbit/s, as described in Recommendation G.704, shall be used.

7.2 PLCP-based mapping of ATM cells

The ATM Physical Layer Convergence Protocol (PLCP) defines a mapping of ATM cells onto existing 44 736 kbit/s facilities. This PLCP is described in the following subclauses.

The PLCP consists of a 125 µs frame within a standard 44 736 kbit/s payload. Note there is no fixed relationship between the PLCP frame and the 44 736 kbit/s frame, i.e. the PLCP begins anywhere inside the 44 736 kbit/s payload. The PLCP frame (Figure 7-1) consists of 12 rows of ATM cells, each preceded by four octets of overhead. Nibble stuffing is required after the twelfth cell to fill the 125 µs PLCP frame. Although the PLCP is not aligned to the 44 736 kbit/s framing bits, the octets in the PLCP frame are nibble-aligned to the 44 736 kbit/s payload envelope. Nibbles begin after the control bits (F, X, P, C or M) of the 44 736 kbit/s frame. Note that the stuff bits are never used in the 44 736 kbit/s, i.e. the payload is always inserted. Octets comprising the PLCP frame are described in the following subclauses.

Note that order and transmission of all PLCP bits and octets are from left to right and top to bottom. The figures represent the Most Significant Bit (MSB) on the left and the Least Significant Bit (LSB) on the right.

PLCP	Framing	POI	POH	PLCP Payload	
A1	A2	P11	Z6	First ATM Cell	
A1	A2	P10	Z5	ATM Cell	
A1	A2	P09	Z4	ATM Cell	
A1	A2	P08	Z3	ATM Cell	
A1	A2	P07	Z2	ATM Cell	
A1	A2	P06	Z1	ATM Cell	
A1	A2	P05	X	ATM Cell	
A1	A2	P04	B1	ATM Cell	
A1	A2	P03	G1	ATM Cell	
A1	A2	P02	X	ATM Cell	
A1	A2	P01	X	ATM Cell	
A1	A2	P00	C1	Twelfth ATM Cell	Trailer
1 octet	1 octet	1 octet	1 octet	53 octets	13 or 14 nibbles
			Object of BIP-8 Calculation		

POI Path Overhead Indicator
POH Path Overhead
BIP-8 Bit Interleaved Parity-8
X Unassigned – Receiver required to ignore

Figure 7-1/G.804 – PLCP frame (125 μs)

7.2.1 Cell rate adaptation

The cell rate adaptation to the payload capacity of the PLCP frame is performed by the insertion of idle cells, as described in Recommendation I.432.1, when valid cells are not available from the ATM layer.

7.2.2 Header Error Control (HEC) generation

The HEC generation shall be compliant with Recommendation I.432.1.

7.2.3 Cell delineation

Since the cells are in predetermined locations within the PLCP, framing on the 44 736 kbit/s signal and then on the PLCP is sufficient in order to delineate cells.

7.2.4 Cell header verification and extraction

The cell header verification shall be compliant with Recommendation I.432.1. All physical layer cells shall be extracted and only valid cells are passed to the ATM layer.

7.2.5 Physical layer OAM

7.2.5.1 PLCP overhead utilization

The following PLCP overhead bytes/nibbles are required to be activated across the UNI:

– A1 Frame alignment;
– A2 Frame alignment;
– B1 PLCP path error monitoring;
– C1 Cycle/stuff counter;
– G1 PLCP path status;
– Px Path overhead identifier;
– Zx Growth octets;
– Trailer nibbles.

7.2.5.2 Frame alignment (A1, A2)

The PLCP framing octets use the same framing pattern as used in the SDH. These octets are defined as A1 = 11110110, A2 = 00101000.

7.2.5.3 PLCP path error monitoring (B1)

The Bit Interleaved Parity-8 (BIP-8) field supports path error monitoring, and is calculated over a 12×54 octet structure consisting of POH field and the associated ATM cells (648 octets) of the previous PLCP frame.

7.2.5.4 Cycle/stuff counter (C1)

In general, the cycle/stuff counter provides a nibble stuffing opportunity cycle and length indicator for the PLCP frame. A stuffing opportunity occurs every third frame of a three-frame (375 μs) stuffing cycle. The value of the C1 code is used as an indication of the phase of the 375 μs stuffing opportunity cycle (see Table 7-1).

Table 7-1 shows that a trailer containing 13 nibbles is used in the first frame of the 375 μs stuffing opportunity cycle. A trailer of 14 nibbles is used in the second frame. The third frame provides a nibble stuffing opportunity. A trailer containing 14 nibbles is used in the third frame if a stuff occurs. If not, the trailer will contain 13 nibbles.

Table 7-1/G.804 – Cycle/stuff counter definition

C1 code	Frame phase of cycle	Trailer length
11111111	1	13
00000000	2	14
01100110	3 (no stuff)	13
10011001	3 (stuff)	14

7.2.5.5 PLCP path status (G1)

The PLCP path status is allocated to convey the received PLCP status and performance to the transmitting far-end. This octet permits the status of the full receive/transmit PLCP path to be monitored at either end of the path. Figure 7-2 illustrates the G1 octet subfields: a 4-bit Far-End Block Error (FEBE), a 1-bit Remote Alarm Indication (RAI), and 3 X bits (X bits are set to all ones

at the transmitter and may be ignored at the receiver). The use of the PLCP path status octet G1 for the Far-End Receive Failure (FERF) is for further study.

Far-End Block Error (FEBE)	RAI	X-X-X
4 Bits	1 bit	3 bits

Figure 7-2/G.804 – PLCP path status (G1) definition

7.2.5.6 Path overhead identifier (P00-P11)

The Path OverHead Identifier (POI) indexes the adjacent Path OverHead (POH) octet of the PLCP. Table 7-2 provides the coding for each of the P00-P11 octets.

7.2.5.7 Growth octets (Z1-Z6)

The growth octets are reserved for future use. These octets are set to Zi-00000000, by the transmitter (i = 1, 2, ..., 6). The receiver shall be capable of ignoring the value contained in these fields.

7.2.5.8 Trailer nibbles

The contents of each of the 13/14 trailer nibbles shall be 1100.

7.3 HEC-based mapping of ATM into 44 736 kbit/s

7.3.1 Mapping of ATM cells into 44 736 kbit/s multiframe

The ATM cells are mapped into the payload with the octet structure of the cells aligned with the nibble structure of the multiframe. The multiframe is organized such that 84 bits of payload follow every overhead bit. The 84 bits can be assumed to be organized into 21 consecutive nibbles. The ATM cell is placed such that the start of a cell always coincides with the start of a nibble. ATM cells may cross multiframe boundaries (see Figure 7-3).

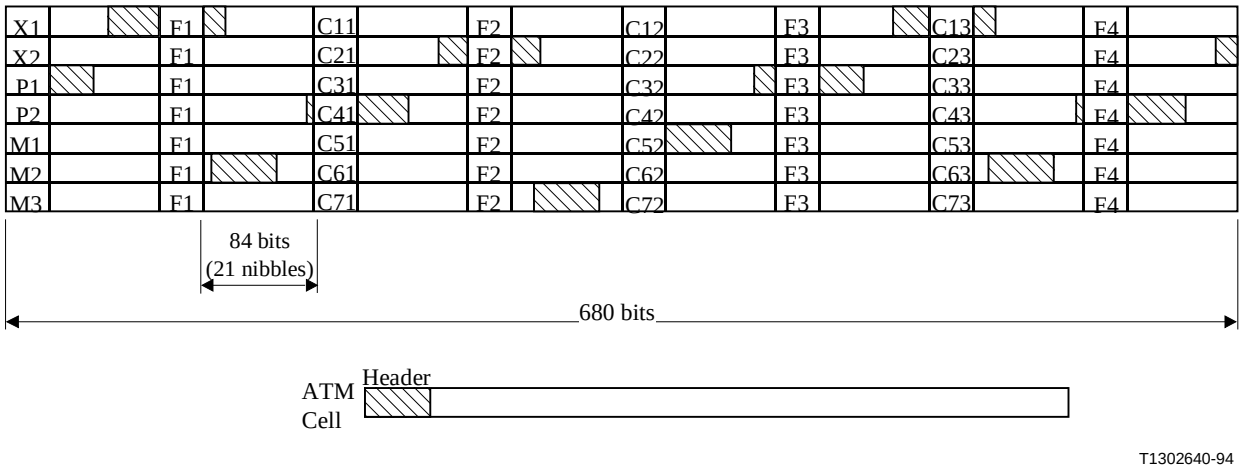

Figure 7-3/G.804 – Frame structure for 44 736 kbit/s used to transport ATM cells

7.3.2 Cell rate adaptation

The cell rate adaptation to the payload capacity of the frames is performed by the insertion of idle cells, as described in 4.4/I.432.1, when no valid cells are available from the ATM layer.

7.3.3 Header Error Control (HEC) generation

The Header Error Control (HEC) value is generated and inserted in the specific field in compliance with Recommendation I.432.1.

7.3.4 Cell delineation

The cell delineation shall be performed using the Header Error Control (HEC) mechanism defined in Recommendation I.432.1.

7.3.5 Cell header verification and extraction

The cell header verification shall be performed in compliance with Recommendation I.432.1.

All the physical layer cells shall be discarded and only valid cells are passed to the ATM layer.

7.3.6 Physical layer OAM

The error detection and performance reporting functions of the C-bit parity application of the 44 736 kbit/s multiframe described in Recommendation G.704 are used. In addition, Loss of Cell Delineation (LCD) and Remote Defect Indication (RDI) are to be reported by C13 Far-End Alarm and Control (FEAC) bit of the overhead bits in the C-bit parity application. The specific 16-bit codewords are to be used from Table 6/G.704.

NOTE – The need for reporting Out of Cell Delineation (OCD) is for further study.

Table 7-2/G.804 – Cycle/stuff counter definition

POI	POI code	Associated POH
P11	00101100	Z6
P10	00101001	Z5
P09	00100101	Z4
P08	00100000	Z3
P07	00011100	Z2
P06	00011001	Z1
P05	00010101	X
P04	00010000	B1
P03	00001101	G1
P02	00001000	X
P01	00000100	X
P00	00000001	C1
X Receiver ignores		

8 Mapping of ATM cells into 97 728 kbit/s

8.1 Frame format

The basic frame structure at 97 728 kbit/s, as described in Recommendation G.832, shall be used.

The ATM cells are mapped into the 756 octets of the C3 inside the 97 728 kbit/s frame with the octet structure of the cell aligned with the octet structure of the payload.

8.2 Cell rate adaptation

The cell rate adaptation to the payload capacity of the 97 728 kbit/s frames is performed by the insertion of idle cells, as described in Recommendation I.432.1, when valid cells are not available from the ATM layer.

8.3 Header Error Control (HEC) generation

The Header Error Control (HEC) value is generated and inserted in the specific field in compliance with Recommendation I.432.1.

8.4 Scrambling of the ATM cell payload

The ATM cell payload (48 bytes) shall be scrambled before mapping into the C3. In the reverse operation, following termination of 97 728 kbit/s signal, the ATM cell payload will be descrambled before being passed to ATM layer. A self-synchronizing scrambler with the generator polynomial $x^{43} + 1$, as described in Recommendation I.432.1, shall be used. Cell payload field scrambling is required to provide security against false cell delineation and replication of the 97 728 kbit/s frame alignment word.

8.5 Cell delineation

The cell delineation shall be performed using the Header Error Control (HEC) mechanism as defined in Recommendation I.432.1.

8.6 Cell header verification and extraction

The cell header verification shall be performed in compliance with Recommendation I.432.1. All physical layer cells shall be extracted and only valid cells are passed to the ATM layer.

8.7 Physical layer OAM

The OAM functionality is performed using the overhead bytes defined in Recommendation G.832.

9 Mapping of ATM cells into 139 264 kbit/s

9.1 Frame format

The basic frame structure at 139 264 kbit/s, as described in Recommendation G.832, shall be used.

The ATM cells are mapped into the 2160 payload octets of the 139 264 kbit/s frame with the octet structure of the cell aligned with the octet structure of the frame (see Figure 9-1).

9.2 Cell rate adaptation

The cell rate adaptation to the payload capacity of the frames is performed by the insertion of idle cells, as described in Recommendation I.432.1, when valid cells are not available from the ATM layer.

9.3 Header Error Control (HEC) generation

The HEC value is generated and inserted in the specific field in compliance with Recommendation I.432.1.

9.4 Scrambling of the ATM cell payload

The ATM cell payload (48 bytes) shall be scrambled before mapping into 139 264 kbit/s signal. In the reverse operation, following termination of 139 264 kbit/s signal, the ATM cell payload will be descrambled before being passed to ATM layer. A self-synchronizing scrambler with the generator polynomial $x^{43} + 1$, as described in Recommendation I.432.1, shall be used. Cell payload field scrambling is required to provide security against false cell delineation and replication of the 139 264 kbit/s frame alignment word.

9.5 Cell delineation

The cell delineation shall be performed using the Header Error Control (HEC) mechanism as defined in Recommendation I.432.1.

9.6 Cell header verification and extraction

The cell header verification shall be performed in compliance with Recommendation I.432.1. All the physical layer cells shall be extracted and only the valid cells are passed to the ATM layer.

9.7 Physical layer OAM

The OAM functionality is performed using the overhead bytes defined in Recommendation G.832.

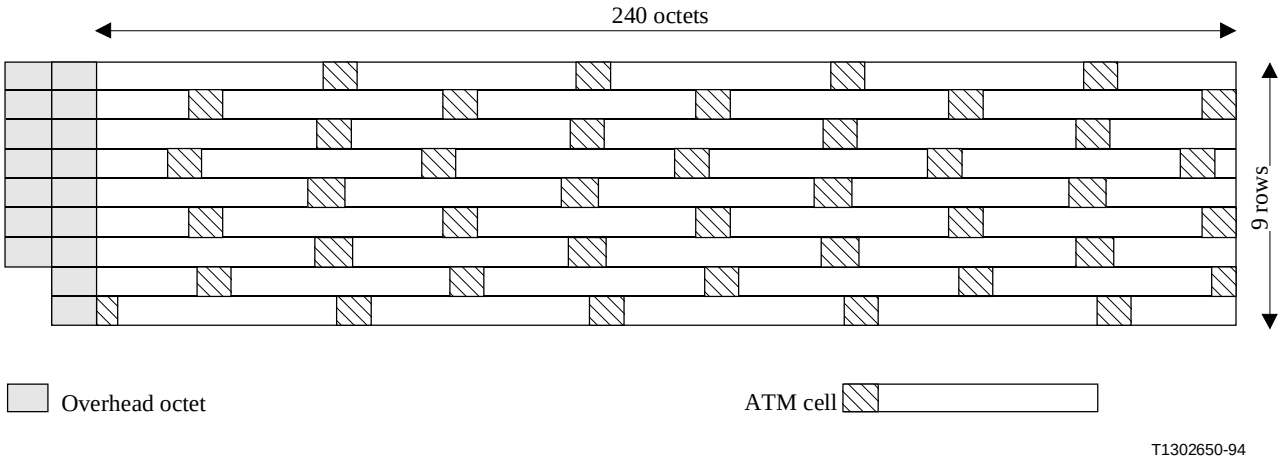

Figure 9-1/G.804 – Frame structure at 139 264 kbit/s

ITU-T RECOMMENDATIONS SERIES

Series A	Organization of the work of the ITU-T
Series B	Means of expression: definitions, symbols, classification
Series C	General telecommunication statistics
Series D	General tariff principles
Series E	Overall network operation, telephone service, service operation and human factors
Series F	Non-telephone telecommunication services
Series G	**Transmission systems and media, digital systems and networks**
Series H	Audiovisual and multimedia systems
Series I	Integrated services digital network
Series J	Transmission of television, sound programme and other multimedia signals
Series K	Protection against interference
Series L	Construction, installation and protection of cables and other elements of outside plant
Series M	TMN and network maintenance: international transmission systems, telephone circuits, telegraphy, facsimile and leased circuits
Series N	Maintenance: international sound programme and television transmission circuits
Series O	Specifications of measuring equipment
Series P	Telephone transmission quality, telephone installations, local line networks
Series Q	Switching and signalling
Series R	Telegraph transmission
Series S	Telegraph services terminal equipment
Series T	Terminals for telematic services
Series U	Telegraph switching
Series V	Data communication over the telephone network
Series X	Data networks and open system communications
Series Y	Global information infrastructure
Series Z	Programming languages