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SERIES V: DATA COMMUNICATION OVER THE TELEPHONE NETWORK

Wideband modems

A 48/56/64 kbit/s data circuit-terminating equipment standardized for use on digital point-to-point leased circuits

ITU-T Recommendation V.38

(Previously CCITT Recommendation)

ITU-T V-SERIES RECOMMENDATIONS

DATA COMMUNICATION OVER THE TELEPHONE NETWORK

1 – General
2 – Interfaces and voiceband modems
3 – **Wideband modems**
4 – Error control
5 – Transmission quality and maintenance
6 – Interworking with other networks

For further details, please refer to ITU-T List of Recommendations.

FOREWORD

The ITU-T (Telecommunication Standardization Sector) is a permanent organ of the International Telecommunication Union (ITU). The ITU-T is responsible for studying technical, operating and tariff questions and issuing Recommendations on them with a view to standardizing telecommunications on a worldwide basis.

The World Telecommunication Standardization Conference (WTSC), which meets every four years, establishes the topics for study by the ITU-T Study Groups which, in their turn, produce Recommendations on these topics.

The approval of Recommendations by the Members of the ITU-T is covered by the procedure laid down in WTSC Resolution No. 1 (Helsinki, March 1-12, 1993).

ITU-T Recommendation V.38, was prepared by ITU-T Study Group 14 (1993-1996) and was approved by the WTSC (Geneva, October 9-18, 1996).

NOTE

1. In this Recommendation, the expression "Administration" is used for conciseness to indicate both a telecommunication administration and a recognized operating agency.

2. The status of annexes and appendices attached to the Series V Recommendations should be interpreted as follows:

- an *annex* to a Recommendation forms an integral part of the Recommendation;
- an *appendix* to a Recommendation does not form part of the Recommendation and only provides some complementary explanation or information specific to that Recommendation.

CONTENTS

Recommendation V.38

A 48/56/64 kbit/s DATA CIRCUIT-TERMINATING EQUIPMENT STANDARDIZED FOR USE ON DIGITAL POINT-TO-POINT LEASED CIRCUITS

(revised in 1996)

1 Introduction

This DCE is intended for use on 56-kbit/s and 64-kbit/s digital point-to-point leased circuits other than ISDN. The DCE is specified herein in terms of the DTE-to-DCE interface(s) and features including rate adaptation, end-to-end signalling, testing and multiplexing facilities. The line signal and the signalling rate that is used to connect this type of DCE locally to a 64-kbit/s digital bearer circuit is considered to be a national matter, and is hence not specified herein. The transmission scheme chosen should, however, be capable of providing an octet timing recovery where a rate adaptation as specified in clause 5 is employed. An octet timing may also become necessary where a rate adaptation of data signalling rates below 48 kbit/s is accomplished (see Appendix III).

The principal characteristics of the DCE are as follows:

a) duplex mode of operation on digital leased circuits (see Note 1);

b) gross bit rates of at least 56 kbit/s;

c) signalling rates up to 56/64 kbit/s;

d) rate adaptation of 48 kbit/s and 56 kbit/s into 64 kbit/s according to schemes specified in Recommendation V.110;

e) inclusion of two different types of DTE-DCE functional interfaces;

f) inclusion of testing facilities;

g) optional provision of a means to differentiate between user and network data;

h) optional inclusion of a multiplexer (for further study);

i) optional inclusion of an equipment management function.

NOTE 1 – The implementation of an optional half-duplex mode of operation is for further study.

NOTE 2 – Figure I.1 gives a schematic block diagram of the arrangement of functional blocks (without the multiplexer function) inside the DCE.

NOTE 3 – The term “line signalling rate” as used in the context of this Recommendation refers to the signalling rate at the input of the transmitter of the transmission unit (see Figure I.1).

2 Signalling rates

2.1 Data signalling rates

The recommended data signalling rates (user rates) are synchronous at 48 kbit/s, 56 kbit/s and 64 kbit/s. For certain national applications or upon bilateral agreement between Administrations, also other data signalling rates below 48 kbit/s are applicable (see Appendix III).

2.2 Signalling rates on line

Where the data signalling rate is 48 kbit/s or 56 kbit/s, a rate adaptation to 64 kbit/s as specified in clause 5 shall be performed at the connection to an international 64-kbit/s bearer circuit. The precise location where this adaptation takes place is a national matter.

NOTE – It should be noted that in some networks the provision of an octet timing may become necessary at the transition from transmission at 56 kbit/s to transmission at 64 kbit/s. Details are outside the scope of this Recommendation, and may be associated with the line signal transmission equipment used. However, a schematic possible scenario is depicted in Figure II.1.

3 Differentiation between user and network data signals

In some cases it may be desirable to provide a means of differentiating between user and network data (e.g. fault detection). The following optional scrambler is provided as a means of accomplishing this differentiation.

NOTE – The potential provision of a scrambler/descrambler inside the transmission unit of the DCE (see Figure I.1) is a national matter, and outside the scope of this Recommendation.

3.1 Scrambler (64 kbit/s only)

Optionally and on bilateral agreement of the Administrations concerned, a self-synchronizing scrambler having the generating polynomial $1 + x^{-18} + x^{-23}$ may be included in the transmitter of the DCE.

The message data sequence applied to the scrambler shall be effectively divided by the generating polynomial. The coefficients of the quotients of this division, taken in descending order, form the data sequence which shall appear at the output of the scrambler. The scrambler data output sequence thus shall be:

$$D_s = D_i \oplus D_s \bullet x^{-18} \oplus D_s \bullet x^{-23}$$

where:

D_s is the data sequence at the output of the scrambler

D_i is the data sequence applied to the scrambler

D_o is the data sequence at the output of the descrambler (see 3.2)

$\oplus$ denotes modulo 2 addition

$\bullet$ denotes binary multiplication

Figure 1 shows a suitable implementation.

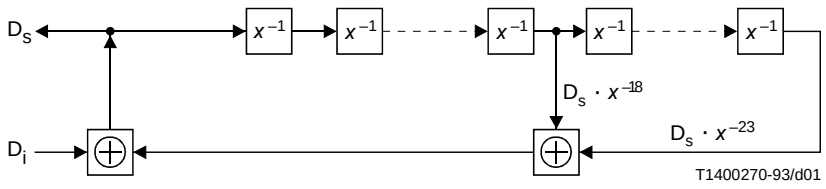


FIGURE 1/V.38

Scrambler

3.2 Descrambler (64 kbit/s only)

Where the optional scrambler specified in 3.1 is provided, also a self synchronizing descrambler having the polynomial $1 + x^{-18} + x^{-23}$ shall be provided in the receiver of the DCE. The message data sequence output by the receiver of the transmission unit (see Figure I.1) shall be effectively multiplied by the generating polynomial $1 + x^{-18} + x^{-23}$ to form the descrambled message. The coefficients of the recovered message sequence taken in descending order form the output data sequence D_o, which is given by:

$$D_o = D_s (1 \oplus x^{-18} \oplus x^{-23})$$

where the notation is defined in 3.1.

Figure 2 shows a suitable implementation.

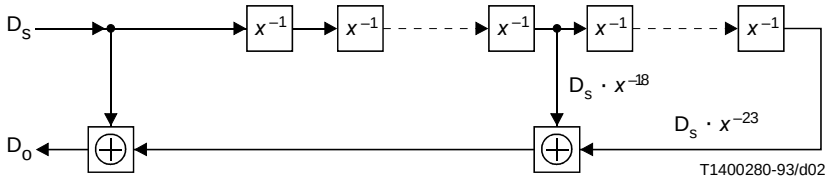


FIGURE 2/V.38

Descrambler

4 Interfaces

One or both types of two functional interfaces shall be provided in the DCE, as specified below. It shall be possible that two DCEs in accordance with this Recommendation can interoperate, where in these DCEs the opposite types of interfaces are employed.

4.1 V.24-type interface

4.1.1 List of interchange circuits

The interchange circuits shall be as in Table 1.

4.1.2 Electrical characteristics

Use of electrical characteristics conforming to Recommendation V.10 and/or V.11 is recommended as specified below, together with the use of the connector and pin assignment plan specified by ISO 4902, ISO/IEC 2110 or ISO/IEC 11569.

i) Concerning circuits 103, 104, 113, 114 and 115, both the generators and the receivers shall be in accordance with Recommendation V.11.

NOTE – In certain instances where V.11 circuits are implemented on both sides of the interface, it may be necessary to add either serial impedance matching resistors or parallel cable terminating resistors as specified in Recommendation V.11 to ensure proper operation of the interchange circuits.

ii) In the case of circuits 105, 106, 107, 108/2 and 109, generators shall comply with Recommendation V.10 or alternatively Recommendation V.11. The receivers shall comply with Recommendation V.10, category 1 or V.11 without termination.

iii) In the case of all other circuits, Recommendation V.10 applies with receivers configured as specified by Recommendation V.10 for category 2.

4.1.3 Operational requirements

The normal operation for this DCE is constant carrier, i.e. the condition of circuit 105 has no influence upon the line signal and upon remote circuit 109. The implementation of an optional half-duplex mode of operation is for further study.

Circuit 106 will follow OFF to ON or ON to OFF transitions on circuit 105 within 0.5 to 3.5 ms (this value is for further study). This time is from the application of an ON or OFF condition on circuit 105.

Optionally, the DCE may provide an end-to-end signalling of local circuit 105 to remote circuit 109. The method used could be as described in Recommendation V.13. Other methods are for further study.

Where, depending on the data signalling rate and the line signalling rate a rate adaptation as specified in clause 5 is employed, both circuits 106 and 109 shall be held in the OFF condition in the event of loss of frame synchronization.

Where the optional scrambler/descrambler function specified in clause 3 is provided, circuit 109 shall be switched to the OFF condition upon the reception of 256 consecutive bits in the binary ONE condition.

The criteria for the control of circuit 109 depending upon a received line signal or other out-of-service codes are a national matter, and are outside the scope of this Recommendation.

TABLE 1/V.38

V.24-type interface

Interchange circuit		NOTES
102	Signal ground or common return	
102a	DTE common return	(Note 1)
102b	DCE common return	(Note 1)
103	Transmitted data	
104	Received data	
105	Request to send	(Note 2)
106	Ready for sending	
107	Data set ready	
108/2	Data terminal ready	(Note 3)
109	Data channel received line signal detector	
113	Transmitter signal element timing (DTE source)	(Note 4)
114	Transmitter signal element timing (DCE source)	
115	Receiver signal element timing (DCE source)	
140	Loopback/Maintenance test	
141	Local loopback	
142	Test indicator	

NOTE 1 – Interchange circuits 102a and 102b are required where the electrical characteristics defined in Recommendation V.10 are used.

NOTE 2 – It shall be possible to apply a permanent ON condition on this circuit inside the DCE.

NOTE 3 – Optional.

NOTE 4 – The use of circuit 113 is for further study, since its application is restricted by the synchronous nature of the network.

4.2 X.24-type interface

4.2.1 List of interchange circuits

The interchange circuits for this interface shall be as in Table 2.

4.2.2 Electrical characteristics

Use of electrical characteristics conforming to Recommendation V.10 and/or V.11 is recommended as specified below, together with the use of the connector and pin assignment plan specified by ISO 4903.

i) Concerning circuits R, S, T and X both the generators and the receivers shall be in accordance with Recommendation V.11.

NOTE – In certain instances where V.11 circuits are implemented on both sides of the interface, it may be necessary to add either serial impedance matching resistors or parallel cable terminating resistors as specified in Recommendation V.11 to ensure proper operation of the interchange circuits.

ii) Concerning circuits C and I, generators shall comply with Recommendation V.10 or alternatively V.11. The receivers shall comply with Recommendation V.10, category 1, or Recommendation V.11 without termination.

4.2.3 Operational requirements

No end-to-end signalling of circuit C to remote circuit I is provided with this type of DCE. Instead, local circuit I shall be in the OFF condition when local circuit C is in the OFF condition.

TABLE 2/V.38

X.24-type interface

Interchange circuit		NOTES
G	Signal ground or common return	(Note 1)
G_a	DTE common return	
T	Transmit	
R	Receive	
C	Control	
I	Indication	
S	Signal element timing	(Note 2)
X	DTE signal element timing	(Note 3)
B	Byte timing	(Notes 4, 5 and 6)

NOTE 1 – This conductor may be used to reduce environmental signal interference at the interface. In the case of shielded interconnecting cable, the additional connection considerations are part of Recommendation X.24 and of ISO 4903.

NOTE 2 – Timing for continuous isochronous data transmission shall be provided.

NOTE 3 – The use and termination of this circuit by the DCE is a national matter, the use being restricted by the synchronous nature of the network.

NOTE 4 – The inclusion of this interchange circuit is optional.

NOTE 5 – It should be noted that this interchange circuit is allocated to the same pole on the connector specified in ISO 4903 as circuit X.

NOTE 6 – The means of providing the byte timing information are a national matter and outside the scope of this Recommendation.

A *DCE not ready* signal (r = 0, i = OFF) shall be output at the interface:

- in the event of a loss of frame synchronization where, depending on the data signalling rate and the line signalling rate, a rate adaptation as specified in clause 5 is employed;
- upon the reception of 256 consecutive bits in the binary ONE condition where the optional scrambler/descrambler function specified in clause 3 is provided.

The DTE should be prepared to receive garbled signals or contiguous binary 1 on circuit R with i = ON, prior to this *DCE not ready* signal.

The criteria for the control of the interface depending on a received line signal are a national matter, and are outside the scope of this Recommendation.

5 Rate adaptation

The bit rate adaptation for 48 kbit/s shall be as specified in Table 7a/V.110. For national connections, rate adaptation of 48 kbit/s in accordance with Recommendation X.50 *bis* may continue to be used as an alternative.

The rate adaptation of 56 kbit/s shall be as specified in Table 7b/V.110. For national connections, rate adaptation in accordance with Table 7c/ V.110 may be used as an alternative.

The precise location where the rate adaptation *in accordance with the schemes specified above* takes place is a national matter. In some national networks, transmission to the international gateway may be at 56 kbit/s or other line signalling rates *or may apply a different adaptation scheme*, and rate adaptation *in accordance with the schemes specified above* may *first* be accomplished at the international gateway.

Where the line signalling rate is 56 kbit/s, no adaptation of a data signalling rate of 48 kbit/s is provided.

6 Testing facilities

While it is recognized that the primary means of fault detection/isolation on digital facilities will be accomplished by the network providers through in-service monitoring, the following testing facilities are specified for the case where user initiated fault isolation is desired. The use of the procedure specified in Recommendation V.54 is provided, other methods for providing fault isolation are for further study.

6.1 Test loops

As in Recommendation V.54, the DCEs are referred to hereafter as DCE A and DCE B.

Test loops 2 for the V.24-type interface case, and 2b for the X.24-type interface case, shall be provided. Test loop 3 shall be provided for the V.24-type interface, and one of the test loops 3a or 3b for the X.24-type interface. The precise location of these type-3 loops is beyond the scope of this Recommendation.

The definitions of these test loops are as described in Recommendations V.54 and X.150, respectively. Operation and signalling at the DTE-DCE interfaces of DCE A and DCE B shall be as specified in Recommendations V.54 and X.21, respectively.

6.1.1 Instigation of remote loop 2/2b

The control of loop 2 (loop 2b respectively) shall utilize the preparation and termination phases as specified in Recommendation V.54.

NOTE – Clauses 5, 6 and 7 of Recommendation V.54 describe the automatic control with synchronous DCEs for simple multipoint circuits, point-to-point duplex circuits and tandem circuits. Only the point-to-point duplex circuit case is applicable where in the DCE the X.24-type interface is employed. Application of the two other configurations with the X.24-type interface is for further study.

The instruction of a DCE (DCE A) to instigate a remote loop 2/2b may be manual or automatic. The automatic case shall be upon the recognition of an OFF-to-ON transition on circuit 140 (in the case of the V.24-type interface) or upon the recognition of a *Send loop 2* command (state L21, c = OFF, t = 0011) (in the case of the X.24-type interface).

This means, irrespective of the type of interface employed, scrambling of a binary 0 with the polynomial $1 + x^{-4} + x^{-7}$ and transmitting it as though it was introduced to the DCE via circuit 103 or circuit T, respectively.

6.1.2 Instigation of the type-3 loop

The instruction of a DCE to instigate a type-3 loop may be manual or automatic. The automatic case shall be upon the recognition of an OFF-to-ON transition on circuit 141 (in the case of the V.24-type interface) or upon the recognition of a *Send loop 3* command (state L31, c = OFF, t = 00001111) (in the case of the X.24-type interface).

6.2 Self tests

The provision of the self-test function specified herein is optional.

The tests described hereafter (in 6.2.1 and 6.2.2) employ an internally generated data pattern that is typically controlled by a switch on the DCE. It shall be possible to perform these tests with or without the DCE being connected to a DTE.

Upon activation of the self-test function, an internally generated data pattern at the selected user signalling rate shall be transmitted as though it was introduced to the DCE via circuit 103 or circuit T, respectively (see Figure I.1). An error detector, capable of identifying errors in the test pattern, shall be connected to the received data path. How the presence of errors is indicated is beyond the scope of this Recommendation.

NOTE – The test pattern has no end-to-end bearing. Its specification is therefore not part of this Recommendation. Examples for test patterns may be alternative binary ONEs and ZEROs (reversals) or the 511-bit test pattern in accordance with Recommendation O.153.

During any self-test mode, interchange circuits 103, 105 and 108/2 (where provided) at the V.24-type interface, and interchange circuits T and C at the X.24-type interface, shall be ignored.

At the V.24-type interface, all generating interchange circuits except 114 (if used), 115 and 142 shall be clamped to the binary 1 or OFF condition. If circuit 113 is used, the DCE shall disregard this interchange circuit and shall use its internal clock.

At the X.24-type interface, the DCE shall signal state *DCE not ready* (r = 0, i = OFF) to the DTE. If circuit X is used, the DCE shall disregard this interchange circuit and shall use its internal clock.

6.2.1 Self test with the type-3 loop

The type-3 loop as defined in Recommendations V.54 and X.150, respectively, shall be activated in the DCE. The self-test function shall be activated, and the DCE operation shall be as described in 6.2.

6.2.2 Self test with remote loop 2/2b

The DCE shall be conditioned to instigate a 2/2b at the remote DCE as specified in 6.1.1. The self-test function shall be activated, and the DCE operation shall be as described in 6.2.

7 Multiplexing

A multiplexing option may be included to combine subchannels into a single aggregate bit stream for transmission. The method for the identification of the individual data subchannels is for further study.

8 Internal management

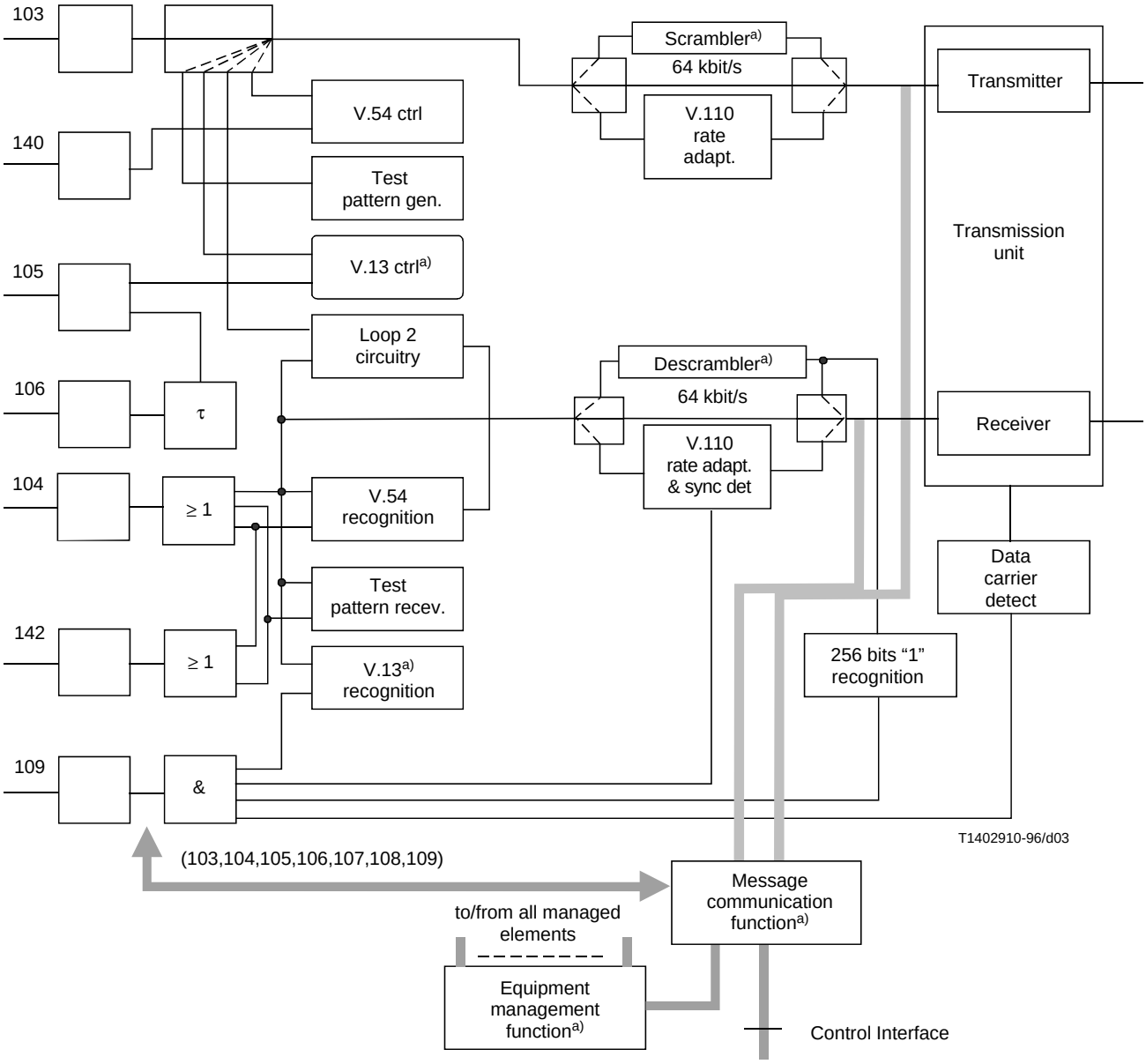
Optionally, internal management functions may be provided. That concerns as examples initialization of the DCE, adjustment of part or all configurable parameters within the DCE. Access to these functions may be done via various means (e.g. front panel menu, DTE-DCE interface, dedicated control interface in local operation mode or via a PSTN/ISDN connection). The corresponding requirements are beyond the scope of the Recommendation.

Appendix I

Functional block diagram

Figure I.1 gives an example for a simplified functional block diagram of a DCE in accordance with this Recommendation, that contains all functional blocks specified in the main part of this Recommendation. For this example it was assumed that the DCE would be capable of transmitting at 64 kbit/s and of converting user data rates of 48 kbit/s and 56 kbit/s to this data signalling rate.

The transmission unit contains all functions of a (typically baseband) transmitter and a receiver, which are necessary to interface the DCE to the cable plant of the respective national network. Details are a national matter. For this example it was assumed that the transmission unit is inside the DCE, and interworks with a transmission unit which is installed at the other end of the local loop (see also Appendix II).



[a)] Optional.

FIGURE I.1/V.38

An example for a simplified functional block diagram

Appendix II

Connection schematic

Figure II.1 provides an example of a 56-kbit/s digital leased circuit between two countries, where 56 kbit/s and 64 kbit/s, respectively, user signalling rates are employed.

DCE B does not conform to this Recommendation.

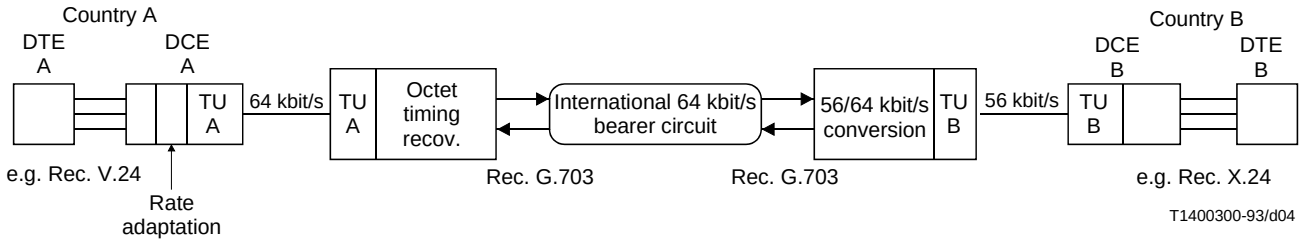


FIGURE II.1/V.38

Appendix III

Rate adaptation of data signalling rates below 48 kbit/s

The following information is provided as an example where it is intended to utilize the DCE specified in the main part of this Recommendation for user signalling rates below 48 kbit/s (without subrate multiplexing). Alternative adaptation schemes may also be used in some countries.

III.1 Data signalling rates

In addition to the data signalling rates specified in the main part of this Recommendation, the following data signalling rates may be provided at the DTE-DCE interface:

- 2400 bit/s;
- 4800 bit/s;
- 9600 bit/s;
- 19 200 bit/s.

III.2 Rate adaptation

The rate adaptation should be accomplished as specified in Recommendation V.110. The following tables shall be applied for the data signalling rates of the incoming signal:

- 2400 bit/s: Table 6c/V.110;
- 4800 bit/s: Table 6e/V.110;
- 9600 bit/s: Table 6e/V.110;
- 19 200 bit/s: Table 6e/V.110.

III.3 Interfaces

III.3.1 Interchange circuits

The V.24/V.28-type interface shall be provided in the DCE. The interchange circuits shall be as in Table 1.

III.3.2 Operational requirements

Optionally, the DCE may provide an end-to-end signalling of local circuit 105 to remote circuit 109. The SB group of S bits as specified in 2.1.2.3/V.110 shall be used to convey the conditions of circuits 105/109.

Optionally, the DCE may provide an end-to-end signalling of local circuit 108/2 to remote circuit 107. The SA group of S bits as specified in 2.1.2.3/V.110 shall be used to convey the condition of circuit 108/2 to circuit 107.

In the event of loss of frame synchronization, both circuits 106 and 109 shall be held in the OFF condition. The requirements specified in 4.1.5, item e/V.110) do not apply.

III.3.3 Testing facilities

Integration of loop 2

The E4 bit as specified in 2.1.2.3/V.110 shall be used to convey the condition of circuit 140. The remote DCE, upon recognition of status bit E4, will establish loop 2 and turn status E5 bit to the ON condition (binary ZERO) in the transmitted frame. The local DCE, upon recognition of status E5 bit being in the ON condition will switch on a visual indicator.

The control of circuits 107 and 142 shall be as described in Table 2/V.54.

Appendix IV

Example of implementation of the transmission unit

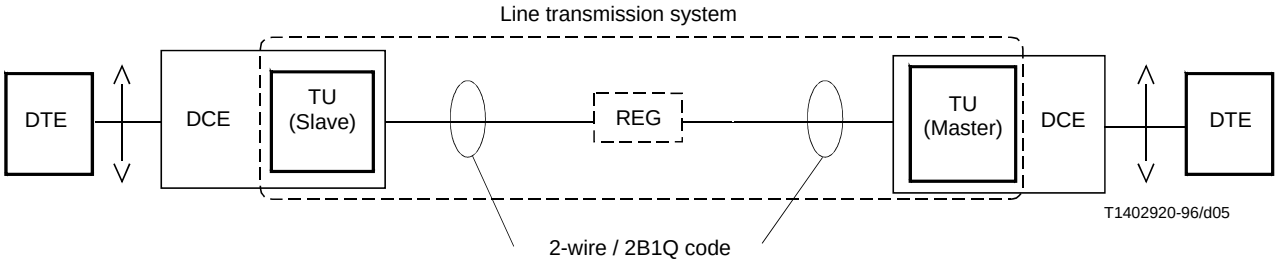
IV.1 General

This Appendix describes functional characteristics of an implementation of a transmission unit as shown in Figure IV.1.

The objectives with this transmission unit are to operate on 2-wire metallic lines that meet minimum ISDN requirements and to use existing components designed for ISDN basic access line transmission system.

The information contained herein is informative and alternative systems may be implemented. The description of these systems requires further study.

IV.2 Physical model of the line transmission system



TU Transmission Unit
REG Regenerator (optional)

FIGURE IV.1/V.38

Physical model of the line transmission system

IV.3 Functional description of the DCE

DCE characteristics (DTE/DCE interface, bit-rate adaptation, end-to-end control or signalling, testing facilities) are specified in the main part to this Recommendation. See Figure IV.2.

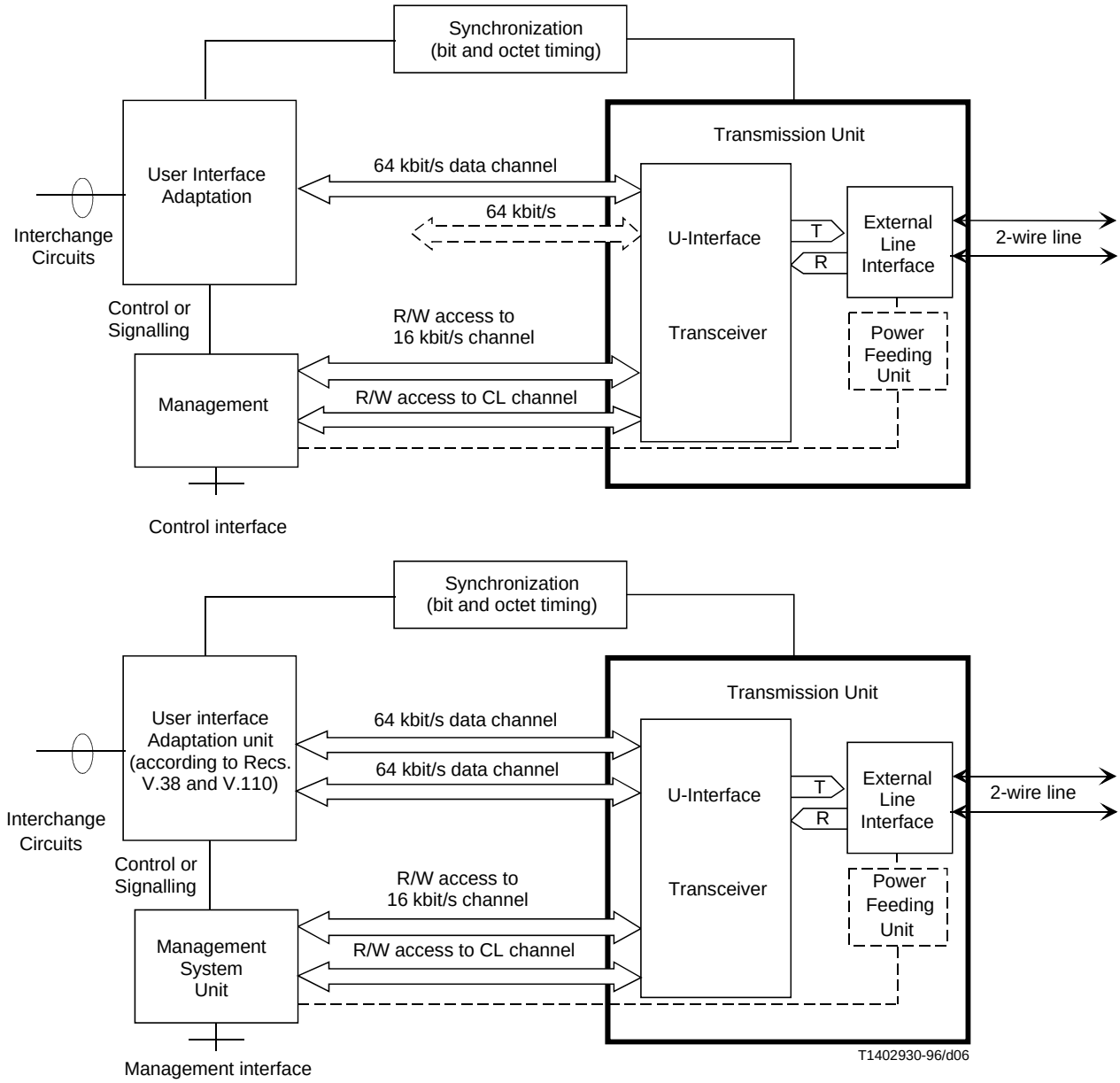


FIGURE IV.2/V.38

Functional block diagram of the DCE

IV.4 Functions of TU functional block

Transmission unit incorporated within the DCE (see Figure IV.1) interwork with a remote transmission unit at the other end of the local loop that is part of the baseband line termination integrated within the DCE (see Figure IV.1).

Operation of both units is not symmetrical. One is configured to operate in the master mode and the other configured to operate in the slave mode. TU acting in master mode is selected when installing the line transmission system (configurable parameter).

TU working in slave mode provides the different NT1 functions. TU working in master mode provides LT functions. NT1 and LT functions are referring to Recommendation G.961. Refer also to Figure IV.3

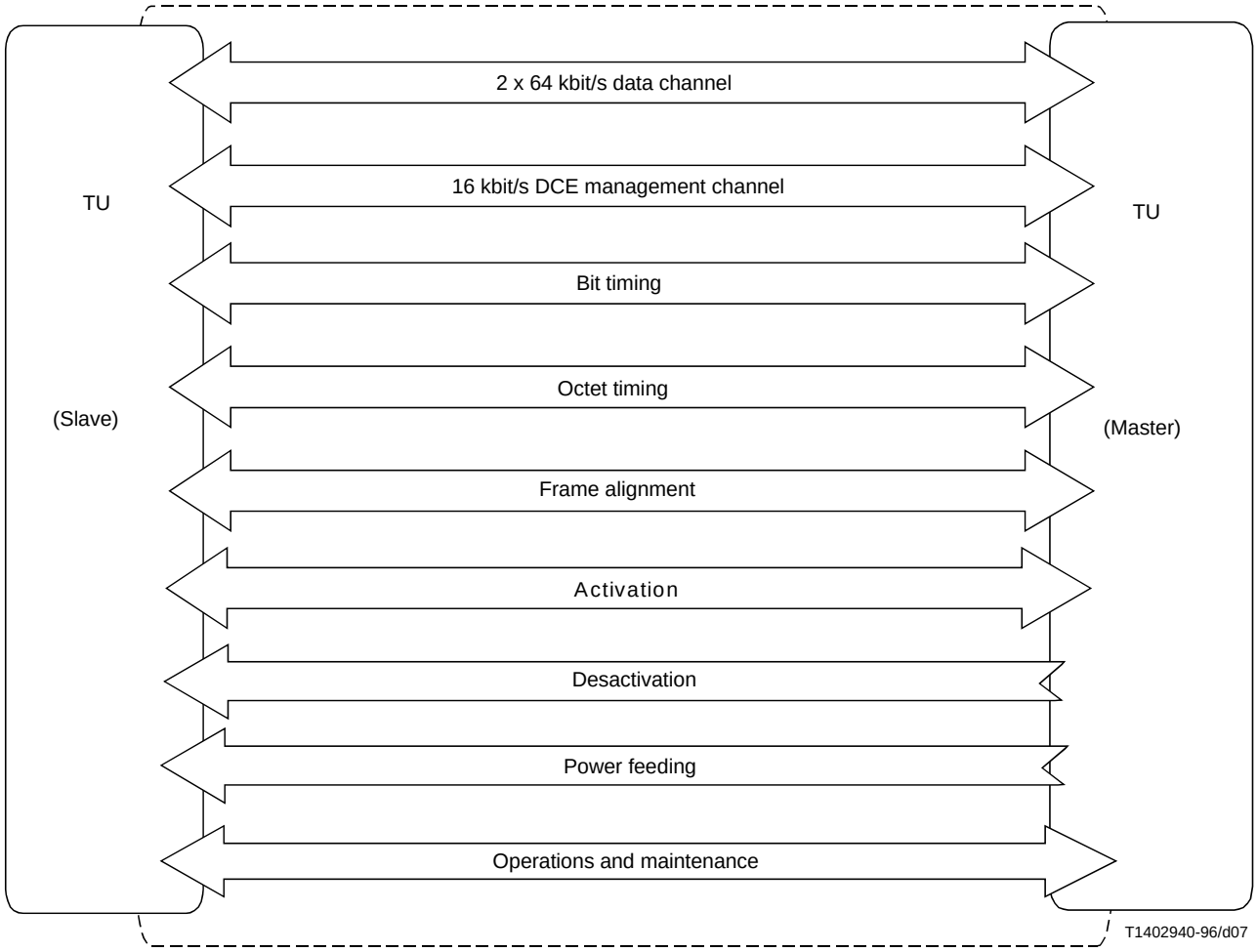


FIGURE IV.3/V.38

Functions of TU functional blocks

IV.4.1 Data channels

This function may provide two bidirectional and independent 64 kbit/s data channels. These correspond to the two B-channels in ISDN basic access signals. For the purpose of this Recommendation, only one 64 kbit/s is used and should correspond to the first B-channel in the ISDN application.

IV.4.2 DCE management channel

This function provides a 16 kbit/s bidirectional channel for the remote management of the DCE. This corresponds to the D-channel in ISDN basic access signals.

When the 16 kbit/s channel is not allocated to the transmission of management information, the use of the eoc (defined in IV.5.7.1) should be alternatively used for the remote management of the DCE.

IV.4.3 Bit timing

This function provides bit timing to enable the TU to recover information from the aggregate stream. Bit timing for direction slave TU to master TU shall be derived from clock received by slave TU from the master TU.

IV.4.4 Octet timing

This function provides 8 kHz octet timing for the 64 kbit/s data channels. It shall be derived from the frame alignment.

IV.4.5 Frame alignment

This function enables TU to recover time division multiplexed channels.

IV.4.6 Activation

This function restores the line transmission system between two TU functional blocks to its normal operational status. At the end of activation procedure, transparency of data and 16 kbit/s management or data channel is achieved; it is not necessary for DTE to be connected during this procedure. It is suggested that only the master TU initiates the activation procedure.

In normal operation, the line transmission system is always activated.

IV.4.7 Deactivation

This procedure is only permitted to master TU. This procedure is initiated by master TU before initiating testing loops in slave TU (and regenerator if required).

IV.4.8 Power feeding

The power feeding of the TU is handled locally by the DCE. In case of power failure a battery is provided to permit a restricted function and to indicate fault conditions to the distant unit.

The regenerator (if required) shall be locally power fed.

Optionally remote power feeding of the regenerator and of the TU function in the DCE may be provided by the master DCE. Remote power feeding of the other DCE functions (user interface adaptation, management system, etc.) is not required.

IV.4.9 Maintenance

The functions needed for operations and maintenance of the transmission system – including the TU and one regenerator (if required) – and for activation/deactivation procedures are combined in one transport resource available in the line signals along with the 64 kbit/s data and 16 kbit/s management channels. This transport resource is named the CL channel.

The following functions are provided by the CL channel:

- maintenance command (loopback control in the TU functional block or in the regenerator);
- maintenance information;
- indication of fault conditions;
- information regarding power feeding in the slave TU.

IV.5 Requirements for a line transmission system using 2B1Q line code

IV.5.1 Line code

The line code is 2B1Q (2 binary, 1 quaternary). This is a 4-level code and it is used without redundancy. This code is described in Appendix II/G.961.

The aggregate bit stream entering the TU functional block before transmission (2 x 64 kbit/s channel, 16 kbit/s management or data channel, CL channel) is grouped into pairs of bits for conversion into quaternary symbols called quats. The 64 kbit/s data channels and the 16 kbit/s management or data channel are scrambled before coding.

M1 through M6 bits of the CL channel are also paired, coded and scrambled the same way. The relationship of the bits in the 64 kbit/s data channels and 16 kbit/s management or data channel to quats are shown in Figure IV.4.

For reasons of convenience the 64 kbit/s data channels and the 16 kbit/s management channel are presented as B1-, B2- and D-channels respectively in Figure IV.4.

	time ----->								
data	B1 (64 kbit/s data channel)				B2 (64 kbit/s data channel)				D (16 kbit/s channel)
pair of bits	b11 b12	b13 b14	b15 b16	b17 b18	b21 b22	b23 b24	b25 b26	b27 b28	d1 d2
quat	q1	q2	q3	q4	q5	q6	q7	q8	q9
bits	8				8				2
quats	4				4				1

B1 64 kbit/s data channel

B2 64 kbit/s data channel

D 16 kbit/s management or data channel

b11 first bit of B1 octet as received by TU

b18 last bit of B1 octet as received by TU

b21 first bit of B2 as received by TU

b28 last bit of B2 octet as received by TU

d1d2 consecutive 16 kbit/s management channel

qi i^{th} quat relative to start of a given 18 bit 2B+D data field

FIGURE IV.4/V.38

2B1Q bit encoding for 64 kbit/s data and 16 kbit/s management channels

IV.5.2 Line modulation rate

The gross bit rate is 160 kbit/s; 144 kbit/s are occupied by the data channels and the 16 kbit/s management channel and the CL channel presents a bit rate of 4 kbit/s. The remaining 12 kbit/s are used for frame alignment word. The line symbol rate (modulation rate) is 80 kbauds.

IV.5.3 Clock tolerance

Clock tolerance of the free running TU clock is ±50 ppm.

IV.5.4 Frame structure

A frame shall be of 120 quaternary symbols transmitted within a nominally 1.5 ms interval. Each frame contains a frame word, data and/or management channel bits and CL channel bits.

IV.5.5 Frame and multiframe word

The Frame Word (FW) is used to allocate bit positions to the data, management channel and CL channels.

The code for the frame word in all frames except the first in a multiframe is:

FW = + 3 + 3 –3 –3 –3 + 3 –3 + 3 + 3

The code for the first word of the first frame of a multiframe is the Inverted Frame Word (IFW):

IFW = –3 –3 + 3 + 3 + 3 –3 + 3 –3 –3

The frame and multiframe words are the same for both directions.

IV.5.6 Frame offset between slave TU and master TU

The slave TU synchronizes transmitted frames with received frames from the master TU. Transmitted frames are offset with respect to received frames by 60 ± 2 quaternary symbols (i.e. about 0.75 ms).

IV.5.7 CL channel

IV.5.7.1 Structure of the CL channel

The CL channel consists of the last three symbols (6 bits) in each basic frame of the multiframe; 48 bits of a multiframe are used for the CL channel.

The bit rate for the CL channel is 4 kbit/s:

- 24 bits per multiframe (2 kbit/s) are allocated to an embedded operation channel (eoc) which supports operations communications needs between the TU;
- 12 bits per multiframe (1 kbit/s) are allocated to a Cyclic Redundancy Check (CRC) function;
- 12 bits per multiframe (1 kbit/s) are allocated to other functions as shown in Figure IV.5.

IV.5.7.2 Functions of the CL channel

Functions of the CL channel listed below are based on bit allocation for the multiframe defined in Figure IV.5:

- Error monitoring function (crc bits).
- Far-end block error (febe bit).
- Activation (act).
- Deactivation (dea).
- Power status of slave TU (ps1, ps2).
- Slave TU test mode indicator (ntm); its use is optional. It may be used by slave TU to indicate that a maintenance action has been locally initiated by the corresponding DTE.
- Alarm indicator bit (aib); its use is optional. It can be used by master TU to indicate a failure of intermediate transmission system.
- Embedded operation channel functions (eoc). Functions provided are essentially 144 kbit/s signal (2B+D) loopbacks, 64 kbit/s signals (B1 and B2) loopbacks in slave TU (type 2 loopback) or in regenerator (loopback 1A) if required. Only master TU is permitted to control loopbacks by this way.

64 eoc message codes have been reserved for standard applications or for internal network use. Other codes may be used for non-standard applications such as supporting DCE management functions. At least 120 codes are available for this purpose. Any use of such messages shall not interfere with 16 kbit/s management channel when provided.

IV.6 DCE management channel

IV.6.1 Protocol and procedure

Detailed protocol and procedure for the management of DCE are for further study.

IV.6.2 Functions provided

This channel may support end-to-end control or signalling and maintenance information and acknowledgements related to:

- alarm;
- performance;

– state of interchange circuits (105/109, C/I) when an in-band end-to-end control channel in the 64 kbit/s data channel is not provided;
– remote loop 2 command and acknowledgement;
– configuration of the remote DCE connected to the master DCE.

IV.7 Equipment management function

IV.7.1 General

This subclause only considers management aspects in relation with the transmission unit.

The equipment management function monitors the different testing facilities of the transmission unit.

It receives and analyses information coming from the control interface, from the user interface, from the local TU functional block, from the remote TU functional block through the CL channel and from the remote end DCE through the management channel assuming that the intervening network supports this function.

The equipment management function handles the interworking of the DCE functions with the monitoring functions of the line transmission system.

IV.7.2 Specific functions of the equipment management function with TU working in slave mode

Equipment management function:

– manages the procedure of activation for the line transmission system initiated by the master TU;
– generates loopback confirmation.

Optionally, when the equipment management function of a slave TU detects a loop command coming from the control interface or from the interchange circuits of the user interface or from the DCE management channel, it communicates this test mode status to the master TU by setting the ntm bit to value ZERO.

IV.7.3 Specific functions of equipment management function with TU working in master mode

Equipment management function:

– initiates and manages the procedure of activation/deactivation for the line transmission system;
– controls the procedures for the setting of loopbacks in the line transmission system.

When the equipment management function of the master TU has detected a loop command coming from the control interface of the master DCE or from the remote end DCE management channel, it communicates this test mode status to the slave TU by setting the aib bit to the value ZERO.

		Framing	12×(2B+D)	CL channel (bits M1 to M6)					
	quat positions	1-9	10-117	118s	118m	119s	119s	120s	120m
	bit positions	1-18	19-234	235	236	237	238	239	240
Multiframe	Frame	Frame word		M1	M2	M3	M4	M5	M6
		TU Master ----------> TU Slave							
A	1	IFW	12x(2B+D)	eoc_{a1}	eoc_{a2}	eoc_{a3}	act	1	1
	2	FW	12x(2B+D)	eoc_{dm}	eoc_{il}	eoc_{i2}	dea	1	febe
	3	FW	12x(2B+D)	eoc_{i3}	eoc_{i4}	eoc_{i5}	1	crc_1	crc_2
	4	FW	12x(2B+D)	eoc_{i6}	eoc_{i7}	eoc_{i8}	1	crc_3	crc_4
	5	FW	12x(2B+D)	eoc_{a1}	eoc_{a2}	eoc_{a3}	1	crc_5	crc_6
	6	FW	12x(2B+D)	eoc_{dm}	eoc_{il}	eoc_{i2}	1	crc_7	crc_8
	7	FW	12x(2B+D)	eoc_{i3}	eoc_{i4}	eoc_{i5}	uoa	crc_9	crc_{10}
	8	FW	12x(2B+D)	eoc_{i6}	eoc_{i7}	eoc_{i8}	aib	crc_{11}	crc_{12}
B, C...									
		TU Slave ----------> TU Master							
1	1	IFW	12x(2B+D)	eoc_{a1}	eoc_{a2}	eoc_{a3}	act	11	1
	2	FW	12x(2B+D)	eoc_{dm}	eoc_{il}	eoc_{i2}	ps_1	11	febe
	3	FW	12x(2B+D)	eoc_{i3}	eoc_{i4}	eoc_{i5}	ps_2	crc_1	crc_2
	4	FW	12x(2B+D)	eoc_{i6}	eoc_{i7}	eoc_{i8}	ntm	crc_3	crc_4
	5	FW	12x(2B+D)	eoc_{a1}	eoc_{a2}	eoc_{a3}	cso	crc_5	crc_6
	6	FW	12x(2B+D)	eoc_{dm}	eoc_{il}	eoc_{i2}	1	crc_7	crc_8
	7	FW	12x(2B+D)	eoc_{i3}	eoc_{i4}	eoc_{i5}	sai	crc_9	crc_{10}
	8	FW	12x(2B+D)	eoc_{i6}	eoc_{i7}	eoc_{i8}	1*	crc_{11}	crc_{12}
2, 3....									

2B+D	data bits (data and management channels)
quat	any pair of bit forming a quaternary symbol
s	sign bit (first) in a quat
m	magnitude bit (second) in a quat
FW/IFW	frame word/inverted frame word, bits 1-18 in a frame
1	reserved for future definition
1*	reserved for network use (network indicator)
CL	CL channel bits M1 to M6 (bits 235-240 in basic frame structure)
eoc	embedded operation channel
eoc_{ai}	address bits
eoc_{dm}	data/message indicator
eoc_i	information (data or message)
crc_n	Cyclic Redundancy Check procedure (applicable to 2B+D and M4) n most significant bit n+1 following most significant bit, etc.
febe	far-end block error (ZERO for errored multiframe)
ps1 et ps2	power status bits (ZERO indicate power problem)
ntm	test mode bit (ZERO indicate the slave TU test mode)
cso	cold start only bit (optional, set to ZERO if not used)
sai	S/T interface activity indicator (optional, set to ONE if not used)
act	activation bit (set to ONE during activation to indicate readiness for layer 2 communication progress)
dea	deactivation bit (ZERO indicates the Master TU's intention to deactivate)
uoa	U Only Activation (optional, set to ONE to activate user interface)
aib	alarm indication bit (ZERO indicates interruption)

FIGURE IV.5/V.38

2B1Q multiframe technique and bit assignment

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