INTERNATIONAL TELECOMMUNICATION UNION

ITU-T V.27

TELECOMMUNICATION
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OF ITU

DATA COMMUNICATION OVER THE TELEPHONE NETWORK

4800 BITS PER SECOND MODEM WITH MANUAL EQUALIZER STANDARDIZED FOR USE ON LEASED TELEPHONE-TYPE CIRCUITS

ITU-T Recommendation V.27

(Extract from the *Blue Book*)

NOTES

1 ITU-T Recommendation V.27 was published in Fascicle VIII.1 the *Blue Book*. This file is an extract from the *Blue Book*. While the presentation and layout of the text might be slightly different from the *Blue Book* version, the contents of the file are identical to the *Blue Book* version and copyright conditions remain unchanged (see below).

2 In this Recommendation, the expression "Administration" is used for conciseness to indicate both a telecommunication administration and a recognized operating agency.

Recommendation V.27

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(Geneva, 1972; amended at Geneva, 1976 and 1980, Malaga-Torremolinos, 1984)

1 Introduction

This modem is intended to be used primarily on Recommendation M.1020 [1] circuits but this does not preclude the use of this modem over circuits of lower quality at the discretion of the Administration concerned.

On leased circuits, considering that there exist and will come into being many modems with features designed to meet the requirements of the Administrations and users, this Recommendation in no way restricts the use of any other modems.

The principal characteristics for this recommended modem for transmitting data at 4800 bits per second on leased circuits are as follows:

a) it is capable of operating in a full-duplex mode or half-duplex mode;

b) differential eight-phase modulation with synchronous mode of operation;

c) possibility of a backward (supervisory) channel at modulation rates up to 75 bauds in each direction of transmission, the use of these channels being optional;

d) inclusion of a manually adjustable equalizer.

2 Line signals

2.1 The carrier frequency is to be 1800 ± 1 Hz. No separate pilot frequencies are provided. The power levels used will conform to Recommendation V.2.

2.2 *Division of power between the forward and backward channels*

If simultaneous transmission of the forward and backward channels occurs in the same direction, a backward channel should be 6 dB lower in power level than the forward (data) channel.

2.3 The data stream to be transmitted is divided into groups of three consecutive bits (tribits). Each tribit is encoded as a phase change relative to the phase of the immediately preceding signal element (see Table 1/V.27). At the receiver the tribits are decoded and the bits are reassembled in correct order. The left-hand digit of the tribit is the one occurring first in the data stream as it enters the modulator portion of the modem after the scrambler.

3 Data signalling and modulation rates

The data signalling rate shall be 4800 bits per second ± 0.01%, i.e. the modulation rate is 1600 bauds ± 0.01%.

4 Received signal frequency tolerance

The carrier frequency tolerance allowance at the transmitter is ± 1 Hz and assuming a maximum frequency drift of ± 6 Hz in the connection between the modems, then the receiver must be able to accept errors of at least ± 7 Hz in the received frequencies.

5 Backward channel

The modulation rate, characteristic frequencies, tolerances, etc. to be as recommended for backward channel in Recommendation V.23. This does not preclude the use of a higher speed backward channel with operational capability of 75 bauds or higher, bearing the same characteristic frequencies as the V.23 backward channel.

6 Interchange circuits

6.1 *List of essential interchange circuits* (see Table 2/V.27)

TABLE 1/V.27

Tribit values			Phase change (see Note)
0	0	1	0°
0	0	0	45°
0	1	0	90°
0	1	1	135°
1	1	1	180°
1	1	0	225°
1	0	0	270°
1	0	1	315°

Note - The phase change is the actual on-line phase shift in the transition region from the centre of one signalling element to the centre of the following signalling element.

TABLE 2/V.27

Interchange circuit		Forward (data) channel half-duplex of full-duplex (see Note 1)	
No	Designation	Without backward channel	With backward channel
102	Signal ground or common return	X	X
103	Transmitted data	X	X
104	Received data	X	X
105 (see Note 2)	Request to send	X	X
106	Ready for sending	X	X
107	Data set ready	X	X
108/1	Connect data set to line	X	X
109	Data channel received line signal detector	X	X
113	Transmitter signal element timing (DTE source)	X	X
114	Transmitter signal element timing (DCE source)	X	X
115	Receiver signal element timing (DCE source)	X	X
118	Transmitter backward channel data		X
119	Received backward channel data		X
120	Transmit backward channel line signal		X
121	Backward channel ready		X
122	Backward channel received line signal detector		X

Note 1 - All essential interchange circuits and any others which are provided shall comply with the functional and operational requirements of Recommendation V.24. All interchange circuits indicated by X shall be properly terminated in the data terminal equipment and in the data circuit-terminating equipment in accordance with the appropriate Recommendation for electrical characteristics § 6.6).

Note 2 - No essential for 4-wire full-duplex continuous carrier operation.

6.2 *Threshold and response times of circuit 109*

A fall in level of the incoming line signal to -31 dBm or lower for more than 10 ± 5 ms will cause circuit 109 to be turned OFF. An increase in level to -26 ± 1 dBm or higher will turn this circuit ON after a delay of:

a) 13 ± 3 ms for fast operations,

b) 100 ms to 1200 ms for slow operation,

where the choice of the delay for slow operation depends upon the application. Delays within the range of b) may be provided for 4-wire full-duplex continuous carrier operation.

6.3 *Response time for circuit 106*

The time between the OFF to ON transition of circuit 105 and the OFF to ON transition of circuit 106 shall be optionally 20 ± 3 ms or 50 ± 20 ms.

6.4 *Clamping in half-duplex mode*

The DCE, when operating in half-duplex mode on a 2-wire line shall hold, where implemented:

a) circuit 104 in the binary 1 condition and circuit 109 in the OFF condition when circuit 105 is in the ON condition and, where required to protect circuit 104 from false signals, for a period of 150 ± 25 ms following the ON to OFF transition on circuit 105; the use of this additional delay is optional, based on system considerations;

b) circuit 119 in the binary 1 condition and circuit 122 in the OFF condition when circuit 120 is in the ON condition and, where required to protect circuit 119 from false signals, for a time interval following the ON to OFF transition on circuit 120. The specific duration of this time interval is left for further study. The additional delay is optional, based on system considerations.

6.5 *Fault condition of interchange circuits*

(See Recommendation V.28, § 7 for association of the receiver failure detection types.)

6.5.1 The DTE should interpret a fault condition on circuit 107 as an OFF condition using failure detection type 1.

6.5.2 The DCE should interpret a fault condition on circuits 105 and 108 as an OFF condition using failure detection type 1.

6.5.3 All other circuits not referred to above may use failure detection type 0 or 1.

6.6 *Electrical characteristics of interchange circuits*

Use of electrical characteristics conforming to Recommendation V.28 is recommended together with the connector and pin assignment plan specified by ISO 2110.

Note - Manufacturers may wish to note that the long-term objective is to replace electrical characteristics specified in Recommendation V.28, and that Study Group XVII has agreed that the work shall proceed to develop a more efficient, all balanced, interface for the V-Series application which minimizes the number of interchange circuits.

7 Timing arrangements

Clocks should be included in the modem to provide the data terminal equipment with transmitter signal element timing, circuit 114 and receiver signal clement timing, circuit 115. Alternatively, the transmitter signal element timing may be originated in the data terminal equipment and be transferred to the modem via circuit 113.

8 Synchronizing signal

During the interval between the OFF to ON transition of circuit 105 and the OFF to ON transition of circuit 106, synchronizing signals for properly conditioning the receiving modem must be generated by the transmitting modem. These signals are defined as:

a) signals to establish basic demodulator requirements;

b) signals to establish scrambler synchronization.

The actual composition of the synchronization signals is continuous 180 degrees phase reversals on line for 9 ± 1 ms followed by continuous 1s at the input to the transmit scrambler for b). Condition b) shall be sustained until the OFF to ON transition of circuit 106.

9 Line signal characteristics

A 50% raised cosine energy spectrum shaping is equally divided between the receiver and transmitter.

10 Scrambler

A self-synchronizing scrambler/descrambler having the generating polynomial:

$$1 + x^{-6} + x^{-7}$$

with additional guards against repeating patterns of 1, 2, 3, 4, 6, 9 and 12 bits, shall be included in the modem. Appendix I shows a suitable logical arrangement.

At the transmitter the scrambler shall effectively divide the message polynomial, of which the input data sequence represents the coefficients in descending order, by the scrambler generating polynomial, to generate the transmitted sequence, and at the receiver the received polynomial, of which the received data sequence represents the coefficients in descending order, shall be multiplied by the scrambler generating polynomial to recover the message sequence.

The detailed scrambling and descrambling processes are described in Appendix I.

11 Equalizer

A manually adjustable equalizer with the capability of compensating for the amplitude and group delay distortion within the limits of Recommendation M.1020 [1] shall be provided in the receiver. The transmitter shall be able to send an equalization pattern while the receiver shall incorporate a means of indicating correct adjustment of the equalizer controls. The equalizer pattern is generated by applying continuous 1s to the input of the transmitter scrambler defined above.

12 Alternative equalization and scrambler techniques

This Recommendation does not preclude the use of alternative equalization techniques, for example manually adjustable transmit equalizers for use in multipoint polled networks and for point-to-point networks with an unattended location.

These techniques, and their incorporation in the modem, and a new scrambler, should be the subject of further study.

Note - For modems with automatic adaptive equalizers, see Recommendation V.27 *bis.*

13 The following information is provided to assist equipment manufacturers:

- the data modem should have no adjustment for send level or receive sensitivity under the control of the operator;
- no fall-back rate has been included because the convenient rate would be 3200 bit/s, not a permitted rate;
- circuit 108/2 has not been included in the list of interchange circuits because it was considered that the modem would not be suitable for switched network use until an automatic equalizer had been recommended.

APPENDIX I

(to Recommendation V.27)

Detailed scrambling and descrambling processes

I.1 *Scrambling*

The message polynomial is divided by the generating polynomial $1 + x^{-6} + x^{-7}$. (See Figure I-1/V.27.) The coefficients of the quotient of this division are taken in descending order from the data sequence to be transmitted.

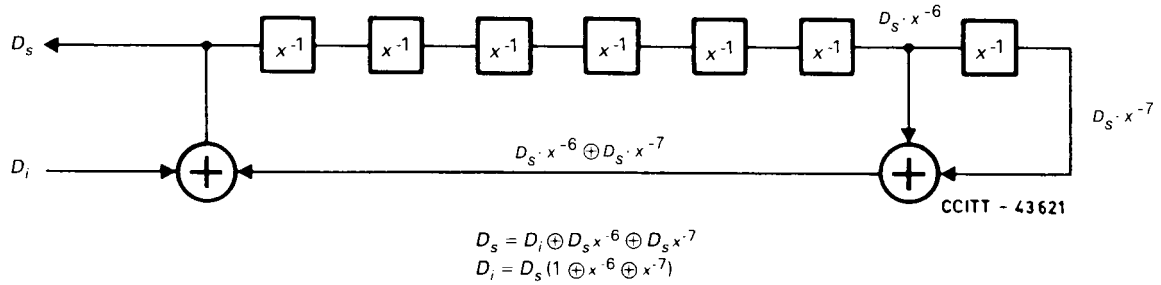
The transmitted bit sequence is continuously searched over a span of 45 bits for sequences of the form

$$p(x) = \sum_{i=0}^{32} a_i x^i$$

where

$a_i = 1$ or 0 and $a_i = a_{i+9}$ or a_{i+12}

If such a sequence occurs, the bit immediately following the sequence is inverted before transmission.



$D_s = D_i \oplus D_s x^{-6} \oplus D_s x^{-7}$
$D_i = D_s (1 \oplus x^{-6} \oplus x^{-7})$

FIGURE I-1/V.27

I.2 *Descrambling*

At the receiver the incoming bit sequence is continuously searched over a span of 45 bits for sequences of the form *p(x)*. If such a sequence occurs, the bit immediately following the sequence is inverted. The polynomial represented by the resultant sequence is then multiplied by the generating polynomial $1 + x^{-6} + x^{-7}$ to form the recovered message polynomial. The coefficients of the recovered polynomial, taken in descending order, form the output data sequence.

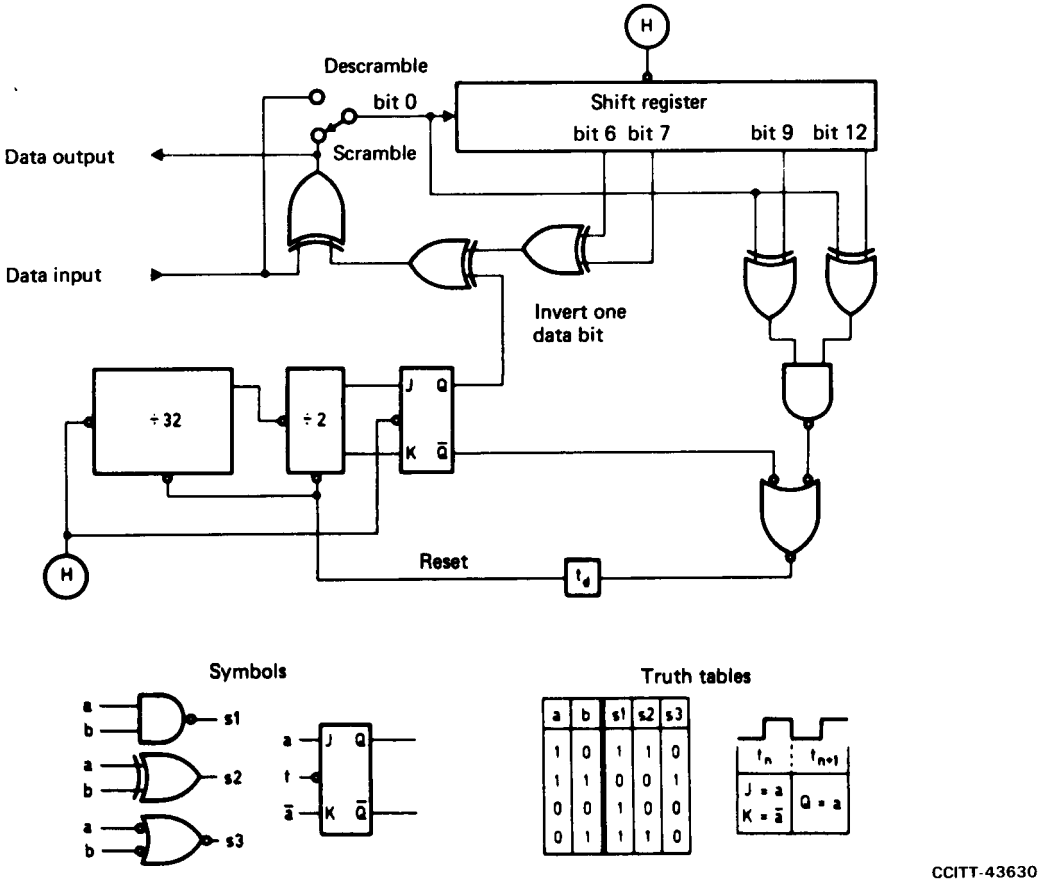
I.3 *Elements of scrambling process*

The factor $1 + x^{-6} + x^{-1}$ randomizes the transmitted data over a sequence length of 127 bits.

The equality $a_i = a_{i+9}$ in the guard polynomial *p(x)* prevents repeated patterns of 1, 3 and 9 bits from occurring for more than 42 successive bits.

The equality $a_i = a_{i+12}$ in *p(x)* prevents repeated patterns of 2, 4, 6 and 12 bits from occurring for more than 45 successive bits.

I.4 Figure I-2/V.27 is given as an indication only, since with another technique this logical arrangement might take another form.



Note 1 – Ⓗ represents the clock signal. The negative going transition is the active transition.

Note 2 – There is a delay time, due to physical circuits, between a negative going transition of Ⓗ and the end of the "0" state represented by t_d on the non-RESET wire; therefore the first coincidence between bit 0 and bit 9 or bit 12 is not taken into account by the counter.

Note 3 – The same voltage convention is used for data signals and logical circuits in the diagram.

FIGURE I-2/V.27

An example of scrambler and descrambler circuitry

Reference

[1] CCITT Recommendation *Characteristics of special quality international leased circuits, with special bandwidth conditioning*, Vol. IV, Rec. M.1020.