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SERIES V: DATA COMMUNICATION OVER THE
TELEPHONE NETWORK

Interworking with other networks

SUPPORT BY AN ISDN OF DATA TERMINAL EQUIPMENT WITH V-SERIES TYPE INTERFACES WITH PROVISION FOR STATISTICAL MULTIPLEXING

Reedition of CCITT Recommendation V.120 published in
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NOTES

Recommendation V.120

SUPPORT BY AN ISDN OF DATA TERMINAL EQUIPMENT
WITH V-SERIES TYPE INTERFACES WITH PROVISION
FOR STATISTICAL MULTIPLEXING

(Melbourne, 1988)

The CCITT,

considering

(a)   that the ISDN will offer the universal interfaces to connect subscriber terminals in accordance with the reference configuration described in Recommendation I.411;

(b)   that during the evolution of ISDN there will exist for a considerable period DTEs with V-Series interfaces which need to connect to ISDN;

(c)   that it would be desirable that terminals with V-Series interfaces interwork easily with ISDN TE1s;

(d)   that statistical multiplexing provides improved utilization of bandwidth in some applications;

(e)   that the D channel signalling protocol is described in Recommendations I.430, I.431, Q.921 and Q.931;

(f)   that there exists CCITT Recommendation V.110 for adapting DTEs with a V-Series interface onto B Channels;

unanimously declares

(1)   that the scope of this Recommendation shall cover the connection to the ISDN of terminals with interfaces for modems conforming to current V-Series Recommendations, operating in accordance with circuit or leased circuit bearer services on bearer channels (B, H0, H11 or H12) (see Note);

(2)   that the following circuit-switched services may be supported:

–   multiplexing of several data links on a single bearer channel; (and/or)

–   automatic establishment and disestablishment of additional data links;

(3)   that the reference configurations of § 1 shall apply;

(4)   that the terminal adaptor (TA) functions necessary to support the connection of DTEs with V-Series type interfaces on an ISDN shall include the following:

–   conversion of the electrical and mechanical interface characteristics;

–   bit rate adaption;

–   end-to-end synchronization;

–   call establishment and disestablishment based on either manual or automatic calling and/or answering;

–   maintenance functions.

Note – The compatibility of V.120 with protocols developed in other Study Groups for Additional Packet Mode Bearer Service (APMBS) as defined in Recommendation I.122 is for further study and the provisions of this Recommendation, V.120, shall not prejudice this study.

Significant further study related both to aspects of the protocol and the alignment with other ISDN protocols is needed on this Recommendation.

1   Reference configurations

1.1   *Customer access configurations*

There are two basic classes of devices capable of data transmission in the ISDN environment:

–   devices directly attached to the ISDN, i.e. TE1s; and

–   devices attached to the ISDN through a terminal adaptor, i.e. V-Series TE2s.

1.2   *Connectivity*

ISDN connectivity requirements include support for TE1-to-TE1, TE2-to-TE2 (TA-to-TA) and TE1-to-TE2 (TE1-to-TA) connections as discussed and illustrated in Figure 1/V.120. This document specifies a terminal adaption protocol based on a modification of LAPD that supports these connections. LAPD is specified in CCITT Recommendation Q.921. The modifications are specified in § 2.4 of this Recommendation.

This protocol provides a consistent protocol for carrying different types of data streams (see §§ 3.3 to 3.5). This approach using a HDLC based protocol provides the capability for multiplexing multiple logical circuits on a channel. This also allows for different higher layer protocols to be running concurrently on a single channel (see § 2.2).

In come cases the speed of the communicating TE2s is the same. It is possible in certain cases to connect devices with different speeds using the frame encapsulation procedures described later in § 2, and in more detail in § 3. The key factors that make this concept viable are TA buffering, TA flow control, HDLC encapsulation and HDLC flow control.

The application of this protocol to TE1-to-TA applications is discussed in Appendix I.

Within I.515, parameter exchange procedureds are *generally described* to allow interworking between incompatible terminal adaptors (TAs) that may not require interworking functions within the network. Interworking between different types of TAs can be accomplished with Multifunctional Terminal Adaptors (MTAs) that are capable of supporting more than one protocol. However, Figure 1/I.515 also depicts other interworking scenarios that will require IWFs when TAs are not capable of supporting more than one protocol.

TA-V   V.120 terminal adaptor supporting V-Series TE2s   T1700250-88
IWF   Interworking function
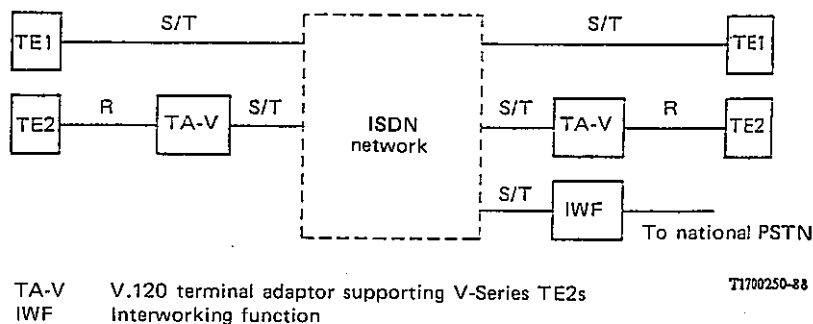
Note – Other configurations are shown in Recommendation I.515.

FIGURE 1/V.120

ISDN connection scenarios for V.120 terminal adaptors

2   Data transport protocol specification

This protocol relies on procedures similar to those in CCITT 1986 Recommendation Q.921/I.441. It provides the capability for use with compatible TE1 or TA equipments.

The use in TE1s of the protocols specified in this document is described in Appendix I. The remainder of this document is concerned with their use in TAs.

2.1   *Functions provided by protocol*

2.1.1   *Categories of functions*

There are two categories of functions provided by this specified protocol. There is a set of base functions and a set of additional functions. The additional functions depend upon the type of data flow (character coded or message).

2.1.2   *Base functions*

The base functions of the protocol include the following:

– transparent transport of data;

– generation and interpretation of messages for peer communication (i.e. post call connection handshake);

–   administration of timers and counters used in communication;

–   error detection.

2.1.3 *Additional functions*

The additional functions of the protocol include the following:

–   transport and interpretation of interface status change at the R reference point;

–   segmenting and reassembly of messages;

–   transport of detected interface errors at the R reference point;

–   support for operation with a network independent clock;

–   multiplexing of synchronous and asynchronous protocols;

–   interworking of two TEs operating at different data rates;

–   flow control;

–   retransmission on error detection.

2.2 *General terminal adaption*

The terminal adaption mechanisms are divided into two general categories:

–   protocol sensitive operation for character or message encapsulation; and

–   bit transparent operation where no alignment (above the bit level) of information from the interface at the R reference point is made within the frame transport in the bearer channel.

The interface bit rate at the R reference point must be less than the bearer channel capability. The terminal adaptor may support single or multiple interfaces at the R reference point. In the later case the protocol applies separately to the data streams associated with each interface. The use of logical link identifiers to distinguish between data streams will be described.

2.2.1 *Protocol sensitive operation with start/stop mode TE2s (asynchronous mode)*

The start and stop bits are removed and parity may be checked (see § 3.3.1). The resultant character(s) is placed in a frame for transport on the bearer channel to a peer entity. The peer entity may be in a peer TA where the reverse process takes place to another interface at an R reference point, or the peer entity may be in a TE1 where the character(s) is passed to a higher layer within the TE1, or in an interworking function. Errors detected on the interface at the R reference point are relayed to the peer entity which will:

1)   notify the higher layer of the detected error; or

2)   replicate the error (see §§ 3.3.1 and 3.3.2) at the outbound interface at the R reference point.

The terminal adaptor will recognize and remove any erroneous NULL characters (created by the initiation of BREAK) before transmission.

2.2.2 *Protocol sensitive operation with synchronous HDLC TE2s (synchronous mode)*

The flags and zero bit insertion are removed and the FCS is checked and removed but the address, control, and information fields flow transparently through the TA. The resultant octet-aligned message is placed in one or more frames for transport to a peer entity over the data link connection on the bearer channel. The original message from the interface at the R reference point may be segmented within the TA and forwarded in parts to the peer entity. This segmenting and forwarding process may occur as the message is received. This avoids the delays associated with accumulating a full message. The peer entity performs the reverse process at the peer interface R reference point.

If an FCS error is detected at the interface at the R reference point, this is relayed to the peer entity which will either:

1)   discard the entire message; or

2)   cause an abort to be sent on the interface at the R reference point in the message which is in progress; or

3)   generate an incorrect FCS in the message which is in progress.

Note – Support of non-octet aligned messages is for further study.

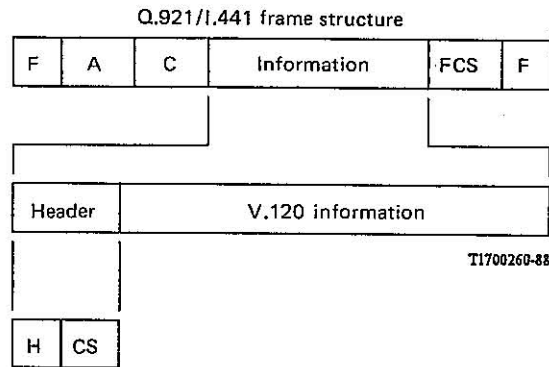### 2.2.3 *Transport operation (bit transparent mode)*

In bit transparent operation the TA will encapsulate the bits from the interface at the R reference point into frames as they are received. These frames are forwarded to a peer entity. The peer TA removes the bits from the frames

and sends them on the interface at the R reference point. No processing or modification of the bits is performed and there is no checking fot bit stream errors on the interface at the R reference point. This mode is used for all modes not covered by the asynchronous or synchronous modes defined above.

Note – In many cases UI frames will be used to convey frames in this mode.

2.3 *General messages and formats*

The frame structure used is that specified in Recommendation Q.921/I.441. There is an optional one or two octet header. The header octet(s), when present, directly follows the control field of the V.120 frame as shown in Figure 2/V.120.


```
            Q.921/I.441 frame structure
     ┌───┬───┬───┬──────────────┬─────┬───┐
     │ F │ A │ C │  Information  │ FCS │ F │
     └───┴───┴───┴──────────────┴─────┴───┘

     ┌───────────┬──────────────────────────┐
     │  Header   │     V.120 information     │
     └───────────┴──────────────────────────┘
                                    T1700260-88
     ┌───┬────┐
     │ H │ CS │
     └───┴────┘
```

F   HDLC flag
A   Address (default is 2 octets)
C   Control (HDLC formats)
FCS   Frame check sequence
H   Terminal adaption header (optional for bit transparent mode)
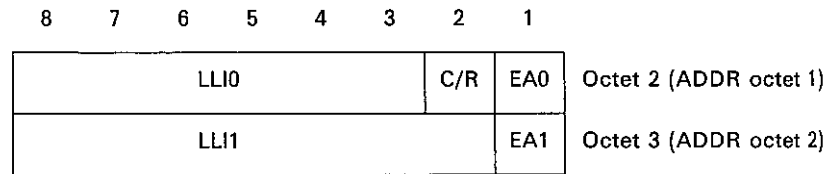CS   Optional header extension for control state information

Note – The A, C, H, CS and information fields are transmitted an octet at a time, low order bit first (bit 1). The FCS is transmitted high order bit first.

FIGURE 2/V.120

Frame format

2.3.1 *Address field*

The format of the V.120 address field in Figure 2/V.120 is similar to that specified in Recommendation Q.921/I.441. The LLI0 and LLI1 fields may be viewed as a single 13 bit logical link identifier (LLI) field or alternatively as two separate fields. This is shown in Figure 3/V.120.

```
       8    7    6    5    4    3    2    1
    ┌──────────────────────────┬─────┬─────┐
    │          LLI0            │ C/R │ EA0 │  Octet 2 (ADDR octet 1)
    ├──────────────────────────┴─────┼─────┤
    │          LLI1                   │ EA1 │  Octet 3 (ADDR octet 2)
    └─────────────────────────────────┴─────┘
```

LLI0   High order 6 bits of LLI
LLI1   Low order 7 bits of LLI
C/R   Command/response bit
EA0   Octet 2 address extension bit — set to 0
EA1   Octet 3 address extension bit — set to 1 (for two octet address field)

FIGURE 3/V.120

Address field format

The LLI is considered to be the concatenation of the LLI0 field with the LLI1 field. The LLI can take on values in the range 0-8191. Table 1/V.120 indicates values that are reserved.

TABLE 1/V.120

Reserved LLI values

LLI	Function
0	In-channel signalling
1-255	Reserved for future standardization
256	Default LLI
257-2047	For LLI assignment
2048-8190	Reserved for future standardization
8191	In-channel layer management

2.3.2   *Address extension bit (EA)*

The address field range is extended by using bit 1, the first transmitted bit, of the address field octets to indicate the final octet of the address field. The presence of a "1" in bit 1 of an address field octet signals that it is the final octet of the address field.

2.3.3   *C/R bit*

The C/R bit identifies a V.120 frame as either a command or a response (see § 2.4). The C/R bit is employed symmetrically for the two directions of transmission and is coded as shown in Table 2/V.120.


TABLE 2/V.120

Coding of C/R bit

C/R	Meaning
0	Command
1	Response

2.3.4   *Control field*

The use of the V.120 control field is described in § 2.4.

2.3.5 *Header octet*

The format of the header octet is shown in Figure 4/V.120 (see §§ 3.3 to 3.5 for details on the use of these fields). The header octet is mandatory for protocol sensitive modes and is optional for bit transparent mode.

bit 8	7	6	5	4	3	2	1
E	BR	res	res	C2	C1	B	F
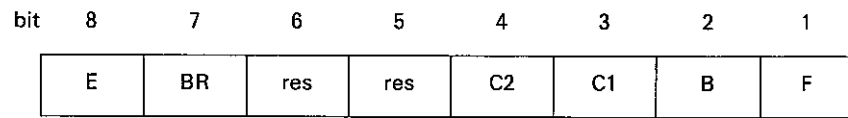
E   Extension bit
BR   Break/HDLC idle bit
C1, C2   Error control bits
B, F   Segmentation bits
res   Reserved for future standardization

FIGURE 4/V.120

Header octet format

2.3.5.1 *E-extension bit (bit 8)*

The E bit is the header extension bit. It allows for extension of the header to provide additional control state information. A "0" bit indicates that a control state information octet follows (see § 2.3.6).

2.3.5.2 *BR-break/HDLC idle bit (bit 7)*

In asynchronous applications, the break bit indicates the invocation of the BREAK function by the TE2. A "1" in this bit position indicates BREAK (see § 3.3).

In protocol sensitive operation for synchronous HDLC applications, the BR bit is used to indicate an HDLC idle condition on the interface at the R reference point. A "1" in this bit position indicates that the interface at the R reference point is receiving HDLC idle condition (see § 3.4).

2.3.5.3 *Bits 5 and 6*

Bit 5 and bit 6 of the header octet are reserved and set to "0".

2.3.5.4 *C1, C2-error control (bits 3 and 4)*

Bit 3 and bit 4 of the header octet are defined as Control 1 and Control 2 respectively and are used for TA error detection and transmission.

The meanings of the C1 and C2 bits are encoded as shown in Table 3/V.120.

TABLE 3/V.120

Coding of C1 and C2 bits

C1	C2	Meaning		
		Synchronous	Asynchronous mode	Bit transparent mode
0	0	No error detected	No error detected	No error detected
0	1	FCS error (interface at R)	Stop-bit error	Not applicable
1	0	Abort	Parity error on the last character in frame	Not applicable
1	1	TA overrun (from interface at the R reference point)	Both stop-bit and parity error	Not applicable

### 2.3.5.5 *B, F-segmentation bits (bit 2 and bit 1)*

The B and F bits are used for segmenting and reassembly of messages in synchronous mode applications. Setting the B bit to "1" indicates that the frame contains an information portion beginning a message. Setting the F bit to "1" indicates the frame contains the final portion of the message. If the entire message is contained within a single frame then both B and F bits will be set to "1". A frame which is neither first nor last is termed a middle frame. For the asynchronous mode and the bit transparent mode these bits are set to "1".

TABLE 4/V.120

Coding of B and F bits

B	F	Synchronous	Asynchronous	Bit transparent
1	0	Begin frame	Not applicable	Not applicable
0	0	Middle frame	Not applicable	Not applicable
0	1	Final frame	Not applicable	Not applicable
1	1	Single frame	Required	Required

2.3.6 *Control state information*

The control state information is contained in the second octet of the header when present. In general, for TAs, this field serves as a physical status/interface control field for the interface at the R reference point. Control state information may be sent whenever one of the mapped control leads changes, although the TA should be able to accept the CS octet anytime the H field is present. Figure 5/V.120 shows the format of the control state information octet. For an example of the mapping of the V.24 leads, see Annex A. See § 2.6 for the procedures and see § 3.2.1 for the use of the RR bit for flow control.

8	7	6	5	4	3	2	1
E	DR	SR	RR	res	res	res	res
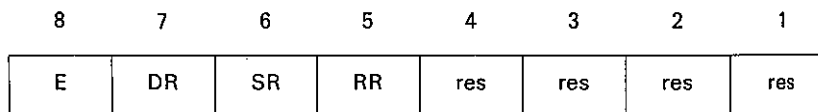
E   Extension bit
DR Data ready
SR Send ready
RR Receive ready
res Reserved for future standardization

FIGURE 5/V.120

Control state information octet

2.3.6.1 *E-extension bit (bit 8)*

The extension bit allows for further extension of the header octets. The E bit set to "1" to indicate no further extension of the header.

2.3.6.2 *DR – data ready (bit 7)*

This bit set to "1" indicates that the interface at the R reference point is activated. For TE1 it implies the terminal interface is activated.

2.3.6.3 *SR – send ready (bit 6)*

This bit set to "1" indicates that the TE is ready to send data.

2.3.6.4 *RR – receive ready (bit 5)*

This bit set to "1" indicates that the TE is ready to receive data.

2.3.6.5   *Bits 4, 3, 2, 1*

Bits 4, 3, 2 and 1 of the control state information octet are reserved and set to "0".

2.3.7   *Interframe time fill*

Interframe time fill should normally be HDLC flags. For special applications it may be all ones.

2.4   *Elements of procedure and procedures*

Two types of logical connections are available using the procedures described in this specification, namely:

1)   support of unacknowledged information transfer only (see § 5.2 of Recommendation Q.921);

2)   support of both multiple frame acknowledged information transfer and unacknowledged information transfer (see § 5.5 of Recommendation Q.921).

For either type, the elements of procedure and procedures are as specified in §§ 3 and 5 of Recommendation Q.921, with the following differences:

–   C/R bit symmetry;

–   receipt of I frame response;

–   transmission of FRMR response;

–   no TE1 management procedures;

–   management of address field LLI.

These differences are detailed below.

2.4.1   *C/R bit symmetry*

The use of the C/R bit is symmetric as described in § 2.3.3.

2.4.2   *Receipt of I frame response*

During multiple frame acknowledged information transfer operation, I frames sent as either commands or responses shall be received. I frame responses are optional to send.

Q.921 variable description

N(S)   Send sequence number

N(R)   Receive sequence number

V(R)   Next expected received N(S)

When a data link layer entity receives a valid I frame command whose N(S) is equal to the current V(R) and whose N(R) is in the proper range, it shall follow the procedures stated in §§ 5.6.2 and 5.6.6 of Recommendation Q.921.

When a data link layer entity that is not in a timer recovery state receives a valid I frame response with F bit set to "0" with its N(S) equal to the current V(R) and whose N(R) is in the proper range, it shall treat the frame as a valid I frame command with P bit set to "0" and follow the procedures stated in §§ 5.6.2 and 5.6.6 of Recommendation Q.921. If the received I frame response has its F bit set to "1", the data link layer entity shall indicate an error to the connection management entity.

When a data link layer entity is in a timer recovery condition and receives a valid I frame response with F bit set to "0" with its N(S) equal to the current V(R) and whose N(R) is in the proper range, it shall treat the frame as a valid I frame command with P bit set to "0" and follow the procedures stated in §§ 5.6.2 and 5.6.6 of Recommendation Q.921.

When a data link layer entity is in a timer recovery condition and receives a valid I frame response with F bit set to "0" with its N(R) in the proper range, it shall clear the timer recovery condition and reset timer T200 as if it had received a supervisory frame response with F bit set to "1", as described in § 5.6.7 of Recommendation Q.921. If the I frame has N(S) equal to the current V(R), it is then processed as if it were an I frame command with P bit set to "0", following the procedures stated in §§ 5.6.2 and 5.6.6 of Recommendation Q.921. If the I frame has N(S) not equal to the current V(R), the data link layer entity shall transmit a REJ command prior to resumption of transmission or retransmission of I frames and enter the REJ exception condition as described in § 5.8.1 of Recommendation Q.921.

2.4.3   *Transmission of FRMR response*

A frame rejection condition results from one of the following:

1)   the receipt of a supervisory or unnumbered frame with incorrect length;

2)   the receipt of an invalid N(R);

3) the receipt of an I frame with an information field which exceeds the maximum allowed length; or

4) the receipt of a command or response control field that is undefined or not implemented.

Upon occurrence of a frame rejection condition, the data link layer entity shall:

– transmit a FRMR response with F bit set to the value of the P bit in the rejected frame;

– indicate an error to the connection management entity; and

– enter the "multiframe not established" state. The "multiframe not established" state is essentially equivalent to the "TE1 assigned" state described in Recommendation Q.921. It is the state initially entered by the data link layer entity when the logical connection establishment procedure is completed successfully.

The format and coding of the FRMR response is as shown in Table 5/Q.921 and Figure 6/Q.921.

2.4.4 *No TE1 management procedures*

The TE1 has no counterpart and the associated Recommendation Q.921 procedures for TE1 management do not apply.

2.4.5 *Management of address field LLI*

The address field is managed using the procedures of § 4.3.

2.5 *Data field length*

The maximum number of octets in a data field (N2xx) is a system parameter. Its value must be less than or equal to N201 (see Recommendation Q.921) minus the length of the header.

2.6 *Control state information processing*

This section describes the use of the control state variables and the processing of the control state information field, when present, defined in § 2.3.6. Use of the control state information field is optional (see octet 5b, bit 7 of low layer compatibility, § 4.4.5).

The terminal adaption entity maintains six control state variables that indicate the current state of the DR, SR and RR indicators as follows:

– send variables DR(S), SR(S) and RR(S) – equal to the current local states of DR, SR and RR, respectively, as transmitted to the far end peer entity;

– receive variables DR(R), SR(R) and RR(R) – equal to the current states of DR, SR and RR, respectively, in the peer entity as received from it.

2.6.1 *Control state information initialization*

Whenever the protocol is initialized to start communications, the protocol entity will set the receive variables (DR(R), SR(R) and RR(R)) to "0" and the send state variables to reflect the status of the interface at the R reference point.

2.6.2 *Sending a control state information field*

A control state information field will be sent whenever a send control state variable changes. A send control state variable will change with a change to the interface at the R reference point or a change to a receive control state variable. The control state information held will be sent following any queued data for interface at the S/T reference point. The control state information field is sent in the last frame containing data received across the interface at the R reference point prior to the control state variable change, or in a separate frame.

The contents of the control state information octet is set to the state of the corresponding send control state variables. DR is set to DR(S), SR is set to SR(S) and RR to RR(S).

2.6.3 *Receiving a control state information field*

Upon receipt of a control state information field, the control field is checked with the receive control state variables: DR to DR(R), SR to SR(R) and RR to RR(R). The receive control state variables are set to their received values.

If SR(R) was "0" and the SR bit in the received control state information field is "1", then the interface at the R reference point and the RR(S) state are changed.

If SR(R) was "1" and the SR bit in the received control state information field is "0", then the interface at the R reference point and the RR(S) state are changed, consistent with one of the following:

- if received data (from peer entity) does not remain to be forwarded (no message in progress), then the control actions can occur immediately;

- if received data (from peer entity) is incomplete (e.g. in protocol sensitive mode the final frame was not received), then the incomplete message is forwarded (continued) until completion on the interface at the R reference point, at which time the control actions can occur;

- if received data (for peer entity) is complete, then the received data is forwarded until completion on the interface at the R reference point, at which time the control actions can occur.

If RR(R) and the RR bit in the received control state information field are not the same, then the interface at the R reference point is changed.

If DR(R) was "0" and the DR bit in the received control state information field is "1", then the interface at the R reference point is changed.

If DR(R) was "1" and the DR bit in the received control state information field is "0", then the interface at the R reference point is changed consistent with the following:

- if the received message from the peer entity is incomplete, it is discarded;

- if the received message from the peer entity is a complete, message, then it should be forwarded to the interface at the R reference point until completetion prior to the control actions taking place.

2.7 *Parameter negotiation*

Parameter negotiation during the bearer channel establishment is in accordance with the procedures described in CCITT Recommendation Q.931. During logical link negotiation, a specific value for a parameter may be requested by including the low layer compatibility information element containing the desired parameters in the SETUP message. The receiving TA may accept the requested parameter values by responding with a CONNect message. If the receiving TA does not accept the parameter values included in the SETUP message, it may negotiate by including the desired values in a low layer compatibility information element in the CONNect message. The originating TA may refuse the parameters receiving in the connect message by initiating clearing with the cause number 21 "Call Rejected".

3 Terminal adaptor (TA) functions

3.1 *Clock synchronization*

The specific mechanisms for providing clock synchronization is implementation dependent. See Appendix II for a discussion.

3.2 *Data flow control and buffering*

Once a frame is assembled (from the interface at the R reference point), it is sent on the interface at the S/T reference point at the nearest opportunity. V.120 procedures may control the flow of frames to the interface at the S/T reference point. The handling of overflow conditions will be described below in the appropriate sections on each mode of operation.

3.2.1 *Asynchronous mode*

In the asynchronous mode, upon the TA receiving a frame from the interface at the S/T reference point, the characters will be sent to the interface at the R reference point at the earliest opportunity. In the asynchronous mode under-run is not a problem, only the over-run condition is of concern. When all buffers are full, the TA flow controls the sender by not acknowledging until a buffer becomes available, when operating in multiple frame acknowledged mode, or using the RR bit in the control state information octet, if available, when operating in unacknowledged mode.

Flow control is indicated when a control state information field with the R bit set to "0" is received. The flow control condition is removed when a flow controlled TA receives a control state information field with the RR bit set to "1". A TA may indicate a change in the state of the RR control state variable by sending UI frames with zero length V.110 information fields containing the control state information field even when it is flow controlled by the other TA.

Note – Some asynchronous terminals may use local flow control.

3.2.2   *Synchronous mode*

In the synchronous mode, a possible under-run condition exists as well as the over-run. Adequate buffering should be provided to normally prevent under-running the interface at the R reference point.

If under-run towards the interface at the R reference point occurs, the current message will be treated by sending an abort or forcing an FCS error.

If an over-run occurs on buffers toward the interface at the S/T reference point a frame will be sent across the interface at the S/T reference point indicating "final" and having the C1 and C2 bits set to "1" following any messages completely received from the interface at the R reference point. Additional data received from the interface at the R reference point will be discarded until the start of a new message is detected.

3.2.3   *Bit transparent mode*

In the bit transparent mode, either under-run or over-run may occur. In this mode the TE2s must operate at the same data rate. Adequate buffering should be provided to minimize under-running the interface at the R reference point.

When the buffers are empty, the interface at the R reference point will be set to the mark hold condition.

If the buffer to the interface at the S/T reference point over-flows, the buffer pool will be set to empty state and accumulation of data restarted.

3.3   *Asynchronous mode operation*

3.3.1   *Character processing – TE2 to S/T direction*

The following processing will be performed on start/stop data received from the TE2:

1)   the start and stop bits will be removed from each character;

2)   the remaining bit in the character may be checked for correct parity;

3)   the parity bit will be removed if the code being used is an 8-bit code; otherwise passed as part of the octet;

4)   codes using less than 8 bits (including parity) are padded in the high order bits.

The resulting data is placed in frames, with the segment bits indicating single segment and set to "1".

Frames may be sent based on a timer, after a certain frame size, after a carriage return, etc. However, the forwarding mechanism used is an implementation issue and may vary.

If a BREAK is detected by the TA on the interface at the R reference point, a frame with the BR bit set in the Header will be transmitted in the same frame or after all queued characters have been sent. The C1 and C2 bits should be set to "0".

If a parity error is detected on a character of data being received from the TE2, the C1 bit is set to "1" and the frame sent following any frames already queued for transmission. Thus, setting of the C1 bit to "1" indicates that the last character in the frame in which the C1 bit is set to "1" was received by the TA with a parity error. If a stop bit error is detected on a character of data being received from the TE2, the C2 bit is set to "1" and the frame sent following any frames already queued for transmission. Thus, setting of the C2 bit to "1" indicates that a stop bit error was detected by the TA immediately following the last character contained in the frame in which the C2 bit is set to "1".

3.3.2   *Character processing – S/T to TE2 direction*

The TA will perform the following processing on the data received from the interface at the S/T reference point:

1)   if the asynchronous character is less than 8 data bits, the characters will be sent to the TE2 as is;

2)   if the asynchronous character contains 8 data bits, each character will be sent to the TE2 with the appropriate parity bit appended;

3)   if the C2 bit is set to "1" indicating a stop bit error, the TA action is not defined;

4)   if the C1 bit is set to "1" and the asynchronous character contains 8 data bits, indicating a parity error, then the TA may force a parity error on the last character sent to the TE2;

5)   if the BREAK bit is set to "1", then the TA will send BREAK to the TE2 following all characters received prior to the break;

6)   start and stop bits will be appended to the characters as required.

3.4 Synchronous mode operation

3.4.1 Message processing – TE2 to S/T direction

The following processing will be performed on the HDLC frame received from the TE2:

1) the beginning flag(s) will be removed;

2) all inserted zeros will be removed;

3) FCS will be accumulated until a flag is detected. The polynomial $G(X) = X^{**}16 + X^{**}12 + X^{**}5 + 1$ will be used for the FCS accumulation. The accumulated FCS will be compared with the FCS received from the TE2;

4) the FCS character received from the TE2 will be removed in all cases except for when UI frames are used to carry HDLC frames, in which case the FCS of the original HDLC frame is also carried as data;

5) the ending flag will be removed.

The resulting data will be segmented, if necessary, with each segment preceded by the header. Segmentation shall be such that no frame transmitted on the interface at the S/T reference point is longer than N201 octets.

If only one segment is required, the header will indicate both beginning segment and final segment in the "B" bit and the "F" bit. If more than one segment is required, the header of the first segment will indicate "begin" segment and the last segment of the message will indicate "final" segment. All intermediate segments will have both "begin" and "final" segment indicators set to "0".

The C1 and C2 bits will be set as follows in the final or only segment to indicate detected error conditions:

– if an FCS error is detected as a result of the FCS accumulation process described in step 3 above, then the C2 bit will be set to "1" with the C1 bit set to "0";

– if an abort sequence is detected on the interface at the R reference point, then the C1 bit will be set to "1" with the C2 bit set to "0";

– if an over-run occurs on buffers toward the interface at the S/T reference point, as described above in § 3.2.2, then both the C1 and C2 bits will be set to "1".

When the TA first detects an HDLC idle condition on the interface at the R reference point, it will transmit a frame with the BR bit in the header set to "1" following any queued data frames.

3.4.2 Message processing – S/T to TE2 direction

The TA will perform the following processing on the data received:

1) The header will be checked as follows:

   a) if the "begin" segment bit is "1" and the previous segment did not have the "final" segment bit set to "1", then the previous message will be terminated with an ABORT sequence;

   b) if the "begin" segment bit is "0" and there is no message currently in process, the segment will be discarded;

   c) if the C1 and C2 error bit is "1" with the "final" bit a "1", an ABORT sequence will be sent to the TE2 instead of the FCS characters.

2) The FCS is recalculated for TA reconstructed messages when transmitted at the interface at the R reference point except in the case where UI frames are used to carry HDLC frames. In this case the FCS of the original HDLC frame is used in the reconstructed frame. The TA has the option of examining the original FCS, which has been passed to it in the data stream and taking appropriate action.

If an under-run occurs toward the interface at the R reference point, then the frame being sent to the TE2 shall be treated as described in § 3.2.2.

If the BR bit is "1", then the TA will set an HDLC idle condition on the interface at the R reference point following data queued for transmission. The HDLC idle condition will be maintained until a frame is received with its BR bit set to "0".

3.5 Bit transparent mode operation

The TA breaks synchronous data stream into fixed size frames and sends it over the channel as it is received from the TE2. The TA takes data from frames received and sends it to the TE2.

The terminal adaption header must be used in bit transparent mode if it is necessary to transmit the control state information. When the terminal adaption header is used in this mode C1 and C2 bits must both be set to "0" (no error). B and F bits must both be set to "1" and reserve bits must be set to "0".

If an under-run occurs toward the interference at the R reference point, then the frame being sent to the TE2 shall be treated as described in § 3.2.3.

For unique applications, the contents of a frame with an FCS error may be delivered across the interface at the R reference point.

4 Connection control procedures

This section describes the procedures for establishing connections for V.120 terminal adaption. Procedures are described for:

– establishment of an ISDN circuit-switched connection; and

– optional procedures for the negotiation of logical link identifiers.

The protocol described in the following sections describing procedures for negotiating logical links is based on Recommendation Q.931 messages, information elements and procedures, but is tailored for this particular application. It is differentiated from the full Recommendation Q.931 procedures by the use of a unique protocol identifier ("00001001"). In addition to the information elements of Recommendation Q.931, an additional information element is required to convey the logical link identifier for this application and is defined in the following sections.

The selection of V.120 as a terminal adaption protocol at the establishment of the bearer channel is specified by information in the bearer capability information and/or low layer compatibility information elements of the bearer channel SETUP procedure.

Logical link negotiation procedures may be carried out by means of user information messages in a Recommendation Q.931 Call associated temporary signalling connection on the ISDN D Channel, or by means of logical link zero within the bearer channel using Recommendation Q.921 elements of procedure (i.e. either UI or I frames). The choice of methods is a terminal equipment option and is partially determined by the availability of end-to-end ISDN signalling capability. The optional establishment of logical links between equipments that support different options may not be possible.

4.1 *Establishment of circuit-switched connection*

The bearer channel between the TAs is controlled using the D channel signalling procedure for call establishment is described in Recommendation Q.931.

On the basis of call setup information, the network provides a bearer channel to the requested end-point. The transfer mode and transfer capability in the bearer capability (BC) information element of the setup message is coded as circuit, unrestricted or restricted.

4.2 *Establishment of logical links*

This procedure requires that all TAs either be "default assignees" or "assignor only". The TAs that must always assign the LLI (e.g., TAs with pre-assigned LLIs) are assignor only, all other TAs are default assignee. An assignor/assignee field is provided in the low layer compatibility (LLC) and bearer capability (BC) information elements for V.120. This field must be coded as "0" when the TA is a default assignee, and as "1" when the TA is an assignor only. The "default assignee" may assume the role of "assignor only" during negotiation.

4.2.1 *During the bearer channel setup phase*

The first logical link is established between the two TAs using the default LLI = 256 using the information provided in the LLC information element.

4.2.2 *During the bearer channel active phase*

4.2.2.1 *Resolving when both sides are default assignees*

The first TA initiating a request for a logical link other than the default will assume the assignee role. The TA that receives that request will assume the assignor role.

If both TAs simultaneously send SETUP messages, the SETUP message containing the larger "call reference" (see Recommendation Q.931 for definition of call reference) is accepted and treated in accordance with the above procedure. The response to the SETUP message with the lower "call reference" is a RELease COMPlete message. If both SETUP messages contain the same "call reference", they are both cleared with RELease COMPlete messages, and the TAs select different "call references" and try again.

4.2.2.2 *LLI assignee*

If a TA is determined to be LLI assignee, it must set the assignor/assignee field contained in any additional SETUP messages to zero.

The LLI assignee TAs request additional logical links by sending a SETUP message without the LLI information element. The TA receiving this SETUP message assigns an LLI by including the LLI information element in the CONNect message.

4.2.2.3 *LLI assignor*

If a TA is determined to be LLI assignor, it must set the assignor/assignee field contained in any additional SETUP message to one.

The LLI assignor TAs set up additional logical links by sending SETUP messages that include the LLI information element. The receiving TA responds with a CONNect message and sets up a logical link using the information provided in the SETUP message.

4.3 *Messages used for logical connection control*

The following messages are used for establishing logical links within a bearer channel.

Call establishment	SETUP
	CONNect
Call clearing	RELease
	RELease COMPlete

4.3.1 *Setup*

See Table 5/V.120.

This message is sent by either TA to indicate that it desires to initiate a new logical link. It must contain protocol discriminator, call reference, and message type. Low layer compatibility information element can optionally be included in the SETUP message. Logical link identifier information element must be included in the SETUP message if the TA is assigning the LLI, and not included if requesting an LLI from the other TA.

TABLE 5/V.120

SETUP message content

Information element	Ref. V.120	Type	Length
Protocol discriminator	4.4.1	M	1
Call Reference	4.4.3	M	2
Message type	4.4.2	M	1
Low layer compatibility	4.4.5	O (Note 1)	2-13
Logical link identifier	4.4.6	O (Note 2)	4

M   Mandatory

O   Optional

Note 1 – Included when the calling user wants to pass low layer compatibility information to the called user.

Note 2 – Included if the calling user has the responsibility for assigning LLI for that physical link.

4.3.2 *CONNect*

See Table 6/V.120.

This message is sent by the TA that has received a SETUP message to indicate that the request for establishment of an additional logical link has been accepted. It must include protocol discriminator, call reference, and message type information elements. The low layer compatibility information element can optionally be included in the CONNect message. The logical link identifier information element must be included if not included in the SETUP message, and is not included otherwise.

CONNect message content

Information element	Ref. V.120	Type	Length
Protocol discriminator	4.4.1	M	1
Call reference	4.4.3	M	2
Message type	4.4.2	M	1
Low layer compatibility	4.4.5	O (Note 1)	2-13
Logical link identifier	4.4.6	O (Note 2)	4

Note 1 – Included to allow the called user to negotiate low layer compatibility information with the calling user.

Note 2 – Included if the called user has the responsibility for assigning LLI.

4.3.3   *RELease*

See Table 7/V.120.

The RELease message is used to indicate that the TA intends to release the call reference and the logical link, and that the TA receiving this message must release the logical link and prepare to release the call reference after sending a RELease COMPlete. This message must contain protocol discriminator, call reference message type, and optionally cause information elements.

TABLE 7/V.120

RELease message content

Information element	Ref. V.120	Type	Length
Protocol discriminator	4.4.1	M	1
Call reference	4.4.3	M	2
Message type	4.4.2	M	1
Cause	4.4.4	O	2-4

4.3.4   *RELease COMPlete*

See Table 8/V.120.

The RELease COMPlete message is sent to acknowledge that the TA sending the message has released the logical link and call reference. This message must contain protocol discriminator, call reference, and message type and optionally cause information elements.

TABLE 8/V.120

RELease COMPlete message content

Information element	Ref. V.120	Type	Length
Protocol discriminator	4.4.1	M	1
Call reference	4.4.3	M	2
Message type	4.4.2	M	1
Cause	4.4.4	O	2-4

4.4   *Information elements*

4.4.1   *Protocol discriminator*

The protocol discriminator is "00001001".
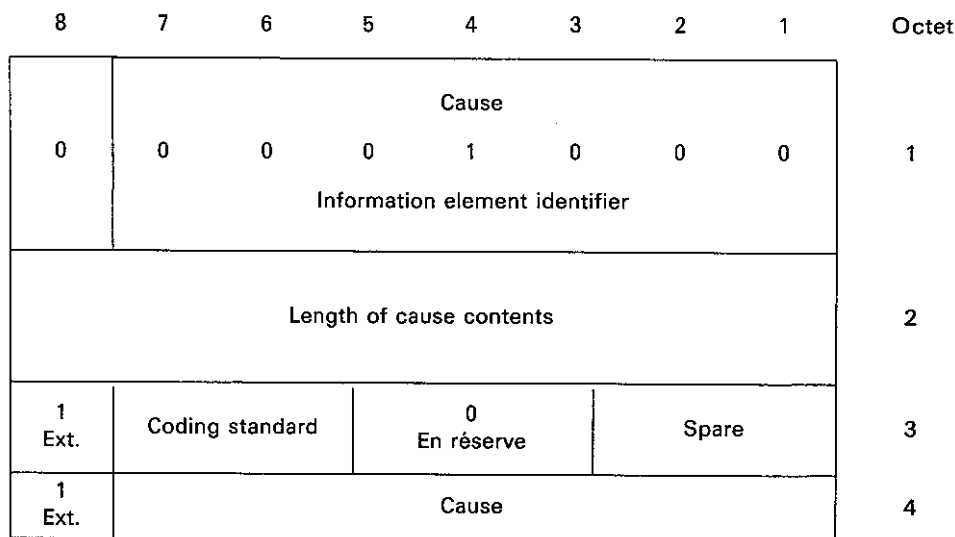
4.4.2 *Message type*

Message types are identical to message types in Recommendation Q.931.

4.4.3 *Call reference*

The call reference field should be two octets in length.

4.4.4 *Cause information element*

See Figure 6/V.120.

8	7	6	5	4	3	2	1	Octet

0	0	0	0	Cause 1	0	0	0	1
		Information element identifier						
Length of cause contents								2
1 Ext.	Coding standard		0 En réserve		Spare			3
1 Ext.	Cause							4

Cause values

16 Normal clearing
21 Call rejected

FIGURE 6/V.120

4.4.5 *Low layer compatibility information element*

See Figure 7/V.120.

4.4.6 *Logical link identifier information element*

The purpose of the logical link identifier information element is to identify a logical link within the bearer channel. The default length of this element is four octets. The logical link identifier information element is coded as shown in Figure 8/V.120.

4.5 *Logical connection control procedures*

This optional procedure defines the method for negotiation logical links other than the default (LLI = 256). For setup and clearing of the bearer channel, the procedure described in Recommendation Q.931 must be followed.

8	7	6	5	4	3	2	1	Octet
0	1	1	1	1	1	0	0	1
Low layer compatibility — Information element identifier								
Length of the low layer compatibility contents								2
1 Ext.	Coding standard		Information transfer capability					3
0/1 Ext.	Transfert mode		Information transfer rate					4
0/1 Ext.	Structure			Configuration		Establishment		4a* (Note 1)
1 Ext.	Symmetry		Information transfer rate (destination → origination)					4b* (Note 1)
0/1 Ext.	0 1 layer 1 ident.		User information layer 1 protocol					5* (Note 3)
0/1 Ext.	Synch./ asynch.	Negot.	User rate					5a* (Note 2)
0/1 Ext.	Hdr/no Hdr	Multi frame	Mode	LLI negot.	Assign/ assgnee	In-Band/out Band	0 Spare	5b* (Notes 2, 3)
0/1 Ext.	Number of stop bits		Number of data bits		Parity			5c* (Note 2)
1 Ext.	Duplex mode	Modem type						5d* (Note 2)
1 Ext.	1 0 Layer 2 ident.		User information layer 2 protocol					6*
1 Ext.	1 1 Layer 3 ident.		User information layer 3 protocol					7*

Note 1 — If default values are used for all fields of octet 4a and 4b, then these octets shall not be included. If default values are used for all fields of octet 4b, but not for one or more fields of octet 4a, then only octet 4a shall be included. Otherwise, both octets 4a and 4b shall be included.

Note 2 — This octet is present only if octet 5 indicates rate adaption.

Note 3 — Description of bits used in octet 5:

User information layer 1 protocol (octet 5)

Bits

5	4	3	2	1

0 1 0 0 0   CCITT standardized terminal adaption V.120 (based on LAPD). This implies the presence of octets 5a, 5b as defined below, and optionally octets 5c and 5d.

Rate adaptation header/no header (octet 5b, bit 7)

Bit

7

0   optional portions of terminal adaption header not included
1   optional portions of terminal adaption header included.

Multiple frame establishment support in data link (octet 5b, bit 6)

Bit

6

0   multiple frame establishment not supported. Only UI frames are allowed
1   multiple frame establishment supported

Mode of operation (octet 5b, bit 5)

Bit

5

0   bit transparent mode of operation
1   protocol sensitive mode of operation

LLI negotiation (octet 5b, bit 4)

Bit

4

0   default LLI = 256 only
1   full LLI negotiation

Assignor/assignee (octet 5b, bit 3)

Bit

3

0   message originator is «default assignee»
1   message originator is «assignor only»

In-band/out-of-band negotiation (octet 5b, bit 2)

Bit

2

0   negotiation is done with user information messages on a call associated temporary signalling connection
1   negotiation is done in-band using logical link zero

FIGURE 7/V.120

Logical link identifier information element

8	7	6	5	4	3	2	1	Octets
		Logical link identifier						
0	0	1	1	0	1	0	0'	1
		Information element identifier						
		Length of logical link identifier contents						
0	0	0	0	0	0	1	0	2
0	0 Spare	Logical link identifier (high order 6 bits)						3
1 Ext.	Logical link identifier (low order 7 bits)							4

FIGURE 8/V.120

4.5.1 *Logical link establishment*

A logical link may be established by either TA by sending a SETUP message.

If the TA sending the SETUP message assigns the LLI, the SETUP message must also include the assigned LLI value for the logical link.

If the TA does not assign the LLI, it must not include the LLI information element in the SETUP message. In this case the LLI is assigned by the receiving TA by including an LLI information element in the CONNect message.

A TA may request a logical link by sending a SETUP message, setting timer T303, and entering "call initiated" state.

If no response to the SETUP message is received before the first expiry of timer T303, the SETUP message must be transmitted and timer T303 restarted. After the second expiry of timer T303, the "Null" state is entered.

A TA receiving the SETUP message must send a CONNect message and enter the "Active" state if able; otherwise, it must send a RELease COMPlete message and enter the "Null' state.

When the initiating TA receives the CONNect message, it must stop timer T303, and enter the "Active" state.

4.5.2 *Logical link clearing*

Either TA may request to clear a logical link by sending a RELease message, setting timer T308, and entering "Release Request" state.

When a TA receives a RELease message, it must release the logical link, send a RELease COMPlete message, release the call reference, and enter the "Null" state.

When the TA initiating a RELease receives RELease COMPlete message, it must stop timer T308, release the logical link, release the call reference, and enter the "Null" state.

If the TA initiating the RELease does not receive a RELease COMPlete message before the first expiry of timer T308, the RELease message must be retransmitted and timer T308 restarted. If RELease COMPlete message is not received before timer T308 expires for the second time, the TA must release the call reference and enter the logical link into the "Null" state.

If both TAs simultaneously request to clear the same logical link by sending RELease messages, both must stop timer T308, release the logical link, release the call reference, and enter the "Null" state.

ANNEX A

(to Recommendation V.120)

Mappings of V.24 circuits to DR, SR, and RR

This Annex describes mapping of V.24 circuits intended to provide proper operation with most DTEs.

A.1   *DR-data ready (bit 7)*

The DR bit maps according to DTE attachment as follows:

–   for sending DR-DR(S) state variable:

    –   indicates DTR-data terminal ready (Recommendation V.24 circuit 108/2) from DTE;

–   for receiving DR-DR(R) state variable: no mapping is required.

Note – Dropping DTR may be used by the TE2 to indicate to the TA to clear the logical link or call.

A.2   *SR-send ready (bit 6)*

The SR bit maps according to DTE attachment as follows:

–   for sending SR-SR(S) state variable;

    –   indicates request to send (RTS – Recommendation V.24 circuit 105) status from DTE;

–   for receiving SR-SR(R) state variable;

    –   drives receive line signal detect (RLSD – Recommendation V.24 circuit 109) to DTE;

    –   the received ST bit is also mapped to the send RR bit (i.e. SR(R) $\rightarrow$ RR(S)).

A.3   *RR-receive ready (bit 5)*

The RR bit maps according to DTE attachment as follows:

–   for sending RR-RR(S) state variable: no mapping is required;

–   for receiving RR-RR(R) state variable:

    –   drives ready for send (RFS – Recommendation V.24 circuit 106) to DTE.

APPENDIX I

(to Recommendation V.120)

TE1 application

The protocols and procefures defined in Recommendation V.120 may be used for data transport by compatible TE1s as well as terminal adapters (TAs). In the TE1 case, the interface at the R reference point is effectively replaced by a virtual interface within the TE1 to a higher layer entity. This appendix describes the application of Recommendation V.120 in TE1s.

I.1   *Asynchronous mode operation*

I.1.1   *Transmission onto the ISDN channel*

The B, F bits are set to "1", and the C1 and C2 bits in the header are set to "0". The data to be transmitted is segmented as required, and each segment is appended to the header before transmission.

If a BREAK is received from the next higher layer, a frame with the BR bit set to "1" in the header will be transmitted at the earliest opportunity following data queued for transmission.

I.1.2   *Reception from the ISDN channel*

Processing of received data is as follows, based on the values of the C1 and C2 bits in the header:

–   if the C1 and C2 bits are both set to "0", the received characters are forwarded to the next higher layer without error indication;

–   if the C1 bit is set to "1", then a parity error indication is forwarded to the next higher layer with the characters received; the parity error applies to the last character in the frame;

–   if the C2 bit is set to "1", then a stop-bit error is forwarded to the next higher layer with the characters received; the error occurred immediately following the last character in the frame.

If the BR bit is set to "1" in the header of the received frame, then a BREAK indication is forwarded to the next higher layer after all data queued has been forwarded.

I.2   *Synchronous mode operation*

The messages passed to and received from the higher layer include the HDLC address and control fields, but do not include HDLC flags, FCS or inserted "0"'s.

I.2.1   *Transmission onto the ISDN channel*

The message length is compared with N2xx. The message is processed depending on its length as follows:

–   if the message length is less than or equal to N2xx, then the entire message is appended behind the header and both in the B and F bits set to "1". The resulting message is then transmitted;

–   if the message length is greater than N2xx, the first N2xx octets are appended to the header, with the B bit set to "1" and the F bit set to "0". The resulting message is then transmitted;

  –   if the remaining portion of the message is greater in length than N2xx, the next N2xx octets are appended to the header, with both the B and F bits set to "0". The resulting message is then transmitted;

  –   if the length of the remaining portion of the message is less than or equal to N2xx, then the remaining portion of the message is appended to the header with the F bit set to "1" and the B bit set to "0". The resulting message is then transmitted.

The C1 and C2 bits are normally set to "0".

I.2.2   *Reception from the ISDN channel*

Any messages that were segmented at the transmit end are reassembled as indicated by the B and F header bits.

The header of a received frame will be checked for error conditions as follows:

–   if the "begin" segment bit is "1" and the previous segment did not have the "final" segment bit set to "1", then the previous message will be aborted;

–   if the "begin" segment bit is set to "0" and there is no message currently in process, the segment will be discarded;

–   if the C1 or C2 error bit is "1" with the "final" bit a "1", the message will be discarded.

If a frame is received with the BR bit set to "1" in the header, then the TE1 management entity will be notified of an HDLC idle condition sent from the far end. The HDLC idle condition is maintained until a frame is received with the BR bit in its header set to "0".

When a message has been reassembled it is passed to the next higher layer.

I.3   *Bit transparent mode operation*

I.3.1   *Transmission onto the ISDN channel*

The transmitting entity accepts data from the process using its services, segments the data into segments of length at most N2xx, and transmits that data within frame to its peer entity. The length of the data segments and the length of the transmitted interframe time fill are adjusted so that the average data transmission rate matches the rate selected during call establishment.

I.3.2   *Reception from the ISDN channel*

The receiving entity upon receiving a frame from its peer entity, checks the FCS and if the FCS is valid it passes any data contained in the frame to the process using its services. If the FCS is not valid the entity may, on an application specific basis, discard the data contained in the errored frame or pass that data, with or without error indication, to the process using the services of the entity.

I.4   *TE1 control state variable processing*

In TE1 applications, the six control state variable DR(S), SR(S), RR(S), DR(R), SR(R), and RR(R) are maintained as described in § 2.3.6, with the following meanings:

–   for sending DR – DS(S) state variable:

–   indicates that the sending TE1 is powered up and connected for communication;

–   for receiving DR – DR(R) state variable:

–   indicates that the sending TE1 (far end) is powered up and connected for communication;

–   for sending SR – SR(S) state variable:

–   indicates that the sending TE1 is ready to send frames;

–   for receiving SR – SR(R) state variable:

–   indicates that the sending TE1 (far end) is ready to send frames;

–   for sending RR – RR(S) state variable:

–   indicates that the sending TE1 is ready to receive frames;

–   for receiving RR – RR(R) state variable:

–   indicates that the sending TE1 (far end) is ready to receive frames.

The following sections describe the procedures for control state variable processing in a TE1 using V.120. Note that the control states in a TE1 as described above are essentially analogous to those in a TA as described in § 2.3.6. Thus, the TE1 control state variable processing described below is completely compatible with that described in § 2.6 for the TA.

I.4.1   *Control state variable initialization*

Whenever the protocol is initialized to start communications, the protocol entity will set the receive state variables (DR(R), SR(R), and RR(R)) to "0" and the send state variables to reflect the status of the TE1 as described above.

I.4.2   *Sending a control state information octet*

A control state information octet will be sent whenever a send control state variable changes. A send control state variable will change with a change to the state of the TE1 as described above. A frame containing the control state information octet will be sent following any queued data for the interface at the S/T reference point.

The control state information field is sent in the last frame assembled when the control state change occurs, or in a separate frame.

The contents of the control state information octet is set to the state of the corresponding send control state variables. DR is set to DR(S), SR is set to SR(S), and RR to RR(S).

I.4.3   *Receiving a control state information octet*

Upon receipt of a control state information octet, the control field is checked with the receive control state variables: DR to DR(R), SR to SR(R), and RR to RR(R). The receive control state variables are set to their received values.

If SR(R) was "0" and the SR bit in the received control state information octet is "1", notification is made to the TE1 management entity.

If SR(R) was "1" and the SR bit in the received control state information octet is "0", notification is made to the TE1 management entity consistent with one of the following:

–   if received data (from the peer entity) does not remain to be forwarded (no message in progress), then the control actions can occur immediately;

–   if received data (from the peer entity) is incomplete (e.g. in protocol sensitive mode the final frame is not received), then the incomplete message is forwarded with indication of incomplete message and the notification made to the TE1 management entity;

–   if received data (from the peer entity) is complete, the message is forwarded and the notification of the TE1 management entity occurs.

If RR(R) and the RR bit in the received control field differ, notification is made to the TE1 management entity.

If DR(R) was "0" and the RR bit in the received control field is "1", notification is made to the TE1 management entity.

If DR(R) was "1" and the DR bit in the received control field is "0", then notification is made to the TE1 management entity consistent with the following:

–   if received data from peer entity is incomplete, it is discarded;

– if received data from peer entity is a complete message, then it should be forwarded until completion prior to the control actions taking place.

APPENDIX II

(to Recommendation V.120)

Clock synchronization

Figure II-1/V.120 shows two DTE/DCE configurations and their respective clock synchronization.

Case 1 — Receive Clock tracks Transmit Clock via data or system synchronization.

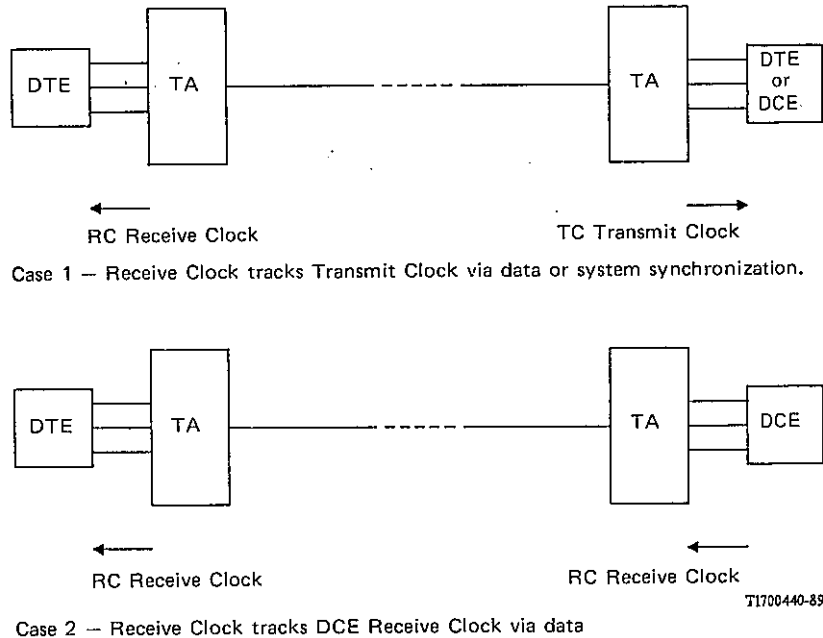Case 2 — Receive Clock tracks DCE Receive Clock via data

FIGURE II-1/V.120

Clock tracking

In the first case in Figure II-1/V.120, the TA is providing the clocks to the DTE or DCE. In the second case in Figure II-1/V.120, the DCE provides the Receive Clock to the TA for data to the DTE, and the TA at the DTE end provides the Receive Clock to the DTE for this same data.

There are three strategies which could be used for clock tracking. The first is to use the data buffers as clock variance buffers by having these buffers absorb the accumulated clock variance. In this case, no clock tracking is performed. If the buffer is completely depleted, and under-run occurs causing an error on the synchronous interface at the R reference point. Buffer space over-run can also happen, causing an error. However, the buffer accumulation or depletion to the point of over-run or under-run due to clock error is a slow process and is predictable in the worst case within the CCITT clock tolerance of 100 parts per million. The second strategy is for the clocks at both ends to be synchronized to the network. This strategy solves the problem but is not applicable to case 2 in Figure II-1/V.120. The third strategy is to monitor the buffer state as data is being received from the interface at the S/T reference point in the TA that is providing the Receive Clock to the DTE. This strategy monitors the rate of data at this interface by checking the buffer state when a new frame is received, and adjusts the clock speed accordingly.

For asynchronous applications, the first strategy (no clock correction) should be sufficient. For these applications a clock tolerance of +1/–2.5% is permissible, see Recommendation V.14. Under-run is not possible and buffering in the TA should be sufficient to avoid over-run.

For synchronous mode applications, appropriate buffer setup and management using no clock correction should be sufficient.

For bit transparent mode applications, continuous data does not allow for buffer resynchronization. For case 2 the frames are read into a buffer at the receiving TA and are clocked out to the TE2 by a time source derived in the TA.

If the data is clocked out at the rate transmitted, each frame will fill the receive buffer to precisely the same level. If the rate is low the fill level will increase and provide an indication that the clock rate must be increased and vice versa.

In some implementations, the clock adjustments might be in the form of repeated small adjustments in the phase of the clock, which would be derived from the ISDN network clock. Where the TE2 is tolerant of large phase steps the process may be simple.

APPENDIX III

(to Recommendation V.120)

**Bearer channel initialization procedures
for circuit switched applications**

To reduce the possibility of transmitting a frame to a TA that is not yet connected:

– a TA that receives a CONNect message from the network should always transmit a frame to initiate the connection, and

– a TA that receives a CONNect ACKnowledge message from the network should wait for T200 or until it receives a frame (whichever is earlier) before transmitting a frame.

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