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DATA COMMUNICATION OVER THE TELEPHONE NETWORK

ELECTRICAL CHARACTERISTICS FOR BALANCED DOUBLE-CURRENT INTERCHANGE CIRCUITS FOR INTERFACES WITH DATA SIGNALLING RATES UP TO 52 Mbit/s

ITU-T Recommendation V.12

(Previously "CCITT Recommendation")

FOREWORD

The ITU-T (Telecommunication Standardization Sector) is a permanent organ of the International Telecommunication Union (ITU). The ITU-T is responsible for studying technical, operating and tariff questions and issuing Recommendations on them with a view to standardizing telecommunications on a worldwide basis.

The World Telecommunication Standardization Conference (WTSC), which meets every four years, establishes the topics for study by the ITU-T Study Groups which, in their turn, produce Recommendations on these topics.

The approval of Recommendations by the Members of the ITU-T is covered by the procedure laid down in WTSC Resolution No. 1 (Helsinki, March 1-12, 1993).

ITU-T Recommendation V.12 was prepared by ITU-T Study Group 14 (1993-1996) and was approved under the WTSC Resolution No. 1 procedure on the 29th of August 1995.

NOTES

1. In this Recommendation, the expression "Administration" is used for conciseness to indicate both a telecommunication administration and a recognized operating agency.

2. The status of annexes and appendices attached to the Series V Recommendations should be interpreted as follows:

- an *annexes* to a Recommendation forms an integral part of the Recommendation;
- an *appendix* to a Recommendation does not form part of the Recommendation and only provides some complemetary explanation or information specific to that Recommendation.

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SUMMARY

This Recommendation specifies the electrical characteristics of a balanced digital interchange circuit, that may be employed when specified for the interchange of serial binary signals between Data Terminal Equipment (DTE) and Data Circuit-Terminating Equipment (DCE) or in any point-to-point interconnection of serial binary signals between data equipments. The balanced digital interchange circuit will normally be utilized on data and timing, or control circuits where the data signalling rate is up to a maximum limit of 52 Mbit/s.

Recommendation V.12

ELECTRICAL CHARACTERISTICS FOR BALANCED DOUBLE-CURRENT INTERCHANGE CIRCUITS FOR INTERFACES WITH DATA SIGNALLING RATES UP TO 52 Mbit/s

(Geneva, 1995)

1 Scope

This Recommendation specifies the electrical characteristics of a balanced digital interchange circuit, normally implemented in integrated circuit technology, that may be employed when specified for the interchange of serial binary signals between Data Terminal Equipment (DTE) and Data Circuit-Terminating Equipment (DCE) or in any point-to-point interconnection of serial binary signals between data equipments.

The interchange circuit includes a generator connected by a balanced interconnecting cable to a load consisting of a receiver and a termination. The electrical characteristics of the circuit are specified in terms of required voltage, and current values obtained from direct measurements of the generator and receiver components at the interchange points. The logic function of the generator and the receiver is not defined by this Recommendation, as it is application dependent. Minimum electrical requirements for the interconnecting cable are furnished.

The provisions of this Recommendation may be applied to the circuits employed at the interchange between equipments where information being conveyed is in the form of binary signals.

Typical points of applicability for this Recommendation are depicted in Figure 1.

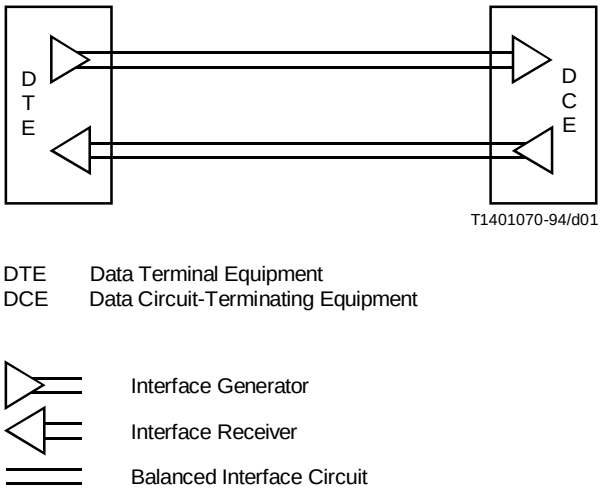


FIGURE 1/V.12

Applications of balanced digital interchange circuit

The balanced digital interchange circuit will normally be utilized on data and timing, or control circuits where the data signalling rate is up to a maximum limit of 52 Mbit/s.

2 References

The following ITU-T Recommendations and other references contain provisions which, through reference in this text, constitute provisions of this Recommendation. At the time of publication, the editions indicated were valid. All Recommendations and other referenced Standards are subject to revision, all users of this Recommendation are therefore encouraged to investigate the possibility of applying the most recent editions of the Recommendations and other references listed below. A list of currently valid ITU-T Recommendations is regularly published.

– ITU-T Recommendation V.11 (1993), *Electrical characteristics for balanced double-current interchange circuits operating at data signalling rates up to 10 Mbit/s*.

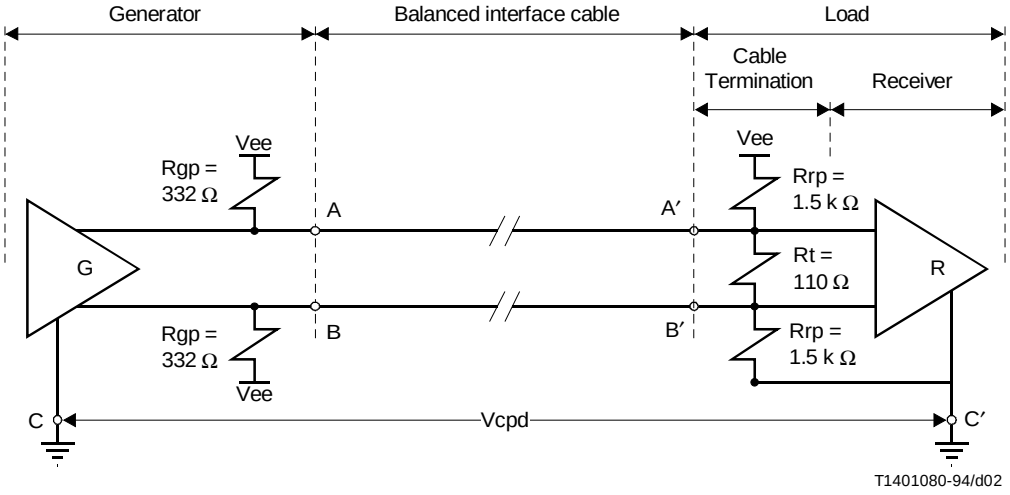
3 Definitions

For the purposes of this Recommendation, the following definition applies:

3.1 star (*): It represents the opposite input condition for a parameter. For example, the symbol Q represents the receiver output state for one input condition, while Q* represents the output state for the opposite input state.

4 Electrical characteristics

The balanced digital interchange circuit is shown in Figure 2. The circuit consists of three parts: the generator (G), the balanced interconnecting cable, and the load. The load is composed of a receiver (R) and a cable termination/fail-safe network. The electrical characteristics of the generator and the receiver are specified in terms of direct electrical measurements while the interconnecting cable is described in terms of its electrical characteristics.



G	Generator
Rgp	Generator Pull Down Resistor
R	Receiver
Rt	Termination Resistor
Rrp	Receiver Bias Resistor (Optional, Receiver Dependent)
Vcpd	Common Potential Difference
Vee	Negative Voltage Power Supply
A, B	Generator Interface Points
A′, B′	Receiver Interface Points
C	Generator Circuit Common
C′	Receiver Circuit Common

NOTE – All resistors ± 2%.

FIGURE 2/V.12

Balanced digital interchange circuit

4.1 Generator characteristics

The generator electrical characteristics are specified in accordance with the measurements illustrated in Figures 3 to 6 and described in 4.1.1 through 4.1.4. The generator circuit meeting these requirements results in a low impedance balanced source that will produce a differential voltage applied to the interconnecting cable in the range of 590 mV to 1500 mV.

The signalling sense of the voltages appearing across the interconnecting cable are defined as follows:

a) The A terminal of the generator shall be negative with respect to the B terminal for a binary 0 (SPACE or OFF) state.

b) The A terminal of the generator shall be positive with respect to the B terminal for a binary 1 (MARK or ON) state.

NOTE – The sense of data binary 0 (SPACE) and data binary 1 (MARK) are inverted from that specified in Recommendation V.11. The logic function of the generator and the receiver is beyond the scope of this Recommendation, and therefore is not defined.

4.1.1 **Open circuit measurement** (Figure 3)

For either binary state, the magnitude of the differential voltage (Voc or Voc*) measured between the two generator output terminals shall not exceed 1.5 V.

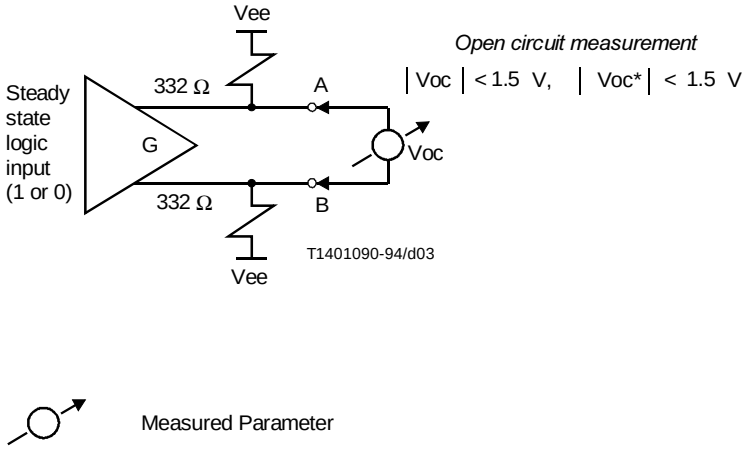


FIGURE 3/V.12

Open circuit measurement

4.1.2 **Test termination measurements** (Figure 4)

With a test load of the resistors shown in Figure 4, the magnitude of the differential output voltage (Vt), shall be 590 mV or greater. For the opposite binary state, the polarity of Vt shall be reversed (Vt*). The magnitude of the difference between Vt and Vt* shall be less than 100 mV. The value of the generator offset voltage (Vos), measured between the centre point of the test load and the generator circuit common shall be in the range of –1.6 V to 0 for either binary state. The magnitude of the difference of Vos for one binary state and Vos* for the opposite binary state shall be 100 mV or less.

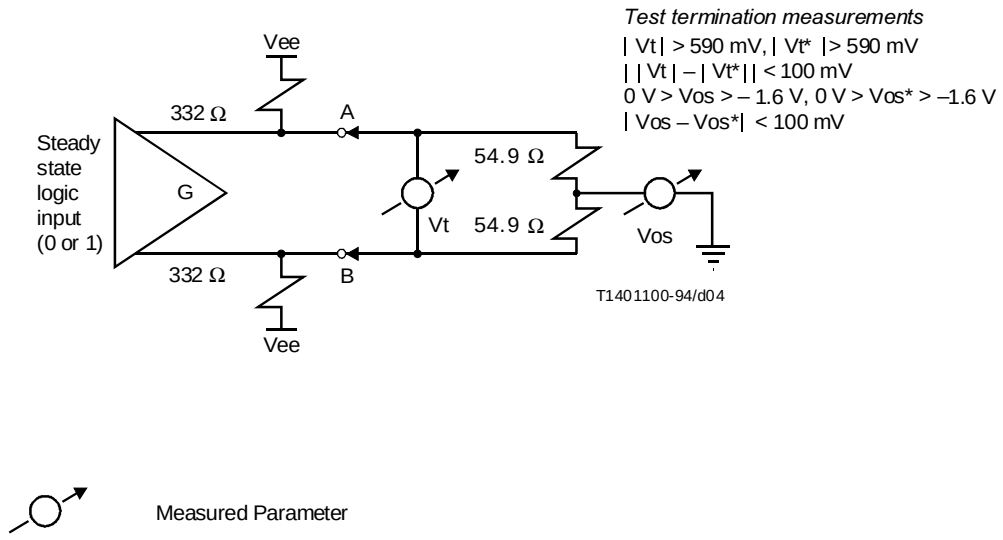


FIGURE 4/V.12

Test termination measurements

4.1.3 **Short-circuit measurement** (Figure 5)

With the generator output terminals short-circuited, the magnitude of the current (Ios) between the output terminals shall not exceed 50 mA for either state.

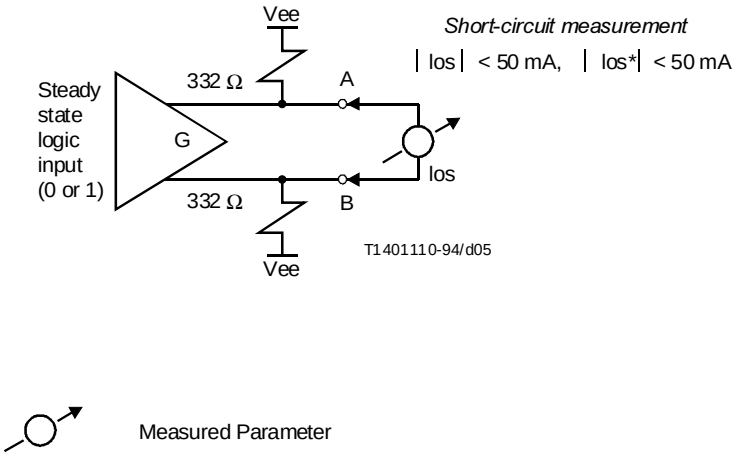
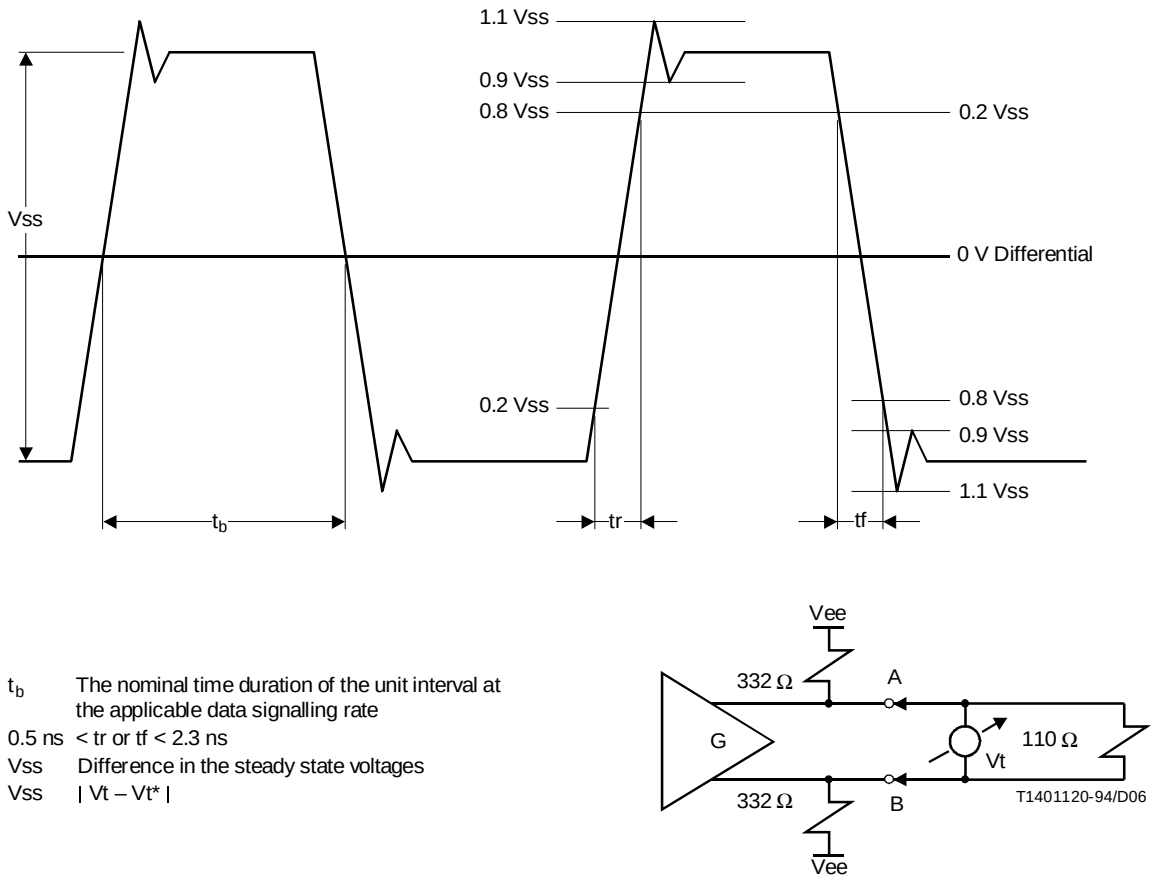


FIGURE 5/V.12

Short-circuit measurement

4.1.4 **Output signal waveform** (Figure 6)

During transitions of the generator output between alternating binary states (one-zero-one-zero, etc.), the differential voltage measured across the 110 Ω test load connected between the generator output terminals shall be such that the voltage monotonically changes between 0.2 and 0.8 of Vss within 0.5 ns to 2.3 ns. After achieving a steady state value, the signal voltage shall not vary more than 10% of Vss from that value, until the next binary transition occurs, and at no time shall the instantaneous magnitude of Vt or Vt* exceed 1500 mV nor be less than 590 mV. Vss is defined as the voltage difference between the two steady state values of the generator output.



t_b The nominal time duration of the unit interval at the applicable data signalling rate

0.5 ns < tr or tf < 2.3 ns

Vss Difference in the steady state voltages

Vss | Vt – Vt* |

FIGURE 6/V.12

Output signal waveform

4.2 Load characteristics

The load is composed of a receiver (R) and a termination/fail-safe network as shown in Figure 2. The electrical characteristics of a receiver without termination or fail-safe provision are specified in terms of measurements illustrated in Figures 7 to 9 and described in 4.2.1 and 4.2.2. A circuit meeting these requirements results in a differential receiver having a high input impedance, and a small input threshold between ± 150 mV.

4.2.1 **Input current-voltage measurements** (Figure 7)

With the voltage on one leg, Via (or Vib), ranging from –0.5 V to –2.0 V, while the voltage on the other leg, Vib (or Via), is held at –1.32 V, the resultant input current Iia (or Iib) shall be no greater than 350 µA. These measurements apply with the receiver's power supplies in both power-on and power-off conditions (as defined by the integrated circuit manufacturer). Note that these measurements are made with any termination resistor or fail-safe provision disconnected.

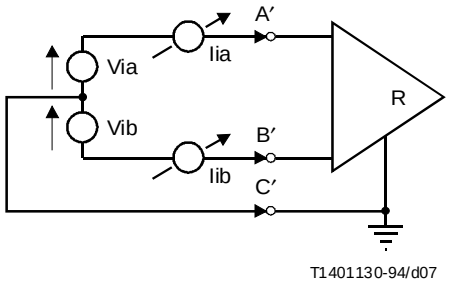


FIGURE 7/V.12

Receiver input current-voltage measurements

4.2.2 **Input sensitivity measurements** (Figure 8)

Over an entire input voltage range of –0.5 V to –2.0 V (referenced to receiver circuit common), the receiver shall not require a differential input voltage of more than 150 mV to correctly assume the intended binary state. Reversing the polarity of Vi shall cause the receiver to assume the opposite binary state. The receiver is required to maintain correct operation for differential input voltages ranging between 150 mV and 1.5 V in magnitude. Note that these measurements are made with any termination resistor or fail-safe provision disconnected.

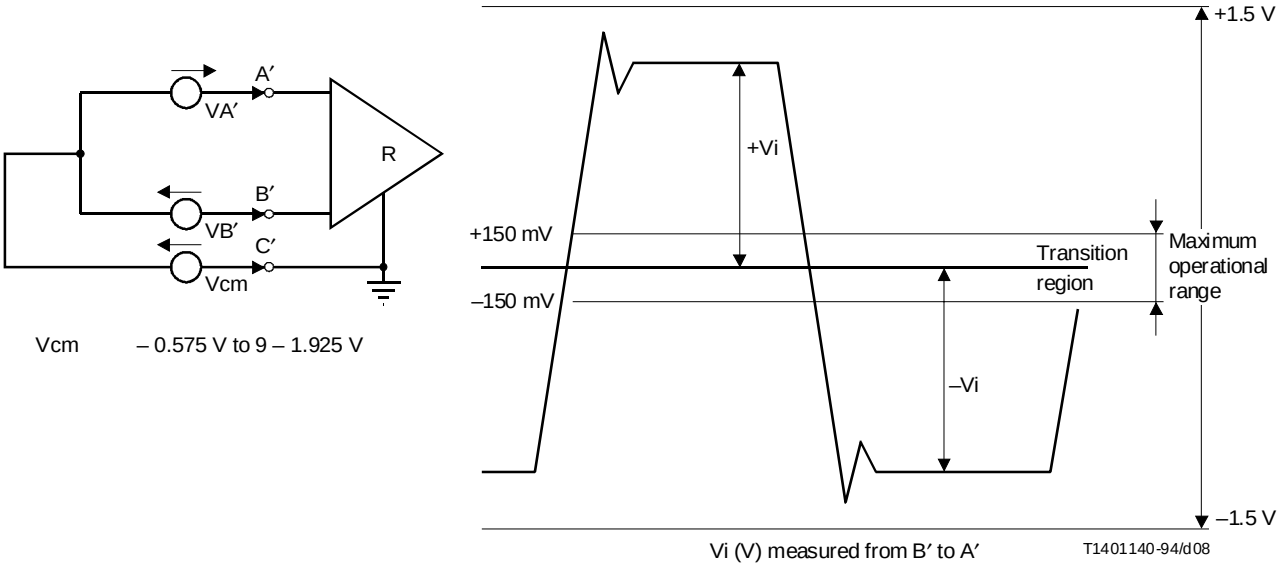
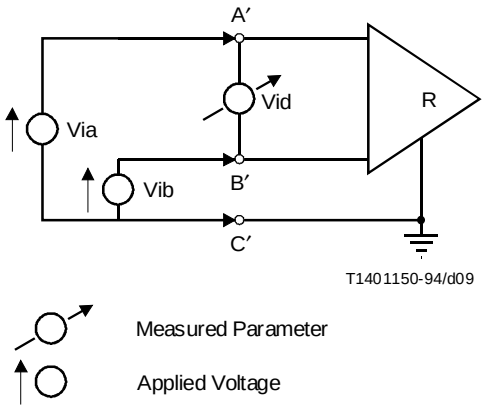


FIGURE 8/V.12

Input sensitivity measurements

Figure 9 illustrates the minimum and maximum operating voltages of the receiver. Note that the logic function of the receiver is not defined by this Recommendation.



NOTE Vcm = (Via + Vib)/2, Vid = Via – Vib.

Applied voltages		Resulting input voltage	Resulting common mode voltage
Via	Vib	Vid	Vcm
–0.50 V	–0.65 V	+0.150 V	–0.575 V
–0.65 V	–0.50 V	–0.150 V	–0.575 V
–0.50 V	–2.00 V	+1.50 V	–1.25 V
–2.00 V	–0.50 V	–1.50 V	–1.25 V
–1.85 V	–2.00 V	+0.150 V	–1.925 V
–2.00 V	–1.85 V	–0.150 V	–1.925 V

FIGURE 9/V.12

Receiver input sensitivity table

4.2.3 Cable termination

For all applications, the use of a cable termination is required. The recommended value is 110 Ω ± 2%. The termination resistor is connected across the cable at the load end of the cable, as close to the receiver input poles as possible.

4.2.4 Fail-safe operation

Other Recommendations and specifications using these electrical characteristics of the balanced digital interchange circuit may require that specific interchange circuits be made fail-safe to certain fault conditions. Such fault conditions may include one or more of the following:

1) open-circuited interconnecting cable;
2) generator in power-off condition.

When detection of one or more of the above fault conditions is required by specific applications, additional provisions are required in the load, and the following items must be determined and specified.

1) Which interchange circuits require fault detection?

2) What faults must be detected?

3) What action must be taken when a fault is detected?

The method of detection of fault conditions is application-dependent and is therefore not further specified. (See I.2.2.)

4.3 Interconnecting cable electrical characteristics

The cable shall consist of twisted pair conductors and have an overall shield. The two wires of each pair shall be connected to the same signal, one to the A/A′ and the other to the B/B′ signal poles.

Maximum single conductor DC Resistance (DCR) at 20 °C	3.5 Ω
Differential Impedance at 50 MHz	110 Ω ± 11 Ω
Maximum Signal Attenuation at 50 MHz	4.5 dB
Mutual Capacitance within pair at 1 kHz	47.6 ± 6.5 pF/m
Propagation Delay maximum:	79 ns
Skew (pair-to-pair)	2.0 ns

See Appendix I.1.2 for further guidance on an example of an interconnecting cable.

5 Circuit protection

Balanced digital interchange generator and receiver devices, under either the power-on or power-off condition, complying to this Recommendation shall not be damaged under the following conditions:

a) generator open circuit;

b) short-circuit across the balanced interconnecting cable;

c) short-circuit to circuit common.

Appendix I

Guidelines for application

I.1 Example on an interconnecting cable

The following subclause provides further information to 4.3 and provides additional guidance concerning operational constraints imposed by the cable parameters of length and termination.

I.1.1 Length

The nominal length of cable separating the generator and the load is 15 metres.

I.1.2 Cable physical characteristics

The following physical characteristics apply to the cable:

Conductor:	0.08 mm^2, 7 strands of 0.13 mm, tinned annealed copper, nominal diameter 0.38 mm.
Insulation:	Polyethylene or polypropylene; 0.24 mm nominal wall thickness; 0.86 mm ± 0.025 mm outside diameter.
Foil Shield:	0.051 mm nominal aluminium/polyester laminated tape spiral wrapped around the cable core.
Braid Shield:	Braided 0.13 mm, tinned plated copper in accordance with 80% minimum coverage, in electrical contact with the aluminium of the foil shield.
Outside Diameter:	≤ 10.6 mm.

I.1.3 Cable termination

The characteristic impedance of twisted pair cable is a function of frequency, wire size and type as well as the kind of insulating materials employed. For example, the characteristic impedance of average 0.08 mm^2, copper conductor, plastic insulated twisted pair cable, to a 50 MHz sine wave will be approximately 110 Ω.

I.2 Examples of generators and receivers

I.2.1 ECL – Emitter coupled logic technology

Emitter Coupled Logic (ECL) families such as 10K, 10H, and 100K have been developed that meet the requirements of this Recommendation by a number of integrated circuit manufacturers. The 100K family is compensated for both Power Supply Voltage and Operating Temperature variations; offering constant thresholds and output levels over both ranges. Some other families are only Power Supply Voltage compensated. The 100K family also accepts a wide range of power supply voltages (Vee) from −4.2 V to −5.7 V.

I.2.2 Fail-safe biasing of receivers (Figure I.1)

In the event that the interchange cable is not present, the receiver must default to a known state. The method of fail-safe biasing is application and component specific, therefore is beyond the scope of this Recommendation.

External resistors can be used to bias the receiver's input into a known state (≥ 150 mV differential) for the case of the disconnected cable. For example, a 1.5 kΩ pull-up and pull-down resistor will bias the receiver to 177 mV, defaulting the receiver to an OFF state.

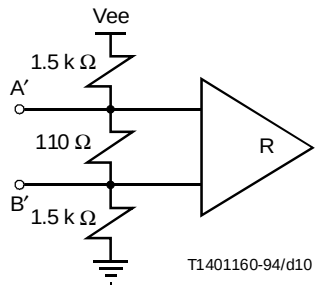


FIGURE I.1/V.12

Receiver fail-safe biasing

It should be noted that it is not necessary to use external resistors on all families of receivers. Some receiver integrated circuits have this feature internal to the integrated circuit.