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SERIES K: PROTECTION AGAINST INTERFERENCE

ITU-T K.131 – Soft error measures of field programmable gate arrays

ITU-T K-series Recommendations – Supplement 11

Supplement 11 to ITU-T K-series Recommendations

ITU-T K.131 – Soft error measures of field programmable gate arrays

Summary

Supplement 11 to ITU-T K-series of Recommendations describes soft error mitigation for field programmable gate arrays (FPGAs). FPGAs are a mainstream component of recent large-scale integrated circuits (LSIs), and many FPGAs are used as the main component in equipment for communication. First, this Supplement describes trends of soft error rates corresponding with the miniaturization of manufacturing process rules for semiconductors, and outlines mitigation techniques such as materials, physical layout and design tools that FPGA venders provide to users. Second, this Supplement discusses the design methodology of communication equipment, including consideration of reliability specification by using these mitigation measures. Finally, this Supplement discusses recent trends for mitigation measures for FPGAs.

History

Edition	Recommendation	Approval	Study Group	Unique ID*
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Introduction

The field programmable gate array (FPGA) is the mainstream component in recent large-scale integrated circuits (LSIs). The configuration data for determining the circuit configuration of an FPGA is stored in static random access memory (SRAM) so that arbitrary functions can be implemented. For that reason, an FPGA may be susceptible to soft errors which have a large influence on the system. Therefore, it is important to implement mitigation measures into the circuit design stage of an FPGA. This Supplement summarizes design examples of soft error mitigation measures for the SRAM-type FPGA.

Supplement 11 to ITU-T K-series Recommendations

ITU-T K.131 – Soft error measures of field programmable gate arrays

1 Scope

This Supplement describes: recent trends in field programmable gate arrays (FPGAs) which show increasing soft error rates; outlines device-level mitigation measures such as physical layout and software tools; and, provides guidance on mitigation measures to be taken when communication equipment is designed. This Supplement provides additional information in support of enhancing the understanding of [ITU-T K.131].

2 References

[ITU-T K.131] Recommendation ITU-T K.131 (2017), *Design methodologies for telecommunication systems applying soft error measures*.

3 Definitions

3.1 Terms defined elsewhere

None.

3.2 Terms defined in this Supplement

None.

4 Abbreviations and acronyms

This Supplement uses the following abbreviations and acronyms:

BRAM Block Random Access Memory (user memory)

CRAM Configuration Random Access Memory (configuration memory)

DRAM Dynamic Random Access Memory

ECC Error Correction Code

FinFET Fin Field Effect Transistor

FIT Failure in Time

FPGA Field Programmable Gate Array

IC Integrated Circuit

LSI Large-Scale Integrated Circuit

MR Maintenance Reliability

RoHS Restriction of Hazardous Substances

SEU Single Event Upset

SR Service Reliability

SRAM Static Random Access Memory

5 Conventions

None.

6 Mitigation measures of FPGAs

6.1 Soft error mitigation measures and transition of improvement contents and their effects

In general FPGAs, the static random access memory (SRAM) cell structure has been used for configuration random access memory (CRAM) (configuration memory) and block random access memory (BRAM) (user memory). Therefore, mitigation measures against soft errors have been required.

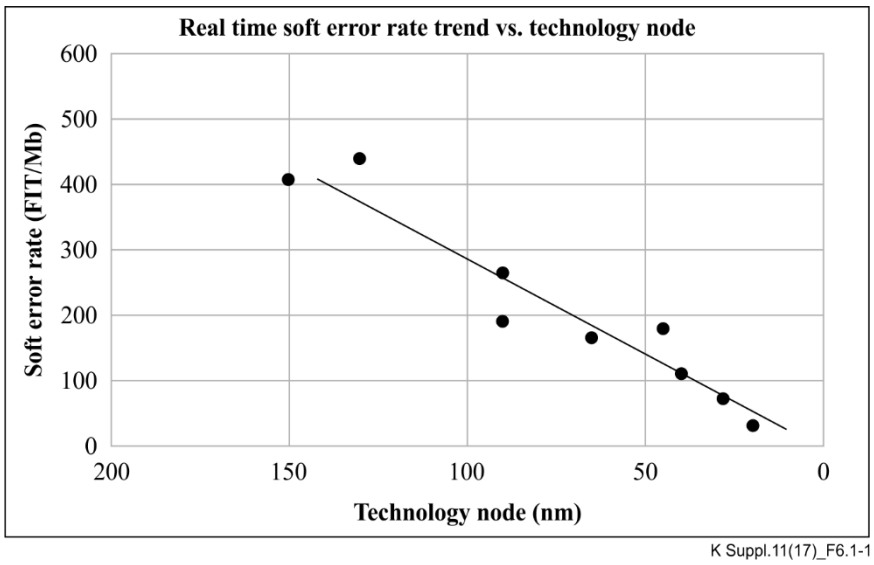
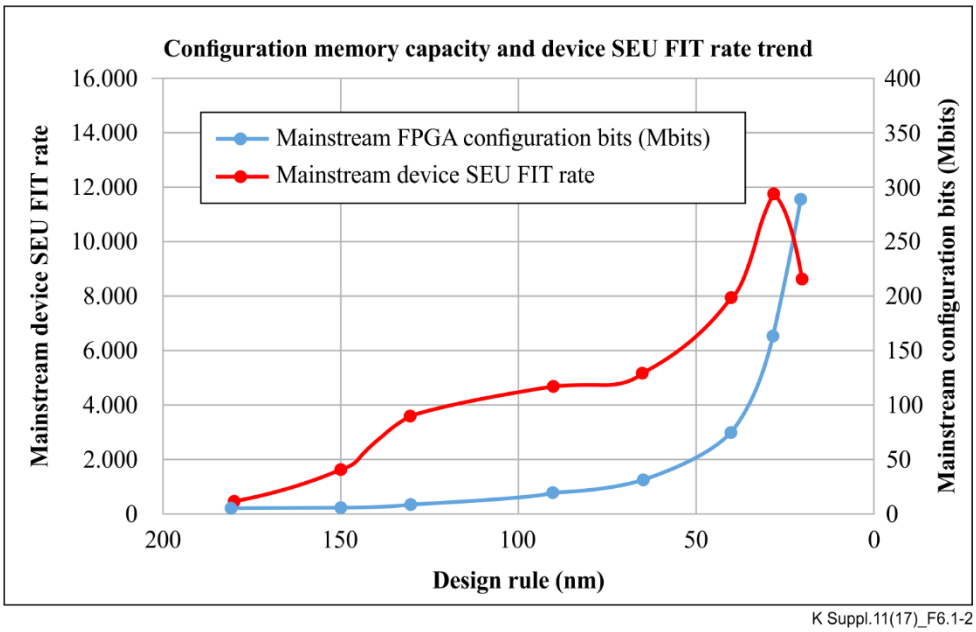


Figure 6.1-1 – Example of CRAM soft error rate vs. feature size (technology node) (See [b-Xilinx-UG116])



NOTE 1 – Single event upset (SEU)
NOTE 2 – Failure in time (FIT)

Figure 6.1-2 – Example of configuration memory capacity and device soft error rate trend (See [b-Xilinx-UG116] and [b-Xilinx-Site])

Figure 6.1-1 shows an example of soft error rate vs. feature size (technology node) in CRAM. As shown in Figure 6.1-2, the FPGA vendor has implemented various mitigation measures which show that the soft error rate has been improved after the 150 nm feature size.

This improvement is due to progress made in the investigation of the influence of soft errors on FPGAs as well as to the application areas of FPGAs, not only in various terrestrial systems but also in aerospace systems such as the Mars Rover etc. In addition, the circuit scale of the FPGAs is gradually increasing; this also drives the fact that aggressive measures against soft errors are required. (The graph in Figure 6.1-2 shows the configuration memory capacity of the maximum product under each feature size (design rule) and the device soft error rate trend based on published information.)

The major measures of soft error rate reduction/mitigation that have been applied until now are discussed in the following clauses.

6.1.1 Improvement example on semiconductor IC wafer process material

The boron compounds, which have been used as one of semiconductor integrated circuit (IC) wafer process materials, contain ^{11}B and ^{10}B. An alpha ray is generated when a thermal neutron strikes boron ^{10}B, which may then become a cause of soft errors. As soft error mitigation measures for semiconductor ICs then, minimizing ^{10}B content by purification of the material, or the introduction of semiconductor IC manufacturing techniques that do not use boron compounds have been developed. Similar measures have been attempted in FPGA products.

6.1.2 Improvement in semiconductor IC packaging materials

Regarding soft errors in semiconductor ICs, their occurrence at dynamic random access memory (DRAM) was initially considered as a problem. The main cause was alpha rays emitted from trace amounts of radioactive isotopes contained in the IC packaging materials. For this mitigation measure, the adoption of ceramic materials to reduce the radioactive isotope content, or the transition of filler in mold compounds from natural raw materials to materials produced from radioactive isotope-free materials, polyimides for alpha ray shielding, etc., have been addressed. Similar mitigation measures have been taken in IC packaging materials used in FPGAs; however, it is also necessary to consider the influence of alpha rays from alpha ray sources contained in solder bump materials and underfill materials used in flip chip packages. Thus, mitigation measures have been taken to reduce the alpha ray sources used for these materials, and ultra-low alpha ray (ULA) materials are used for advanced FPGAs today.

When soft error mitigation measures are considered in equipment development, the soft error rate caused by both neutron rays and alpha rays should be combined at the design stage. However, since an irradiation of accelerated alpha rays to the equipment is hard to implement for soft error evaluation at the equipment level, only neutron irradiation testing using an accelerator-driven neutron source is performed.

6.1.3 SRAM layout improvement

Soft error of SRAM

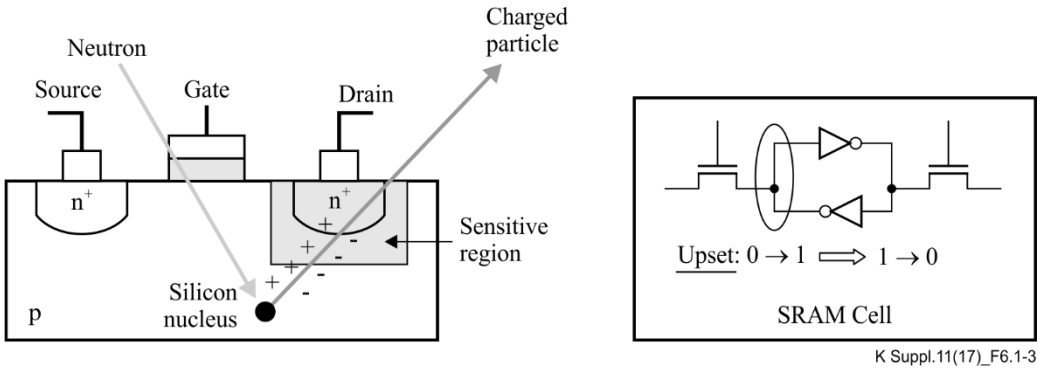


Figure 6.1-3 – Soft error mechanism due to neutron ray in SRAM (See [b-Xilinx-WP395])

As shown in Figure 6.1-3, soft errors in SRAM are caused by the influence to the nodes in the SRAM of the charged particles produced by the collision of a neutron in silicon atoms. Generally, soft error improvements in SRAM have been introduced through methods including suppressing logical inversion by increasing critical charge and increasing load capacitance of the corresponding node.

6.1.4 SRAM circuit layout improvement

With the progress of miniaturization of semiconductor ICs, the possibility arises that a plurality of adjacent SRAM cells generates soft errors at the same time (multi-bit error). If a multi-bit error occurs within the simultaneous read subject bits, there is a possibility that error detection and correction code generation cannot be performed properly. For this reason, using a more powerful error detection and correction code to correct a multi-bit error directly and adopting a bit interleave configuration which distributes the simultaneous read subject bits into multiple different words, have been become more common.

6.2 Soft error mitigation measures

To reduce the influence of soft errors, various mitigation measures are provided by FPGA vendors. The mitigation measures for BRAM and CRAM are explained, respectively, in this clause.

6.2.1 Soft error mitigation measures for BRAM

For BRAM used as user memory, data errors due to soft errors can be mitigated by using error correction code (ECC) functions which correct errors in read data.

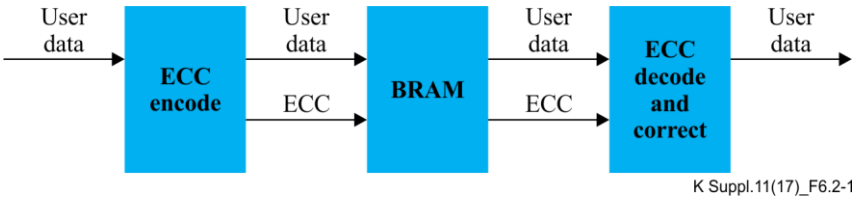


Figure 6.2-1 – Example of soft error mitigation measures for BRAM by ECC (See [b-Altera] and [b-Xilinx-UG473])

NOTE – The error correction function implemented in the BRAM corrects the read data, and the bit error of the memory in the BRAM cannot be corrected.

6.2.2 Soft error mitigation measures for CRAM

6.2.2.1 Variety of soft error reduction macro feature

FPGA vendors develop macros to reduce the impact of CRAM soft errors and provide them as part of their FPGA development tools. These soft error reduction macros have the following four functions:

1) CRAM soft error detection function;
2) CRAM soft error correction function;
3) CRAM classification function;
4) CRAM error injection function.

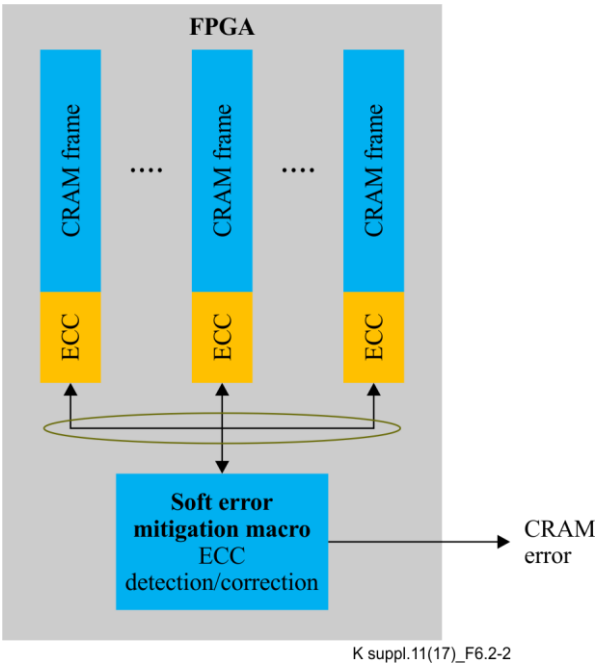


Figure 6.2-2 – Example of soft error reduction macro configuration (See [b-Altera] and [b-Xilinx-WP395])

6.2.2.2 CRAM soft error detection/correction function

The soft error detection/correction function is a function for detecting and correcting a bit error of the CRAM; these functions operate in the background of the circuit created by the user.

The soft error detection function of the CRAM detects that an error has occurred in any one of all of the bits of the CRAM. Since the number of bits of the CRAM can be significant, error detection cannot be performed simultaneously for all CRAM bits, but rather is performed by scanning each CRAM frame. (See Figure 6.2-2.)

The soft error correction function of the CRAM automatically overwrites the detected error bit with the restoration data and restores it to its original state.

As error correction completes in a short time immediately after detecting an error, that time can be almost ignored with respect to the detection scan time.

[Expected effect]

By enabling the soft error detection/correction function, if the scan period (T) of error detection is less than or equal to the duration time of the client signal interruption defined in the service reliability (SR) requirements, it can be excluded from the FIT number count of SR requirements. (See Figure 6.2-3).

NOTE 1 – Since the number of bits of the CRAM of the FPGA depends mainly on the number of logic of the FPGA, the scan period is not constant in each FPGA, and as the number of logic increases, the scan period may become longer.

In the current 28 nm and 20 nm feature size FPGAs, the nominal value of the scan period (T) for error detection is less than 100 ms. Since the scan period differs for each device of each FPGA vendor, it is necessary to check the scan period beforehand at the time of functional specification examination.

NOTE 2 – The soft error correction function of the CRAM is to correct the bit error of the CRAM, and there is a case that the error of the user circuit is not recovered even after the error of the CRAM is corrected.

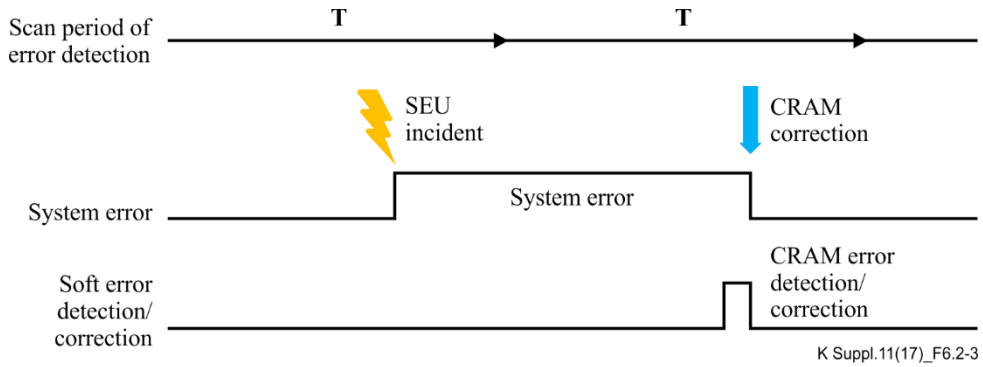


Figure 6.2-3 – Example of an operation when a soft error occurs

6.2.2.3 CRAM classification function

The classification function of the CRAM classifies the CRAM used for the whole user circuit or the CRAM used for some blocks in the user circuit in accordance with the vendor's own rules, as "used" CRAM, and it has capability to notify the classification result.

Using the design tool of the FPGA vendor enables the user to check the information on the CRAM error bits against the user circuit usage information which is related to each other in advance. The occurrence of the error bit is judged whether it matches to "used" CRAM or not, and the user is notified of the result.

[Expected effect]

By enabling the classification function, it is possible to distinguish whether the soft error has occurred in the "used" CRAM bit or not, so unnecessary error information can be reduced. Therefore, an effective use of this detection notification can be one of SR / maintenance reliability (MR) measures at the system level.

NOTE – When classification function is used, classification rules of CRAM classification function are different for each FPGA vendors, so conversion to FIT rate by soft error must follow classification specification.

CRAM classified as "used" by the classification function may include unused CRAM which may not affect user circuit operation in addition to the CRAM which is used for the user circuit. Therefore, even when a CRAM classified as "used" CRAM causes a soft error, it is not necessarily indicating a functional failure of the user circuit, so a fault rating taking account of other fault detection results may be effective in some cases.

When classification function is used, external ROM may be necessary in some cases, and it is necessary to use it per SR requirements.

6.2.2.4 CRAM error injection function

With the CRAM error injection function, errors can be inserted into the actual CRAM.

It is possible to check the CRAM error detection/correction/notification function at the system level by using the CRAM error injection function.

6.3 Example of execution for improving SR/MR

Examples of methods to improve SR/MR toward a desired reliability class are discussed in the following clauses.

6.3.1 Improvement in BRAM

By using the ECC circuit provided by the FPGA vendor, the soft error rate can be improved to nearly zero FIT. It is strongly recommended to use ECC circuit.

6.3.2 Improvement in CRAM

By using the soft error mitigation measures provided by the FPGA vendor, it is possible to reduce the soft error rate. Examples of methods for reducing the soft error rates are discussed in the following clauses.

6.3.2.1 Relationship on SR/MR system and direction of improvement

Soft errors affects network services and facility maintenance. An influence for SR/MR in system operation are as follows:

– it is subjected into the SR class when the network signal is continuously interrupted;

– it is not subjected into the SR class when the network signal is recovered within the time in the SR class;

– it is subjected into the MR class if any circuit packs and/or any IC device are not recovered in the network system;

– it is not subjected into the MR class when all circuit packs and/or all devices are automatically recovered.

6.3.2.2 Examples of SR/MR improvement measures

1) Examples of method for improving SR

The network signal interrupted time can be improved by using the following measures:

– error detection/correction function provided by FPGA vendor;

– classification function provided by FPGA vendor;

– strength of SEU tolerance at user logic (redundancy, etc.).

2) Examples of method for improving MR

The following methods can improve if any circuit packs and/or any IC device are not recovered in the network system:

– automatic FPGA reconfiguration and reinitialization;

– automatic circuit pack reinitialization.

6.3.2.3 Example SR/MR mitigation procedure

An example of mitigation procedures for improving FIT number of SR/MR is shown in Figure 6.3-1.

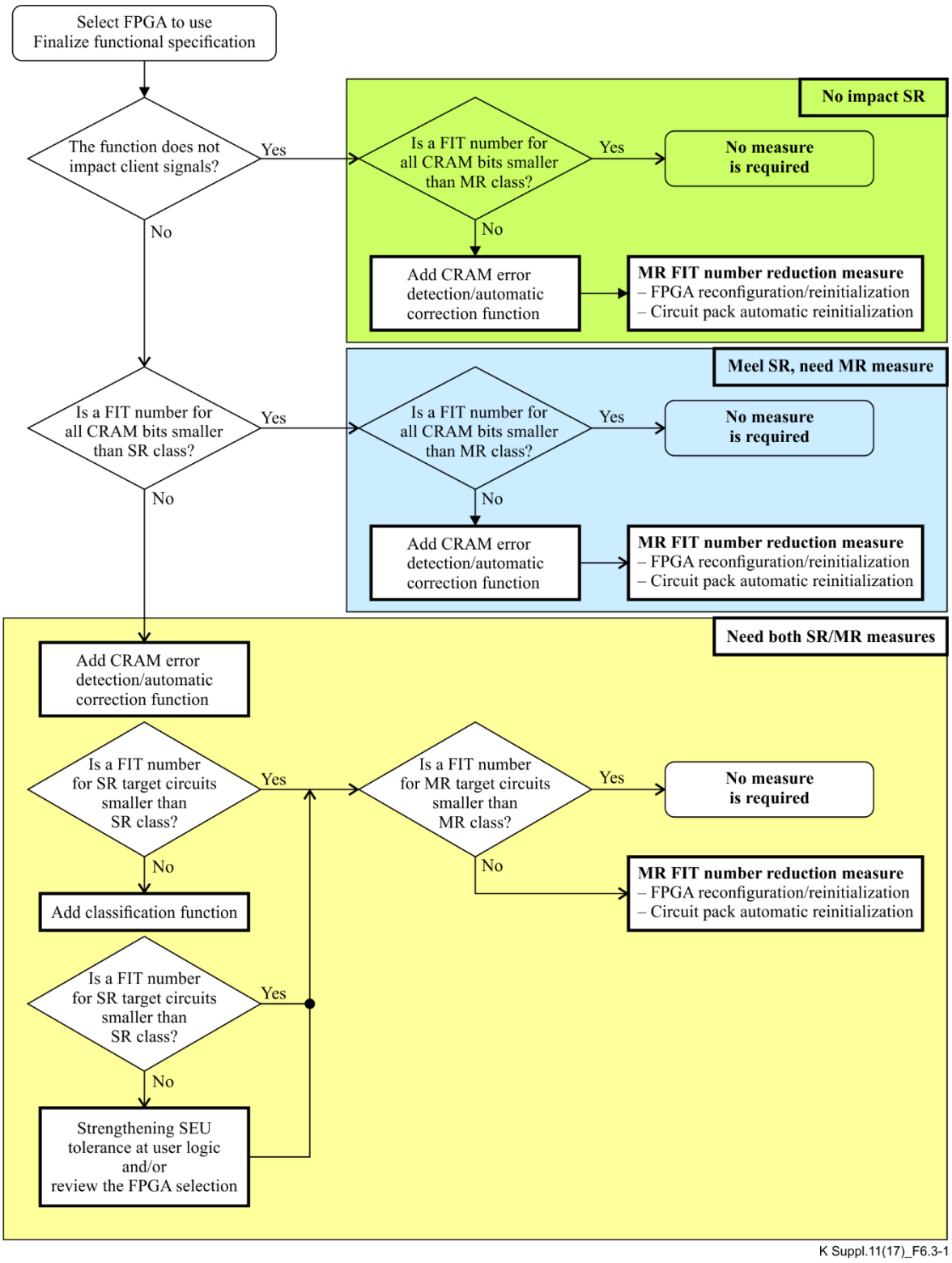


Figure 6.3-1 – Example of a method for improving SR/MR

6.4 Technology trends

6.4.1 Introduction of FinFET

The use of the Fin field effect transistor (FinFET) was started from 22 nm or 16 nm technology.

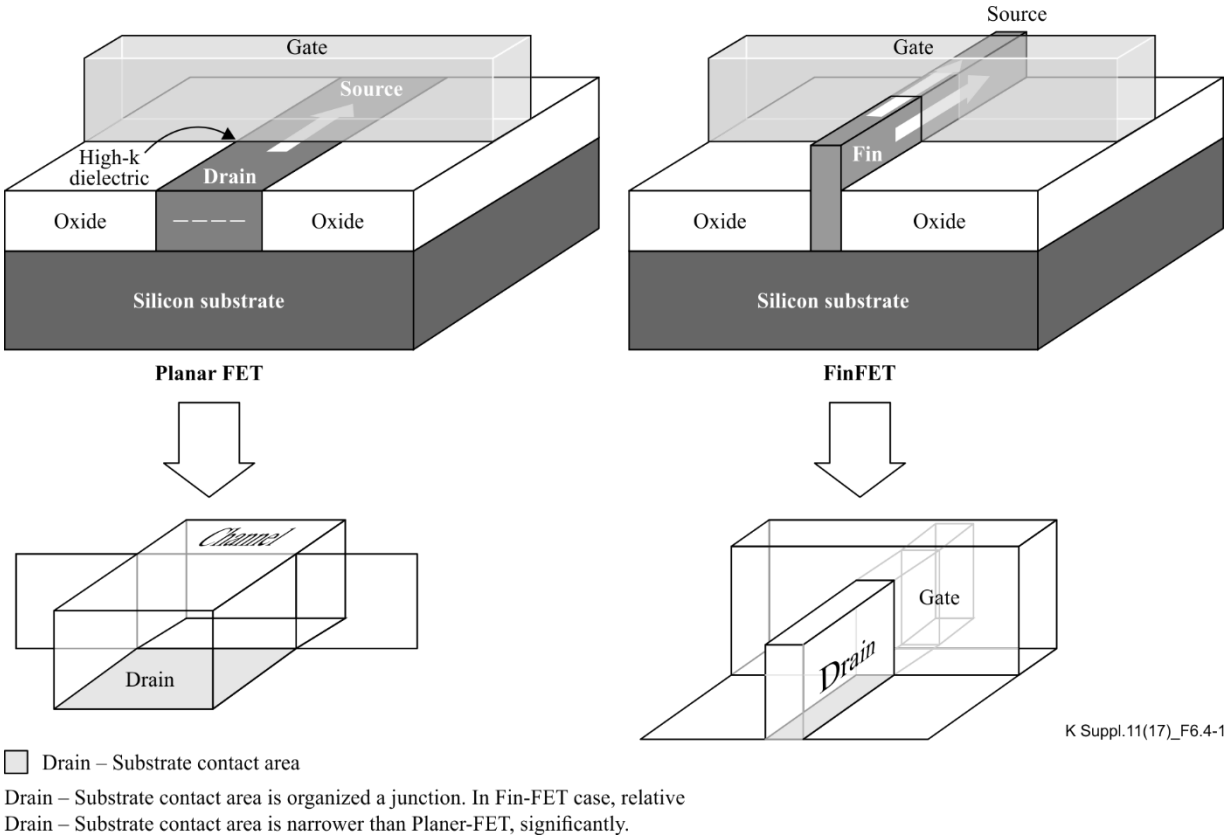


Figure 6.4-1 – Schematic of Planar FET and FinFET and schematic of drain – substrate contact part (See [b-Xilinx-WP472])

Although the Planar field effect transistor (FET) has been used conventionally, the relation between the capability of the FET and the drain–substrate junction area tends to relatively increase the contact area of the junction as the miniaturization of the semiconductor technology progresses, and the relative influence of soft error tends to increase. However, using the FinFET greatly reduces the contact area of the relative junction. (See Figure 6.4-1.) As a result, it is expected that an FPGA using FinFET can remarkably improve its soft error rate [FIT/Mb] together with various other improvements. (It has been confirmed that [FIT/Mb] of one FPGA product using 16 nm FinFET technology has been greatly improved compared with FPGAs using 20 nm Planar FET technology in just one generation prior.)

6.4.2 Semiconductor IC package trend

In recent years, in order to comply with restrictions on the use of hazardous substances (RoHS) compliance, lead-free IC packaging materials are being promoted, and lead-free solder bumps are beginning to be applied at mass production level in flip chip packages. Since solder bumps are disposed in the vicinity of the transistor circuit, removal of lead as an alpha ray emitting material is in a direction to reduce soft errors.

6.4.3 Trend of FPGA vendor provided circuits

An increase in the SRAM memory capacity as the scale of the FPGA product expands leads to an increase in time until a soft error detection circuit detects a CRAM soft error by CRAM area scan. As a reduction of the detection time by scan against this, it is possible to reduce the detection time in the whole device by mounting a plurality of detection circuits and operating the detection function in parallel.

In the error correction circuit after the detection, the correction time has been reduced and the multi-bit error correction capability has been improved. In the future, it is feared that expansion of multi-bit error due to miniaturization of transistors, but efforts are being made to eliminate concerns by improving multi-bit error correction capability with memory layout interleaving.

The error insertion circuit improves ease of use, improves from the existing single-bit error insertion to the function capable of multi-bit error insertion, and improves so that it can be evaluated according to more realistic neutron ray soft error event.

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