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SERI”ES K: PROTECTION AGAINST INTERFERENCE

Characteristics and ratings of silicon PN junction voltage clamping components used for the protection of telecommunication installations

Recommendation ITU-T K.129

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Characteristics and ratings of silicon PN junction voltage clamping components used for the protection of telecommunication installations

Summary

Recommendation ITU-T K.129 defines the basic electrical parameters to be met by silicon PN junction voltage clamping components used for the protection of telecommunication equipment or lines from surges. Examples of equipment include those located within a telecommunication centre, customer premise, access or trunk network. It is intended that this Recommendation be used for the harmonization of existing or future specifications issued by PN diode surge protective component manufacturers, telecommunication equipment manufacturers, administrators or network operators.

History

Edition	Recommendation	Approval	Study Group	Unique ID*
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Keywords

Avalanche breakdown, electrical characteristics, electrical ratings, fold-back, forward conduction, overvoltage protection, punch-through, surge protective component (SPC), test methods, Zener breakdown.

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1 Scope

Silicon PN-junction surge protective components (SPCs) are special silicon diodes designed to limit overvoltages and divert surge currents by a voltage clamping action. This Recommendation applies to silicon PN-junction SPCs used in surge protective devices (SPDs) and telecommunication equipment ports to provide overvoltage protection for installations during lightning surges and alternating current (AC) power faults, in accordance with [b-ITU-T K.11]. Telecommunication equipment port test levels and criteria are defined by [b-ITU-T K.20], [b-ITU-T K.21] and [b-ITU-T K.45], as appropriate and are supported by [b-ITU-T K.44] with test circuit details and application guidance. In conjunction, [ITU-T K.103] should be read as it explains the parameters measured or verified in this Recommendation.

The following PN-junction component technologies are covered:

– Zener breakdown;

– avalanche breakdown;

– fold-back;

– punch-through;

– forward conduction.

This Recommendation contains information on:

a) terminology;

b) letter and circuit symbols;

c) essential electrical ratings and characteristics;

d) rating verification and characteristic measurement;

f) mechanical requirements and identification.

2 References

The following ITU-T Recommendations and other references contain provisions which, through reference in this text, constitute provisions of this Recommendation. At the time of publication, the editions indicated were valid. All Recommendations and other references are subject to revision; users of this Recommendation are therefore encouraged to investigate the possibility of applying the most recent edition of the Recommendations and other references listed below. A list of the currently valid ITU-T Recommendations is regularly published. The reference to a document within this Recommendation does not give it, as a stand-alone document, the status of a Recommendation.

[ITU-T K.103] Recommendation ITU-T K.103 (2015), *Surge protective component application guide – Silicon PN junction components*.

3 Definitions

3.1 Terms defined elsewhere

This Recommendation uses the following terms defined elsewhere:

3.1.1 acceptor [b-IEC IEV], definition 521-02-39: Imperfection in a crystal lattice which, when it is predominant, permits hole conduction by the acceptance of electrons.

3.1.2 ambient temperature [b-IEC TR 62240-1]: Temperature of the environment in which a semiconductor component is operating.

3.1.3 avalanche breakdown (of a PN junction) [b-IEC IEV], definition 521-05-07: Breakdown that is caused by the cumulative multiplication of charge carriers in a semi-conductor under the action of a strong electric field which causes some carriers to gain enough energy to liberate new hole-electron pairs by ionization.

3.1.4 avalanche voltage [b-IEC IEV], definition 521-05-08: Applied voltage at which avalanche breakdown occurs.

3.1.5 bidirectional transistor [b-IEC IEV], definition 521-04-49: Transistor which has substantially the same electrical characteristics when the terminals normally designated as emitter and collector are interchanged.

3.1.6 bipolar junction transistor [b-IEC IEV], definition 521-04-47: Transistor having at least two junctions and whose functioning depends on both majority carriers and minority carriers.

3.1.7 breakdown (of a reverse-biased PN junction) [b-IEC IEV], definition 521-05-06: Phenomenon, the initiation of which is observed as a transition from a state of high dynamic resistance to a state of substantially lower dynamic resistance for increasing magnitude of reverse current.

3.1.8 breakdown voltage, $V_{(BR)}$ [b-IEC 60747-2]: Voltage in the region where breakdown occurs.

3.1.9 case temperature [b-IEC 60747-1]: Temperature of a reference point, on or near the surface of the case.

3.1.10 conduction electron [b-IEC IEV], definition 521-02-14: Electron in the conduction band of a semiconductor, which is free to flow under the action of an electric field.

3.1.11 donor [b-IEC IEV], definition 521-02-38: Imperfection in a crystal lattice which, when it is predominant, permits electron conduction by the donation of electrons.

3.1.12 extrinsic semiconductor [b-IEC IEV], definition 521-02-08: Semiconductor in which charge carrier concentration depends upon impurities or other imperfections.

3.1.13 forward current, I_F [b-IEC 60747-2]: Current flowing through the diode in forward direction.

3.1.14 forward direction (of a PN junction) [b-IEC IEV], definition 521-05-03: Direction of current that results when the P-type semiconductor region is at a positive voltage relative to the N-type region.

3.1.15 forward recovery voltage, V_{FR} [b-IEC 60747-2]: Varying voltage occurring during the forward recovery time after instantaneous switching from zero or a specified reverse voltage to a specified forward current.

3.1.16 forward voltage, V_F [b-IEC 60747-2]: Voltage across the terminals which results from the flow of current in the forward direction.

3.1.17 hole conduction [b-IEC IEV], definition 521-02-18: Conduction in a semiconductor, in which holes in a crystal lattice are propagated through the lattice under the influence of an electric field.

3.1.18 Kelvin measurement [b-IEC 62624]: Four-wire electrical resistance technique that uses separate contacts for measuring voltage across a device from that used to apply a known current through the device.

NOTE 1 – This separation minimizes current flow through the voltage probes, which minimizes errors due to contact or lead resistance.

NOTE 2 – Used for characterization of materials with electrical resistances comparable to or lower than the leads and contacts.

3.1.19 lead temperature [b-IEC 60747-1]: Temperature of a reference point, on or near the surface of a specified component lead.

3.1.20 N-type semiconductor [b-IEC IEV], definition 521-02-09: Extrinsic semiconductor in which the conduction electron density exceeds the hole density.

3.1.21 peak pulse current (impulse discharge current) [b-IEC 61000-5-5]: Peak value of a specified current waveform.

3.1.22 PN junction [b-IEC IEV], definition 521-02-78: Junction between P and N type semiconductor materials.

3.1.23 P-type semiconductor [b-IEC IEV], definition 521-02-10: Extrinsic semiconductor in which the hole density exceeds the conduction electron density.

3.1.24 punch-through (between two PN junctions) [b-IEC IEV], definition 521-05-12: Contact between the space charge regions of two PN junctions as a result of widening of one or both of them.

3.1.25 reverse current, I_R [b-IEC 60747-2]: Current flowing through the diode when reverse voltage is applied.

3.1.26 reverse direction (of a PN junction) [b-IEC IEV], definition 521-05-04: Direction of current that results when the N-type semiconductor region is at a positive voltage relative to the P-type region.

3.1.27 reverse voltage, V_R [b-IEC 60747-2]: Constant voltage applied to a diode in the reverse direction.

NOTE – This term normally applies to the portion of the reverse characteristic before breakdown occurs.

3.1.28 s pace-charge region [b-IEC IEV], definition 521-02-79: Region in which the net charge density is not zero.

NOTE – The net charge is caused by electrons, holes, ionized acceptors and donors.

3.1.29 storage temperature [b-IEC 60747-1]: Temperature at which the device may be stored without any voltage being applied.

3.1.30 temperature coefficient of breakdown voltage αV_{BR} [b-IEC 61643-321]: Ratio of the change in breakdown voltage V_{BR} to changes in temperature.

NOTE – Expressed as either millivolts per degree Kelvin or per cent per degree Kelvin (mV/K or %/K).

3.1.31 thermal resistance [b-IEC IEV], definition 521-05-13: Quotient of the difference between the virtual temperature of the device and the temperature of a stated external reference point, by the steady-state power dissipation in the device.

3.1.32 total capacitance [b-IEC 60747-3]: Capacitance at the diode terminals, measured under specified bias conditions.

3.1.33 transient thermal impedance [b-IEC 60747-1]: Quotient of:

a) the change in temperature difference between two specified points or regions at the end of a time interval, and

b) the step-function change in power dissipation beginning at that time interval which causes the change in temperature difference.

NOTE – The term used in practice must indicate the two specified points or regions, for example, as in "junction-case transient thermal impedance". The use of the shortened term "transient thermal impedance" is permitted only if no ambiguity is likely to occur.

3.1.34 Zener breakdown (of a PN junction) [b-IEC IEV], definition 521-05-09: Breakdown caused by the transition of electrons from the valence band to the conduction band due to tunnel action under the influence of a strong electric field in a PN junction.

3.1.35 Zener voltage [b-IEC IEV], definition 521-05-10: Minimum voltage across a PN junction at which Zener breakdown occurs.

3.2 Terms defined in this Recommendation

This Recommendation defines the following terms:

3.2.1 clamping (limiting) voltage: Breakdown voltage developed across the diode at a specified impulse current.

NOTE – Normally the maximum value of clamping voltage is reported for the rated value of peak pulse current.

3.2.2 discrete (semiconductor) component: Semiconductor component that is specified to perform an elementary function and that is not divisible into separate components functional in themselves. (modified version of [b-IEC IEV], definition 521-04-02)

NOTE – There is no clear delimitation possible between discrete components and integrated circuits. In principle, a discrete component consists of a single circuit element only. However, a component sold and specified as a discrete component may internally consist of more than one circuit element.

3.2.3 fold-back breakdown (of a bidirectional bipolar junction transistor diode): Re-entrant breakdown characteristic caused by transistor action after the initiation of breakdown producing a region of negative dynamic resistance before reverting back to a low positive dynamic resistance condition.

NOTE – The negative resistance region and its voltage range is only pronounced for breakdown voltages in excess of about 20 V.

3.2.4 fold-back diode: Bidirectional bipolar junction transistor packaged with only the collector and emitter terminals made available.

3.2.5 punch-through voltage: Low-current peak voltage marking the start of the diode clamping characteristic.

NOTE – This punch-through diode term may also be applied to fold-back diodes.

3.2.6 semiconductor component: Component whose essential characteristics are due to the flow of charge carriers within a semi-conductor. (modified version of [b-IEC IEV], definition 521-04-01)

NOTE – The definition includes components whose essential characteristics are only in part due to the flow of charge carriers in a semiconductor but that are considered as semiconductor components for the purpose of specification.

3.2.7 (semiconductor) diode: Two-terminal semiconductor component having an asymmetrical voltage-current characteristic. (modified version of [b-IEC IEV], definition 521-04-03)

NOTE 1 – Unless otherwise qualified, this term usually means a device with the voltage-current characteristic typical of a single PN junction.

NOTE 2 – Voltage clamping diodes are normally classified by clamping phenomenon; Zener, avalanche, fold-back, punch-through and forward conduction. Acronyms such as ABD (avalanche breakdown diode), TVS (transient voltage suppressor) and SAD (silicon avalanche diode) may also be used.

3.2.8 snap-back voltage: Lowest voltage in the clamping characteristic after the punch-through voltage occurs.

NOTE – This punch-through diode term may also be applied to fold-back diodes.

3.2.9 terminal (of a semiconductor component): Conductive element provided for external connection. (modified version of [b-IEC IEV], definition 521-05-02)

3.2.10 total power dissipation: Rated (maximum) value of the power that can be continuously dissipation by the diode at a specified ambient, case or lead temperature without exceeding the maximum rated junction temperature.

3.2.11 virtual junction temperature, internal equivalent temperature (of a semiconductor component): Theoretical temperature which is based on a simplified representation of the thermal and electrical behaviour of the semiconductor device. (modified version of [b-IEC IEV], definition 521-05-14)

4 Abbreviations and acronyms

This Recommendation uses the following abbreviations and acronyms:

ABD Avalanche Breakdown Device

AC Alternating Current

DC Direct Current

ICT Information and Communication Technology

SAD Silicon Avalanche Diode

SPC Surge Protective Component

TVS Transient Voltage Suppressor

WEEE Waste Electrical and Electronic Equipment

5 Conventions

5.1 Letter symbols

The general rules and letter symbols of clause 4 of [b-IEC 60747-1] apply to this Recommendation. To indicate a limit or rated value, the letter symbol subscript appends $_{M}$ or $_{max}$ to indicate maximum and $_{min}$ to indicate a minimum.

C_{tot} Total capacitance

dI_F/dt Rate of forward current rise

$I_{(BR)}$ Breakdown current

I_F Forward current

I_{PP} Peak pulse current

I_{PP} Peak pulse current

I_R Reverse current

P_{PP} Maximum peak pulse power

P_{tot} Total power dissipation

$R_{th(j\text{-}a)}$ Thermal resistance junction to ambient

$R_{th(j\text{-}c)}$ Thermal resistance junction to case

$R_{th(j\text{-}l)}$ Thermal resistance junction to lead

T_a Operating ambient temperature

T_c Case temperature

T_J Virtual junction temperature, internal equivalent temperature

T_l Lead temperature

T_{stg} Storage temperature

$V_{(BR)}$ Breakdown voltage

$V_{(PT)}$ Punch-through voltage

$V_{(SB)}$ Snap-back voltage

V_C Clamping voltage

V_F Forward biased PN junction voltage

V_{FRM} Peak forward recovery voltage

V_R Reverse working voltage

V_{RWM} Stand-off or maximum reverse working voltage

$Z_{th(j\text{-}a)(t)}$ Transient thermal impedance, junction to ambient

$Z_{th(j\text{-}c)(t)}$ Transient thermal impedance, junction to case

$Z_{th(j\text{-}l)(t)}$ Transient thermal impedance, junction to lead

$\alpha V_{(BR)}$ Temperature coefficient of breakdown voltage $V_{(BR)}$

5.2 Component graphical symbols

5.2.1 General

This Recommendation uses the following SPC graphical symbols from [b-IEC 60617]:

5.2.2 Single PN-junction symbols

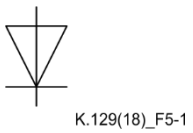

Figure 5-1 – Semiconductor diode, general symbol (symbol S00641)

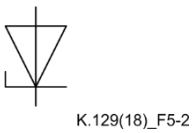

Figure 5-2 – Breakdown diode, unidirectional (symbol S00646)

5.2.3 Multiple PN-junction symbols

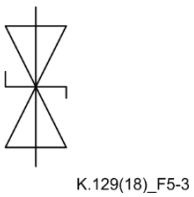

Figure 5-3 – Breakdown diode, bidirectional (symbol S00647)

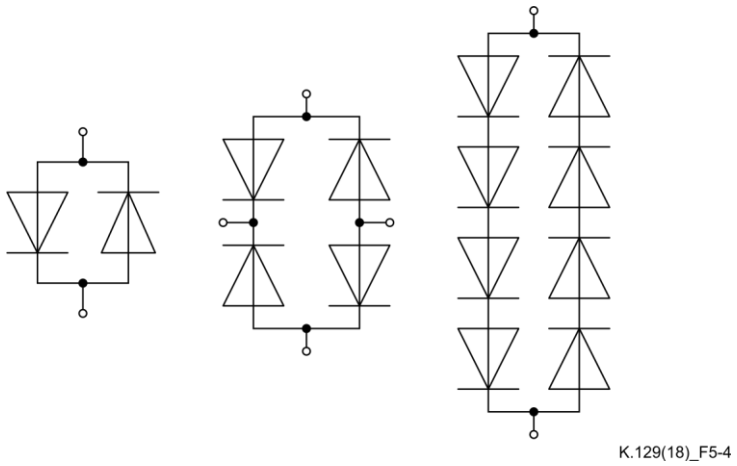

Figure 5-4 – Examples of diode arrays

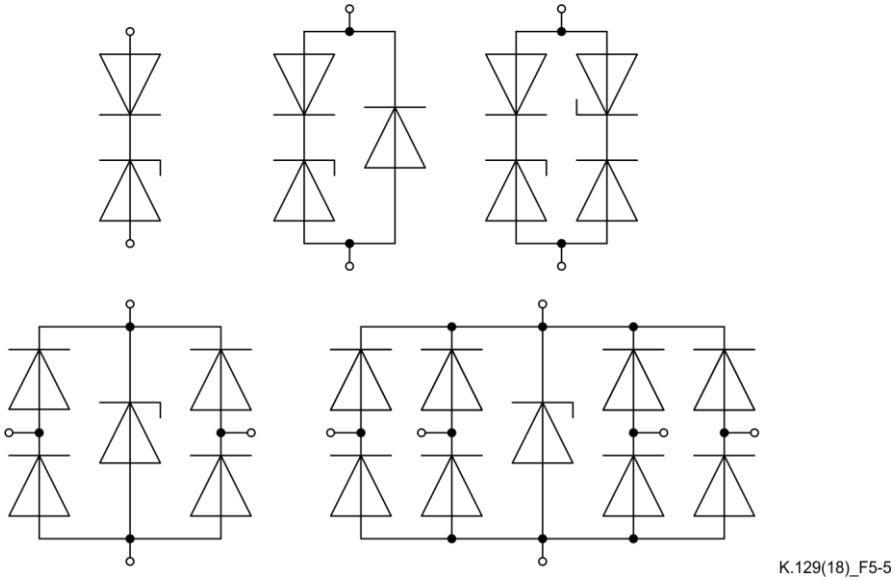

Figure 5-5 – Examples of breakdown diodes combined with diodes and diode arrays

6 Environments

The preferred climatic conditions are taken from the IEC classification of environmental conditions standards and the storage temperature ranges are taken from the IEC semiconductor devices standards.

6.1 Normal service conditions

This standard is for components mounted in stationary equipment and device installations that are weather-protected, see [b-IEC 60721-3-3]. The two preferred microclimates within the products are selected from [b-IEC 60721-3-9].

6.1.1 Normal microclimate

– ambient air temperature within the range of 0°C to 70°C;

– air pressure within the range of 80 kPa to 106 kPa;

– relative humidity within the range of 25% to 75%.

6.1.2 Extended microclimate

– ambient air temperature within the range of −40°C to 85°C;

– air pressure within the range of 70 kPa to 106 kPa;

– relative humidity 10% to 95%.

6.2 Storage temperature range, T_{stgmin} to T_{stgmax}

The temperatures over which a component can be stored without any voltage applied has the following preferred temperature ranges (selected from [b-IEC 60747-1] and [b-IEC 60749-1]):

a) 0°C to 125°C;

b) −55°C to 125°C;

c) −65°C to 150°C.

NOTE – In some cases the storage temperature range may be limited by the component shipping containers and not by the component itself.

6.3 Lead soldering temperature, T_{lmax}

Legislation, such as the waste electrical and electronic equipment (WEEE) directive and restriction of hazardous substances (RoHS) directive in the European Union, has accelerated the use of lead-free soldering. Removing the lead from solder results in increased soldering temperatures and component manufactures now routinely specify maximum soldering conditions in terms of component lead temperature, T_{lmax}, and temperature duration time, t_{lmax}, see [b-IEC 60068-2-20]. Examples are 260°C for 10 s and 260°C for 40 s.

7 Essential characteristics and ratings

7.1 General

For compatibility with general purpose breakdown diodes, the format of this clause follows that of [b-IEC 60747-3]. Many of the ratings and characteristics are required to be quoted at a temperature of 25°C and at one other specified temperature.

7.2 Electrical characteristics

7.2.1 PN-junction structure electrical characteristics

7.2.1.1 Single PN-junction

This classification covers forward biased diodes, reverse biased diodes, Zener breakdown diodes and avalanche breakdown diodes. Symmetrical breakdown diodes are made by the series connection of a PN-junction and a NP-junction giving a limiting voltage of $V_{(BR)} + V_F$. Such arrangements can be made in a single chip. The electrical characteristics and symbol identification for a forward conducting diode and a breakdown diode are shown in Figure 7-1 and Figure 7-2, respectively.

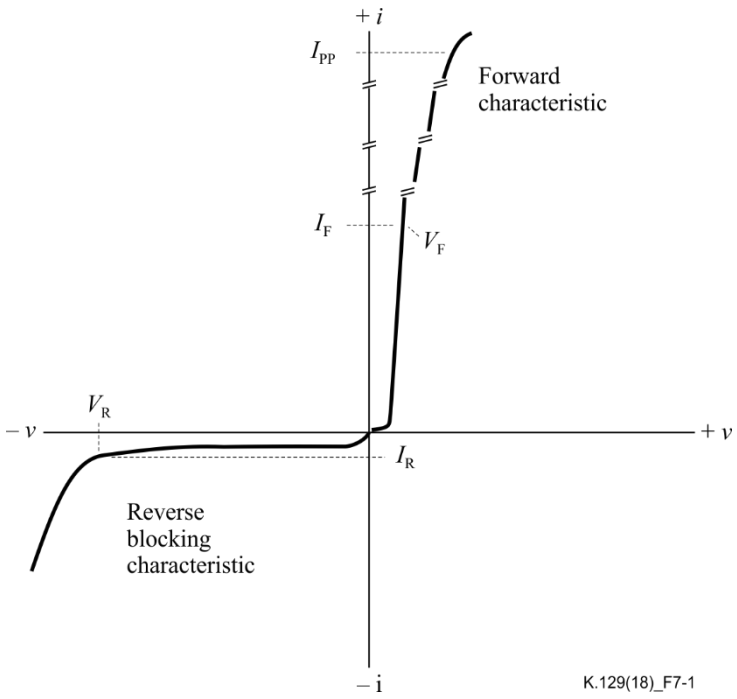

Figure 7-1 – Diode characteristic

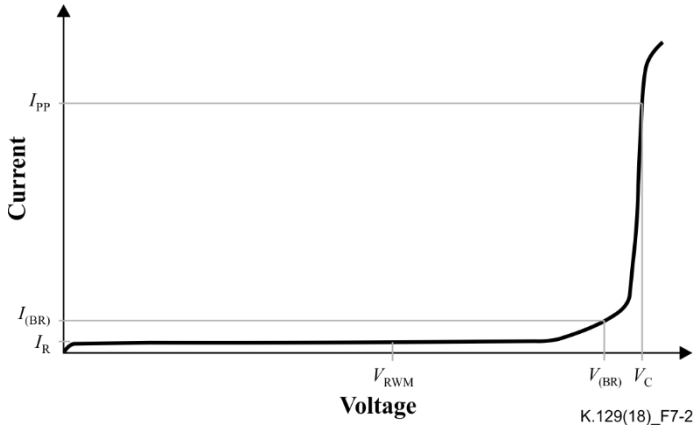

Figure 7-2 – Breakdown diode characteristic

7.2.1.2 Multiple PN-junction

This classification for transistor-like structures covers punch-through diodes and fold-back diodes. The voltage limiting characteristic for these types is strongly re-entrant. The electrical characteristic and symbol identification is shown in Figure 7-3.

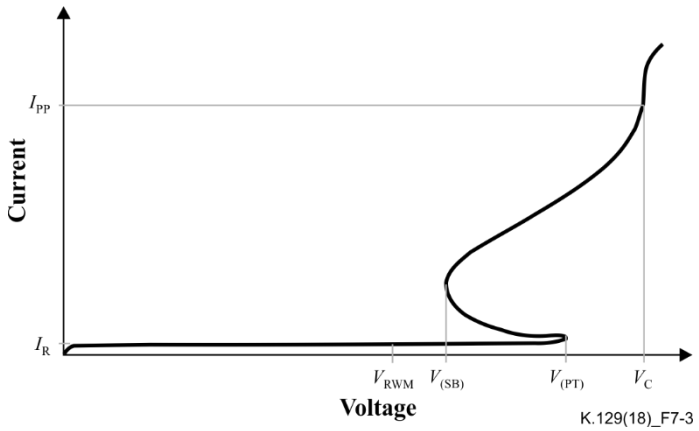

Figure 7-3 – Punch-through diode and fold-back diode characteristic

7.2.2 Reverse current, I_R

Maximum value at a specified reverse voltage.

7.2.3 Breakdown voltage, $V_{(BR)}$

Minimum value for a specified current.

7.2.4 Clamping voltage, V_C

Maximum value for specified current.

7.2.5 Punch-through voltage, $V_{(PT)}$

Maximum value.

7.2.6 Snap-back voltage, $V_{(SB)}$

Minimum value.

7.2.7 Forward biased PN junction voltage, V_F

Maximum value at specified forward current.

7.2.8 Total capacitance, C_{tot}

Maximum value for specified terminal and electrical conditions.

7.2.9 Thermal resistance (R_{th})

Maximum value or a graph of maximum total power dissipation as a function of temperature over the range of operating temperatures.

7.2.10 Thermal impedance (Z_{th})

A graph of thermal impedance as a function of time up to the thermal resistance value.

7.3 Thermal ratings

7.3.1 Storage temperature (T_{stg})

Minimum and maximum values.

7.3.2 Operating ambient temperature (T_a)

Minimum and maximum values.

7.3.3 Lead soldering temperature, T_l

T_{lmax}, and temperature duration time, t_{lmax}.

7.3.4 Virtual junction temperature, internal equivalent temperature, T_J

Maximum value.

7.4 Electrical ratings

7.4.1 Peak pulse current, I_{PP}

Maximum value at a specified ambient or sink or case and virtual junction temperature.

7.4.2 Maximum peak pulse power, P_{PP}

Maximum value at specified current waveform.

7.4.3 Total power dissipation, P_{tot}

Where thermal resistance is not given in the characteristics, maximum total power dissipation as a function of temperature over the range of operating temperatures shall be given.

8 Measuring and test methods

8.1 Mounting and ambient conditions

For these tests, the component should be mounted as detailed in the product documentation. All room temperature electrical measurements, as well as recoveries followed by measurements, shall be carried out under the following conditions as recommended in clause 4, chapter 1 of [b-IEC 60749-1]:

– temperature: 20°C to 30°C;

– relative humidity: 25% to 75%, where appropriate;

– air pressure: 80 kPa to 106 kPa.

Referee tests shall be carried out under the following standard atmospheric conditions (see clause 4, chapter 1 of [b-IEC 60749-1]):

– temperature: 24°C to 26°C;

– relative humidity: 25% to 75%;

– air pressure: 80 kPa to 106 kPa.

8.2 Test circuits

8.2.1 Pulsed current

This circuit, shown in Figure 8-1, forces a current of defined polarity, amplitude and duration through the SPC under test. The SPC conduction voltage is digitally recorded at a defined time during the current pulse duration.

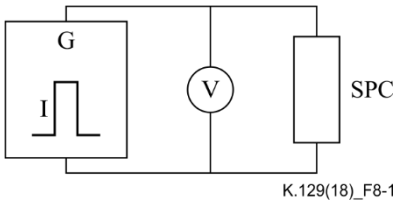

Figure 8-1 – Current pulse, voltage measurement circuit

8.2.2 Pulsed voltage

This circuit, shown in Figure 8-2, applies a voltage of defined polarity, amplitude and duration to the SPC under test. The SPC current is digitally recorded at a defined time during the voltage pulse duration.

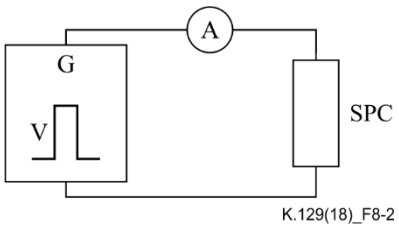

Figure 8-2 – Voltage pulse, current measurement circuit

8.2.3 Current ramp

This circuit, show in Figure 8-3, forces a current of defined polarity, amplitude and duration through the SPC under test. The SPC conduction voltage is digitally recorded at a defined time during the current pulse duration.

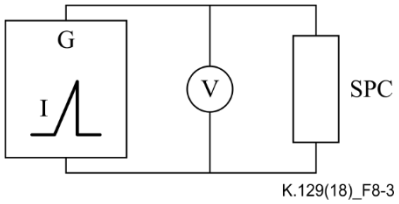

Figure 8-3 – Current ramp, voltage measurement circuit

8.2.4 Surge

This circuit, shown in Figure 8-4, forces a surge impulse current of defined polarity, amplitude and waveshape through the SPC under test. The SPC conduction voltage is digitally recorded at a defined event during the current impulse duration.

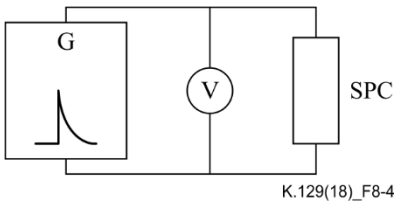

Figure 8-4 – Surge verification and voltage measurement circuit

8.2.5 Capacitance

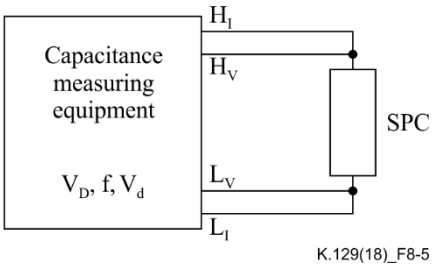

Figure 8-5 – Kelvin connected capacitance measurement

8.3 Measuring methods for electrical characteristics

8.3.1 Stand-off or maximum reverse working voltage, V_{RWM}

a) *Purpose*

To measure the reverse current of a diode under specified reverse voltage.

b) *Circuit diagram*

Figure 8-2.

c) *Circuit description and requirements*

Main elements are a voltage pulse generator of sufficient voltage and duration, a time or event programmable digital ammeter of sufficient sensitivity and the SPC under test.

d) *Measurement procedure*

Using the circuit of Figure 8-2, a voltage pulse of V_{RWM} is applied to the SPC, the current I_R is measured after the initial capacitive charging current component is negligible. The same technique can be used for a diode to measure I_R for a voltage pulse of V_R, see Figure 7-1.

e) *Specified conditions*

– ambient or case temperature (T_a, T_c);

– reverse voltage (V_{RMW} or V_R).

8.3.2 Breakdown voltage, $V_{(BR)}$

a) *Purpose*

To measure the breakdown voltage of a diode at a specified current.

b) *Circuit diagram*

Figure 8-1.

c) *Circuit description and requirements*

Main elements are a current pulse generator of sufficient current and duration, a time or event programmable digital voltmeter of sufficient sensitivity and the SPC under test.

d) *Measurement procedure*

Using the circuit of Figure 8-1 a current pulse of $I_{(BR)}$ is applied to the SPC, the voltage $V_{(BR)}$ is measured before any heating effects cause a change in the $V_{(BR)}$ value.

e) *Specified conditions*

– ambient or case temperature (T_a, T_c);

– breakdown current ($I_{(BR)}$).

8.3.3 Clamping voltage V_C

a) *Purpose*

To measure the clamping voltage of a diode at a specified current.

b) *Circuit diagram*

Figure 8-1 or Figure 8-4.

c) *Circuit description and requirements*

Main elements are a current pulse generator of sufficient current and duration (Figure 8-1) or a defined surge impulse generator (Figure 8-4), a time or event programmable digital voltmeter of sufficient sensitivity and the SPC under test.

d) *Measurement procedure*

Using the circuit of Figure 8-1 or Figure 8-4, a current pulse or impulse of I_{PP} is applied to the SPC, the maximum voltage V_C is measured after any transient effects have died out.

e) *Specified conditions*

– ambient or case temperature (T_a, T_c;

– peak pulse current (I_{PP});

– pulse duration used if appropriate;
– surge impulse used if appropriate.

8.3.4 Punch-through voltage $V_{(PT)}$

a) *Purpose*

To measure the peak low-current voltage of a diode. This applies to punch-through or fold-back diodes.

b) *Circuit diagram*

Figure 8-3.

c) *Circuit description and requirements*

Main elements are a current ramp generator of sufficient current and duration (Figure 8-3), a time or event programmable digital voltmeter of sufficient sensitivity and the SPC under test.

d) *Measurement procedure*

Using the circuit of Figure 8-3, a current ramp of sufficient amplitude to reach the $V_{(PT)}$ region is applied to the SPC. The voltage $V_{(PT)}$ is measured by programming the digital voltage recorder to measure the maximum voltage that occurs.

e) *Specified conditions*

– ambient or case temperature (T_a, T_c).

8.3.5 Snap-back voltage $V_{(SB)}$

a) *Purpose*

To measure the peak low-current voltage of a diode. This applies to punch-through or fold-back diodes.

b) *Circuit diagram*

Figure 8-3.

c) *Circuit description and requirements*

Main elements are a current ramp generator of sufficient current and duration (Figure 8-3), a time or event programmable digital voltmeter of sufficient sensitivity and the SPC under test.

d) *Measurement procedure*

Using the circuit of Figure 8-3, a current ramp of sufficient amplitude to reach the $V_{(SB)}$ region is applied to the SPC. The voltage $V_{(SB)}$ is measured by programming the digital voltage recorder to measure the minimum voltage that occurs after $V_{(PT)}$. The current ramp speed should be selected to avoid possible transient effects, if too fast, or heating effects, if too slow.

e) *Specified conditions*

– ambient or case temperature (T_a, T_c).

8.3.6 Forward biased PN junction voltage, V_F

a) *Purpose*

To measure the forward voltage of a diode at a specified current.

b) *Circuit diagram*

Figure 8-1 or Figure 8-4.

c) *Circuit description and requirements*

Main elements are a current pulse generator of sufficient current and duration (Figure 8-1) or a defined surge impulse generator (Figure 8-4), a time or event programmable digital voltmeter of sufficient sensitivity and the SPC under test.

d) *Measurement procedure*

Using the circuit of Figure 8-1 or Figure 8-4, a current pulse or impulse of I_{PP} is applied to the SPC, the forward voltage V_F is measured after any transient effects have died out and before any pulse heating effects cause a change in the V_F value.

e) *Specified conditions*

– ambient or case temperature (T_a, T_c);

– peak pulse current (I_{PP});

– pulse duration used if appropriate;

– surge impulse used if appropriate.

8.3.7 Peak forward recovery voltage, V_{FRM}

a) *Purpose*

To measure the peak forward recovery voltage of a diode at a specified rate of forward current rise (di_F/dt).

b) *Circuit diagram*

Figure 8-1.

c) *Circuit description and requirements*

Main elements are a current pulse generator of sufficient current (I_F) and specified rate of current rise (di_F/dt) (Figure 8-1), a time or event programmable digital voltmeter of sufficient sensitivity and the SPC under test.

d) *Measurement procedure*

Using the circuit of Figure 8-1, a current pulse is applied to the SPC, the maximum forward voltage V_{FRM} is measured after any transient effects have died out, see Figure 8-6.

e) *Specified conditions*

– ambient or case temperature (T_a, T_c);

– forward current (I_F);

– rate of forward current rise (di_F/dt).

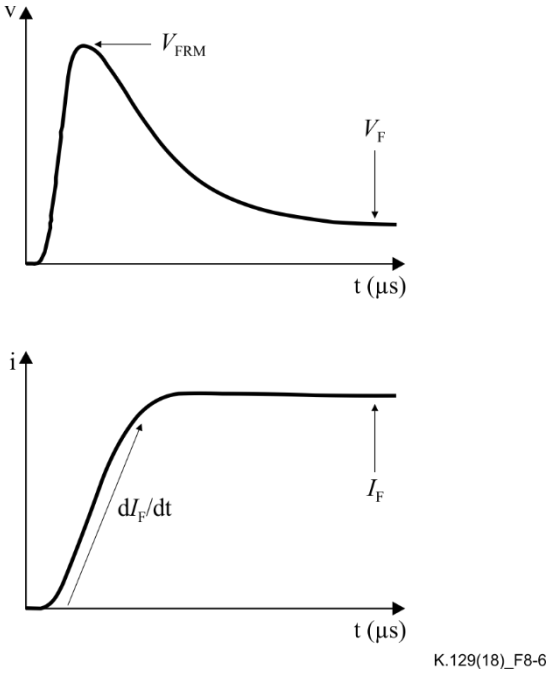

Figure 8-6 – Diode forward voltage and current waveforms versus time

8.3.8 Total capacitance C_{tot}

a) *Purpose*

To measure the capacitance of a diode at a specified direct current (DC) voltage (V_D), AC voltage (V_d) and frequency (f).

b) *Circuit diagram*

Figure 8-5.

c) *Circuit description and requirements*

Main elements are a Kevin connection capacitance measurement meter, the Kelvin voltage (H_V, L_V) and current (H_I, L_I) leads and the SPC under test.

d) *Measurement procedure*

Set the capacitance meter for the specified DC bias voltage (V_D), AC test voltage (V_d) and frequency (f). Measure the SPC capacitance. There may be a requirement to measure the capacitance at more than one value of DC bias voltage (V_D).

e) *Specified conditions*

- ambient or case temperature (T_a, T_c);
- DC bias voltage (V_D);
- AC test voltage (V_d);
- frequency (f).

8.4 Measuring methods for thermal characteristics

8.4.1 Introduction

The measurement of thermal resistance and transient thermal impedance is based on the use of a temperature-sensitive parameter of the semiconductor as an indicator of virtual junction temperature (T_J). The forward voltage (V_F) of a diode, at a small percentage of rated current, can be used as the temperature-sensitive parameter or the breakdown voltage ($V_{(BR)}$).

8.4.2 Transient thermal impedance $Z_{th(j\text{-}a)(t)}$ or $Z_{th(j\text{-}c)(t)}$ or $Z_{th(j\text{-}l)(t)}$

a) *Purpose*

To measure the transient thermal impedance ($Z_{th(j\text{-}a)(t)}$ or $Z_{th(j\text{-}c)(t)}$ or $Z_{th(j\text{-}l)(t)}$) of a SPC at a specified ambient (T_a), case (T_c), or lead (T_l) temperature.

b) *Circuit diagram*

Figure 8-7.

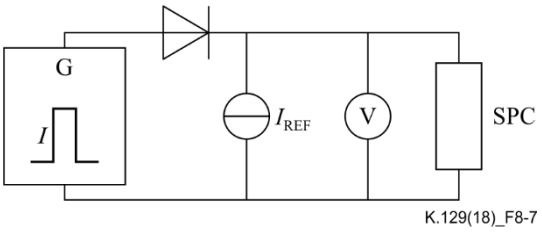

Figure 8-7 – Transient thermal impedance test circuit

c) *Circuit description and requirements*

Main elements are a reference current source (I_{REF}) for the temperature sensitive parameter, a high current pulsed source ($I >> I_{REF}$) for applying the power pulse to the SPC, a time or event programmable digital voltmeter of sufficient sensitivity and the SPC under test.

d) *Measurement procedure*

The I_{REF} current flows continuously. The current pulse I should be of sufficient amplitude that it causes a temperature rise of at least 50 K at the end of the pulse duration (t). The temperature rise is calculated from the difference in the reference parameter immediately before and immediately after the pulse divided by the reference parameter temperature coefficient. The transient thermal impedance is calculated from the calculated temperature rise divided by the product of the pulsed current and the average voltage measured during the pulse duration.

e) *Specified conditions*

– ambient or case or lead temperature (T_a, T_c, T_l);

– pulse duration (t).

8.4.3 Thermal resistance $R_{th(j-a)}$ or $R_{th(j-c)}$ or $R_{th(j-l)}$

The technique for thermal resistance ($R_{th(j-a)}$ or $R_{th(j-c)}$ or $R_{th(j-l)}$) is the same as transient thermal impedance, see clause 8.4.2, except the pulse duration must be long enough for the temperature rise to have stabilised at a constant value. Typically, the pulse duration to achieve thermal equilibrium is in the region of 100 s.

8.4.4 Temperature coefficient of breakdown voltage $V_{(BR)}$, $\alpha V_{(BR)}$

a) *Purpose*

To measure the temperature coefficient of breakdown voltage ($\alpha V_{(BR)}$) of a diode at a specified current. This approach can also be used for determining the temperature coefficient of forward voltage (αV_F).

b) *Circuit diagram*

Figure 8-1.

c) *Circuit description and requirements*

Main elements are a current pulse generator of sufficient current and duration, a time or event programmable digital voltmeter of sufficient sensitivity and the SPC under test. The SPC is mounted in a temperatures control oven

d) *Measurement procedure*

Using the circuit of Figure 8-1, a current pulse of $I_{(BR)}$ is applied to the SPC, the voltage $V_{(BR)}$ is measured before any heating effects cause a change in the $V_{(BR)}$ value. This measurement is repeated at several temperatures within the specified operating temperature range. The temperature coefficient between successive temperatures is the change in $V_{(BR)}$ divided by the change in temperature. Often $\alpha_{V(BR)}$ is quoted as a %/K obtained by multiplying the calculated *V/K* value by 100 and dividing by the average value of $V_{(BR)}$ between the two temperatures.

e) *Specified conditions*

– temperature range;

– breakdown current ($I_{(BR)}$).

8.5 Verification test methods for ratings (limiting values)

8.5.1 Peak pulse current, I_{PP}

a) *Purpose*

To verify the peak pulse current (I_{PP}) of a diode at a specified ambient temperature (T_a).

b) *Circuit diagram*

Figure 8-2 and Figure 8--4.

c) *Circuit description and requirements*

The Figure 8-2 circuit has a voltage pulse generator to apply the specified V_{RMW} or V_R to the SPC. A time or event programmable digital ammeter of sufficient sensitivity measures the I_R value. The Figure 8-4 circuit applies a specified surge impulse of I_{PP} to the SPC for a specified number of times and polarities.

d) *Measurement procedure*

Using the circuit of Figure 8-2, measure the selected SPC I_R value, see clause 8.3.1. Using the circuit of Figure 8-4 apply the specified surge impulse of I_{PP} to the SPC for the specified number of times and polarities. After the surge impulse testing is completed re-measure the selected SPC I_R value. The final value of I_R shall not have degraded to exceed the specified maximum limit I_R value.

e) *Specified conditions*

- ambient or case temperature (T_a, T_c);
- peak pulse current (I_{PP});
- surge impulse waveshape;
- surge impulse repetitions and polarities;
- maximum data sheet value of I_R.

8.5.2 Maximum peak pulse power P_{PP}

This parameter is fictive in that it is the product of two values that do not necessarily occur at the same instant of time. The maximum peak pulse power value (P_{PP}) is the product of the peak pulse current (I_{PP}) and the maximum value of clamping voltage (V_C).

8.5.3 Power dissipation, P_{tot}

The maximum power dissipation at a specified ambient temperature is the quotient of the difference between the maximum junction temperature (T_{JMAX}) and the specified ambient (T_a) and the thermal resistance value ($R_{th(j-a)}$).

9 Mechanical requirements and identification

9.1 Robustness of terminations

If applicable, the user shall specify a suitable test from [b-IEC 60068-2-21].

9.2 Solderability

Solder terminations shall meet the requirements of [b-IEC 60068-2-20].

9.3 Marking

Legible and permanent marking shall be applied to the surge protective component, as necessary, to ensure that the user can determine the following information by inspection:

a) manufacturer;

b) year of manufacture;

c) component number or code.

If requested and agreed, the customer's identification should be marked on each component.

NOTE 1 – The necessary information can also be coded.

NOTE 2 – When space is not sufficient for printing these data, it should be provided in the technical documentation after agreement between the manufacturer and purchaser.

9.4 Documentation

Documents shall be provided to the user so that from the information in clause 9.3, the user can determine the following additional information:

a) appropriate component parameters as set out in this standard;

b) component mounting requirements and processes;

c) ordering information.

The following information should be supplied by the user:

a) drawing giving all dimensions, finishes and termination details;

b) type or model;

c) quantity;

d) quality assurance requirements.

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