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SERIES G: TRANSMISSION SYSTEMS AND MEDIA, DIGITAL SYSTEMS AND NETWORKS

Optical transport network module framer interfaces

ITU-T G-series Recommendations – Supplement 58

ITU-T

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Supplement 58 to ITU-T G-series Recommendations

Optical transport network module framer interfaces

Summary

Supplement 58 to ITU-T G-series Recommendations describes several interoperable component-to-component multilane interfaces (across different vendors) to connect an optical module (with or without digital signal processor (DSP)) to a framer device in a vendor's equipment supporting 40G, 100G or beyond 100G optical transport network (OTN) interfaces.

Only the structure of the 11G, 28G or 56G physical lanes of the different OTN module framer interface (MFI) examples is provided in this Supplement. For their electrical characteristics, the OIF-CEI IA specifications can be used.

This Supplement relates to Recommendation ITU-T G.709/Y.1331.

History

Edition	Recommendation	Approval	Study Group	Unique ID*
2.0	ITU-T G Suppl. 58	2017-06-30	15	11.1002/1000/13343

* To access the Recommendation, type the URL http://handle.itu.int/ in the address field of your web browser, followed by the Recommendation's unique ID. For example, http://handle.itu.int/11.1002/1000/11830-en.

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Supplement 58 to ITU-T G-series Recommendations

Optical transport network module framer interfaces

1 Scope

This Supplement describes multilane interfaces between an optical transport network (OTN) framer device and an optical module with or without digital signal processor (DSP) (module framer interface). The module framer interfaces (MFIs) described in this Supplement carry optical transport unit k (OTUk; k = 3, 4) or optical transport unit Cn (OTUCn) signals. Electrical parameters for these interfaces can use specifications provided in the relevant clauses of OIF CEI IA specifications.

2 References

[ITU-T G.652] Recommendation ITU-T G.652 (2009), *Characteristics of a single-mode optical fibre and cable*.

[ITU-T G.695] Recommendation ITU-T G.695 (2015), *Optical interfaces for coarse wavelength division multiplexing applications*.

[ITU-T G.709] Recommendation ITU-T G.709/Y.1331 (2016), *Interfaces for the optical transport network*.

[ITU-T G.709.1] Recommendation ITU-T G.709.1/Y.1331.1 (2017), *Flexible OTN short-reach interface.*

[ITU-T G.959.1] Recommendation ITU-T G.959.1 (2016), *Optical transport network physical layer interfaces*.

3 Definitions

None.

4 Abbreviations and acronyms

This Supplement uses the following abbreviations and acronyms:

DSP	Digital Signal Processor
FlexO	Flexible Optical Transport Network
FlexO-n	group of n bonded short-reach 100G FlexO interfaces that carry an OTUCn
FOIC	FlexO Interface
FOIC1.k	an individual short-reach 100G FlexO interface that is a group of k FlexO Lanes that carry one OTUC of an OTUCn
LD	Local Degrade
LLM	Logical Lane Marker
MFAS	Multi-Frame Alignment Signal
MFI	Module Framer Interface
OSDP	Optical Line DSP
OTL	Optical Transport Lane
OTLC.n	group of n Optical Transport Lanes that carry one OTUC of an OTUCn

OTLk.n	group of n Optical Transport Lanes that carry one OTUk
OTN	Optical Transport Network
OTU	Optical Transport Unit
OTUCn	Optical Transport Unit Cn
OTUk	Optical Transport Unit k
WDM	Wavelength Division Multiplexing

5 Conventions

Transmission order: The order of transmission of information in all the figures in this supplement is first from left to right and then from top to bottom. Within each byte, the most significant bit is transmitted first. The most significant bit (bit 1) is illustrated at the left in all the figures.

6 Introduction

This Supplement begins with some examples of first generation module framer interface (MFI) for OTU3 and OTU4 signals carried over multiple 11G electrical lanes (using OTL3.4 and OTL4.10 structures, respectively).

Then it describes some examples of second generation MFI for OTU4 and OTUCn signals carried over multiple 28G electrical lanes (using OTL4.4, OTLC.4, and FOIC1.4 structures, respectively). Note that in the case of an OTUCn signal, n OTLC.4 or n FOIC1.4 interface structures are used.

Finally, it describes an example of third generation MFI for OTUCn signal carried over multiple 56G electrical lanes (using FOIC1.2 structure). Note that n FOIC1.2 interfaces (FlexO-n group) are used to carry an OTUCn signal.

Users of this Supplement should not assume that possible MFIs are limited to the ones provided in clauses 7, 8 and 9.

7 Signal formats and rates carried over 11G electrical lanes

This clause describes some MFI structures using 11G physical lanes in order to carry 40G OTU3 or 100G OTU4 signals. The electrical characteristics of each 11G physical lane may comply with [b-OIF-CEI-03.1] CEI-11G-*x*R specifications.

7.1 OTL3.4 structure

The original purpose of the OTL3.4 interface, as defined in clause 8.1 and Annex C of [ITU-T G.709], was to enable the re-use of pluggable modules developed for Ethernet 40GBASE-R applications. Modules developed for [b-IEEE 802.3] 40GBASE-LR4 and 40GBASE-ER4 can have corresponding optical specifications for OTU3 interfaces with application codes C4S1-2D1 and C4L1-2D1, respectively, in [ITU-T G.695]. These modules have a four-lane wavelength division multiplexing (WDM) interface to and from a transmit/receive pair of [ITU-T G.652] optical fibres.

These pluggable modules use a four-lane electrical chip-to-module interface (XLAUI), whose specification is found in Annex 83B of [b-IEEE 802.3]. These modules include a simple retimer. This application of the OTL3.4 interface is found in Figure 7-1.

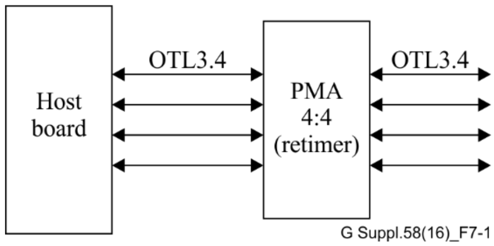

Figure 7-1 – Illustration of the application of an OTL3.4 interface

Another application example of the OTL3.4 interface is to connect a 40G OTN framer and optical line DSP (ODSP) devices in order to carry an OTU3 signal.

The bit rates of the OTL3.4 lanes are specified in [ITU-T G.709] and indicated in Table 7-1.

Table 7-1 – Bit rates of OTL3.4

OTL type	OTL nominal bit rate	OTL bit-rate tolerance
OTL3.4	4 × 255/236 × 9 953 280 kbit/s	±20 ppm
OTL3.4 lane	255/236 × 9 953 280 kbit/s	±20 ppm
NOTE – The nominal OTL3.4 lane bit rate is approximately: 10 754 603.390 kbit/s.		

7.2 OTL4.10 structure

The original purpose of the OTL4.10 interface, as defined in clause 8.1 and Annex C of [ITU-T G.709], was to enable the re-use of first generation pluggable modules developed for Ethernet 100GBASE-R applications. Modules developed for [b-IEEE 802.3] specified 100GBASE-LR4 and 100GBASE-ER4. They have corresponding optical specifications for OTU4 interfaces with the optical parameters as specified for the application codes 4I1-9D1F and 4L1-9C1F, respectively, in [ITU-T G.959.1]. Non-IEEE specified optical interfaces include [ITU-T G.695] application code C4S1-9D1F and [ITU-T G959.1] application code 4L1-9D1F. These modules have a four-lane WDM interface to and from a transmit/receive pair of [ITU-T G.652] optical fibres.

These first generation modules connect to the host board via a ten-lane electrical interface. The conversion between ten and four lanes is performed using a 100GBASE-R [b-IEEE 802.3] PMA sublayer as specified in clause 83 of [b-IEEE 802.3]. The specification of the ten-lane electrical chip-to-module interface (CAUI-10) is found in Annex 83B of [b-IEEE 802.3]. The application of the OTL4.10 interface is illustrated in Figure 7-2.

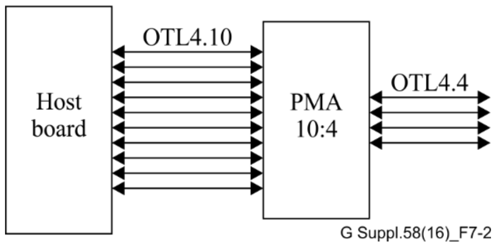

Figure 7-2 – Illustration of the original application of an OTL4.10 interface

Another application example of the OTL4.10 interface is to connect first generation 100G OTN framers with optical line DSP (ODSP) devices in order to carry an OTU4 signal.

Each OTL4.10 lane carries two bit-multiplexed logical lanes of an OTU4 as described in Annex C of [ITU-T G.709]. The logical lane format has been chosen so that the [b-IEEE 802.3] 10:4 PMA (gearbox) will convert the OTU4 signal between a format of ten lanes of OTL4.10 and four lanes of

OTL4.4. Each OTL4.4 lane carries five bit-multiplexed logical lanes of an OTU4 as described in Annex C of [ITU-T G.709].

The bit rate of an OTL4.10 lane is specified in Table 7-2.

Table 7-2 – Bit rates of OTL4.10

OTL type	OTL nominal bit rate	OTL bit-rate tolerance
OTL4.10	10 × 255/227 × 9 953 280 kbit/s	±20 ppm
OTL4.10 lane	255/227 × 9 953 280 kbit/s	±20 ppm
NOTE – The nominal OTL4.10 lane bit rate is approximately: 11 180 997.357 kbit/s.		

8 Signal formats and rates carried over 28G electrical lanes

This clause describes some MFI structures using 28G physical lanes in order to carry 100G OTU4 or B100G OTUCn signals. The electrical characteristics of each 28G physical lane may comply with [b-OIF CEI-03.1] CEI-28G-*x*R specifications.

8.1 OTL4.4 structure

The original purpose of the OTL4.4 interface, as defined in this clause and Annex C of [ITU-T G.709], was to enable the re-use of second (and beyond) generation pluggable modules developed for Ethernet 100GBASE-R applications. Modules developed for [b-IEEE 802.3] specified 100GBASE-LR4 and 100GBASE-ER4. They have corresponding optical specifications for OTU4 interfaces with the optical parameters as specified for the application codes 4I1-9D1F and 4L1-9C1F, respectively, in [ITU-T G.959.1]. Non-IEEE specified optical interfaces include [ITU-T G.695] application code C4S1-9D1F and [ITU-T G959.1] application code 4L1-9D1F. These modules have a four-lane WDM interface to and from a transmit/receive pair of [ITU-T G.652] optical fibres.

Most second generation (and beyond) pluggable modules use a four-lane electrical chip-to-module interface (CAUI-4), whose specification is found in [b-IEEE 802.3] Annex 83E. These modules include a simple retimer (as opposed to the 10:4 gearbox found in first generation modules). This application of the OTL4.4 interface is illustrated in Figure 8-1.

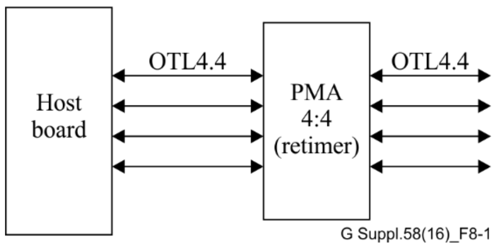

Figure 8-1 – Illustration of the original application of an OTL4.4 interface

Another application example of the OTL4.4 interface is to connect second generation multi-100G OTN framers with optical line DSP (ODSP) devices in order to carry independent OTU4 signals and to connect these framers with emerging line side optical modules.

Each OTL4.4 lane carries five bit-multiplexed logical lanes of an OTU4 as described in Annex C of [ITU-T G.709].

The bit rates of the OTL4.4 are specified in [ITU-T G.709] indicated in Table 8-1.

Table 8-1 – Bit rates of OTL4.4

OTL type	OTL nominal bit rate	OTL bit-rate tolerance
OTL4.4	4 × 255/227 × 24 883 200 kbit/s	±20 ppm
OTL4.4 lane	255/227 × 24 883 200 kbit/s	±20 ppm
NOTE – The nominal OTL4.4 lane bit rate is approximately: 27 952 493.392 kbit/s.		

8.2 OTLC.4 structure

In B100G OTN design, the interfaces between the B100G OTN framer and ODSP devices will support OTU4 and OTUCn signals. This interface benefits from a common interface format. The purpose of the OTLC.4 interfaces is to support such a common interface format based on the existing OTL4.4 format. These interfaces carry either four physical lanes of an OTU4 (i.e., OTL4.4) or OTUCn (i.e., OTLC.4). See Figure 8-2.

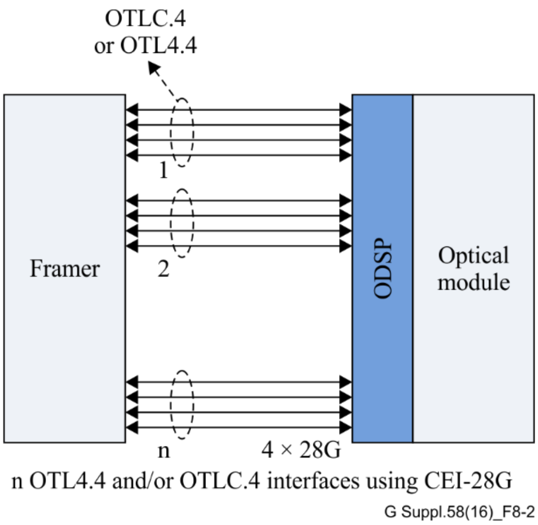

Figure 8-2 – Example applications of an OTL4.4/OTLC.4 interface

An OTUCn is split into n times OTUC and each OTUC frame is extended with 256 FEC columns at the end of the frame which contain a RS (255,239) FEC as specified for the OTUk in Annex A of [ITU-T G.709]. Each OTUC frame with RS (255,239) FEC therefore results in an octet-based block frame structure with four rows and 4080 columns, that is the same as an OTUk (k = 1,2,3,4) frame structure. This frame structure is scrambled as specified for the OTUk in clause 11.2 of [ITU-T G.709] and split into 20 5G OTLC logical lanes as per 5G OTL4 logical lane specification in Annex C of [ITU-T G.709]. 5G OTLC logical lanes are combined into four OTLC.4 physical lanes as per the OTL4.4 specifications in Annex C of [ITU-T G.709].

The third OA2 byte in each OTUC with RS (255,239) FEC frame is replaced by a logical lane marker (LLM) byte as per the OTL4.4 specifications in Annex C of [ITU-T G.709] to support the reordering of the 5G OTL4 and OTLC logical lanes within the scope of the 20 logical lanes in a 100G OTU4 or OTUC group.

OTL4.4 physical lanes do not support an OTU4 Identifier. Due to this, groups of four OTLx.4 (x = 4, C) physical lanes carrying one OTU4 or one OTUC instance have to be connected as a 100G group. Physical lanes within such a 100G group can be interchanged, but physical lanes of different 100G groups must not be interchanged.

The bit rates of an OTLC.4 lane with RS (255,239) FEC are specified in Table 8-2.

Table 8-2 – Bit rate of OTLCn with RS (255,239) FEC

OTL type	OTL nominal bit rate	OTL bit-rate tolerance
OTLCn	n × 4 × 255/226 × 24 883 200 kbit/s	±20 ppm
OTLC slice	4 × 255/226 × 24 883 200 kbit/s	±20 ppm
OTLC.4 lane	255/226 × 24 883 200 kbit/s	±20 ppm
NOTE – The nominal OTLCn, OTLC slice and OTLC.4 lane bit rates are approximately and respectively: n × 112 304 707.965 kbit/s, 112 304 707.965 kbit/s and 28.076 176.991 kbit/s.		

8.3 FOIC1.4 structure

The original purpose of the n*FOIC1.4 interface (i.e., FlexO-n group), as defined in clause 11 of [ITU-T G.709.1], is to provide an interoperable modular short-reach OTN interface for B100G OTUCn (n ≥ 1) transport signals, by bonding n * 100G standard-rate interfaces.

As the OTUCn is split into n times OTUC, each individual short-reach 100G FlexO interface (carrying an OTUC) is distributed on four lanes (FOIC1.4) and operates at almost the same interface rate as OTL4.4 (with just −4.46 ppm offset between the two nominal rates).

So, second (and beyond) generation pluggable modules developed for Ethernet 100GBASE-R applications and supporting the OTU4 rate and OTL4.4 interface could be seamlessly reused for 100G FlexO-SR transport and FOIC1.4 interface. Modules developed for [b-IEEE 802.3] specified 100GBASE-LR4 and 100GBASE-ER4. They have corresponding optical specifications for OTU4 (and so for 100G FlexO-SR) interfaces with the optical parameters as specified for the application codes 4I1-9D1F and 4L1-9C1F, respectively, in [ITU-T G.959.1]. Non-IEEE specified optical interfaces include [ITU-T G.695] application code C4S1-9D1F and [ITU-T G959.1] application code 4L1-9D1F. These modules have a four-lane WDM interface to and from a transmit/receive pair of [ITU-T G.652] optical fibres.

Most of these pluggable modules use a four-lane electrical chip-to-module interface (CAUI-4), whose specification is found in [b-IEEE 802.3] Annex 83E, and include a simple retimer.

This application of n*FOIC1.4 bonded interfaces (short-reach FlexO-n group) is illustrated in Figure 8-3a.

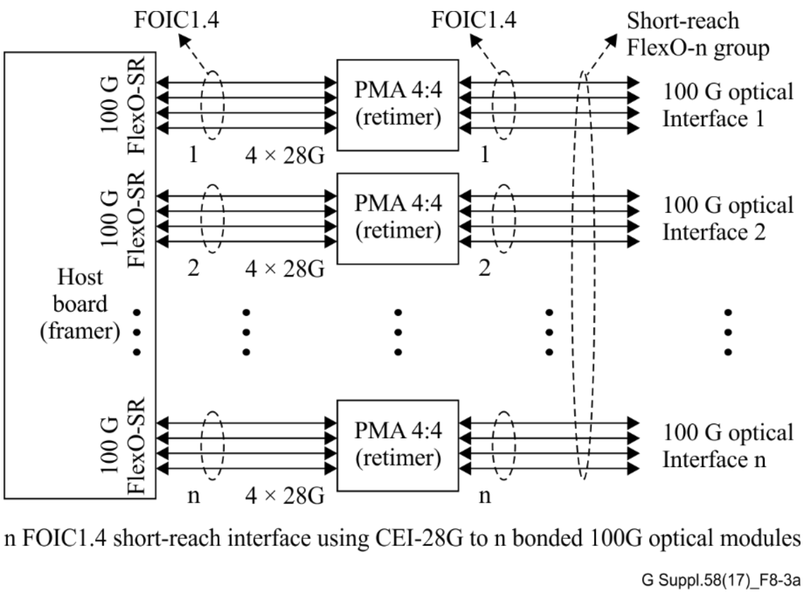

Figure 8-3a – Original application of a FOIC1.4 interface

NOTE – The FOIC1.4 interface could also be used similarly to an OTLC.4 interface in order to connect a beyond 100G OTN framer with one or more optical line DSP (ODSP) devices supporting FlexO interfaces on the host side. One possible advantage for implementers is that the FOIC1.4 lane operates at the same rate as an OTL4.4 lane, so slightly slower than an OTLC.4 lane and with a stronger RS-10 FEC. Another advantage is that the bit rate of a FOIC1.4 lane is exactly half the bit rate of a FOIC1.2 lane (the FOIC1.2 lane is obtained by simple bit-interleaving of two FOIC1.4 lanes). Depending on the application, implementers could make use of the FlexO overhead. Although some overhead may become optional, they are generated at the source and may be ignored at the sink (see clause 9.1 for the handling of FlexO overhead for this type of application). This alternate application is illustrated in Figure 8-3b.

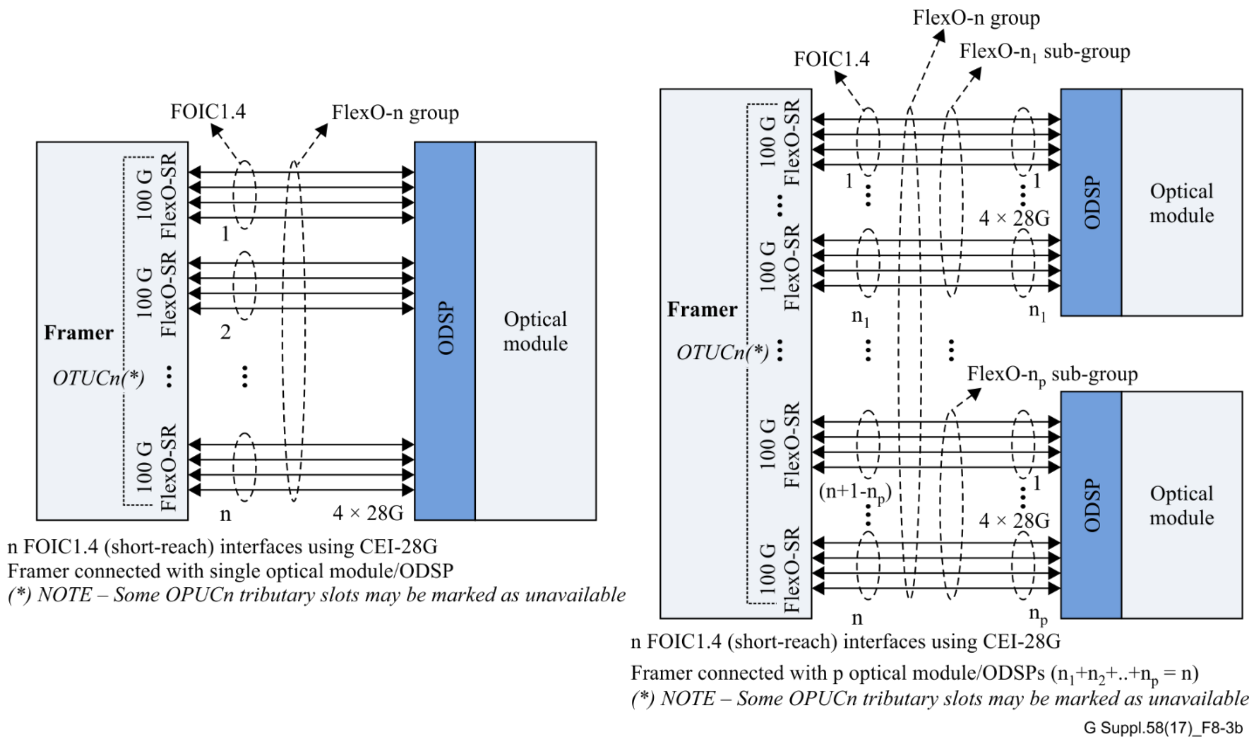

Figure 8-3b – Alternate application of a FOIC1.4 interface

The bit rates of the FOIC1.4 are specified in [ITU-T G.709.1] indicated in Table 8-3.

Table 8-3 – Bit rates of short-reach FlexO-n and FOIC1.4

FOIC type	FOIC nominal bit rate	FOIC bit-rate tolerance
FlexO-n (SR)	n × 4 × 256/241 × 239/226 × 24 883 200 kbit/s	±20 ppm
FOIC1.4	4 × 256/241 × 239/226 × 24 883 200 kbit/s	±20 ppm
FOIC1.4 lane	256/241 × 239/226 × 24 883 200 kbit/s	±20 ppm
NOTE – The nominal FOIC1.4 lane bit rate is approximately: 27 952 368.611 kbit/s.		

9 Signal formats and rates carried over 56G electrical lanes

This clause describes some MFI structures using 56G physical lanes in order to carry B100G OTUCn (n ≥ 1) signals. The electrical characteristics of each 56G physical lane may comply with OIF CEI-56G-*x*R-PAM4 specifications.

9.1 FOIC1.2 structure

As shown in Figures 7-1 and 10-1 of [ITU-T G.709.1], an OTUCn signal (n ≥ 1), full-rate or sub-rated (with some OPUCn tributary slots marked as unavailable), can be carried over n * FOIC1.2

bonded interfaces (short-reach FlexO-n group, with v=1 and k=2). Each FOIC1.2 interface carry two physical lanes of a 100G short-reach FlexO frame (carrying an OTUC).

An application example of the FOIC1.2 interface is to connect third generation beyond 100G OTN framers with ODSP devices over 56G electrical lanes and connecting these framers with emerging line side optical modules. See Figure 9-1.

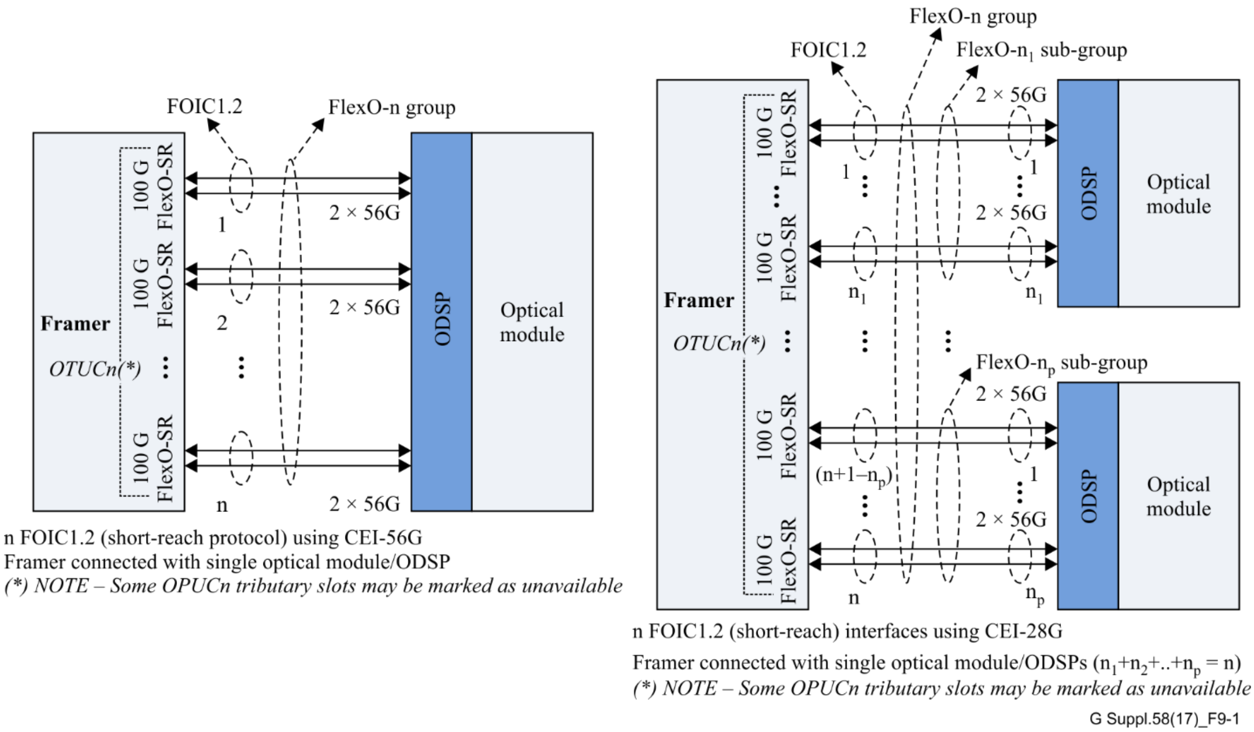

Figure 9-1 – Example applications of a FOIC1.2 interface

As per the OTUCn mapping specification in clause 10 of [ITU-T G.709.1] the OTUCn is split into n times OTUC, and each OTUC is synchronously mapped into an individual 100G FlexO frame. The 100G FlexO frame consists of frame alignment markers, overhead, FEC [RS-10(544,514) parity], and payload area in which the OTUC is transported (see clause 8 of [ITU-T G.709.1]).

Two possible applications examples are considered. In the first case, the FlexO is terminated at both ends of the MFI. In the second case, the FlexO is terminated at the framer and [fully or partially] passed-through at the ODSP. The second case is for further study.

In the first application example (n*FOIC1.2 electrical interface carrying OTUCn between a B100G OTN framer and one or p optical line DSP devices), each 100G FlexO frame is terminated at both end of the MFI.

Thus, some FlexO OH become optional and though they are generated at the source, they may be ignored at the sink.

The FlexO multi-frame alignment signal (MFAS) is generated at the source and fully interpreted at the sink per clause 9.2.1 of [ITU-T G.709.1].

The use of the OSMC and FCC overhead across the MFI is for further study.

Additionally, the Rx Line pre-FEC detected local degrade (LD) status bit is optionally carried in bit 8 of the STAT field.

The Rx ODSP detects the Rx line pre-FEC local degrade and forward the LD status bit to the Rx framer device through the MFI.

After synchronous scrambling and RS-10 FEC parity insertion (see clauses 8.4 and 10.5 of [ITU-T G.709.1]), each individual 100G FlexO frame is distributed on four 28G FlexO lanes as per the FOIC1.4 specifications in clause 11.1 of [ITU-T G.709.1].

Each 56G physical lane of a FOIC1.2 is formed by simple bit-multiplexing of two 28G FlexO lanes from the same 100G FlexO. At the sink, the bits from each individual 56G FOIC1.2 lane are disinterleaved into two 28G FlexO lanes. The sink will identify each of the four 28G FlexO lane within a FOIC1.2 interface according to its alignment marker specific pattern (unique UMx and UPx values). The sink must be able to accept the four 28G FlexO lanes in any position, and in addition to 28G FlexO lanes alignment and deskew, proceed to reordering of these four 28G FlexO lanes prior to reassembly into a 100G FlexO frame. Following this 100G FlexO frame alignment, the FlexO overhead is terminated, and the OTUC is demapped and aligned. At the framer sink, the Rx line pre-FEC LD status bit is extracted from the FlexO overhead area and the n OTUC demapped from the n FOIC1.2 interfaces are deskewed to retrieve the original OTUCn signal. At the ODSP sink, n_i OTUC demapped from n_i FOIC1.2 interfaces could be deskewed, crunched (removing unavailable tributary slots), and assembled as the OTUCn_i(-M) digital signal to be transmitted.

Groups of two FOIC1.2 physical lanes carrying one 100G FlexO frame (so one OTUC instance) have to be connected as a 100G group. Physical lanes within such a 100G group can be interchanged, but physical lanes of different 100G groups must not be interchanged.

The bit rates of FOIC1.2 are specified in Table 9-1.

Table 9-1 – Bit rates of short-reach FlexO-n and FOIC1.2

FOIC type	FOIC nominal bit rate	FOIC bit-rate tolerance
FlexO-n (SR)	n × 2 × 256/241 × 239/226 × 49 766 400 kbit/s	±20 ppm
FOIC1.2	2 × 256/241 × 239/226 × 49 766 400 kbit/s	±20 ppm
FOIC1.2 lane	256/241 × 239/226 × 49 766 400 kbit/s	±20 ppm
NOTE – The nominal FOIC1.2 lane bit rate is approximately: 55 904 737.223 kbit/s.		

Bibliography

[b-IEEE 802.3] IEEE Std. 802.3 (2015), *IEEE Standard for Information Technology – Telecommunications and Information Exchange Between Systems – Local and Metropolitan Area Networks – Specific Requirements Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications.*

[b-OIF CEI-03.1] Optical Internetworking Forum Implementation Agreement OIF-CEI-03.1 (2014), *Common Electrical I/O (CEI) – Electrical and Jitter Interoperability agreements for 6G+ bps, 11G+ bps and 25G+ bps I/O.*

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