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Guidelines concerning the measurement of wander

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NOTES

1 Supplement 35 to the G-series Recommendations was approved in Melbourne (1988) and published in Fascicle III.5 of the *Blue Book*. This file is an extract from the *Blue Book.* While the presentation and layout of the text might be slightly different from the *Blue Book* version, the contents of the file are identical to the *Blue Book* version and copyright conditions remain unchanged (see below).

2 In this Supplement, the expression "Administration" is used for conciseness to indicate both a telecommunication administration and a recognized operating agency.

Supplement No. 35

GUIDELINES CONCERNING THE MEASUREMENT OF WANDER

(Contribution from United States of America, referred to in
Recommendations G.812 and G.824)

Wander measurement methodology

The purpose of this Supplement is to present one suitable method of verification of timing accuracy of clocks. Guidelines concerning the measurement of jitter are contained in Supplement No. 38 of the O-Series.

1 Output wander measurement

1.1 *Slave clock*

The measurement strategy is to be able to derive the values of the model parameters contained in the Annex to Recommendation G.812 for the slave clock under test.

Once these parameter values have been obtained compliance with the specifications contained in Recommendation G.812 may be verified.

To adequately characterize the performance of e clock a series of tests must be performed. In general, the test fall into the three categories of operatio

1) ideal operation;

2) stressed operation;

3) holdover operation.

1.1.1 *Test configuration*

The objective of the test procedure is to be able nate the parameters in the clock model described above for a given clock under test. The architecture for a clock testing arrangement is shown in Figure 1. The components and their interconnection are described next.

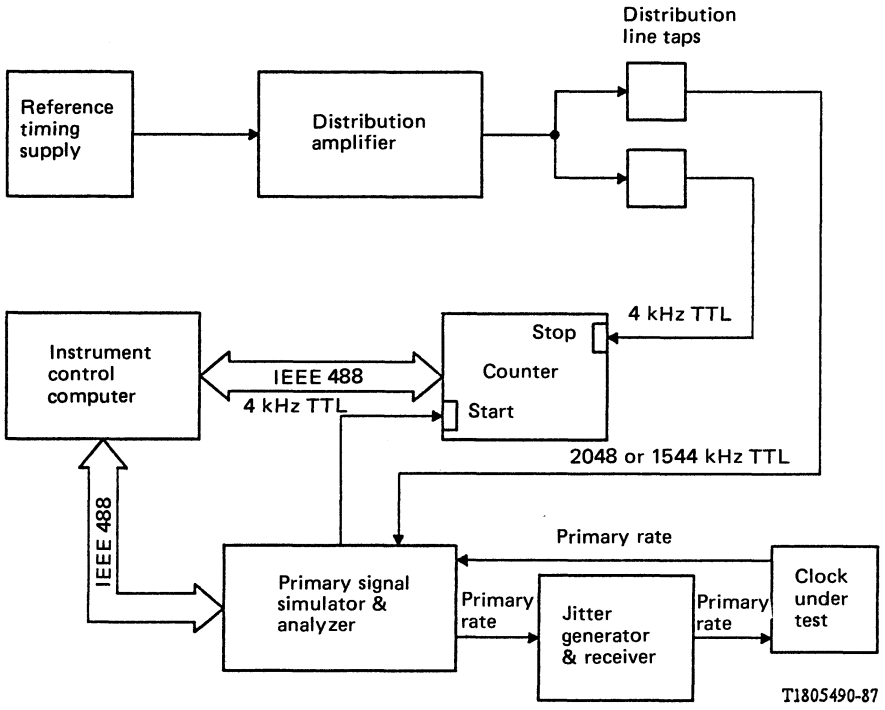

FIGURE 1

Test configuration

1.1.1.1 *Reference clock*

The test configuration is designed to provide the clock under test with a primary rate digital reference timed from a stable reference oscillator. In clock testing, it is the relative phase-time compared to the reference input that is critical[1]. Thus, the absolute accuracy of the reference input is not critical. What is important is that short-term instability of the reference oscillator be small to ensure low measurement noise and a low background tracking error in the control loop of the clock being tested.

[1] In holdover testing, the longer term stability and drift of the reference oscillator is important.

1.1.1.2 *Digital reference simulation*

The testing arrangement is designed to provide a primary rate digital reference with impairment to the clock to allow for stress testing of the clock. To accomplish this a primary rate digital signal simulator and analyzer is employed that has the capability to be externally synchronized. For the 1544 kHz primary rate digital signal[2] a 1544 kHz timing signal is supplied to the simulator/analyzer to control outgoing transmit timing. The 1544 kHz signal is produced via a distribution amplifier and synthesizer line tap. This distribution arrangement allows one to develop multiple taps of timing signals synthesized from the 10 MHz input from the reference oscillator. Each line tap is a dedicated synthesizer producing the timing signal required. The jitter produced from these synthesizers should be less than 1000 ps rms.

The primary rate impairment simulator is programmed via an IEEE 488 control bus to produce the desired interruption events to stress the clock. The primary rate digital signal is next bridged through a jitter generator and receiver. The jitter generator is used to insert background jitter to the digital signal. It is important to simulate a realistic level of background jitter for several reasons. Primarily, when interruptions occur the background jitter can be a major source of phase build-out error as the synchronization unit attempts to bridge the interruption. Secondly, the jitter transfer characteristics of the clock can be evaluated.

The jitter generation unit is provided an external jitter modulation input. The jitter signal used is bandlimited white noise. A signal from a white noise source is filtered using a low pass single pole filter with 150 Hz 3 dB cutoff. The main reason for lowpass filtering the jitter is to avoid producing bit errors from high frequency alignment jitter. The jitter power should be set to reflect realistic jitter levels in the network. It is important that sinusoidal jitter be avoided as a test jitter input, as certain phase detection techniques are very insensitive to sinusoidal jitter.

1.1.1.3 *Output timing signal recovery*

To test a clock, reference input is provided from the output of the jitter generator. To recover the output timing signal from the clock, an outgoing primary rate signal is selected from the unit controlled by the clock under test. This digital signal is connected to the receive portion of the Primary Rate Signal Simulator and Analyzer. In this unit the receiver timing function is decoupled from the transmit timing used in the generator. The receiver extracts a 4 kHz frame timing signal from the input signal and provides this timing signal at an external port. This 4 kHz timing signal is phase coherent with the outgoing timing from the clock under test.

1.1.1.4 *Phase-time data collection*

A counter is used to observe the relative phase-time error of the output 4 kHz timing signal compared to a reference 4 kHz timing signal. The reference 4 kHz timing signal is derived from the distribution amplifier and synthesizer units. The synthesizer jitter in generating the 4 kHz reference signal is less than 1000 ps. By performing the phase comparison at 4 kHz the observation range of phase variation is 250 μs. If care is given to start a test near the centre of this range, there should not be a problem associated with cycle slipping for all tests except holdover testing. However, even this range can be extended by resolving cycle slips in the data collection software.

In reality, the measurement resolution is limited by the intrinsic jitter in the counter as well as trigger error. Experience has shown that the measurement resolution jitter can be maintained below 100 ps rms with reasonable care given to cabling and trigger levels. More importantly, the overall background jitter noise level can be checked prior to testing to ensure proper performance. For the components used in the particular system described, overall jitter levels of 1000 ps rms are typically attainable. This is more than adequate for measuring the levels of phase stability expected from clocks.

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[2] The following discussion is applicable in an analogous manner to the 2048 kHz primary rate digital signal.

1.1.1.5 *Data collection*

An instrument control computer should be used to automate the testing procedure and collect and analyze the phase-time data. The control computer is interfaced via an IEEE 488 bus to both the Counter and the Primary Rate Digital Signal Simulator and Analyzer.

A key function of the control computer is to gather phase-time data from the counter. The instrument controller obtains a phase-time sample from the counter every 10 seconds. The counter is programmed to average 4000 samples over a 3 second window and return the average to the controller. The resulting measurement bandwidth is 0.33 Hz. The phase-time data is processed in real-time to obtain running estimates of the Allan variance for 10, 100, 1000 and 10 000 second observation intervals. The program also calculates a running estimate of the frequency departure and the drift.

1.1.1.6 *Data analysis*

The objective of the data analysis is to estimate from the data the parameters associated with the clock model. From the Allan variance data, one can determine the presence of either the white noise PM or white noise FM components expected from the model. The frequency departure estimator is the y_{bias} term in the model, and the drift estimator D is the drift component in the model.

1.1.2 *Basic technique and procedure*

This paragraph contains the basic techniques and procedures for testing the three categories of slave clock operation. Appendix I provides examples of the application of these test using actual measurement data.

1.1.2.1 *Ideal operation*

The purpose of this testing is to obtain a baseline performance metric for a clock. The model predicts that clocks under ideal conditions should produce a white noise PM phase instability. This white noise PM should be small as it represents the best case performance of a clock (clearly less than 1 μs based on current MRTIE output requirements). It should be measured in the presence of realistic levels of jitter to assure acceptable jitter transfer.

In the standard test procedure described, the bandwidth of the measurement is 0.33 Hz. In some clock designs, there is significant noise between this 0.33 Hz cutoff and the 10 Hz cutoff associated with jitter. It is important to evaluate the jitter in this band. This could be accomplished by developing an additional measurement program to capture this fast wander data.

1.1.2.2 *Stressed operation*

This area of testing is critically important to adequately evaluate clocks. The difficulty in this testing is selection of the appropriate disruption events. For some clocks any event that appears as a severely errored second will produce a phase build-out event. In some clocks any outage or spurious noise spikes will perturb a counter in the phase detection producing a spurious phase hit which may or may not be phase built-out depending on its severity. On the other hand, clocks can be designed to observe the framing pulse position to extract phase. In such clocks, an interruption need not produce a phase build-out event unless there is an actual shift in the framing pulse position (for example a protection switch event).

It is proposed that one stress test which should be performed is to simulate an SES event with a short outage (100 ms) at a rate of 10 SES per day in the presence of background input jitter. Typically an outage of this magnitude will force a clock to attempt to phase build-out without switching references. An example of this stress test is given in the next section and should serve to clarify the concepts and the significance of the results.

Other stress inputs should also be considered in evaluating a clock.

– *Error bursts*: An error burst can be simulated in which the underlying timing waveform is not perturbed. Under this condition, it would be advantageous for a clock not to phase build-out. Such a test would gain in importance if it is determined that the majority of error burst events are actually pure data errors with no perturbation in timing.

– *Phase bit*: Phase hits are produced by protection activity, as well as from other clocks. Phase hits are interruption events that should either force a phase build-out event or inadvertently be followed by the clock. In either case they will degrade a clock's performance. This is an area for further study.

– *Restart events*: Restart events are a phenomena associated with certain clocks. A restart event is associated with a clock giving up its current state, and defaulting back to its initial conditions. The results are a transient event which can be significant. Restart events should not happen during normal clock operation, and thus should not likely be included in a general clock testing plan. However, it is important that the behaviour be better understood and controlled.

– *Frequently hit*: It is important that clocks do not follow references that exhibit large frequency hits. However the ability to detect frequency hits is closely tied to the selection of the tracking bandwidth of a given clock PLL. The solution to the problem will depend on the degree to which the bandwidth of various clocks in a network can be standardized.

1.1.2.3 *Holdover operation*

In holdover testing, the objective is to estimate the initial frequency offset (y_{bias}) and the Drift (D) of the clock model. The initial frequency offset is dependent on the accuracy of the frequency estimate obtained in the control loop, and the frequency settability of the local oscillator. It is important to test holdover from a reasonable stress condition prior to holdover to capture the control loops capability of obtaining an accurate frequency estimate.

In determining the drift estimate, one critical factor for quartz oscillators is that it typically takes observation intervals lasting over days to obtain a statistically significant drift estimator. This is a hard reality that cannot be avoided. In addition, attention must be placed on the temperature conditions maintained during the test. This is a subject for further study.

1.2 *Primary reference clock*

This section requires further study.

APPENDIX I

(to Supplement No. 35)

Example applications

This section presents the results of the application of some of the testing procedures for two clocks. It is important to point out that the two clocks tested have different internal architectures. The main result of the tests is that the model for clock performance was supported. This model can be summarized as follows:

1) For short observation intervals outside the tracking bandwidth of the PLL, the stability of the output timing signal is determined by the short-term stability of the local synchronizer time base.

2) In the absence of reference disruptions, the stability of the output timing signal behaves as a white noise PM process as the observation period is increased to be within the tracking bandwidth of the PLL.

3) In the presence of disruptions, the stability of the output timing signal behaves as a white noise FM process as the observation period is increased to be within the tracking bandwidth of the PLL.

4) In the presence of disruptions, the output timing signal may incur a systematic frequency offset with respect to the reference. This results from a bias in the phase build-out when reference is restored.

The specific test results are described below.

I.1 *Local clock evaluation*

The results described in this section are for actual performance data.

I.1.1 *Unstressed primary rate input tests*

The first test performed was to evaluate the timing signal output under ideal reference input conditions. The primary rate reference input is produced by the generator timed from the Caesium reference. The jitter outside the tracking bandwidth of the stratum 3 PLL is much less than 1 ns. Typically, 300 ps as measured by the counter.

For this test, the jitter test set was bypassed, and the primary rate from the primary rate simulator and analyzer was fed directly into the synchronizer. The test was run for 67 hours. The results are presented in Figure I-1. The square root of the Allan variance is plotted vs. observation time. The data points marked by triangles apply to this test.

The test results are consistent with the model. For observation times outside the tracking bandwidth of this PLL (less than 60 seconds), the Allan variance indicated a white FM noise resulting from the local quartz oscillator. As the observation time increases, the PLL tracks the reference and the noise process converges to white FM.

The magnitude of the white PM noise is 85 ns rms. One component of this noise is the rms time error of the oscillator in 60 seconds (the bandwidth of this PLL is 1/60 sec). In addition, there is a component resulting from the resolution of the phase detector. A phenomena that arises in digital loops is that the phase error can make excursions of at least one bit in either direction of the nominal setpoint. This effect is reduced when the input has jitter on the order of a phase detector bit.

I.1.2 *Stressed primary rate input test*

The purpose of this test is to emulate the behaviour of the synchronizer under stress conditions that arise in actual networks. For this test, a short outage event was produced under program control by the primary rate simulator and analyzer every 15 minutes. The outage events duration was randomized with a uniform distribution over the range of 10 to 100 ms.

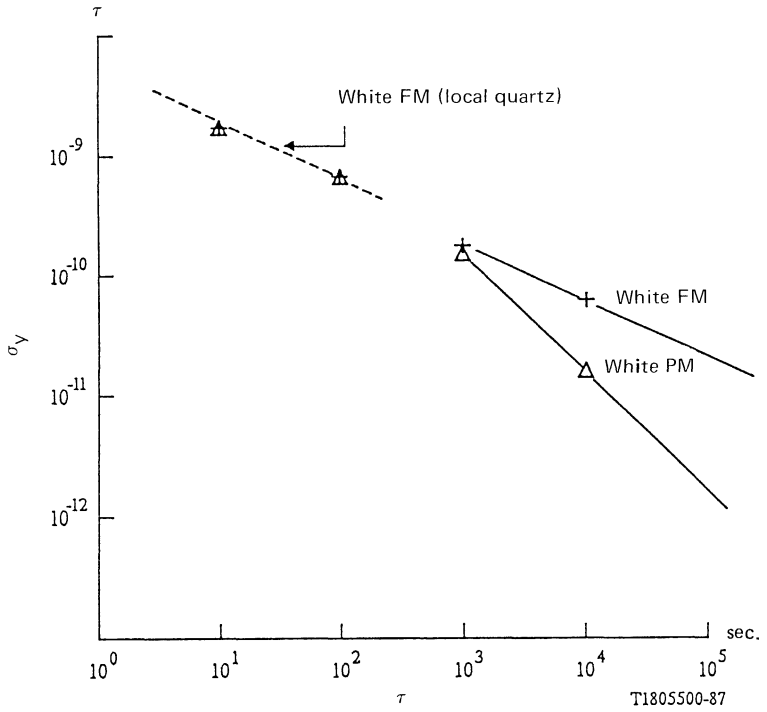
For this test, the jitter set was bypassed, and the primary rate signal from the primary rate simulator and analyzer was fed directly into the synchronizer. The test was run for 50 hours. The results are presented in Figure I-1. The square root of the Allan variance is plotted vs. observation time. The data points marked by plus signs apply to this test.

I.1.2.1 *Allan variance results*

The test results are consistent with the model. For observation times outside the tracking bandwidth of this PLL (less than 60 seconds), the Allan variance indicates a white FM noise resulting from the local quartz oscillator. As the observation time increases, the PLL is experiencing a disruption every 900 seconds. The residual phase build-out error accumulates and produces a random walk in phase (white noise FM). The build-out error per disruption is calculated as 180 ns rms.

I.1.2.2 *Systematic frequency offset*

The stress test data shows a statistically significant frequency offset. The frequency offset over the 50 hour test was 3×10^{-11}. Given the white FM noise, the rms error is 1.5×10^{-11}. These numbers reflect a bias error in the phase build-out in the range of 15 to 45 ns. Such bias errors in clocks result in frequency offsets. The implications of this is that to some extent all clocks in a network operate plesiochronously. Given a worse case level of disruption of ten per day the resulting frequency offset is of the order of parts in 10^{12}.



Δ Undisturbed clean DS1, observation time 240,100 sec

$\bar{Y}$ = 7E-13 white PM 148 ns/τ , $\tau > 10^3$, 85 ns daily r.m.s., prediction error

\+ Clean 1544 kbit/s 1 outage/15 minutes observation time 180,000 sec

$\hat{Y}$ = 3E−11 (1 σ = 1.5 E−11) white FM 6E−9/$\sqrt{\tau}$, $\tau > 10^3$, 1.76 μs daily r.m.s. (180 ns RMS/disruption) prediction error

f_3 dB = 1/60 sec

Measurement interval τ_0 = 10 sec. Measurement bandwidth = 0.33 Hz.

FIGURE I-1

Example of local node clock

I.1.2.3 *Significance of stress test results*

To obtain a meaningful interpretation of the stress test results one must consider the disruption level. In this test the disruption level was 100 disruptions per day. This is an order of magnitude greater than what can be expected on actual primary rate links. In this particular PLL the build-out error process is independent from one event to the next. This can be proven by testing at several disruption levels. The results indicated a rms error of 180 ns per disruptions. Given 10 disruptions per day the resulting daily rms error is 570 ns.

I.2 *Transit clock evaluation*

The results described in this section are for actual performance data.

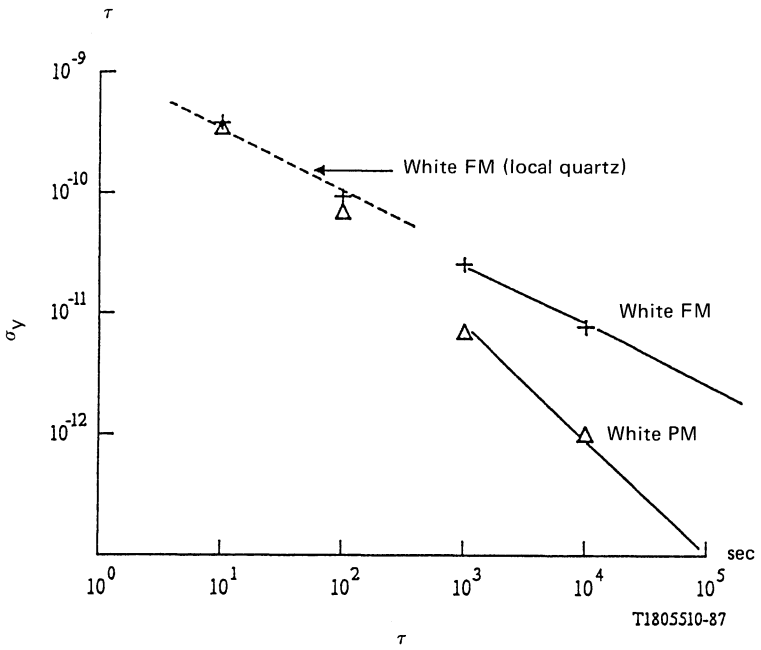
I.2.1 *Unstressed primary rate input test*

The first test performed was to evaluate the timing signal output under ideal reference input conditions. The primary rate reference input is produced by the primary rate simulator and analyzer timed from the Caesium reference. The jitter outside the tracking bandwidth of the stratum 3 PLL is much less than 1 ns. Typically, 300 ps as measured by the counter.

For this test, the jitter test set was included. The jitter test set was given an external jitter modulation input. The jitter signal was band limited white noise. A single pole filter was employed with a 150 Hz 3 dB cutoff. The jitter was low passed filter to avoid producing framing errors resulting from high frequency alignment jitter. The external signal was adjusted to achieve a peak-to-peak jitter level of 1.5 μs. The test was run for 23 hours. The results are presented in Figure I-2. The square root of the Allan variance is plotted vs. observation time. The data points marked by triangles apply to this test.

The test results are consistent with the model. For observation times outside the tracking bandwidth of this PLL (less than 450 seconds), the Allan variance indicated a white FM noise resulting from the local quartz oscillator. As the observation time increases, the PLL tracks the reference and the noise process converges to white PM.

The magnitude of the white PM noise is 6 ns rms. This is an exceptionally good number and results from the tight time constant for the loop (450 seconds). In this case the input jitter prevents the edge jumping effects.



Δ Undisturbed DS1[a]. Input observation time 83,000 sec

$\overline{Y}$ = +6E−13 white PM 1E−8/τ, $\tau > 10^3$, 6 ns daily r.m.s. prediction error

\+ 1544 kbit/s[a] 1 outage/30 minutes. Observation time 253,800 sec

$\overline{Y}$ = +6E−13. White FM 8E−10/$\sqrt{\tau}$, $\tau > 10^3$, 235 nsec daily r.m.s. prediction error

f_3 dB = 1/450 sec

[a] 1.5 μ sec p-p. Jitter BW = 150 Hz.

Measurement interval τ_0 = 10 sec. Measurement bandwidth = 0.33 Hz.

FIGURE I-2

Example of transit node clock

I.2.2 *Stressed primary rate input test*

The purpose of this test is to emulate the behaviour of the synchronizer under stress conditions that arise in actual networks. For this test, a short outage event was produced under program control by the primary rate simulator and analyzer every 30 minutes. The outage events duration was randomized with a uniform distribution over the range of 10 to 100 ms.

For this test, the jitter test set was included. The jitter test set was given an external jitter modulation input. The jitter signal was bandlimited white noise. A single pole filter was employed with a 150 Hz 3 dB cutoff. The jitter was low passed filter to avoid producing framing errors resulting from high frequency alignment jitter. The external signal was adjusted to achieve a peak-to-peak jitter level of 1.5 μs. The test was run for 70 hours. The results are presented in Figure I-2. The square root of the Allan variance is plotted vs. observation time. The data points marked by plus signs apply to this test.

I.2.2.1 *Allan variance results*

The test results are consistent with the model. For observation times outside the tracking bandwidth of this PLL (less than 450 seconds), the Allan variance indicated a white FM noise resulting from the local quartz oscillator. As the observation time increases, the PLL is experiencing a disruption every 1800 seconds. The residual phase build-out error accumulates and produces a random walk in phase (white noise FM). The build-out error per disruption is calculated at 34 ns rms. A contributor to this error is the input primary rate jitter. The algorithm averages the input to improve the estimate of the phase error to build-out.

I.2.2.2 *Systematic frequency offset*

The stress test data shows a statistically insignificant frequency offset. The frequency offset over the 70 hour test was 6×10^{-13}. Given the white FM noise, the rms error is 1.5×10^{-12}. Given this uncertainty, there is no indication of a bias in the data. In the worse case the bias should not be more than the uncertainty level of 1.5×10^{-12}.

I.2.2.3 *Significance of stress test results*

To obtain a meaningful interpretation of the stress test results one must consider the disruption level. In this test the disruption level was 48 disruptions per day. This is five times greater than what can be expected on actual primary rate links. In this particular PLL the build-out error process should be independent from one event to the next based on a knowledge of the PLL design. This can be proven by testing at several disruption levels. The results indicated an rms error of 34 ns per disruption. Given 10 disruptions per day, the resulting daily rms error is 100 ns.

I.3 *Allan variance confidence limits*

Sample variances (like sample Allan variances) are distributed as chi-square. Based on J. Barnes work described in [1], the confidence interval for the Allan variance can be determined assuming a given noise process. In calculating the sample Allan variances a complete overlap of lag intervals was used. This is the most efficient use of data. However, it is incorrect to assume independence in overlapping samples when calculating confidence intervals. This is described in complete detail in [1]. For brevity, the methods for calculating the confidence interval described in reference [1] were employed.

The 90% confidence factors for white PM noise are bounded within 0.9 and 1.1 for all lag times up to 10,000 assuming an observation period of a day. For white FM noise over a day observation interval the confidence factors were as follows. For 1000 second lag interval the lower bound is 0.9, and the upper bound is 1.2. At 10 000 the confidence factors are 0.75 and 1.5.

As an example of what these factors mean consider the white FM noise component in Figure I-2 (plus sign tagged data). For the 10 000 second lag, the square root of the sample variance is 8×10^{-12}. The 90% confidence interval for the true variance is bounded by the confidence factors multiplied by the sample variance. This leads to the square root of the Allan variance being bounded between 6.9×10^{-12} and 9.8×10^{-12} with a 90% confidence level.

Reference

[1] BARNES (J. A.): Data Analysis and Confidence Intervals, *NBS Time and Frequency Seminar Notes*, chapter 6, August, 1986.

Geneva, 2004