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ITU-T

TELECOMMUNICATION
STANDARDIZATION SECTOR
OF ITU

G.8263/Y.1363

(08/2017)

SERIES G: TRANSMISSION SYSTEMS AND MEDIA, DIGITAL SYSTEMS AND NETWORKS

Packet over Transport aspects – Synchronization, quality and availability targets

SERIES Y: GLOBAL INFORMATION INFRASTRUCTURE, INTERNET PROTOCOL ASPECTS, NEXT-GENERATION NETWORKS, INTERNET OF THINGS AND SMART CITIES

Internet protocol aspects – Transport

Timing characteristics of packet-based equipment clocks

Recommendation ITU-T G.8263/Y.1363

ITU-T

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Recommendation ITU-T G.8263/Y.1363

Timing characteristics of packet-based equipment clocks

Summary

Recommendation ITU-T G.8263/Y.1363 outlines requirements for timing devices used in synchronizing network equipment that operates in the interworking function (IWF) and other network elements (NEs) as defined in Recommendation ITU-T G.8261/Y.1361. Recommendation ITU-T G.8263/Y.1363 defines the requirements for packet-based equipment clocks.

History

Edition	Recommendation	Approval	Study Group	Unique ID*
1.0	ITU-T G.8263/Y.1363	2012-02-13	15	11.1002/1000/11524
1.1	ITU-T G.8263/Y.1363 (2012) Amd. 1	2013-08-29	15	11.1002/1000/12014
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2.0	ITU-T G.8263/Y.1363	2017-08-13	15	11.1002/1000/13320

Keywords

Clock, jitter, synchronization, wander.

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FOREWORD

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Recommendation ITU-T G.8263/Y.1363

Timing characteristics of packet-based equipment clocks

1 Scope

This Recommendation outlines minimum requirements for the timing functions of the packet slave clocks as defined in [ITU-T G.8265]. It supports frequency synchronization distribution when using packet-based methods.

This Recommendation allows for proper network operation when a packet slave clock is timed from a packet master clock as defined in [ITU-T G.8265].

This Recommendation focuses on mobile applications, and in particular on the delivery of frequency synchronization for end applications, such as mobile base stations. It supports the architecture defined in [ITU-T G.8265]. Other applications are for further study.

This Recommendation focuses on two different deployment cases for the packet slave clock as follows.

– Packet slave clock embedded in a device co-located with the end application, as shown after the connection C1 in Figure 3 of [ITU-T G.8261.1].

– Packet slave clock embedded within the end application, as shown after the connection C2 in Figure 3 of [ITU-T G.8261.1]. This second case is for further study for the first version of this Recommendation.

Other deployment cases for the packet slave clock are for further study.

This Recommendation focuses on the types of networks corresponding to the hypothetical reference models, HRM-1 and HRM-2, defined in [ITU-T G.8261.1].

NOTE – For long observation intervals, the packet-based equipment clock – slave – frequency (PEC-S-F) is expected to compensate for temperature variation effects; therefore, the output of the PEC-S-F will converge to the 1 ppb slope.

The HRM-2 type of network is for further study for the first version of this Recommendation. Other types of networks are outside the scope of this Recommendation.

This Recommendation defines the minimum requirements for the packet slave clocks. These requirements apply under the normal environmental conditions specified for the equipment.

This Recommendation includes clock accuracy, packet delay variation (PDV) noise tolerance, holdover performance and noise generation. The start-up conditions (e.g., variable filtering bandwidth at start-up and stabilization period) are for further study.

2 References

The following ITU-T Recommendations and other references contain provisions which, through reference in this text, constitute provisions of this Recommendation. At the time of publication, the editions indicated were valid. All Recommendations and other references are subject to revision; users of this Recommendation are therefore encouraged to investigate the possibility of applying the most recent edition of the Recommendations and other references listed below. A list of the currently valid ITU-T Recommendations is regularly published. The reference to a document within this Recommendation does not give it, as a stand-alone document, the status of a Recommendation.

[ITU-T G.703] Recommendation ITU-T G.703 (2016), *Physical/electrical characteristics of hierarchical digital interfaces.*

[ITU-T G.810]	Recommendation ITU-T G.810 (1996), *Definitions and terminology for synchronization networks*.
[ITU-T G.811]	Recommendation ITU-T G.811 (1997), *Timing characteristics of primary reference clocks*.
[ITU-T G.823]	Recommendation ITU-T G.823 (2000), *The control of jitter and wander within digital networks which are based on the 2048 kbit/s hierarchy*.
[ITU-T G.824]	Recommendation ITU-T G.824 (2000), *The control of jitter and wander within digital networks which are based on the 1544 kbit/s hierarchy*.
[ITU-T G.8260]	Recommendation ITU-T G.8260 (2015), *Definitions and terminology for synchronization in packet networks*.
[ITU-T G.8261]	Recommendation ITU-T G.8261/Y.1361 (2008), *Timing and synchronization aspects in packet networks*.
[ITU-T G.8261.1]	Recommendation ITU-T G.8261.1/Y.1361.1 (2012), *Packet delay variation network limits applicable to packet-based methods (Frequency synchronization).*
[ITU-T G.8265]	Recommendation ITU-T G.8265/Y.1365 (2010), *Architecture and requirements for packet-based frequency delivery*.
[ITU-T G.8265.1]	Recommendation ITU-T G.8265.1/Y.1365.1 (2014), *Precision time protocol telecom profile for frequency synchronization*.

3 Definitions

Definitions related to synchronization are contained in [ITU-T G.810] and [ITU-T G.8260].

4 Abbreviations and acronyms

For the purposes of this Recommendation, the following abbreviations and acronyms are used:

CBR	Constant Bit Rate
CES	Circuit Emulation Service
CUT	Clock Under Test
EEC	synchronous Ethernet Equipment Clock
FPP	Floor Packet Percentageool
FR	Frequency Reference
GM	Grandmaster
HRM	Hypothetical Reference Model
IWF	Interworking Function
MAFE	Maximum Average Frequency Error
MTIE	Maximum Time Interval Error
NE	Network Element
PDV	Packet Delay Variation
PEC-M	Packet-based Equipment Clock – Master
PEC-S	Packet-based Equipment Clock – Slave

PEC-S-F	Packet-based Equipment Clock – Slave – Frequency
PHY	Physical (layer)
PRC	Primary Reference Clock
PSD	Power Spectral Density
PTP	Precision Time Protocol
PTS	Packet Timing Signal
PTSF	Packet Timing Signal Fail
SEC	Synchronous digital hierarchy Equipment Clock
SSM	Synchronization Status Message
TDEV	Time Deviation

5 Frequency accuracy

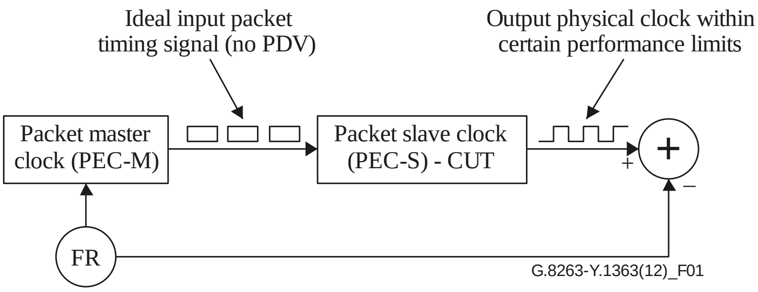
5.1 Packet-based equipment clock – slave – frequency

Under free running conditions, the output frequency accuracy of the PEC-S-F should not be greater than 4.6 ppm with regard to a reference traceable to an ITU-T G.811 clock.

NOTE – The time interval for this accuracy is for further study. Values of 1 month and 1 year have been proposed.

6 Noise generation

The noise generation of a packet-based equipment clock – slave (PEC-S) represents the amount of phase noise produced at the output of the PEC-S when there is an ideal input reference packet timing signal (PTS). Figure 1 illustrates the testing procedure:



CUT Clock under test
FR Frequency reference

Figure 1 – Noise generation testing procedure

It should be noted that packet-based equipment clocks – slave – frequency according to the architecture defined in [ITU-T G.8265] (see Figure 1 of [ITU-T G.8265]) are not cascaded; therefore, specification of noise generation produced at the output of the clock is not required when there is an ideal input reference signal. In fact, the applicable noise generation requirement is already covered by the specifications provided in clause 7 of this Recommendation. However, this specification is provided in order to enable network operators to measure the noise produced by the PEC-S-F under ideal conditions, separately from the scenarios where PDV is applied (PDV noise tolerance testing).

The maximum time interval error (MTIE) is measured through an equivalent 10 Hz, first-order, low-pass measurement filter, at a maximum sampling time of 1/30 s.

6.1 Packet-based equipment clock – slave – frequency

When the PEC-S-F is in the locked mode of operation, synchronized to a PDV free reference, and its MTIE output is measured using the same reference as the packet master clock which generated the PTS, the MTIE should have the limits described in Table 1, if the temperature is constant (within ±1 K).

Table 1 – Wander generation (maximum time interval error) for packet-based equipment clock – slave – frequency with constant temperature

MTIE limit (ns)	**Observation interval** τ (s)
1 000	$0.1 < \tau \leq 1000$
τ	$\tau > 1\,000$ (Note)
NOTE – The maximum applicable observation interval is for further study.	

The resultant requirement is shown by the solid line in Figure 2.

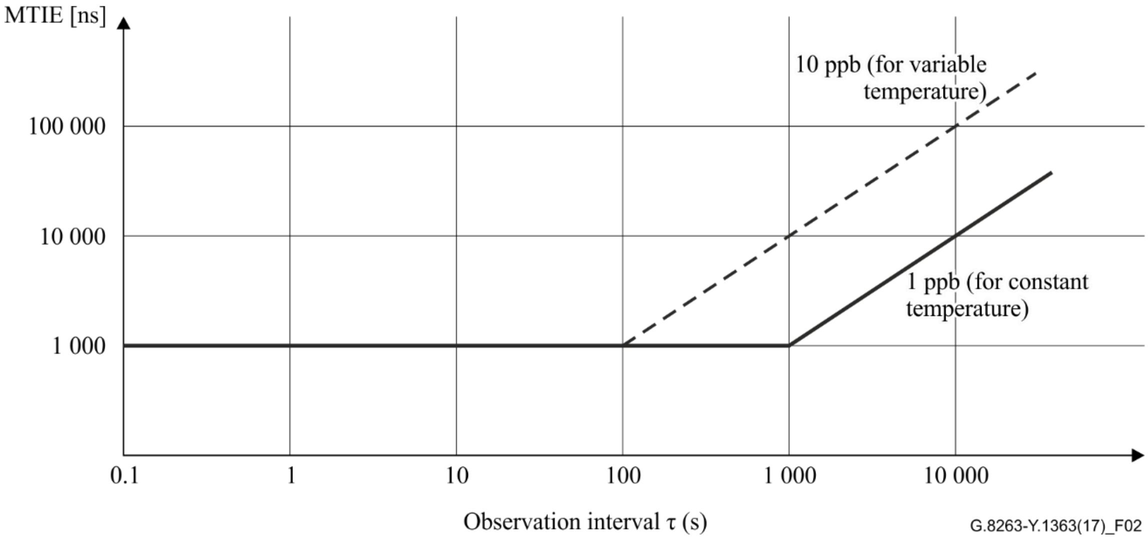


Figure 2 – Wander generation (maximum time interval error) for packet-based equipment clock – slave – frequency

NOTE – For long observation intervals, the PEC-S-F is expected to compensate for temperature variation effects; therefore, the output of the PEC-S-F will converge to the 1 ns/s slope.

When temperature effects are included, the limits are given in Table 2.

Table 2 –Wander generation (maximum time interval error) for packet-based equipment clock – slave – frequency with temperature effects

Additional MTIE allowance (ns)	**Observation interval τ (s)**
1000	$0.1 < \tau \leq 100$
$10\ \tau$	$\tau > 100$ (Note)
NOTE 1 – The maximum applicable observation interval is for further study. NOTE 2 – When testing under the worst case temperature variation and depending on the time constant of the loop, the ageing characteristics of the oscillator may add an additional noise at the output of PEC-S-F that may slightly exceed the variable temperature mask.	

The resultant requirements are shown by the dashed line in Figure 2.

7 Packet delay variation noise tolerance

7.1 Packet-based equipment clock – slave – frequency

The PDV noise tolerance of the PEC-S-F indicates the minimum PDV noise at the input of the PEC-S-F. It indicates the noise at the PTS that the PEC-S-F must tolerate.

The model for a packet slave clock is shown in Figure A.1. The transfer characteristics of PEC-S-F determines its property with regard to the filtering of PDV noise at the PTS and generates a clock frequency traceable to the input timing signal available at the packet master clock.

The PEC-S-F must tolerate the noise at the limits specified in clause 8.1.1 of [ITU-T G.8261.1] (PDV network limits at point C). Under these conditions, the output clock of the PEC-S-F must:

– not cause the packet timing signal fail- (PTSF-) unusable signal to be triggered (this is for further study);
– not cause the clock to go into holdover;
– maintain the clock within the following prescribed performance limits, depending on the applicable use case:
  • the limits defined for case 3 in clause 7.2.2 of [ITU-T G.8261.1], as defined in reference point D in Figure 3 of [ITU-T G.8261.1], where *n* = 16 ppb as shown in Table 1 of [ITU-T G.8261.1] and Figure 4 of [ITU-T G.8261.1],
  • the limits defined for case 2 in clause 7.2.2 of [ITU-T G.8261.1], as defined in reference point D in Figure 3 of [ITU-T G.8261.1] – this case is for further study.

NOTE 1 – The above limits apply to a PEC-S-F external to the end application (point C1 in Figure 3 of [ITU-T G.8261.1]). The limits corresponding to the end application at the point E in Figure 3 of [ITU-T G.8261.1] for the case of a PEC-S-F embedded in the end application (point C2 in Figure 3 of [ITU-T G.8261.1]) are for further study.

NOTE 2 – For the particular packet rate used by an actual PEC-S-F implementation, within the range specified in [ITU-T G.8265.1], the clock must tolerate the PDV generated by the network as specified in [ITU-T G.8261.1]. More specifically, for HRM-1 of [ITU-T G.8261.1], the PEC-S-F must also meet the output performance specification for its particular packet rate when only 1% of the timing packets sent by the packet master remain in the 150 µs fixed cluster range, starting at the floor delay in every observation window of 200 s.

NOTE 3 – The way to generate a PTS (PDV pattern) experiencing noise at the limits specified in clause 8 of [ITU-T G.8261.1] is for further study. For the purpose of PDV input tolerance testing, the maximum duration of the test period is for further study. Possible testing methodologies for HRM-1 of [ITU-T G.8261.1] are given in Appendix I.

NOTE 4 – As described in clause 8.1.2 of [ITU-T G.8261.1], many networks may exhibit lower PDV compared with the network limit for HRM-1 specified in clause 8.1.1 of [ITU-T G.8261.1]. This Recommendation defines one type of packet slave clock that is suitable for use with HRM-1, as described in clause 8.1.1 of [ITU-T G.8261.1]. Some operators may decide to use a different type of packet slave clock if their network limits comply with clause 8.1.2 of [ITU-T G.8261.1]; this alternate type of packet slave clock is for further study.

8 Long-term phase transient response (holdover)

When a PEC-S clock loses all its references, it enters the holdover state. This clause describes the behaviour required of the PEC-S clock during this state.

NOTE – This specification for holdover assumes that an ideal input was applied to the PEC-S-F before entering holdover.

8.1 Packet-based equipment clock – slave – frequency

For the PEC-S-F deployed as per ITU-T G.8265 architecture, in general, there are no requirements for long-term holdover. In this case, it is expected that when the quality at the output of the PEC-S-F is not sufficiently good [e.g., primary reference clock (PRC) traceability is lost], the output timing reference should be squelched so as to let the end application enter holdover.

However, in some cases, it might not be possible to squelch the output reference timing signal [e.g., reference timing signal carried by 2 048 kbit/s traffic signal, as related to some circuit emulation service (CES) applications]. In these cases, when available, the synchronization status message (SSM) carried in the 2 048 kbit/s signal as per [ITU-T G.704] could be used to inform the connected equipment that PRC traceability has been lost. As an alternative, a management alarm could be raised in order to inform connected equipment through the management layer.

If none of these options is possible (e.g., end application does not support the SSM), then some long-term holdover may be required. In this case, the following holdover specification applies.

The phase error, Δx at the output of the PEC-S-F relative to the input at the moment of loss of reference should, over any period of S s, not exceed the following limit:

$$|\Delta x(S)| \leq \{(a_1 + a_2)S + 0.5\, b\, S^2 + c\}[\text{ns}]$$

The derivative of $\Delta x(S)$, the fractional frequency offset, should, over any period of S seconds, meet the following:

$$|\mathrm{d}(\Delta x(S))/\,\mathrm{d}S| \leq \{a_1 + a_2 + bS\}[\text{ns/s}]$$

In applying the above requirements for the derivative of $\Delta x(S)$, the period S must begin after any transient associated with entry into holdover is over.

NOTE 1 – Symbol a_1 represents an initial frequency offset under constant temperature conditions (±1 K).

NOTE 2 – Symbol a_2 accounts for temperature variations after the clock went into holdover. If there are no temperature variations, the term a_2S should not contribute to the phase error.

NOTE 3 – Symbol b represents the average frequency drift caused by aging. This value is derived from typical aging characteristics after 60 days of continuous operation. It is not intended to measure this value on a per day basis, as the temperature effect will dominate.

NOTE 4 – The phase offset c takes care of any additional phase shift that may arise during the transition at the entry of the holdover state.

The permissible phase error specifications are shown in Table 3.

Table 3 – Transient response specifications during hold-over

a_1 (ns/s)	1.0
a_2 (ns/s)	10
b (ns/s^2)	1.16×10^{-5}
c (ns)	150

9 Phase response to packet timing interruptions

Phase response to packet timing interruptions is for further study.

10 Interfaces

The requirements of this Recommendation are related to reference points internal to the network elements (NEs) in which the clock is embedded and are, therefore, not necessarily available for measurement or analysis by the user. Therefore, the performance of the PEC-S-F is not defined at these internal reference points, but rather at the external interfaces of the equipment.

The synchronization input interface for equipment in which the PEC-S-F may be contained is Ethernet, where the timing is carried at the packet layer.

The synchronization output interfaces for equipment in which the PEC-S-F may be contained are:

– 1 544 kbit/s interfaces according to [ITU-T G.703];

– 2 048 kHz external interfaces according to [ITU-T G.703];

– 2 048 kbit/s interfaces according to [ITU-T G.703];

– synchronous Ethernet interfaces.

NOTE 1 – The performance of this interface may not meet [b-ITU-T G.8262].

Not all of the above interfaces need be implemented on all equipment. These interfaces should comply with the requirements as defined in this Recommendation. The use of other interfaces is for further study.

NOTE 2 – For synchronous Ethernet interfaces, refer to Appendix III of [b-ITU-T G.8262].

Annex A

Packet-based clock functional model

(This annex forms an integral part of this Recommendation.)

This annex describes a functional model.

Figure A.1 shows a functional model of a PEC-S-F. The PTS is processed by a packet selection algorithm to select the packets that are going to be used to recover the clock. The time information carried in the selected packets are used as an input to the time scale comparator to compare the master and local time scales. The time difference between the arrival and departure times can be used as an error signal to control the rate of the local oscillator driving the local time scale, such that the local time scale advances at the same rate as the master time scale. The local reference may come from a stable oscillator, or the output clock. Figure A.1 represents a functional model and it is not intended to specify any specific implementation. Any specific detail on implementation is outside the scope of this Recommendation.

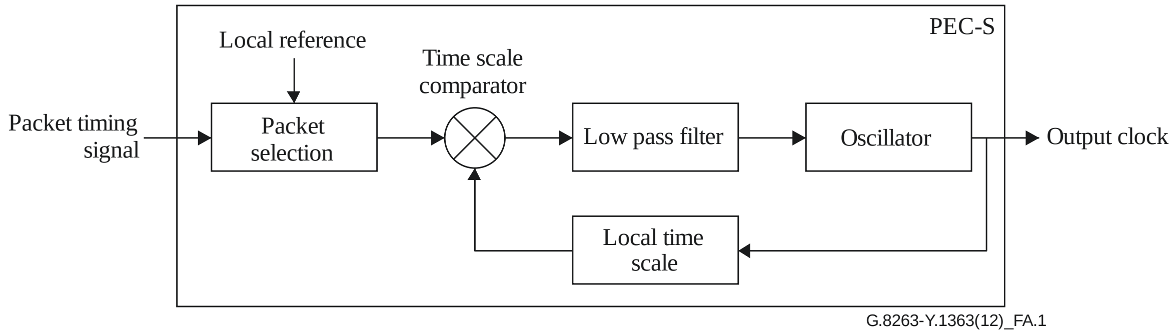


Figure A.1 – Functional model of a packet-based equipment clock – slave – frequency

Appendix I

Packet delay variation noise tolerance – testing methodology

(This appendix does not form an integral part of this Recommendation.)

While suitable test signals that check conformance to the masks in [ITU-T G.8261.1] (case 3 of [ITU-T G.8261.1], as defined in reference point D in Figure 3 of [ITU-T G.8261.1]) are being studied, the testing methodologies described in clause I.2 can be used to generate suitable PDV test patterns. As such, the applicable mask is that which is shown in Table 1 and Figure 4 of [ITU-T G.8261.1]; no other masks are appropriate.

These methodologies are applicable only to HRM-1 of [ITU-T G.8261.1]. Suitable methodologies for HRM-2 are for further study. Other methodologies for generating suitable test signals that check conformance to the masks in [ITU-T G.8261.1] for HRM-1 are also possible; this is for further study.

I.1 Testing set-up for packet delay variation noise tolerance testing

The general testing set-up for PDV noise tolerance testing is shown in Figure I.1.

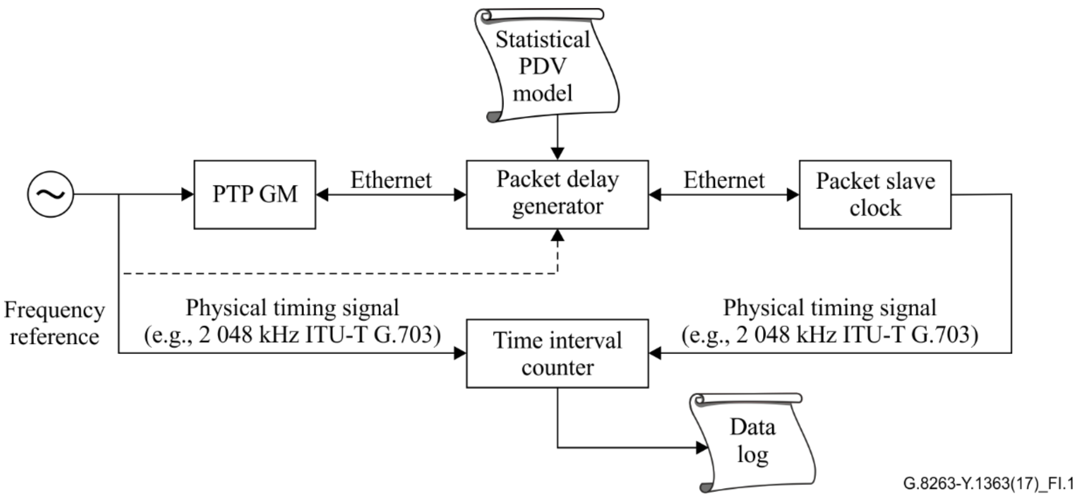


Figure I.1 – Packet delay variation noise tolerance testing set-up

NOTE – The dotted line between the "Frequency reference" and the "Packet delay generator" block is optional.

The whole experiment is timed by a frequency reference clock, e.g., a caesium PRC. This generates the input reference for a precision time protocol (PTP) grandmaster (GM). The Sync messages generated by the PTP GM are delayed by a packet delay generator, and correspondingly the Delay_Request messages generated by the packet slave clock are also delayed using the same packet delay generator.

The delay sequences are generated by means of a statistical model, with the parameters chosen to generate a delay distribution with properties similar to the network limits criterion defined in [ITU-T G.8261.1] (i.e., for HRM-1: 1% of the packets experiencing a delay within 150 µs of the minimum delay in each observation interval of 200 s). Several methodologies for generating suitable PDV patterns are possible, some of which are described for information purposes in clause I.2.

In general, it is recommended that the two delay sequences for the Sync and Delay_Request messages be similar in properties, being generated using the same statistical model, but not identical. This avoids correlation effects where the sequences use similar values at the same time.

The packet slave clock generates a physical output timing signal (e.g., a 2 048 kHz ITU-T G.703 signal) which is compared back to the timing signal from the frequency reference by a time interval counter. The data log can then be compared to the output mask defined in Figure 4 of [ITU-T G.8261.1] to check the compliance of the slave.

The test procedure is to be carried out under constant temperature conditions (within ±1 K): Any stress testing under a noisy thermal environment is for further study.

When measuring PDV tolerance, the PDV test pattern should start to be applied before communication between the packet master clock and the packet slave clock is established. This order of operations will ensure that all "Event" packets are impacted by the PDV test pattern.

NOTE 1 – A stabilization period is required when applying the PDV test patterns to the packet slave clock, before verifying the output signal produced by the packet slave clock is within acceptable limits. The duration of this stabilization period is for further study.

NOTE 2 – In general, it is the intention of PDV tolerance testing that the packet slave clock does not have prior knowledge of packet master clocks from previous measurements. In a practical test set-up, steps may be taken to ensure that the packet slave clock does not have this prior knowledge. For example, the packet slave clock may need to be restarted or even power cycled between measurements. However, it should be noted that in the case of power cycling, the required stabilization period will likely increase.

NOTE 3 – The recommended warm-up time of the equipment should be followed when performing the PDV tests.

I.2 Test methodologies

Three methods for generating suitable PDV test patterns that check conformance to the masks specifying the PDV network limits in [ITU-T G.8261.1] for HRM-1 are described in this clause based on:

– flicker noise;

– combined sinusoidal waveforms;

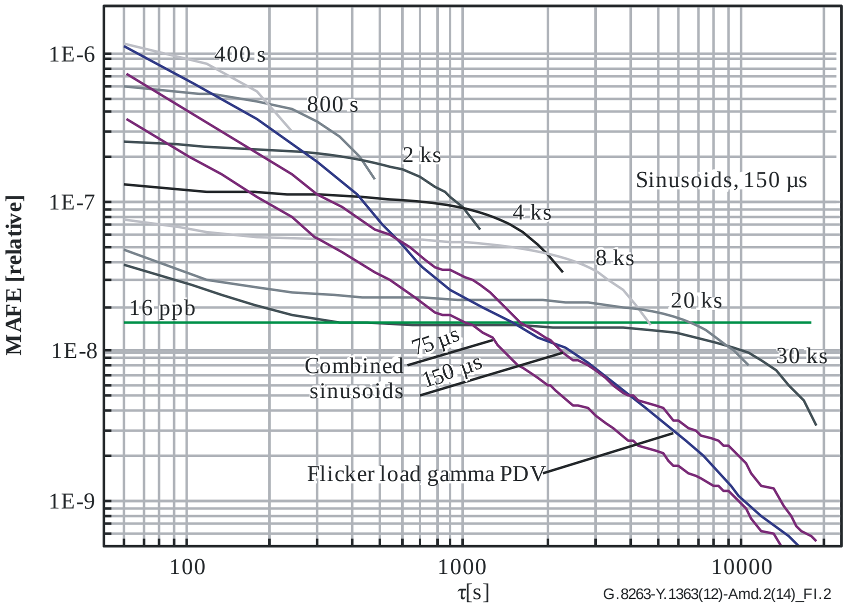
– a single sinusoidal waveform.

Indications for the rationale for using each method are given in each relevant subclause. Table I.1 summarizes the pros and cons of each method.

Table I.1 – Comparison of packet delay variation noise tolerance testing methods

Method	Pros	Cons
Flicker noise	Simple test, with limited duration Emulates some typical characteristics of packet networks	Does not take into account complex or extreme network scenarios, e.g., with floor delay movements
Combined sinusoidal waveforms	Simple test, with limited duration Emulates some typical characteristics of packet networks Includes floor delay movements, emulating moderate variations of traffic load	Does not take into account extreme network scenarios, e.g., low-noise delay floor moving full swing, defined by the network limit in a worst-case time frame
Single sinusoidal waveform (optional)	Stress test corresponding to worst case scenarios, with extreme variations of the load (e.g., up to 100% of output ports capacity in all the nodes of the network), with important floor delay movements May in some cases allow determination of the slave clock bandwidth	Long test duration when low frequencies are used Does not emulate typical characteristics of real networks

Figure I.2 summarizes the maximum average frequency error (MAFE) curves of the delay test patterns using 1% minimum selection and a 60 s selection window. The PDV patterns represented by curves at higher τ values require higher stability of the clock in order to remain within the clock output limit.



NOTE – The applicable network limit values are stated in microseconds.

Figure I.2 – Maximum average frequency error curves of the test patterns

NOTE – The generation of PDV patterns that implement the maximum tolerance allowed are artificially generated with these methods. As such, they may not represent PDV that may exist or occur in a real deployment or PDV that would be generated as a result of a packet timing master sending packets across a packet network. Some of the methodologies described to generate PDV patterns, especially the third (single sinusoidal waveform), may prevent use of the full benefits of advanced filtering techniques. As a result, in order to successfully tolerate these artificial PDV patterns, a narrower clock bandwidth and a local oscillator that is very stable may be required.

I.2.1 Packet delay variation patterns based on flicker noise

The method for generating PDV patterns described in this clause consists of a combination of flicker noise with a probability density function given by a Γ-distribution as a statistical model of PDV.

I.2.1.1 Purpose and applicability

This method is based on a simplified statistical model for a network experiencing bursty traffic. Previous studies of Internet traffic ([b-Barnes, 1992], [b-Barnes, 1971]) have shown that the traffic distribution is bursty at many different scales, and that this self-similar behaviour can be represented by using flicker noise to modulate the traffic load. Secondly, it can be shown that the queueing action of a packet switch or router imposes A Γ-distribution on the probability density function of the delays through the switch or router.

The resulting statistical model is shown schematically in Figure I.3.

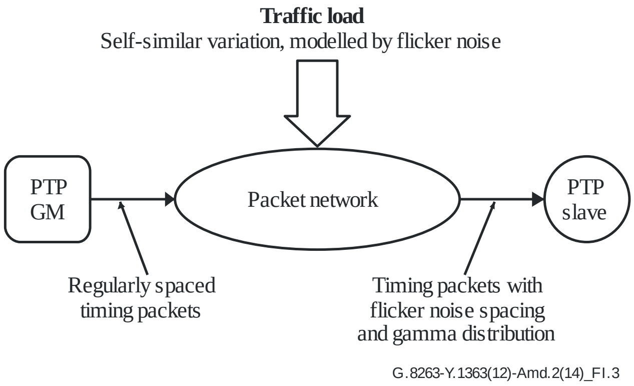


Figure I.3 – Statistical model of packet delay variation for timing packets

It does not include the potential transients which can occur in packet networks, such as floor delay steps or floor delay variations. In addition, it may not model accurately a network which has significant non-bursty traffic [e.g., constant bit rate (CBR) traffic].

This method is therefore considered suitable as a minimum test for characterizing the noise tolerance of a packet slave clock. Additional testing is recommended to ensure that the packet slave clock will tolerate more complex network situations with transients.

I.2.1.2 Parameters and example

The parameters of the PDV pattern, including the standard deviation of the flicker pattern and the α and β parameters of the Γ-function, are related to physical characteristics of the network, such as the total load on the network, the individual load on the output port of each switch, and the number of switches in the network.

The procedure for defining a PDV sequence is as follows:

1) produce a flicker sequence representing values of load between 0% and 100%;
2) map the individual values of load in the flicker sequence to PDV Γ-distributions specified by α, β and ρ.

I.2.1.3 Generation of the flicker sequence of load values

The flicker sequence of load values is generated by using the technique of Barnes, Jarvis and Greenhall. The technique is described in [b-Barnes, 1992], with additional details and generalizations given in [b-Barnes, 1971] and [b-Corsini]. In this technique, a sequence of independent and identically distributed random samples is input into a bank of cascaded lead or lag filters whose frequency response approximates a transfer function that is inversely proportional to the square root of *f*, i.e.:

$$H(f) = \frac{1}{\sqrt{f}} \tag{I-1}$$

where *f* is the Fourier frequency and *H*(*f*) is the frequency response. If white noise, with constant power spectral density (PSD) *A*, is input to this filter, the PSD of the output is:

$$S_{\text{out}}(f) = \left|H(f)\right|^2 A = \frac{A}{f} \tag{I-2}$$

The PSD given by Equation (I-2) represents flicker noise, i.e., it is proportional to 1/*f*.

The bank of lead or lag filters is sometimes referred to as a Barnes–Jarvis–Greenhall filter, and each lead or lag filter in the bank is sometimes referred to as a stage of the Barnes–Jarvis–Greenhall filter. Each stage has approximately constant gain at low frequency and high frequency, with the low-frequency gain greater than the high-frequency gain and a −20 dB/decade transition between the low- and high-frequency regions. This results in a frequency response for the Barnes–Jarvis–Greenhall filter that resembles a series of "steps", i.e., flat levels connected by −20 dB/decade slopes. The spacing of the poles and zeros of the stages are chosen so that the gain is inversely proportional to the square root of frequency. The number of stages and spacing of the poles and zeros determines the range of frequency over which the filter operates, i.e., the implementation of the filter is in the discrete domain (see below) and the filter operates over a finite frequency range. Finally, the filter transfer function is multiplied by a constant whose value is chosen to achieve the desired level (i.e., in Equation (I-1), the magnitude of the frequency response is 1 at $f = 1$ Hz).

The Barnes–Jarvis–Greenhall filter is implemented in discrete time as follows (see [b-Barnes, 1971]). Let M equal the number of stages, and let $Y_n^{(k)}$ be the state of stage k at time step n. Then the discrete-time state equations for the filter are:

$$\begin{aligned} Y_n^{(1)} &= \phi^{(1)} Y_{n-1}^{(1)} + P_n \\ Y_n^{(2)} &= \phi^{(2)} Y_{n-1}^{(2)} + Y_n^{(1)} - \theta^{(2)} Y_{n-1}^{(1)} \\ &\vdots \\ Y_n^{(k)} &= \phi^{(k)} Y_{n-1}^{(k)} + Y_n^{(k-1)} - \theta^{(k)} Y_{n-1}^{(k-1)} \\ &\vdots \\ Y_n^{(M)} &= \phi^{(M)} Y_{n-1}^{(M)} + Y_n^{(M-1)} - \theta^{(M)} Y_{n-1}^{(M-1)} \end{aligned} \tag{I-3}$$

The filter states are initialized to zero, i.e.:

$$Y_0^{(k)} = 0, \quad k = 1, 2, ..., M \tag{I-4}$$

The filter coefficients are given by:

$$\begin{aligned} &R = 2.5 \\ &\phi^{(1)} = 0.13 \\ &\omega^{(1)} = \frac{1 - \phi^{(1)}}{\sqrt{\phi^{(1)}}} \\ &\text{and for } k = 1, 2, ..., M: \\ &\omega^{(k)} = \frac{\omega^{(1)}}{R^{k-1}} \\ &\theta^{(k)} = 1 + \frac{\omega^{(k)} \left[\omega^{(k)} - \sqrt{\left(\omega^{(k)}\right)^2 + 4} \right]}{2} \\ &\mu^{(k)} = \frac{\omega^{(k)}}{R} \\ &\phi^{(k)} = 1 + \frac{\mu^{(k)} \left[\mu^{(k)} - \sqrt{\left(\mu^{(k)}\right)^2 + 4} \right]}{2} \end{aligned} \tag{I-5}$$

The output of the final stage, $Y_k^{(M)}$, is the flicker noise process. The P_n are samples of a zero-mean, discrete-time white noise process. The standard deviation of this process determines the level of the flicker noise process. The quantity R determines the spacing between the successive poles and zeros.

It has been found that choosing R = 2.5 and M = 8 can produce flicker noise over five decades of time; this has been verified by simulating flicker noise with these values of R and M [and $\phi^{(1)} = 0.13$], computing the time deviation (TDEV) statistic, and verifying that TDEV has flicker noise dependence (i.e., is approximately constant over the observation interval).

The foregoing indicates that the process P_n is white, i.e., the successive samples are statistically independent. In many applications, P_n also is Gaussian; however, in the case here it is convenient to take the P_n as having a probability distribution that is uniform over the range [0,1]. It is desired that the load values also be in this range (i.e., 0% – 100%). However, choosing the P_n to be in the range [0,1] does not guarantee that the output of the Barnes–Jarvis–Greenhall filter (i.e., the $Y_n^{(M)}$) will also be in this range. Nonetheless, load values that are in the range [0,1] can be obtained by scaling the $Y_n^{(M)}$ as follows. Assume that the Barnes–Jarvis–Greenhall filter has been used to generate N flicker noise samples $Y_n^{(M)}$, $n = 1, 2, 3, \ldots, N$. Let $Y_{\max}^{(M)}$ and $Y_{\min}^{(M)}$ be the maximum and minimum of these samples, respectively. Then the load value, $X_n^{(M)}$, corresponding to the nth sample is given by:

$$X_k^M = \frac{Y_k^M - Y_{\min}^M}{Y_{\max}^M - Y_{\min}^M} = 100 \cdot \frac{Y_k^M - Y_{\min}^M}{Y_{\max}^M - Y_{\min}^M} \% \qquad \text{(I-6)}$$

Note that, for this method of scaling the output values of the Barnes–Jarvis–Greenhall filter, there will be exactly one load value of 0%, one load value of 100%, and each successive load will be different from the previous value.

Finally, the samples uniformly distributed over the range [0,1] are generated using a random number generator. The cycle length of the random number generator must be at least as long as the desired number of phase samples, to ensure that the samples exhibit the properties of an independent random process.

The flicker characteristic of a data set is seen in the TDEV calculation as zero slope. This is illustrated in Figure I.4, which is a plot of TDEV for a PDV pattern generated using the methodology described here and below.

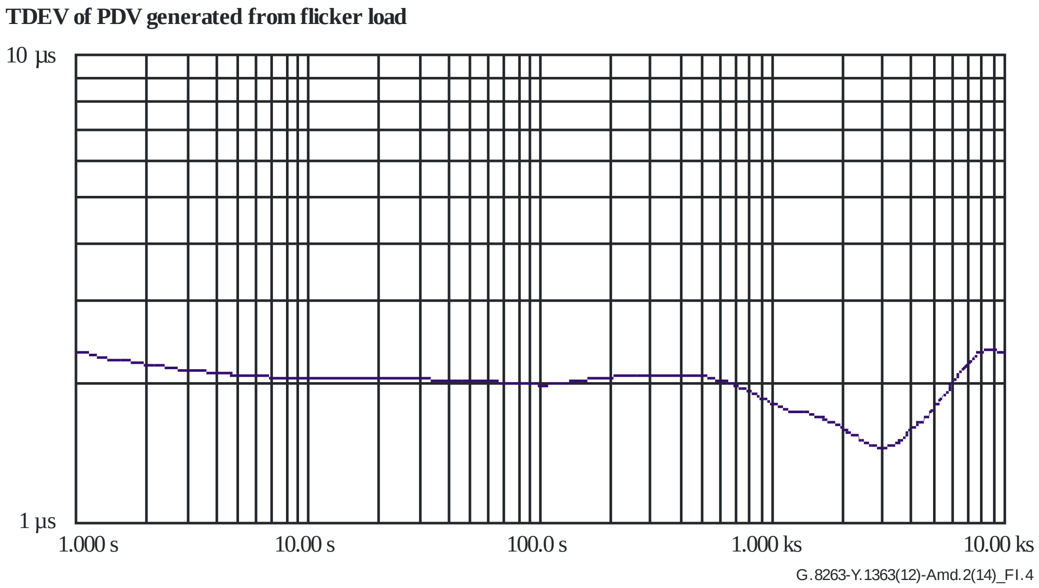


Figure I.4 – Time deviation of packet delay variation generated from flicker load

I.2.1.4 Γ-distribution generation

A Γ-distribution is defined by two parameters, α and β. A third parameter, ρ, is needed to represent offset. This is because in its pure form, the Γ-distribution has a minimum of zero, whereas minimum network packet delay for any particular scenario is a number greater than zero. The probability density function for the Γ-distribution based on these parameters is as follows:

$$p_X(x) = \frac{1}{\Gamma(\alpha)} \beta^{\alpha} (x-\rho)^{\alpha-1} e^{-\beta(x-\rho)}, \qquad x \geq \rho \tag{I-7}$$

where X is the random Γ-variable and x is the independent variable of the distribution.

Fitting a set of measurement data to a Γ-distribution involves invoking a process of determining the three parameters, α, β and ρ. The first step, after determining ρ is to shift the data set to the classic Γ position by subtracting ρ. In other words, ρ is assigned to zero instead. Having done this shift, there are then various methods for calculating α and β from the data. One such procedure is the *method of moments* and another is *maximum likelihood estimation*.

The *method of moments* procedure will be described here. The first step is to calculate the first and second moments m_1 and m_2 of the distribution, that is, to estimate the expected value of random variable, E(X), and the expected value of the square of the random variable, E(X^2). These moments m_1 and m_2 can be estimated using Equations (I-8) and (I-9).

$$m_1 = (X_1 + \cdots + X_n)/n \tag{I-8}$$

$$m_2 = (X_1^{\,2} + \cdots + X_n^{\,2})/n \tag{I-9}$$

The relationship between these moments and α and β is shown in Equations (I-10) and (I-11).

$$\alpha\beta = m_1 \tag{I-10}$$

$$\beta^2\alpha(\alpha + 1) = m_2 \tag{I-11}$$

Solving for α and β yields Equations (I-12) and (I-13).

$$\alpha = m_1^{\,2}/(m_2 - m_1^{\,2}) \tag{I-12}$$

$$\beta = (m_2 - m_1^{\,2}) / m_1 \tag{I-13}$$

To define a relationship between load and the three Γ-distribution parameters, measurement data from an ITU-T G.8261.1 HRM-1 network with load incremented from 0% to 100% in 1% steps. The PDV data for each of these steps was then fitted for the α, β and ρ parameters.

For the modelling, the overall minimum (57.32 µs in this case) was subtracted from the data. Then α and β were calculated with a Γ-distribution fit after subtracting ρ (minimum) from each segment. The approach then is to derive a closed-form solution for the three parameters α, β and ρ. For that purpose, the 100% point was kept as a special case, as a floor step occurred at 100% load (the floor moved to 95 µs above the minimum floor with the one percentile 114 µs above the minimum floor), and the points from 1% to 99% were used for curve fitting. High-order polynomials (6th order) were fitted to the three sets of points, the α, β and ρ sequences. Thus the equations are of the form:

$$y = Ax^6 + Bx^5 + Cx^4 + Dx^3 + Ex^2 + Fx + G \tag{I-14}$$

where x is the load value expressed as a percentage (i.e., x ranges from 0 to 100).

The original α, β and ρ data along with fitted curves are shown in Figures I.5, I.6 and I.7.

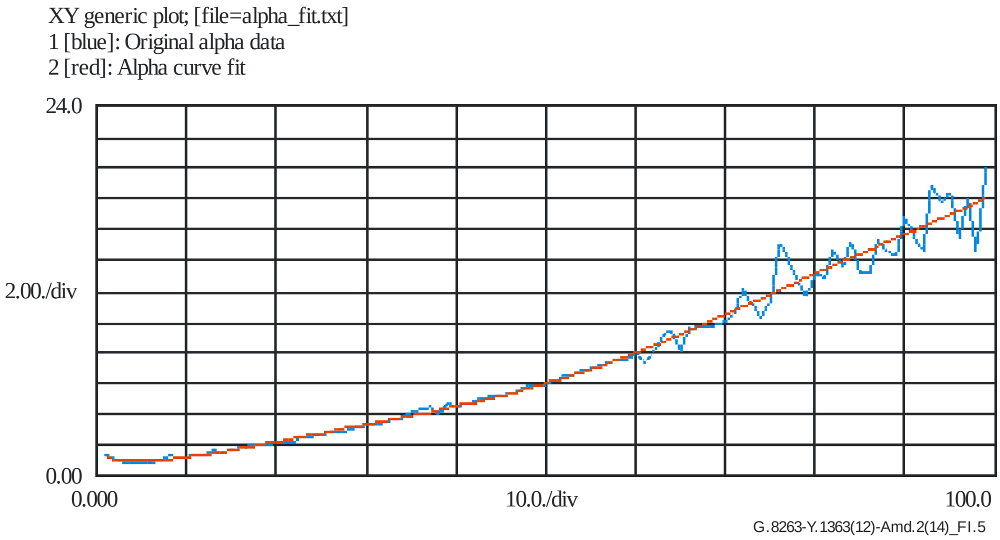


Figure I.5 – α-Data

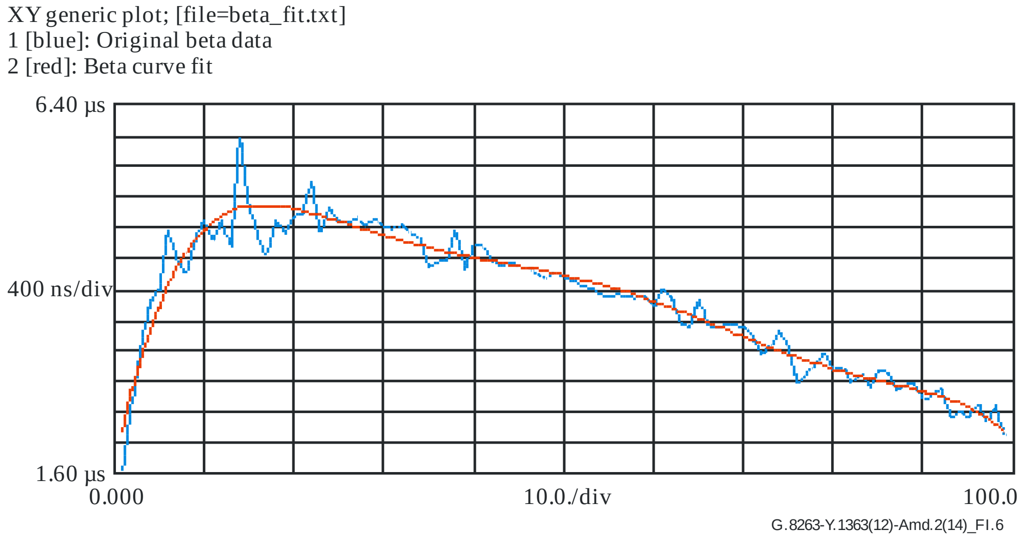


Figure I.6 – β-data

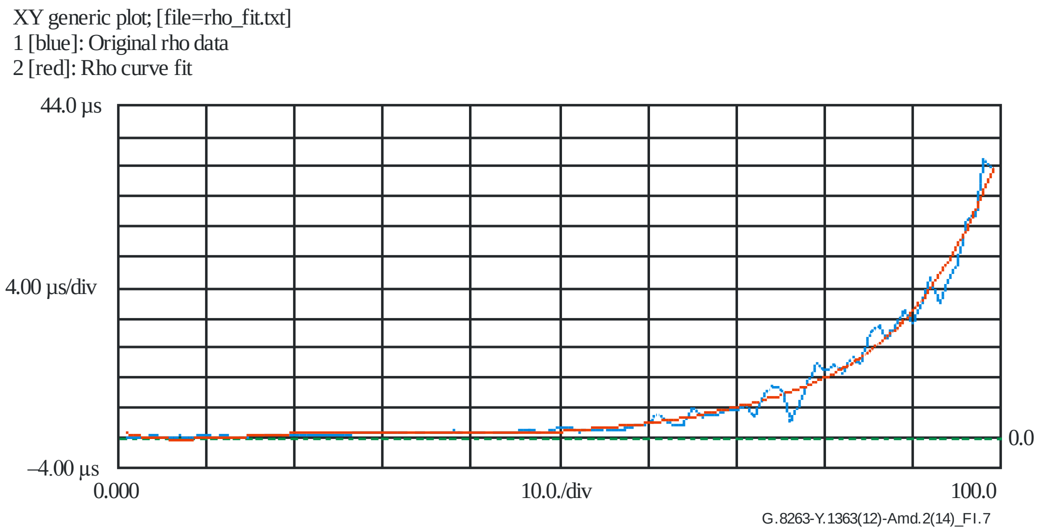


Figure I.7 – ρ-Data

The derived polynomial parameters are listed in Table I.2 (note that for higher order polynomial equation coefficients, it is important to maintain the large number of digits, as shown in Table I.2).

Table I.2 – Derived polynomial parameters

	α	*β*	*ρ*
A	3.0302171048327E-10	−3.7527709385196E-16	1.0843935243576E-15
B	−9.7822643361772E-08	1.2590219237780E-13	−2.8578719666972E-13
C	1.1854660981753E-05	−1.6595170368502E-11	2.9508400604002E-11
D	−6.6624332958641E-04	1.0886566230108E-09	−1.4410536532614E-09
E	1.8713517871851E-02	−3.7186572402355E-08	3.3119857891960E-08
F	−1.4120879264166E-01	5.9390899042069E-07	−2.9200865252098E-07
G	1.3306420437613E+00	1.6110589771449E-06	8.1781119355525E-07

To take a specific example, for load = 60%, the value 60 is applied to the equations; and

$$\alpha = 8.0255194029732E+00$$

$$\beta = 3.8429770506754E-06$$

$$\rho = 2.0554033188099E-06$$

The equations apply for load values up to 99. For load values above 99, the 100% load values are used:

$$\alpha = 2.0132036140218E+01$$

$$\beta = 2.96693980102245E-06$$

$$\rho = 5.59439990063761E-05$$

The three equations for α, β and ρ, along with the special case α, β and ρ values for loads above 99%, are then applied to a flicker sequence with a load ranging between 0% and 100%. The minimum PDV value of 57.32 µs originally subtracted from the data is added back in.

I.2.1.5 Flicker load packet delay variation Γ-sequence

A flicker sequence of 360 values, each corresponding to a 4 min duration, and with each value used to produce a corresponding Γ-distribution using the relations described in clause I.2.1.4, produces a 24 h sequence. The resulting PDV sequence is shown in Figure I.8, along with a plot of the one-percentile taken over 200 s windows. The maximum is 146.35 µs, which is 89.03 µs above the 57.32 µs floor.

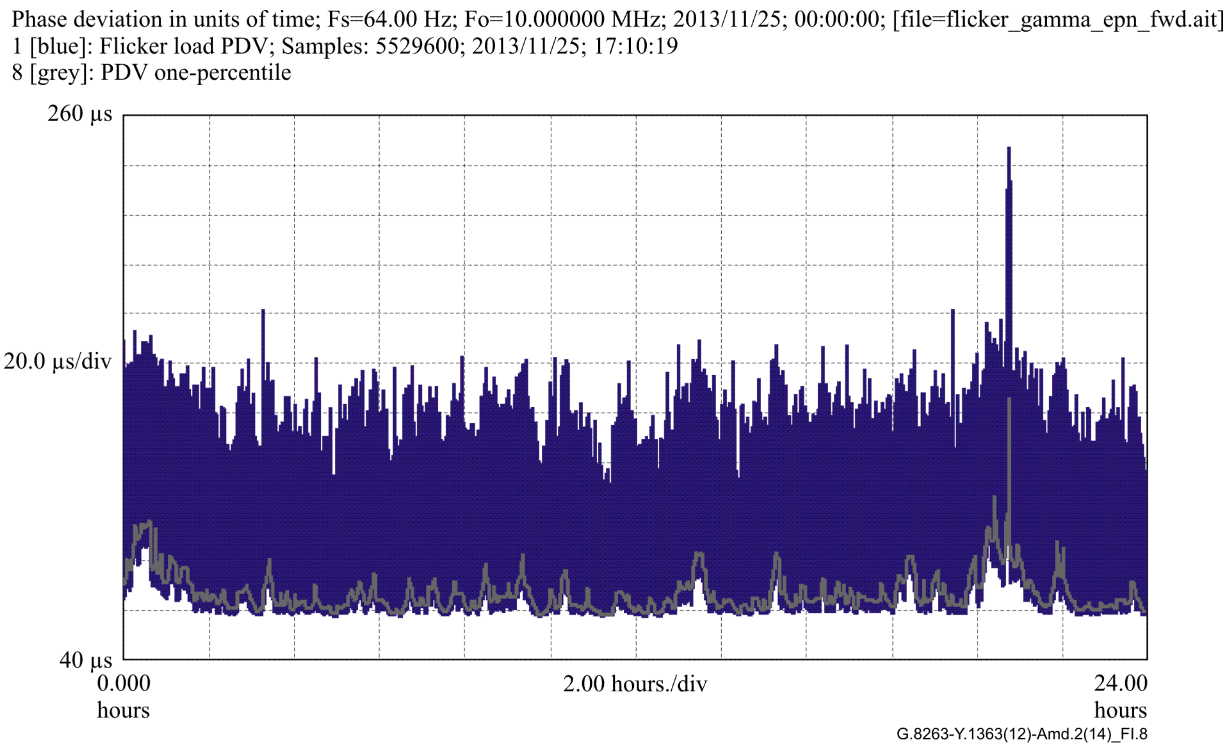


Figure I.8 – Packet delay variation one-percentile

I.2.2 Packet delay variation patterns based on combined sinusoidal waveforms

The method for generating PDV patterns described in this clause consists of a combination of sinusoidal waveforms, namely summing sinusoidal test patterns, and normalizing the resulting pattern into the network limit specified in [ITU-T G.8261.1]. The sinusoidal test patterns are described in clause I.2.3, Steps 1 and 2 where each sinusoid is composed of a 145 µs sine function added together with a 1 ms noise pattern where the combination satisfies the 150 µs network limit.

I.2.2.1 Purpose and applicability

The single-frequency sinusoidal patterns are worst-case patterns that can be derived from the ITU-T G.8261.1 network limit. Since such patterns do not exist in real networks, another test pattern based on summing up the sine waves can be created. Even though the pattern is still artificial and does not include all PDV statistics that can be encountered, it more closely resembles real network behaviour. Another reason to create such patterns is that a single pattern containing multiple frequency components is faster to run than a test sequence where the different sinusoidal patterns are run consecutively.

I.2.2.2 Parameters and example

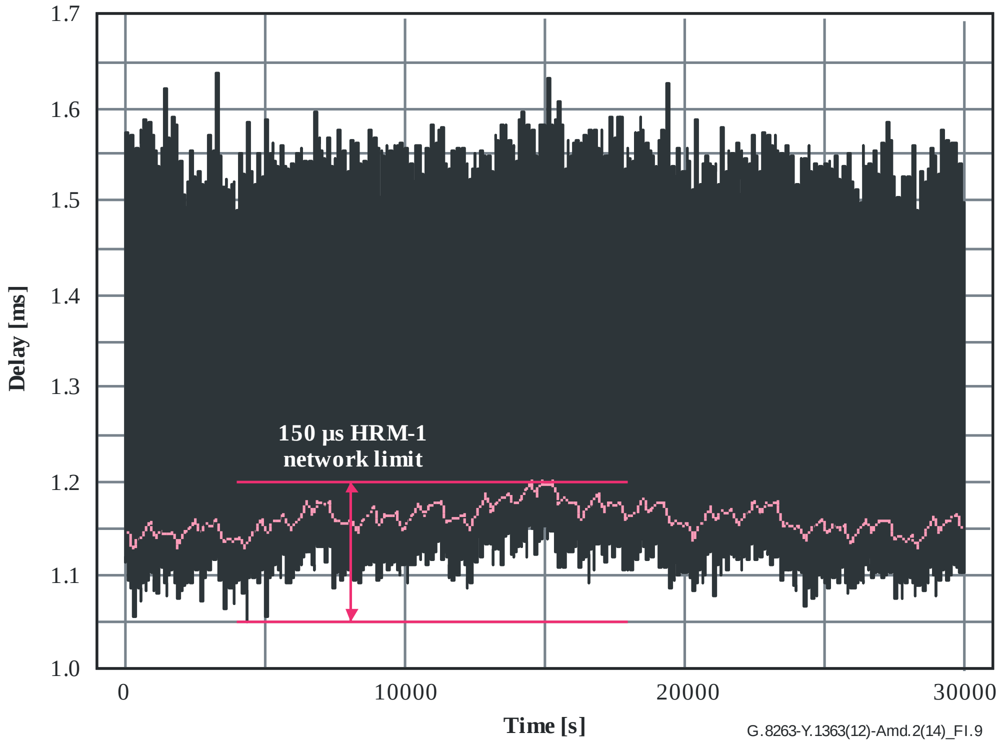
In real networks, there is a distinct diurnal pattern. To mimic this pattern, the sine-wave components with the longest periods are set into phases where they reach maxima at the same time. The three longest periods are 30 ks, 20 ks, and 8 ks and they are aligned to reach a peak at 15 ks. The other periods, 4 ks, 2 ks, 800 s, 400 s, 200 s, 100 s, and 50 s are slightly phase shifted so that the same phase does not occur simultaneously in multiple components. The phases are summarized in Table I.3.

Table I.3 – Phases of the summed sine wave components

Period	30 ks	20 ks	8 ks	4 ks	2 ks	800 s	400 s	200 s	100 s	50 s
Sine phase 0° at	7.5 ks	10 ks	5 ks, 13 ks	1.5 ks	1 ks	600 s	0 s	0 s	50 s	25 s

After adding the patterns together, the values are divided by a normalizing factor so that in all 200 s windows at least 1% of packets are within the network limit specified in [ITU-T G.8261.1].

Figure I.9 provides an example of a PDV pattern generated using a similar method.



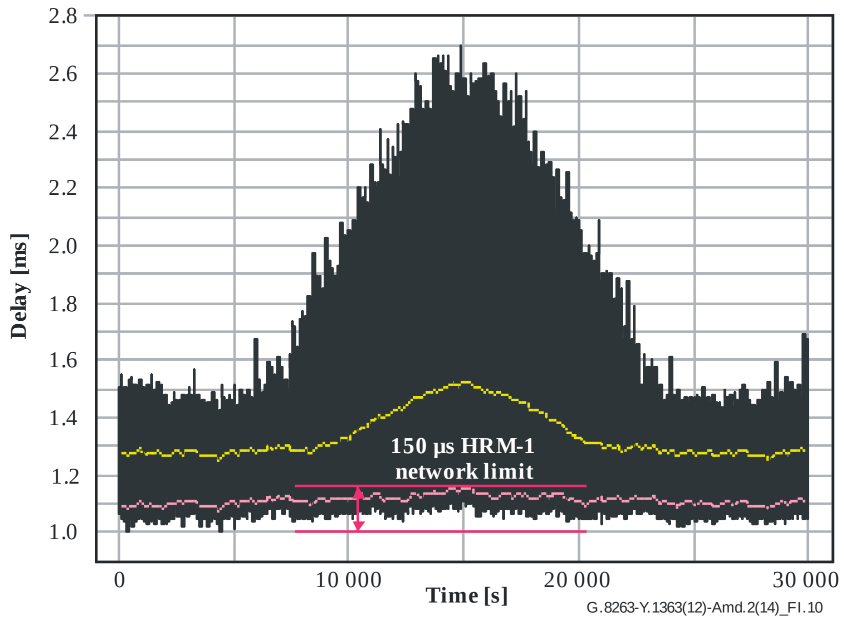
NOTE – The purple curve represents the 1% curve.

Figure I.9 – Packet delay variation pattern based on combined sinusoidal waveforms

I.2.2.3 Improving the pattern for testing packet selection capability of clocks

The sinusoidal test patterns exhibit a deficiency where clocks without packet filtering achieve the same or even slightly better performance than clocks that do packet filtering. This is because the average delay of all packets has the same or even smoother pattern than the average of the minimum delay packets.

The pattern can be enhanced by replacing a part of the values exceeding a 2% envelope by values that exhibit a pattern with a larger amplitude, as shown in Figure I.10. The fastest 2% of packets in each 200 s window may not be replaced. In this way, clocks without packet filtering will produce worse clock output than clocks with filtering. Various patterns can be used. However, the peak-to-peak amplitude of the average delay curve, calculated in 200 s windows, may be maximally 300 µs.



NOTE – The lower curve shows the 1% envelope and the upper curve shows the average delay.

Figure I.10 – Example of an enhanced packet delay variation pattern based on a combined sinusoidal waveform

I.2.3 Packet delay variation patterns based on a single sinusoidal waveform

The method for generating PDV patterns described in this clause consists of considering a single sinusoidal waveform to modulate the floor delay of random delays samples based on a power-law distribution. Several frequencies can be successively applied to test properties and the tolerance of the packet slave clock. It is an adaptation to PDV noise of the traditional methods used to characterize the noise tolerance of physical (PHY) layer clocks.

I.2.3.1 Purpose and applicability

This method does not intend to model typical network behaviour. However, the method may be useful in studying the detailed behaviour of packet clocks. By changing the period of the sinusoid, information can be obtained about the filter bandwidth of packet clocks. On the other hand, by varying the amplitude, information can be obtained about thresholds regarding linear and nonlinear regimes of the clocks. Note, however, that there are no requirements defined in [ITU-T G.8263] concerning this parameter.

I.2.3.2 Parameters and example

In order to modulate the floor delay of PDV samples using a sinusoidal waveform, the process described below is suggested.

Step 1:

A sinusoidal pattern is generated, and corresponds to the low frequency component applied to the floor delay. This sinusoidal pattern, $w(t)$, is defined with two parameters:

– A: characterizes the peak-to-peak of the sinusoidal waveform;

– T: characterizes the period of the sinusoidal waveform.

The sinusoidal pattern, is given by:

$$w(t) = \frac{A}{2}\left(1 + \sin\frac{2\pi t}{T}\right) \qquad \text{(I-15)}$$

The parameters A and T are chosen from Table I.4.

Step 2:

A PDV noise is added to the initial sinusoid, based on the following probability density function:

$$p(x) = \frac{1+\gamma}{Y}\left(1-\frac{x}{Y}\right)^{\gamma} \quad \text{(I-16)}$$

where Y is the amplitude of the noise and γ is a shape parameter. The corresponding cumulative probability distribution function is given by:

$$P(x) = \int_0^x p(u)\,\mathrm{d}u = 1-\left(1-\frac{x}{Y}\right)^{1+\gamma} \quad \text{(I-17)}$$

The following description describes usage in testing the tolerance of clocks to the HRM-1 network limit. However, it is not suggested that the pattern be used for compliance testing, because it is expected that such worst-case delay patterns never occur in practical HRM-1 networks.

To ensure that the number of samples in each window with delays less than 150 μs is close to 1% of the total number of samples in the window (i.e., that any differences from 1% are due only to statistical variability), either the amplitude Y or the shape parameter γ of the distribution of step 1 may be varied with time. If Y is varied with time, it is given by:

$$Y(t) = \frac{150\,\mu\text{s} - w(t)}{1-(0.99)^{1/(1+\gamma)}} \quad \text{(I-18)}$$

where $w(t)$ is given by Equation (I-15) with A in microsecond and γ is chosen from Table I.4. If γ varies with time, it is given by:

$$\gamma(t) = \frac{\ln(0.99)}{\ln\left(1-\frac{150\,\mu\text{s} - w(t)}{Y}\right)} - 1 \quad \text{(I-19)}$$

where Y is chosen from Table I.4. Note that, if Equation (I-18) is used, $Y(t)$ may be outside the range in Table I.4 for some values of time, depending on the value of γ.

In addition, the quantities Y and γ may be kept fixed in time. In this case, both values are chosen from Table I.4.

NOTE 1 – If fixed Y and γ are used, they should be chosen so that the number of PDV samples in each window with delays less than 150 μs is close to 1% of the total number of samples in the window. This is especially important if step 3, which is optional, is not applied. The probability distribution given by Equations (I-15) and (I-16) may be obtained from a probability distribution that is uniform between 0 and 1 by a power-law transformation with exponent γ (i.e., $x = u^{\gamma}$), followed by a scaling by the factor Y, followed by a reflection about $x = Y/2$.

Step 3:

This step is optional. The delay samples of the resulting PDV pattern including the sinusoidal waveform are rearranged in order to ensure that 1% of the samples are below 150 µs for each 200 s window for the HRM-1 PDV network limits. This step is applicable to jumping (i.e., non-overlapping) windows.

NOTE 2 – This step is optional because the sinusoidally modulated PDV test pattern is not necessarily more challenging for the slave clock when the floor packet percentage (FPP) is smaller. For this test pattern, the portions of the test pattern that are easiest for the slave clock to tolerate are the portions at the peaks and troughs of the sinusoid, i.e., where the rate of change of the sinusoid is smallest and the floor does not change much from one window to the next. However, the peaks are also where the FPP is smallest.

If more than 1% of the samples in a window have delays less than 150 µs, then a number of samples, N, are selected randomly from those samples whose delays are less than 150 µs. Those samples are moved to values greater than 150 µs. The new value for each sample is selected randomly from a uniform distribution that ranges from 150 µs to the maximum delay from steps 1 and 2. The number of samples N is the largest number that still leaves 1% or more of the samples with delays less than 150 µs.

If fewer than 1% of the samples in a window have delays less than 150 µs, then a number of samples, N, are selected randomly from those samples whose delays are greater than 150 µs. Those samples are moved to values less than 150 µs. The new value for each sample is selected randomly from a uniform distribution that ranges from the value of the sinusoidal modulation of the minimum delay to 150 µs. The number of samples N is the smallest number that results in 1% or more of the samples with delay less than 150 µs.

Several resulting PDV patterns including the sinusoidal waveform are generated with varying periods T, and applied successively to the PEC-S slave clock.

Table I.4 provides a summary of the possible ranges to be considered for the parameters Y, γ, A and T when stressing a PEC-S for HRM-1 of [ITU-T G.8261.1]. Note that if Equation (I-18) is used, A, T and γ are chosen and Y is computed; if Equation (I-19) is used, A, T and Y are chosen and γ is computed.

Table I.4 – Lower limit of maximum tolerable sinusoidal input packet delay variation for HRM-1

Initial PDV noise parameters		**Sinusoidal waveform parameters**	
Y (µs)	γ	A (µs)	T (s)
[500, 10 000]	(−1, +4] (Note 1)	[0-150)	[200, 86 400]
NOTE 1 – γ Must be strictly greater than −1. If $\gamma = -1$, the probability density function of Equation (I-16) is identically 0, and if $\gamma < -1$, the probability density function is negative. NOTE 2 – The range of A does not include the endpoint 150 µs.			

Figure I.11 provides an example of a PDV pattern generated using this method, for the case where Y and γ are fixed in time:

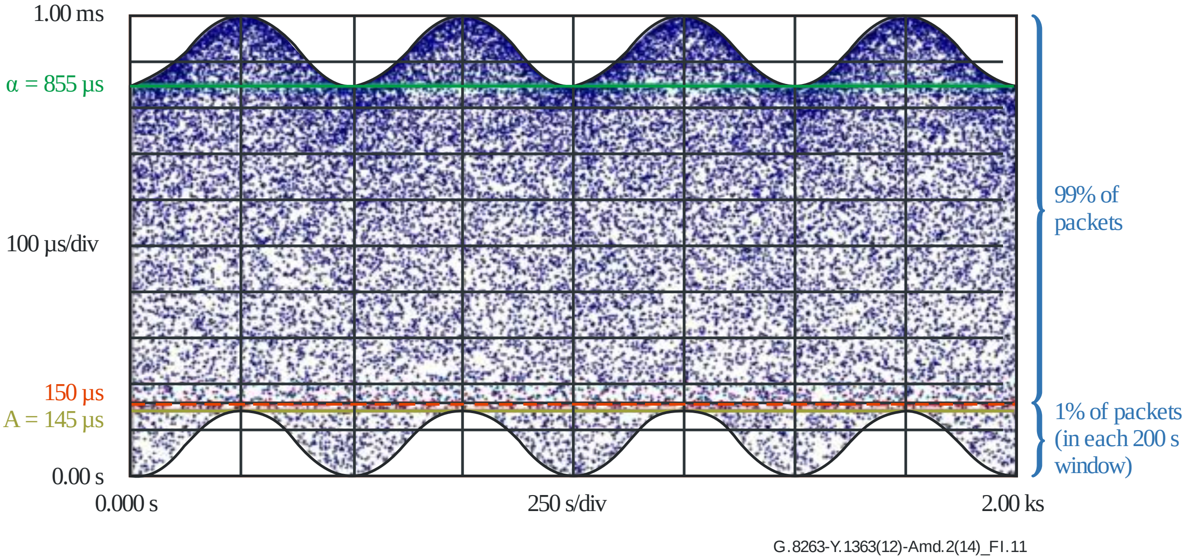


Figure I.11 – Example of a packet delay variation pattern based on a single sinusoidal waveform

(Y = 855 µs, γ = −0.5, A = 145 µs, T = 500 s)

Appendix II

Considerations on packet rates

(This appendix does not form an integral part of this Recommendation.)

This Recommendation does not require any specific packet rate for the packet based clock.

The applicable reference in the PEC-F-S case is [ITU-T G.8265.1] where the packet rate has been defined to be in the range of one packet every 16 s to 128 packets/s. It is not expected that a specific PEC-S-F implementation will meet the performance requirements over the whole of this range, and the actual value to be used depends on the stability of the oscillator, the traffic load and type of the network, and on the target application.

Experience has shown that for a PEC-S-F as specified in this Recommendation, packet rates higher than 1 packet/s are typically used to meet the requirements specified in case 3 of clause 7.2.2 of [ITU-T G.8261.1], when operated over a network similar to HRM-1 of [ITU-T G.8261.1].

The choice of a packet rate may significantly impact the requirements on the oscillator stability.

Note that the packet rate of interest for this Recommendation is during the steady state conditions (the start-up is out of scope).

Appendix III

Considerations on a packet-based equipment clock – slave – frequency time constant

(This appendix does not form an integral part of this Recommendation.)

This Recommendation does not require any specific time constant for the PEC-S-F packet-based clock. This Recommendation only requires that the relevant output performance objectives specified in [ITU-T G.8261.1] (e.g., Figure 4 of [ITU-T G.8261.1]) are respected when the input PDV noise applied to the PEC-S-F is within the PDV network limits specified in [ITU-T G.8261.1] (e.g., clause 8 of [ITU-T G.8261.1]).

NOTE 1 – The time constant, τ_c, is related to the 3 dB bandwidth of the PLL, $f_{3\,dB}$, by the following relationship: $\tau_c = 1/(2\pi\, f_{3\,dB})$.

Studies have been performed considering a PEC-S-F following the packet-based slave clock functional model defined in Annex A, based upon a second order phase-locked loop, in order to determine appropriate time constant values. In these studies, PDV data in line with the HRM-1 network limit defined in [ITU-T G.8261.1] have been considered.

These studies have shown that a time constant considerably higher than traditional clocks based on the PHY layer [e.g., synchronous digital hierarchy equipment clock/synchronous Ethernet equipment clock; (SEC/EEC)], of the order of 1 ks or more, may be necessary to meet the requirements of Figure 4 of [ITU-T G.8261.1].

NOTE 2 – The time constant of a given PEC-S-F implementation also depends on the budget allocated to the oscillator noise, which is especially related to the variable temperature effects. Oscillator noise, caused by aging and environmental effects, can indeed limit the practical performance of a PEC-S-F and should therefore be taken into consideration.

The PEC-S-F acts as a low-pass filter for input noise whilst acting as a high-pass filter for oscillator noise. For a given oscillator performance, the selection of the loop time constant represents a compromise between the practical attenuation of input noise and the admittance of oscillator noise.

If the target performance of the PEC-S-F corresponds to the requirements of Figure 4 of [ITU-T G.8261.1], the long-term fractional frequency offset of the output (i.e., as measured at observation intervals greater than 1 125 s) should not exceed 16 ppb under applicable input noise conditions and under the applicable environmental conditions, and throughout the lifetime of the oscillator.

To separate the influence of the oscillator from the influence of the input noise, two particular operating conditions can be considered: firstly, for a candidate time constant in the PEC-S-F, the influence of the oscillator could be found using minimum levels of input noise; in such a case, a target objective of x ppb long-term fractional frequency offset could be used to set a minimum performance for the oscillator. The time constant of the PEC-S-F can then be chosen so that the long-term fractional frequency offset of the output remains below $(16 - x)$ ppb under applicable input noise conditions within the PDV network limits when using an ideal oscillator.

Note that the time constant of interest for this Recommendation, and discussed in this appendix, is during the steady state conditions (the start-up is out of scope).

Appendix IV

Variable temperature testing methodology

(This appendix does not form an integral part of this Recommendation.)

Where variable temperature testing is required, it should be conducted using the temperature profile shown in Figure IV.1.

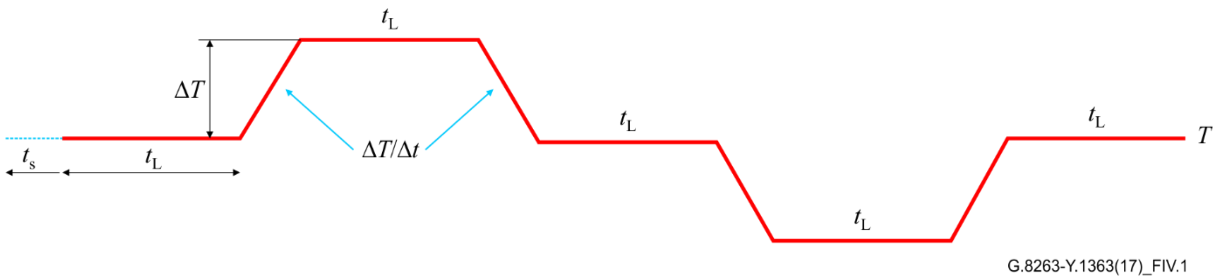


Figure IV.1 – Temperature profile

The test should be repeated at different test reference temperatures, *T*, to cover the required temperature range. As a minimum the tests should be performed at nominal and temperature extremes, i.e., the reference temperature *T* set to $T_{min} + \Delta T$, T_{nom} and $T_{max} - \Delta T$.

The test stabilisation time t_s should be long enough to remove start-up effects. The loop recovery time t_L is dictated by the loop time constant and should be, as a minimum, three times the loop time constant to allow the loop to recover.

The constrained temperature excursion ΔT and the ramp rate $\Delta T/\Delta t$ should aligned to the environmental profile.

As an example, the constrained temperature excursion ΔT could be set to 20 °C and the ramp rate $\Delta T/\Delta t$ to 0.5°C/minute, if these are the applicable environmental conditions.

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