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# The control of jitter and wander within digital networks which are based on the 1544 kbit/s hierarchy

ITU-T Recommendation G.824

(Formerly CCITT Recommendation)

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**ITU-T Recommendation G.824**

# The control of jitter and wander within digital networks which are based on the 1544 kbit/s hierarchy


## Summary

This ITU-T Recommendation specifies the maximum network limits of jitter and wander that shall not be exceeded at relevant transport or synchronization network interfaces and the minimum equipment tolerance to jitter and wander that shall be provided at any relevant synchronization or transport interface.

The requirements for jitter and wander characteristics that are specified in this ITU-T Recommendation must be adhered to ensure interoperability of equipment produced by different manufacturers and satisfactory network performance.



## Source

ITU-T Recommendation G.824 was revised by ITU-T Study Group 13 (1997-2000) and approved under the WTSC Resolution 1 procedure on 10 March 2000.

## Keywords

Clocks, input jitter tolerance, input wander tolerance, network limits, output jitter, output wander, synchronization, timing.

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In some areas of information technology which fall within ITU-T's purview, the necessary standards are prepared on a collaborative basis with ISO and IEC.

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## CONTENTS

## Introduction and background

In a transport network, jitter and wander accumulate on data paths according to the jitter and wander generation and transfer characteristics of each piece of equipment interconnected. This equipment may include different types of multiplexers/demultiplexers, cross-connects and line systems, for example.

An excessive amount of jitter and wander can adversely affect both digital signals (e.g. by generation of bit errors, uncontrolled slips and other abnormalities) and analogue signals (e.g. by unwanted phase modulation of the transmitted signal). The consequences of such impairment will, in general, depend on the particular service that is being carried and the terminating or adaptation equipment involved.

It is therefore necessary to set limits on the magnitude of jitter and wander at network interfaces, in order to guarantee proper quality of the transmitted signals and a proper design of the equipment.

**ITU-T Recommendation G.824**

# The control of jitter and wander within digital networks which are based on the 1544 kbit/s hierarchy

## 1 Scope

This ITU-T Recommendation specifies the relevant parameters and their limiting values that are able to satisfactorily control the amount of jitter and wander present at synchronous digital hierarchy (SDH) and plesiochronous digital hierarchy (PDH) network-node interfaces (NNI) based on the 1544 kbit/s hierarchy.

An excessive amount of jitter and wander can adversely affect both digital (generation of bit errors, uncontrolled slips) and analogue signals (unwanted phase modulation of the transmitted signal). It is therefore necessary to set limits to the presence of jitter and wander at the network interfaces, in order to guarantee a proper quality of the transmitted signals.

The scope of this ITU-T Recommendation is to define the parameters and the relevant values that are able to control satisfactorily the amount of jitter and wander present at PDH network interfaces.

The electrical characteristics of the relevant network interfaces are described in ITU-T Recommendation G.703.

The jitter and wander control philosophy is based on the need:

a) to recommend a maximum network limit that should not be exceeded at any relevant interface (i.e. jitter and wander transfer, generation, and tolerance);

b) to recommend a consistent framework for the specification of individual digital equipment;

c) to provide sufficient information and guidelines for organizations to measure and study jitter and wander accumulation in any network configuration.

## 2 References

The following ITU-T Recommendations and other references contain provisions which, through reference in this text, constitute provisions of this Recommendation. At the time of publication, the editions indicated were valid. All Recommendations and other references are subject to revision; all users of this Recommendation are therefore encouraged to investigate the possibility of applying the most recent edition of the Recommendations and other references listed below. A list of the currently valid ITU-T Recommendations is regularly published.

[1] ITU-T Recommendation G.703 (1998), *Physical/electrical characteristics of hierarchical digital interfaces*.

[2] CCITT Recommendation G.743 (1988), *Second order digital multiplex equipment operating at 6312 kbit/s and using positive justification.*

[3] CCITT Recommendation G.752 (1988), *Characteristics of digital multiplex equipment based on a second order bit rate of 6312 kbit/s and using positive justification.*

[4] ITU-T Recommendation G.783 (1997), *Characteristics of synchronous digital hierarchy (SDH) equipment functional blocks.*

[5] CCITT Recommendation G.801 (1988), *Digital transmission models.*

[6] ITU-T Recommendation G.803 (2000), *Architecture of transport networks based on the Synchronous Digital Hierarchy (SDH).*

[7] ITU-T Recommendation G.810 (1996), *Definitions and terminology for synchronization networks.*

[8] ITU-T Recommendation G.811 (1997), *Timing characteristics of primary reference clocks.*

[9] ITU-T Recommendation G.812 (1998), *Timing requirements for slave clocks suitable for use as node clocks in synchronization networks.*

[10] ITU-T Recommendation G.813 (1996), *Timing characteristics of SDH equipment slave clocks (SEC).*

[11] CCITT Recommendation G.822 (1988), *Controlled slip rate objectives on an international digital connection.*

[12] ITU-T Recommendation G.823 (2000), *The control of jitter and wander within digital networks which are based on the 2048 kbit/s hierarchy.*

[13] ITU-T Recommendation G.825 (2000), *The control of jitter and wander within digital networks which are based on the synchronous digital hierarchy (SDH).*

[14] ITU-T Recommendation G.957 (1999), *Optical interfaces for equipments and systems relating to the synchronous digital hierarchy.*

[15] ITU-T Recommendation I.431 (1993), *Primary rate user-network interface – Layer 1 specification.*

[16] ITU-T Recommendation O.150 (1996), *General requirements for instrumentation for performance measurements on digital transmission equipment.*

[17] ITU-T Recommendation O.171 (1997), *Timing jitter and wander measuring equipment for digital systems which are based on the Plesiochronous Digital Hierarchy(PDH).*

[18] ITU-T Recommendation O.172 (1999), *Jitter and wander measuring equipment for digital systems which are based on the synchronous digital hierarchy (SDH).*

[19] ITU-T Recommendation Q.541 (1993), *Digital exchange design objectives – General.*

## 3 Definitions

This ITU-T Recommendation defines the following terms. Additional definitions relating to synchronization networks are provided in ITU-T Recommendation G.810.

**3.1 synchronous interface**: For the purpose of this ITU-T Recommendation, a synchronous interface is defined such that the bit rate of the interface is derived from a source that is ultimately traceable to a PRC.

**3.2 asynchronous interface**: These interfaces provide an output signal with frequency that is not traceable to a PRC and that meets the frequency offset requirements given in ITU-T Recommendation G.703.

**3.3 traffic interface**: These interfaces may be synchronous (i.e. normally PRC-traceable) or asynchronous (i.e. meeting the frequency offset requirements of ITU-T Recommendation G.703) and network limits are specified using the MRTIE (Maximum Relative Time Interval Error) parameter in this ITU-T Recommendation. Input jitter/wander tolerance is also specified in this ITU-T Recommendation. This interface category can be further sub-divided as follows:

a) Interface is not able or required to provide synchronization. An example is an interface supporting only 44 736 kbit/s PDH signals according to ITU-T Recommendation G.703.

b) Interface is not able to provide synchronization at the defined performance level, but nevertheless is used to provide timing to other network elements such as terminal equipment, remote concentrators, etc. Examples include 1544 and 44 736 kbit/s PDH signals

transported on SDH, which may be subject to pointer justifications. ITU-T Recommendation G.803 recommends that these interfaces not be used for synchronization.

c) Interface is able to provide synchronization at the defined performance level, in which case it is defined to be a synchronization interface.

**3.4 synchronization interface**: These interfaces are synchronous (i.e. normally PRC-traceable) and suitable for timing network clocks (SSUs and SECs). The network limits for synchronization interfaces are specified using MTIE (Maximum Time Interval Error) and TDEV (Time Deviation) parameters with values given in this ITU-T Recommendation. The input jitter/wander tolerance of clock equipment ports is specified in ITU-T Recommendation G.812 (for equipment containing an SSU function) and Option 2 of ITU-T Recommendation G.813 (for equipment containing an SEC function).

**3.5 phase transient**: Perturbations in phase of limited duration seen at synchronization and traffic interfaces, which may be due to clock switching or pointer justifications. The duration of phase transients caused by clock switching depends upon the clock involved. A G.813 clock may have a transient that has duration in the range of milliseconds to seconds, while a G.812 clock transient may take hours. The duration of phase transients due to pointer adjustments is presently undefined, but is expected to be on the order of seconds. Phase transients are specified by maximum phase deviation and by maximum temporary frequency offset.

## 4 Abbreviations

This ITU-T Recommendation uses the following abbreviations:

| | |
|---|---|
| AU-n | Administrative Unit, level n |
| FPM | Flicker Phase Modulation |
| ITU-T | International Telecommunications Union – Telecommunication Standardization Sector |
| MRTIE | Maximum Relative Time Interval Error |
| MTIE | Maximum Time Interval Error |
| NE | Network Element |
| NNI | Network Node Interface |
| PDH | Plesiochronous Digital Hierarchy |
| PRBS | Pseudo-Random Binary Sequence |
| PRC | Primary Reference Clock |
| SDH | Synchronous Digital Hierarchy |
| SEC | SDH Equipment Clock |
| SSU | Synchronization Supply Unit |
| STM-N | Synchronous Transport Module, level N |
| TDEV | Time Deviation |
| UI | Unit Interval |
| UIpp | Unit Interval – Peak-to-Peak |
| VC | Virtual Container |
| WFM | White Frequency Modulation |

## 5 Network limits for jitter and wander at traffic interfaces

### 5.1 Jitter limits

Specification of maximum permissible values of output jitter at hierarchical network interfaces is necessary to enable the interconnection of digital network components (line section, multiplex equipment, exchanges) to form a digital path or connection. These limits should be met regardless of the number of interconnected network components preceding the interface. The limits are intended to be compatible with the minimum jitter tolerance of all equipment operating at the same hierarchical level. Note that clock input ports may have different requirements as described in 7.2.1.

There is a close relationship between network limits and input tolerance such that the jitter measurement filter cut-off frequencies used in Table 1 have the same values as the jitter tolerance mask corner frequencies used in 7.2. The limits represent maximum permissible output jitter limits at hierarchical interfaces of a digital network. In circumstances where the maximum permissible jitter amplitude occurs at an interface between two countries, it is left to the discretion of National Administrations to take the appropriate remedial action. This situation is unlikely to occur very often.

For equipment which are not controlled by a network synchronizing system, but by an autonomous clock (e.g. quartz oscillator), more stringent output jitter values may be defined in the relevant equipment specifications. Examples are the muldex in ITU-T Recommendation G.734 and concerning the primary rate access in Recommendation I.431.

The arrangements for measuring output jitter at a digital interface are illustrated in ITU-T Recommendation O.172. The specific jitter limits and values of filter cut-off frequencies are given in Table 1. The high-pass measurement filters of Table 1 have a single-order characteristic and a roll-off of 20 dB/decade. The low-pass measurement filters have a maximally-flat, Butterworth characteristic and a roll-off of –20 dB/decade. Further specifications for the frequency response of the jitter measurement function such as measurement filter accuracy and additional allowed filter poles are given in ITU-T Recommendation O.172. In particular, jitter on PDH tributaries to SDH should be measured with test equipment that conforms with ITU-T Recommendation O.172 because of the unusual nature of jitter due to pointer justification.

The jitter and wander requirements for an interface will be different depending on whether the signal at the interface is used to transport traffic and/or synchronization. In cases where a traffic signal is used to carry synchronization, the wander limit in Figure 3 applies.

**Table 1/G.824 – Maximum permissible jitter at traffic interfaces**

| Digital rate (kbit/s) | Measurement filter bandwidth –3 dB frequencies (Hz) | Peak-to-Peak amplitude (UIpp) |
|---|---|---|
| 1544 | 10 to 40 k | 5.0 |
| | 8 to 40 k | 0.1 |
| 6312 | 10 to 60 k | 5.0 |
| | 3 to 60 k | 0.1 (Note 1) |
| 32 064 | 10 to 400 k | 5.0 |
| | 8 to 400 k | 0.1 (Note 1) |
| 44 736 | 10 to 400 k | 5.0 |
| | 30 to 400 k | 0.1 |
| 97 728 | 10 to 1000 k | 5.0 |
| | 240 to 1000 k | 0.1 |

**Table 1/G.824 – Maximum permissible jitter at traffic interfaces *(concluded)***

| |
|---|
| NOTE 1 – This value requires further study. |
| NOTE 2 – 1544 kbit/s 1 UI = 647 ns<br>6312 kbit/s 1 UI = 158 ns<br>32 064 kbit/s 1 UI = 31.1 ns<br>44 736 kbit/s 1 UI = 22.3 ns<br>97 728 kbit/s 1 UI = 10.2 ns. |

## 5.2 Wander limits

Network output wander specifications at synchronous network nodes are necessary to ensure satisfactory network performance (e.g. slips, error bursts). For network nodes the following limits are specified, based on the assumption of a non-ideal synchronizing signal (containing jitter, wander, frequency departure, and other impairments) on the line delivering timing information.

Besides conforming to wander limits given here, 1544 kbit/s and 44 736 kbit/s signals should conform to the frequency limits given in ITU-T Recommendation G.703.

Measurement methods for MTIE and MRTIE are discussed in Appendix II/G.823.

### 5.2.1 Synchronous 1544 kbit/s network interface

At the network interface, the wander of a 1544 kbit/s network signal shall not exceed an MTIE ($\tau$) of 28 UI (18 µs) for $\tau$ = 24 hours; nor shall it exceed an MTIE ($\tau$) of 13 UI (8.4 µs) for $\tau$ = 15 minutes (see Table 2).

**Table 2/G.824 – Synchronous network interface for 1544 kbit/s rate**

| Observation interval ($\tau$) in seconds | MTIE in µs |
|---|---|
| $\tau \leq 900$ | 8.4 |
| $900 < \tau \leq 86\,400$ | 18.0 |

### 5.2.2 Synchronous 44 736 kbit/s network interface

The wander of a 44 736 kbit/s network signal shall not exceed the MRTIE limits given in Table 3 and illustrated in Figure 1.

**Table 3/G.824 – Wander limit for 44 736 kbit/s network interface**

| Observation interval $\tau$ in seconds | MRTIE ($\tau$) in ns |
|---|---|
| $0.1 < \tau \leq 0.195$ | $7700\,\tau$ |
| $0.195 < \tau \leq 5200$ | $1400 + 230\,\tau^{0.5}$ |
| $5200 < \tau$ | 18 000 |

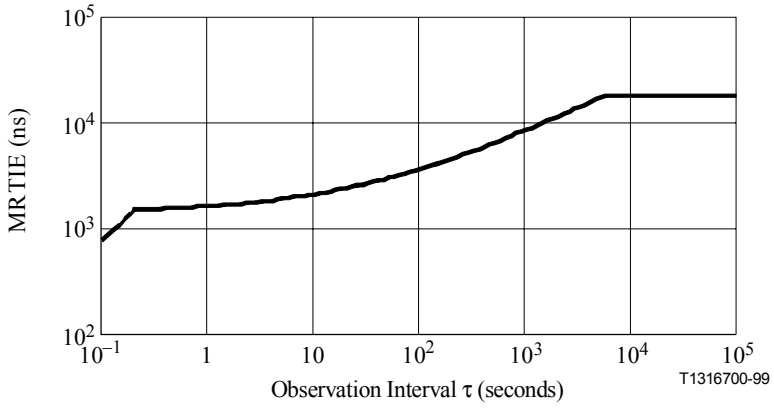



**Figure 1/G.824 – Wander limit for 44 736 kbit/s network interface**

### 5.3 Phase transients

At the network interface, during phase transients (typically due to network synchronization rearrangements), the phase deviation shall not exceed 1 μs, and the frequency of the signal shall not be offset from the nominal frequency by more than 61 ppm. Phase transients are expected to be a rare occurrence.

## 6 Network limits for jitter and wander at synchronization interfaces

The signals used for synchronization of digital networks based on the 1544 kbit/s hierarchy are 1544 kbit/s signals and STM-N signals. This clause gives limits for 1544 kbit/s signals used for synchronization; limits for STM-N signals used for transport of synchronization are given in ITU-T Recommendation G.825.

### 6.1 Network limits for jitter

Network limits for jitter on 1544 kbit/s signals used for synchronization are the same as those for jitter on 1544 kbit/s traffic signals (see 5.1).

### 6.2 Network limits for wander

#### 6.2.1 Primary Reference Clock (PRC) output

The network limit for wander that may be generated at the output interface of a PRC is given in Table 4. See also Figure 2.

**Table 4/G.824 – MTIE limit at the output of a PRC**

| Observation interval, τ (seconds) | MTIE (ns) |
|---|---|
| $0.05 < \tau \leq 1000$ | $10 + 0.29\ \tau$ |
| $1000 < \tau$ | $290 + 0.01\ \tau$ |
| NOTE – The region $\tau < 0.05$ seconds corresponds to phase variations with spectral components greater than 10 Hz. | |

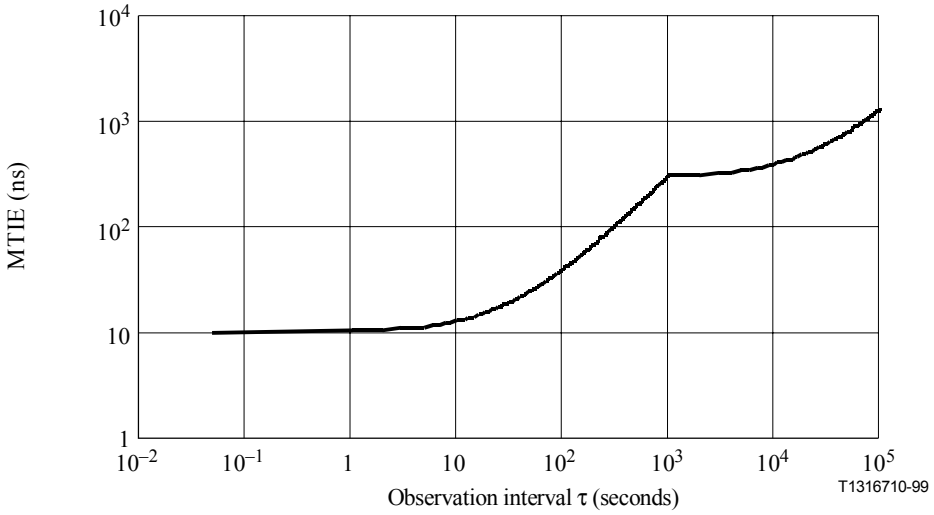



**Figure 2/G.824 – MTIE limit at the output of a Primary Reference Clock**

### 6.2.2 1544 kbit/s reference interface

The network limit for wander that may be generated at the output for a 1544 kbit/s interface is given in Table 5.

**Table 5/G.824 – MTIE limit for 1544 kbit/s reference signals**

| Observation interval, τ (seconds) | MTIE (ns) |
|---|---|
| $0.05 \leq \tau \leq 280$ | $300 + 2.5\ \tau$ |
| $280 < \tau$ | $997 + 0.01\ \tau$ |

The resulting overall specification is illustrated in Figure 3.

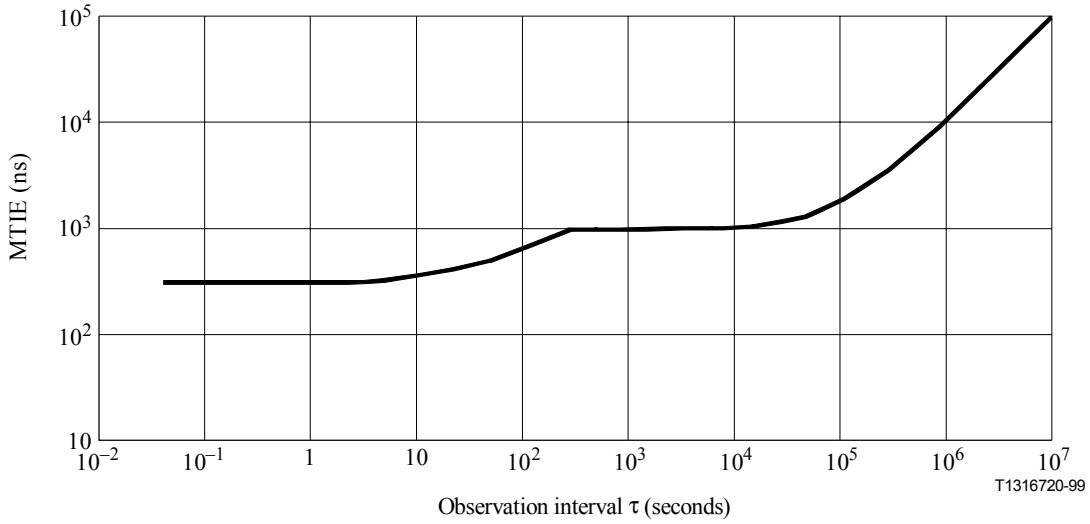



**Figure 3/G.824 – MTIE limit for 1544 kbit/s reference signals**

The TDEV for an observation interval of $\tau$ seconds shall not exceed the mask given in Table 6.

**Table 6/G.824 – TDEV limit for 1544 kbit/s reference signals**

| Observation interval, $\tau$ (seconds) | TDEV (ns) |
|---|---|
| $0.05 < \tau \leq 10$ | 100 |
| $10 < \tau \leq 1000$ | $31.623\ \tau^{0.5}$ |

The resulting overall specification is illustrated in Figure 4.

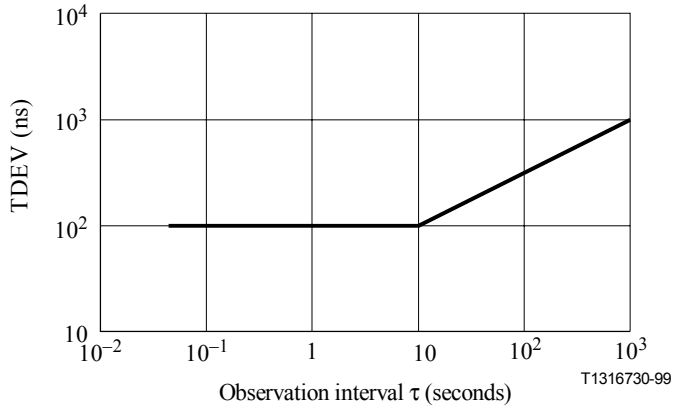



**Figure 4/G.824 – TDEV limit for 1544 kbit/s reference signals**

Simulation and analyses have shown (see Annex A) that in order to meet the slip rate performance in ITU-T Recommendation G.822, the short-term stability of the input reference to an Option-2 SEC must be more stable than that specified in Table 5. Therefore, the Time Deviation (TDEV) of the input 1544 kbit/s synchronization reference to a G.813 Option-2 clock, for Observation Interval $\tau$, shall not exceed the values in Table 7. The performance specified in Tables 5 and 6 have been derived from different sources; however, both specifications are required to be met.

**Table 7/G.824 – TDEV limit for 1544 kbit/s reference signals suitable for timing an Option-2 SEC**

| Observation interval, $\tau$ (seconds) | TDEV (ns) |
|---|---|
| $0.05 < \tau \leq 10$ | 10 |
| $10 < \tau \leq 1000$ | $3.1623\ \tau^{0.5}$ |

The resulting overall specification is illustrated in Figure 5.

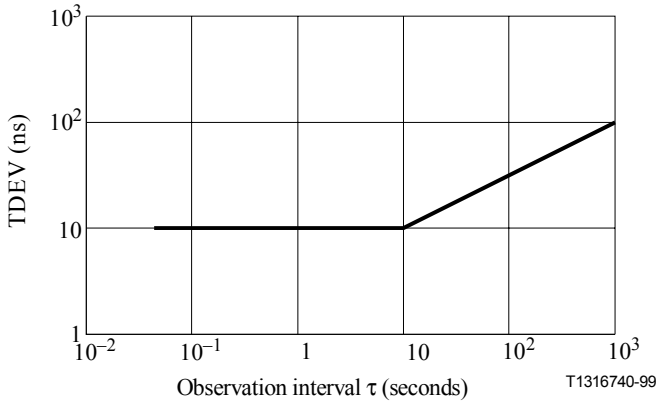



**Figure 5/G.824 – TDEV limit for 1544 kbit/s reference signals suitable for timing an Option-2 SEC**

## 7 Tolerance of jitter and wander at network interfaces

### 7.1 Basic specification philosophy

Jitter and wander control inherently depends on both network and equipment design. Network considerations are discussed in Clauses 5 and 6. The principal parameters of importance when considering the jitter and wander performance of digital equipment are:

a) the amount of jitter and wander that can be tolerated at the input;

b) the portion of this input jitter and wander which is transferred to the output; and

c) the amount of jitter and wander generated by the equipment.

The intention of this subclause is to provide a foundation for the development of equipment requirements, which will ensure that various network equipment is compatible from the standpoint of jitter and wander performance. The three performance parameters are listed here for technical completeness, since items b) and c) are equipment specifications.

### 7.2 Jitter and wander tolerance of traffic input ports

In order to ensure that equipment will operate satisfactorily when connected to a hierarchical interface within the network, it is necessary that the equipment input ports be capable of accommodating levels of network output jitter and wander up to the maximum network limits specified in 7.2.1 through 7.2.5. Specification of input jitter tolerance in terms of a single Recommendation applicable to all categories of digital equipment ensures that a certain minimum jitter tolerance is satisfied by all network elements. Most specifications of equipment input tolerance are in terms of the amplitude of sinusoidal jitter that can be applied at various frequencies without causing a designated degradation of error performance. The simplicity of this form of specification has great appeal, since it is easily verified with conventional test equipment. However, it is important to recognize that the test condition is not, in itself, intended to be representative of the type of jitter commonly found in a network. For some equipment, therefore, it may be necessary to specify supplemental jitter tolerance tests, and reference to the individual equipment Recommendation

should always be made.[1] As a minimum guideline for equipment tolerance, it is recommended that all digital input ports of equipment be able to tolerate the sinusoidal jitter and wander defined by the figures and tables in 7.2.1 through 7.2.5. The limits are to be met in an operating environment. Note that clock input ports may have different requirements as described in 7.3.

The wander/jitter is superimposed upon a timing signal which is ideally synchronous with a reference clock, and in practice reasonably stable. Instrumentation in accordance with ITU-T Recommendations O.171 and O.172 is appropriate for measurement of jitter in PDH and SDH systems, respectively.

NOTE – ITU-T Recommendation O.172 includes test set specifications for the measurement of SDH tributaries operating at PDH bit rates, where the test set requirements are more stringent than those relating only to PDH systems. Therefore, instrumentation in accordance with ITU-T Recommendation O.172 shall be used at PDH interfaces in SDH systems.

In deriving the specifications contained in Tables 8, 9, 10, 11 and 12 for frequencies above 6 kHz, 2.5 kHz, 8 kHz, 30 kHz and 240 kHz, respectively, the effects of the amount of alignment jitter of the equipment clock recovery are considered to be predominant.

Very low frequency wander accumulates in the network, and transmission equipment, such as digital line systems and asynchronous multiplexer/demultiplexer using justification techniques, are effectively transparent to these very low frequency changes in phase. However, such phase variation does need to be accommodated at the input of certain equipment (e.g. digital exchanges and synchronous muldexes).

When two or more inputs are terminated at a node and one of the two is used to synchronize the node, the node will need to tolerate up to 18 μs phase difference between two of the inputs.

Equipment wander tolerance must be compatible with network output wander limits specified in 5.2. Insufficient wander tolerance at synchronous equipment input ports might result in controlled or uncontrolled slips, depending on the specific slip control strategy employed.

### 7.2.1 1544 kbit/s input jitter and wander tolerance

As a minimum guideline for equipment tolerance, it is recommended that all 1544 kbit/s digital input ports of equipment be able to tolerate the sinusoidal jitter and wander defined by Figure 6 and Table 8. The limits are to be met in an operating environment. The test sequence to be used is a PRBS of length $2^{20} – 1$, defined in ITU-T Recommendation O.150.

[1] In the case of wander, a sinusoidal tolerance mask does not necessarily reflect all possible wander that might occur in a network because, in a real network, much of the wander is due to random phase noise and phase transients, rather than sinusoidal or periodic signals. However, it is expected that if the equipment (external to the network) connected at the traffic interface is designed with appropriate buffer storage and transfer characteristics such that it will meet its respective output requirements when wander at the level of the mask is input, then the equipment will accommodate wander generated in a large proportion of real connections.

**Table 8/G.824 – Jitter and wander tolerance of 1544 kbit/s input ports**

| Frequency $f$ (Hz) | Peak-to-Peak Amplitude (UI) |
|---|---|
| $1.2 \times 10^{-5} \leq f \leq 3.5 \times 10^{-4}$ | 28 (18 µs)<br>(Note 2) |
| $3.5 \times 10^{-4} < f \leq 5.6 \times 10^{-4}$ | $9.8 \times 10^{-3} f^{-1}$ ($6.35 \times 10^{-3} f^{-1}$ µs) |
| $5.6 \times 10^{-4} < f \leq 0.014$ | 17 (11 µs) |
| $0.014 < f \leq 0.016$ | $0.238 f^{-1}$ ($0.154 f^{-1}$ µs) |
| $0.016 < f \leq 0.16$ | 15 (10 µs) |
| $0.16 < f \leq 0.19$ | $2.4 f^{-1}$ ($1.6 f^{-1}$ µs) |
| $0.19 < f \leq 3.9$ | 13 (8.4 µs) |
| $3.9 < f \leq 10$ | $50.7 f^{-1}$ ($32.8 f^{-1}$ µs) |
| $10 < f \leq 120$ | 5 (3.2 µs) |
| $120 < f \leq 6000$ | $600 f^{-1}$ ($384 f^{-1}$ µs) |
| $6000 < f \leq 40\,000$ | 0.1 (0.0648 µs)<br>(Note 1) |
| NOTE 1 – This value requires further study.<br>NOTE 2 – The value 18 µs represents a relative phase deviation between the incoming signal and the internal local timing signal derived from the reference clock. An example of a reference configuration explaining the 18 µs value is given in Annex A. | |

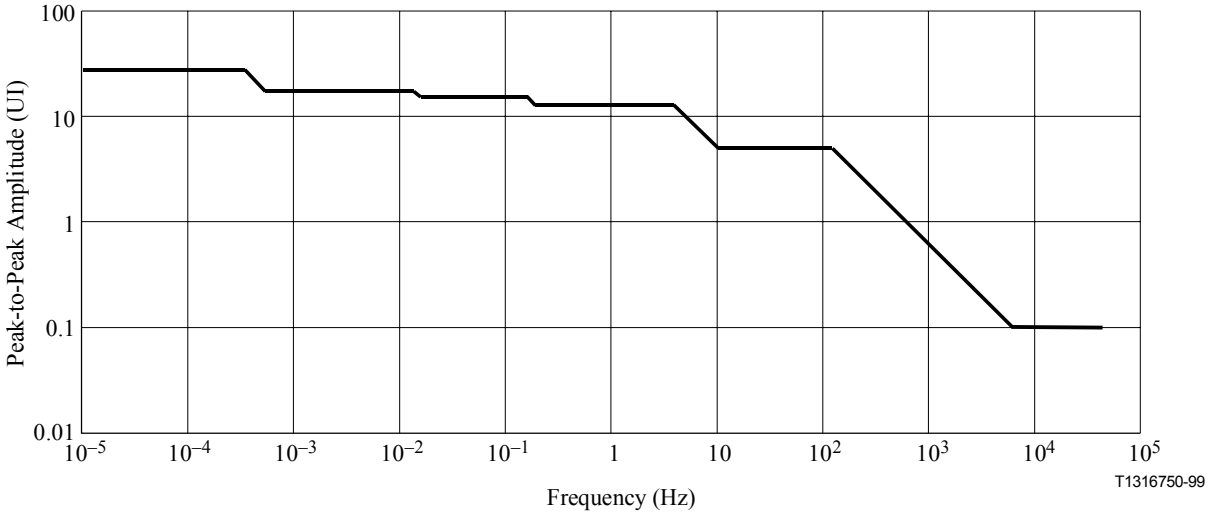



**Figure 6/G.824 – Jitter and wander tolerance of 1544 kbit/s input ports**

### 7.2.2 6312 kbit/s input jitter and wander tolerance

As a minimum guideline for equipment tolerance, it is recommended that all 6312 kbit/s digital input ports of equipment be able to tolerate the sinusoidal jitter and wander defined by Figure 7 and Table 9. The limits are to be met in an operating environment. The test sequence to be used is a PRBS of length $2^{20} - 1$ (note that this value requires further study), defined in ITU-T Recommendation O.150.

**Table 9/G.824 – Jitter and wander tolerance of 6312 kbit/s input ports**

| Frequency $f$ (Hz) | Peak-to-Peak amplitude (UI) |
|---|---|
| $1.2 \times 10^{-5} \leq f < 10$ | $8.479\, f^{-0.2293}$ ($1.343\, f^{-0.2293}$ μs) |
| $10 \leq f \leq 50$ | 5 (0.79 μs) |
| $50 < f \leq 2500$ | $250\, f^{-1}$ ($39.6\, f^{-1}$) |
| $2500 < f \leq 60\,000$ | 0.1 (0.016 μs) |
| NOTE – The value 18 μs at 12 μHz represents a relative phase deviation between the incoming signal and the internal local timing signal derived from the reference clock. An example of a reference configuration explaining the 18 μs value is given in Annex A. | |

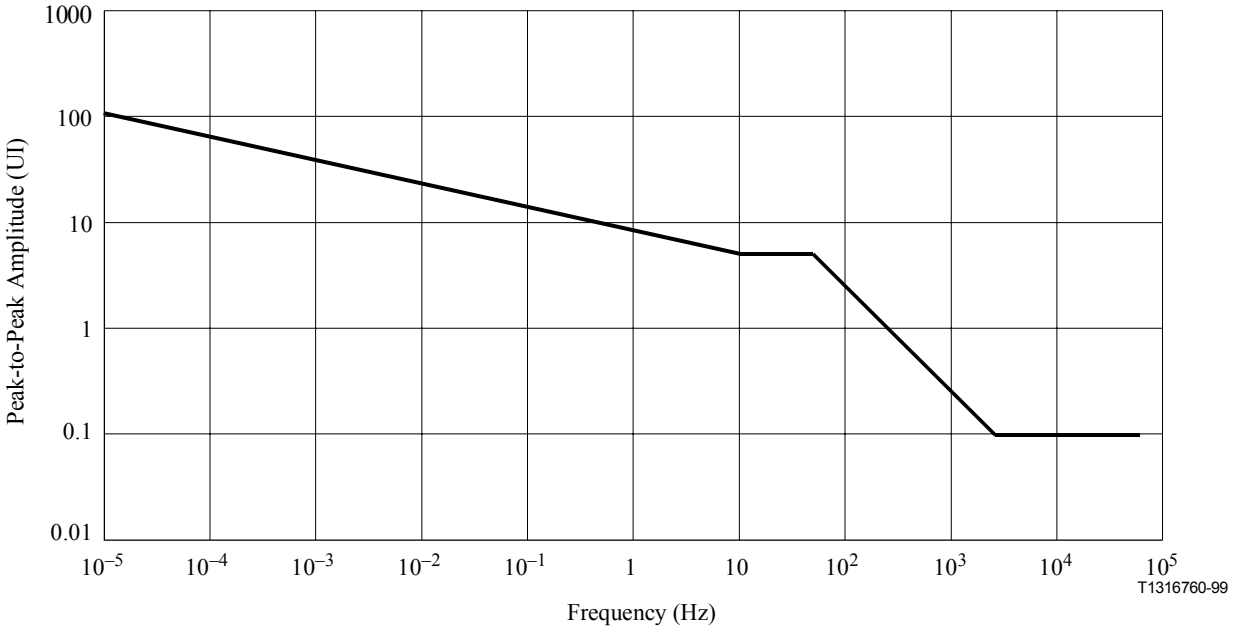



**Figure 7/G.824 – Jitter and wander tolerance of 6312 kbit/s input ports**

### 7.2.3 32 064 kbit/s input jitter and wander tolerance

As a minimum guideline for equipment tolerance, it is recommended that all 32 064 kbit/s digital input ports of equipment be able to tolerate the sinusoidal jitter and wander defined by Figure 8 and Table 10. The limits are to be met in an operating environment. The test sequence to be used is a PRBS of length $2^{20} – 1$, defined in ITU-T Recommendation O.150.

**Table 10/G.824 – Jitter and wander tolerance of 32 064 kbit/s input ports**

| Frequency $f$ (Hz) | Peak-to-Peak Amplitude (UI) |
|---|---|
| $1.2 \times 10^{-5} \leq f < 10$ | $5.206\, f^{-0.4155}$ ($0.1624\, f^{-0.4155}$ µs) |
| $10 \leq f \leq 400$ | 2 (0.0625 µs) |
| $400 < f \leq 8000$ | $800\, f^{-1}$ ($25\, f^{-1}$) |
| $8000 < f \leq 400\,000$ | 0.1 ($3.12 \times 10^{-3}$ µs) |
| NOTE – The value 18 µs at 12 µHz represents a relative phase deviation between the incoming signal and the internal local timing signal derived from the reference clock. An example of a reference configuration explaining the 18 µs value is given in Annex A. | |

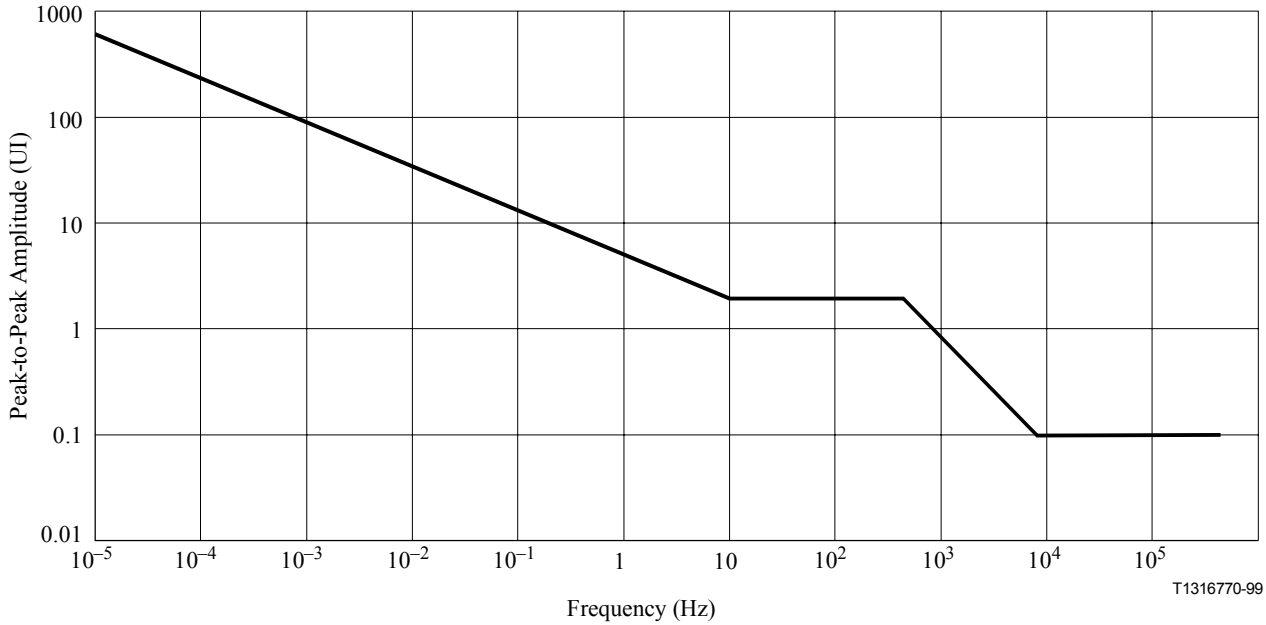



**Figure 8/G.824 – Jitter and wander tolerance of 32 064 kbit/s input ports**

### 7.2.4 44 736 kbit/s input jitter and wander tolerance

As a minimum guideline for equipment tolerance, it is recommended that all 44 736 kbit/s digital input ports of equipment be able to tolerate the sinusoidal jitter and wander defined by Figure 9 and Table 11. The limits are to be met in an operating environment. The test sequence to be used is a PRBS of length $2^{20} - 1$ (note that this value requires further study), defined in ITU-T Recommendation O.150.

**Table 11/G.824 – Jitter and wander tolerance of 44 736 kbit/s input ports**

| Frequency $f$ (Hz) | Peak-to-Peak Amplitude (UI) |
|---|---|
| $1.2 \times 10^{-5} \leq f \leq 6.12 \times 10^{-5}$ | 805 (18 µs)<br>(Note) |
| $6.12 \times 10^{-5} < f \leq 1.675$ | $62.6 + 5.81 f^{-1/2}$ ($1.4 + 0.130 f^{-1/2}$ µs) |
| $1.675 < f \leq 21.9$ | $110 f^{-1}$ ($2.45 f^{-1}$ µs) |
| $21.9 < f \leq 600$ | 5 (0.112 µs) |
| $600 < f \leq 30\,000$ | $3000 f^{-1}$ ($67.1 f^{-1}$ µs) |
| $30\,000 < f \leq 400\,000$ | 0.1 ($2.24 \times 10^{-3}$ µs) |
| NOTE – The value 18 µs represents a relative phase deviation between the incoming signal and the internal local timing signal derived from the reference clock. An example of a reference configuration explaining the 18 µs value is given in Annex A. | |

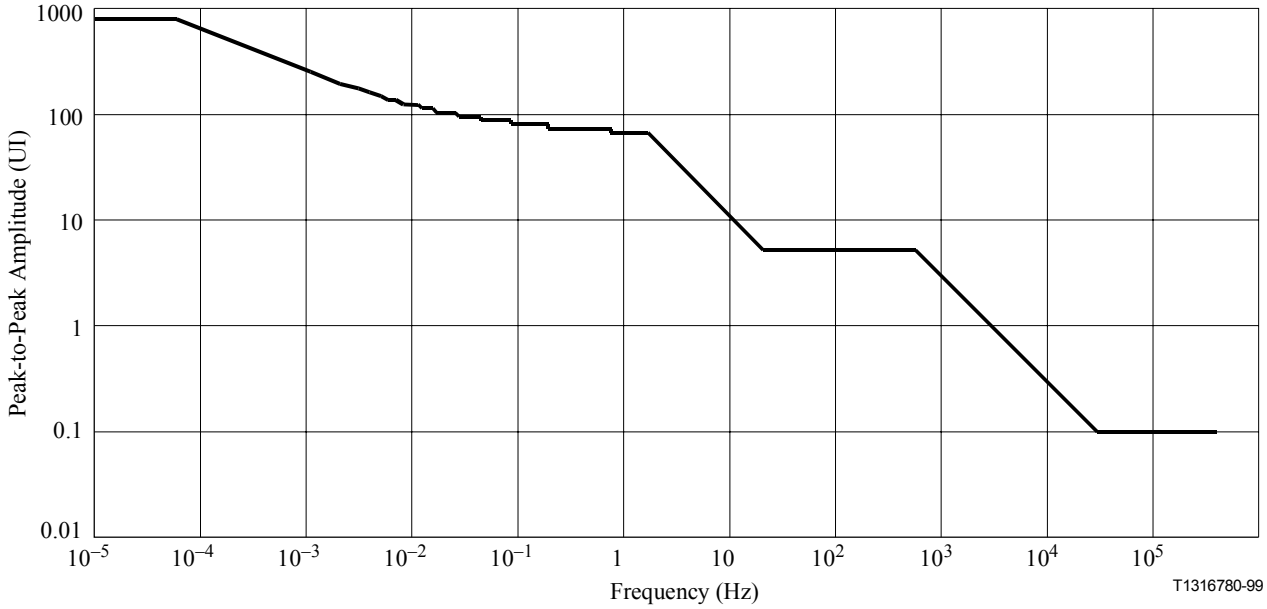



**Figure 9/G.824 – Jitter and wander tolerance of 44 736 kbit/s input ports**

### 7.2.5 97 728 kbit/s input jitter and wander tolerance

As a minimum guideline for equipment tolerance, it is recommended that all 97 728 kbit/s digital input ports of equipment be able to tolerate the sinusoidal jitter and wander defined by Figure 10 and Table 12. The limits are to be met in an operating environment. The test sequence to be used is a PRBS of length $2^{23} - 1$ (note that this value requires further study), defined in ITU-T Recommendation O.150.

**Table 12/G.824 – Jitter and wander tolerance of 97 728 kbit/s input ports**

| Frequency $f$ (Hz) | Peak-to-Peak Amplitude (UI) |
|---|---|
| $1.2 \times 10^{-5} \leq f < 10$ | $6.285\, f^{-0.4973}$ ($0.0643\, f^{-0.4973}$ µs) |
| $10 \leq f \leq 12\,000$ | 2 (0.0205 µs) |
| $12\,000 < f \leq 240\,000$ | $24\,000\, f^{-1}$ ($246\, f^{-1}$) |
| $240\,000 < f \leq 1\,000\,000$ | 0.1 ($1.02 \times 10^{-3}$ µs) |
| NOTE – The value 18 µs at 12 µHz represents a relative phase deviation between the incoming signal and the internal local timing signal derived from the reference clock. An example of a reference configuration explaining the 18 µs value is given in Annex A. | |

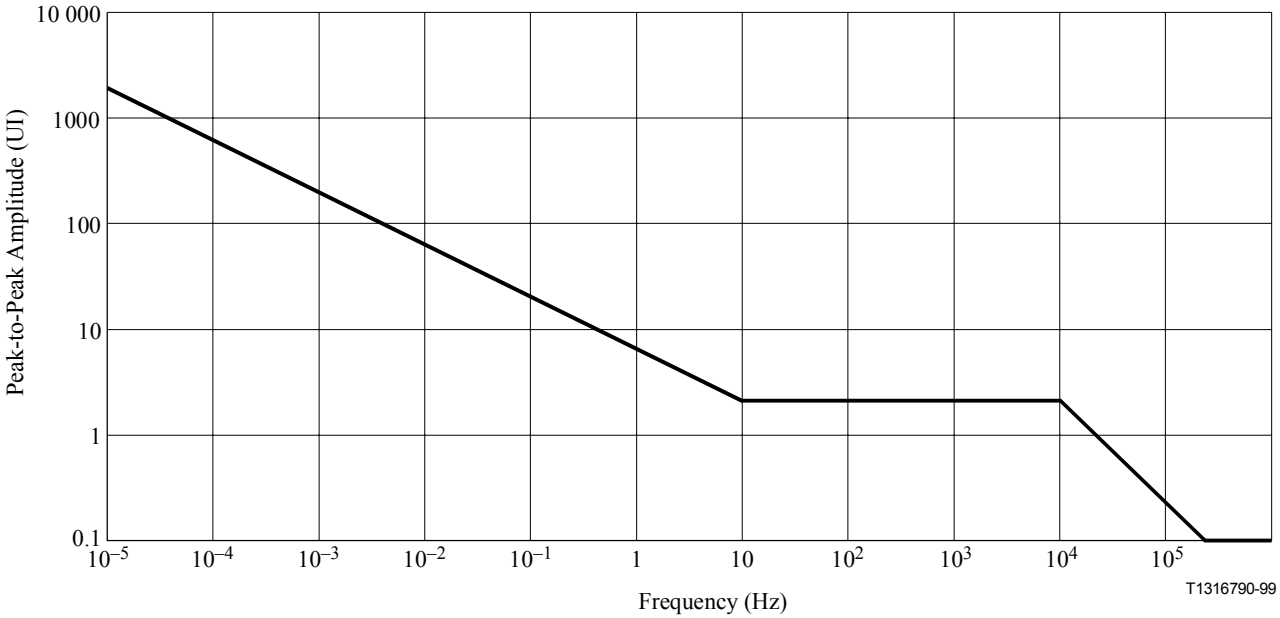



**Figure 10/G.824 – Jitter and wander tolerance of 97 728 kbit/s input ports**

## 7.3 Jitter and wander tolerance of clock input ports

The jitter and wander tolerance of clock input ports depends upon the type of equipment. Specifications for noise tolerance of slave clocks suitable for use as node clocks in synchronization networks are defined in ITU-T Recommendation G.812 Types II and III and specifications for noise tolerance of SDH equipment clocks are defined in ITU-T Recommendation G.813 for Option 2.

ANNEX A

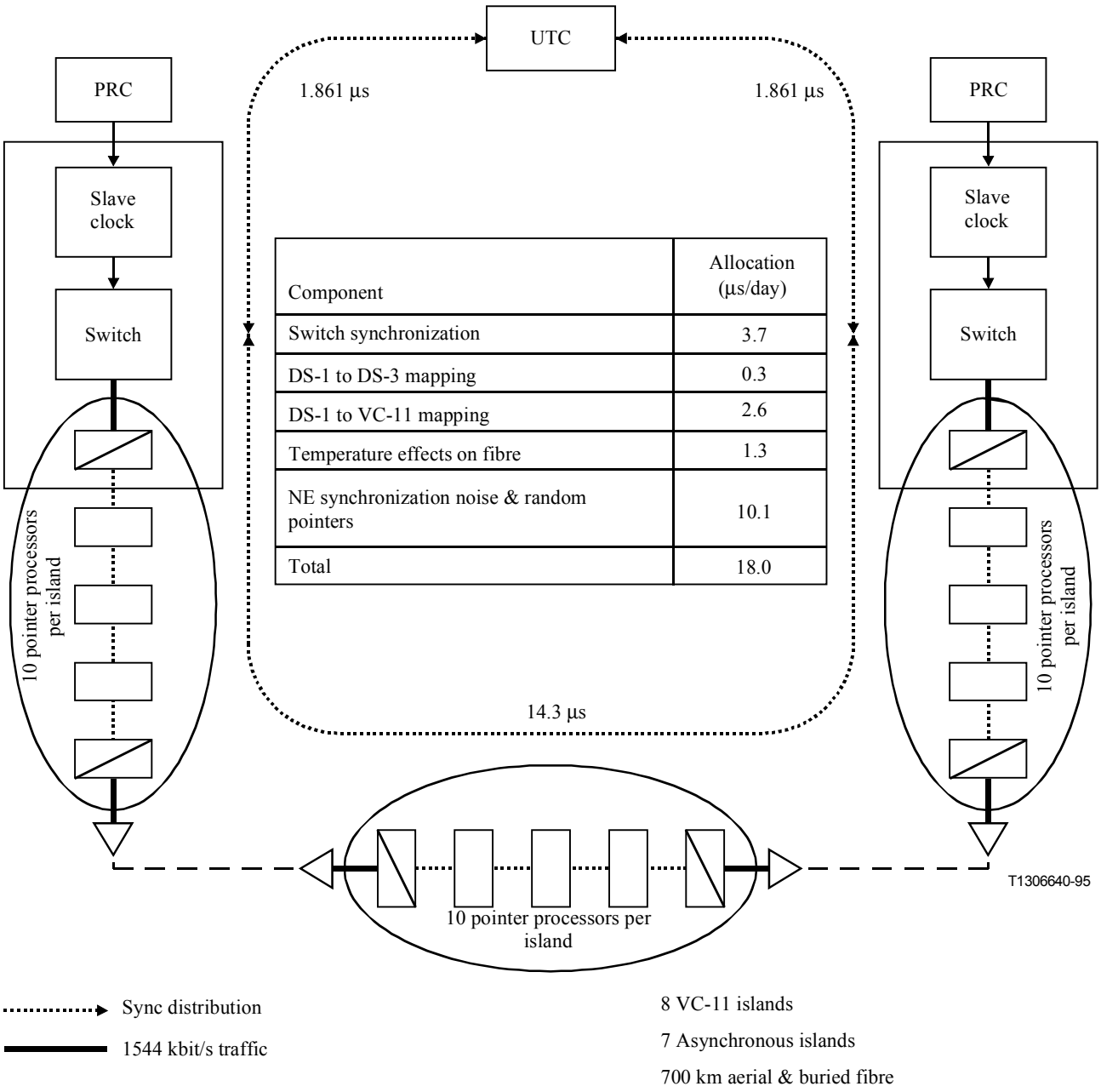
## Wander reference models and wander budgets

### A.1 1544 kbit/s wander accumulation

The network limit TDEV mask for input to an SDH option-2 SEC is given in Table 5. The purpose of the mask is to ensure acceptable wander accumulation and slip performance for 1544 kbit/s payloads transported through a network that includes SDH VC 11 islands, and ultimately terminating in controlled slip buffers that have hysteresis as small as 18 μs. A VC-11 island is an SDH network with asynchronous interfaces; a VC-11 island reference connection for wander is shown in Figure A.1. Jitter and wander are generated by each VC-11 island, as well as other parts of the network. A wander budget based on extensive simulation studies[2] was developed for the 1544 kbit/s signals transported over these islands, and is also shown in Figure A.1. This wander budget allocates 10.1 μs of wander per day to SDH NE synchronization noise and random pointer adjustments. This budget was developed using ITU-T Recommendation G.822 as a guideline. ITU-T Recommendation G.822 specifies in a national and local network that there should be less than an average of 2.3 slips in 24 hours (46% of 5 slips in 24 hours) at least 98.9% of the time.

The assumptions of the model for the 1544 kbit/s wander and slip simulations are described below in A.1.1. The simulations showed that, for a network of 8 VC-11 islands with each SDH NE synchronized by a signal that meets the TDEV mask of Figure 5, there will be 1 or fewer 1544 kbit/s slips per day 94.6% of the time and 2 or fewer 1544 kbit/s slips per day 99.0% of the time. The model does not accommodate all networks of large numbers of VC-11 islands. ITU-T Recommendation G.801 states that the hypothetical reference connection "...does not represent the rare worst case connection; although it does aim to encompass the vast majority of connections".

[2] Extensive simulation studies were also performed for both 1544 kbit/s and 44 736 kbit/s jitter accumulation, using appropriate VC-11 and AU-3 island reference models. The results showed that the SDH NE synchronization requirements for acceptable 1544 kbit/s wander accumulation are tighter than for acceptable 1544 kbit/s or 44 736 kbit/s jitter accumulation (see Figure 5 and Figure 8/G.813 respectively).




| Component | Allocation (µs/day) |
|---|---|
| Switch synchronization | 3.7 |
| DS-1 to DS-3 mapping | 0.3 |
| DS-1 to VC-11 mapping | 2.6 |
| Temperature effects on fibre | 1.3 |
| NE synchronization noise & random pointers | 10.1 |
| Total | 18.0 |

**Figure A.1/G.824 – SDH VC-11 island wander reference model and wander budget**

### A.1.1 1544 kbit/s wander accumulation and slip simulation model assumptions

In the simulation model, each node of each SDH island was synchronized by a clock phase noise model that contained a Flicker Phase Modulation (FPM) component and White Frequency Modulation (WFM) component. The WFM noise component was produced by generating a Gaussian white noise random sequence with zero mean and standard deviation equal to the specified amplitude, and then integrating this process. The FPM noise component was produced by generating a Gaussian white noise random sequence with zero mean and standard deviation equal to the specified amplitude, and then passing this sequence through a set of filters as described and

implemented by Barnes and Greenhall[3]. The FPM and WFM amplitudes were chosen such that TDEV for the resulting phase noise just met the mask of Figure 5. This resulting phase noise was filtered by a single-pole, 0.1 Hz low-pass filter, which represented the SDH NE clock. VC-11 pointer processors were assumed to have a 2-byte threshold spacing, and AU-3 pointer processors were assumed to have a 4-byte threshold spacing. The desynchronizers in each island were not modelled, as these do not affect long-term phase variation and 1544 kbit/s slip performance. The simulation results described at the end of the above subclause were for a network of 8 VC-11 islands with 10 pointer processor nodes per island. For each simulation case (i.e. for the 8 VC-11 island case described above and for various other cases), a number of independent replications were run to obtain statistically significant results.

1544 kbit/s slip performance was obtained using an approximate slip buffer model. In this model, the slip buffer size is equal to the sum of the frame size and the hysteresis. The buffer fill at any given time is equal to the sum of the initial buffer fill, the 1544 kbit/s phase input, and the total phase due to all slips up to that time. For each of the independent replications of the 1544 kbit/s phase accumulation simulation, the slip buffer simulation was run a number of times, with a different slip buffer initial condition for each run. The initial buffer fills were chosen to be uniformly-spaced.[4] For each of these runs, the number of slips was recorded; a statistical analysis was performed on the results of all the runs to obtain estimates of the probabilities of obtaining various numbers of slips in one day.

The input to the slip buffer model should be the total 1544 kbit/s phase, due to all the components of the wander budget in Figure A.1. However, it was not practical to run multiple, independent replications of 1-day simulations of 1544 kbit/s-to-44 736 kbit/s mapping and of 1544 kbit/s-to-VC-11 mapping (the computational requirements for this would have been prohibitive). In addition, a model for the component due to temperature effects on the fiber was not available. Therefore, these components were not simulated; they were accounted for by reducing the slip buffer hysteresis by their budgeted amounts in Figure A.1. The slip buffer hysteresis used in the simulations was therefore 13.8 μs. The component of 1544 kbit/s wander due to switch synchronization was simulated using a random phase noise model similar to the one above for SDH NE synchronization noise. The main difference between the two models is that the noise levels for switch synchronization are somewhat higher.

## A.2 44 736 kbit/s wander accumulation

The network limit for 44 736 kbit/s traffic interfaces is given by the MRTIE mask of Figure 1. This subclause describes the wander reference model and wander budget that were used to develop this network limit.

In developing wander specifications, it is necessary to consider the total transport network – synchronous and asynchronous, as well as the 44 736 kbit/s signal source synchronization. For transport of a 44 736 kbit/s signal over SDH AU-3 islands, one must consider all causes of wander on the signal. Further, one must consider the effects of interconnecting independent SDH islands. Figure A.2 shows the AU-3 wander reference model that was developed for 44 736 kbit/s wander allocation and budgeting. Simulations have shown that wander accumulation over cascaded AU-3 islands tends to dominate the wander generated in any particular island.

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[3] See Annex A of BARNES (James A.), GREENHALL (Charles A.): Large Sample Simulation of Flicker Noise, *19th Annual Precise Time and Time Interval (PTTI) Applications Planning Meeting*, December, 1987.

[4] For most cases, the number of independent wander accumulation simulation replications was 300 and, for each replication, the number of slip buffer simulations was 51.

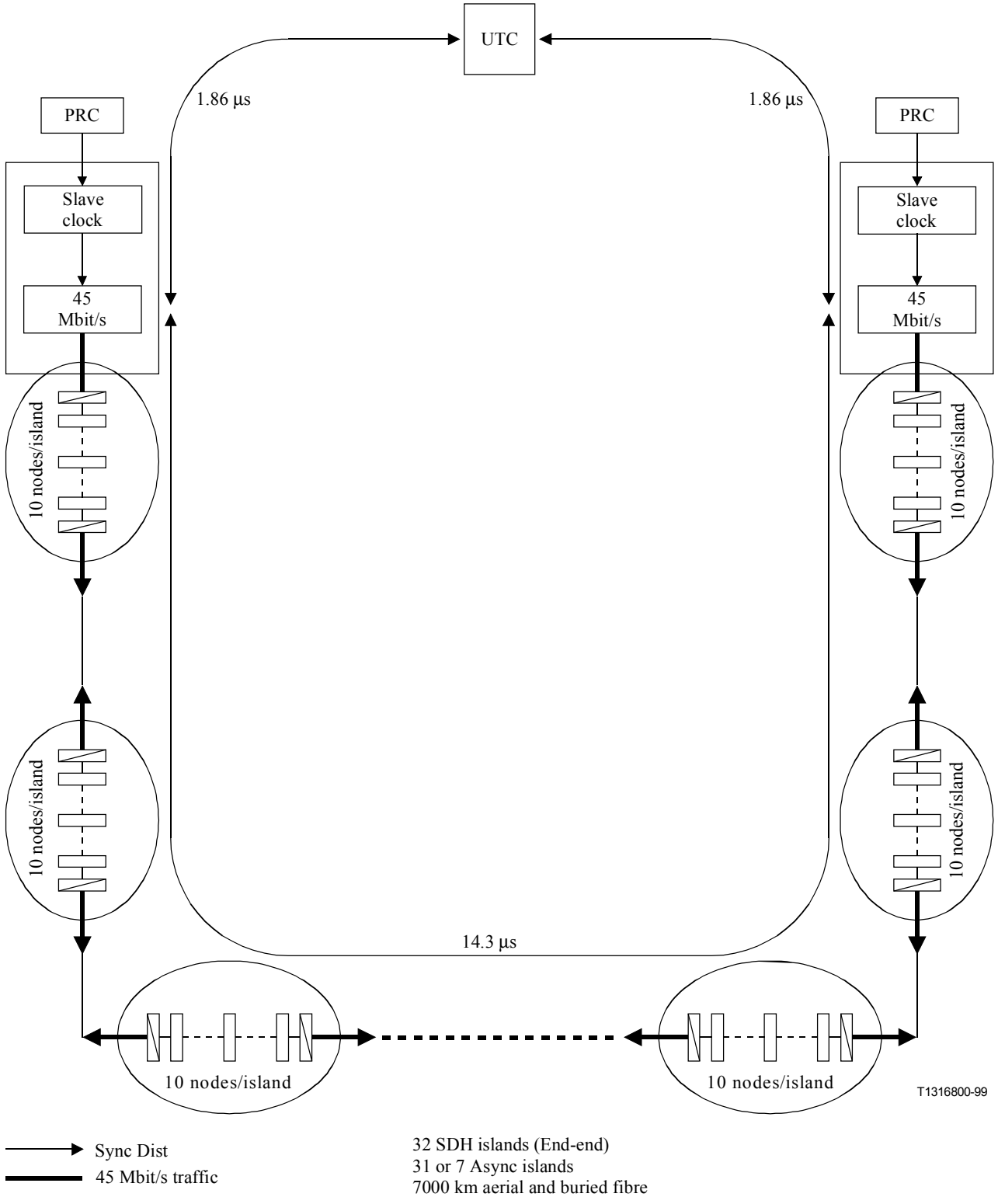


**Figure A.2/G.824 – SDH AU-3 island wander reference model**

The wander budget for transport of 44 736 kbit/s signals over AU-3 islands is given in Table A.1.

**Table A.1/G.824 – Wander budget for transport of 44 736 kbit/s signals over AU-3 islands**

| Component | Allocation (μs/day) |
|---|---|
| DS-1 Switch Synchronization | 3.72 |
| 44 736 kbit/s to AU-3 mapping | 0.72 |
| Asynchronous network | 0.70 |
| Temperature effects on fibre | 1.30 |
| Periodic pointer adjustments due to synchronization failure | 0.80 |
| Transients in synchronization distribution | 1.00 |
| NE synchronization noise and random pointer adjustments | 9.76 |
| TOTAL | 18.0 |

The wander budget allocates 9.76 μs/day (peak-to-peak) to SDH NE synchronization noise and random pointer adjustments. This allocation cannot be achieved by SDH networks whose synchronization interfaces meet the TDEV requirement of Figure 4, nor by SDH networks whose synchronization interfaces meet the TDEV requirement of Figure 5. However, simulations have shown that the slip performance of 1544 kbit/s signals carried by the 44 736 kbit/s signal will be acceptable in SDH networks whose synchronization interfaces meet the TDEV requirement of Figure 5.

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