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SERIES G: TRANSMISSION SYSTEMS AND MEDIA, DIGITAL SYSTEMS AND NETWORKS

Digital networks – Quality and availability targets

The control of jitter and wander within digital networks which are based on the 2048 kbit/s hierarchy

ITU-T Recommendation G.823

(Formerly CCITT Recommendation)

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ITU-T Recommendation G.823

The control of jitter and wander within digital networks which are based on the 2048 kbit/s hierarchy

Summary

This ITU-T Recommendation specifies the maximum network limits of jitter and wander that shall not be exceeded and the minimum equipment tolerance to jitter and wander that shall be provided at any relevant transport or synchronization interfaces which are based on the 2048 kbit/s hierarchy.

The requirements for the jitter and wander characteristics that are specified in this ITU-T Recommendation must be adhered to in order to ensure interoperability of equipment produced by different manufacturers and a satisfactory network performance.

Source

ITU-T Recommendation G.823 was revised by ITU-T Study Group 13 (1997-2000) and approved under the WTSC Resolution 1 procedure on 10 March 2000.

Keywords

Clocks, Input Jitter Tolerance, Input Wander Tolerance, Network Limits, Output Jitter, Output Wander, Synchronization, Timing.

FOREWORD

The International Telecommunication Union (ITU) is the United Nations specialized agency in the field of telecommunications. The ITU Telecommunication Standardization Sector (ITU-T) is a permanent organ of ITU. ITU-T is responsible for studying technical, operating and tariff questions and issuing Recommendations on them with a view to standardizing telecommunications on a worldwide basis.

The World Telecommunication Standardization Conference (WTSC), which meets every four years, establishes the topics for study by the ITU-T study groups which, in turn, produce Recommendations on these topics.

The approval of ITU-T Recommendations is covered by the procedure laid down in WTSC Resolution 1.

In some areas of information technology which fall within ITU-T's purview, the necessary standards are prepared on a collaborative basis with ISO and IEC.

NOTE

In this Recommendation, the expression "Administration" is used for conciseness to indicate both a telecommunication administration and a recognized operating agency.

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As of the date of approval of this Recommendation, ITU had not received notice of intellectual property, protected by patents, which may be required to implement this Recommendation. However, implementors are cautioned that this may not represent the latest information and are therefore strongly urged to consult the TSB patent database.

CONTENTS

Introduction and background

In a digital network, jitter and wander accumulate on transmission paths according to the jitter and wander generation and transfer characteristics of each equipment interconnected. This equipment may be different types of multiplexers/demultiplexers, cross-connects, clocks and line systems, for example.

An excessive amount of jitter and wander can adversely affect both digital (e.g. by generation of bit errors, slips and other abnormalities) and analogue signals (e.g. by unwanted phase modulation of the transmitted signal). The consequences of such impairment will, in general, depend on the particular service that is being carried and the terminating or adaptation equipment involved.

It is therefore necessary to set limits on the maximum magnitude of jitter and wander, and the corresponding minimum jitter and wander tolerance at network interfaces, in order to guarantee a proper quality of the transmitted signals and a proper design of the equipment. These network limits are independent of the particular service that is being carried.

ITU-T Recommendation G.823

The control of jitter and wander within digital networks which are based on the 2048 kbit/s hierarchy

1 Scope

This ITU-T Recommendation specifies the relevant parameters and their limiting values that are able to satisfactorily control the amount of jitter and wander present at Network Node Interfaces (NNI) of Plesiochronous Digital Hierarchy (PDH) and synchronization networks which are based on the first-level hierarchical bit rate of 2048 kbit/s.

This ITU-T Recommendation also specifies the jitter and wander requirements at PDH User-Network Interfaces (UNI). However, particular terminals or services may have additional jitter and wander requirements and in those cases the relevant ITU-T Recommendations shall apply.

Requirements for NNI of PDH and synchronization networks which are based on the first-level hierarchical bit rate of 1544 kbit/s are specified in ITU-T Recommendation G.824 and requirements for Synchronous Digital Hierarchy (SDH) NNI are specified in ITU-T Recommendation G.825.

The jitter and wander requirements specified in this ITU-T Recommendation are applicable to the interfaces irrespective of the underlying transport mechanism (PDH, SDH or ATM networks, for example).

The jitter and wander requirements for an interface will be different, depending on whether the signal at the interface is used to transport traffic and/or synchronization. The requirements for both traffic and synchronization interfaces are specified in this ITU-T Recommendation in the appropriate clauses.

A synchronization network that conforms to the network limits for jitter and wander specified in this ITU-T Recommendation will be suitable for the synchronization of SDH and Public Switched Telephone Network (PSTN) networks.

This ITU-T Recommendation also specifies the jitter and wander requirements for interfaces using the generic frame structures at PDH rates as defined in ITU-T Recommendation G.832.

The electrical characteristics of the relevant PDH network interfaces are defined in ITU-T Recommendation G.703.

The jitter and wander control philosophy of this ITU-T Recommendation is based on the need:

a) to specify a maximum network limit of jitter and wander that shall not be exceeded at any relevant interface;

b) to specify a minimum equipment tolerance to jitter and wander that shall be provided at any relevant interface;

c) to establish a consistent framework for the specification of individual digital equipment types; and

d) to provide sufficient information and guidelines for organizations to measure and study jitter and wander characteristics in any network configuration.

2 References

The following ITU-T Recommendations and other references contain provisions which, through reference in this text, constitute provisions of this Recommendation. At the time of publication, the editions indicated were valid. All Recommendations and other references are subject to revision; all users of this Recommendation are therefore encouraged to investigate the possibility of applying the most recent edition of the Recommendations and other references listed below. A list of the currently valid ITU-T Recommendations is regularly published.

– ITU-T Recommendation G.703 (1998), *Physical/electrical characteristics of hierarchical digital interfaces.*

– ITU-T Recommendation G.707 (1996), *Network node interface for the Synchronous Digital Hierarchy (SDH).*

– ITU-T Recommendation G.783 (1997), *Characteristics of Synchronous Digital Hierarchy (SDH) equipment functional blocks.*

– ITU-T Recommendation G.803 (2000), *Architecture of transport networks based on the Synchronous Digital Hierarchy (SDH).*

– ITU-T Recommendation G.810 (1996), *Definitions and terminology for synchronization networks.*

– ITU-T Recommendation G.811 (1997), *Timing characteristics of primary reference clocks.*

– ITU-T Recommendation G.812 (1998), *Timing requirements of slave clocks suitable for use as node clocks in synchronization networks.*

– ITU-T Recommendation G.813 (1996), *Timing characteristics of SDH equipment slave clocks (SEC).*

– CCITT Recommendation G.822 (1988), *Controlled slip rate objectives on an international digital connection.*

– ITU-T Recommendation G.824 (2000), *The control of jitter and wander within digital networks which are based on the 1544 kbit/s hierarchy.*

– ITU-T Recommendation G.825 (2000), *The control of jitter and wander within digital networks which are based on the Synchronous Digital Hierarchy (SDH).*

– ITU-T Recommendation G.832 (1998), *Transport of SDH elements on PDH networks – Frame and multiplexing structures.*

– ITU-T Recommendation O.150 (1996), *General requirements for instrumentation for performance measurements on digital transmission equipment.*

– ITU-T Recommendation O.171 (1997), *Timing jitter and wander measuring equipment for digital systems which are based on the Plesiochronous Digital Hierarchy (PDH).*

– ITU-T Recommendation O.172 (1999), *Jitter and wander measuring equipment for digital systems which are based on the Synchronous Digital Hierarchy (SDH).*

3 Definitions

This ITU-T Recommendation defines the following terms. Additional definitions relating to synchronization networks are provided in ITU-T Recommendation G.810, whilst the architectural principles of synchronization networks are described in ITU-T Recommendation G.803.

Information regarding the wander reference models used in this ITU-T Recommendation is provided in Annexes A and B.

3.1 synchronous interface: These interfaces provide an output signal with frequency that is normally traceable to a PRC.

3.2 asynchronous interface: These interfaces provide an output signal with frequency that is not traceable to a PRC and that meets the frequency offset requirements given in ITU-T Recommendation G.703.

3.3 traffic interface: These interfaces may be asynchronous or synchronous and network jitter and wander limits are specified using the Maximum Relative Time Interval Error (MRTIE) parameter in this ITU-T Recommendation. Input jitter and wander tolerance is also specified in this ITU-T Recommendation. This interface category can be further sub-divided as follows:

a) Interface is not able to provide synchronization, and is not required to. An example is an interface supporting only 34 368 or 139 264 kbit/s PDH signals according to ITU-T Recommendation G.703.

b) Interface is not able to provide synchronization at the defined performance level, but nevertheless is used to provide timing to other network elements such as terminal equipment, remote concentrators, etc. Examples include 2048, 34 368 and 139 264 kbit/s PDH signals transported on SDH, which may be subject to pointer justifications. ITU-T Recommendation G.803 recommends that these interfaces are not to be used for synchronization.

c) Interface is able to provide synchronization at the defined performance level, in which case it is defined to be a synchronization interface. An example is a synchronization interface operating at 2048 kbit/s. This sub-category may also include interfaces using the generic frame structures at PDH rates as defined in ITU-T Recommendation G.832.

3.4 synchronization interface: These interfaces are synchronous and network wander limits are specified using Maximum Time Interval Error (MTIE) and Time Deviation (TDEV) parameters with values given in this ITU-T Recommendation. The input jitter and wander tolerance of clock equipment ports is specified in other Recommendations (refer to 7.2).

4 Abbreviations

This ITU-T Recommendation uses the following abbreviations. Additional abbreviations relating to synchronization networks are provided in ITU-T Recommendation G.810.

ATM	Asynchronous Transfer Mode
AU-n	Administrative Unit, level n
CLK	Clock
CMI	Coded Mark Inversion
ITU-T	International Telecommunication Union – Telecommunication Standardization Sector
LPF	Low-Pass Filter
MRTIE	Maximum Relative Time Interval Error
MS-AIS	Multiplex Section Alarm Indication Signal
MTIE	Maximum Time Interval Error
NE	Network Element
NNI	Network Node Interface
PDH	Plesiochronous Digital Hierarchy
pk-pk	peak-to-peak

PLL	Phase Locked Loop
ppm	parts per million
PRBS	Pseudo-Random Binary Sequence
PRC	Primary Reference Clock
PSTN	Public Switched Telephone Network
RMS	Root Mean Square
RTIE	Relative Time Interval Error
SDH	Synchronous Digital Hierarchy
SEC	SDH Equipment Clock
SSU	Synchronization Supply Unit
STM-N	Synchronous Transport Module, level N
TDEV	Time Deviation
TIE	Time Interval Error
TU-m	Tributary Unit, level m
UI	Unit Interval
UIpp	Unit Interval, peak-to-peak
UNI	User-Network Interface
UTC	Universal Time Coordinated
VC-n	Virtual Container, level n

5 Network limits for traffic interfaces

5.1 Network limits for output jitter at traffic interfaces

The limits given in this clause represent the maximum permissible levels of jitter at interfaces within a digital network. Jitter as measured over a 60 second interval shall not exceed the limits specified in Table 1, when using the specified measurement filters.

There is a close relationship between network limits and input tolerance such that the jitter measurement filter cut-off frequencies used in this clause have the same values as the jitter tolerance mask corner frequencies used in 7.1. Appendix I/G.825 has further information regarding this relationship.

The limits given in Table 1 shall be met for all operating conditions and regardless of the amount of equipment preceding the interface. In general, these network limits are compatible with the minimum tolerance to jitter that all equipment input ports are required to provide.

The functional description for measuring output jitter at a digital interface is provided in ITU-T Recommendation O.172.

The high-pass measurement filters of Table 1 have a first-order characteristic and a roll-off of 20 dB/decade. The low-pass measurement filters have a maximally-flat, Butterworth characteristic and a roll-off of –60 dB/decade. Further specifications for the frequency response of the jitter measurement function such as measurement filter accuracy and additional allowed filter poles are given in ITU-T Recommendation O.172.

Instrumentation in accordance with ITU-T Recommendations O.172 and O.171 is appropriate for measurement of jitter in SDH and PDH systems, respectively.

NOTE – ITU-T Recommendation O.172 includes test set specifications for the measurement of SDH tributaries operating at PDH bit rates, where the test set requirements are more stringent than those relating only to PDH systems. Therefore, instrumentation in accordance with ITU-T Recommendation O.172 shall be used at PDH interfaces in SDH systems.

Table 1/G.823 – Maximum permissible jitter at traffic interfaces

Interface	Measurement bandwidth, –3 dB frequencies (Hz)	Peak-to-peak amplitude (UIpp) (Note 3)
64 kbit/s (Note 1)	20 to 20 k	0.25
	3 k to 20 k	0.05
2048 kbit/s	20 to 100 k	1.5
	18 k to 100 k (Note 2)	0.2
8448 kbit/s	20 to 400 k	1.5
	3 k to 400 k (Note 2)	0.2
34 368 kbit/s	100 to 800 k	1.5
	10 k to 800 k	0.15
139 264 kbit/s	200 to 3.5 M	1.5
	10 k to 3.5 M	0.075

NOTE 1 – For the codirectional interface only.

NOTE 2 – For 2048 kbit/s and 8448 kbit/s interfaces within the network of an operator, the high-pass cut-off frequency may be specified to be 700 Hz (instead of 18 kHz) and 80 kHz (instead of 3 kHz) respectively. However, at interfaces between different operator networks, the values in the table apply, unless involved parties agree otherwise.

NOTE 3 –

64 kbit/s	1 UI = 15.6 μs
2048 kbit/s	1 UI = 488 ns
8448 kbit/s	1 UI = 118 ns
34 368 kbit/s	1 UI = 29.1 ns
139 264 kbit/s	1 UI = 7.18 ns

5.2 Network limits for output wander at traffic interfaces

The MRTIE specifications given in this subclause are intended for application to both asynchronous and synchronous PDH interfaces. Refer to Figures B.1 and B.2, respectively, for the reference network configurations. In the case of asynchronous interfaces, a frequency offset within the limits specified in ITU-T Recommendation G.703 is permitted, in addition to the wander specified in the following subclauses.

It is required that, within a synchronized network, digital equipment provided at nodes shall accommodate permitted phase deviations on the incoming signal, i.e. under normal synchronized conditions, impairments will not occur.

However, it should be recognized that, as a result of some performance degradations, failure conditions, maintenance actions and other events, the phase difference between the incoming signal and the internal timing signal of the terminating equipment may exceed the jitter and wander tolerance of the equipment which may result in an abnormal event such as a slip or bit-error burst.

In addition, at a node which connects to an independently-synchronized network (or where plesiochronous operation is used in national networks), the phase difference between the incoming signal and the internal timing signal of the terminating equipment may eventually exceed the wander tolerance of the equipment in which case an abnormal event such as a slip may occur. The maximum permissible long-term mean controlled slip rate resulting from this mechanism is derived from the clock performance defined in ITU-T Recommendation G.811, i.e. no more than one slip in 70 days.

NOTE – The wander specifications defined in the following subclauses are consistent with the derivation of network limits described for the case of SDH network transport in Appendix I.

The wander measurement requirements (e.g. sampling time and measurement interval) for MTIE, MRTIE and TDEV parameters, the 10 Hz wander measurement filter characteristic and the functional description for measuring output wander are described in ITU-T Recommendation O.172.

Instrumentation in accordance with ITU-T Recommendation O.172 is appropriate for measurement of wander parameters.

Measurement methodologies used to measure the MRTIE parameter are described in Appendix II.

5.2.1 2048 kbit/s interface output wander limit

The maximum level of wander that may exist at a 2048 kbit/s network interface, expressed in MRTIE, shall not exceed the limit given in Table 2. The resultant overall specification is illustrated in Figure 1.

Table 2/G.823 – 2048 kbit/s interface output wander limit

Observation Interval τ (sec)	MRTIE requirement (µs)
$0.05 < \tau \le 0.2$	$46\ \tau$
$0.2 < \tau \le 32$	9
$32 < \tau \le 64$	$0.28\ \tau$
$64 < \tau \le 1\ 000$ (Note)	18
NOTE – For the asynchronous configuration (refer to Figure B.1), the maximum observation interval to be considered is 80 seconds.	

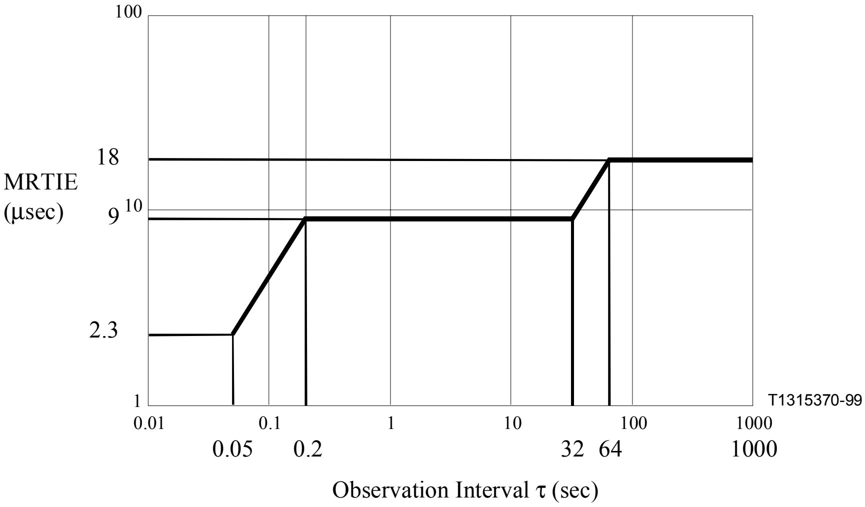


Figure 1/G.823 – 2048 kbit/s interface output wander limit

5.2.2 34 368 kbit/s interface output wander limit

The maximum level of wander that may exist at a 34 368 kbit/s network interface, expressed in MRTIE, shall not exceed the limit given in Table 3. The resultant overall specification is illustrated in Figure 2.

NOTE – 34 368 kbit/s signals can be framed in accordance with ITU-T Recommendation G.832.

Table 3/G.823 – 34 368 kbit/s interface output wander limit

Observation Interval τ (sec)	**MRTIE requirement (µs)**
$0.05 < \tau \leq 0.073$	$14\ \tau$
$0.073 < \tau \leq 2.5$	1
$2.5 < \tau \leq 10$	$0.4\ \tau$
$10 < \tau \leq 80$	4

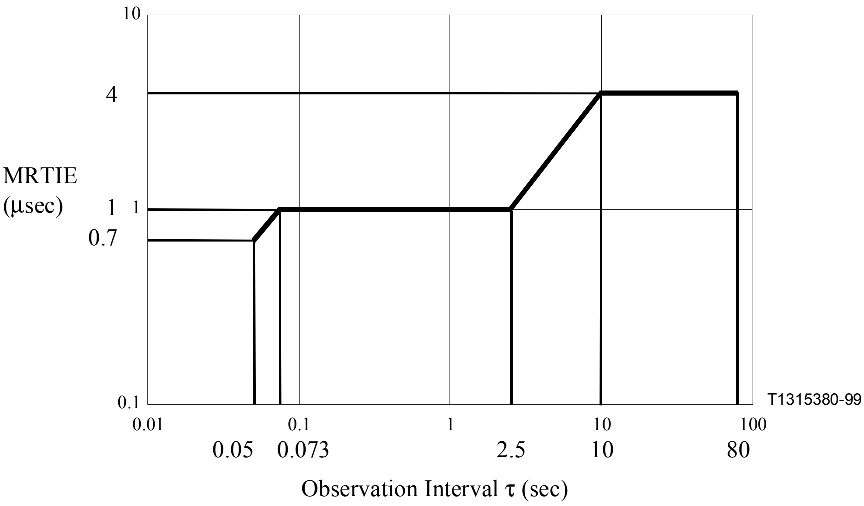


Figure 2/G.823 – 34 368 kbit/s interface output wander limit

5.2.3 139 264 kbit/s interface output wander limit

The maximum level of wander that may exist at a 139 264 kbit/s network interface, expressed in MRTIE, shall not exceed the limit given in Table 4. The resultant overall specification is illustrated in Figure 3.

NOTE – 139 264 kbit/s signals can be framed in accordance with ITU-T Recommendation G.832.

Table 4/G.823 – 139 264 kbit/s interface output wander limit

Observation Interval τ (sec)	MRTIE requirement (μs)
0.05 < τ ≤ 0.15	6.8 τ
0.15 < τ ≤ 2.5	1
2.5 < τ ≤ 10	0.4 τ
10 < τ ≤ 80	4

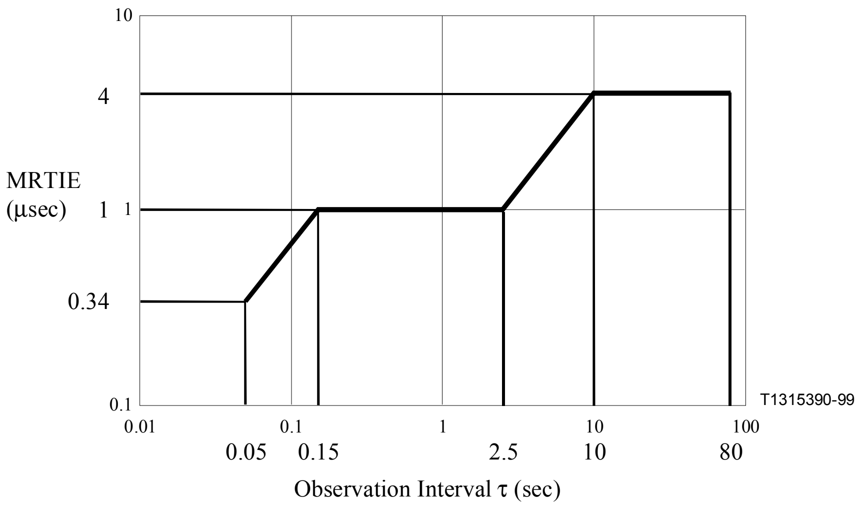


Figure 3/G.823 – 139 264 kbit/s interface output wander limit

6 Network limits for synchronization interfaces

The specification of network limits for synchronization interfaces is primarily intended to reflect the results of a theoretical analysis of the worst-case accumulation of jitter and wander in a synchronization network. These values then serve to specify tolerance requirements for synchronization equipment.

It should, however, also be possible to verify through measurements in a real network that the jitter and wander at a particular interface does not exceed the specified limits. The location of the interface in the synchronization chain of that network determines what margin may be expected with reference to the network limits.

As shown in Figure B.3, an SSU may receive its timing via SDH or PDH distribution. The network limit at the output of these distribution chains represents the amount of jitter and wander that an SSU may experience at its input. Since there is more jitter allowed at PDH interfaces than at SDH Synchronous Transport Module, level N (STM-N) interfaces, the network limit for the PDH distribution outputs represents the worst-case that the SSU should tolerate at its input.

The jitter and wander tolerance of an SEC should be (at least) the amount of jitter and wander at the input of the last SEC of a synchronization chain. Since the contribution of the last SEC in the chain to the network limit at SEC outputs (that is the amount of jitter and wander that may be expected at the output of the last SEC of the chain) is small, the network limit at the SEC output interface can be used as the jitter and wander tolerance requirement for an SEC.

6.1 Network limits for output jitter at synchronization interfaces

The maximum allowable high frequency noise components of a timing signal are specified by the network limits for jitter given in Table 5. These network limits are compatible with the minimum tolerance to jitter that clock equipment input ports are required to provide. The limits given in Table 5 shall be met for all operating conditions at 2048 kbit/s and 2048 kHz synchronization interfaces.

Jitter as measured over a 60 second interval shall not exceed the specified limits, when using the specified measurement filters.

The functional description for measuring output jitter at a digital interface is provided in ITU-T Recommendation O.172. Further requirements concerning the measurement of jitter are defined in 5.1.

Table 5/G.823 – Maximum permissible jitter at synchronization interfaces

Output Interface	Measurement bandwidth, –3 dB frequencies (Hz)	Peak-to-peak amplitude (UIpp)
PRC	20 to 100 k	0.05
SSU	20 to 100 k	0.05
SEC	20 to 100 k	0.5
	49 to 100 k	0.2
PDH synchronization	20 to 100 k	1.5
	18 k to 100 k	0.2
NOTE – For 2048 kbit/s and 2048 kHz synchronization interfaces, UIpp refers to the reciprocal of the clock frequency.		

6.2 Network limits for output wander at synchronization interfaces

At very low frequencies, synchronization networks are transparent to wander. Consequently, two signals received in the same node that derive their timing from the same source, but over different paths, may in the worst-case have opposite phase deviation. The minimum wander tolerance in the frequency range where relevant equipment is affected by the differential phase variation between two inputs is therefore higher than the network limit for absolute wander. The performance of a clock is only influenced by the phase variation that is experienced at the selected synchronization input. That is why the absolute network limits in the following subclauses can be used directly to specify wander tolerance of the SSU and SEC.

The network limit requirements for TDEV are derived from simulation, taking into account the 18 μs wander budget and the requirements of ITU-T Recommendation G.822 (further information is provided in Annex A). However, large diurnal wander with a period of one day and sinusoidal characteristic may cause the TDEV network limit (at SSU, SEC or PDH interfaces) to be exceeded, even if the corresponding MTIE requirement is met. This is because the TDEV parameter does not strongly filter sinusoidal components of wander.

From the large number of available timing characteristics, a subset has been selected to constrain both the standardization as well as the operational verification effort. The selected characteristics are considered to provide sufficient information to ensure satisfactory operation of SDH and PSTN networks.

The wander measurement requirements (e.g. sampling time and measurement interval) for MTIE and TDEV parameters, the 10 Hz wander measurement filter characteristic and the functional description for measuring output wander are described in ITU-T Recommendation O.172.

Instrumentation in accordance with ITU-T Recommendation O.172 is appropriate for measurement of wander parameters.

Measurement methodologies used to measure the MTIE parameter are described in Appendix II.

6.2.1 PRC interface output wander limit

The network limit for wander at the output interface of a PRC, expressed in MTIE, is given in Table 6. The resultant overall specification is illustrated in Figure 4.

Table 6/G.823 – Network limit for wander at PRC interfaces expressed in MTIE

Observation Interval τ (sec)	MTIE requirement (ns)
$0.1 < \tau \leq 1\,000$	$25 + 0.275\,\tau$
$\tau > 1\,000$	$290 + 0.01\,\tau$

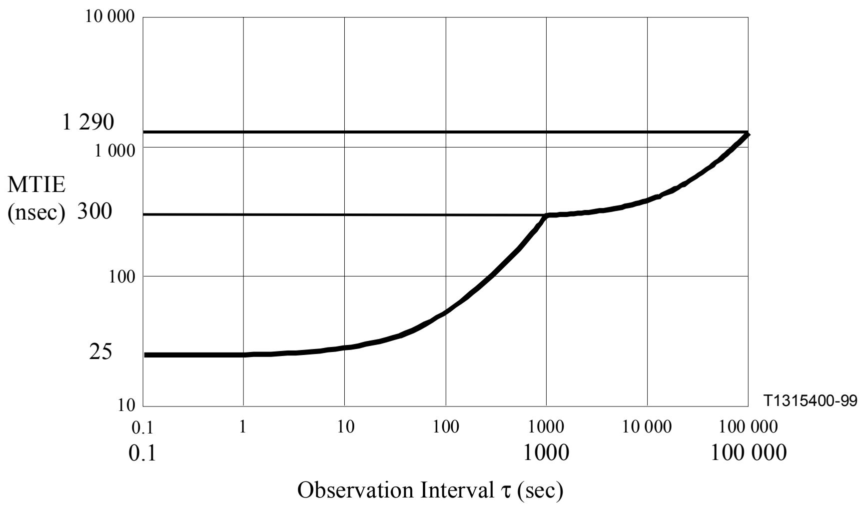


Figure 4/G.823 – Network limit for wander (MTIE) at PRC interfaces

The network limit for wander at the output interface of a PRC, expressed in TDEV, is given in Table 7. The resultant overall specification is illustrated in Figure 5.

Table 7/G.823 – Network limit for wander at PRC interfaces expressed in TDEV

Observation Interval τ (sec)	TDEV requirement (ns)
0.1 < τ ≤ 100	3
100 < τ ≤ 1 000	0.03 τ
1 000 < τ ≤ 10 000	30
10 000 < τ ≤ 1 000 000	27 + 0.000 3 τ

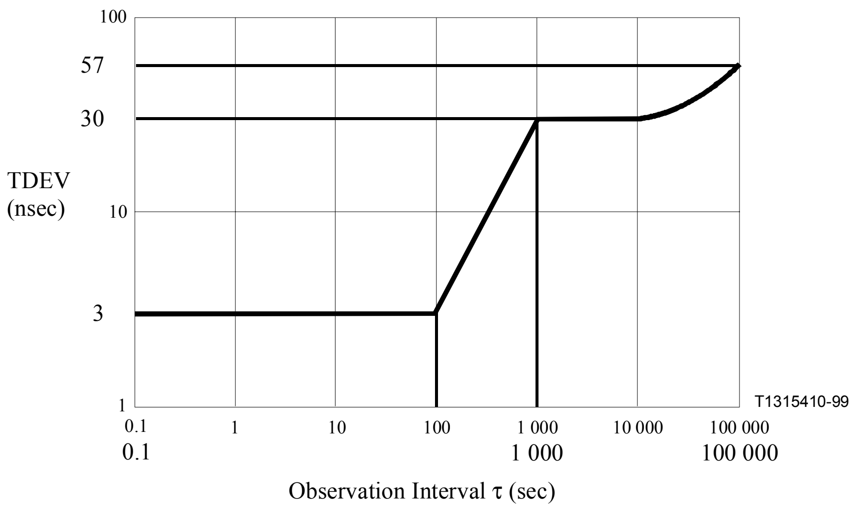


Figure 5/G.823 – Network limit for wander (TDEV) at PRC interfaces

6.2.2 SSU interface output wander limit

The network limit for wander at the output interface of an SSU, expressed in MTIE, is given in Table 8. The resultant overall specification is illustrated in Figure 6.

NOTE – The values are relative to UTC, i.e. they include the wander of the PRC.

Table 8/G.823 – Network limit for wander at SSU interfaces expressed in MTIE

Observation Interval τ (sec)	MTIE requirement (ns)
0.1 < τ ≤ 2.5	25
2.5 < τ ≤ 200	10 τ
200 < τ ≤ 2 000	2 000
τ > 2 000	$433\ \tau^{0.2} + 0.01\ \tau$

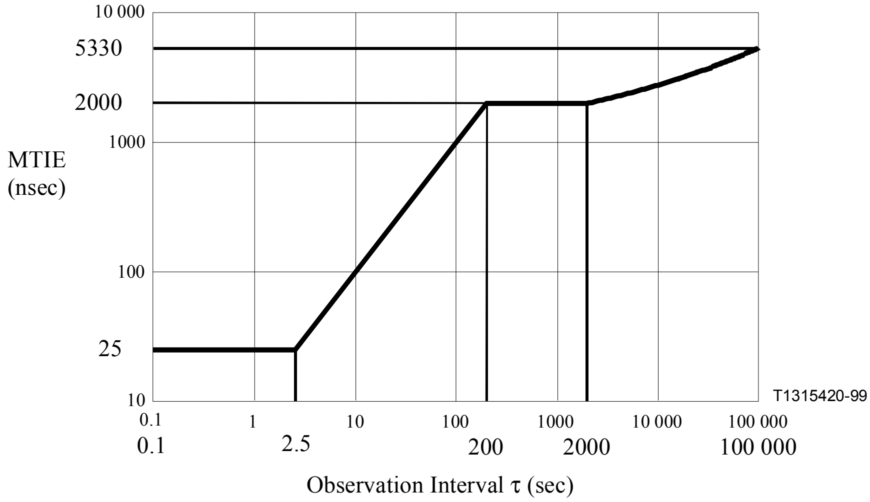


Figure 6/G.823 – Network limit for wander (MTIE) at SSU interfaces

The network limit for wander at the output interface of an SSU, expressed in TDEV, is given in Table 9. The resultant overall specification is illustrated in Figure 7.

Table 9/G.823 – Network limit for wander at SSU interfaces expressed in TDEV

Observation Interval τ (sec)	TDEV requirement (ns)
$0.1 < \tau \leq 4.3$	3
$4.3 < \tau \leq 100$	$0.7\ \tau$
$100 < \tau \leq 1\ 000\ 000$	$58 + 1.2\ \tau^{0.5} + 0.000\ 3\ \tau$

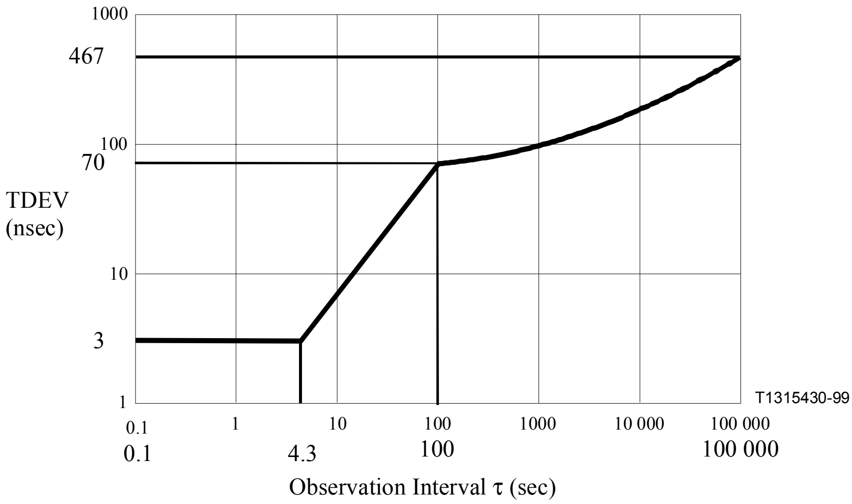


Figure 7/G.823 – Network limit for wander (TDEV) at SSU interfaces

6.2.3 SEC interface output wander limit

The network limit for wander at the output interface of an SEC, expressed in MTIE, is given in Table 10. The resultant overall specification is illustrated in Figure 8.

NOTE – The values are relative to UTC, i.e. they include the wander of the PRC.

Table 10/G.823 – Network limit for wander at SEC interfaces expressed in MTIE

Observation Interval τ(sec)	MTIE requirement (ns)
$0.1 < \tau \le 2.5$	250
$2.5 < \tau \le 20$	$100\ \tau$
$20 < \tau \le 2\,000$	2 000
$\tau > 2\,000$	$433\ \tau^{0.2} + 0.01\ \tau$

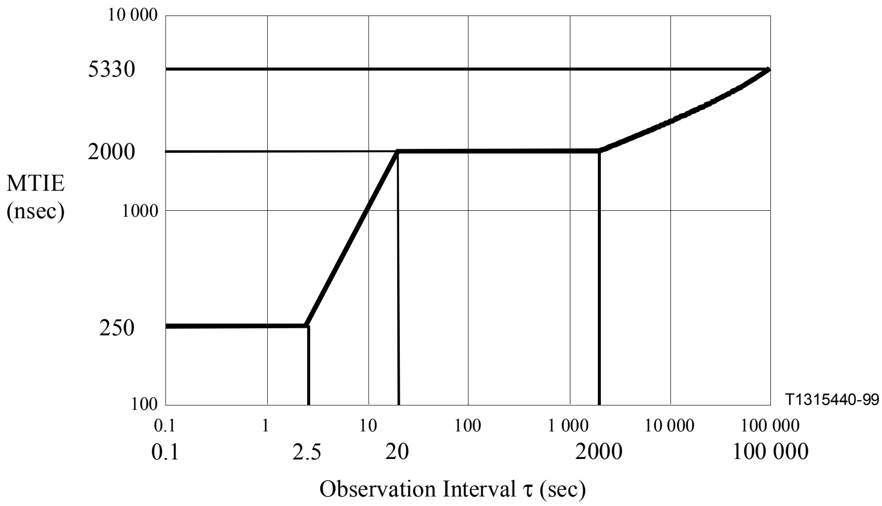


Figure 8/G.823 – Network limit for wander (MTIE) at SEC interfaces

The network limit for wander at the output interface of an SEC, expressed in TDEV, is given in Table 11. The resultant overall specification is illustrated in Figure 9.

Table 11/G.823 – Network limit for wander at SEC interfaces expressed in TDEV

Observation Interval τ (sec)	TDEV requirement (ns)
$0.1 < \tau \le 17.14$	12
$17.14 < \tau \le 100$	$0.7\ \tau$
$100 < \tau \le 1\,000\,000$	$58 + 1.2\ \tau^{0.5} + 0.000\,3\ \tau$

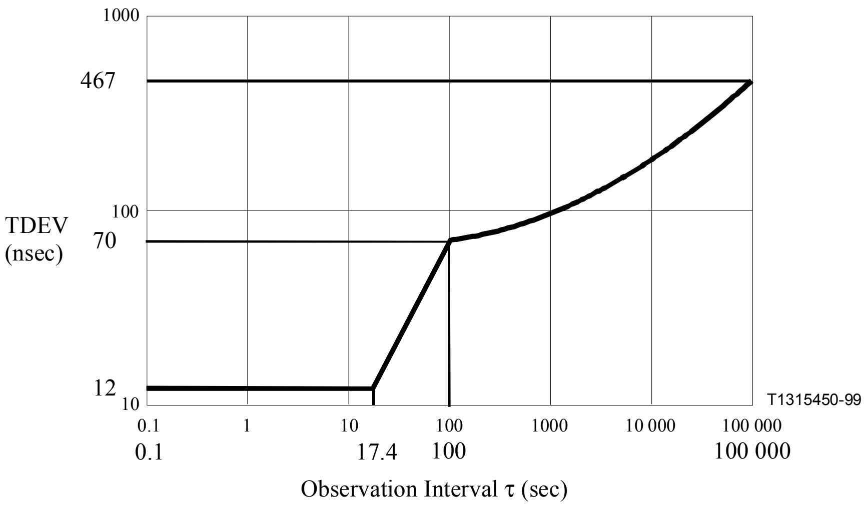


Figure 9/G.823 – Network limit for wander (TDEV) at SEC interfaces

6.2.4 PDH synchronization interface output wander limit

The network limit for wander at a PDH synchronization output interface, expressed in MTIE, is given in Table 12. The resultant overall specification is illustrated in Figure 10.

NOTE 1 – In the case when a 34 368 kbit/s or 139 264 kbit/s signal framed in accordance with ITU-T Recommendation G.832 is used as a synchronization interface, the output wander limit is for further study.

Table 12/G.823 – Network limit for wander at PDH synchronization interfaces expressed in MTIE

Observation Interval τ (sec)	MTIE requirement (ns)
$0.1 < \tau \leq 7.3$	732
$7.3 < \tau \leq 20$	$100\ \tau$
$20 < \tau \leq 2\ 000$	2 000
$\tau > 2\ 000$	$433\ \tau^{0.2} + 0.01\ \tau$

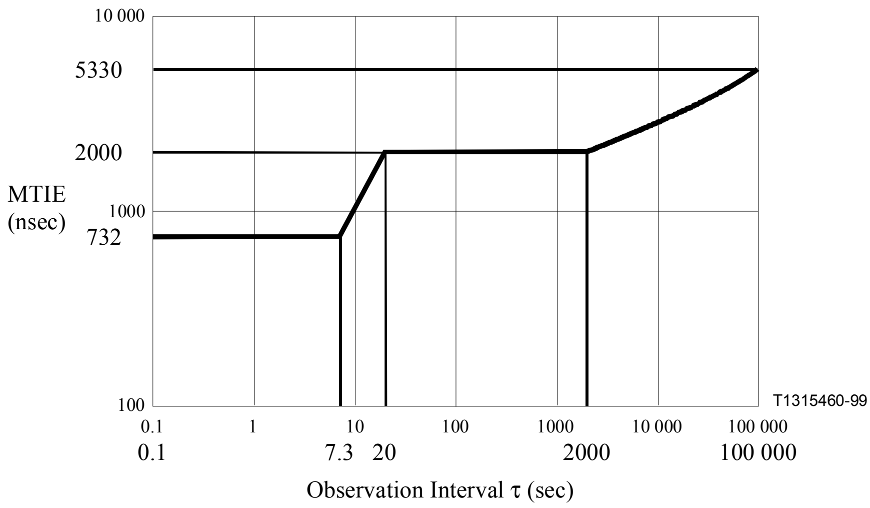


Figure 10/G.823 – Network limit for wander (MTIE) at PDH synchronization interfaces

The network limit for wander at a PDH synchronization output interface, expressed in TDEV, is given in Table 13. The resultant overall specification is illustrated in Figure 11.

NOTE 2 – In the case when a 34 368 kbit/s or 139 264 kbit/s signal framed in accordance with ITU-T Recommendation G.832 is used as a synchronization interface, the output wander limit is for further study.

Table 13/G.823 – Network limit for wander at PDH synchronization interfaces expressed in TDEV

Observation Interval τ (sec)	TDEV requirement (ns)
$0.1 < \tau \leq 48$	34
$48 < \tau \leq 100$	$0.7\ \tau$
$100 < \tau \leq 1\ 000\ 000$	$58 + 1.2\ \tau^{0.5} + 0.000\ 3\ \tau$

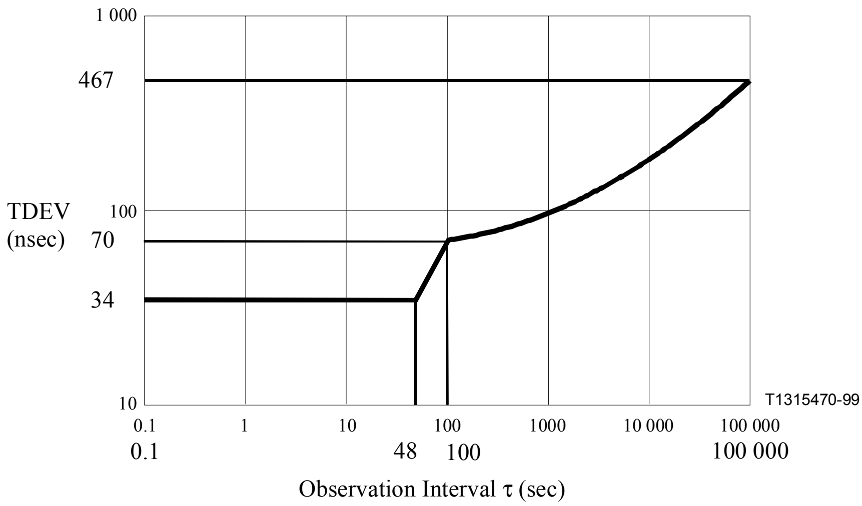


Figure 11/G.823 – Network limit for wander (TDEV) at PDH synchronization interfaces

7 Jitter and wander tolerance of network interfaces

7.1 Jitter and wander tolerance of traffic interfaces

In order to ensure that, in general, any equipment can be connected to any appropriate interface within a network, it is necessary to arrange that the input ports of all equipment types are capable of accommodating levels of jitter and wander up to at least the minimum limits defined in the following subclauses.

The jitter and wander tolerance of a PDH interface indicates the minimum level of phase noise that the input port shall accommodate whilst:

a) not causing any alarms;

b) not causing any slips; and

c) not causing any bit errors.

All digital input ports of equipment shall be able to tolerate a digital signal that has:

a) electrical characteristics in accordance with the requirements of ITU-T Recommendation G.703;

b) a constant frequency offset (relative to the nominal value) within the range defined in Table 14;

c) a rate of change in frequency up to at least 1 ppm/minute for 2048 kbit/s interfaces and up to at least 0.5 ppm/minute for 34 368 kbit/s and 139 264 kbit/s interfaces; and

d) a sinusoidal phase deviation having an amplitude-frequency relationship defined in the following subclauses.

In principle, these requirements shall be met regardless of the information content of the digital signal. However, for test purposes, the content of the signal with jitter and wander modulation should be a structured test sequence as defined in the following subclauses.

When specifying or assessing interface tolerance, two equipment operating conditions can be distinguished:

a) non-synchronized operation, where the receiving equipment is not being timed from a source that is synchronous with the interface under consideration. In this case, it is the equipment capability to accommodate phase variation on the incoming signal (in terms of clock recovery circuitry and synchronizer/desynchronizer buffers) that is of interest; and

b) synchronized operation, where the receiving equipment is being timed from a source that is synchronous with the interface under consideration. In this case, slip buffer dimension and operation is also of interest.

Unless otherwise stated, the tolerance specifications in the following subclauses apply to both non-synchronized and synchronized operating conditions.

The peak-to-peak phase amplitude specification above 10 Hz reflects the maximum permissible jitter magnitude in a digital network. However the specification below 10 Hz does not aim to represent the maximum permissible wander that might occur in practice. Below 10 Hz, the limits are derived such that where necessary, the provision of this level of buffer storage at the input of an equipment facilitates the accommodation of wander generated in a large proportion of real connections.

For convenience of testing, the required tolerance is defined in terms of the peak-to-peak amplitude and frequency of sinusoidal jitter which modulates a digital test pattern. It is important to recognize that this test condition is not, in itself, intended to be representative of the type of jitter found in practice in a network.

Guidance on the measurement setup for input jitter and wander tolerance is provided in Appendix III.

Instrumentation in accordance with ITU-T Recommendation O.171 is appropriate for generation of jitter and wander in PDH systems.

Table 14/G.823 – Maximum frequency offset at traffic interfaces

Interface	Maximum frequency offset (±ppm)	Example Application
64 kbit/s	0	Switch input channel
2048 kbit/s	0	Switch, 1/0 cross-connect
	4.6	Byte-synchronous mapping into SDH
	50	PDH, asynchronous mapping into SDH
8448 kbit/s	30	PDH
34 368 kbit/s	20	PDH, asynchronous mapping into SDH
	4.6	Signal defined in ITU-T Recommendation G.832
139 264 kbit/s	15	PDH, asynchronous mapping into SDH
	4.6	Signal defined in ITU-T Recommendation G.832
NOTE – Frequency offset values are aligned with ITU-T Recommendations G.703 and G.813.		

7.1.1 64 kbit/s input jitter and wander tolerance

The level of jitter and wander that can be accommodated by a 64 kbit/s codirectional network interface, expressed in peak-to-peak sinusoidal phase amplitude, shall exceed the values given in Table 15. The resultant overall specification is illustrated in Figure 12. The test sequence to be used is a PRBS of length $2^{11} - 1$, defined in ITU-T Recommendation O.150.

Table 15/G.823 – Minimum requirement for 64 kbit/s input jitter and wander tolerance

Frequency f (Hz)	Requirement (pk-pk phase amplitude)
12 μ < f ≤ 4.3	18 μs
4.3 < f ≤ 20	$77 f^{-1}$ μs
20 < f ≤ 600	0.25 UI
600 < f ≤ 3 k	$150 f^{-1}$ UI
3 k < f ≤ 20 k	0.05 UI
NOTE – 1 UI = 15.6 μs.	

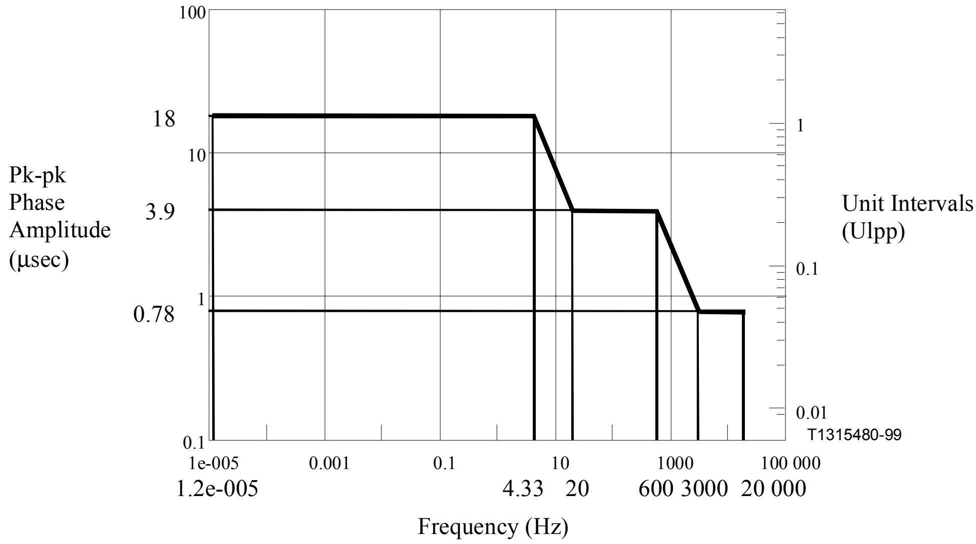


Figure 12/G.823 – 64 kbit/s input jitter and wander tolerance limit

7.1.2 2048 kbit/s input jitter and wander tolerance

The level of jitter and wander that can be accommodated by a 2048 kbit/s network interface, expressed in peak-to-peak sinusoidal phase amplitude, shall exceed the values given in Table 16. The resultant overall specification is illustrated in Figure 13. The test sequence to be used is a PRBS of length $2^{15} - 1$, defined in ITU-T Recommendation O.150.

Table 16/G.823 – Minimum requirement for 2048 kbit/s input jitter and wander tolerance

Frequency f (Hz)	Requirement (pk-pk phase amplitude)
12 µ < f ≤ 4.88 m	18 µs
4.88 m < f ≤ 10 m	$0.088\ f^{-1}$ µs
10 m < f ≤ 1.67	8.8 µs
1.67 < f ≤ 20	$15\ f^{-1}$ µs
20 < f ≤ 2.4 k (Note 1)	1.5 UI
2.4 k < f ≤ 18 k (Note 1)	$3.6 \times 10^3\ f^{-1}$ UI
18 k < f ≤ 100 k (Note 1)	0.2 UI
NOTE 1 – For 2048 kbit/s interfaces within the network of an operator, the frequencies may be specified as 93 Hz (instead of 2.4 kHz) and 700 Hz (instead of 18 kHz). However, at interfaces between different operator networks, the values in the table apply, unless involved parties agree otherwise. NOTE 2 – 1 UI = 488 ns.	

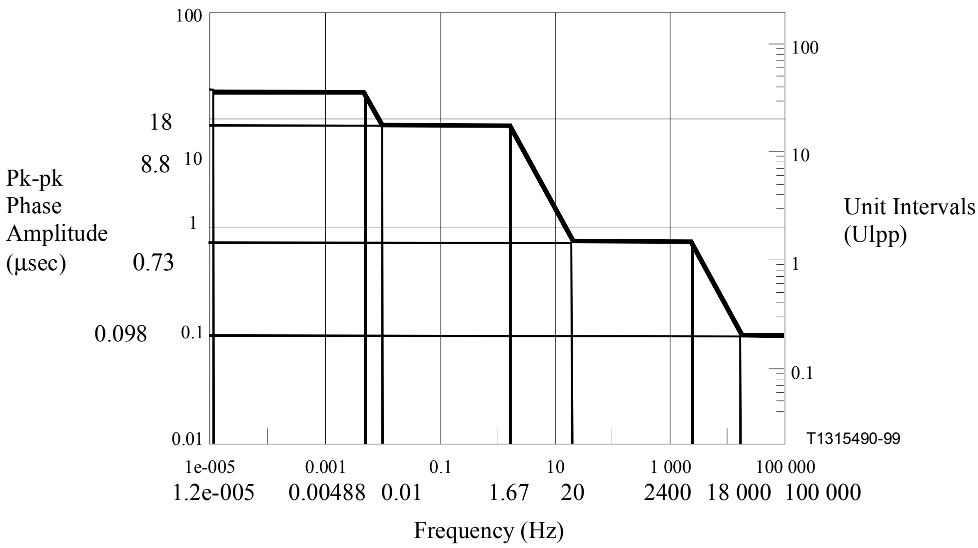


Figure 13/G.823 – 2048 kbit/s input jitter and wander tolerance limit

7.1.3 8448 kbit/s input jitter and wander tolerance

The level of jitter and wander that can be accommodated by a 8448 kbit/s network interface, expressed in peak-to-peak sinusoidal phase amplitude, shall exceed the values given in Table 17. The resultant overall specification is illustrated in Figure 14. The test sequence to be used is a PRBS of length $2^{15} - 1$, defined in ITU-T Recommendation O.150.

NOTE – Tolerance requirements for frequencies below 20 Hz are not defined because an 8448 kbit/s mapping for SDH networks is not defined in ITU-T Recommendation G.707.

Table 17/G.823 – Minimum requirement for 8448 kbit/s input jitter and wander tolerance

Frequency f (Hz)	**Requirement (pk-pk phase amplitude)**
20 < f ≤ 400 (Note 1)	1.5 UI
400 < f ≤ 3 k (Note 1)	600 f^{-1} UI
3 k < f ≤ 400 k (Note 1)	0.2 UI
NOTE 1 – For 8448 kbit/s interfaces within the network of an operator, the frequencies may be specified as 10.7 kHz (instead of 400 Hz) and 80 kHz (instead of 3 kHz). However, at interfaces between different operator networks, the values in the table apply, unless involved parties agree otherwise. NOTE 2 – 1 UI = 118 ns.	

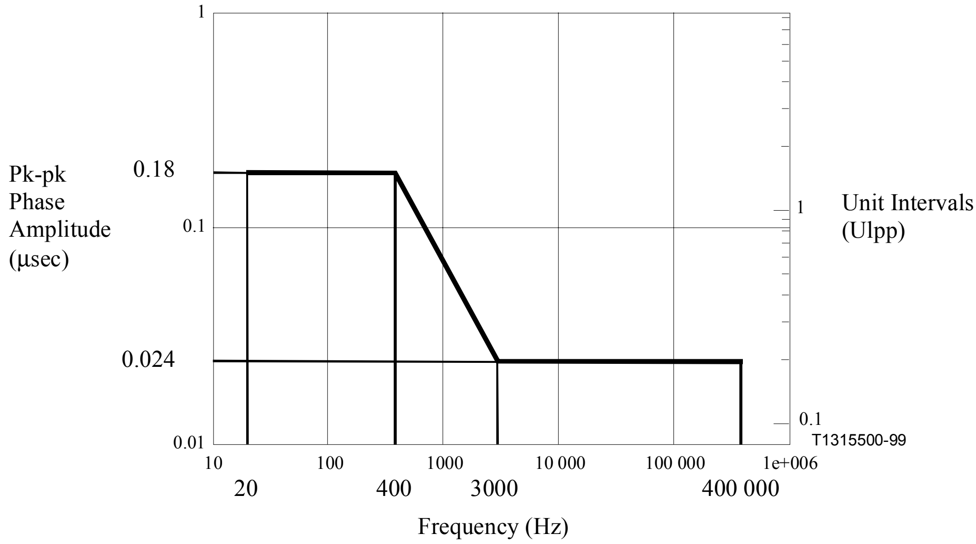


Figure 14/G.823 – 8448 kbit/s input jitter and wander tolerance limit

7.1.4 34 368 kbit/s input jitter and wander tolerance

The level of jitter and wander that can be accommodated by a 34 368 kbit/s network interface, expressed in peak-to-peak sinusoidal phase amplitude, shall exceed the values given in Table 18. The resultant overall specification is illustrated in Figure 15. The test sequence to be used is a PRBS of length $2^{23} - 1$, defined in ITU-T Recommendation O.150; for signals in accordance with ITU-T Recommendation G.832, the test sequence to be used is for further study.

Table 18/G.823 – Minimum requirement for 34 368 kbit/s input jitter and wander tolerance

Frequency f (Hz)	Requirement (pk-pk phase amplitude)
10 m < f ≤ 32 m	4 µs
32 m < f ≤ 130 m	$0.13\ f^{-1}$ µs
130 m < f ≤ 4.4	1 µs
4.4 < f ≤ 100	$4.4\ f^{-1}$ µs
100 < f ≤ 1 k	1.5 UI
1 k < f ≤ 10 k	$1.5 \times 10^{3}\ f^{-1}$ UI
10 k < f ≤ 800 k	0.15 UI
NOTE – 1 UI = 29.1 ns.	

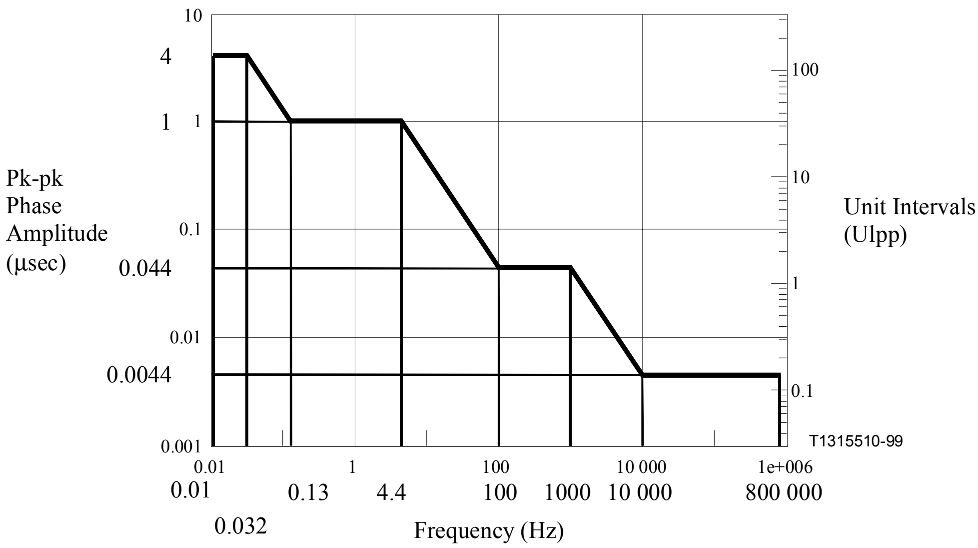


Figure 15/G.823 – 34 368 kbit/s input jitter and wander tolerance limit

7.1.5 139 264 kbit/s input jitter and wander tolerance

The level of jitter and wander that can be accommodated by a 139 264 kbit/s network interface, expressed in peak-to-peak sinusoidal phase amplitude, shall exceed the values given in Table 19. The resultant overall specification is illustrated in Figure 16. The test sequence to be used is a PRBS of length $2^{23} - 1$, defined in ITU-T Recommendation O.150; for signals in accordance with Recommendation G.832, the test sequence to be used is for further study.

Table 19/G.823 – Minimum requirement for 139 264 kbit/s input jitter and wander tolerance

Frequency f (Hz)	Requirement (pk-pk phase amplitude)
10 m < f ≤ 32 m	4 µs
32 m < f ≤ 130 m	$0.13 f^{-1}$ µs
130 m < f ≤ 2.2	1 µs
2.2 < f ≤ 200	$2.2 f^{-1}$ µs
200 < f ≤ 500	1.5 UI
500 < f ≤ 10 k	$750 f^{-1}$ UI
10 k < f ≤ 3.5 M	0.075 UI
NOTE – 1 UI = 7.18 ns.	

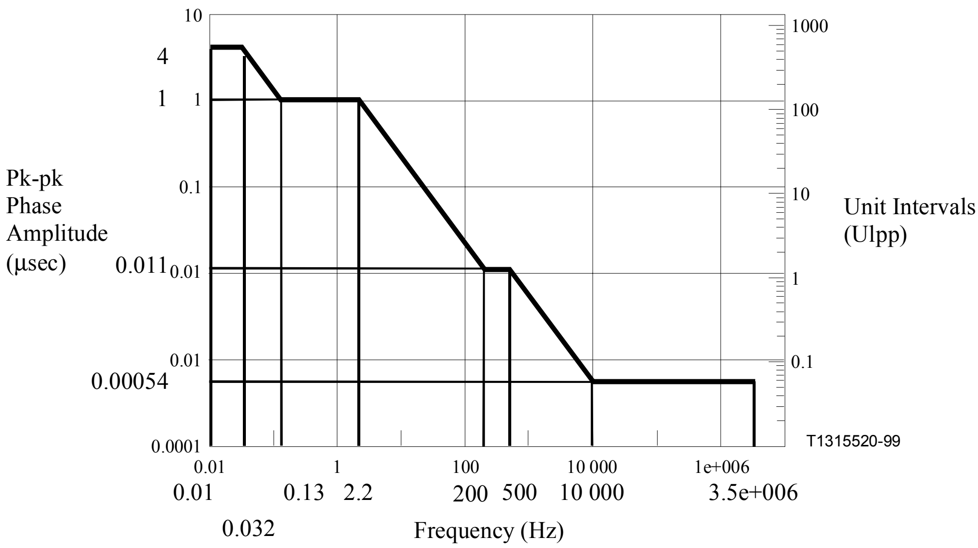


Figure 16/G.823 – 139 264 kbit/s input jitter and wander tolerance limit

7.2 Jitter and wander tolerance of synchronization interfaces

The input jitter and wander tolerance of synchronization interfaces shall meet the jitter and wander tolerance specifications of clock input ports given in Type I of ITU-T Recommendation G.812 (for equipment containing an SSU function) and Option 1 of ITU-T Recommendation G.813 (for equipment containing an SEC function).

ANNEX A

Network model underlying the synchronization network limit

A.1 Introduction

The method of deriving network limits is based on numerical simulations, carried out on a certain network model that is representative of a "reasonable worst-case" network from the point of view of synchronization. A description of this reference network and other assumptions that went into the composition of the network limits are outlined in this annex.

A.2 Considerations on the network model

The synchronization network limits are a compromise between several conflicting requirements, since one needs to align specifications of the individual equipment with the performance criteria that are applicable to the network as a whole. The number of possible networks that are and can be built is almost without bound, therefore a reference network is needed that is "worse" than the large majority of the real networks from a synchronization point of view. The list below contains the most important elements that need to be considered when a reference network is constructed:

a) the first element is the specification of individual clocks that are part of the synchronization trail to a network element: the more phase noise each clock is allowed to produce the higher the network limit will be. These noise specifications are defined in ITU-T Recommendations G.811, G.812 and G.813 for PRCs, SSUs and SECs, respectively;

b) the composition of the complete synchronization chain in terms of how many clocks of each type (PRC, SSU or SEC) are cascaded and in what order is the second important element. Such a synchronization reference chain is defined in ITU-T Recommendation G.803 and consists of 1 PRC followed by 10 SSUs and 20 SECs (there may be 40 more SECs between the SSUs but those are of no consequence for the problem at hand); and

c) apart from the noise generated by the individual clocks, diurnal wander and the phase transients that occur on the synchronization links are also factors. The (conservative) assumption was that between any two SSUs there will be on average 1 transient per 25 days. The size of each transient was taken to be 1 μs with random polarity. Compared to the cumulative effect of clock noise and transients, the effect of diurnal wander is negligible if the synchronization trail is predominantly transported over buried optical cable.

The three items mentioned above completely determine the network limit for synchronization interfaces. However, a reference data network is also needed to verify whether these limits are consistent with existing performance requirements.

The important aspects of the architecture of the reference data connection are those that influence the wander accumulation of the data signal, i.e. the number of SDH islands on the link and the number of pointer processors inside each island. This reference data connection should be representative for any 2048 kbit/s link between two pieces of equipment that have slip-buffer termination (e.g. two international gateway switches) – this is because an equipment with slip-buffer termination completely re-times the signal. The reference data connection was chosen to consist of 4 SDH islands, each having 8 TU-12 pointer processors, in an otherwise PDH connection. The network model also (conservatively) assumes that each node that needs timing is synchronized via an independent worst-case synchronization chain.

Finally, the performance requirements against which the resulting differential wander on the receiving slip-buffer is to be evaluated are specified in this ITU-T Recommendation and ITU-T Recommendation G.822. This ITU-T Recommendation prescribes a maximum amount of differential input wander of 18 μs over a time period that is defined to be 24 hours. ITU-T Recommendation G.822 specifies a slip performance better than 0.3 per day (98.9% of the time) for the national part of a 27 500 km reference connection. This national part was considered to be the right benchmark for the network model.

The elements in the list above lead to the reference network shown in Figure A.1. This model includes multiple PRCs to make it applicable for data paths that traverse multiple PRC timing domains.

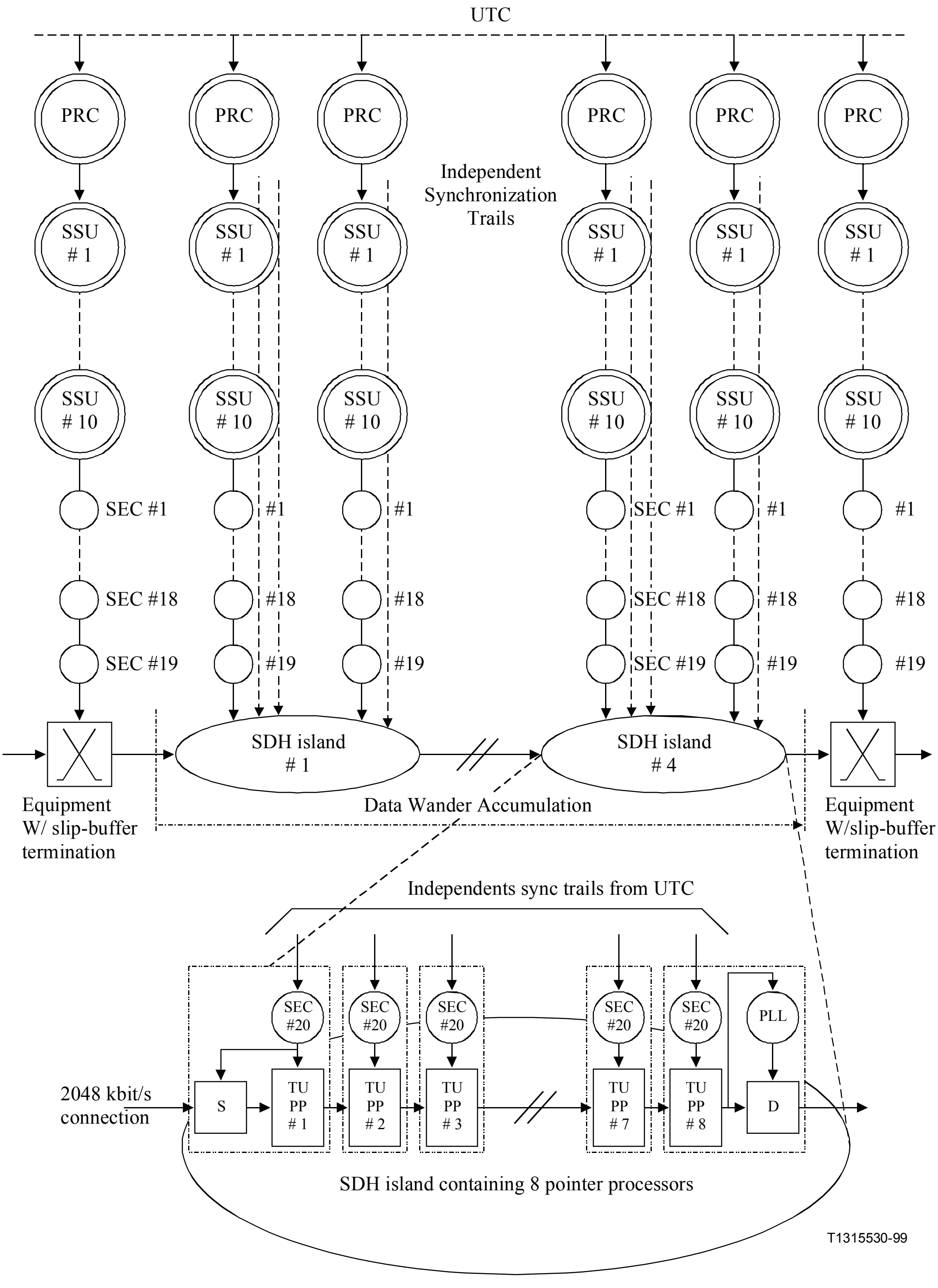


Figure A.1/G.823 – Network model for data and clock wander accumulation

To determine the differential wander at the input of the receiving slip-buffer terminating equipment, two other factors are of importance which were not directly included in the simulations, but for which separate allocations have been made in the wander budget (see also A.3):

a) the mapping wander of 2048 kbit/s signals into VC-12 has to be taken into account; and

b) the diurnal wander caused by environmental influences on the optical fibres that carry the signals under consideration has to be taken into account.

A.3 Information regarding the simulations

Figure A.2 depicts the model that was used in the simulations to generate the noise on the clock inputs of all SDH equipment along the data path and the transmitting and receiving slip-buffer terminating equipment. The intrinsic noise and the transients are generated separately. The intrinsic noise of 1 PRC and 10 SSUs followed by 20 SECs is based on data from ITU-T Recommendations G.811, G.812 and G.813.

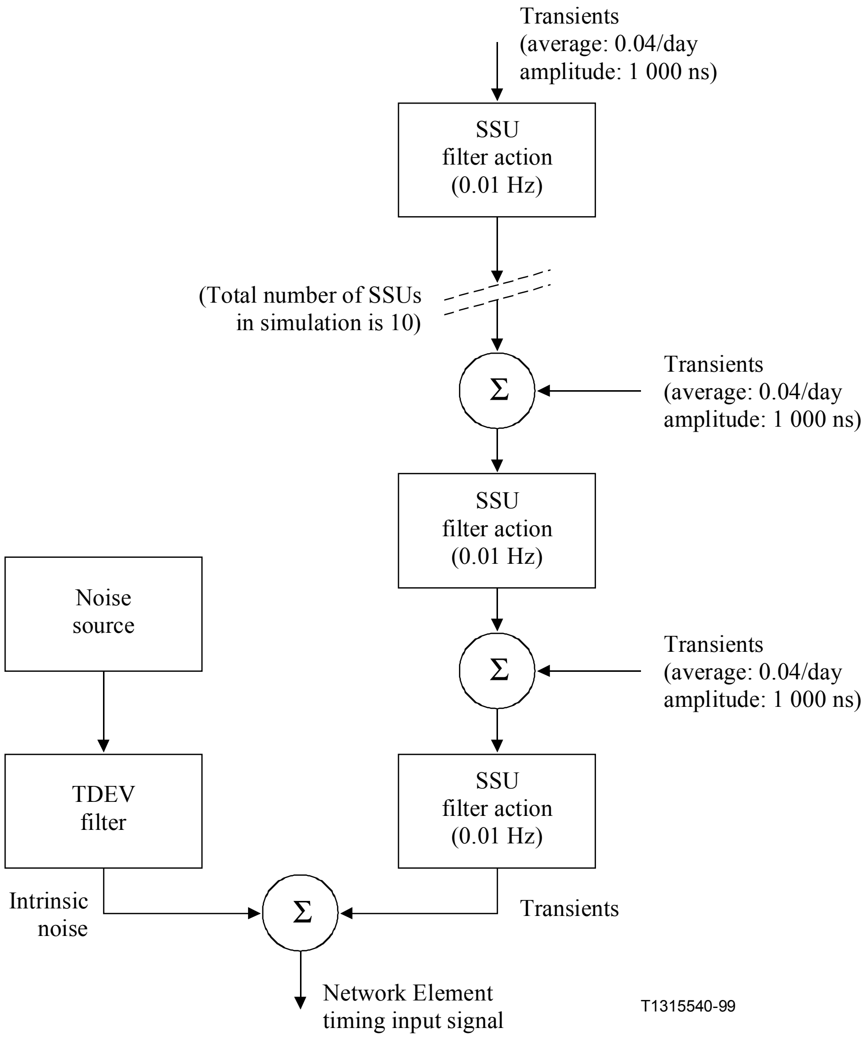


Figure A.2/G.823 – Clock noise generator in simulation program

For the purpose of the simulations, some more assumptions had to be made to keep the complexity to an acceptable level without affecting the results significantly:

a) the elastic stores in the TU-12 pointer processors are taken to be two bytes. This is the minimum elastic store space as prescribed by ITU-T Recommendation G.783;

b) the mapping method of the 2048 kbit/s data stream into the VC-12 is taken to be asynchronous;

c) the initial buffer fill of the TU-12 pointer processor elastic stores is random with a uniform distribution. To eliminate the effect of initial distribution, the first 50 000 points of each simulation run were discarded;

d) the time-increment between subsequent phase points is taken to be 1 second; and

e) the desynchronizer filters have not been taken into account, as this does not affect the long-term effects that are of importance when evaluating wander and slip performance.

Some factors that were not included in the simulations are:

f) the diurnal wander caused by environmental influences on the optical fibres that carry the data signals under consideration has not been taken into account. This effect is separately accounted for, by allocating 1 μs in the wander budget. This number is based on a fibre optical link of 6 000 km length, subject to a temperature change of 2°C and with a temperature coefficient of 85 ps/km/°C;

g) the mapping wander of 2048 kbit/s signals into VC-12 was not included, but was accounted for afterwards, by allocating 2 μs in the wander budget to cater for this effect. This number is based on the argument that the VC-12 mapping wander is at most 2 UI for one island. It is assumed that the wander processes are uncorrelated – RMS addition is therefore allowed. For four islands, a wander budget of 4 UI (corresponding to 2 μs at 2048 kbit/s) is allocated;

h) the effect of AU-4 pointer processing has been neglected, given the complication of including it in the simulations and since its contribution is not significant; and

i) the wander that is caused by PDH multiplexing and line equipment that is part of the reference connection was also considered to be a small contributor and was not taken into account in the simulations.

From the above listed allocation, the following budget for the 18 μs can be derived:

Diurnal wander due to environmental effects:	1 μs
Mapping wander due to asynchronous 2048 kbit/s mapping:	2 μs
Wander caused by clock noise and transients:	15 μs
Total:	18 μs

Simulations on the network model of Figure A.1 show that the differential wander on the input of the receiving slip buffer caused by clock noise is 12.6 μs over 24 hours (averaged MTIE over 40 runs of 800 000 seconds). The corresponding slip-rate is 0.016 slips/day on average.

Thus, the above assumptions and network model lead to a consistent set of specifications.

ANNEX B

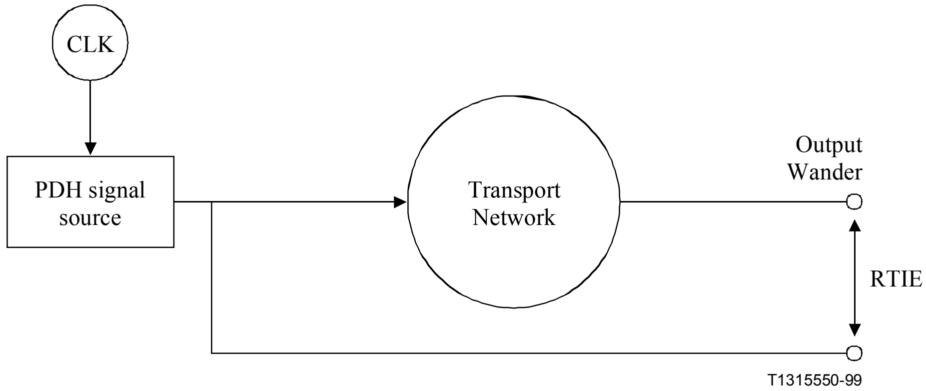
Network wander reference model and parameters

B.1 Wander reference model for traffic interfaces

Wander is always specified and measured as a Relative Time Interval Error (RTIE) between the signal of interest and some reference clock. However, the reference clock against which the RTIE is specified or measured depends on the type of signal of interest. For the purposes of this ITU-T Recommendation, two cases can be distinguished, which are described in B.1.1 and B.1.2.

B.1.1 Asynchronous PDH connection

The appropriate reference for specifying the output wander of asynchronous PDH signals is the signal source itself. For measurement purposes, since that source is not normally available for use as the reference clock, it can be substituted by a suitably-processed version of the output signal. Appendix II has further information regarding this. The reference model is illustrated in Figure B.1.

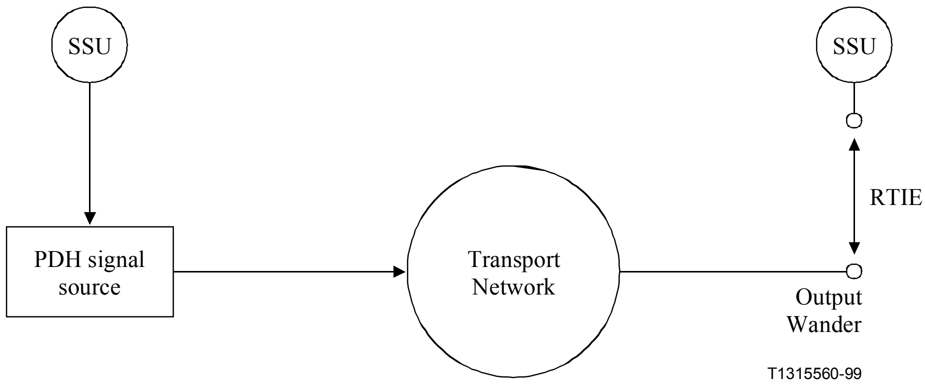


NOTE – CLK frequency offset conforms to bit-rate specifications of ITU-T Recommendation G.703.

Figure B.1/G.823 – Wander reference model for asynchronous PDH connection

B.1.2 Synchronous PDH connection

The appropriate reference for specifying the output wander of synchronous PDH signals (i.e. most 2048 kbit/s signals as well as signals framed according to ITU-T Recommendation G.832) is the network clock reference used at the PDH signal termination. This means that the wander of two reference clock distribution networks must be added to the output wander generated by the transport network. The reference model is illustrated in Figure B.2.



NOTE 1 – SSU outputs conform to network wander limit of 6.2.2.
NOTE 2 – Both SSUs are traceable to a PRC.

Figure B.2/G.823 – Wander reference model for synchronous PDH connection

Although for the asynchronous and synchronous cases, different wander sources contribute to the total output wander, the resulting RTIE is not very different. Due to a lack of correlating effects and statistically-speaking, the transport network wander is the dominant source when compared with the synchronization network wander. Consequently the same network limits have been set for both cases in the output wander specifications given in 5.2.

B.1.3 Specification of wander by MRTIE parameter

There are several parameters in use for specifying wander in standard specifications, such as MTIE and TDEV. For the purposes of this ITU-T Recommendation, MRTIE (Maximum Relative Time

Interval Error) has been selected for traffic interfaces because it is most suitable to allow derivation of consequent equipment performance specifications.

For asynchronous payloads (refer to Figure B.1), the MRTIE specifies the wander accumulated by the network relative to the input signal phase. This is reasonable because it provides information for designing the filter required for any filtering of the transported signal clock in order to achieve the required phase stability of the payload.

For synchronous payloads (refer to Figure B.2), the MRTIE specifies the wander of the payload output relative to the clock phase of an input buffer (e.g. located in an exchange). This is reasonable because it provides information for designing the buffer size.

Measurement methodologies used to measure the MRTIE parameter are described in Appendix II.

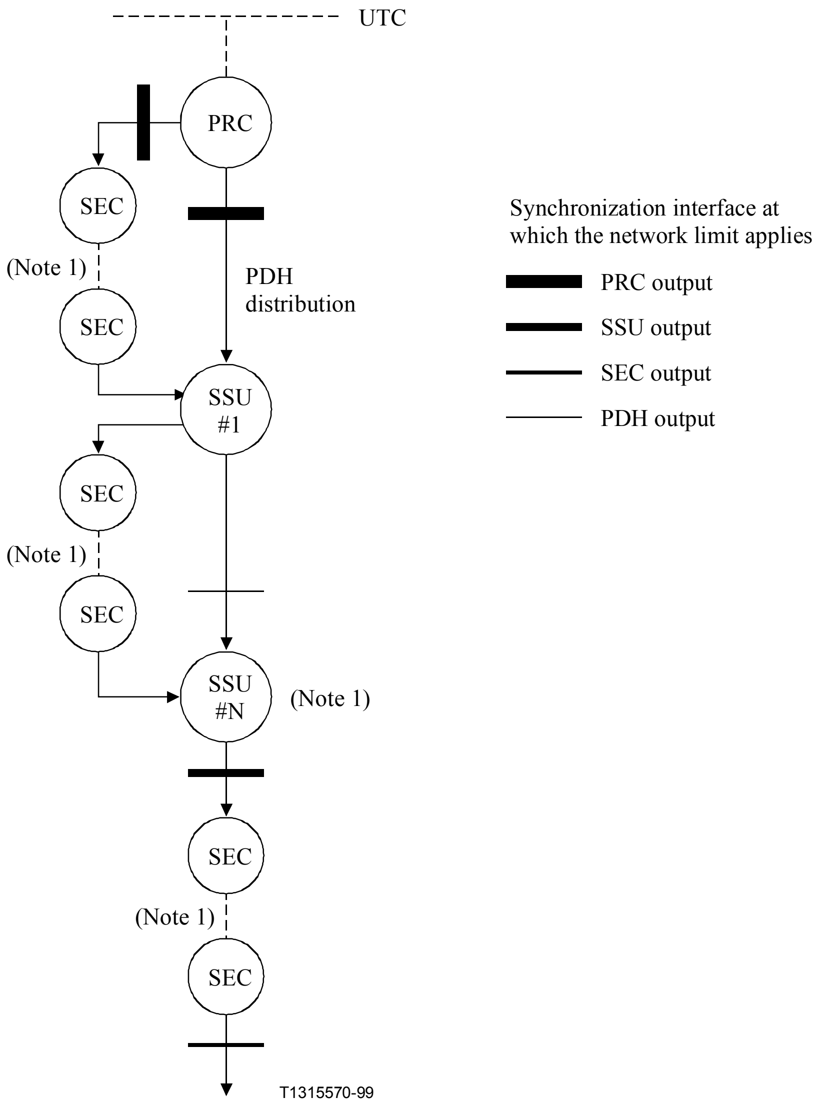
B.2 Wander reference model for synchronization interfaces

The synchronization interfaces that are specified in this ITU-T Recommendation are illustrated in Figure B.3. This figure is an expanded version of Figure 8-5/G.803, showing examples of actual physical interfaces that may appear in synchronization networks. Universal Time Coordinated (UTC) is indicated in Figure B.3 as the reference relative to which all network limits are specified. There is no physical entity or interface associated with UTC, due to the way it is defined.

Two alternative synchronization distribution methods may be used between Synchronization Supply Unit (SSUs), and between Primary Reference Clock (PRC) and SSUs:

a) SDH distribution makes use of the SDH section layer and may be a cascade of sections with at most 20 intermediate SDH network elements, each containing an SDH Equipment Clock (SEC); and

b) PDH distribution makes use of a 2048 kbit/s PDH path that may be traversing a number of intermediate PDH multiplexing stages and PDH line systems. These are not shown explicitly because they do not contain clocks that are subject to this ITU-T Recommendation.



NOTE 1 – The maximum numbers of SSU and SEC clocks in these chains is defined in ITU-T Recommendation G.803.

NOTE 2 – PRC function is defined in ITU-T Recommendation G.811.

NOTE 3 – SSU function is defined in ITU-T Recommendation G.812 (Type I)

NOTE 4 – SEC function is defined in ITU-T Recommendation G.813 (Option 1)

Figure B.3/G.823 – Synchronization reference chain showing where the network limits apply

Figure B.3 shows that four types of synchronization interfaces can be distinguished in the synchronization network:

a) synchronization interfaces at PRC outputs;

b) synchronization interfaces at SSU outputs;

c) synchronization interfaces at SEC outputs; and

d) synchronization interfaces at PDH distribution outputs.

This ITU-T Recommendation therefore provides four sets of network limit requirements in 6.2, one for each type of interface.

B.2.1 Specification of wander by MTIE and TDEV parameters

The two timing parameters that have been selected to characterize transients and low frequency noise on a synchronization interface are MTIE (Maximum Time Interval Error) and TDEV (Time Deviation). Detailed definitions of MTIE and TDEV are provided in ITU-T Recommendation G.810.

MTIE is considered useful to capture the phase transients in a timing signal, since it describes the maximum phase variation of a timing signal over a period of time. However, MTIE is inadequate to show the underlying noise on the timing signal, because of its sensitivity to phase transients. Random noise is better characterized by TDEV which is an RMS power estimator instead of a peak estimator.

TDEV tends to remove transients in a timing signal, and is therefore a better estimator of the underlying noise processes. To be strictly correct, transients and periodic components should be removed from data prior to calculating TDEV. This is not appropriate however for measurements on network interfaces since there is no *a priori* knowledge of the types of disturbances experienced in the timing signal. This means that it cannot be guaranteed that the TDEV results from processing of raw phase data truly reflect the random noise processes in a timing signal on a network interface, but they can provide a good estimate (refer to B.3/G.810).

APPENDIX I

Wander limit considerations for SDH transport networks

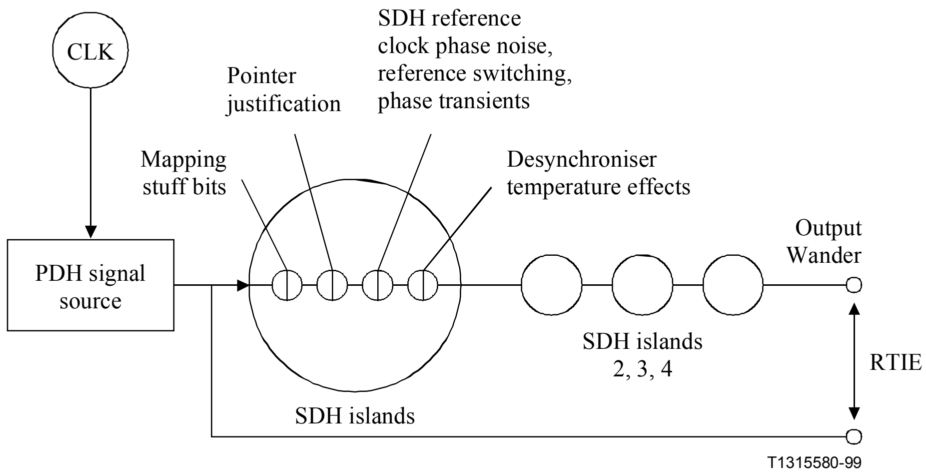
I.1 Introduction

The information in this appendix is provided to assist an understanding of the derivation of the network wander limits and input wander tolerances for traffic interfaces that are specified in this ITU-T Recommendation.

I.1.1 Wander reference model for SDH

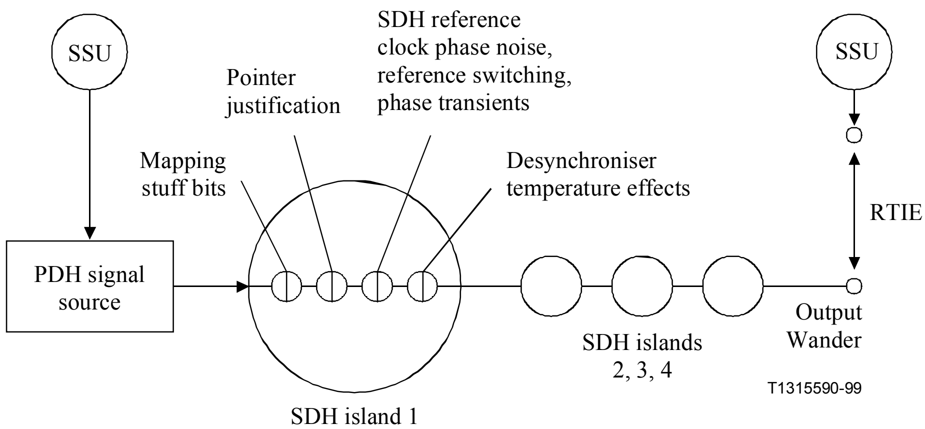
The wander reference models as shown in Figures I.1 and I.2 are simplified representations of the wander reference model described in Annex A. They also illustrate how the generic reference models of Annex B can accommodate network-specific sources of wander using the example of an SDH transport network.

Four cascaded SDH islands have been considered to be a reasonable modelling approach in previous jitter and wander accumulation computer simulation calculations. This approach is also adopted in this appendix. Figures I.1 and I.2 illustrate the principal sources of wander on network connections that have been considered when deriving the network limits and interface tolerances.



NOTE – CLK frequency offset conforms to bit-rate specifications of ITU-T Recommendation G.703.

Figure I.1/G.823 – Wander reference model for asynchronous PDH signals



NOTE 1 – SSU outputs conform to network wander limit of 6.2.2.
NOTE 2 – Both SSUs are traceable to a PRC.

Figure I.2/G.823 – Wander reference model for synchronous PDH signals

I.1.2 Sources of wander

The wander accumulated on payload signals when they are transported over a network connection employing SDH network elements depends on the total dynamic fill of all intermediate signal processing buffers in those network elements. The buffer fill of a single Network Element (NE) depends on the relative wander between the incoming data and the read clock. The read clock may be provided from an external source (e.g. in a pointer processor) or may be provided from a recovered clock (e.g. in a desynchronizer).

The buffer fill may be changed by reference clock phase noise and transient effects (e.g. bit-stuffing, pointer processing) and by temperature effects in phase-locked loops (e.g. desynchronizer clock recovery).

I.1.3 Wander accumulation limiting effects

At least when considering 2048 kbit/s connections, the total amount of these buffers in a single connection may exceed the 18 µs limit requested as a limit for the daily wander in this ITU-T Recommendation. But under normal operating conditions, these buffer fills remain almost constant due to a stable network synchronization performance. Furthermore, the fluctuating part of the buffer fills contributes only randomly to the accumulation because of a lack of correlating effects between different buffers.

I.1.4 Network configuration and performance

The SDH islands (refer to Figures I.1 and I.2) are normally internally-synchronized so that pointer justifications (at least at TU-12 level) are rare events. An exceptional case is when one or more of the NEs is operated using a clock source that is in holdover mode, so generating an approximately regular sequence of pointer justifications.

Under normal conditions, it is unlikely that two or more of these SDH islands are not internally-synchronized. It is also unlikely that a double pointer justification is generated in a single NE. Therefore it is improbable that the cumulative wander effect of more than two simultaneous pointer justifications will occur. Such rare cases may cause wander that will exceed the network limits specified in this ITU-T Recommendation.

In general, the performance of the SDH islands should be good enough so that the error and slip performance of the transported signal are not more than marginally affected by excessive phase noise effects that would cause buffer overflow in some NE.

I.1.5 Correlation of wander sources

The normal operating mode of the SDH network is the synchronous mode, which means that the rate of pointer justification is rather low. From this condition follows the conclusion that the occurrence of simultaneous, but independent, pointer justifications in cascaded SDH islands is unlikely. The following accumulation model accounts for this by using a statistical accumulation approach (i.e. a power-law accumulation).

In the case of wander generated by a single SDH island, a worst-case accumulation is assumed which simply totals all wander-generating effects within that island.

The correlation of bit-stuffing wander effects depends on the frequency offset of the PDH payload against that of the network clocks of the islands. This is an issue for synchronous 2048 kbit/s connections, as follows:

a) for frequency offsets below approx. 10^{-10} to 10^{-9} the network clock phase noise will randomize the bit-stuffing; and

b) for higher frequency offsets of the payload signal and with all SDH islands synchronized to nominal frequency, the bit-stuffing effects are correlated.

This is further considered in Annex A.

I.1.6 Network conditions for the output wander limits

The network conditions for the output wander limits specified in this ITU-T Recommendation are described in Annex A. It is intended that such networks will meet the specified limits when using any equipment conforming to G.783 specifications.

For more complex network connection configurations, the application of some method of wander reduction may be necessary in order to obtain the desired level of performance. For synchronous 2048 kbit/s connections, this may be performed by a re-timing function, for example. For other PDH connections an appropriate low-pass filtering function may be required.

I.2 Derivation of wander specification limits

For services which are provided by higher-order PDH connections, a short-term phase stability is required because these services normally use an adaptive synchronization to the received bit stream.

Short-term phase distortion is generated by the bit-stuffing techniques employed in asynchronous multiplex systems. This effect has first been studied for the PDH multiplex systems which use optimized stuff ratio values in order to minimize the effect. In SDH multiplex systems, the worst-case stuff ratio of zero-one is used, which generates short-term wander of an entire unit interval.

At the time of creation of this ITU-T Recommendation, SDH systems are widely deployed in the networks. This means that the network wander limit shall be met by the existing SDH networks.

Referring to Figures I.1 and I.2, PDH connections may pass through several SDH islands which are interconnected using PDH interfaces. In each of these SDH islands, phase distortion according to the bit- and byte-stuffing is created. For example, bit-stuffing is used when mapping the PDH payload to a VC-n payload and byte-stuffing (that is to say, pointer justification) is used when accommodation of the VC-n phase to the SDH frame is required.

In addition to the wander generated by the bit- and byte-stuffing techniques, the pointer processor hysteresis causes wander of the reference clock to be transferred to the PDH signal at the mapping or at the demapping node. The worst-case reference clock wander is caused by the reaction of the SDH Equipment Clock (SEC) function to a reference input switch event. The related phase transient has a maximum amplitude of 240 ns (refer to 10.1/G.813).

This leads to the following two scenarios using a 34 368 kbit/s signal as the example.

1) *Wander budget for 1 SDH island with phase transient at the demapping node*

The desynchronizer may use a digital PDH clock filtering circuit using the SEC output as a reference. This would cause the SEC output wander to be transferred to the recovered PDH clock.

Furthermore there may be a single pointer justification added to the phase offset just before the appearance of the SEC output transient.

The resulting wander budget is the following (values are rounded):

± stuffing:	60 ns
SEC phase transient:	240 ns
TU-3 pointer justification:	160 ns
Total:	460 ns

NOTE 1 – The stuffing effect at the mapping node takes into account the reference clock noise at that point and the phase transient represents the reference clock effect at the demapping node. The effect of the intermediate network is taken into account by one pointer justification.

2) *Wander budget for 1 SDH island with phase transient at the mapping node*

Any phase transient (i.e. transient frequency offset) of the reference clock (SEC output) at the mapping node causes a modification of the stuff-bit sequence which ultimately is compensated by the pointer justifications. Provided that not all the intermediate pointer processor buffers are at their threshold, no compensating pointer justifications are received at the desynchronizer node. Consequently, the PDH signal is recovered at an equivalent frequency offset of opposite polarity (this is known as the "phase ramp effect"). The 240 ns reference input switching phase transient at the mapping node consequently leads to a similar phase transient of the recovered PDH output.

The resulting wander budget is the following (values are rounded):

Mapping phase transient:	240 ns
Double pointer justification:	320 ns
Total:	560 ns

NOTE 2 – The effect of the reference clock wander at the mapping node is taken into account by the phase transient and the effects of the intermediate network together with the effect of the reference clock wander at the demapping node is accounted for by the double pointer.

I.2.1 Wander specification limits

The values in the above wander budgets for the mapping and demapping nodes are worst-case values. However, the impact of a phase transient on the output wander cannot be calculated by simply adding the values of both wander budgets because reference clock switching is a rare event and should be considered at only one end of the connection. It is therefore considered reasonable to use a value for output wander of a single SDH network island of the order of 500 ns.

When four SDH network islands of such intrinsic wander are cascaded using a statistical wander accumulation approach, the intrinsic wander is multiplied by a factor of the square root of the number of cascaded islands (in this case, a factor of two). The result is a total network output wander of 1 000 ns.

This applies similarly to the 139 264 kbit/s connections with the only difference that the stuffing effect is almost zero.

From this follows that for practical specification purposes, the maximum short-term output wander at higher-order PDH interfaces would be of the order of 1 000 ns which is consequently defined as the first plateau of the output wander specifications given in 5.2.

In order to derive the longer-term output wander specification, the effect of the reference clock phase noise has to be considered. This wander is bounded by a limit of 2 000 ns according to the synchronization network wander limit specification at long observation intervals. When the above analysis is done using the increased reference clock effect, the result is of the order of 4 000 ns which is the second plateau of the output wander specifications given in 5.2.

APPENDIX II

Measurement methodologies for output wander

Instrumentation in accordance with ITU-T Recommendation O.172 is appropriate for measurement of wander parameters.

II.1 Synchronization interfaces

II.1.1 Synchronous signals

When the signal is synchronous, and is used to carry synchronization, its wander is measured by comparing its phase with that of another PRC. The test configuration for measuring MTIE of a synchronous signal is shown in Figure II.1 (the standard estimator formula for calculating MTIE is given in Annex B/G.810).

The PRC used for the wander measurement need not be the same as that used to originate the synchronous signal, for most measurement applications. However, it should be noted that the worst-case frequency difference between two PRCs could give rise to a phase difference of the order of 2 µs per day.

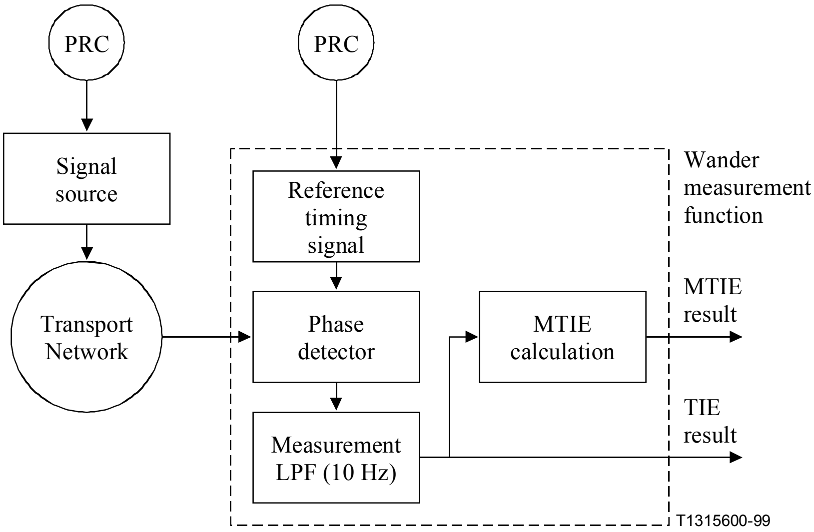


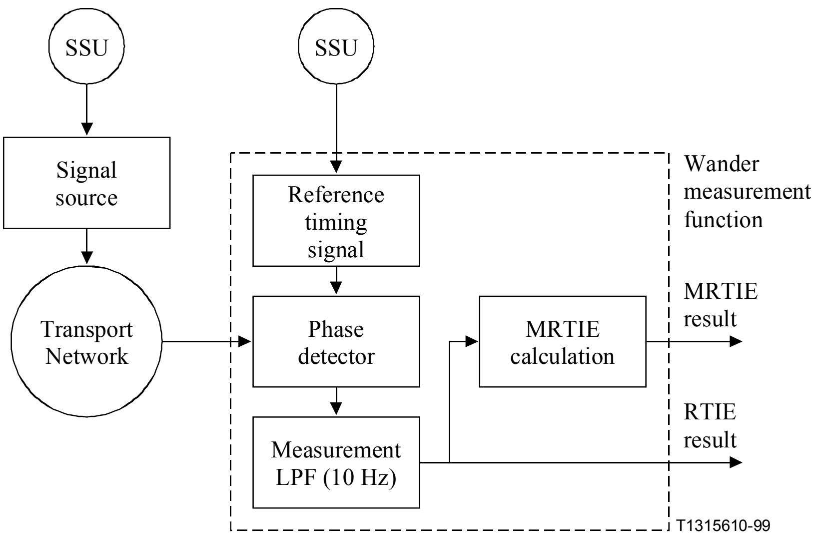
Figure II.1/G.823 – MTIE measurement of synchronous signals

II.2 Traffic interfaces

PDH signals, such as 2048, 34 368 and 139 264 kbit/s, can be either synchronous (i.e. normally PRC-traceable) or asynchronous (e.g. engineered to operate in a free-run mode with bounded frequency accuracy in accordance with ITU-T Recommendation G.703 but not traceable to a PRC). For both cases, MRTIE is used as the wander specification parameter at network interfaces.

II.2.1 Synchronous signals (PDH bit-rates)

Similar considerations apply as for synchronization interfaces. The measurement configuration is as shown in Figure II.2.



NOTE 1 – 1 SSU outputs conform to network wander limit of 6.2.2.
NOTE 2 – Both SSUs are traceable to a PRC.

Figure II.2/G.823 – MRTIE measurement of synchronous signals (PDH)

II.2.2 Asynchronous signals (PDH bit-rates)

In this case, a frequency difference can exist between the measurement reference frequency and the clock frequency originating the PDH signal, e.g. 50 ppm difference is allowed by G.703 at 2048 kbit/s. This difference causes a phase ramp in the measured wander, resulting in a distortion of the desired MRTIE parameter.

In order to support the wander reference model for PDH signals transported on SDH networks (described in Appendix I) and the corresponding output wander specifications given in 5.2, two situations are described further:

a) asynchronous signals, source reference clock available; and

b) asynchronous signals, source reference clock unavailable.

II.2.2.1 Asynchronous signals, source reference clock available

When the source reference clock is available at the measurement point, the MRTIE of an asynchronous signal may be readily measured as shown in Figure II.3. Note that the measurement point and the source reference should normally be colocated, in order to ensure that wander is not introduced into the measurement reference signals during transmission of the source reference clock.

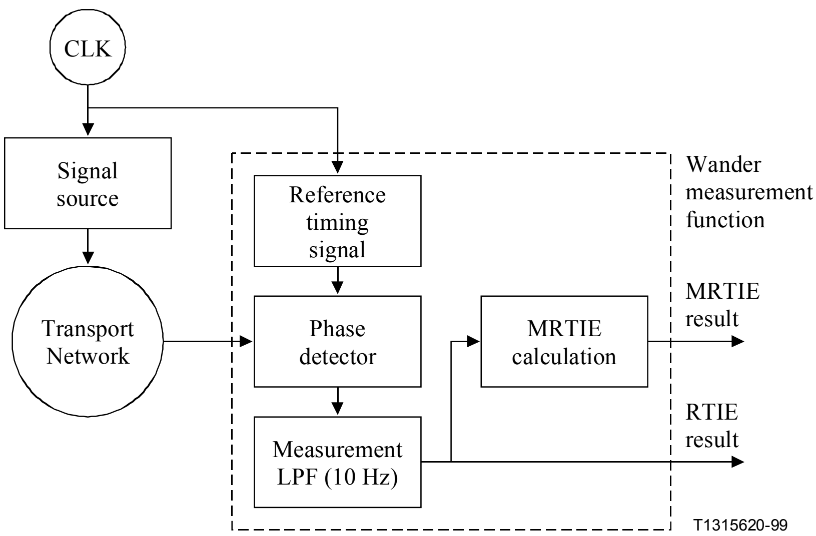


Figure II.3/G.823 – MRTIE measurement of asynchronous signals, source reference clock available

II.2.2.2 Asynchronous signals, source reference clock unavailable

When the source reference is not available at the measurement point, there will be a frequency difference between the source reference and the measurement reference, resulting in a ramp of phase in the wander measurement. This phase ramp must be removed before MRTIE is calculated, otherwise the phase ramp would obscure MRTIE information of interest at longer observation intervals.

One method of removing the phase ramp is shown in Figure II.4. This represents a "stop-start" method of measurement, where phase samples are acquired, stored and post-processed to obtain the MRTIE parameter.

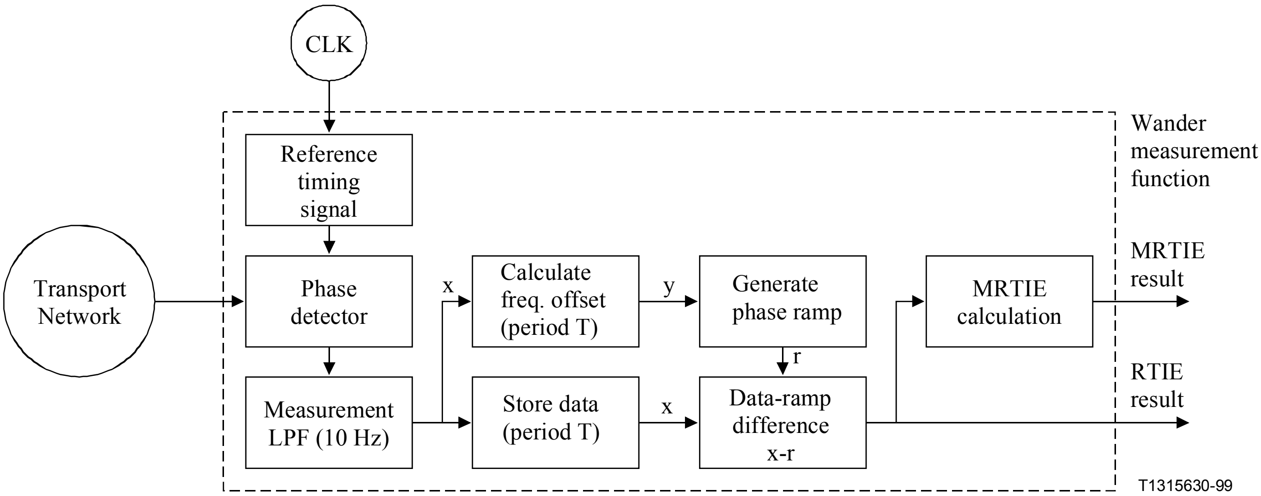


Figure II.4/G.823 – MRTIE measurement of asynchronous signals, source reference clock unavailable

In this method, the frequency difference y (in ppm) is estimated by the algorithm:

$$y = \frac{6}{N(N-1)\tau_0} \sum_{i=1}^{N} x_i \left[\frac{2i}{N+1} - 1 \right] \qquad \text{(II-1)}$$

where τ_0 is the sampling interval in seconds, N is the total number of phase samples in the measurement period and x_i is the TIE in µs.

In addition, the desired RTIE result is given by:

$$RTIE_n = x_n - y\tau_0 n \qquad \text{(II-2)}$$

The results of the measurement will depend on the measurement period $T = N\tau_0$ over which the frequency offset and MRTIE are calculated. The minimum measurement period T should be at least as long as the maximum observation interval of interest. For example, the 34 368 kbit/s output wander requirement of 5.2.2 has a specification extending up to an observation interval of 80 seconds.

NOTE – The signal source clock and the measurement reference clock should both have sufficient phase stability that the measurement result is only marginally affected by frequency drift effects, for example.

APPENDIX III

Measurement guidelines for input jitter and wander tolerance of equipment interfaces

A generic measurement setup for jitter and wander tolerance measurements is shown in Figure III.1. Note that not all elements are necessarily needed for every measurement of tolerance.

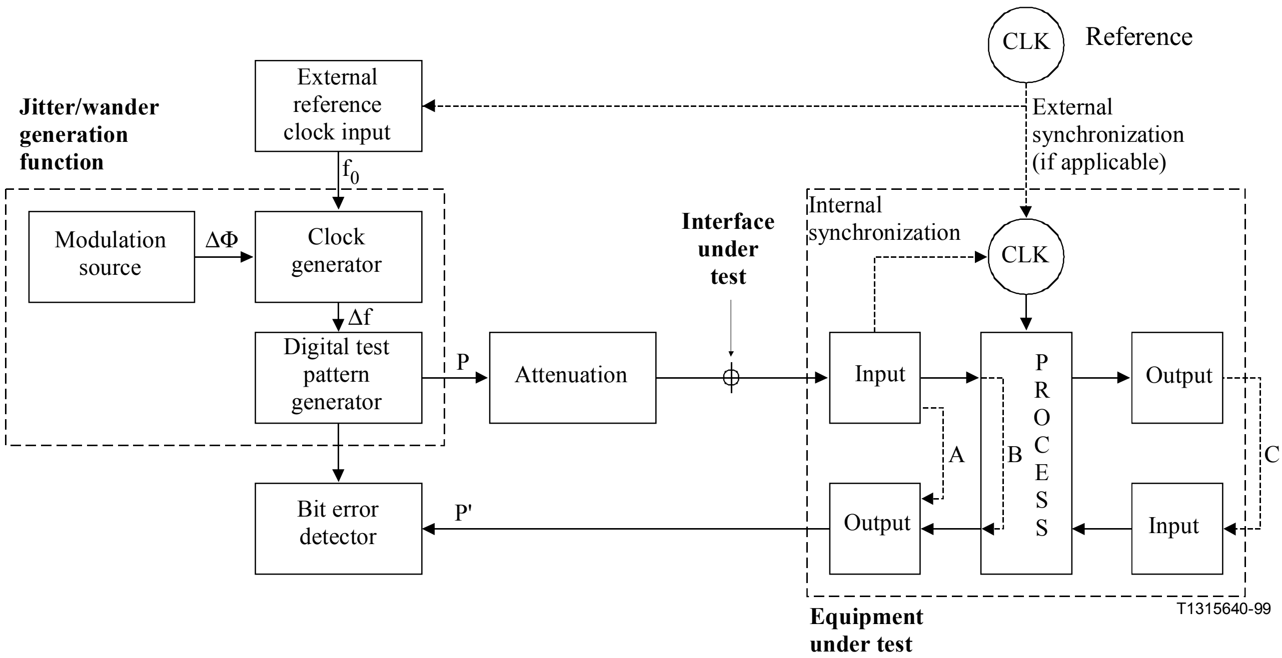


Figure III.1/G.823 – Generic measurement setup for input jitter and wander tolerance testing

The actual measurement setup is determined by the following considerations:

System clock

The equipment under test clock can be externally synchronized (if a reference input is available) or be synchronized from the interface under test.

Constraints on Δf

The clock generator can be used to generate a fixed frequency offset Δf upon which the jitter and wander is modulated. The frequency offset must be limited to the values applicable to the interface or equipment under test. The frequency offset should be held constant during a stabilization period and the subsequent measurement. The allowed frequency offset can be dependent on the path that the measurement signal takes through the system and the way that the equipment under test clock is synchronized.

Constraints on ΔΦ

The modulation source is used to superpose a jitter or wander effect ΔΦ on top of the clock signal, which can also have a fixed frequency offset Δf. These jitter and wander phase perturbations usually have a sinusoidal, triangular or noisy (PRBS-generated) characteristic. The exact perturbations are prescribed in the applicable jitter and wander tolerance requirements.

Choice of test-pattern (P and P')

The test-pattern P must match the bit rate of the particular interface that is being subjected to the jitter and wander tolerance test. Pattern P' is not necessarily the same as pattern P, but it is of importance that a part of pattern P is present in P'. This part, let us call it Q, is passed transparently through the equipment under test. The bit error detector can only search for errors in this common part Q.

Routing the signal through the equipment under test

Depending upon which parts of the system are actually to be tested and the capabilities of the equipment under test, the signal can be looped back in different configurations. For example:

a) directly behind the input (path A), to test the tolerance of the receiving circuitry;

b) in the routing functionality (path B), which could test, in addition, buffer hysteresis, stuffing mechanisms, etc.; or

c) externally through some other inputs and outputs of the system (path C).

The choice of the actual path can influence the selection of test-pattern P' and the part Q, over which errors can be monitored.

Attenuation

The attenuation function is needed for optical interfaces to be able to determine the 1 dB sensitivity penalty (in terms of optical power) at a certain bit-error ratio. For electrical interfaces the (frequency-dependent) attenuation should represent the worst-case cable length.

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