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Digital transmission systems – Digital networks – Design objectives for digital networks

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Timing characteristics of SDH equipment slave clocks (SEC)

ITU-T Recommendation G.813

(Previously CCITT Recommendation)

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ITU-T RECOMMENDATION G.813

TIMING CHARACTERISTICS OF SDH EQUIPMENT SLAVE CLOCKS (SEC)

Summary

This Recommendation outlines minimum requirements for timing devices used in synchronizing network equipment that operate according to the principles governed by the Synchronous Digital Hierarchy (SDH).

Source

ITU-T Recommendation G.813 was prepared by ITU-T Study Group 13 (1993-1996) and was approved under the WTSC Resolution No. 1 procedure on the 27th of August 1996.

Keywords

Clock Performance Objectives, Clock Performance Parameters, Jitter Performance, SDH Equipment Clock, Wander Performance.

FOREWORD

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The approval of Recommendations by the Members of the ITU-T is covered by the procedure laid down in WTSC Resolution No. 1 (Helsinki, March 1-12, 1993).

In some areas of information technology which fall within ITU-T's purview, the necessary standards are prepared on a collaborative basis with ISO and IEC.

NOTE

In this Recommendation, the expression "Administration" is used for conciseness to indicate both a telecommunication administration and a recognized operating agency.

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Recommendation G.813

TIMING CHARACTERISTICS OF SDH EQUIPMENT SLAVE CLOCKS (SEC)

(*Geneva, 1996*)

1 Scope

This Recommendation outlines requirements for timing devices used in synchronizing network equipment that operate according to the principles governed by the Synchronous Digital Hierarchy (SDH). These requirements apply under the normal environmental conditions specified for the SDH equipment. In normal operation SDH equipment contains a slave clock traceable to a primary reference clock. In general the SDH equipment clock (SEC) will have multiple reference inputs. In the event that all links between the master and the slave clock fail, the equipment should be capable of maintaining operation (holdover) within prescribed performance limits.

The SEC is part of the SDH equipment, the functions of which are specified in Recommendation G.783 as the Synchronous Equipment Timing Source (SETS). Slave clocks used in SDH equipment must meet specific requirements in order to comply with network jitter requirements for plesiochronous tributaries.

This Recommendation contains two options for the SEC. The first option, referred to as "Option 1," applies to SDH networks optimised for the 2048 kbit/s hierarchy. These networks allow the worst-case synchronization reference chain as specified in Figure 6-4/G.803. The second option, referred to as "Option 2," applies to SDH networks optimized for the particular 1544 kbit/s hierarchy that includes the rates 1544 kbit/s, 6312 kbit/s, and 44 736 kbit/s. The synchronization reference chain for these networks is under study.

An SDH equipment slave clock should comply with all of the requirements specific to one option and should not mix requirements between options 1 and 2. In the sections where one requirement is specified, the requirements are common to both options. It is the intention that options 1 and 2 should be harmonised in the future.

Careful consideration should be taken when interworking between networks with SECs based on option 1 and networks with SECs based on option 2.

This Recommendation defines the minimum requirements for clocks in SDH NEs. However, some SDH NEs may have a higher quality clock. This Recommendation allows for proper network operation when a SEC (Option 1 or 2) is timed from another SEC (like option), or a higher quality clock. Hierarchical timing distribution is recommended for SDH networks. Timing should not be passed from a SEC in free-run/holdover mode to a higher quality clock since the higher quality clock should not follow the SEC signal during fault conditions.

2 References

The following Recommendations and other references contain provisions which, through reference in this text, constitute provisions of this Recommendation. At the time of publication, the editions indicated were valid. All Recommendations and other references are subject to revision: all users of this Recommendation are therefore encouraged to investigate the possibility of applying the most recent edition of the Recommendations and other references listed below. A list of the currently valid ITU-T Recommendations is regularly published.

[1] CCITT Recommendation G.703 (1991), *Physical/electrical characteristics of hierarchical digital interfaces*.

[2] ITU-T Recommendation G.783 (1994), *Characteristics of Synchronous Digital Hierarchy (SDH) equipment functional blocks.*

[3] ITU-T Recommendation G.810 (1996), *Definitions and terminology for synchronization networks*.

[4] CCITT Recommendation G.811 (1988), *Timing requirements at the outputs of primary reference clocks suitable for plesiochronous operation of international digital links.*

[5] CCITT Recommendation G.812 (1988), *Timing requirements at the outputs of slave clocks suitable for plesiochronous operation of international digital links*.

[6] CCITT Recommendation G.822 (1988), *Controlled slip rate objectives on an international digital connection*.

[7] ITU-T Recommendation G.823 (1993), *The control of jitter and wander within digital networks which are based on the 2048 kbit/s hierarchy.*

[8] ITU-T Recommendation G.824 (1993), *The control of jitter and wander within digital networks which are based on the 1544 kbit/s hierarchy.*

[9] ITU-T Recommendation G.825 (1993), *The control of jitter and wander within digital networks which are based on the Synchronous Digital Hierarchy (SDH).*

3 Definitions

The terms and definitions used in this Recommendation are contained in Recommendation G.810.

4 Abbreviations

For the purposes of this Recommendation, the following abbreviations are used:

CMI Coded Mark Inversion

FPM Flicker Phase Modulation

MTIE Maximum Time Interval Error

NE Network Element

OAM Operation And Maintenance

PLL Phase Locked Loop

PRC Primary Reference Clock

SDH Synchronous Digital Hierarchy

SEC SDH Equipment Clock

SSMB Synchronization Status Message Byte

STM Synchronous Transport Module

TDEV Time Deviation

UI Unit Interval

UTC Coordinated Universal Time

WFM White Frequency Modulation

5 Frequency accuracy

a) *Option 1*

Under free-running conditions, the SEC output frequency accuracy should not be greater than 4.6 ppm with regard to a reference traceable to a G.811 clock.

NOTE – The time interval for this accuracy is for further study. Values of 1 month and 1 year have been proposed.

b) *Option 2*

Under free-running conditions, the SEC output frequency accuracy should not be greater than 20 ppm. Note that payload performance is not guaranteed for a fractional frequency deviation with a magnitude greater than 4.6 ppm. However, Operations and Maintenance (OAM) functionality shall be supported when a SEC is performing at the minimum accuracy.

6 Pull-in, hold-in, and pull-out ranges

6.1 Pull-in range

a) *Option 1*

The minimum pull-in range should be ±4.6 ppm, whatever the internal oscillator frequency offset may be.

b) *Option 2*

The minimum pull-in range shall be ±20 ppm, whatever the internal oscillator frequency offset may be.

6.2 Hold-in range

a) *Option 1*

The hold-in range for Option 1 is not required.

b) *Option 2*

The minimum hold-in range shall be ±20 ppm, whatever the internal oscillator frequency offset may be.

6.3 Pull-out range

a) *Option 1*

The pull-out range is for further study. A minimum value of ±4.6 ppm has been proposed.

b) *Option 2*

The pull-out range is not specified.

7 Noise generation

The noise generation of a SEC represents the amount of phase noise produced at the output when there is an ideal input reference signal or the clock is in holdover state. A suitable reference, for practical testing purposes, implies a performance level at least 10 times more stable than the output requirements. The ability of the clock to limit this noise is described by its frequency stability. The measures MTIE and Time Deviation (TDEV) are useful for characterisation of noise generation performance.

MTIE and TDEV are measured through an equivalent 10 Hz, first-order, low-pass measurement filter, at a maximum sampling time τ_0 of 1/30 seconds. The minimum measurement period for TDEV is twelve times the integration period ($T = 12\tau$).

7.1 Wander in locked mode

a) *Option 1*

When the SEC is in the locked mode of operation, the MTIE measured using the synchronized clock configuration defined in Figure 1a/G.810 should have the limits in Table 1, if the temperature is constant (within ±1 °K):

TABLE 1/G.813

Wander generation (MTIE) for option 1 with constant temperature

MTIE limit	Observation interval τ
40 ns	$0.1 < \tau \leq 1$ s
$40\tau^{0.1}$ ns	$1 < \tau \leq 100$ s
$25.25\tau^{0.2}$ ns	$100 < \tau \leq 1000$ s

The resultant requirement is shown by the thick solid line in Figure 1.

When temperature effects are included, the allowance for the total MTIE contribution of a single SEC increases by the values in Table 2.

TABLE 2/G.813

Additional wander generation (MTIE) for option 1 with temperature effects

Additional MTIE allowance	Observation interval τ
0.5τ ns	$\tau \leq 100$ s
50 ns	$\tau > 100$ s

The resultant requirements are shown by the thin solid line in Figure 1.

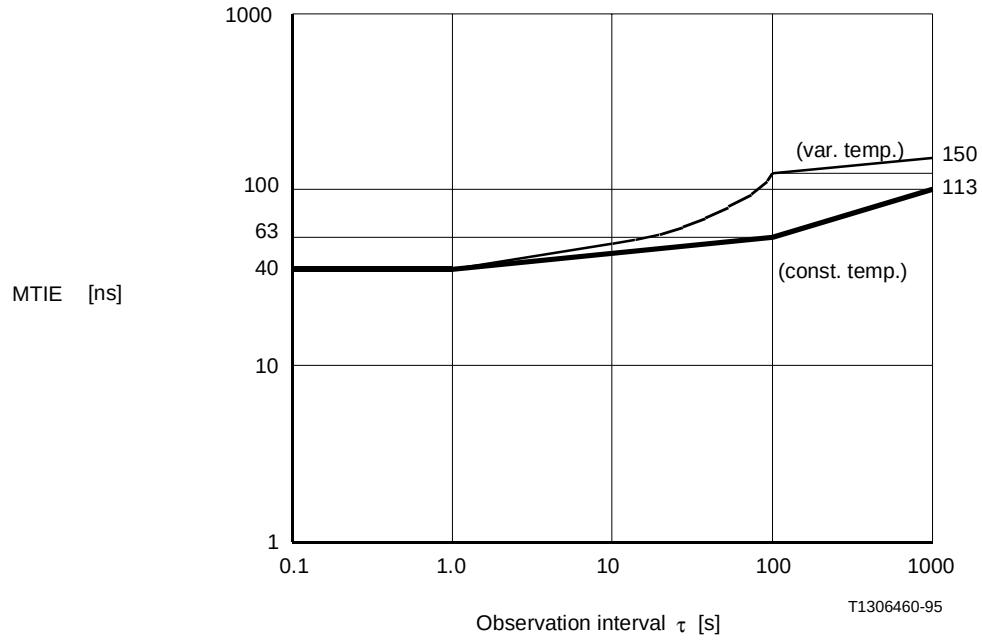

FIGURE 1/G.813

Wander generation (MTIE) for option 1

When the SEC is in the locked mode of operation, the TDEV measured using the synchronized clock configuration defined in Figure 1a/G.810 should have the limits in Table 3, if the temperature is constant (within ±1 °K):

TABLE 3/G.813

Wander generation (TDEV) for option 1 with constant temperature

TDEV limit	Observation interval τ
3.2 ns	$0.1 < \tau \leq 25$ s
$0.64\tau^{0.5}$ ns	$25 < \tau \leq 100$ s
6.4 ns	$100 < \tau \leq 1000$ s

The resultant requirements are shown in Figure 2.

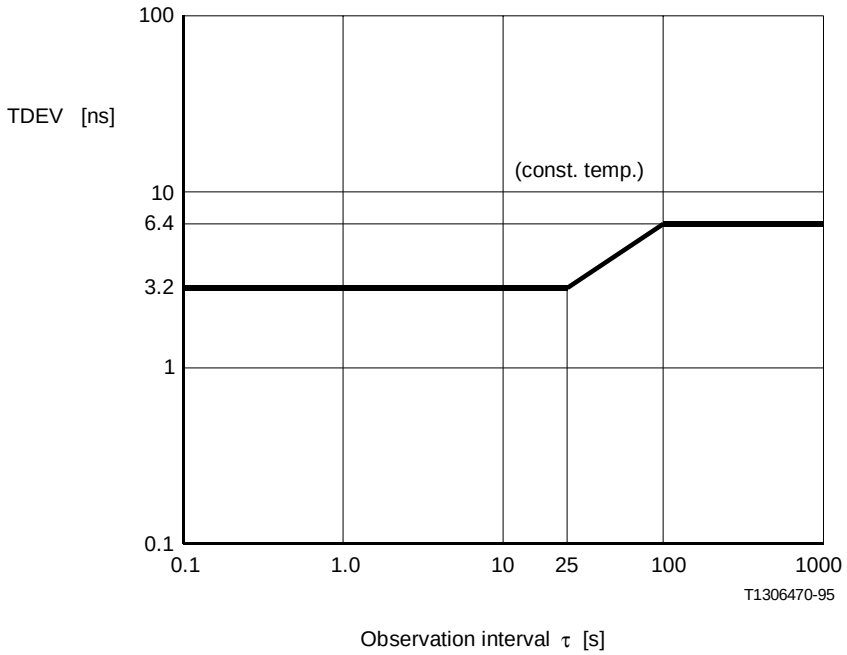

FIGURE 2/G.813

Wander generation (TDEV) for option 1 with constant temperature

b) *Option 2*

When the SEC clock is in the locked mode of operation synchronized to a wander free reference, the MTIE and TDEV measured at the output under constant temperature (within ±1 °K) shall be below the limits in Tables 4 and 5.

TABLE 4/G.813

Wander generation (MTIE) for option 2 with constant temperature

MTIE limit	Observation interval τ
20 ns	$0.1 < \tau \leq 1$ s
$20\tau^{0.48}$ ns	$1 < \tau \leq 10$ s
60 ns	$10 < \tau \leq 1000$ s

TABLE 5/G.813

Wander generation (TDEV) for option 2 with constant temperature

TDEV limit	Observation interval τ
$3.2\tau^{-0.5}$ ns	$0.1 < \tau \leq 2.5$ s
2 ns	$2.5 < \tau \leq 40$ s
$0.32\tau^{0.5}$ ns	$40 < \tau \leq 1000$ s
10 ns	$1000 < \tau \leq 10\,000$ s

The resultant requirements are shown in Figures 3 and Figure 4.

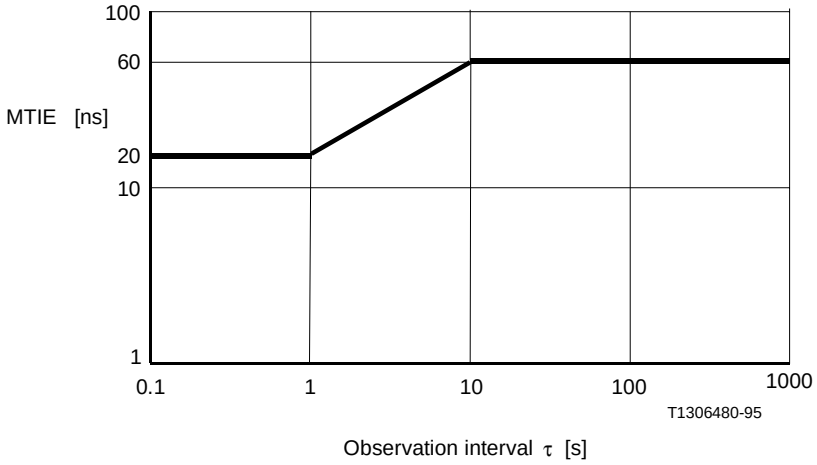

FIGURE 3/G.813

Wander generation (MTIE) for option 2 with constant temperature

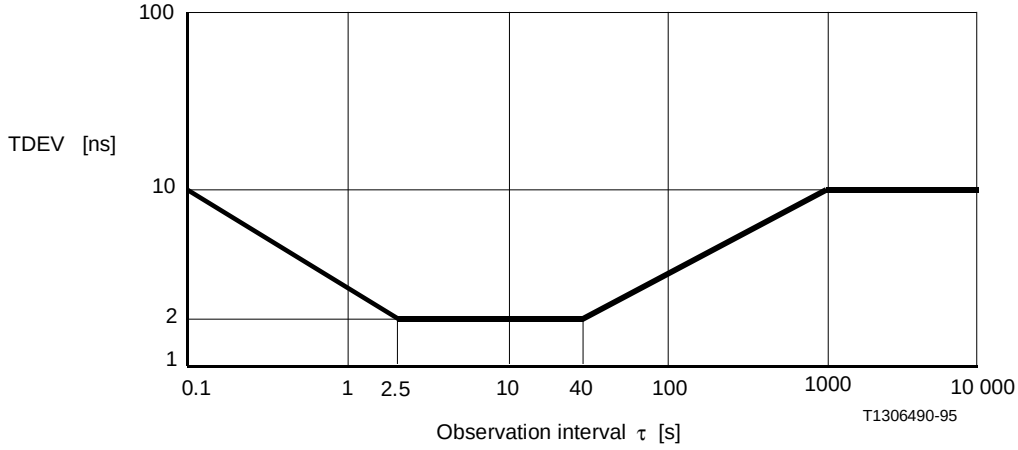

FIGURE 4/G.813

Wander generation (TDEV) for option 2

7.2 Non-locked Wander

When a clock is not locked to a synchronization reference, the random noise components are negligible compared to deterministic effects like initial frequency offset. Consequently the non-locked wander effects are included in 10.2.

7.3 Jitter

While most requirements in this Recommendation are independent of the output interface at which they are measured, this is not the case for jitter production; jitter generation requirements utilize

existing Recommendations that have different limits for different interface rates. These requirements are stated separately for the interfaces identified in clause 11. To be consistent with other jitter requirements the values are in UIpp, where the UI corresponds to the reciprocal of the bit rate of the interface.

Note that in general all filter values specified in this generation section for STM-N interfaces have been harmonised with the filter values for the network limit as specified in Recommendation G.825, except for the 12 kHz high pass filter used in option 2 which is specified in Recommendation G.783. An attempt to further harmonise the filter bandwidth specifications will be made in the future.

NOTE – Due to the stochastic nature of jitter, the peak-to-peak values given in this subclause eventually are exceeded. The requirements should therefore be fulfilled in at least 99% of all measurements made.

a) *Option 1*

Output Jitter at a 2048 kHz interface

In the absence of input jitter, the intrinsic jitter at a 2048 kHz output interface, as measured over a 60-second interval, should not exceed 0.05 UI peak-peak when measured through a single pole band-pass filter with corner frequencies at 20 Hz and 100 kHz.

Output Jitter at an STM-N interface

In the absence of input jitter at the synchronization interface, the intrinsic jitter at optical STM-N output interfaces, as measured over a 60-second interval, should not exceed the limits given in Table 6. The allowed jitter on an STM-1 electrical (CMI) interface is for further study.

TABLE 6/G.813

STM-N jitter generation for option 1

Interface	Measuring filter	Peak-to-peak amplitude
STM-1	500 Hz to 1.3 MHz	0.50 UI
	65 kHz to 1.3 MHz	0.10 UI
STM-4	1000 Hz to 5 MHz	0.50 UI
	250 kHz to 5 MHz	0.10 UI
STM-16	5000 Hz to 20 MHz	0.50 UI
	1 MHz to 20 MHz	0.10 UI
For STM-1 1 UI = 6.43 ns For STM-4 1 UI = 1.61 ns For STM-16 1 UI = 0.40 ns		

b) *Option 2*

In the absence of input jitter at the synchronization interface, the intrinsic jitter at optical STM-N output interfaces shall be less than 0.10 UIpp measured with a bandpass filter as stated in Table 7.

TABLE 7/G.813

STM-N jitter generation for option 2

Interface	Measuring filter
STM-1	12 kHz to 1.3 MHz
STM-4	12 kHz to 5 MHz
STM-16	12 kHz to 20 MHz

8 Noise Tolerance

The noise tolerance of a SEC indicates the minimum phase noise level at the input of the clock that should be accommodated whilst:

– Maintaining the clock within prescribed performance limits The exact performance limits are for further study.

– Not causing any alarms.

– Not causing the clock to switch reference.

– Not causing the clock to go into holdover.

In general, the noise tolerance of the SEC is the same as the network limit for the synchronization interface in order to maintain acceptable performance. However, the synchronization interface network limit may be different according to the application. Therefore in order to determine the SEC noise tolerance, the worst case network limit should be used. An explanation of the different network limits for acceptable payload performance is given in Appendix I for information.

The wander and jitter tolerances given in 8.1 and 8.2 represent the worst levels that a synchronization carrying interface should exhibit. The TDEV signal used for a conformance test should be generated by adding white, gaussian noise sources, of which each has been filtered to obtain the proper type of noise process with the proper amplitude.

MTIE and TDEV are measured through an equivalent 10 Hz, first-order, low-pass measurement filter, at a maximum sampling time τ_0 of 1/30 seconds. The minimum measurement period for TDEV is twelve times the integration period ($T = 12\tau$).

8.1 Wander Tolerance

a) *Option 1*

The SEC input wander tolerance expressed in MTIE and TDEV limits is given in Tables 8 and 9.

TABLE 8/G.813

Input wander tolerance (MTIE) for option 1

MTIE limit	Observation interval τ
0.25 μs	$0.1 < \tau \leq 2.5$ s
0.1τ μs	$2.5 < \tau \leq 20$ s
2 μs	$20 < \tau \leq 400$ s
0.005τ μs	$400 < \tau \leq 1000$ s

TABLE 9/G.813

Input wander tolerance (TDEV) for option 1

TDEV limit	Observation interval τ
12 ns	$0.1 < \tau \leq 7$ s
1.7τ ns	$7 < \tau \leq 100$ s
170 ns	$100 < \tau \leq 1000$ s

The resultant requirements are shown in Figures 5 and 6.

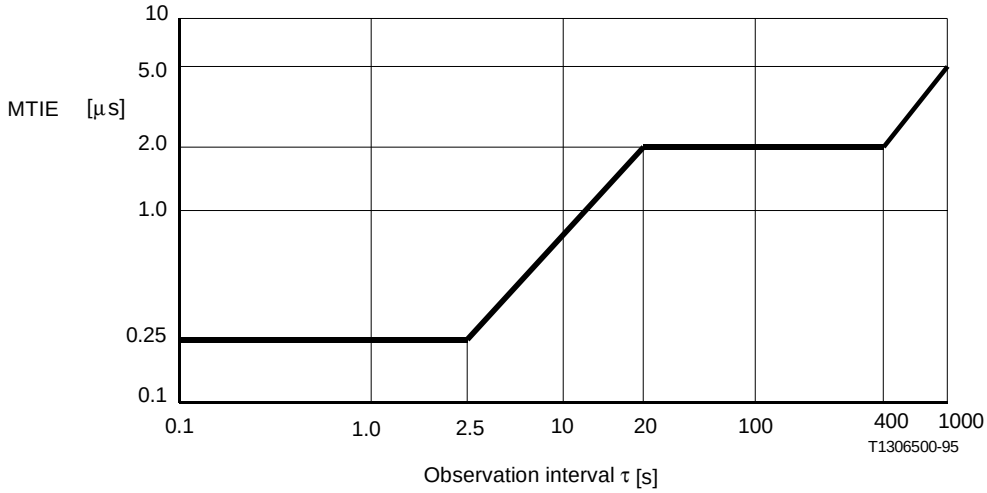

FIGURE 5/G.813

Input wander tolerance (MTIE) for option 1

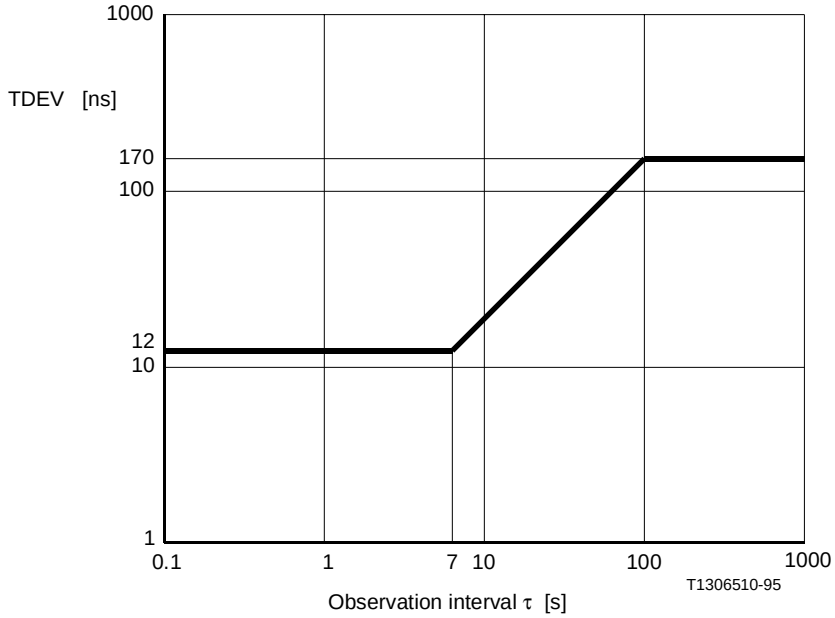

FIGURE 6/G.813

Input wander tolerance (TDEV) for option 1

While suitable test signals that check conformance to the mask in Figure 6 are being studied, test signals with a sinusoidal phase variation can be used, according to the levels in Table 10.

TABLE 10/G.813

Lower limit of maximum tolerable sinusoidal input wander for option 1

Peak-to-peak wander amplitude		Wander frequency				
A_1(μs)	A_2(μs)	f_4 (MHz)	f_3 (MHz)	f_2 (MHz)	f_1 (Hz)	f_0 (Hz)
0.25	2	0.32	0.8	16	0.13	10

The resultant requirements are shown in Figure 7.

FIGURE 7/G.813

Lower limit of maximum tolerable sinusoidal input wander for option 1

b) *Option 2*

The SEC input wander tolerance expressed in TDEV is specified in Table 11.

TABLE 11/G.813

Input wander tolerance (TDEV) for option 2

TDEV limit	Observation interval τ
17 ns	$0.1 < \tau \leq 3$ s
5.77τ ns	$3 < \tau \leq 30$ s
$31.6325\tau^{0.5}$ ns	$30 < \tau \leq 1000$ s

The resultant requirement is shown in Figure 8. A requirement expressed in MTIE is not defined.

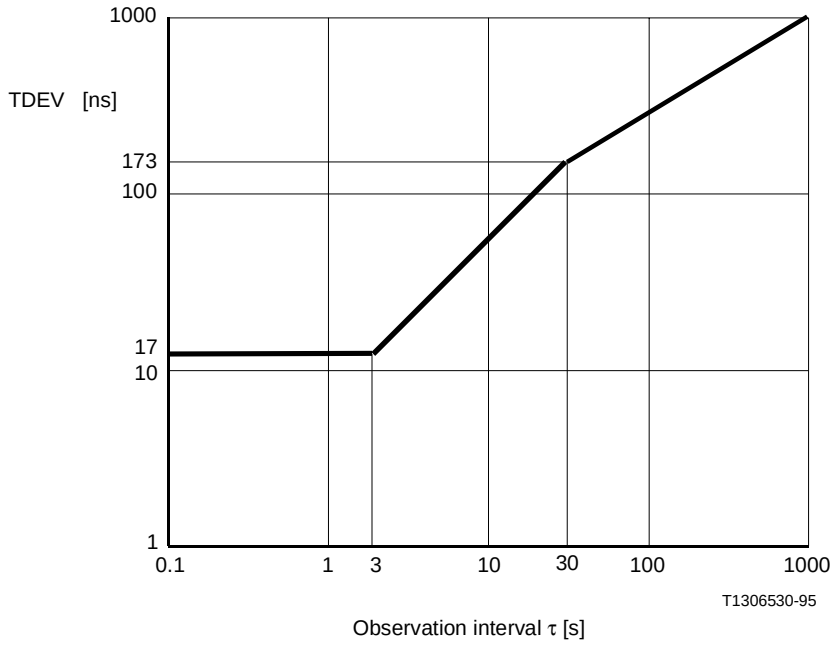

FIGURE 8/G.813

Input wander tolerance (TDEV) for option 2

8.2 Jitter Tolerance

a) *Option 1*

The lower limit of maximum tolerable input jitter for 2048 kHz and 2048 kbit/s signals carrying synchronization to a SEC is given in Figure 9.

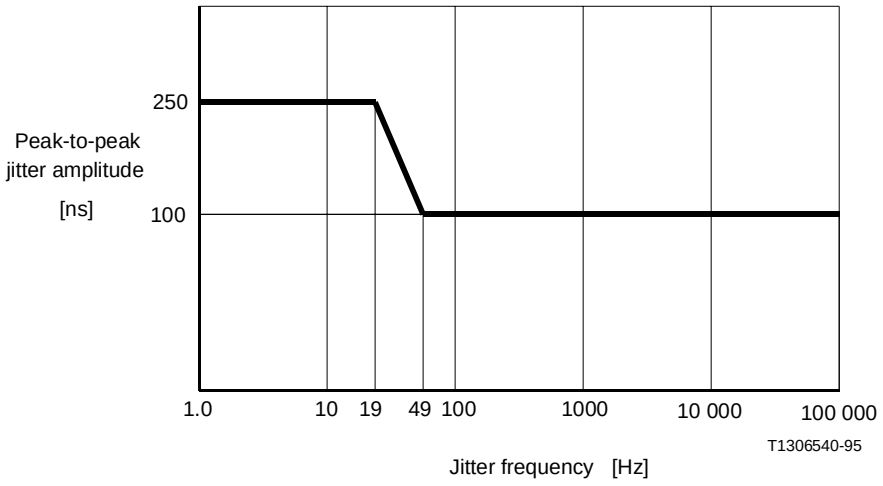

FIGURE 9/G.813

Lower limit of maximum tolerable input jitter

b) *Option 2*

The lower limit of maximum tolerable jitter for STM-N signals carrying synchronization to a SEC is given in Figure 10 and Table 12. For option 2 networks, the normal practice is to select synchronization reference links that operate well within the network limit; therefore, the plateau at A_3 and the frequencies f_1 and f_2 in Figure 10 and Table 12 are inconsistent with the network limit in Recommendation G.825. This results in an option 2 clock having reduced tolerance to jitter than is specified for the network limit defined in Recommendation G.825. An attempt to harmonise these STM-N jitter tolerance levels will be made in the future.

Jitter tolerance for external 1544 kbit/s synchronization references is to be determined.

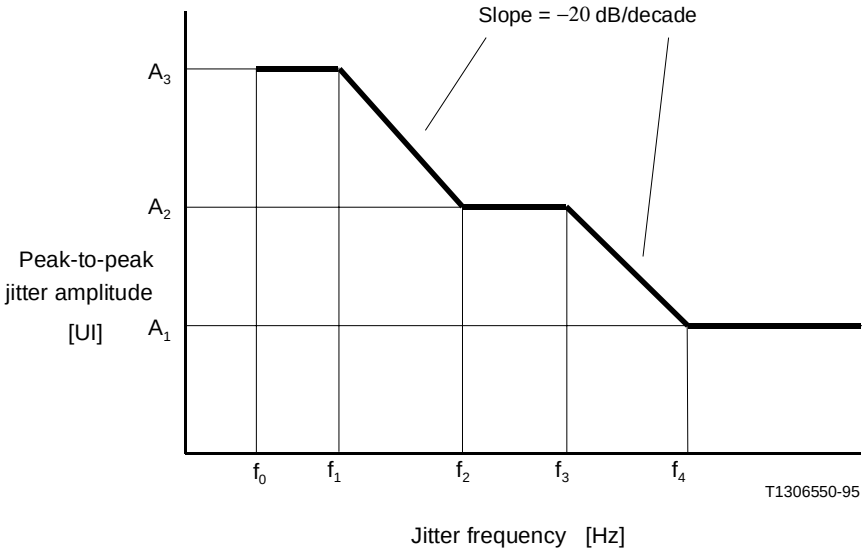

FIGURE 10/G.813

G.813 jitter tolerance for option 2

TABLE 12/G.813

G.813 jitter tolerance for option 2

STM-N level	f_0 (Hz)	f_1 (Hz)	f_2 (Hz)	f_3 (Hz)	f_4 (Hz)	A_1 (UI_{pp})	A_2 (UI_{pp})	A_3 (UI_{pp})
1	10	30	300	6.5k	65k	0.15	1.5	15
4	10	30	300	25k	250k	0.15	1.5	15
16	10	600	6000	100k	1000k	0.15	1.5	15

9 Noise transfer

The transfer characteristic of the SEC determines its properties with regard to the transfer of excursions of the input phase relative to the carrier phase. The SEC can be viewed as a low-pass filter for the differences between the actual input phase and the ideal input phase of the reference. The minimum and maximum allowed bandwidths for this low-pass filter behaviour are based on the considerations described in Appendix II and are indicated below.

In the pass band the phase gain of the SEC should be smaller than 0.2 dB (2.3%). The above applies to a linear SEC model. However, this model should not restrict implementation.

a) *Option 1*

The minimum bandwidth requirement for a SEC is 1 Hz. The maximum bandwidth requirement for a SEC is 10 Hz.

b) *Option 2*

The SDH NE, when referenced to a STM-N timing signal that meets the input TDEV mask in Figure 8 and Table 11, shall output signals that meet the output TDEV limits in Table 13.

TABLE 13/G.813

Wander transfer for option 2 (maximum output wander when input wander meets Table 11/G.813)

TDEV limit	Observation interval τ
10 ns	$0.1 < \tau \leq 1.7$ s
5.77τ ns	$1.7 < \tau \leq 30$ s
$31.63\tau^{0.5}$ ns	$30 < \tau \leq 1000$ s

TDEV is measured through an equivalent 10 Hz, first-order, low-pass measurement filter at a maximum sampling time τ_0 of 1/30 seconds. The minimum measurement period for TDEV is twelve times the integration period ($T = 12\tau$).

The resultant requirement is shown in the mask of Figure 11. The purpose of these masks is to ensure that the maximum bandwidth of a SEC is 0.1 Hz. These masks should not to be used to verify phase gain peaking. There is no requirement for a minimum bandwidth.

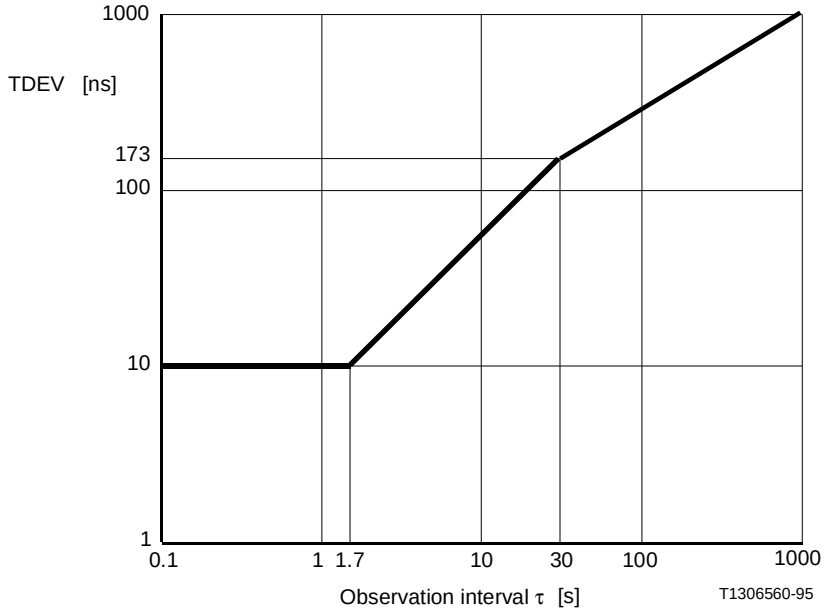

FIGURE 11/G.813

Wander transfer for option 2 (maximum output wander when input wander meets Figure 8/G.813)

10 Transient response and holdover performance

The requirements in this clause apply to situations where the input signal is affected by disturbances or transmission failures (e.g. short interruptions, switching between different synchronization signals, loss of reference, etc.) that result in phase transients at the SEC output (see clause 11). The ability to withstand disturbances is necessary to avoid transmission defects or failures. Transmission failures and disturbances are common stress conditions in the transmission environment.

Measurements of MTIE for Option 2 clocks are measured through an equivalent 100 Hz, first-order, low-pass measurement filter.

To ensure transmission integrity, it is recommended that all the phase movements at the output of the SEC stay within the level described in the following subclauses.

10.1 Short-term phase transient response

a) *Option 1*

This requirement reflects the performance of the clock in cases when the (selected) input reference is lost due to a failure in the reference path and a second reference input signal, traceable to the same reference clock, is available simultaneously or shortly after the detection of the failure (e.g. in cases of autonomous restoration). In such cases the reference is lost for at most 15 s. The output phase variation, relative to the input reference before it was lost, is bounded by the following requirements:

The phase error should not exceed $\Delta t + 5 \times 10^{-8}.S$ seconds over any period S up to 15 seconds. Δt represents two phase jumps that may occur during the transition into and out of the holdover state which both should not exceed 120 ns with a temporary frequency offset of no more than 7.5 ppm.

The resultant overall requirement is summarized in Figure 12. This Figure is intended to depict the worst case phase movement attributable to an SEC reference clock switch. Clocks may change state more quickly than is shown here. Background information on the requirements that drove this requirement are provided in Appendix II.

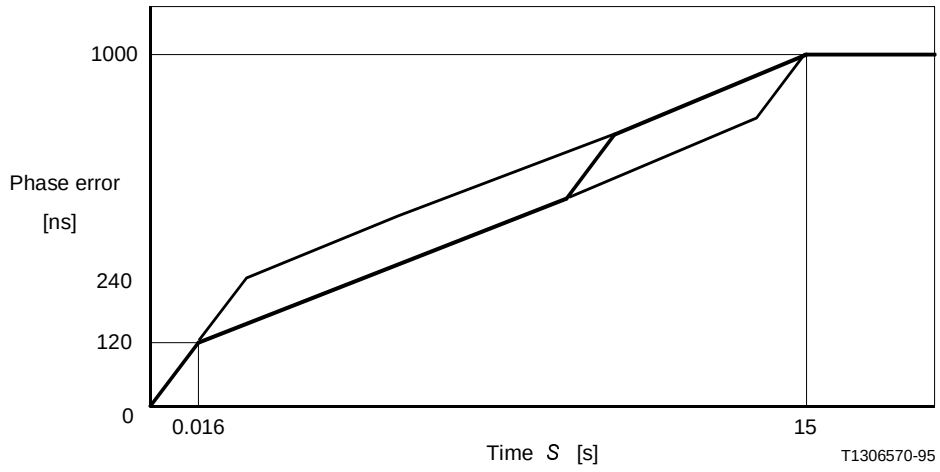

FIGURE 12/G.813

Maximum phase transient at the output due to reference switching for Option 1

Figure 12 shows two-phase jumps in the clock switching transient. The first jump reflects the initial response to a loss of the synchronization reference source and subsequent entry into hold-over. The magnitude of this jump corresponds to a frequency offset less than 7.5 ppm for a duration less than 16 ms. After 16 ms, the phase movement is restricted to lie underneath the line with a slope of 5×10^{-8} in order to constrain pointer activity. The second jump, which is to take place within 15 s after entering holdover, accounts for the switching to the secondary reference. The same requirements are applicable for this jump. After the second jump the phase error should remain constant and smaller than 1 μs

NOTE – The output phase excursion, when switching between references which are not traceable to the same PRC, is for further study.

In cases where the input synchronization signal is lost for more than 15 s, the requirements in 10.2 apply.

b) *Option 2*

During clock rearrangement operations (e.g. reference switching), the output of the clock should meet the MTIE requirement in Table 14.

TABLE 14/G.813

MTIE at the output due to reference switching for option 2

MTIE limit	Observation interval τ
Not specified	$\tau \leq 0.014$ s
(7.6+885τ) ns	0.014 s< $\tau \leq 0.5$ s
(300+300τ) ns	0.5 s < $\tau \leq 2.33$ s
1000 ns	2.33 s< τ

This MTIE requirement is illustrated in Figure 13.

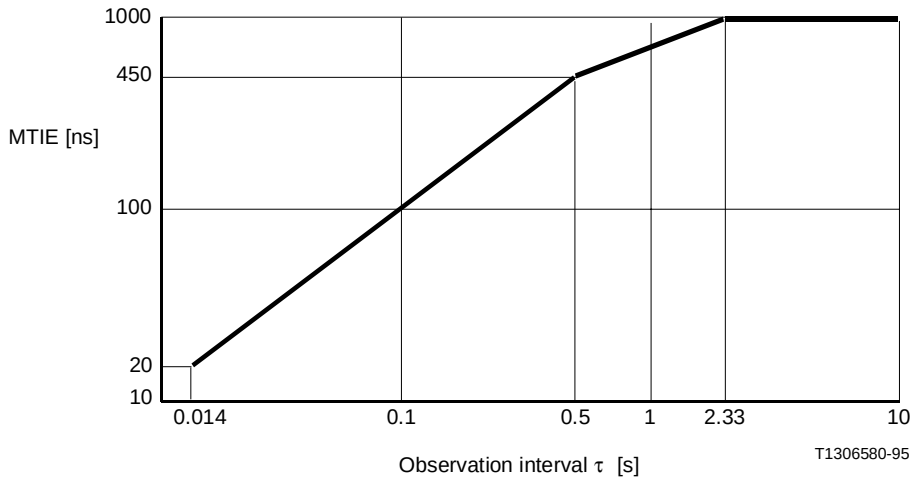

FIGURE 13/G.813

MTIE at the output due to reference switching for option 2

10.2 Long-term phase transient response (Holdover)

This requirement bounds the maximum excursions in the output timing signal. Additionally, it restricts the accumulation of the phase movement during input signal impairments or internal disturbances.

a) *Option 1*

When a SEC loses its reference, it is said to enter the holdover state. The Phase Error, ΔT, at the output of the SEC relative to the input at the moment of loss of reference should not, over any period of $S > 15$ s, exceed the following limit:

$$\Delta T(S) = \{(a_1 + a_2)\, S + 0.5\, b\, S^2 + c\} \quad [\text{ns}]$$

where:

a_1 = 50 ns/s (see Note 1);

a_2 = 2000 ns/s (see Note 2);

b = 1.16×10^{-4} ns/s^2 (see Note 3);

c = 120 ns (see Note 4).

This limit is subject to a maximum frequency offset of ± 4.6 ppm. The behaviour for $S < 15$s is defined in 10.1.

NOTES

1 The frequency offset a_1 represents an initial frequency offset corresponding to 5×10^{-8} (0.05 ppm).

2 The frequency offset a_2 accounts for temperature variations after the clock went into holdover and corresponds to 2×10^{-6} (2 ppm). If there are no temperature variations, the term $a_2 S$ should not contribute to the phase error.

3 The drift b is caused by ageing: 1.16×10^{-4} ns/s^2 corresponds to a frequency drift of 1×10^{-8}/day (0.01 ppm/day). This value is derived from typical ageing characteristics after 10 days of continuous operation. It is not intended to measure this value on a per day basis as the temperature effect will dominate.

4 The phase offset c takes care of any additional phase shift that may arise during the transition at the entry of the holdover state.

The resultant overall requirement for constant temperature (i.e. when the temperature effect is negligible) is summarized in Figure 14.

$$\Delta T(S) = \left(a_1 S + \frac{b}{2} S^2 + c \right) \quad [\text{ns}]$$

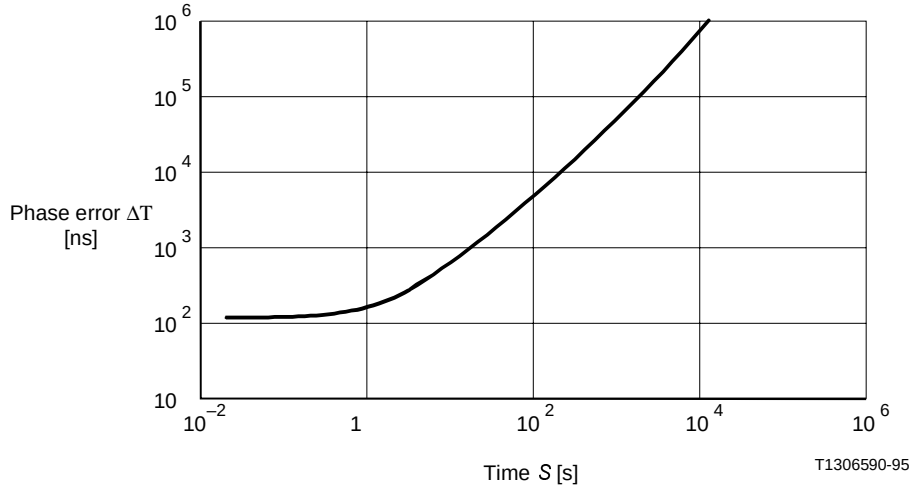

FIGURE 14/G.813

Permissible phase error for a SEC under holdover operation at constant temperature

b) *Option 2*

During entry into holdover a phase transient may be generated. It is expected that any such transient would occur within the first 64 seconds of holdover. Any transient associated with entry into holdover shall have an MTIE (relative to the input at the moment of reference loss) not greater than Table 15.

TABLE 15/G.813

MTIE during entry into holdover for option 2

MTIE limit	Observation interval τ
Not specified	$\tau < 0.014$ s
$(7.6+885\tau)$ ns	$0.014 \text{ s} \leq \tau < 0.5$ s
$(300+300\tau)$ ns	$0.5 \text{ s} \leq \tau < 2.33$ s
$(884+50\tau)$ ns	$2.33 \text{ s} \leq \tau < 64$ s
Not specified	$64 \text{ s} \leq \tau$

This MTIE requirement is illustrated in Figure 15.

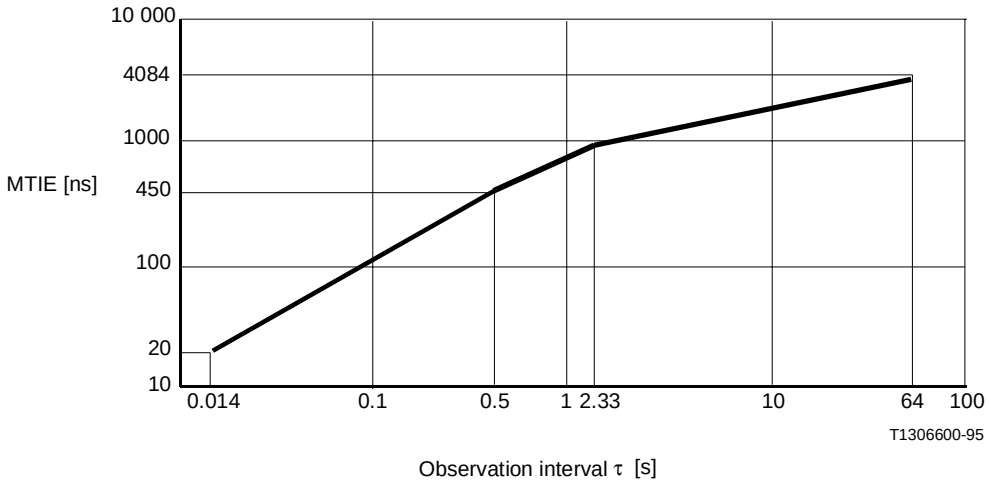

FIGURE 15/G.813

MTIE during entry into holdover for option 2

The initial fractional frequency offset observed in the first minute after 64 seconds shall be less than 0.05 ppm.

Any drift in frequency shall be less than 5.8×10^{-6} ppm/sec. Drift is defined as the change in fractional frequency offset per unit of time. These specifications apply at constant temperature.

10.3 Phase response to input signal interruptions

a) *Option 1*

For short-term interruptions on synchronization input signals, that do not cause reference switching, the output phase variation should not exceed 120 ns, with a maximum frequency offset of 7.5 ppm for a maximum period of 16 ms.

b) *Option 2*

This is for further study.

10.4 Phase discontinuity

a) *Option 1*

In cases of infrequent internal testing or other internal disturbances (but excluding major hardware failures, e.g. those that would give rise to clock equipment protection switches) within the SDH equipment clock, the following conditions should be met:

- the phase variation over any period *S* up to 16 ms should not exceed 7.5*S* ns
- the phase variation over any period *S* from 16 ms up to 2.4 s should not exceed 120 ns
- for periods greater than 2.4 s, the phase variation for each interval of 2.4 s should not exceed 120 ns with a temporary offset of no more than 7.5 ppm up to a total amount of 1μs.

b) *Option 2*

This is for further study.

11 Interfaces

The requirements in this Recommendation are related to reference points internal to the Network Elements (NEs) in which the clock is embedded and are therefore not necessarily available for measurement or analysis by the user. Therefore the performance of the SEC is not defined at these internal reference points, but rather at the external interfaces of the equipment. The input and output interfaces for SDH equipment in which the SEC may be contained are:

– 1544 kbit/s interfaces according to clause 2/G.703.

– 2048 kHz external interfaces according to clause 10/G.703.

– 2048 kbit/s interfaces according to clause 6/G.703.

– STM-N traffic interfaces.

Note that all of the above interfaces may not be implemented on all equipment. These interfaces should comply with the additional jitter and wander requirements as defined in this Recommendation.

Appendix I

Guidance on the relationship between network limits and input noise tolerances

The network limit represents the worst case accumulation of jitter and wander within the synchronization distribution network for a particular application. The main purpose for defining a network limit is that it provides the maximum amount of jitter and wander that any synchronization element in the network may experience at its input in order to meet performance limits. The network limit should not be exceeded at the output of a synchronization element anywhere in the network. The network limits therefore provide indirectly the requirements for the lower limit of maximum tolerable jitter and wander at the input of synchronization elements.

It is possible that depending upon the application or clock , there may be different constraints imposed on the synchronization interface. However, the noise tolerance for a specific clock should be that requirement which places the more stringent requirements on the clock.

I.1 Option 1 network limits

For Option 1 SECs, only one network limit applies for all applications and this is defined in Figures 5 to 7 in the main body of the Recommendation.

I.2 Option 2 network limits

For Option 2, in order to have acceptable 45 Mbit/s payload jitter accumulation through AU-3 islands, the synchronization signal input to a SEC must have a network limit bounded by Figure 8 of the main body of the Recommendation.

In order to have acceptable wander accumulation and slip performance for 1544 kbit/s payloads transported through VC-11 islands and terminating in controlled slip buffers, with hysteresis as small as 18 μs, the synchronization input to a SEC must be bounded by Figure I.1.

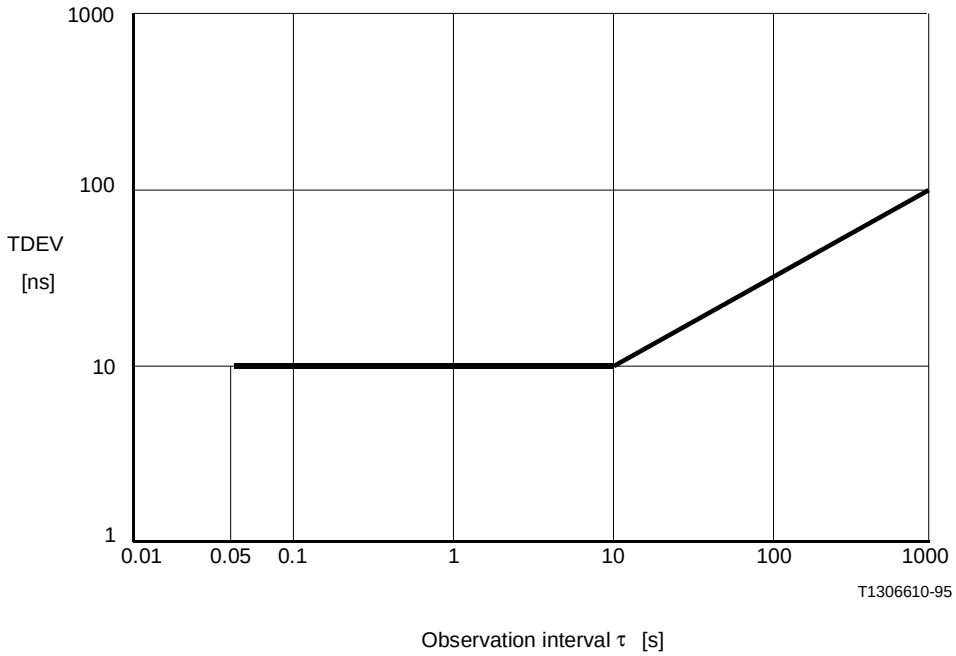

FIGURE I.1/G.813

Synchronization network limit to maintain 1544 kbit/s slip performance as defined in Recommendation G.822

Appendix II

Considerations on bandwidth requirements, noise accumulation, and payload wander accumulation

II.1 Introduction

In locked mode a SEC will generally mimic the behaviour of a 2-nd order linear analogue phase locked loop. This allows the use of the terms (equivalent) 3 dB bandwidth and (equivalent) damping factor, as they are used in analog PLL theory, irrespective of the fact that in the implementation of a SEC, digital and/or non-linear techniques may be used.

In this Appendix the considerations on the choice of equivalent bandwidth are discussed, given the constraints imposed by the stated requirements and assumptions. In addition, considerations are given for the Option 2 network limit TDEV mask (for acceptable wander and slip performance for 1544 kbit/s transport over VC-11 islands) in Figure I.1 and the Option 2 wander generation MTIE and TDEV masks in Figures 3 and 4.

II.2 Relevant network requirements and assumptions for option 1

II.2.1 G.825 STM-N jitter acceptance

Table 2/G.825 states that the tolerance for jitter on the STM-4 signal decreases linearly along a 7.5 ppm slope between A_2 (0.25 μs) and A_3 (1.5 UI) levels. The STM-4 case is the most restrictive in this respect. In the cases of STM-1 and STM-16 the requirements are 15.2 ppm and 9.5 ppm respectively.

This requirement leads directly to an upper limit for the SEC bandwidth. When the SEC switches reference it will experience a phase jump on its input, because in general the phases of the various references are uncorrelated. Such jumps may lead to a phase jump on the output with a magnitude of at most 120 ns. The jumps are shown in Figure II.2. Their magnitude of 120 ns is between the A_2 and A_3 levels in Table 2/G.825 and hence the 7.5 ppm limit applies. In other words it must take at least 16 ms to reach the 120 ns phase offset at the output. A time constant of 16 ms corresponds to a bandwidth of at most 10 Hz in a PLL model with a reasonable damping factor (e.g. larger than 3).

II.2.2 Wander accumulation in a synchronization distribution chain

The choice of bandwidth for the SEC needs to consider the worst case synchronization reference chain as described in Figure 6-4/G.803. To limit the wander accumulation, the bandwidth ratio between the SEC and the G.812 clock must be large enough. An upper limit for the bandwidth of an G.812 like clock is given in Recommendation Q.551 to be 0.1 Hz. This assumption leads to the consideration that the SEC bandwidth should be at least 1 Hz. If the G.812/SEC bandwidth ratio is sufficiently large, only a fraction of the chain according to Figure II.1 has to be considered for the noise contribution of the SECs to the noise at the output of the synchronization chain.

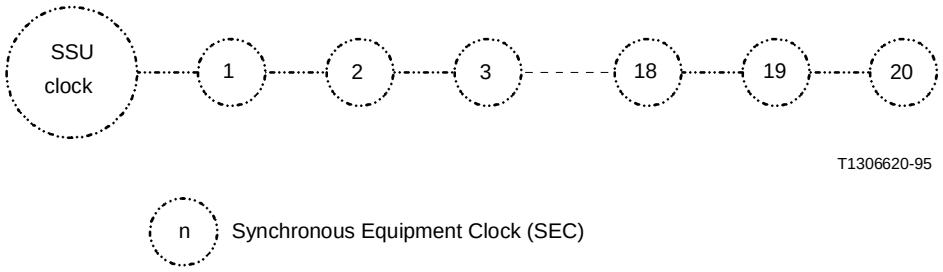

FIGURE II.1/G.813

Synchronization reference chain

Simulations have been carried out using standard clock recovery device models. The simulation results show that the output noise is predominantly determined by the SECs, and that increasing the bandwidth of the SECs significantly reduces the jitter and wander produced by the chain. This leads to a minimum bandwidth requirement in the order of 1 Hz.

II.2.3 Phase transients due to automatic timing restoration

The reference chain of Figure 6-4/G.803 shows that a path carrying synchronization through the network may contain up to 10 G.812 clocks and 60 SECs. Since the wander on such a synchronization distribution trail is limited to 5 µs, it is necessary to limit phase transients that are the consequence of automatic timing restoration in a chain of SECs.

A value of 1 µs is assumed as the upper limit for such a phase transient. Moreover, if phase transients stay below 1 µs, the SEC chain shows the same MTIE performance as a single G.812. Such a practice avoids the risk that the downstream G.812 generates an alarm or performs reference switching due to a bad input, since it may be assumed that G.812s in general can accept the 1 µs transients that may be generated by the upstream G.812.

From the 1 µs requirement a lower limit of the SEC bandwidth can be deduced, by considering the restoration time of a SEC chain and the holdover accuracy of the SEC. Given that two-phase jumps with a contribution of 120 ns each may be needed to switch to and from holdover, there are 15 s to

operate with an inaccuracy of 50 ns/s (0.05 ppm) and still stay within the 1000 ns phase transient limit (see Figure II.2).

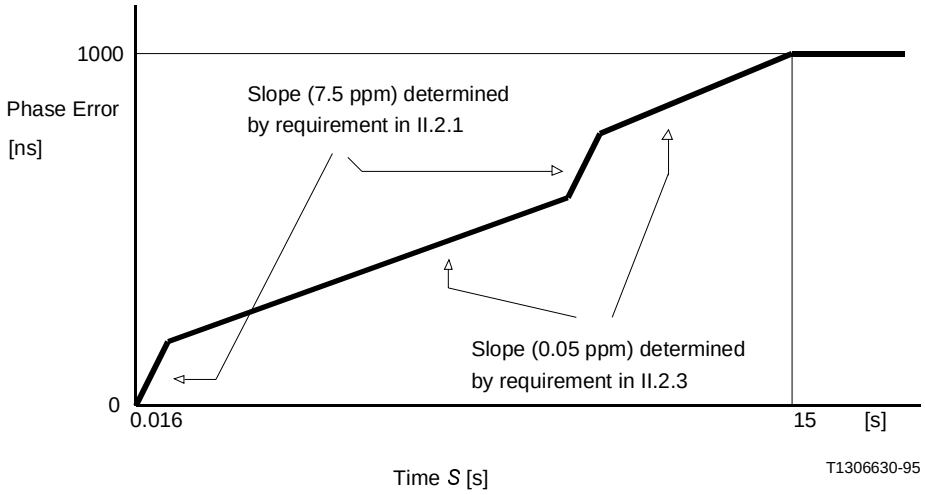

FIGURE II.2/G.813

SEC output phase under reference switching

This imposes a trade-off between the processing time of the synchronization status messages that trigger the timing restoration, and the bandwidth of the SECs. The simulations used in the derivation of Figure II.2 assumed an SSMB and reference switching time in the order of 200-600 ms. This corresponds to a minimum SEC bandwidth of 1 Hz. However tests carried out on early generation SDH equipment have ranges of reference switching completion times up to 10 seconds when switching to and from holdover mode. The future objective should be to reduce this reference switching time to and from holdover mode.

This simulation was done on the longest chain (20) of SECs in a ring. The 1000 ns phase transient limit is reached only in one SEC of the ring when the failure is located in a specific location on the ring. Furthermore, the simulation assumed that each switch in each node gives rise to the maximum phase step of +120 ns.

II.2.4 Conclusion

In summary the requirements listed above lead to the bandwidth constraints for the SEC in Table II.1.

TABLE II.1/G.813

Requirements for SEC bandwidth constraints for option 1

Requirement	Resulting SEC bandwidth constraint
G.825 STM-N jitter acceptance	< 10 Hz
Wander accumulation in a synchronization distribution chain; G.812/SEC bandwidth ratio	> 1 Hz
Wander accumulation in a synchronization distribution chain; SEC accumulation	> 1 Hz
1 μs maximum phase transients due to automatic timing restoration	> 1 Hz

From this it is concluded that the bandwidth of the SEC should be in the range 1 - 10 Hz.

II.3 Relevant network requirements and assumptions for option 2

II.3.1 Clock bandwidth requirements

The following considerations were taken into account in determining the maximum bandwidth of a G.813 clock used in networks based on the G.824 1544 kbit/s hierarchy:

– 1544 kbit/s facilities from the G.824 hierarchy used for synchronization distribution may experience a phase transient of up to 81 ns in any 1.326 ms period (1/8 UI at the 1544 kbit/s rate) up to a maximum of 1000 ns total (1000 ns in 16.4 ms, or $\Delta f/f$ = 61 ppm max.).

– If not adequately filtered, this 1544 kbit/s synchronization transient may encode large phase changes onto payloads which are synchronized into SDH payload containers (particularly 44 736 kbit/s payloads into AU-3) through the asynchronous stuffing process.

– The Option 2 G.813 clock must filter and slow this rapid phase rate of change, or up to 25 UI of jitter may be encoded into 44 736 kbit/s payloads through the asynchronous stuffing process (44 736 kbit/s jitter measured through a 10 Hz single pole high-pass filter). Since the network jitter limit for 44 736 kbit/s payloads in the G.824 hierarchy is 5 UIpp, this performance level is undesirable.

– A network jitter allocation budget for 44 736 kbit/s payloads passing through SDH islands was determined which allowed up to 32 44 736 kbit/s SDH islands, and allowed 44 736 kbit/s jitter budgets for SDH 44 736 kbit/s mapping jitter, jitter from AU-3 pointers, and 44 736 kbit/s mapping jitter accumulation from conventional asynchronous transport processes (PDH transport). The SDH 44 736 kbit/s mapping jitter portion of this budget allowed up to 0.4 UIpp 44 736 kbit/s jitter per synchronizer/desynchronizer pair (SDH island).

– To limit 44 736 kbit/s jitter encoded through the SDH mapping process due to the 1544 kbit/s synchronization transient to ~0.4 UIpp, a maximum NE clock filtering bandwidth of 0.1 Hz is required for NEs controlled by G.813 Option 2 clocks.

There is no lower bandwidth limit specified for Option 2 G.813 NE clocks.

II.3.2 Network limit TDEV mask

The network limit TDEV mask in Figure I.1 was based on studies of wander accumulation on 1544 kbit/s signals transported through SDH VC-11 islands. A VC-11 island is an SDH network with asynchronous interfaces; a VC-11 island reference connection for wander is shown in Figure II.3.

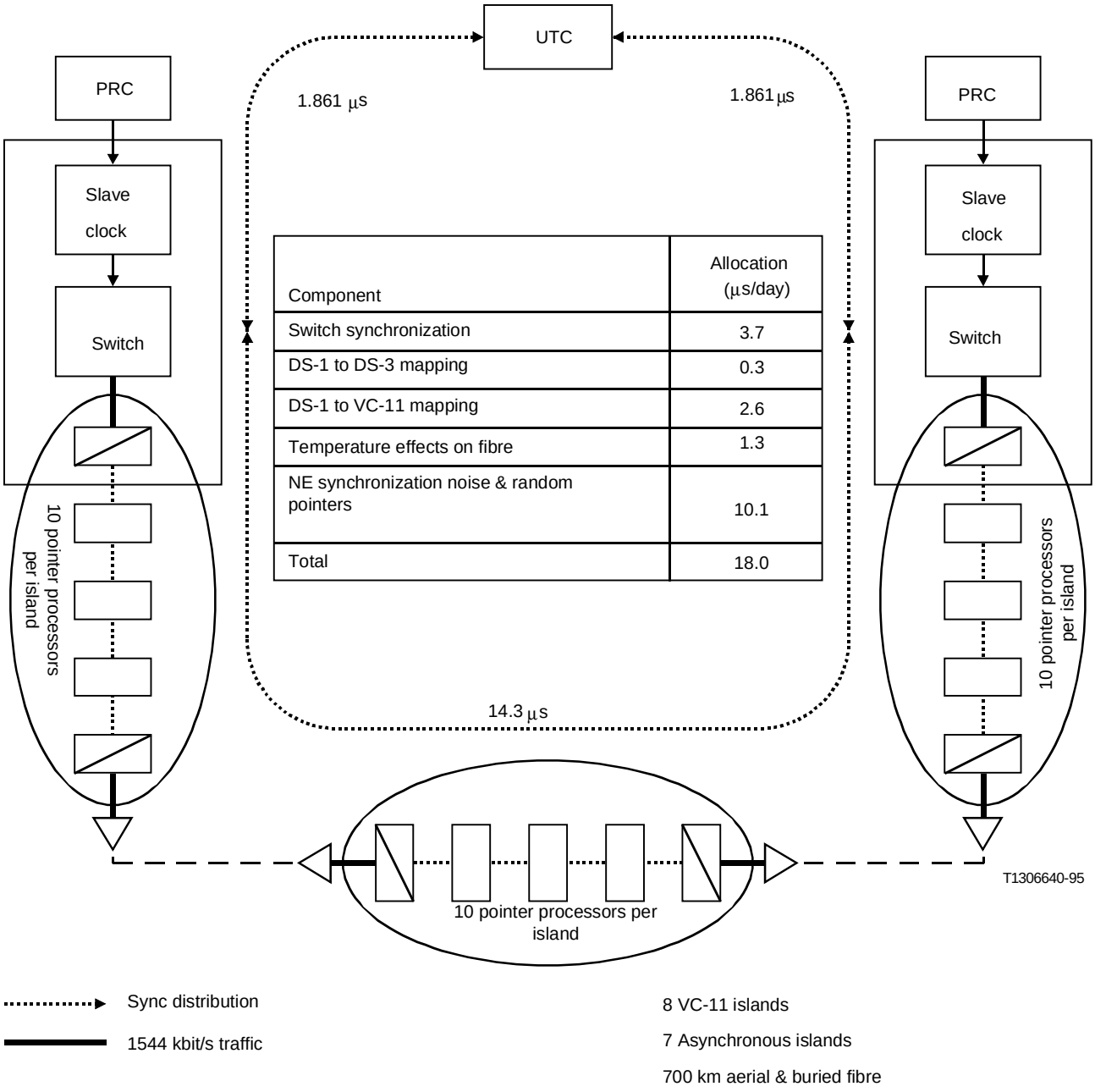

FIGURE II.3/G.813

SDH VC-11 island wander reference model and wander budget

As these VC-11 islands are interconnected, jitter and wander can accumulate as 1544 kbit/s signals are mapped and demapped from SDH signals. Extensive simulation studies were performed for 1544 kbit/s wander accumulation.[1] A wander budget was developed for the 1544 kbit/s signals transported over these islands, and is also shown in Figure II.3. This wander budget allocates 10.1 µs of wander per day to SDH NE synchronization noise and random pointer adjustments. This budget was

[1] Extensive simulation studies were also performed for both 1544 kbit/s and 44 736 kbit/s jitter accumulation, using appropriate VC-11 and AU-3 island reference models. The results showed that the SDH NE synchronization requirements for acceptable 1544 kbit/s wander accumulation are tighter than for acceptable 1544 kbit/s or 44 736 kbit/s jitter accumulation (see Appendix I).

developed using Recommendation G.822 as a guideline. Recommendation G.822 specifies in a national and local network that there should be less than an average of 2.3 slips in 24 hours (46% of 5 slips in 24 hours) at least 98.9% of the time.

The model assumptions for the 1544 kbit/s wander and slip simulations are described below in II.3.2.1. It was found that, for a network of 8 VC-11 islands with each SDH NE synchronized by a signal that meets the TDEV mask of Figure I.1, there will be 1 or fewer 1544 kbit/s slips per day 94.6% of the time and 2 or fewer 1544 kbit/s slips per day 99.0% of the time. It was decided that not all networks of large number of VC-11 islands need to be accommodated. Recommendation G.801 states that the hypothetical reference connection "...does not represent the rare worst case connection; although it does aim to encompass the vast majority of connections."

II.3.2.1 1544 kbit/s wander accumulation and slip simulation model assumptions

In the simulation model, each node of each SDH island was synchronized by a clock phase noise model that contained a Flicker Phase Modulation (FPM) component and White Frequency Modulation (WFM) component. The WFM noise component was produced by generating a Gaussian white noise random sequence with zero mean and standard deviation equal to the specified amplitude, and then integrating this process. The FPM noise component was produced by generating a Gaussian white noise random sequence with zero mean and standard deviation equal to the specified amplitude, and then passing this sequence through a set of filters as described and implemented in [1]. The FPM and WFM amplitudes were chosen such that TDEV for the resulting phase noise just met the mask of Figure I.1. This resulting phase noise was filtered by a single-pole, 0.1 Hz low-pass filter, which represented the SDH NE clock. VC-11 pointer processors were assumed to have a 2-byte threshold spacing, and AU-3 pointer processors were assumed to have a 4-byte threshold spacing. The desynchronizers in each island were not modelled, as these do not affect long-term phase variation and 1544 kbit/s slip performance. The simulation results described at the end of the above subclause were for a network of 8 VC-11 islands with 10 pointer processor nodes per island. For each simulation case (i.e. for the 8 VC-11 island case described above and for various other cases), a number of independent replications were run to obtain statistically significant results.

1544 kbit/s slip performance was obtained using an approximate slip buffer model. In this model, the slip buffer size is equal to the sum of the frame size and the hysteresis. The buffer fill at any given time is equal to the sum of the initial buffer fill, the 1544 kbit/s phase input, and the total phase due to all slips up to that time. For each of the independent replications of the 1544 kbit/s phase accumulation simulation, the slip buffer simulation was run a number of times, with a different slip buffer initial condition for each run. The initial buffer fills were chosen to be uniformly-spaced.[2] For each of these runs, the number of slips was recorded; a statistical analysis was performed on the results of all the runs to obtain estimates of the probabilities of obtaining various numbers of slips in one day.

The input to the slip buffer model should be the total 1544 kbit/s phase, due to all the components of the wander budget in Figure II.3. However, it was not practical to run multiple, independent replications of 1-day simulations of 1544 kbit/s-to-44 736 kbit/s mapping and of 1544 kbit/s-to-VC-11 mapping (the computational requirements for this would have been prohibitive). In addition, a model for the component due to temperature effects on the fiber was not available. Therefore, these components were not simulated; they were accounted for by reducing the slip buffer hysteresis by their budgeted amounts in Figure II.3. The slip buffer hysteresis used in the simulations was therefore 13.8 μs. The component of 1544 kbit/s wander due to switch synchronization was simulated using a random phase noise model similar to the one above for SDH NE synchronization noise. The main

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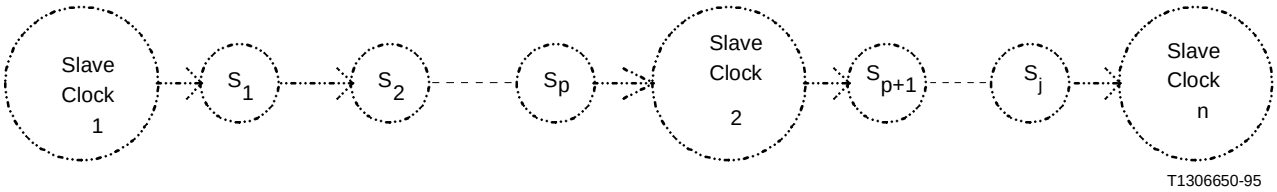
[2] For most cases, the number of independent wander accumulation simulation replications was 300 and, for each replication, the number of slip buffer simulations was 51.

difference between the two models is that the noise levels for switch synchronization are somewhat higher.

II.3.3 Wander accumulation in a synchronization distribution chain

This subclause describes noise accumulation studies for synchronization reference chains. The purpose of this work was to verify that the wander generation requirements in Figures 3 and 4 are consistent with the network limit in Figure I.1.

Figure II.4 represents a generic model for synchronization distribution via SDH facilities in a network based on Option 2. With the exception of the first slave clock, the model assumes that all slave clocks in the chain derive timing from the optical carrier and not an embedded asynchronous payload signal. Each slave clock is of higher quality than the Option 2 SEC. This model can represent distribution topologies for any synchronization distribution architecture (linear, line-timed rings, etc.), and is consistent with the architecture of models in Recommendation G.803.



S_i i^{th} SDH NE clock in chain

j Total number of SDH NE clocks

n Total number of slave clocks

p Number of SDH NE clocks between slave clocks

NOTE – Slave clock n is shown here as the last element in the reference chain.
S_j could be the last element in the reference chain.

FIGURE II.4/G.813

SDH synchronization distribution reference chain (option 2)

Simulations were performed for noise accumulation in several examples of Option 2 synchronization reference chains. These examples include a chain of up to 10 externally-timed SDH NEs and a line-timed ring with 16 SDH NEs. The output of each clock was assumed to be the sum of the input filtered by a low-pass filter, plus the internal noise generation and any transients due to reference switching or internal rearrangement. Each SDH NE clock was assumed to have a bandwidth of 0.1 Hz (see clause 9, Option 2). Each slave clock was assumed to have a bandwidth of 0.01 Hz. The wander generation of each SDH NE clock was assumed to meet the TDEV and MTIE masks of 7.1, Option 2. The noise generation model was constructed by superposing appropriately-filtered White Phase Modulation (WPM), FPM, and WFM sources.

For a chain of 10 externally-timed SDH NEs and no phase transients, simulation results show that the output of the last clock in the chain (the tenth SDH NE) has TDEV approximately a factor of 3 below the mask in Figure I.1 for integration times less than about 400 s. For longer integration times, TDEV for the last clock output levels off and then decreases while the TDEV mask continues to increase with WFM characteristic. For a line-timed ring with 16 SDH NEs and no phase transients, simulation results show that the output of the last SDH NE clock has TDEV approximately a factor of 3 below the mask in Figure I.1 for integration times less than approximately 100 s. For longer integration times, TDEV for the last clock output levels off and then decreases while the TDEV mask continues to increase with WFM characteristic. For a chain of 4 externally-timed SDH NEs and

2 transients per chain per day, with each transient having amplitude of 150 ns and sign chosen randomly at initialization, simulation results show that the output of the last clock in the chain (the fourth SDH NE) has TDEV approximately a factor of 3 below the mask in Figure I.1/G.813 for integration times less than approximately 100 s. For longer integration times, TDEV for the last clock increases less rapidly than the mask until about 5000 s, and then increases with approximately WFM slope (this is consistent with the randomly-occurring step transients). For long integration times (beyond 10 000 s), TDEV for the last clock is approximately a factor of 8 to 10 below the mask.

References

[1] BARNES (James A.), GREENHALL (Charles A.): Large Sample Simulation of Flicker Noise, *19th Annual Precise Time and Time Interval (PTTI) Applications Planning Meeting*, December 1987.

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