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Digital networks – General aspects

ATM cell mapping into plesiochronous digital hierarchy (PDH)

ITU-T Recommendation G.804

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ITU-T Recommendation G.804

ATM cell mapping into plesiochronous digital hierarchy (PDH)

Summary

This Recommendation provides the mapping to be used for the transport of ATM cells over PDH at the various hierarchical bit rates defined in ITU-T Rec. G.702. These mappings cover both the 1544 kbit/s and 2048 kbit/s-based hierarchies and are used in conjunction with the frame structures defined in ITU-T Rec. G.832.

Source

ITU-T Recommendation G.804 was approved on 13 June 2004 by ITU-T Study Group 15 (2001-2004) under the ITU-T Recommendation A.8 procedure.

Keywords

AAL2, ATM, mapping, PDH.

FOREWORD

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ITU-T Recommendation G.804

ATM cell mapping into plesiochronous digital hierarchy (PDH)

1 Introduction

This Recommendation identifies the way of transporting ATM cells over PDH networks at different hierarchical bit rates.

1.1 Scope

Existing transmission networks are based on Plesiochronous Digital Hierarchy (PDH) as defined in ITU-T Rec. G.702. ATM is considered as the suitable technique to support B-ISDN. The Synchronous Digital Hierarchy (SDH) will form the basis of transport of the ATM cells.

During the transition period, there is a need to transport ATM cells using existing PDH transmission networks. This Recommendation provides the mapping to be used for this transport of ATM cells on the different PDH bit rates for both 1544 and 2048 kbit/s hierarchies.

1.2 References

The following ITU-T Recommendations and other references contain provisions which, through reference in this text, constitute provisions of this Recommendation. At the time of publication, the editions indicated were valid. All Recommendations and other references are subject to revision; users of this Recommendation are therefore encouraged to investigate the possibility of applying the most recent edition of the Recommendations and other references listed below. A list of the currently valid ITU-T Recommendations is regularly published. The reference to a document within this Recommendation does not give it, as a stand-alone document, the status of a Recommendation.

– ITU-T Recommendation G.702 (1988), *Digital hierarchy bit rates*.

– ITU-T Recommendation G.704 (1998), *Synchronous frame structures used at 1544, 6312, 2048, 8448 and 44 736 kbit/s hierarchical levels*.

– ITU-T Recommendation G.706 (1991), *Frame alignment and cyclic redundancy check (CRC) procedures relating to basic frame structures defined in Recommendation G.704*.

– ITU-T Recommendation G.832 (1998), *Transport of SDH elements on PDH networks – Frame and multiplexing structures*.

– ITU-T Recommendation I.363.2 (2000), *B-ISDN ATM Adaptation Layer specification: Type 2 AAL*.

– ITU-T Recommendation I.432.1 (1999), *B-ISDN user-network interface – Physical layer specification: General characteristics*.

1.3 Definitions

This Recommendation defines the following terms:

1.3.1 idle cell: A cell which is inserted and extracted by the physical layer in order to adapt the cell flow rate at the boundary between the ATM layer and the physical layer to the available payload capacity of the transmission used.

1.3.2 valid cell: A cell whose header has no errors or has been modified by the cell Header Error Control (HEC) verification process.

1.3.3 nibble: A nibble is a group of four bits.

1.4 Abbreviations

This Recommendation uses the following abbreviations:

AAL	ATM Adaptation Layer
AAL2-CPS	AAL type 2 Common Part Sublayer
AIS	Alarm Indication Signal
ATM	Asynchronous Transfer Mode
BIP-8	Bit Interleaved Parity-8
B-ISDN	Broadband aspects of Integrated Services Digital Network
CID	Channel Identifier
CIF	Channel Identification Field
CRC	Cyclic Redundancy Check
FEAC	Far-End Alarm and Control
FEBE	Far-End Block Error
FERF	Far-End Receive Failure
HEC	Header Error Control
LCD	Loss of Cell Delineation
OAM	Operation, Administration and Maintenance
PDH	Plesiochronous Digital Hierarchy
PLCP	Physical Layer Convergence Protocol
POH	Path OverHead
POI	Path Overhead Identifier
RAI	Remote Alarm Indication
SDH	Synchronous Digital Hierarchy
SYF	Synchronization Field
TS	Time Slot

1.5 Conventions

The order of transmission of information in all diagrams in this Recommendation is first from left to right and then top to bottom. Within each byte the most significant bit is transmitted first. The most significant bit (bit 1) is illustrated at the left of all diagrams.

2 Mapping of ATM cells into 1544 kbit/s

2.1 Frame format

The multiframe structure for the 24-frame multiframe as described in ITU-T Rec. G.704 shall be used.

The ATM cell is mapped into bits 2 to 193 (i.e., time slots 1 to 24 described in ITU-T Rec. G.704) of the 1544 kbit/s frame with the octet structure of the cell aligned with the octet structure of the frame (see Figure 2-1).

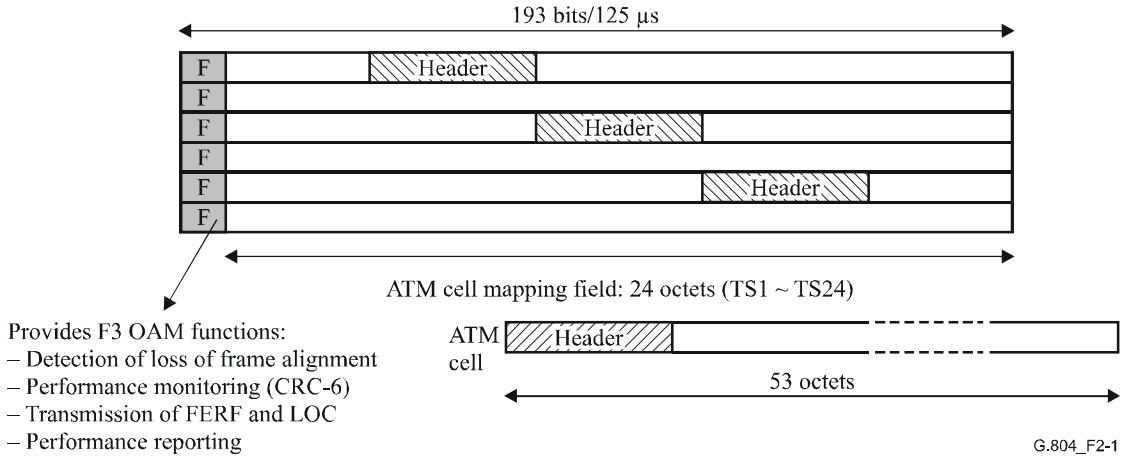

Figure 2-1/G.804 – Frame structure for 1544 kbit/s used to transport ATM cells

2.2 Cell rate adaptation

The cell rate adaptation to the payload capacity of the frames is performed by the insertion of idle cells, as described in ITU-T Rec. I.432.1, when valid cells are not available from the ATM layer.

2.3 Header Error Control (HEC) generation

The Header Error Control (HEC) value is generated and inserted in the specific field in compliance with ITU-T Rec. I.432.1.

2.4 Scrambling of the ATM cell payload (optional)

As an option, the ATM cell payload (48 bytes) can be scrambled before mapping into the 1544 kbit/s signal. If this option is used, then, in the reverse operation, following the termination of 1544 kbit/s signal, the ATM cell payload will be descrambled before being passed to the ATM layer. The self-synchronizing scrambler with the generator polynomial $x^{43} + 1$, as described in ITU-T Rec. I.432.1, is used. If this option is not used, then no descrambling is done in the reverse operation.

2.5 Cell delineation

The cell delineation shall be performed using the Header Error Control (HEC) mechanism as defined in ITU-T Rec. I.432.1.

2.6 Cell header verification and extraction

The cell header verification shall be performed in compliance with ITU-T Rec. I.432.1. All physical layer cells shall be extracted and only valid cells are passed to the ATM layer.

2.7 Physical layer OAM

The error detection and performance reporting functions described in ITU-T Rec. G.704 are used. In addition, the Loss of Cell Delineation (LCD) is to be reported by a priority data link message. The specific 16-bit codeword is for further study.

3 Mapping of ATM cells into 2048 kbit/s

The mapping of ATM cells in a G.704 2048 kbit/s frame is described below. Annex A contains the description of an alternative method that can optionally be used when AAL2 CPS-packets are contained in the ATM cells.

3.1 Frame format

The basic frame structure at 2048 kbit/s as described in ITU-T Rec. G.704 shall be used.

The ATM cell is mapped into bits 9 to 128 and bits 137 to 256 (i.e., time slots 1 to 15 and time slots 17 to 31 described in ITU-T Rec. G.704) of the 2048 kbit/s frame with the octet structure of the cell aligned with the octet structure of the frame (see Figure 3-1).

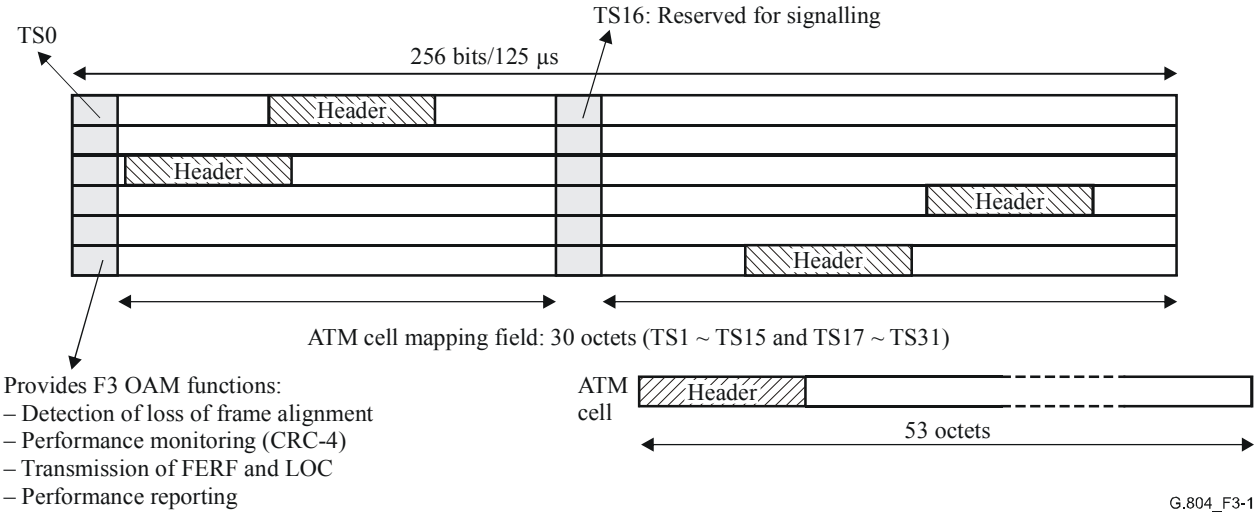

Figure 3-1/G.804 – Frame structure for 2048 kbit/s used to transport ATM cells

3.2 Cell rate adaptation

The cell rate adaptation to the payload capacity of the frames is performed by the insertion of idle cells, as described in ITU-T Rec. I.432.1, when valid cells are not available from the ATM layer.

3.3 Header Error Control (HEC) generation

The Header Error Control (HEC) value is generated and inserted in the specific field in compliance with ITU-T Rec. I.432.1.

3.4 Scrambling of the ATM cell payload

The ATM cell payload (48 bytes) shall be scrambled before mapping into the 2048 kbit/s signal. In the reverse operation, following the termination of the 2048 kbit/s signal, the ATM cell payload will be descrambled before being passed to the ATM layer. A self-synchronizing scrambler with the generator polynomial $x^{43} + 1$, as described in ITU-T Rec. I.432.1, shall be used. Cell payload field scrambling is required to provide security against false cell delineation and replication of the 2048 kbit/s frame alignment word.

3.5 Cell delineation

The cell delineation shall be performed using the Header Error Control (HEC) mechanism as defined in ITU-T Rec. I.432.1.

3.6 Cell header verification and extraction

The cell header verification shall be performed in compliance with ITU-T Rec. I.432.1. All the physical layer cells shall be extracted and only the valid cells are passed to the ATM layer.

3.7 Physical layer OAM

Overhead bits for physical layer OAM functionality are defined in ITU-T Rec. G.704.

4 Mapping of ATM cells into 6312 kbit/s

4.1 Frame format

The basic frame structure at 6312 kbit/s as described in ITU-T Rec. G.704 shall be used.

The ATM cell is mapped into bits 1 to 768 (i.e., time slots 1 to 96 described in ITU-T Rec. G.704) of the 6312 kbit/s frame with the octet structure of the cell aligned with the octet structure of the 6312 kbit/s frame. Bits 769 to 784 (time slots 97 and 98) are reserved for user communication channels and the last five bits (F-bits) are used for frame alignment and OAM (see Figure 4-1).

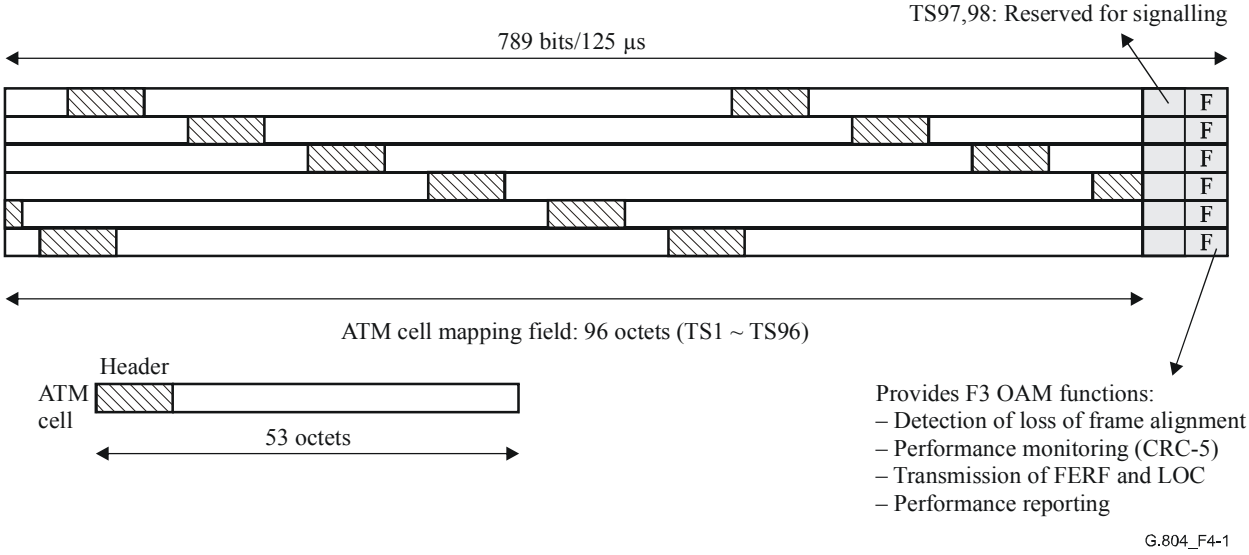

Figure 4-1/G.804 – Frame structure for 6312 kbit/s used to transport ATM cells

4.2 Cell rate adaptation

The cell rate adaptation to the payload capacity of the frames is performed by the insertion of idle cells, as described in ITU-T Rec. I.432.1, when valid cells are not available from the ATM layer.

4.3 Header Error Control (HEC) generation

The Header Error Control (HEC) value is generated and inserted in the specific field in compliance with ITU-T Rec. I.432.1.

4.4 Scrambling of the ATM cell payload

The ATM cell payload (48 bytes) shall be scrambled before mapping into the 6312 kbit/s signal. In the reverse operation, following the termination of the 6312 kbit/s signal, the ATM cell payload will be descrambled before being passed to the ATM layer. A self-synchronizing scrambler with the generator polynomial $x^{43} + 1$, as described in ITU-T Rec. I.432.1, shall be used. Cell payload field scrambling is required to provide security against false cell delineation and replication of the 6312 kbit/s frame alignment word.

4.5 Cell delineation

The cell delineation shall be performed using the Header Error Control (HEC) mechanism as defined in ITU-T Rec. I.432.1.

4.6 Cell header verification and extraction

The cell header verification shall be performed in compliance with ITU-T Rec. I.432.1. All the physical layer cells shall be extracted and only the valid cells are passed to the ATM layer.

4.7 Physical layer OAM

The error monitoring is performed by the CRC-5 procedure defined in ITU-T Rec. G.706. The transmission of the FERF is performed using the F-bits as described in ITU-T Rec. G.704. The FERF should also be used to indicate the LCD. The transmission of FEBE is for further study.

5 Mapping of ATM cells into 8448 kbit/s

The standardization of this mapping is not foreseen anymore.

6 Mapping of ATM cells into 34 368 kbit/s

6.1 Frame format

The basic frame structure at 34 368 kbit/s as described in ITU-T Rec. G.832 shall be used.

The ATM cells are mapped into the 530 payload octets of the 34 368 kbit/s frame with the octet structure of the cell aligned with the octet structure of the frame (see Figure 6-1).

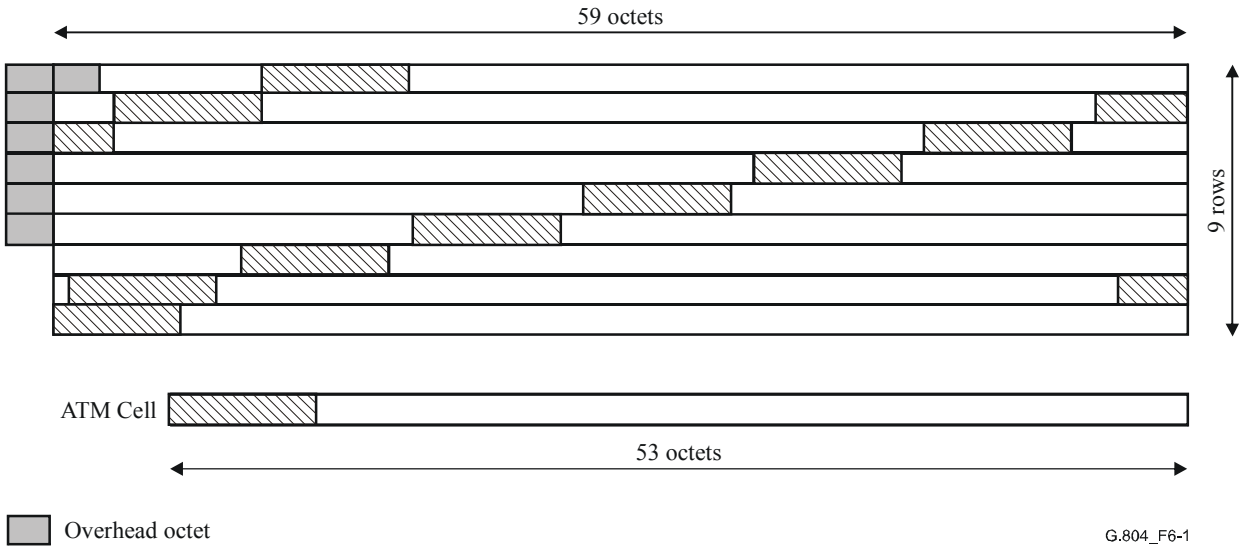

Figure 6-1/G.804 – Frame structure for 34 368 kbit/s used to transport ATM cells

6.2 Cell rate adaptation

The cell rate adaptation to the payload capacity of the frames is performed by the insertion of idle cells, as described in ITU-T Rec. I.432.1, when valid cells are not available from the ATM layer.

6.3 Header Error Control (HEC)

The Header Error Control (HEC) value is generated and inserted in the specific field in compliance with ITU-T Rec. I.432.1.

6.4 Scrambling of the ATM cell payload

The ATM cell payload (48 bytes) shall be scrambled before mapping into the 34 368 kbit/s signal. In the reverse operation, following the termination of the 34 368 kbit/s signal, the ATM cell payload

will be descrambled before being passed to the ATM layer. A self-synchronizing scrambler with the generator polynomial $x^{43} + 1$, as described in ITU-T Rec. I.432.1, shall be used. Cell payload field scrambling is required to provide security against false cell delineation and the replication of the 34 368 kbit/s frame alignment word.

6.5 Cell delineation

The cell delineation shall be performed using the HEC mechanism as defined in ITU-T Rec. I.432.1.

6.6 Cell header verification and extraction

The cell header verification shall be performed in compliance with ITU-T Rec. I.432.1. All physical layer cells shall be extracted and only valid cells are passed to the ATM layer.

6.7 Physical layer OAM

Overhead bytes for physical layer OAM functionality are defined in ITU-T Rec. G.832.

7 Mapping of ATM cells into 44 736 kbit/s

7.1 Frame format

The multiframe format at 44 736 kbit/s, as described in ITU-T Rec. G.704, shall be used.

7.2 PLCP-based mapping of ATM cells

The ATM Physical Layer Convergence Protocol (PLCP) defines a mapping of ATM cells onto existing 44 736 kbit/s facilities. This PLCP is described in the following subclauses.

The PLCP consists of a 125 µs frame within a standard 44 736 kbit/s payload. Note there is no fixed relationship between the PLCP frame and the 44 736 kbit/s frame, i.e., the PLCP begins anywhere inside the 44 736 kbit/s payload. The PLCP frame (Figure 7-1) consists of 12 rows of ATM cells, each preceded by four octets of overhead. Nibble stuffing is required after the twelfth cell to fill the 125 µs PLCP frame. Although the PLCP is not aligned to the 44 736 kbit/s framing bits, the octets in the PLCP frame are nibble-aligned to the 44 736 kbit/s payload envelope. Nibbles begin after the control bits (F, X, P, C or M) of the 44 736 kbit/s frame. Note that the stuff bits are never used in the 44 736 kbit/s, i.e., the payload is always inserted. Octets comprising the PLCP frame are described in the following subclauses.

Note that order and transmission of all PLCP bits and octets are from left to right and top to bottom. The figures represent the Most Significant Bit (MSB) on the left and the Least Significant Bit (LSB) on the right.

PLCP	Framing	POI	POH	PLCP Payload	
A1	A2	P11	Z6	First ATM Cell	
A1	A2	P10	Z5	ATM Cell	
A1	A2	P09	Z4	ATM Cell	
A1	A2	P08	Z3	ATM Cell	
A1	A2	P07	Z2	ATM Cell	
A1	A2	P06	Z1	ATM Cell	
A1	A2	P05	X	ATM Cell	
A1	A2	P04	B1	ATM Cell	
A1	A2	P03	G1	ATM Cell	
A1	A2	P02	X	ATM Cell	
A1	A2	P01	X	ATM Cell	
A1	A2	P00	C1	Twelfth ATM Cell	Trailer
1 octet	1 octet	1 octet	1 octet	53 octets	13 or 14 nibbles
			Object of BIP-8 Calculation		

POI Path Overhead Identifier
POH Path OverHead
BIP-8 Bit Interleaved Parity-8
X Unassigned – Receiver required to ignore

Figure 7-1/G.804 – PLCP frame (125 μs)

7.2.1 Cell rate adaptation

The cell rate adaptation to the payload capacity of the PLCP frame is performed by the insertion of idle cells, as described in ITU-T Rec. I.432.1, when valid cells are not available from the ATM layer.

7.2.2 Header Error Control (HEC) generation

The HEC generation shall be compliant with ITU-T Rec. I.432.1.

7.2.3 Cell delineation

Since the cells are in predetermined locations within the PLCP, framing on the 44 736 kbit/s signal and then on the PLCP is sufficient in order to delineate cells.

7.2.4 Cell header verification and extraction

The cell header verification shall be compliant with ITU-T Rec. I.432.1. All physical layer cells shall be extracted and only valid cells are passed to the ATM layer.

7.2.5 Physical layer OAM

7.2.5.1 PLCP overhead utilization

The following PLCP overhead bytes/nibbles are required to be activated across the UNI:

– A1 Frame alignment;
– A2 Frame alignment;
– B1 PLCP path error monitoring;
– C1 Cycle/stuff counter;
– G1 PLCP path status;
– Px Path overhead identifier;

– Zx Growth octets;
– Trailer nibbles.

7.2.5.2 Frame alignment (A1, A2)

The PLCP framing octets use the same framing pattern as used in the SDH. These octets are defined as A1 = 11110110, A2 = 00101000.

7.2.5.3 PLCP path error monitoring (B1)

The Bit Interleaved Parity-8 (BIP-8) field supports path error monitoring, and is calculated over a 12×54 octet structure consisting of POH field and the associated ATM cells (648 octets) of the previous PLCP frame.

7.2.5.4 Cycle/stuff counter (C1)

In general, the cycle/stuff counter provides a nibble stuffing opportunity cycle and length indicator for the PLCP frame. A stuffing opportunity occurs every third frame of a three-frame (375 µs) stuffing cycle. The value of the C1 code is used as an indication of the phase of the 375 µs stuffing opportunity cycle (see Table 7-1).

Table 7-1 shows that a trailer containing 13 nibbles is used in the first frame of the 375 µs stuffing opportunity cycle. A trailer of 14 nibbles is used in the second frame. The third frame provides a nibble stuffing opportunity. A trailer containing 14 nibbles is used in the third frame if a stuff occurs. If not, the trailer will contain 13 nibbles.

Table 7-1/G.804 – Cycle/stuff counter definition

C1 code	Frame phase of cycle	Trailer length
11111111	1	13
00000000	2	14
01100110	3 (no stuff)	13
10011001	3 (stuff)	14

7.2.5.5 PLCP path status (G1)

The PLCP path status is allocated to convey the received PLCP status and performance to the transmitting far-end. This octet permits the status of the full receive/transmit PLCP path to be monitored at either end of the path. Figure 7-2 illustrates the G1 octet subfields: a 4-bit Far-End Block Error (FEBE), a 1-bit Remote Alarm Indication (RAI), and 3 X bits (X bits are set to all ones at the transmitter and may be ignored at the receiver). The use of the PLCP path status octet G1 for the Far-End Receive Failure (FERF) is for further study.

Far-End Block Error (FEBE)	RAI	X-X-X
4 Bits	1 bit	3 bits

Figure 7-2/G.804 – PLCP path status (G1) definition

7.2.5.6 Path overhead identifier (P00-P11)

The Path Overhead Identifier (POI) indexes the adjacent Path OverHead (POH) octet of the PLCP. Table 7-2 provides the coding for each of the P00-P11 octets.

Table 7-2/G.804 – Cycle/stuff counter definition

POI	POI code	Associated POH
P11	00101100	Z6
P10	00101001	Z5
P09	00100101	Z4
P08	00100000	Z3
P07	00011100	Z2
P06	00011001	Z1
P05	00010101	X
P04	00010000	B1
P03	00001101	G1
P02	00001000	X
P01	00000100	X
P00	00000001	C1
X Receiver ignores		

7.2.5.7 Growth octets (Z1-Z6)

The growth octets are reserved for future use. These octets are set to Zi-00000000, by the transmitter (i = 1, 2, ..., 6). The receiver shall be capable of ignoring the value contained in these fields.

7.2.5.8 Trailer nibbles

The contents of each of the 13/14 trailer nibbles shall be 1100.

7.3 HEC-based mapping of ATM into 44 736 kbit/s

7.3.1 Mapping of ATM cells into 44 736 kbit/s multiframe

The ATM cells are mapped into the payload with the octet structure of the cells aligned with the nibble structure of the multiframe. The multiframe is organized such that 84 bits of payload follow every overhead bit. The 84 bits can be assumed to be organized into 21 consecutive nibbles. The ATM cell is placed such that the start of a cell always coincides with the start of a nibble. ATM cells may cross multiframe boundaries (see Figure 7-3).

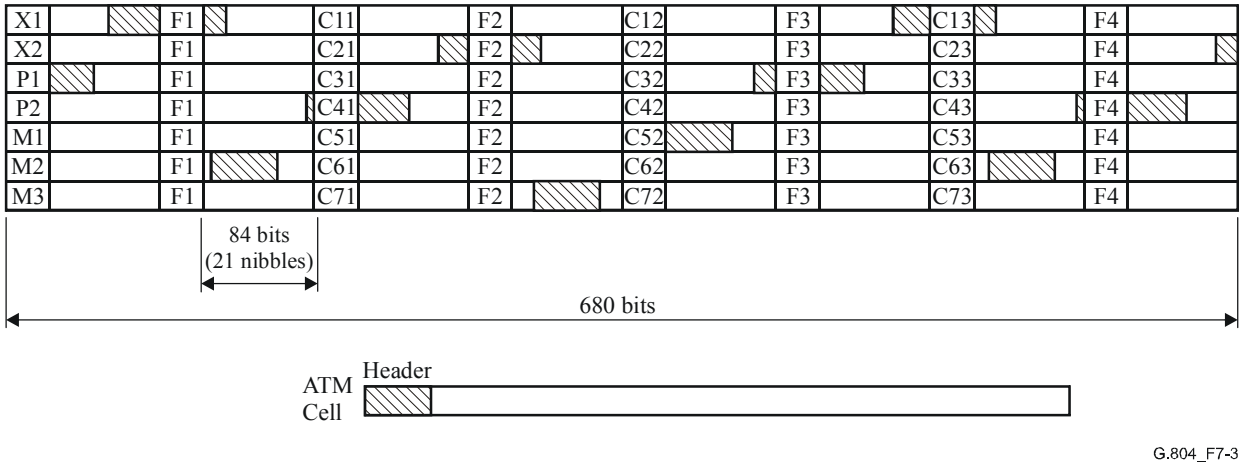

Figure 7-3/G.804 – Frame structure for 44 736 kbit/s used to transport ATM cells

7.3.2 Cell rate adaptation

The cell rate adaptation to the payload capacity of the frames is performed by the insertion of idle cells, as described in 7.3.5/I.432.1, when no valid cells are available from the ATM layer.

7.3.3 Header Error Control (HEC) generation

The Header Error Control (HEC) value is generated and inserted in the specific field in compliance with ITU-T Rec. I.432.1.

7.3.4 Cell delineation

The cell delineation shall be performed using the Header Error Control (HEC) mechanism defined in ITU-T Rec. I.432.1.

7.3.5 Cell header verification and extraction

The cell header verification shall be performed in compliance with ITU-T Rec. I.432.1.

All the physical layer cells shall be discarded and only valid cells are passed to the ATM layer.

7.3.6 Physical layer OAM

The error detection and performance reporting functions of the C-bit parity application of the 44 736 kbit/s multiframe described in ITU-T Rec. G.704 are used. In addition, Loss of Cell Delineation (LCD) and Remote Defect Indication (RDI) are to be reported by the C13 Far-End Alarm and Control (FEAC) bit of the overhead bits in the C-bit parity application. The specific 16-bit codewords are to be used from Table 6/G.704.

NOTE – The need for reporting Out of Cell Delineation (OCD) is for further study.

8 Mapping of ATM cells into 97 728 kbit/s

8.1 Frame format

The basic frame structure at 97 728 kbit/s, as described in ITU-T Rec. G.832, shall be used.

The ATM cells are mapped into the 756 octets of the C3 inside the 97 728 kbit/s frame with the octet structure of the cell aligned with the octet structure of the payload.

8.2 Cell rate adaptation

The cell rate adaptation to the payload capacity of the 97 728 kbit/s frames is performed by the insertion of idle cells, as described in ITU-T Rec. I.432.1, when valid cells are not available from the ATM layer.

8.3 Header Error Control (HEC) generation

The Header Error Control (HEC) value is generated and inserted in the specific field in compliance with ITU-T Rec. I.432.1.

8.4 Scrambling of the ATM cell payload

The ATM cell payload (48 bytes) shall be scrambled before mapping into the C3. In the reverse operation, following termination of 97 728 kbit/s signal, the ATM cell payload will be descrambled before being passed to the ATM layer. A self-synchronizing scrambler with the generator polynomial $x^{43} + 1$, as described in ITU-T Rec. I.432.1, shall be used. Cell payload field scrambling is required to provide security against false cell delineation and replication of the 97 728 kbit/s frame alignment word.

8.5 Cell delineation

The cell delineation shall be performed using the Header Error Control (HEC) mechanism as defined in ITU-T Rec. I.432.1.

8.6 Cell header verification and extraction

The cell header verification shall be performed in compliance with ITU-T Rec. I.432.1. All physical layer cells shall be extracted and only valid cells are passed to the ATM layer.

8.7 Physical layer OAM

The OAM functionality is performed using the overhead bytes defined in ITU-T Rec. G.832.

9 Mapping of ATM cells into 139 264 kbit/s

9.1 Frame format

The basic frame structure at 139 264 kbit/s, as described in ITU-T Rec. G.832, shall be used.

The ATM cells are mapped into the 2160 payload octets of the 139 264 kbit/s frame with the octet structure of the cell aligned with the octet structure of the frame (see Figure 9-1).

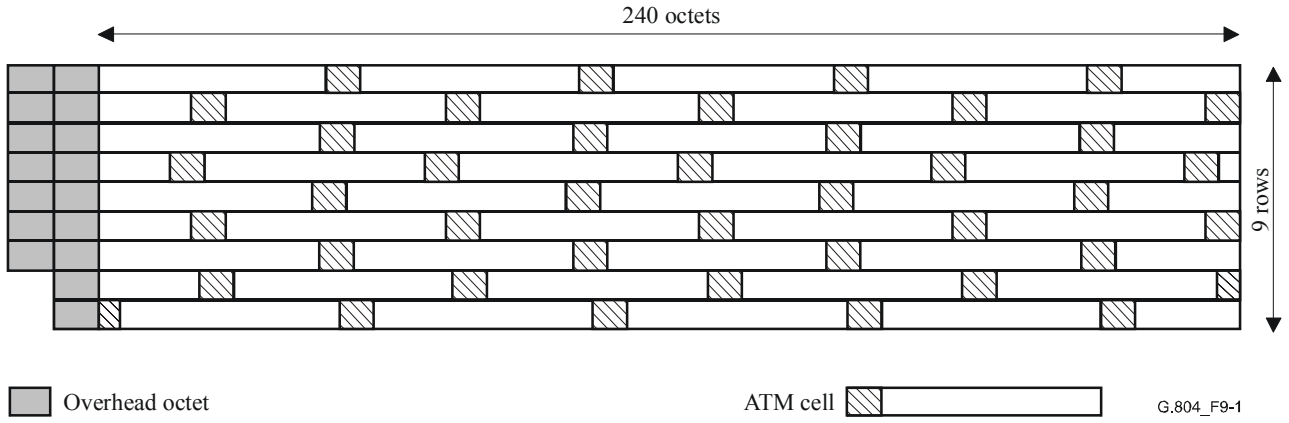

Figure 9-1/G.804 – Frame structure at 139 264 kbit/s

9.2 Cell rate adaptation

The cell rate adaptation to the payload capacity of the frames is performed by the insertion of idle cells, as described in ITU-T Rec. I.432.1, when valid cells are not available from the ATM layer.

9.3 Header Error Control (HEC) generation

The HEC value is generated and inserted in the specific field in compliance with ITU-T Rec. I.432.1.

9.4 Scrambling of the ATM cell payload

The ATM cell payload (48 bytes) shall be scrambled before mapping into 139 264 kbit/s signal. In the reverse operation, following termination of 139 264 kbit/s signal, the ATM cell payload will be descrambled before being passed to the ATM layer. A self-synchronizing scrambler with the generator polynomial $x^{43} + 1$, as described in ITU-T Rec. I.432.1, shall be used. Cell payload field scrambling is required to provide security against false cell delineation and replication of the 139 264 kbit/s frame alignment word.

9.5 Cell delineation

The cell delineation shall be performed using the Header Error Control (HEC) mechanism as defined in ITU-T Rec. I.432.1.

9.6 Cell header verification and extraction

The cell header verification shall be performed in compliance with ITU-T Rec. I.432.1. All the physical layer cells shall be extracted and only the valid cells are passed to the ATM layer.

9.7 Physical layer OAM

The OAM functionality is performed using the overhead bytes defined in ITU-T Rec. G.832.

Annex A

Transport of AAL2 CPS-packets in 2048 kbit/s frames

A.1 General

Clause 3 defines the mapping of ATM cells into 2048 kbit/s G.704 frames. When the ATM cells are carrying AAL2 CPS-packets, the utilization of the following method may provide bandwidth savings. The specified method is related to 2048 kbit/s PDH frames and it is provided as an option.

The AAL2 Common Part Sublayer (CPS) is specified in ITU-T Rec. I.363.2, in particular, the format and coding of the CPS PDU is described in 9.2/I.363.2.

A.2 Description of the method for transporting AAL2 channels in 2048 kbit/s frames

The header of the ATM cells carrying AAL2 CPS-packets is not transported. In addition, their Start Field and the pad are not transported either. AAL2 CPS-packets are kept unchanged and are directly inserted in G.704 frames. A dedicated field called Synchronization Field (SYF) is inserted in the first time slot (TS) of each G.704 frame to perform AAL2 CPS-packet delineation and channel identification.

– For AAL2 CPS-packet delineation a pointer is used. The pointer field (PTR) is 5-bit long. The pointer value represents the number of octets between the SYF and the first octet of the AAL2 CPS-packet.
– The remaining 3 bits of the SYF are used for channel identification. The utilization of the Channel Identification Field (CIF) is described in clause A.5.

The format of the SYF is given in Figure A.1.

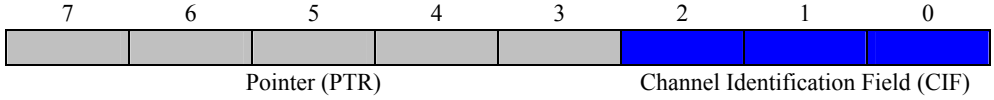

Figure A.1/G.804 – Format of the Synchronization Field (SYF)

For the coding of the pointer field, the following rules apply:

– In the case where the G.704 frame contains no AAL2 CPS-packet, the value 31 is allocated to the pointer.

– In the case where the G.704 frame only contains the remaining part of an AAL2 CPS-packet which has started in the previous G.704 frame, the value 30 is allocated to the pointer.

AAL2 CPS-packets are consecutively concatenated in G.704 frames. A mapping example is depicted in Figure A.2 (only useful TS are represented, i.e., TS 0 and TS 16 have been omitted in the figure). TS 1 contains the SYF (only the Pointer Field value is represented in the figure). It is pointed out that some frames may be empty (E) because no AAL2 CPS-packet has to be inserted. In that case, the next AAL2 CPS-packet to be transported is inserted at the beginning of the next frame, therefore, the value 0 is inserted in the corresponding Pointer Field (see for example frame n+7). The number of empty octets is variable depending on traffic conditions.

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	TS number
2																														frame n
13																														frame n+1
28																														frame n+2
15																E	E	E	E	E	E	E	E	E	E	E	E	E	E	frame n+3
0																														frame n+4
19																				E	E	E	E	E	E	E	E	E	E	frame n+5
31	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	frame n+6
0																														frame n+7
30																														frame n+8
2			E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	frame n+9

Format of the AAL2 CPS-packet:

3 octets	1 to 45 octets
CPS-Packet Header	CPS-Packet Payload

Figure A.2/G.804 – Transport of AAL2 CPS-packets in G.704 2048 kbit/s frames

A.3 Scrambling of the AAL2 CPS-packets

In line with 3.4, AAL2 CPS-packets shall be scrambled before mapping into the 2048 kbit/s signal.

A.4 N × 64 kbit/s case

The same method is also applicable to the case where N × 64 kbit/s frames are utilized (with N < 30). In addition, TS allocated for the transport of ATM cells may be divided in several groups. When more than one N × 64 kbit/s group is utilized, only one SYF is used, and it is inserted in the first octet of the first N × 64 kbit/s group.

As an example for illustrating this rule, Figure A.3 depicts the case where two TS groups from the G.704 2048 kbit/s framing are utilized:

– 14 × 64 kbit/s from TS 3 to TS 16

– 4 × 64 kbit/s from TS 21 to TS 24

TS 3 contains the SYF (only the Pointer Field value is represented in the figure).

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	TS number
		1	2	3	4	5	6	7	8	9	10	11	12	13	14					15	16	17	18							Utilized TS number
		2																												Frame n
		30																												Frame n+1
		1																												Frame n+2
		11																												Frame n+3
		14																			E	E	E							Frame n+4
		31	E	E	E	E	E	E	E	E	E	E	E	E	E					E	E	E	E							Frame n+5
		0																												Frame n+6
		11												E	E					E	E	E	E							Frame n+7

Figure A.3/G.804 – Utilization of N × 64 kbit/s framing (N < 30)

A.5 Utilization of the Channel Identification Field (CIF)

The 3-bit Channel Identification Field (CIF) enables 8 different types of channels to be addressed in 2048 kbit/s frames. Addressing capabilities of the CIF perform two functions:

– to solve conflicts between AAL2 CPS-packet CID numbers in the case where more than one VC carrying AAL2 channels have to be transported;

– to allow the transport of composite flows, i.e., ATM and AAL2 flows can be transported simultaneously.

The AAL2 CPS packet header contains an 8-bit Channel Identifier (CID) used for identifying an AAL2 channel. CID number conflicts may appear as soon as AAL2 channels belonging to several ATM VCs are mapped in the same 2048 kbit/s frame. The CIF enables the identification of different VCs when AAL2 channels to be transported in 2048 kbit/s frames belong to more than one ATM VC.

In addition, systems based on this Recommendation may carry all ATM traffic types: AAL1, AAL5 and AAL2, i.e., composite ATM traffic. Addressing capabilities of the CIF enable it to carry composite ATM traffic. CIF values permit the distinguishing of cell flows and mini-cell flows in each frame. Only one value of CIF is necessary to address ATM cell flow, whereas more than one CIF value may be allocated to AAL2 CPS-packet flows if AAL2 CPS-packets belong to more than one VC.

The value 0 of CIF is reserved to frames which contain no beginning of ATM cell or of AAL2 CPS-packet (i.e., this includes empty frames). Therefore, up to seven CIF values are available.

A limitation of the method is that it is possible to carry both an ATM cell and an AAL2 CPS-packet in the same frame, only if the first octet of their header is not located in the same frame. Whenever this happens, the introduction of the second occurrence has to be delayed until the beginning of the next frame.

Figure A.4 illustrates the combined transport of ATM cells and AAL2 CPS-packets. In this example, CIF value 0 has been allocated to empty traffic, CIF value 7 has been allocated to pure ATM traffic, and CIF values 1, 2, 3 and 4 have been allocated to four different ATM VC numbers carrying AAL2 traffic.

1		2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	TS number
2	**1**										Mini-cell (a)																				Frame n
13	**2**																				Mini-cell (b)										Frame n+1
28	**1**																														Frame n+2
15	**0**							Mini-cell (c)									E	E	E	E	E	E	E	E	E	E	E	E	E	E	Frame n+3
31	**0**	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	Frame n+4
0	**7**	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	Frame n+5
24	**0**	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	E	E	E	E	E	Frame n+6
0	**1**															Mini-cell (d)															Frame n+7
5	**3**															Mini-cell (e)															Frame n+8
30	**3**																				Mini-cell (f)										Frame n+9
21	**7**																						1	2	3	4	5	6	7	8	Frame n+10
30	**7**	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	Frame n+11
16	**4**	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53														Frame n+12
25	**0**				Mini-cell (g)																						E	E	E	E	Frame n+13
31	**0**	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	Frame n+14
PTR	**CIF**																														
SYF																															

Figure A.4/G.804 – Combined transport of ATM cells and AAL2 CPS-packets in 2048 kbit/s frames

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