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ITU-T G.707/Y.1322

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TELECOMMUNICATION
STANDARDIZATION SECTOR
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Internet protocol aspects – Transport

Network node interface for the synchronous digital hierarchy (SDH)

ITU-T Recommendation G.707/Y.1322

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ITU-T Recommendation G.707/Y.1322

Network node interface for the synchronous digital hierarchy (SDH)

Summary

This Recommendation provides the requirements for the STM-N signals at the network node interface of a synchronous digital network, including B-ISDN in terms of:

– bit rates;

– frames structures;

– formats for mapping and multiplexing of client signals (e.g., PDH, ATM and Ethernet) elements;

– functionalities of the overheads.

Revision 7.0 of ITU-T Recommendation G.707/Y.1322 is based on:

• revision 6.0 approved 2003-12-14;

• Corrigendum 1 approved 2004-06-13;

• Amendment 1 approved 2004-08-22;

• Corrigendum 2 approved 2005-08-22; and

• editorial (non-technical) corrections.

Amendment 1 provides a reciprocal linkage from the SDH Recommendation to the G-PON Recommendation G.984.3, and explains how the G-PON encapsulation method (GEM) transport of SDH signals fits into the multiplexing hierarchy.

Source

ITU-T Recommendation G.707/Y.1322 was approved on 9 January 2007 by ITU-T Study Group 15 (2005-2008) under the ITU-T Recommendation A.8 procedure, including Amendment 1 to ITU-T Recommendation G.707/Y.1322 (2007), which was approved on 29 July 2007 by ITU-T Study Group 15 (2005-2008) under the ITU-T Recommendation A.8 procedure.

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FOREWORD

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As of the date of approval of this Recommendation, ITU had received notice of intellectual property, protected by patents, which may be required to implement this Recommendation. However, implementers are cautioned that this may not represent the latest information and are therefore strongly urged to consult the TSB patent database at http://www.itu.int/ITU-T/ipr/.

CONTENTS

ITU-T Recommendation G.707/Y.1322

Network node interface for the synchronous digital hierarchy (SDH)

1 Scope

This Recommendation covers the network node interface (NNI) specifications which are necessary to enable interconnection of network elements at their synchronous digital hierarchy (SDH) interfaces for the transport of different types of payloads.

Therefore, this Recommendation specifies:

– the bit rates for STM-N signals;

– the frames structures for STM-N signals;

– the formats for mapping and multiplexing of client signals (e.g., PDH, ATM and Ethernet) elements into an STM-N frame;

– the functionalities to be implemented in the different overheads of an STM-N frame;

at the NNI of a synchronous digital network, including B-ISDN.

2 References

The following ITU-T Recommendations and other references contain provisions which, through reference in this text, constitute provisions of this Recommendation. At the time of publication, the editions indicated were valid. All Recommendations and other references are subject to revision; users of this Recommendation are therefore encouraged to investigate the possibility of applying the most recent edition of the Recommendations and other references listed below. A list of the currently valid ITU-T Recommendations is regularly published. The reference to a document within this Recommendation does not give it, as a stand-alone document, the status of a Recommendation.

– ITU-T Recommendation G.691 (2006), *Optical interfaces for single-channel STM-64 and other SDH systems with optical amplifiers*.

– ITU-T Recommendation G.702 (1988), *Digital hierarchy bit rates*.

– ITU-T Recommendation G.703 (2001), *Physical/electrical characteristics of hierarchical digital interfaces*.

– ITU-T Recommendation G.704 (1998), *Synchronous frame structures used at 1544, 6312, 2048, 8448 and 44 736 kbit/s hierarchical levels*.

– ITU-T Recommendation G.709/Y.1331 (2003), *Interfaces for the Optical Transport Network (OTN)*.

– ITU-T Recommendation G.780/Y.1351 (2004), *Terms and definitions for synchronous digital hierarchy (SDH) networks*.

– ITU-T Recommendation G.783 (2006), *Characteristics of synchronous digital hierarchy (SDH) equipment functional blocks*.

– ITU-T Recommendation G.7041/Y.1303 (2005), *Generic framing procedure* (*GFP*).

– ITU-T Recommendation G.7042/Y.1305 (2006), *Link capacity adjustment scheme (LCAS) for virtual concatenated signals*.

– ITU-T Recommendation G.802 (1988), *Interworking between networks based on different digital hierarchies and speech encoding laws*.

– ITU-T Recommendation G.803 (2000), *Architecture of transport networks based on the synchronous digital hierarchy (SDH)*.

– ITU-T Recommendation G.806 (2006), *Characteristics of transport equipment – Description methodology and generic functionality*.

– ITU-T Recommendation G.831 (2000), *Management capabilities of transport networks based on the synchronous digital hierarchy (SDH).*

– ITU-T Recommendation G.841 (1998), *Types and characteristics of SDH network protection architectures*.

– ITU-T Recommendation G.957 (2006), *Optical interfaces for equipments and systems relating to the synchronous digital hierarchy*.

– ITU-T Recommendation G.984.3 (2004), *Gigabit-capable Passive Optical Networks (G-PON): Transmission convergence layer specifications.*

– ITU-T Recommendation G.991.2 (2003), *Single-pair high-speed digital subscriber line (SHDSL) transceivers.*

– ITU-T Recommendation I.432.1 (1999), *B-ISDN user-network interface – Physical layer specification: General characteristics*.

– ITU-T Recommendation I.432.2 (1999), *B-ISDN user-network interface – Physical layer specification: 155 520 kbit/s and 622 080 kbit/s operation*.

– ITU-T Recommendation O.181 (2002), *Equipment to assess error performance on STM-N interfaces*.

– ITU-T Recommendation Q.921 (1997), *ISDN user-network interface – Data link layer specification.*

– ITU-R Recommendation F.750-4 (2000), *Architectures and functional aspects of radio-relay systems for synchronous digital hierarchy (SDH)-based networks*.

– ITU-R Recommendation S.1149-2 (2005), *Network architecture and equipment functional aspects of digital satellite systems in the fixed-satellite service forming part of synchronous digital hierarchy transport networks*.

– ETSI ETS 300 216 (1992), *Network Aspects (NA); Metropolitan Area Network (MAN); Physical layer convergence procedure for 155,520 Mbit/s.*

– IEEE Standard 802.3 (2005), *Information technology – Telecommunications and information exchange between systems – Local and metropolitan area networks – Specific requirements Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications Amendment: Media Access Control (MAC) Parameters, Physical Layers, and Management Parameters for 10 Gb/s Operation.*

3 Terms and definitions

3.1 Terms defined elsewhere

This Recommendation uses the following terms defined elsewhere:

3.1.1 synchronous digital hierarchy (SDH): See ITU-T Rec. G.780/Y.1351.

3.1.2 synchronous transport module (STM): See ITU-T Rec. G.780/Y.1351.

3.1.3 virtual container-n (VC-n): See ITU-T Rec. G.780/Y.1351.

3.1.4 administrative unit-n (AU-n): See ITU-T Rec. G.780/Y.1351.

3.1.5 tributary unit-n (TU-n): See ITU-T Rec. G.780/Y.1351.

3.1.6 container-n (n=11, 12, 2, 3, 4): See ITU-T Rec. G.780/Y.1351.

3.1.7 network node interface (NNI): See ITU-T Rec. G.780/Y.1351.

Figure 3-1 gives a possible network configuration to illustrate the location of NNI specified in this Recommendation.

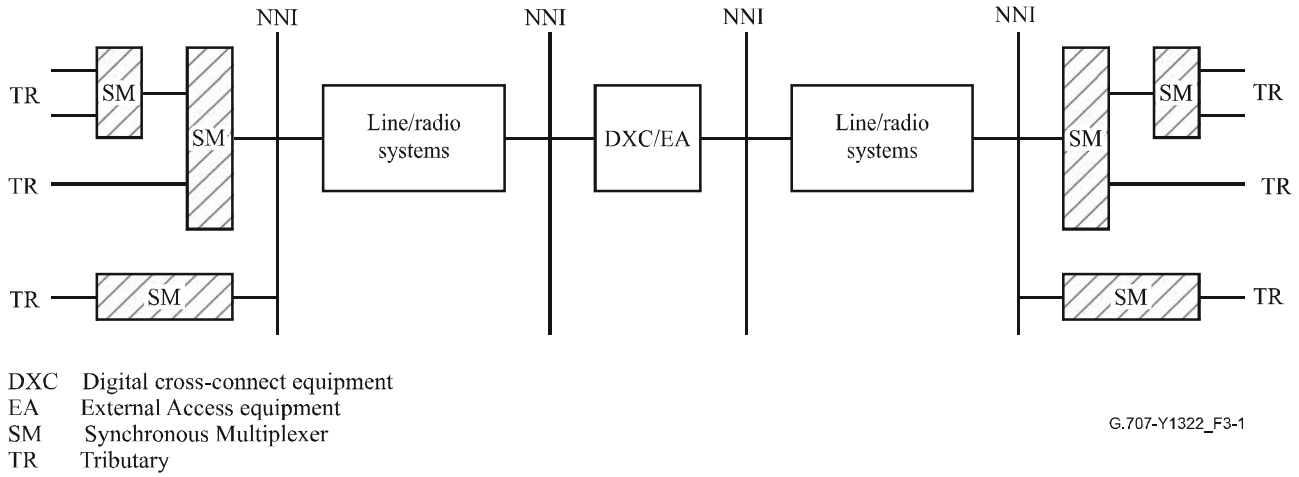


Figure 3-1 – Location of the NNI

3.1.8 pointer: See ITU-T Rec. G.780/Y.1351.

3.1.9 administrative unit group (AUG): See ITU-T Rec. G.780/Y.1351.

3.1.10 SDH mapping: See ITU-T Rec. G.780/Y.1351.

3.1.11 SDH multiplexing: See ITU-T Rec. G.780/Y.1351.

3.1.12 SDH aligning: See ITU-T Rec. G.780/Y.1351.

3.1.13 Bit Interleaved Parity-X (BIP-X): See ITU-T Rec. G.780/Y.1351.

3.1.14 concatenation: See ITU-T Rec. G.780/Y.1351.

3.1.15 shortened binary-BCH: See ITU-T Rec. G.780/Y.1351.

3.1.16 generator polynomial: See ITU-T Rec. G.780/Y.1351.

3.1.17 systematic code: ITU-T Rec. G.780/Y.1351.

3.1.18 tributary unit group (TUG): See ITU-T Rec. G.780/Y.1351.

3.1.19 dSTM-12*NMi* interface: See ITU-T Rec. G.780/Y.1351.

3.2 Terms defined in this Recommendation

This Recommendation defines the following terms:

3.2.1 gSTM-11 interface: An SDH transmission interface which transports one TU-11, with G-PON based Section overhead. gSTM-11 interfaces are defined for G-PON transport technologies. Refer to Table H.1.

3.2.2 gSTM-12 interface: An SDH transmission interface which transports one TU-12, with G-PON based Section overhead. gSTM-12 interfaces are defined for G-PON transport technologies. Refer to Table H.1.

3.2.3 gSTM-2 interface: An SDH transmission interface which transports one TU-2, with G-PON based Section overhead. gSTM-2 interfaces are defined for G-PON transport technologies. Refer to Table H.1.

3.2.4 gSTM-3 interface: An SDH transmission interface which transports one TU-3, with G-PON based Section overhead. gSTM-3 interfaces are defined for G-PON transport technologies. Refer to Table H.1.

4 Acronyms and abbreviations

This Recommendation uses the following abbreviations:

AIS	Alarm Indication Signal
API	Access Point Identifier
APS	Automatic Protection Switching
ATM	Asynchronous Transfer Mode
AU-n	Administrative Unit-n
AUG-N	Administrative Unit Group-N
BCH	Bose-Chaudhuri-Hocquenghem
BCH-3	Triple error correcting BCH code
BER	Bit Error Ratio
BIP-X	Bit Interleaved Parity-X
C-n	Container-n
CAS	Channel Associated Signalling
CRC-N	Cyclic Redundancy Check, width N
CTRL	Control word sent from source to sink
DCC	Data Communication Channel
DQDB	Distributed Queue Dual Bus
DNU	Do Not Use
dSTM	SHDSL based Synchronous Transport Module
EOS	End of Sequence
FCS	Frame Check Sequence
FDDI	Fibre Distributed Data Interface
FEBE	Far End Block Error (renamed as REI)
FEC	Forward Error Correction
FERF	Far End Receive Failure (renamed as RDI)
FSI	FEC Status Indication
GEM	G-PON Encapsulation Method
GID	Group Identification
gSTM	GEM based Synchronous Transport Mode
HDLC	High-level Data Link Control
HEC	Header Error Control
HOVC	Higher Order Virtual Container
IEC	Incoming Error Count

IP	Internet Protocol
ISF	Incoming Signal Failure
ISDN	Integrated Services Digital Network
ISID	Idle Signal Identification
LAPD	Link Access Protocol for D-channel
LAPS	Link Access Procedure – SDH
LCAS	Link Capacity Adjustment Scheme
LCD	Loss of Cell Delineation
LOP	Loss of Pointer
LOVC	Lower Order Virtual Container
LSB	Least Significant Bit
MAN	Metropolitan Area Network
MFI	MultiFrame Indicator
MSB	Most Significant Bit
MS-AIS	Multiplex Section Alarm Indication Signal
MSF-AIS	Multiplex Section FEC Alarm Indication Signal
MSOH	Multiplex Section Overhead
MS-RDI	Multiplex Section Remote Defect Indication
MS-REI	Multiplex Section Remote Error Indication
MST	Member Status
MSTE	Multiplex Section Terminating Element
NDF	New Data Flag
NNI	Network Node Interface
NORM	Normal Operating Mode
ODI	Outgoing Defect Indication
ODUk	Optical channel Data Unit-k
OEI	Outgoing Error Indication
OH	Overhead
OPUk	Optical channel Payload Unit-k
OTN	Optical Transport Network
OTUk	Optical channel Transport Unit-k
PDH	Plesiochronous Digital Hierarchy
PLM	Payload Mismatch
POH	Path Overhead
PPP	Point-to-Point Protocol
PTE	Path Terminating Element
PTR	Pointer

RDI	Remote Defect Indication (former FERF)
REI	Remote Error Indication (former FEBE)
RFI	Remote Failure Indication
RS-Ack	Re-sequence Acknowledge
RSOH	Regenerator Section Overhead
SD	Signal Degrade
SDH	Synchronous Digital Hierarchy
SLM	Signal Label Mismatch
SOH	Section Overhead
SQ	Sequence Indicator
SSU	Synchronization Supply Unit
STM(-N)	Synchronous Transport Module (-N)
TCM	Tandem Connection Monitoring
TC-RDI	Tandem Connection Remote Defect Indication
TC-REI	Tandem Connection Remote Error Indication
TCOH	Tandem Connection Overhead
TCT	Tandem Connection Trace
TCTE	Tandem Connection Terminating Element
TIM	Trace Identifier Mismatch
TSID	Test Signal Identification
TTI	Trail Trace Identifier
TU-n	Tributary Unit-n
TUG(-n)	Tributary Unit Group (-n)
UNEQ	UNEQuipped
VC-n	Virtual Container-n
VC-n-X	X concatenated Virtual Container-ns
VC-n-Xc	X Contiguously concatenated VC-ns
VC-n-Xv	X Virtually concatenated VC-ns
VCG	Virtual Concatenation Group
WAN	Wide Area Network

5 Conventions

The order of transmission of information in all the figures in this Recommendation is first from left to right and then from top to bottom. Within each byte, the most significant bit is transmitted first. The most significant bit (bit 1) is illustrated at the left in all the figures.

6 Basic multiplexing principles

6.1 Multiplexing structure

Figure 6-1 shows the relationship between various multiplexing elements that are defined in Table 6-1, and illustrates possible multiplexing structures.

Figures 6-2, 6-3, 6-4 and 6-5 show how various signals are multiplexed using these multiplexing elements.

Details of the multiplexing method and mappings are given in clauses 7 and 10.

Descriptions of the various multiplexing elements are given in clauses 8 to 10.

Descriptions of the various concatenations are given in clause 11.

NOTE – High rate VC-4-Xc could be used without any constraints in point-to-point connections. SDH networks may be limited to a certain bit rate of VC-4-Xc (e.g., X ≤ 64), e.g., due to rings with MS SPRING that has to reserve 50% of the STM-N bandwidth for protection.

Table 6-1 – VC types and capacity

VC type	VC bandwidth	VC payload
VC-11	1 664 kbit/s	1 600 kbit/s
VC-12	2 240 kbit/s	2 176 kbit/s
VC-2	6 848 kbit/s	6 784 kbit/s
VC-3	48 960 kbit/s	48 384 kbit/s
VC-4	150 336 kbit/s	149 760 kbit/s
VC-4-4c	601 344 kbit/s	599 040 kbit/s
VC-4-16c	2 405 376 kbit/s	2 396 160 kbit/s
VC-4-64c	9 621 504 kbit/s	9 584 640 kbit/s
VC-4-256c	38 486 016 kbit/s	38 338 560 kbit/s

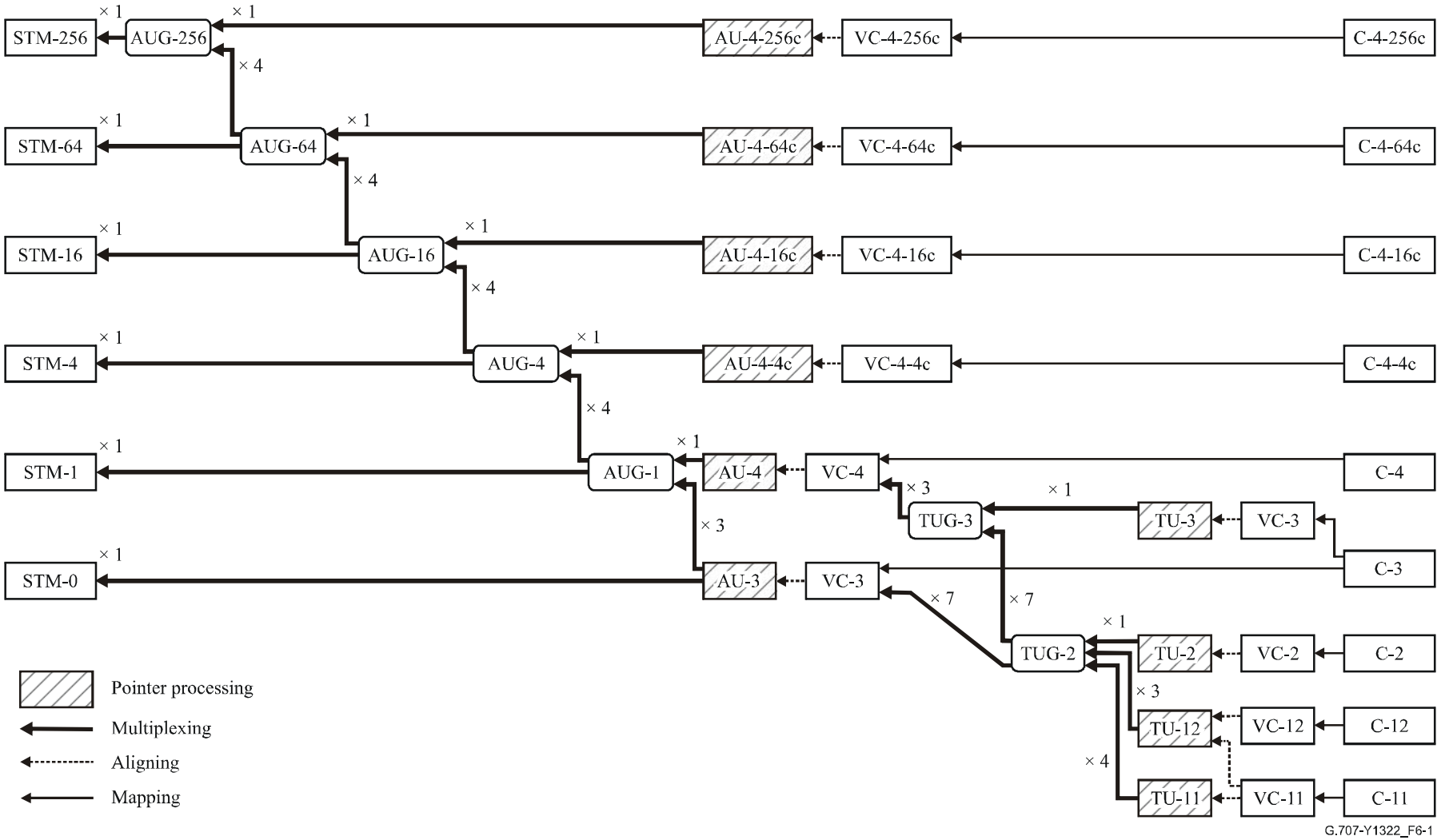
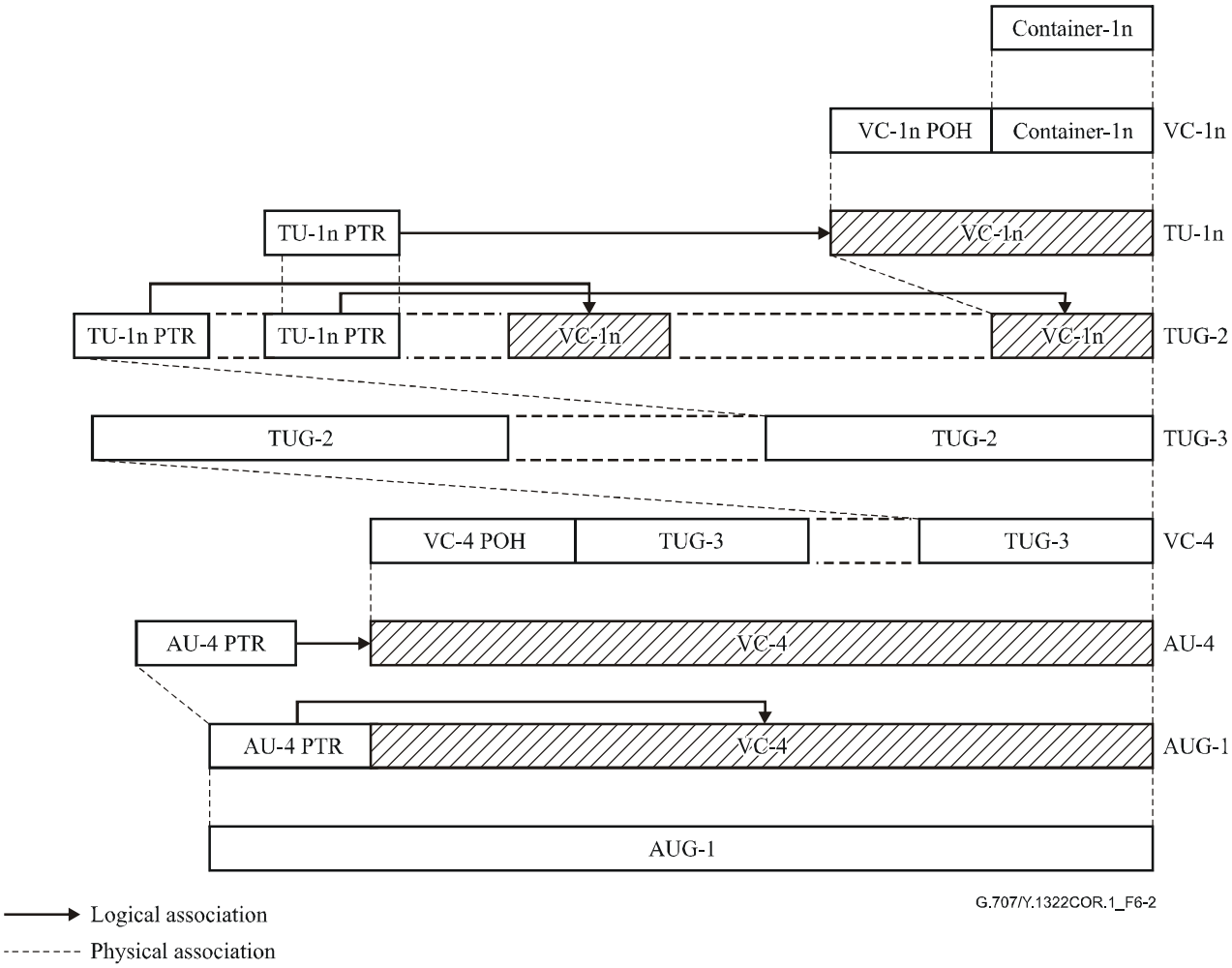
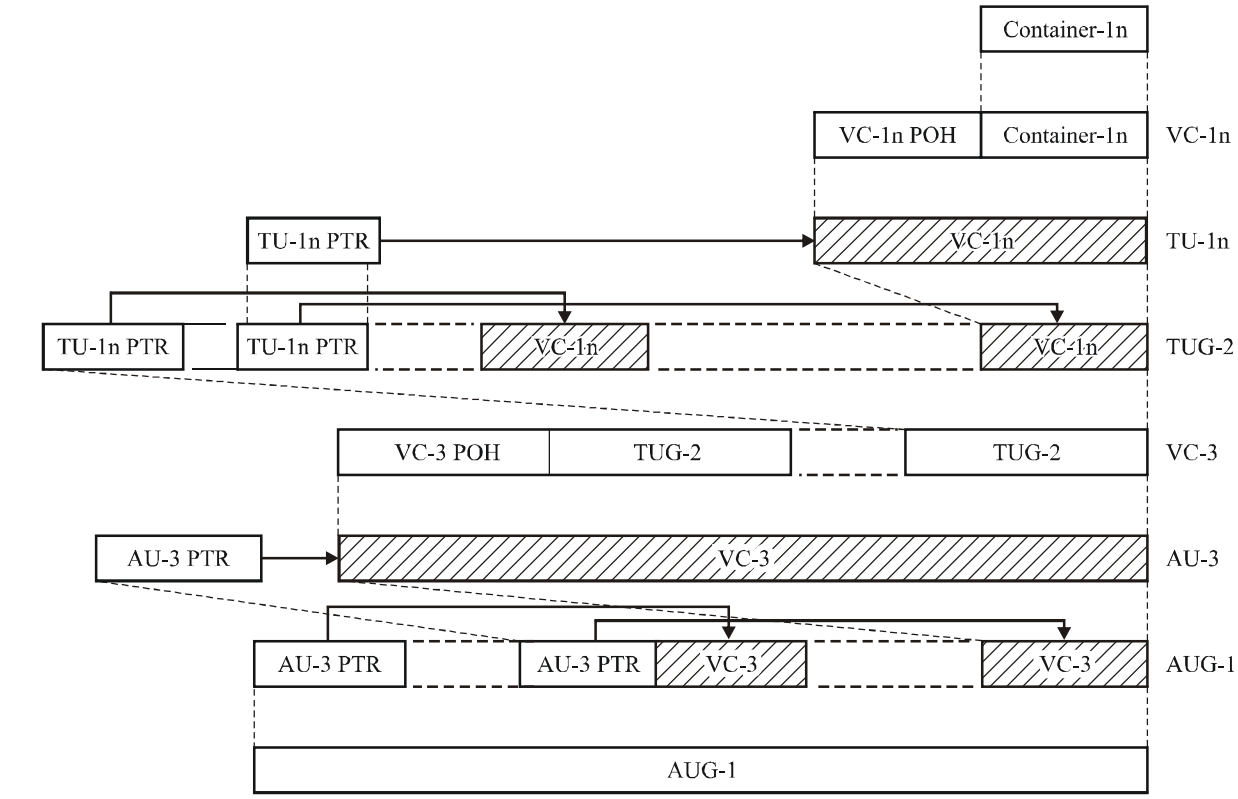


Figure 6-1 – Multiplexing structure



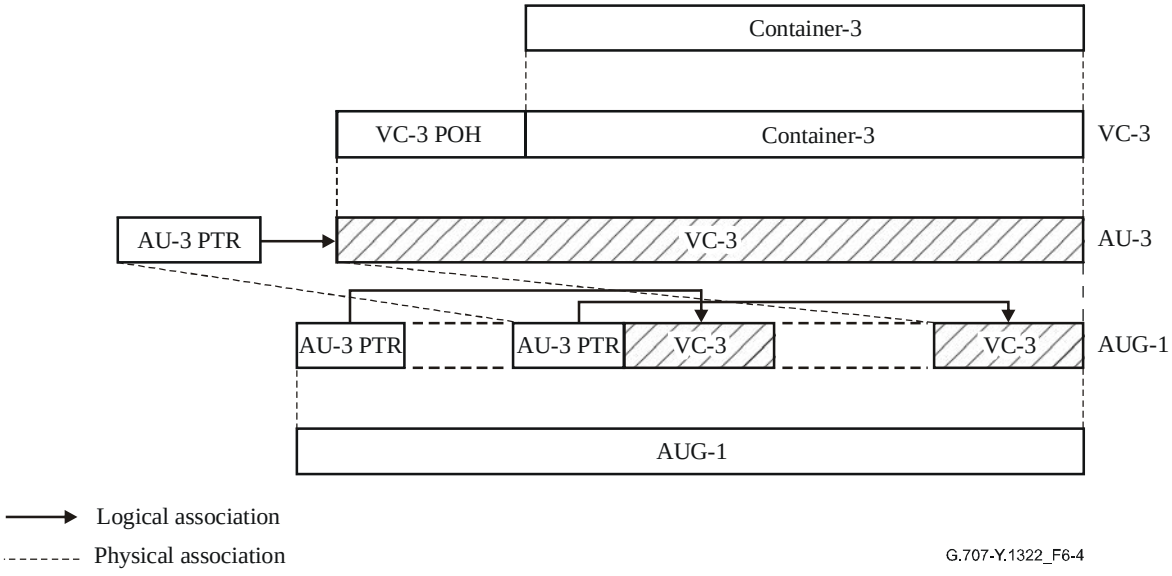
NOTE 1 – Unshaded areas are phase aligned. Phase alignment between the unshaded and shaded areas is defined by the pointer (PTR) and is indicated by the arrow.
NOTE 2 – n = 1, 2.

Figure 6-2 – Multiplexing method directly from container-11/container-12 using AU-4



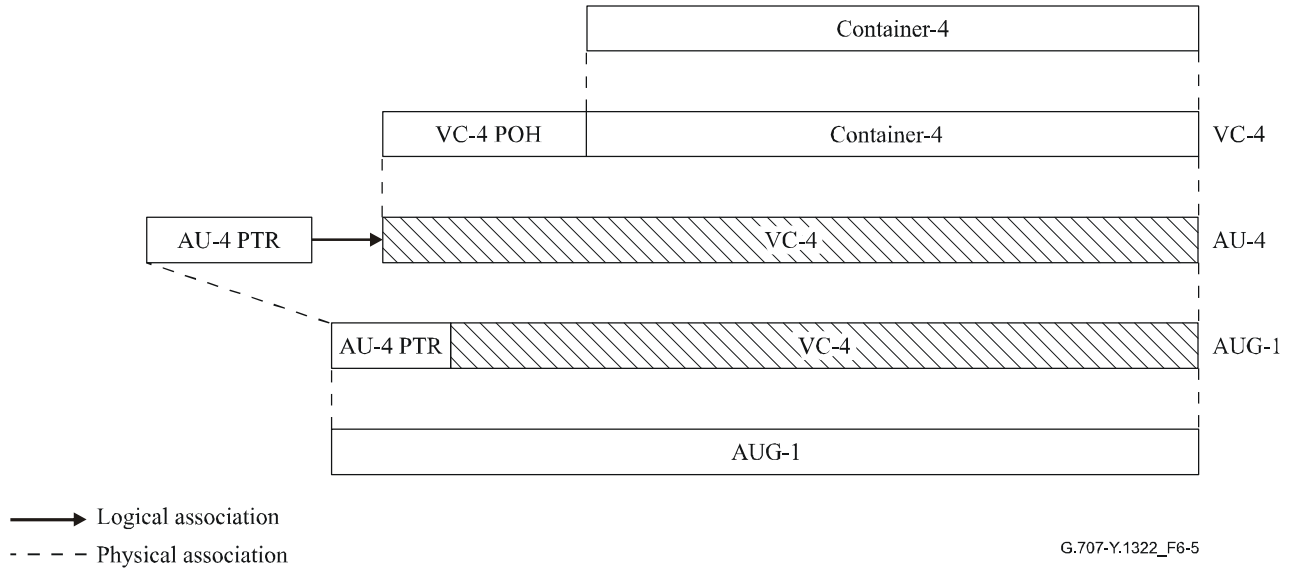
NOTE 1 – Unshaded areas are phase aligned. Phase alignment between the unshaded and shaded areas is defined by the pointer (PTR) and is indicated by the arrow.
NOTE 2 – n = 1, 2.

Figure 6-3 – Multiplexing method directly from container-11/container-12 using AU-3



NOTE – Unshaded areas are phase aligned. Phase alignment between the unshaded and shaded areas is defined by the pointer (PTR) and is indicated by the arrow.

Figure 6-4 – Multiplexing method directly from container-3 using AU-3



NOTE – Unshaded areas are phase aligned. Phase alignment between the unshaded and shaded areas is defined by the pointer (PTR) and is indicated by the arrow.

Figure 6-5 – Multiplexing method directly from container-4 using AU-4

6.2 Basic frame structure

STM-N frame structure is shown in Figure 6-6. The three main areas of the STM-N frame are indicated:

– SOH;

– Administrative unit pointer(s);

– Information payload.

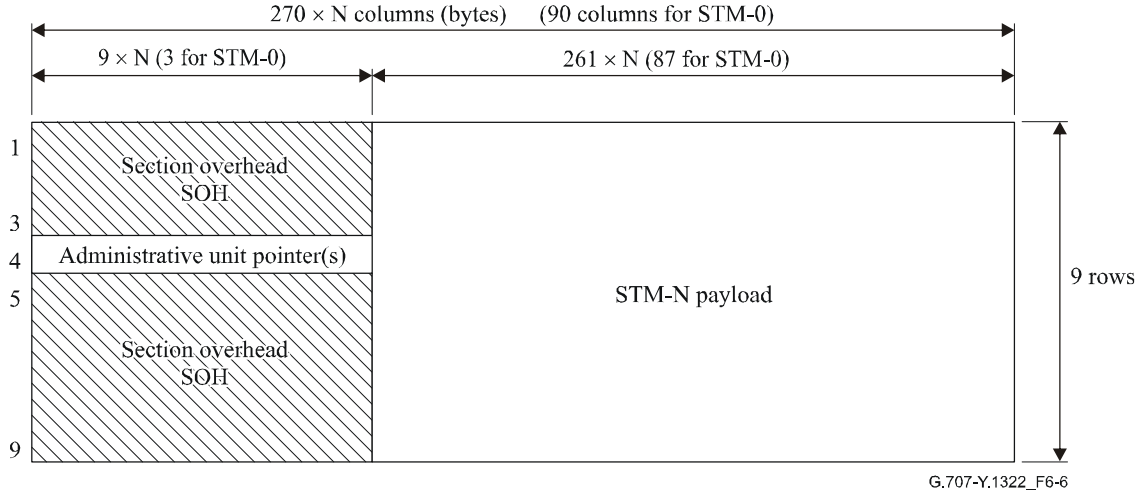


Figure 6-6 – STM-N frame structure

6.2.1 Section overhead

Rows 1-3 and 5-9 of columns 1 to 9 × N of the STM-N in Figure 6-6 are dedicated to the SOH.

The allocation of SOH capacity and an explanation of the overhead functions are given in clause 9.

6.2.2 Administrative unit pointers

Row 4 of columns 1 to 9 × N in Figure 6-6 is available for administrative unit pointers. The application of pointers and their detailed specifications are given in clause 8.

6.2.3 Administrative units in the STM-N

The STM-N payload supports one AUG-N where the:

a) AUG-256 may consist of:
   1) four AUG-64;
   2) one AU-4-256c.

b) AUG-64 may consist of:
   1) four AUG-16;
   2) one AU-4-64c.

c) AUG-16 may consist of:
   1) four AUG-4;
   2) one AU-4-16c.

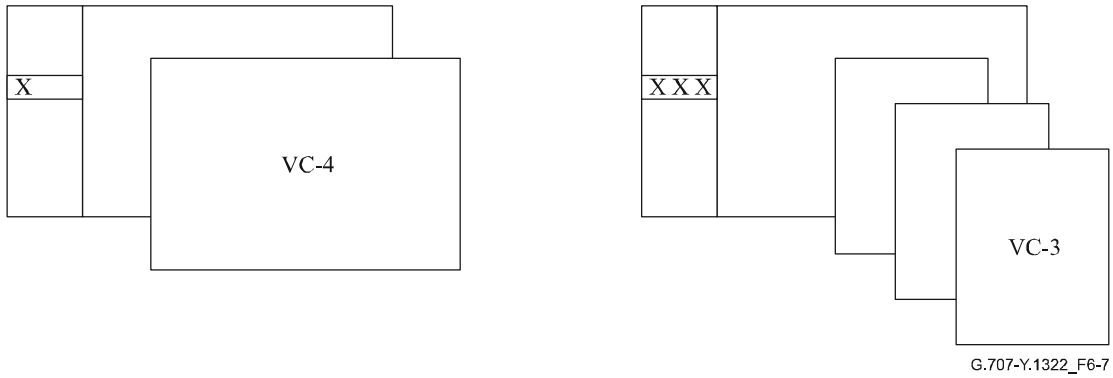
d) AUG-4 may consist of:
   1) four AUG-1;
   2) one AU-4-4c.

e) AUG-1 may consist of:
   1) one AU-4;
   2) three AU-3s.

The VC-n associated with each AU-n does not have a fixed phase with respect to the STM-N frame. The location of the first byte of the VC-n is indicated by the AU-n pointer. The AU-n pointer is in a fixed location in the STM-N frame. Examples are illustrated in Figures 6-2, 6-3, 6-4, 6-5, 6-6, 6-7 and 6-8.

The AU-4 may be used to carry, via the VC-4, a number of TU-ns (n=11, 12, 2, 3) forming a two-stage multiplex. An example of this arrangement is illustrated in Figures 6-7 a and 6-8 a. The VC-n associated with each TU-n does not have a fixed phase relationship with respect to the start of the VC-4. The TU-n pointer is in a fixed location in the VC-4 and the location of the first byte of the VC-n is indicated by the TU-n pointer.

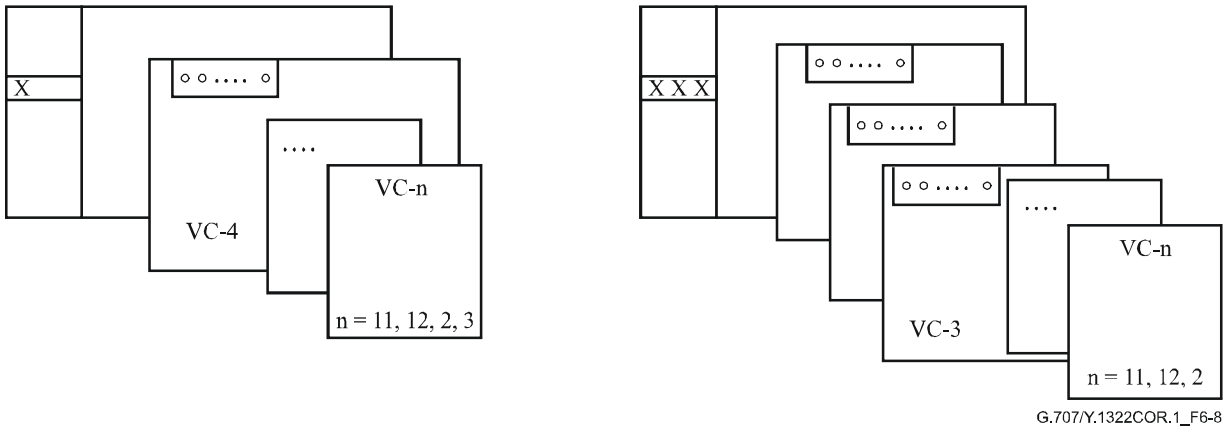
The AU-3 may be used to carry, via the VC-3, a number of TU-ns (n=11, 12, 2) forming a two-stage multiplex. An example of this arrangement is illustrated in Figures 6-7 b and 6-8 b. The VC-n associated with each TU-n does not have a fixed phase relationship with respect to the start of the VC-3. The TU-n pointer is in a fixed location in the VC-3 and the location of the first byte of the VC-n is indicated by the TU-n pointer.



a) STM-1 with one AU-4 **b) STM-1 with three AU-3s**

X AU-n pointer
AU-n AU-n pointer + VC-n (see clause 8)

Figure 6-7 – Administrative units in STM-1 frame



a) STM-1 with one AU-4 containing TUs **b) STM-1 with three AU-3s containing TUs**

X AU-n pointer
o TU-n pointer
AU-n AU-n pointer + VC-n (see clause 8)
TU-n TU-n pointer + VC-n (see clause 8)

Figure 6-8 – Two-stage multiplex

6.2.4 Maintenance signals

6.2.4.1 Alarm indication signals

An alarm indication signal (AIS) is a signal sent downstream as an indication that an upstream defect has been detected.

6.2.4.1.1 MS-AIS

The multiplex section AIS (MS-AIS) is specified as all "1"s in the entire STM-N, excluding the STM-N RSOH.

6.2.4.1.2 MSF-AIS

The multiplex section FEC AIS (MSF-AIS) is specified as all "1"s in the entire STM-N, excluding the STM-N RSOH except P1 and Q1 bytes.

6.2.4.1.3 AU/TU-AIS

The administrative unit AIS (AU-AIS) is specified as all "1"s in the entire AU-n (n=3, 4, 4-Xc), including the AU-n pointer.

The tributary unit AIS (TU-AIS) is specified as all "1"s in the entire TU-n (n=11, 12, 2, 3), including the TU-n pointer.

6.2.4.1.4 VC-AIS

An AU/TU-AIS incoming to a tandem connection (TC) is translated into a virtual container AIS (VC-AIS) within the tandem connection because a valid AU-n/TU-n pointer is needed for tandem connection monitoring (TCM).

VC-n (n=3, 4, 4-Xc) AIS is specified as all "1"s in the entire VC-n with a valid network operator byte N1, supporting TCM functionality, and a valid error detection code in the B3 byte.

VC-m (m=11, 12, 2) AIS is specified as all "1"s in the entire VC-m with a valid network operator byte N2, supporting TCM functionality, and a valid error detection code in bits 1 and 2 of the V5 byte.

6.2.4.2 Unequipped VC-n/VC-m signal

6.2.4.2.1 Case of network supporting the transport of tandem connection signals

For the case of networks supporting the transport of tandem connection signals, the VC-n (n=3, 4) or VC-4-Xc unequipped signal is a signal having an all "0"s in the higher order virtual container path signal label byte (C2), the tandem connection monitoring byte (N1) and the path trace byte (J1), and a valid BIP-8 byte (B3). The virtual container payload and the remaining path overhead bytes are unspecified.

For the case of networks supporting the transport of tandem connection signals, the VC-m (m=11, 12, 2) unequipped signal is a signal having an all "0"s in the lower order virtual container path signal label (bits 5, 6, 7 of byte V5), the tandem connection monitoring byte (N2) and the path trace byte (J2), and a valid BIP-2 (bits 1, 2 of byte V5). The virtual container payload and the remaining path overhead bytes are unspecified.

These signals indicate to downstream transport processing functions (refer to ITU-T Rec. G.803) that the virtual container is unoccupied, not connected to a path termination source function. Additional information on the quality is only available by means of the BIP monitoring.

Within a tandem connection, an unequipped VC-n/VC-m signal generated before the tandem connection will have a valid (non all "0"s) tandem connection monitoring byte (N1, N2).

6.2.4.2.2 Case of network not supporting the transport of tandem connection signals

For the case of networks not supporting the transport of tandem connection signals, the VC-n (n=3, 4) or VC-4-Xc unequipped signal is a signal having an all "0"s in the higher order virtual container path signal label byte (C2) and the path trace byte (J1), and a valid BIP-8 byte (B3). The virtual container payload and the remaining path overhead bytes are unspecified.

For the case of networks not supporting the transport of tandem connection signals, the VC-m (m=11, 12, 2) unequipped signal is a signal having an all "0"s in the lower order virtual container path signal label (bits 5, 6, 7 of byte V5) and the path trace byte (J2), and a valid BIP-2 (bits 1, 2 of byte V5). The virtual container payload and the remaining path overhead bytes are unspecified.

6.2.4.3 Supervisory-unequipped VC-n/VC-m signal

6.2.4.3.1 Case of network supporting the transport of tandem connection signals

For the case of networks supporting the transport of tandem connection signals, the VC-n (n=3, 4) or VC-4-Xc supervisory-unequipped signal is a signal having an all "0"s in the higher order virtual

container path signal label byte (C2) and the tandem connection monitoring byte (N1), a valid BIP-8 byte (B3), a valid path trace identifier byte (J1), and a valid path status byte (G1). The virtual container payload is unspecified. The content of the remaining path overhead bytes F2, H4, F3 and K3 is for further study.

The VC-n (n=3, 4) supervisory-unequipped signal is an enhanced unequipped VC-n signal.

For the case of networks supporting the transport of tandem connection signals, the VC-m (m=11, 12, 2) supervisory-unequipped signal is a signal having an all "0"s in the lower order virtual container path signal label (bits 5, 6, 7 of byte V5) and the tandem connection monitoring byte (N2), a valid BIP-2 (bits 1, 2 of byte V5), a valid path trace byte (J2), and valid path status (bits 3 and 8 of byte V5). The virtual container payload is unspecified. The content of the remaining path overhead bytes/bits V5 bit 4 and K4 is for further study.

The VC-m (m=11, 12, 2) supervisory-unequipped signal is an enhanced unequipped VC-m signal.

These signals indicate to downstream transport processing functions (refer to ITU-T Rec. G.803) that the virtual container is unoccupied, and sourced by a supervisory generator. Additional information on quality, source and status of the connection is available by means of the bit error, path trace and path status indications.

Within a tandem connection, a supervisory-unequipped VC-n/VC-m signal generated before the tandem connection will have a valid (non all "0"s) tandem connection monitoring byte (N1, N2).

6.2.4.3.2 Case of network not supporting the transport of tandem connection signals

For the case of networks not supporting the transport of tandem connection signals, the VC-n (n=3, 4) or VC-4-Xc supervisory-unequipped signal is a signal having an all "0"s in the higher order virtual container path signal label byte (C2), a valid BIP-8 byte (B3), a valid path trace identifier byte (J1), and a valid path status byte (G1). The virtual container payload is unspecified. The content of the remaining path overhead bytes F2, H4, F3, K3 and N1 is for further study.

For the case of networks not supporting the transport of tandem connection signals, the VC-m (m=11, 12, 2) supervisory-unequipped signal is a signal having an all "0"s in the lower order virtual container path signal label (bits 5, 6, 7 of byte V5), a valid BIP-2 (bits 1, 2 of byte V5), a valid path trace byte (J2), and valid path status (bits 3 and 8 of byte V5). The virtual container payload is unspecified. The content of the remaining path overhead bytes/bits V5 bit 4, N2 and K4 is for further study.

6.3 Hierarchical bit rates

The zero level of the synchronous digital hierarchy shall be 51 840 kbit/s.

The first level of the synchronous digital hierarchy shall be 155 520 kbit/s.

Higher synchronous digital hierarchy bit rates shall be obtained as integer multiples of the first level bit rate and shall be denoted by the corresponding multiplication factor of the first level rate.

The bit rates listed in Table 6-2 constitute the synchronous digital hierarchy.

Table 6-2 – SDH hierarchical bit rates

Synchronous digital hierarchy level	Hierarchical bit rate (kbit/s)
0	51 840
1	155 520
4	622 080
16	2 488 320
64	9 953 280
256	39 813 120
NOTE – The specification of levels higher than 256 requires further study.	

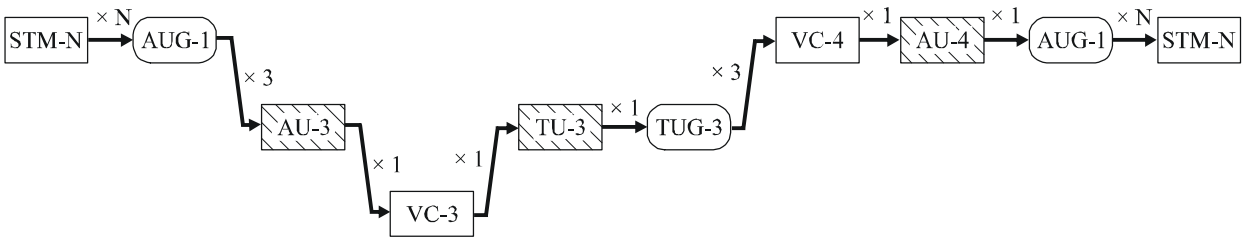
6.4 Interconnection of STM-Ns

The SDH is designed to be universal, allowing transport of a large variety of signals including all those specified in ITU-T Rec. G.702. However, different structures can be used for the transport of virtual containers. The following interconnection rules will be used:

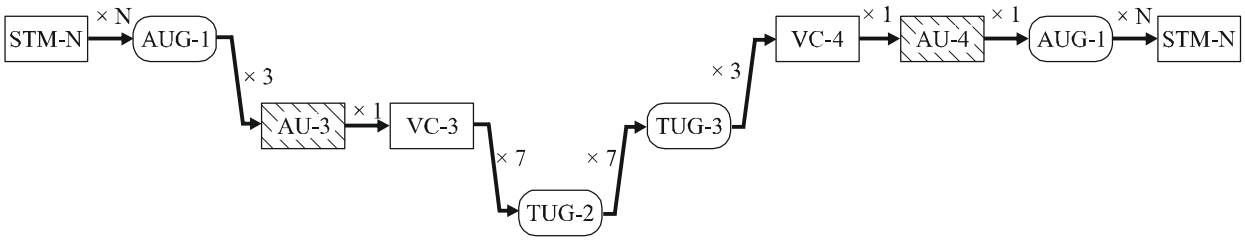
a) The rule for interconnecting two AUG-1s based upon two different types of administrative unit, namely AU-4 and AU-3, will be to use the AU-4 structure. Therefore, the AUG-1 based upon AU-3 will be demultiplexed to the VC-3 or TUG-2 level according to the type of the payload, and remultiplexed within an AUG-1 via the TUG-3/VC-4/AU-4 route. This is illustrated in Figures 6-9 a and 6-9 b.

b) The rule for interconnecting VC-11s transported via different types of tributary unit, namely TU-11 and TU-12, will be to use the TU-11 structure. This is illustrated in Figure 6-9 c. VC-11, TU-11 and TU-12 are described in the following clauses.

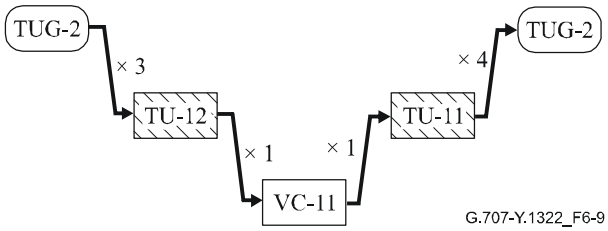
c) The rule for interconnecting concatenated VC-3s/4s transported via different types of concatenation, namely contiguous and virtual, will be to use the contiguous concatenation unless otherwise mutually agreed by the operators providing the transport.



a) Interconnection of VC-3 with C-3 payload



b) Interconnection of TUG-2



c) Interconnection of VC-11

Figure 6-9 – Interconnection of STM-Ns

This SDH interconnection rule does not modify the interworking rules defined in ITU-T Rec. G.802 for networks based upon different plesiochronous digital hierarchies and speech encoding laws.

6.5 Scrambling

The STM-N (N=0, 1, 4, 16, 64, 256) signal must have sufficient bit timing content at the NNI. A suitable bit pattern, which prevents a long sequence of "1"s or "0"s is provided by using a scrambler.

The STM-N (N=0, 1, 4, 16, 64, 256) signal shall be scrambled with a frame synchronous scrambler of sequence length 127 operating at the line rate.

The generating polynomial shall be $1 + X^6 + X^7$. Figure 6-10 gives a functional diagram of the frame synchronous scrambler.

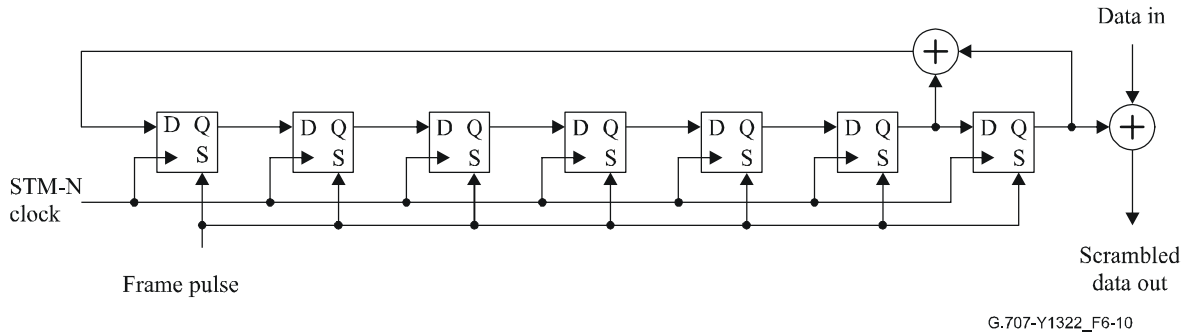


Figure 6-10 – Frame synchronous scrambler (functional diagram)

The scrambler shall be reset to "1111111" on the most significant bit of the byte following the last byte of the first row of the STM-N SOH S (1,9,N). This bit, and all subsequent bits to be scrambled shall be added modulo 2 to the output from the X^7 position of the scrambler. The scrambler shall run continuously throughout the complete STM-N frame.

The first row of the STM-N ($N \leq 64$) SOH ($9 \times N$ bytes, 3 bytes for STM-0, including the A1 and A2 framing bytes) shall not be scrambled.

NOTE 1 – Care should be taken in selecting the binary content of the Z0 bytes and of the bytes reserved for national use which are excluded from the scrambling process of the STM-N signal to ensure that long sequences of "1"s or "0"s do not occur.

For the first row of the STM-256 SOH bytes only S (1,3,193) [1,705] to S (1,4,64) [1,832] shall not be scrambled.

NOTE 2 – The scrambler shall continue to run during the above-mentioned frame positions.

NOTE 3 – Thus STM-256, SOH bytes S (1,1,1) [1,1] to S (1,3,192) [1,704] and S (1,4,65) [1,833] to S (1,9,256) [1,2304] shall be scrambled with the scrambler running from the reset in the previous STM-256 frame.

NOTE 4 – For the unused bytes in row 1 of the STM-256 frame, a pattern should be used that provides sufficient transitions and no significant DC unbalance after scrambling.

6.6 Physical specification of the NNI

Specifications for physical electrical characteristics of the NNI are contained in ITU-T Rec. G.703.

Specifications for physical optical characteristics of the NNI are contained in ITU-T Recs G.957 and G.691.

7 Multiplexing method

7.1 Multiplexing of administrative units into STM-N

7.1.1 Multiplexing of administrative unit groups (AUGs) into STM-N

7.1.1.1 Multiplexing of AUG-N into STM-N, N=(1, 4, 16, 64, 256)

The AUG-N is a structure of 9 rows by $N \times 261$ columns plus $N \times 9$ bytes in row 4 (for the AU-n pointers). The STM-N consists of an SOH as described in clause 9.2 and a structure of 9 rows by $N \times 261$ columns with $N \times 9$ bytes in row 4 (for the AU-n pointers). The AUG-N is multiplexed into this structure and has a fixed phase relationship with respect to the STM-N as shown in Figure 7-1.

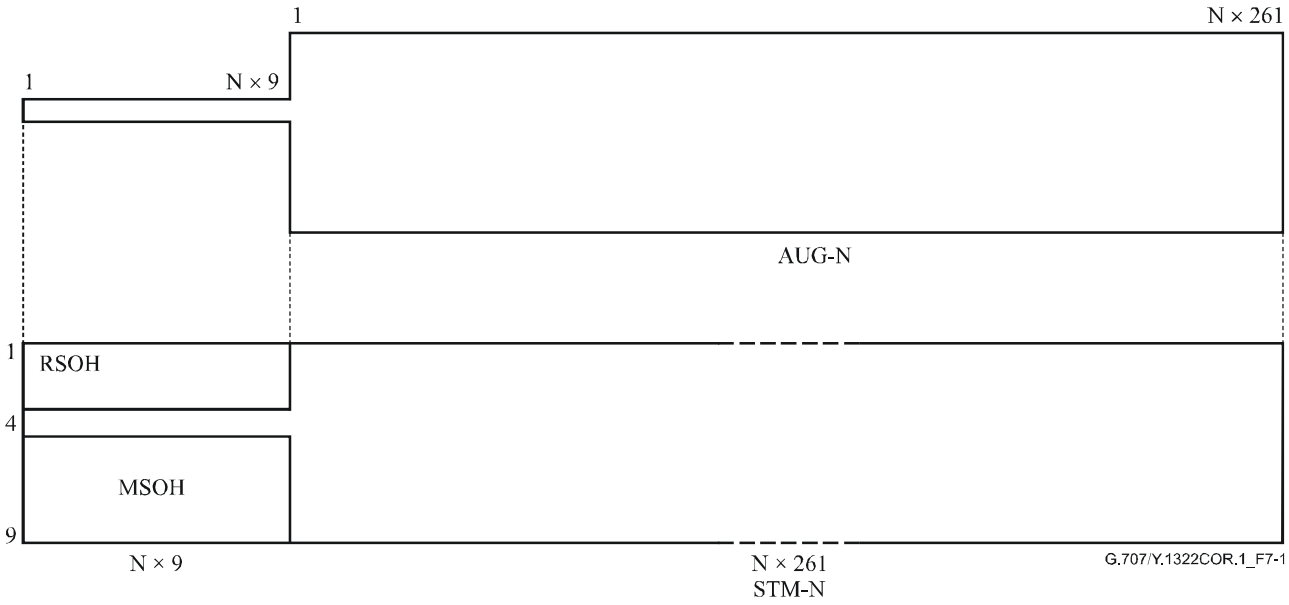


Figure 7-1 – Multiplexing of AUG-N into STM-N

7.1.1.2 Multiplexing of AUG-Ns into AUG-4×N

The arrangement of 4 AUG-Ns multiplexed into the AUG-4×N is shown in Figure 7-2. The AUG-N is a structure of 9 rows by N × 261 columns plus N × 9 bytes in row 4 (for the AU-n pointers). The 4 AUG-Ns are block interleaved into the AUG-4×N structure with a block length of N bytes. The AUG-Ns have a fixed phase relationship with respect to the AUG-4×N.

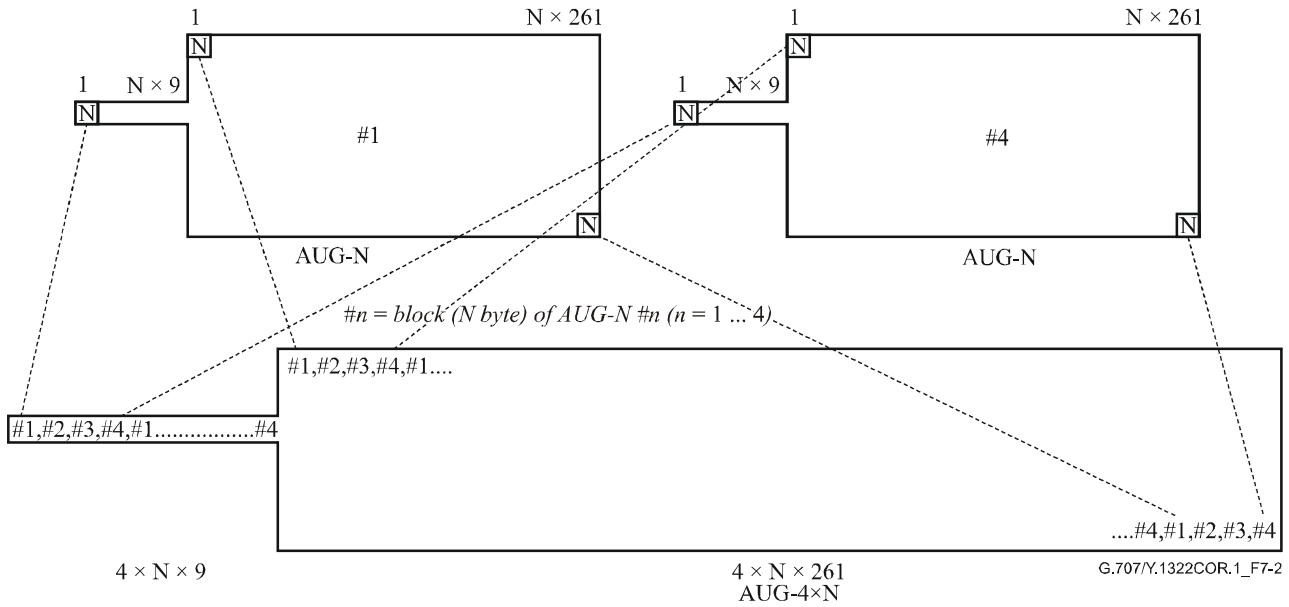
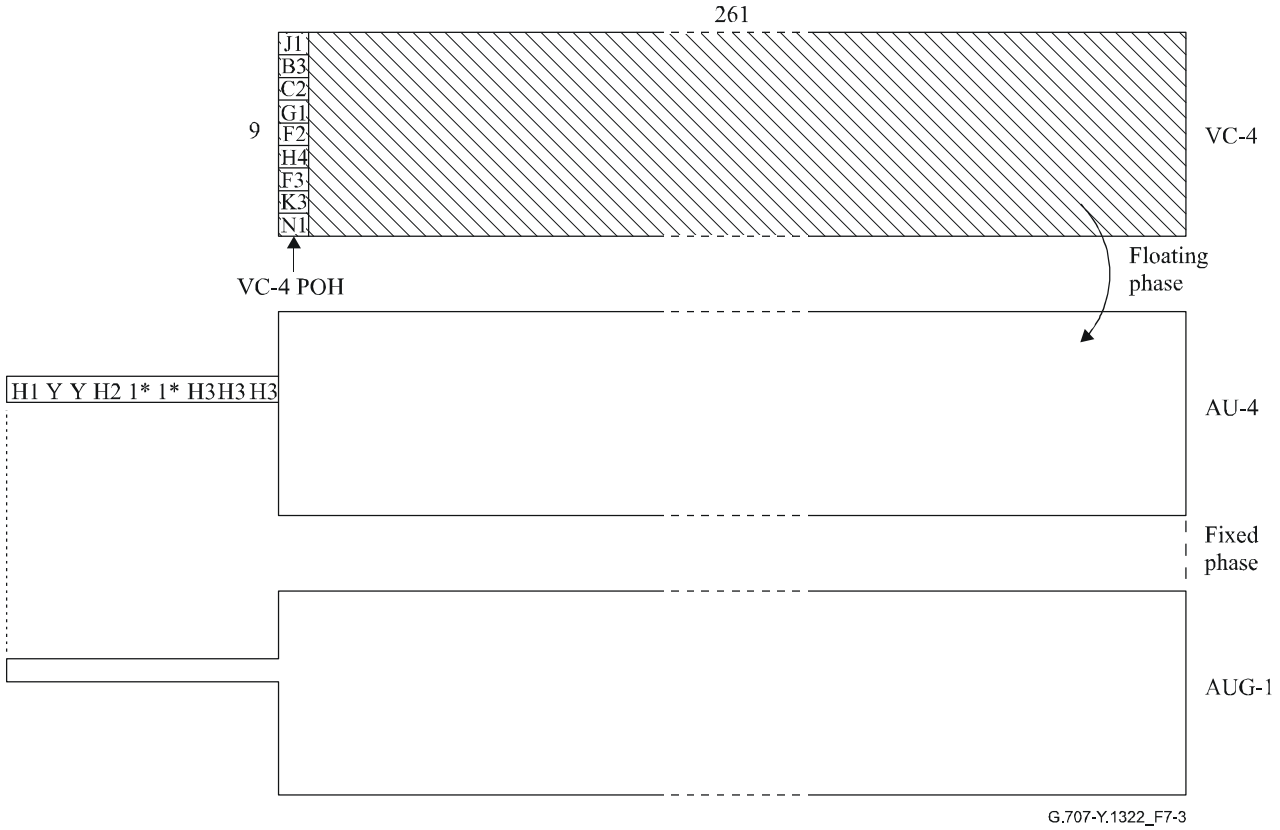


Figure 7-2 – Multiplexing of 4 AUG-Ns into AUG-4×N

7.1.2 Multiplexing of an AU-4 via AUG-1

The multiplexing arrangement of a single AU-4 via the AUG-1 is depicted in Figure 7-3. The 9 bytes at the beginning of row 4 are allocated to the AU-4 pointer. The remaining 9 rows by 261 columns is allocated to the virtual container-4 (VC-4). The phase of the VC-4 is not fixed with respect to the AU-4. The location of the first byte of the VC-4 with respect to the AU-4 pointer is given by the pointer value. The AU-4 is placed directly in the AUG-1.

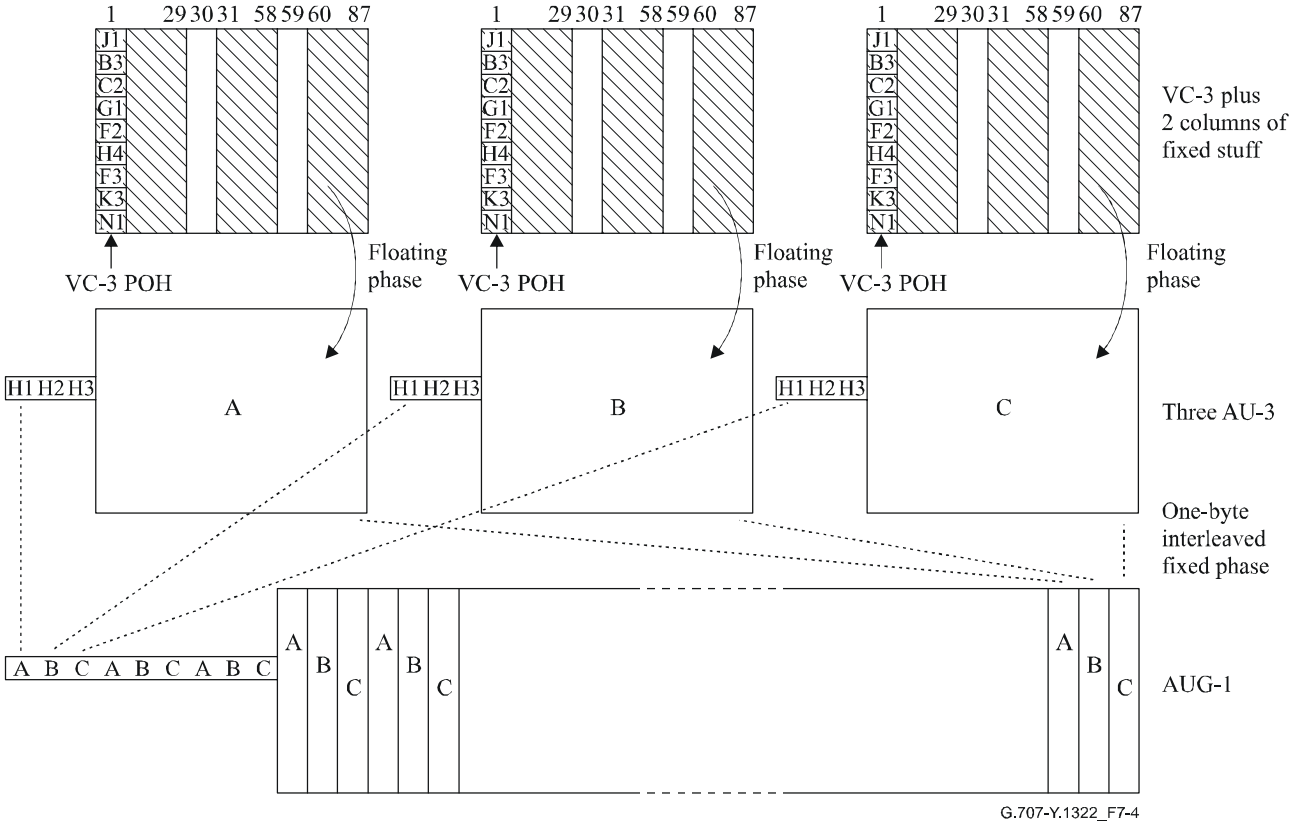


1* All 1s byte
Y 1001 SS11 (S bits are unspecified)

Figure 7-3 – Multiplexing of AU-4 via AUG-1

7.1.3 Multiplexing of AU-3s via AUG-1

The multiplexing arrangement of three AU-3s via the AUG-1 is depicted in Figure 7-4. The 3 bytes at the beginning of row 4 are allocated to the AU-3 pointer. The remaining 9 rows by 87 columns is allocated to the VC-3 and two columns of fixed stuff. The bytes in each row of the two columns of fixed stuff of each AU-3 shall be the same. The phase of the VC-3 and the two columns of fixed stuff is not fixed with respect to the AU-3. The location of the first byte of the VC-3 with respect to the AU-3 pointer is given by the pointer value. The three AU-3s are one-byte interleaved in the AUG-1.

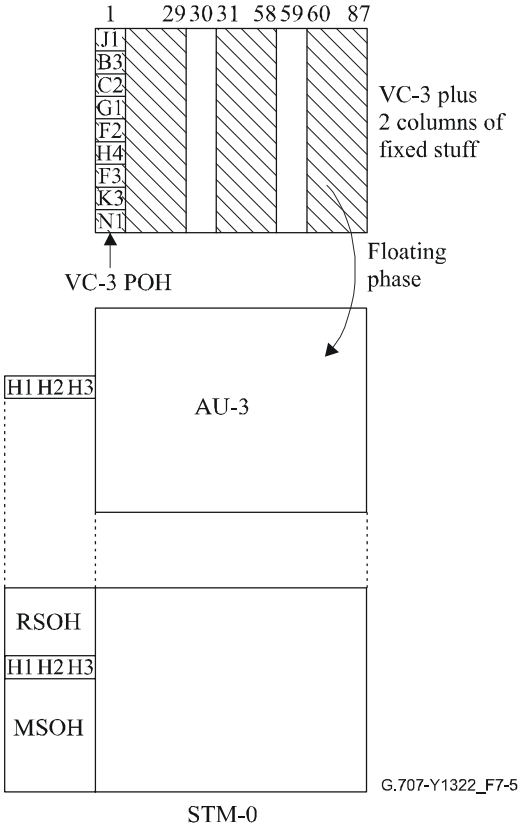


NOTE – The byte in each row of the two columns of fixed stuff of each AU-3 shall be the same.

Figure 7-4 – Multiplexing of AU-3s via AUG-1

7.1.4 Multiplexing of AU-3 into STM-0

The AU-3 is a structure of 9 rows by 87 columns plus 3 bytes in row 4 (for the AU-3 pointers). The STM-0 consists of an SOH as described in clause 9.2 and a structure of 9 rows by 87 columns with 3 bytes in row 4 (for the AU-3 pointers). The AU-3 is multiplexed into this structure and has a fixed phase relationship with respect to the STM-0 as shown in Figure 7-5.



NOTE – The byte in each row of the two columns of fixed stuff of each AU-3 shall be the same.

Figure 7-5 – Multiplexing of AU-3 into STM-0

7.2 Multiplexing of tributary units into VC-4 and VC-3

7.2.1 Multiplexing of tributary unit group-3s (TUG-3s) into a VC-4

The arrangement of three TUG-3s multiplexed in the VC-4 is shown in Figure 7-6. The TUG-3 is a 9-row by 86-column structure. The VC-4 consists of one column of VC-4 POH, two columns of fixed stuff and a 258-column payload structure. The three TUG-3s are single byte interleaved into the 9-row by 258-column VC-4 payload structure and have a fixed phase with respect to the VC-4.

As described in clause 7.1, the phase of the VC-4 with respect to the AU-4 is given by the AU-4 pointer.

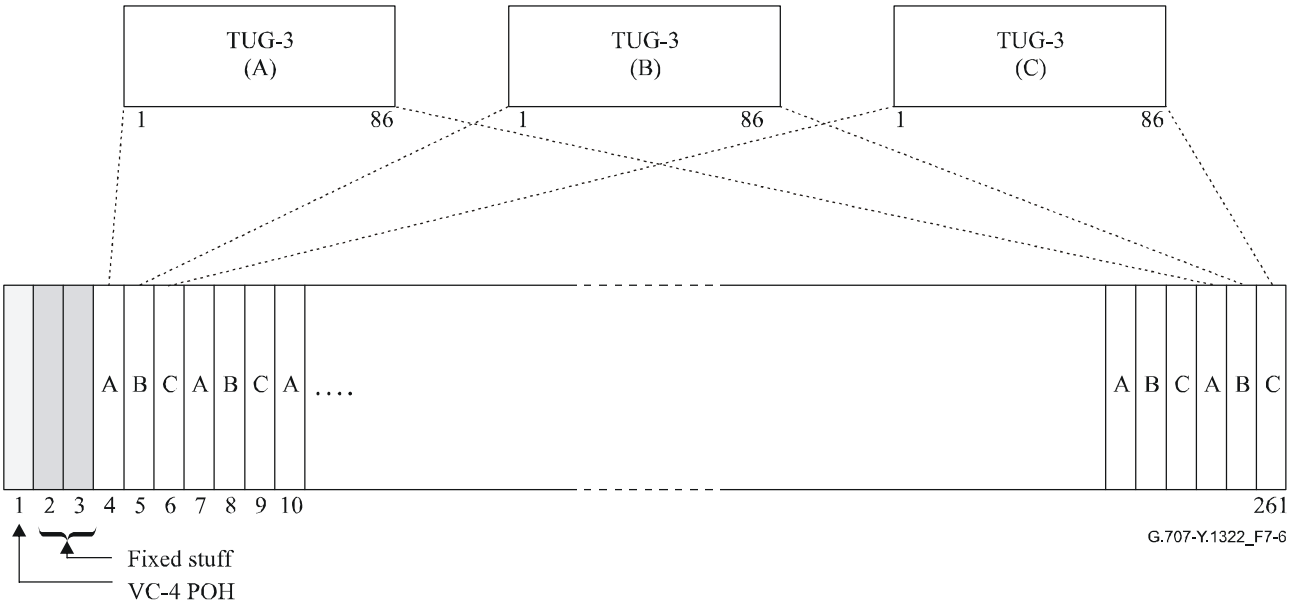


Figure 7-6 – Multiplexing of three TUG-3s into a VC-4

7.2.2 Multiplexing of a TU-3 via TUG-3

The multiplexing of a single TU-3 via the TUG-3 is depicted in Figure 7-7. The TU-3 consists of the VC-3 with a 9-byte VC-3 POH and the TU-3 pointer. The first column of the 9-row by 86-column TUG-3 is allocated to the TU-3 pointer (bytes H1, H2, H3) and fixed stuff. The phase of the VC-3 with respect to the TUG-3 is indicated by the TU-3 pointer.

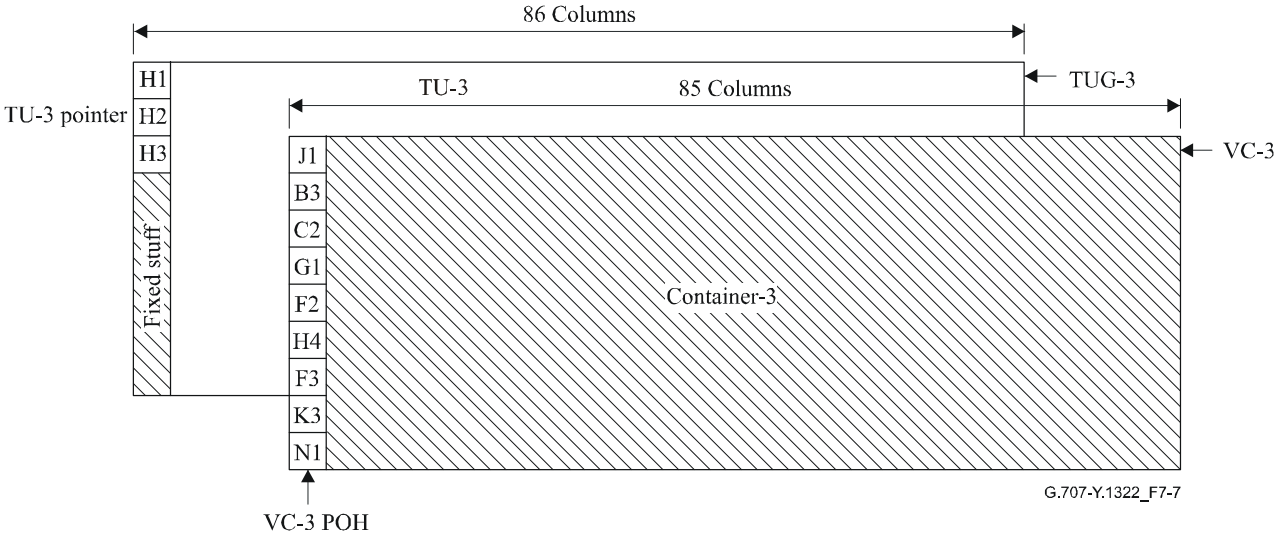


Figure 7-7 – Multiplexing of a TU-3 via a TUG-3

7.2.3 Multiplexing of TUG-2s via a TUG-3

The multiplexing structure for the TUG-2 via the TUG-3 is depicted in Figure 7-8. The TUG-3 is a 9-row by 86-column structure with the first two columns of fixed stuff.

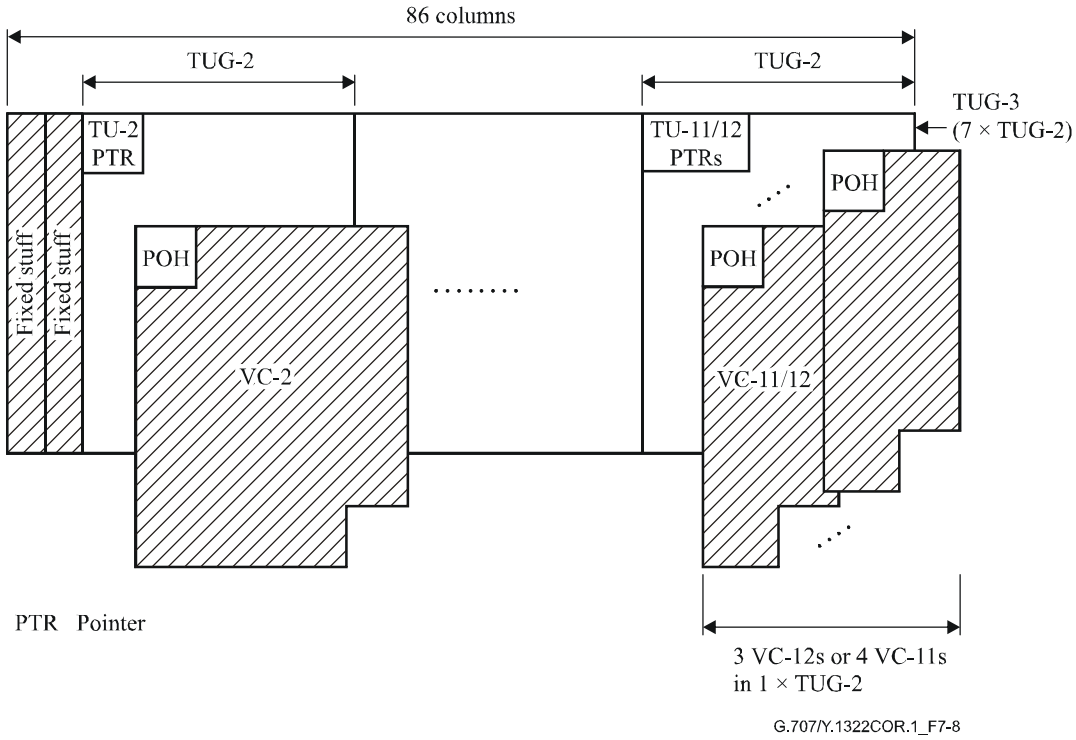


Figure 7-8 – Multiplexing of seven TUG-2s via a TUG-3

A group of seven TUG-2s can be multiplexed via the TUG-3.

The arrangement of seven TUG-2s multiplexed via the TUG-3 is depicted in Figure 7-9. The TUG-2s are one-byte interleaved in the TUG-3.

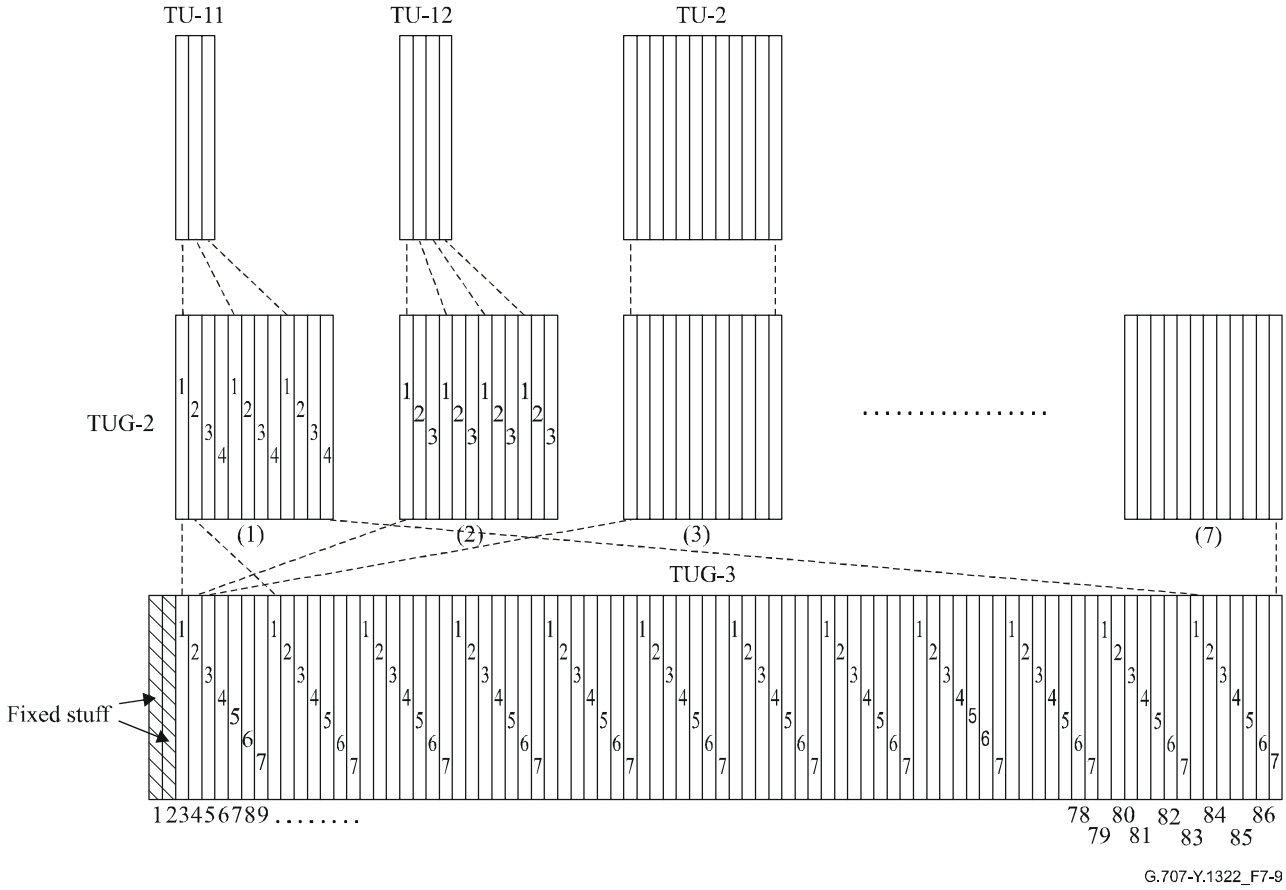


Figure 7-9 – Multiplexing of seven TUG-2s via a TUG-3

7.2.4 Multiplexing of TUG-2s into a VC-3

The multiplexing structure for TUG-2s into a VC-3 is depicted in Figure 7-10. The VC-3 consists of VC-3 POH and a 9-row by 84-column payload structure. A group of seven TUG-2s can be multiplexed into the VC-3.

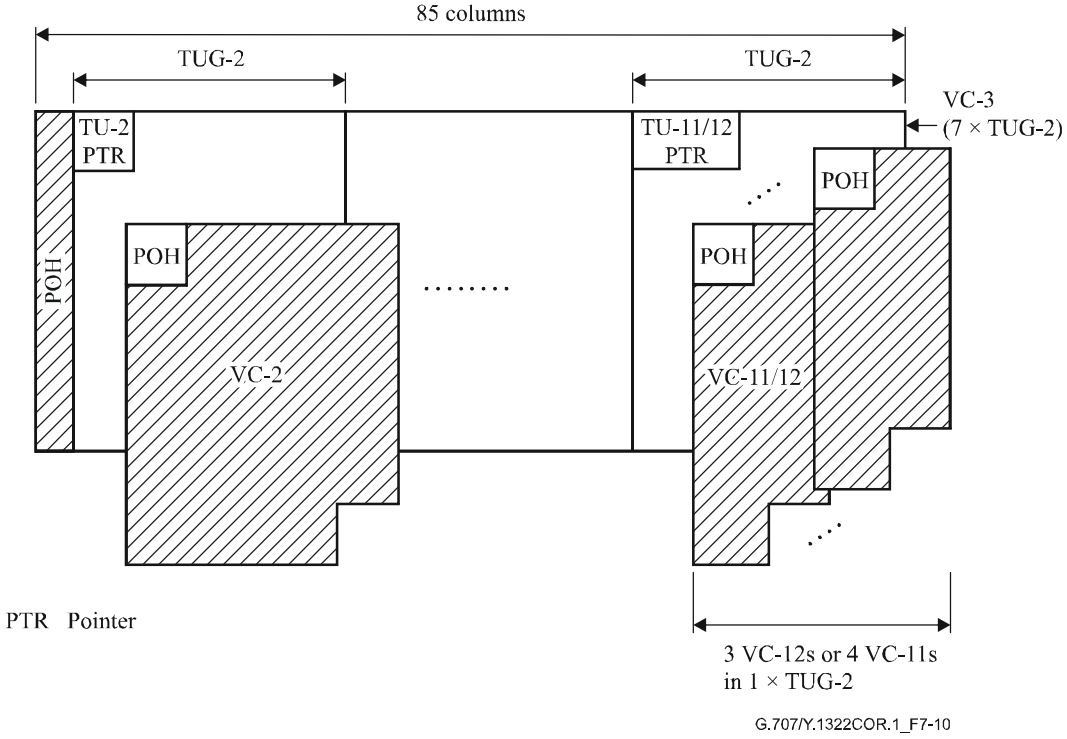


Figure 7-10 – Multiplexing of seven TUG-2s into a VC-3

The arrangement of seven TUG-2s multiplexed into the VC-3 is depicted in Figure 7-11. The TUG-2s are one-byte interleaved in the VC-3. An individual TUG-2 has a fixed location in the VC-3 frame.

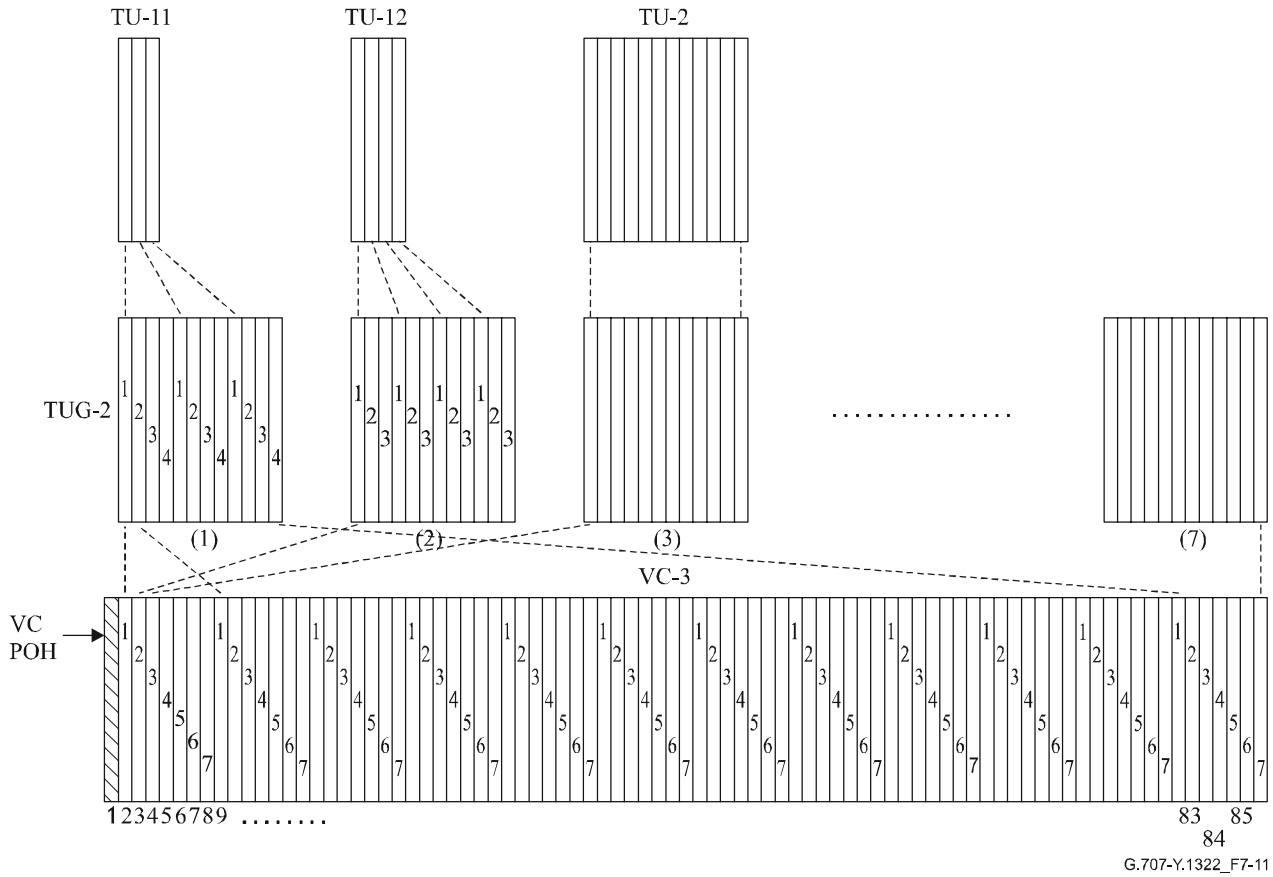


Figure 7-11 – Arrangement of seven TUG-2s multiplexed into a VC-3

7.2.5 Multiplexing of a TU-2 via TUG-2s

The multiplexing arrangement of a single TU-2 via the TUG-2 is depicted in Figure 7-11.

7.2.6 Multiplexing of TU-11s or TU-12s via TUG-2s

The multiplexing arrangements of four TU-11s or three TU-12s via the TUG-2 are depicted in Figure 7-11. The TU-11s/TU-12s are one-byte interleaved in the TUG-2.

7.3 AU-n/TU-n numbering scheme

An STM-N frame comprises N × 270 columns (numbered 1 to N × 270). The first N × 9 columns contain the SOH and AU-4/AU-4-Xc pointer(s) with the remaining N × 261 columns containing the higher order data payload (higher order tributaries).

The higher order payload columns may be addressed by means of a two (B,A), three (C,B,A), four (D,C,B,A) or five (E,D,C,B,A) figure address, where A represents the AU-3 number, B the AUG-1 number, C the AUG-4 number, D the AUG-16 number and E the AUG-64 number. Refer to Figures 7-12 to 7-25.

In the case of an AU-4 structured frame, the payload columns may be addressed by means of a three figure address (K, L, M) where K represents the TUG-3 number, L the TUG-2 number, and M the TU-11/TU-12 number. Refer to Figures 7-27 and 7-28 and Table 7-1. In the case of an AU-3 structured frame, only L and M coordinates are used. Refer to Figure 7-29 and Table 7-2.

In order to provide a simple and convenient means of determining the total tributary capacity, i.e., the number of lower order tributaries provided, the payload columns are allocated a time slot number. The number of time slots per tributary in each frame is determined by the payload configuration.

AU time slots (TS) are numbered from left to right in the STM-N as shown in Figures 7-12 to 7-26. TU time slots (TS) are numbered from left to right in the VC-4/VC-3 as shown in Figures 7-27 to 7-29.

AUs and TUs can either be numbered in a sequential hierarchy, indicated in Figures 7-12 to 7-29 by "time slot number", or by using the multiplex hierarchy, indicated in Figures 7-12 to 7-29 by "address".

For example, an STM-256 can comprise 64 AU-4-4c numbered 1 to 64, where AU-4-4c with time slot number 17 has address (2, 1, 1, 0, 0) and a VC-4 can comprise 63 TU-12 numbered 1 to 63, where TU-12 with time slot number 17 has address (2, 6, 1).

7.3.1 Numbering of AU-ns (VC-ns) in an STM-256

The STM-256 can comprise four AUG-64s, which shall be numbered #1 to #4:

– AUG-64 #1 is accommodated in columns 1…64, 257…320, 513…576, etc., of the STM-256;

– AUG-64 #2 is accommodated in columns 65…128, 321…384, 577…640, etc., of the STM-256;

– AUG-64 #3 is accommodated in columns 129…192, 385…448, 641…704, etc., of the STM-256;

– AUG-64 #4 is accommodated in columns 193…256, 449…512, 705…768, etc., of the STM-256.

Each AUG-64 can comprise four AUG-16s, which shall be numbered #1 to #4. Each AUG-16 can comprise four AUG-4s, which shall be numbered #1 to #4. Each AUG-4 can comprise four AUG-1s, which shall be numbered #1 to #4. Each AUG-1 can comprise three AU-3s, which shall be numbered #1 to #3.

7.3.1.1 Numbering of AU-4s (VC-4s) in an STM-256

Any AU-4 can be allocated a number in the form #E, #D, #C, #B, #A, where E designates the AUG-64 number (1 to 4), D designates the AUG-16 number (1 to 4), C designates the AUG-4 number (1 to 4), B designates the AUG-1 number (1 to 4), and A is always 0, see Figure 7-12. The location of the columns in the STM-256 occupied by AU-4 (E,D,C,B,0) is given by:

Xth column = $1 + 64 \times [E–1] + 16 \times [D–1] + 4 \times [C–1] + [B–1] + 256 \times [X–1]$ for X = 1 to 270.

Therefore, AU-4 (1,1,1,1,0) resides in columns 1, 257, 513, 769, … 68 865 of the STM-256, and AU-4 (4,4,4,4,0) resides in columns 256, 512, 768, …, 69 120 of the STM-256.

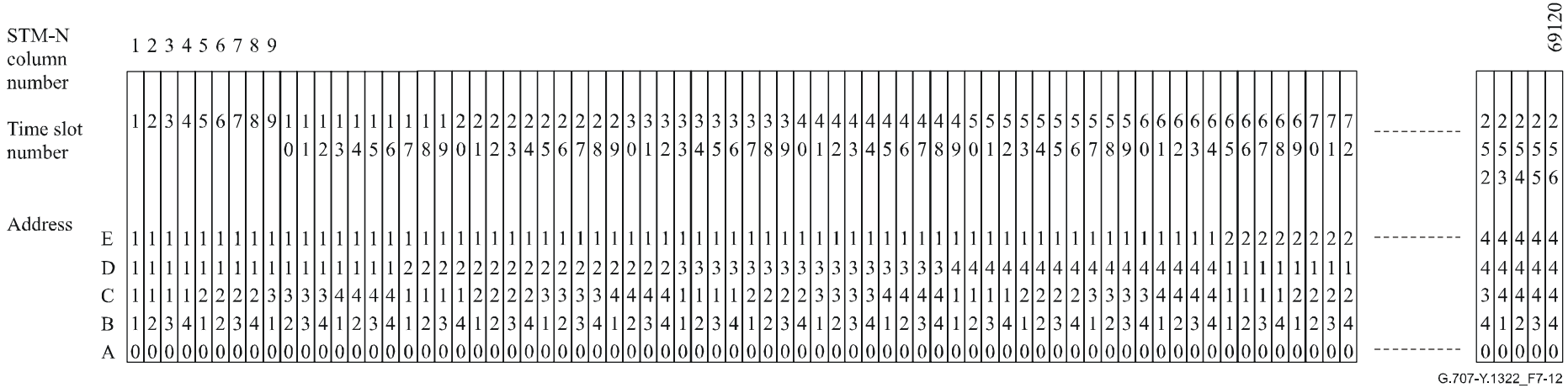


Figure 7-12 – AU-4 numbering scheme within an STM-256's AU pointer row and playload columns

7.3.1.2 Numbering of AU-3s (VC-3s) in an STM-256

Any AU-3 can be allocated a number in the form #E, #D, #C, #B, #A, where E designates the AUG-64 number (1 to 4), D designates the AUG-16 number (1 to 4), C designates the AUG-4 number (1 to 4), B designates the AUG-1 number (1 to 4), and A designates the AU-3 number (1 to 3), see Figure 7-13. The location of the columns in the STM-256 occupied by AU-3 (E,D,C,B,A) is given by:

Xth column = 1 + 64 × [E–1] + 16 × [D–1] + 4 × [C–1] + [B–1] + 256 × [A–1] + 768 × [X–1] for X = 1 to 90.

Therefore, AU-3 (1,1,1,1,1) resides in columns 1, 769, 1537, 2305, … 68 353 of the STM-256, and AU-3 (4,4,4,4,3) resides in columns 768, 1536, 2304, … 69 120 of the STM-256.

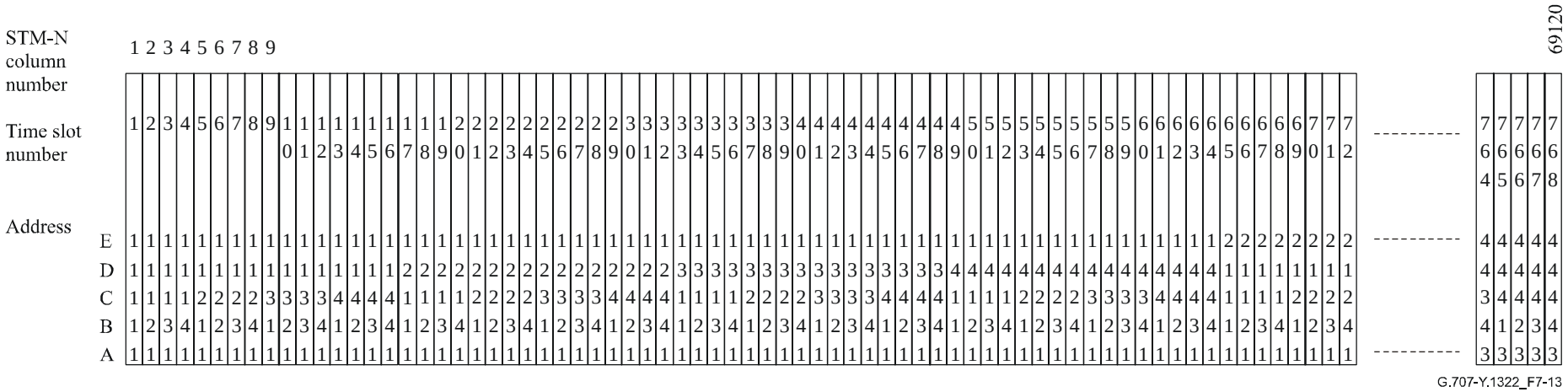


Figure 7-13 – AU-3 numbering scheme within an STM-256's AU pointer row and playload columns

7.3.1.3 Numbering of AU-4-4cs (VC-4-4cs) in an STM-256

Any AU-4-4c can be allocated a five-figure address in the form #E, #D, #C, #B, #A, where E designates the AUG-64 number (1 to 4), D designates the AUG-16 number (1 to 4), C designates the AUG-4 number (1 to 4), B and A are always 0, see Figure 7-14. The location of the columns in the STM-256 occupied by AU-4-4c (E,D,C,0,0) is given by:

Xth column = [X mod 4] + 64 × [E–1] + 16 × [D–1] + 4 × [C–1] + 256 × [X DIV 4] for X = 1 to 1080.

Therefore, AU-4-4c (1,1,1,0,0) resides in columns 1,2,3,4, 257,258,259,260, 513,514,515,516, … 68 865,68 866,68 867,68 868 of the STM-256, and AU-4-4c (4,4,4,0,0) resides in columns 253,254,255,256, 509,510,511,512, 765,766,767,768, … 69 117,69 118,69 119,69 120 of the STM-256.

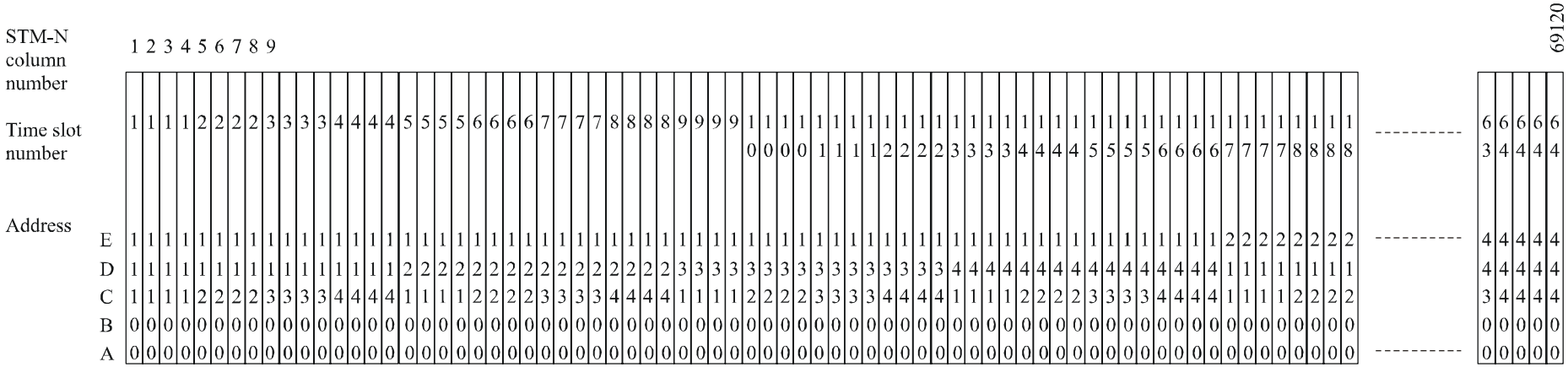


Figure 7-14 – AU-4-4c numbering scheme within an STM-256's AU pointer row and playload columns

7.3.1.4 Numbering of AU-4-16cs (VC-4-16cs) in an STM-256

Any AU-4-16c can be allocated a five-figure address in the form #E, #D, #C, #B, #A, where E designates the AUG-64 number (1 to 4), D designates the AUG-16 number (1 to 4), C, B and A are always 0, see Figure 7-15. The location of the columns in the STM-256 occupied by AU-4-16c (E,D,0,0,0) is given by:

Xth column = [X mod 16] + 64 × [E–1] + 16 × [D–1] + 256 × [X DIV 16] for X = 1 to 4320.

Therefore, AU-4-16c (1,1,0,0,0) resides in columns 1…16, 257…272, …, 68 865…68 880 of the STM-256, and AU-4-16c (4,4,0,0,0) resides in columns 241…256, 497…512, …, 69 105…69 120 of the STM-256.

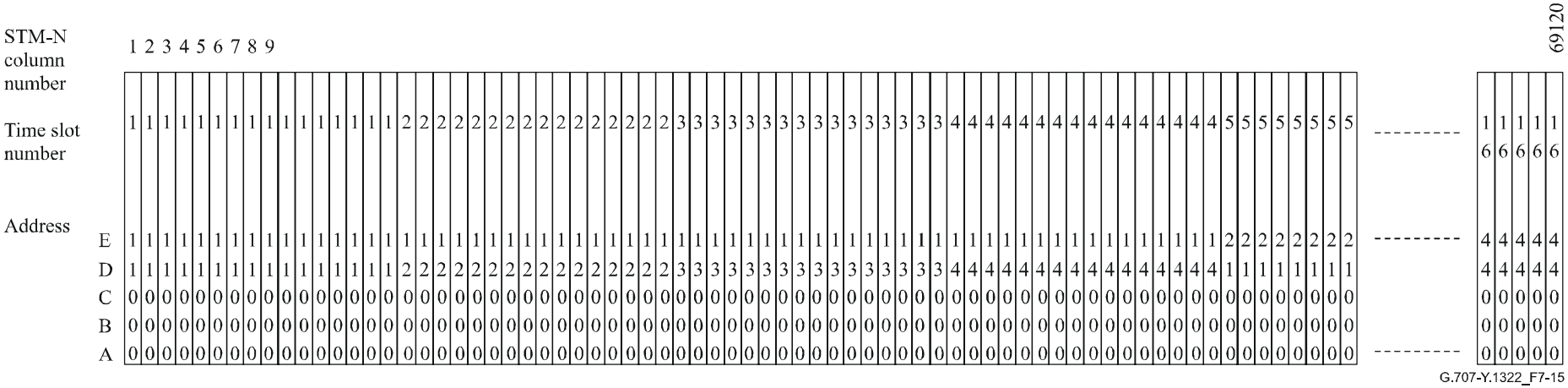


Figure 7-15 – AU-4-16c numbering scheme within an STM-256's AU pointer row and playload columns

7.3.1.5 Numbering of AU-4-64cs (VC-4-64cs) in an STM-256

Any AU-4-64c can be allocated a five-figure address in the form #E, #D, #C, #B, #A, where E designates the AUG-64 number (1 to 4), D, C, B and A are always 0, see Figure 7-16. The location of the columns in the STM-256 occupied by AU-4-64c (E,0,0,0,0) is given by:

Xth column = [X mod 64] + 64 × [E–1] + 256 × [X DIV 64] for X = 1 to 17 280.

Therefore, AU-4-16c (1,0,0,0,0) resides in columns 1…64, 257…321, …, 68 865…68 928 of the STM-256, and AU-4-16c (4,0,0,0,0) resides in columns 193…256, 449…512, …, 69 057…69 120 of the STM-256.

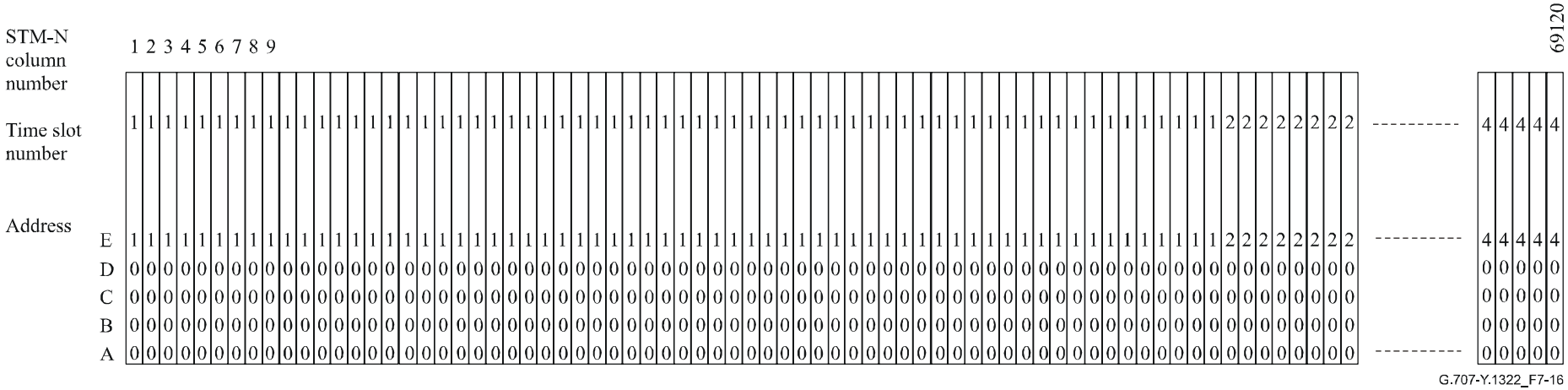


Figure 7-16 – AU-4-64c numbering scheme within an STM-256's AU pointer row and playload columns

7.3.1.6 Numbering of an AU-4-256c in an STM-256

There is one AU-4-256c in an STM-256 signal. This signal does not need a number, but can be referred to as (0,0,0,0,0).

7.3.2 Numbering of AU-ns (VC-ns) in an STM-64

The STM-64 can comprise four AUG-16s, which shall be numbered #1 to #4:

– AUG-16 #1 is accommodated in columns 1…16, 65…80, 129…144, etc., of the STM-64;

– AUG-16 #2 is accommodated in columns 17…32, 81…96, 145…160, etc., of the STM-64;

– AUG-16 #3 is accommodated in columns 33…48, 97…112, 161…176, etc., of the STM-64;

– AUG-16 #4 is accommodated in columns 49…64, 113…128, 177…192, etc., of the STM-64.

Each AUG-16 can comprise four AUG-4s, which shall be numbered #1 to #4. Each AUG-4 can comprise four AUG-1s, which shall be numbered #1 to #4. Each AUG-1 can comprise three AU-3s, which shall be numbered #1 to #3.

7.3.2.1 Numbering of AU-4s (VC-4s) in an STM-64

Any AU-4 can be allocated a number in the form #D, #C, #B, #A, where D designates the AUG-16 number (1 to 4), C designates the AUG-4 number (1 to 4), B designates the AUG-1 number (1 to 4), and A is always 0, see Figure 7-17. The location of the columns in the STM-64 occupied by AU-4 (D,C,B,0) is given by:

Xth column = $1 + 16 \times [D–1] + 4 \times [C–1] + [B–1] + 64 \times [X–1]$ for X = 1 to 270.

Therefore, AU-4 (1,1,1,0) resides in columns 1, 65, 129, 193, … 17 217 of the STM-64, and AU-4 (4,4,4,0) resides in columns 64, 128, 192, …, 17 280 of the STM-64.

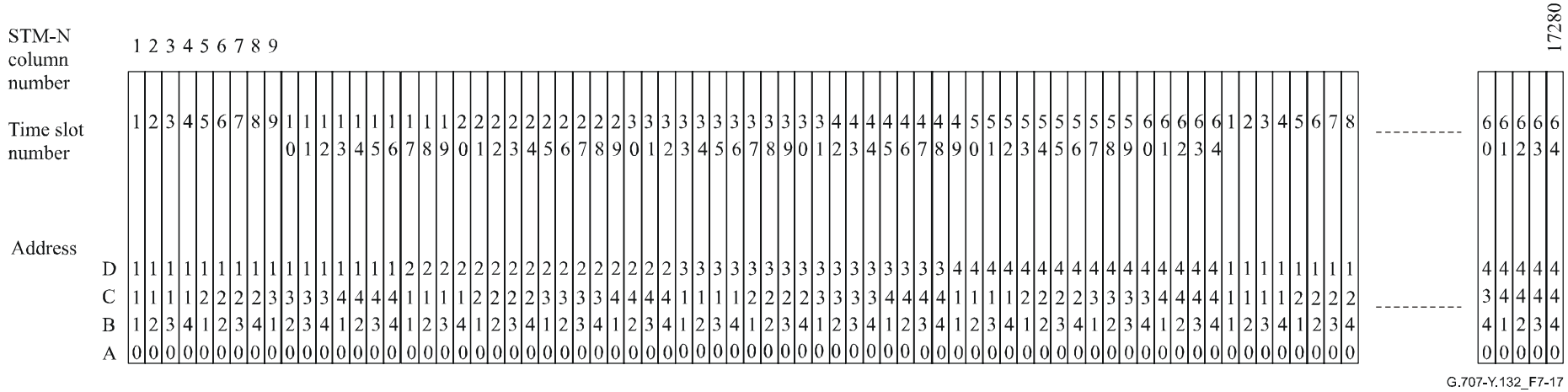


Figure 7-17 – AU-4 numbering scheme within an STM-64's AU pointer row and playload columns

7.3.2.2 Numbering of AU-3s (VC-3s) in an STM-64

Any AU-3 can be allocated a number in the form #D, #C, #B, #A, where D designates the AUG-16 number (1 to 4), C designates the AUG-4 number (1 to 4), B designates the AUG-1 number (1 to 4), and A designates the AU-3 number (1 to 3), see Figure 7-18. The location of the columns in the STM-64 occupied by AU-3 (D, C, B, A) is given by:

Xth column = 1 + 16 × [D–1] + 4 × [C–1] + [B–1] + 64 × [A–1] + 192 × [X–1] for X = 1 to 90.

Therefore, AU-3 (1,1,1,1) resides in columns 1, 193, 385, 577, … 17 089 of the STM-64, and AU-3 (4,4,4,3) resides in columns 192, 384, 576 …, 17 280 of the STM-64.

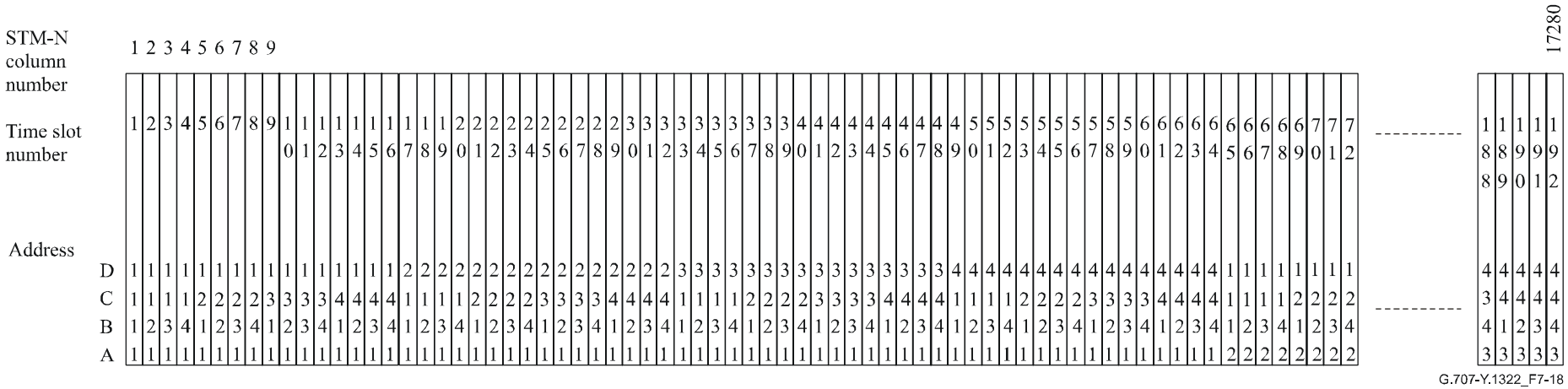


Figure 7-18 – AU-3 numbering scheme within an STM-64's AU pointer row and playload columns

7.3.2.3 Numbering of AU-4-4cs (VC-4-4cs) in an STM-64

Any AU-4-4c can be allocated a four-figure address in the form #D, #C, #B, #A, where D designates the AUG-16 number (1 to 4), C designates the AUG-4 number (1 to 4), B and A are always 0, see Figure 7-19. The location of the columns in the STM-64 occupied by AU-4-4c (D,C,0,0) is given by:

Xth column = $[X \bmod 4] + 16 \times [D-1] + 4 \times [C-1] + 64 \times [X \text{ DIV } 4]$ for X = 1 to 1080.

Therefore, AU-4-4c (1,1,0,0) resides in columns 1,2,3,4,65,66,67,68,129,130,131,132, …, 17 217, 17 218, 17 219, 17 220 of the STM-64, and AU-4-4c (4, 4, 0, 0) resides in columns 61,62,63,64,125, 126,127,128, …, 17 277, 17 278, 17 279, 17 280 of the STM-64.

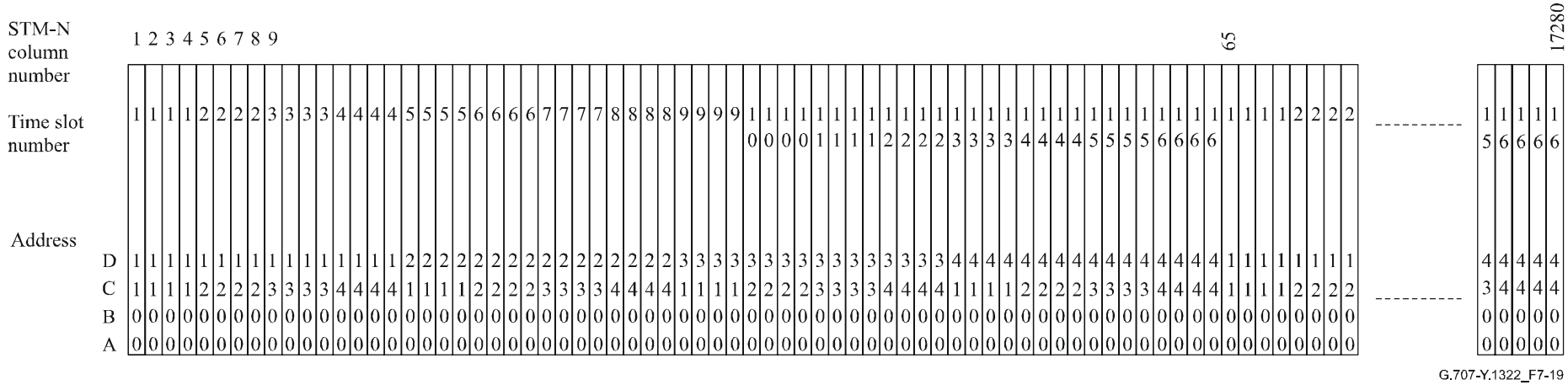


Figure 7-19 – AU-4-4c numbering scheme within an STM-64's AU pointer row and playload columns

7.3.2.4 Numbering of AU-4-16cs (VC-4-16cs) in an STM-64

Any AU-4-16c can be allocated a four-figure address in the form #D, #C, #B, #A, where D designates the AUG-16 number (1 to 4), C, B and A are always 0, see Figure 7-20. The location of the columns in the STM-64 occupied by AU-4-16c (D,0,0,0) is given by:

Xth column = [X mod 16] + 16 × [D–1] + 64 × [X DIV 16] for X = 1 to 4320.

Therefore, AU-4-16c (1,0,0,0) resides in columns 1…16, 65…80, …, 17 205…17 220 of the STM-64, and AU-4-16c (4,0,0,0) resides in columns 49…64, 113…128, …, 17 265…17 280 of the STM-64.

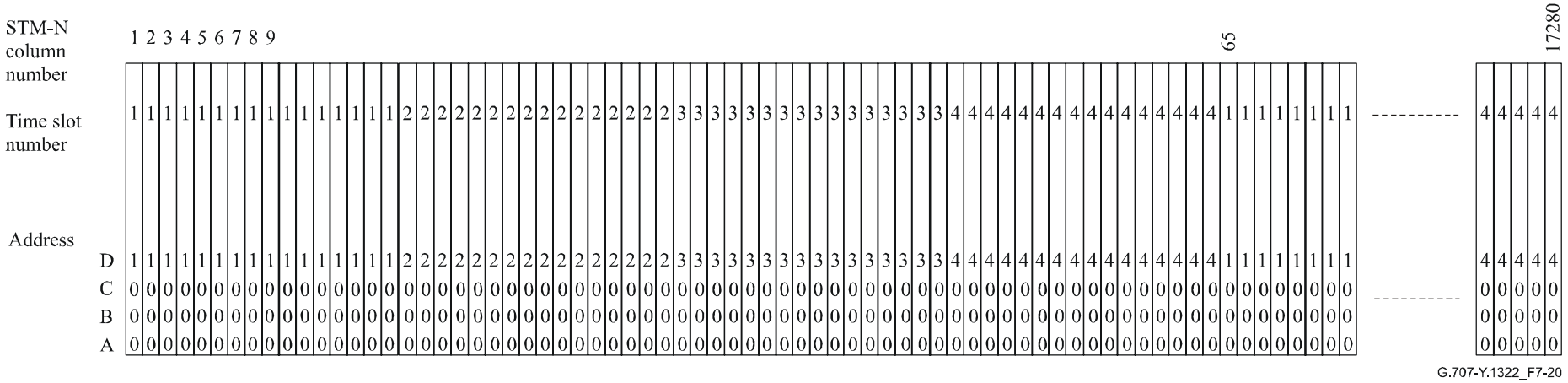


Figure 7-20 – AU-4-16c numbering scheme within an STM-64's AU pointer row and playload columns

7.3.2.5 Numbering of an AU-4-64c in an STM-64

There is one AU-4-64c in an STM-64 signal. This signal does not need a number, but can be referred to as (0,0,0,0).

7.3.3 Numbering of AU-ns (VC-ns) in an STM-16

The STM-16 can comprise four AUG-4s, which shall be numbered #1 to #4:

– AUG-4 #1 is accommodated in columns 1…4, 17…20, 33…36, etc., of the STM-16;

– AUG-4 #2 is accommodated in columns 5…8, 21…24, 36…40, etc., of the STM-16;

– AUG-4 #3 is accommodated in columns 9…12, 25…28, 41…44, etc., of the STM-16;

– AUG-4 #4 is accommodated in columns 13…16, 29…32, 45…48, etc., of the STM-16.

Each AUG-4 can comprise four AUG-1s, which shall be numbered #1 to #4. Each AUG-1 can comprise three AU-3s, which shall be numbered #1 to #3.

7.3.3.1 Numbering of AU-4s (VC-4s) in an STM-16

Any AU-4 can be allocated a number in the form #C, #B, #A, where C designates the AUG-4 number (1 to 4), B designates the AUG-1 number (1 to 4), and A is always 0, see Figure 7-21. The location of the columns in the STM-16 occupied by AU-4 (C,B,0) is given by:

Xth column = $1 + 4 \times [C–1] + [B–1] + 16 \times [X–1]$ for X = 1 to 270.

Therefore, AU-4 (1,1,0) resides in columns 1, 17, 33, …, 4305 of the STM-16, and AU-4 (4,4,0) resides in columns 16, 32, 48, …, 4320 of the STM-16.

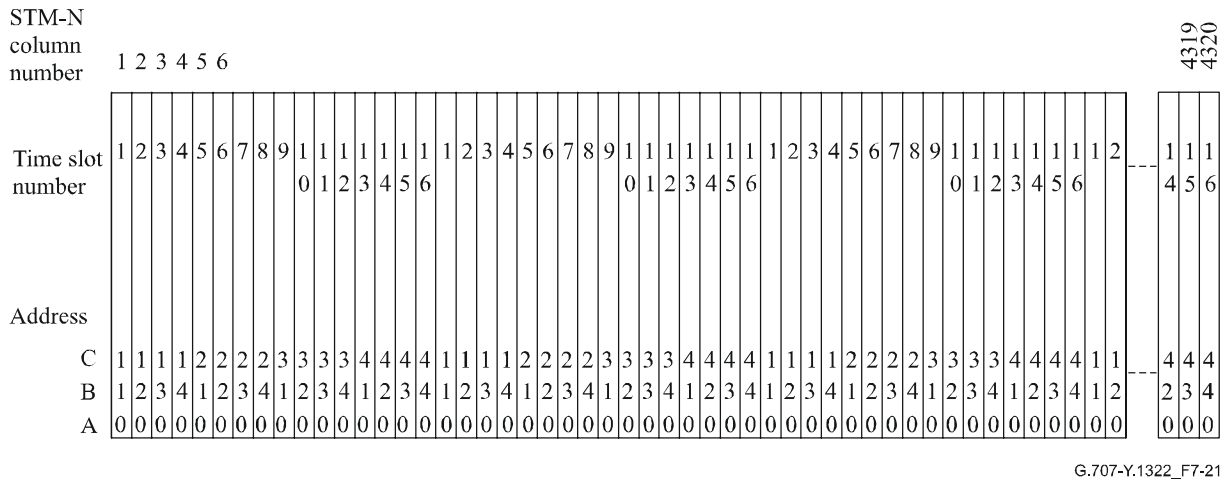


Figure 7-21 – AU-4 numbering scheme within an STM-16's AU pointer row and payload columns

7.3.3.2 Numbering of AU-3s (VC-3s) in an STM-16

Any AU-3 can be allocated a number in the form #C, #B, #A, where C designates the AUG-4 number (1 to 4), B designates the AUG-1 number (1 to 4), and A designates the AU-3 number (1 to 3), see Figure 7-22. The location of the columns in the STM-16 occupied by AU-3 (C,B,A) is given by:

Xth column = $1 + 4 \times [C–1] + [B–1] + 16 \times [A–1] + 48 \times [X–1]$ for X = 1 to 90.

Therefore, AU-3 (1,1,1) resides in columns 1, 49, 97, …, 4273 of the STM-16, and AU-3 (4,4,3) resides in columns 48, 96, 144, …, 4320 of the STM-16.

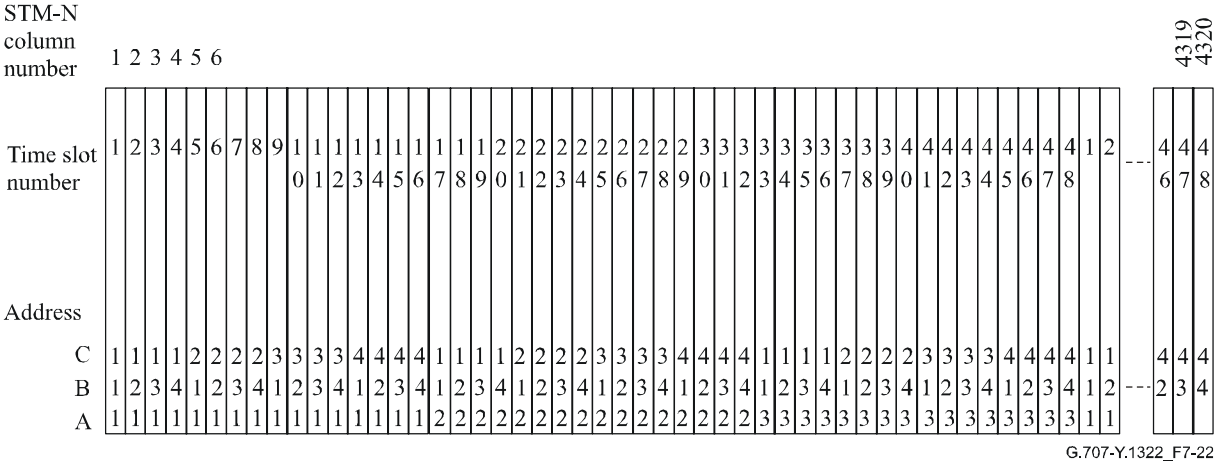


Figure 7-22 – AU-3 numbering scheme within an STM-16's AU pointer row and payload columns

7.3.3.3 Numbering of AU-4-4cs (VC-4-4cs) in an STM-16

Any AU-4-4c can be allocated a three-figure address in the form #C, #B, #A, where C designates the AUG-4 number (1 to 4), B and A always 0, see Figure 7-23. The location of the columns in the STM-16 occupied by AU-4-4c (C,0,0) is given by:

4X-3th column = $1 + [C–1] + 16 \times [X–1]$ for X = 1 to 270.

4X-2th column = $2 + [C–1] + 16 \times [X–1]$ for X = 1 to 270.

4X-1th column = $3 + [C–1] + 16 \times [X–1]$ for X = 1 to 270.

4Xth column = $4 + [C–1] + 16 \times [X–1]$ for X = 1 to 270.

Therefore, AU-4-4c (1,0,0) resides in columns 1…4, 17…20, …, 4305…4308 of the STM-16, and AU-4-4c (4,0,0) resides in columns 13…16, 29…32, …, 4317…4320 of the STM-16.

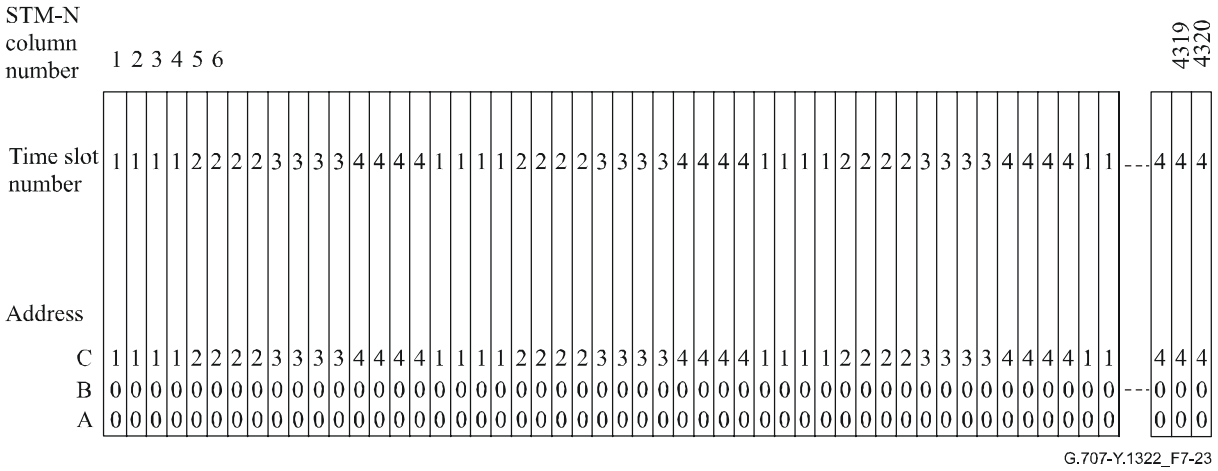


Figure 7-23 – AU-4-4c numbering scheme within an STM-16's AU pointer row and payload columns

7.3.3.4 Numbering of AU-4-16c in an STM-16

There is one AU-4-16c in an STM-16 signal. This signal does not need a number, but can be referred to as (0,0,0).

7.3.4 Numbering of AU-ns (VC-ns) in an STM-4

The STM-4 can comprise four AUG-1s, which shall be numbered #1 to #4;

– AUG-1 #1 is accommodated in columns 1, 5, 9, etc., of the STM-4;

– AUG-1 #2 is accommodated in columns 2, 6, 10, etc., of the STM-4;

– AUG-1 #3 is accommodated in columns 3, 7, 11, etc., of the STM-4;

– AUG-1 #4 is accommodated in columns 4, 8, 12, etc., of the STM-4.

Each AUG-1 can comprise three AU-3s, which shall be numbered #1 to #3.

7.3.4.1 Numbering of AU-4s (VC-4s) in an STM-4

Any AU-4 can be allocated a number in the form #B, #A, where B designates the AUG-1 number (1 to 4), and A is always 0, see Figure 7-24. The location of the columns in the STM-4 occupied by AU-4 (B,0) is given by:

Xth column = 1 + [B–1] + 4 × [X–1] for X = 1 to 270.

Therefore, AU-4 (1,0) resides in columns 1, 5, 9, …, 1077 of the STM-4, and AU-4 (4,0) resides in columns 4, 8, 12, …, 1080 of the STM-4.

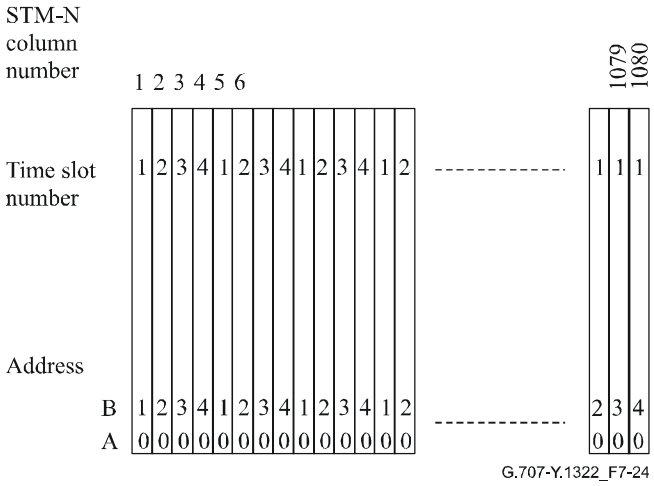


Figure 7-24 – AU-4 numbering scheme within an STM-4's AU pointer row and payload columns

7.3.4.2 Numbering of AU-3s (VC-3s) in an STM-4

Any AU-3 can be allocated a number in the form #B, #A, where B designates the AUG-1 number (1 to 4), and A designates the AU-3 number (1 to 3), see Figure 7-25. The location of the columns in the STM-4 occupied by AU-3 (B,A) is given by:

Xth column = 1 + [B–1] + 4 × [A–1] + 12 × [X–1] for X = 1 to 90.

Therefore, AU-3 (1,1) resides in columns 1, 13, 25, …, 1069 of the STM-4, and AU-4 (4,3) resides in columns 12, 24, 36, …, 1080 of the STM-4.

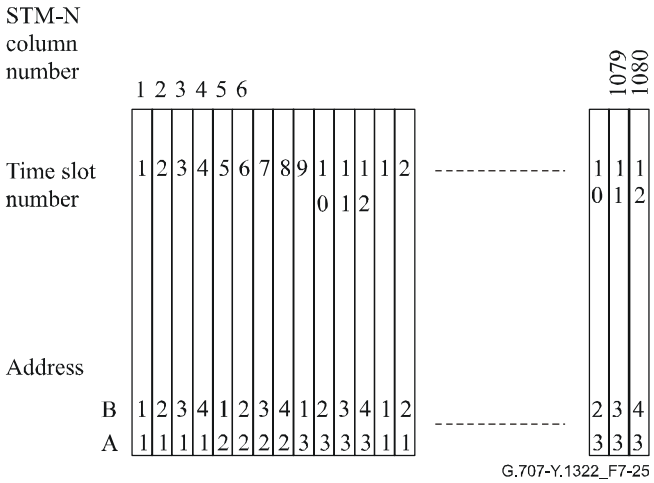


Figure 7-25 – AU-3 numbering scheme within an STM-4's AU pointer row and payload columns

7.3.4.3 Numbering of an AU-4-4c in an STM-4

There is one AU-4-4c in an STM-4 signal. This signal does not need a number, but can be referred to as (0,0).

7.3.5 Numbering of AU-ns (VC-ns) in an STM-1 signal

7.3.5.1 Numbering of AU-4 (VC-4) in an STM-1 signal

There is one AU-4 (VC-4) in an STM-1 signal. This signal does not need a number, but can be referred to as (0).

7.3.5.2 Numbering of AU-3 (VC-3) in an STM-1 signal

Any AU-3 can be allocated a number in the form #A, where A designates the AU-3 number (1 to 3), see Figure 7-26. The location of the columns in the STM-1 occupied by AU-3 (A) is given by:

Xth column = $1 + [A–1] + 3 \times [X–1]$ for X = 1 to 90.

Therefore, AU-3 (1) resides in columns 1, 4, 7, .., 268 of the STM-1, and AU-3 (3) resides in columns 3, 6, 9, .., 270 of the STM-1.

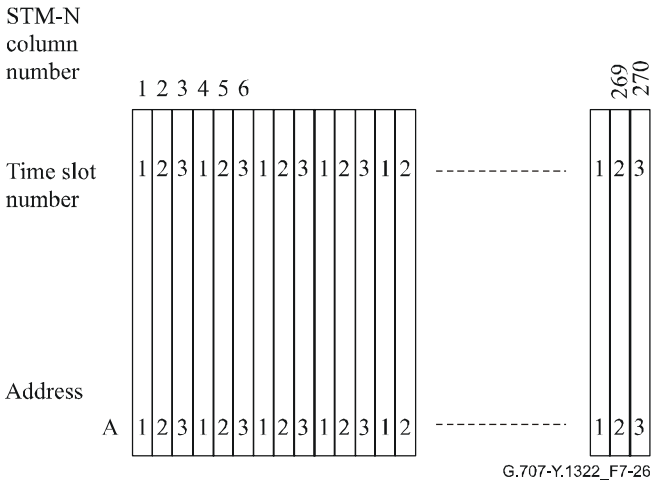


Figure 7-26 – AU-3 numbering scheme within an STM-1's AU pointer row and payload columns

7.3.6 Numbering of AU-3 (VC-3) in an STM-0 signal

There is one AU-3 (VC-3) in an STM-0 signal. This signal does not need a number, but can be referred to as (0).

7.3.7 Numbering of TU-3s in a VC-4

The VC-4 can comprise three TUG-3s which shall be numbered #1, #2, and #3.

– TUG-3 #1 (Corresponding to TUG-3 (A) in Figure 7-6) is accommodated in columns 4, 7, 10, …, 259 of the VC-4;

– TUG-3 #2 (Corresponding to TUG-3 (B) in Figure 7-6) is accommodated in columns 5, 8, 11, …, 260 of the VC-4;

– TUG-3 #3 (Corresponding to TUG-3 (C) in Figure 7-6) is accommodated in columns 6, 9, 12, …, 261 of the VC-4.

Each TUG-3 can comprise a TU-3.

Thus any TU-3 can be allocated a three-figure address in the form #K, #L, #M, where K designates the TUG-3 number (1 to 3); L and M are always 0. The location of the columns in the VC-4 occupied by TU-3 (K,0,0) is given by the formula:

$$\text{Xth column} = 4 + [K–1] + 3 \times [X–1] \qquad \text{for } X = 1 \text{ to } 86.$$

Thus TU-3 (1,0,0) resides in columns 4, 7, 10, …, 259 of the VC-4, and TU-3 (3,0,0) resides in columns 6, 9, 12, …, 261 of the VC-4.

7.3.8 Numbering of TU-2s in a VC-4

Each TUG-3 can comprise seven TUG-2s which shall be numbered #1 to #7 and each TUG-2 can comprise a TU-2.

Thus any TU-2 can be allocated a three-figure address in the form #K, #L, #M, where K designates the TUG-3 number (1 to 3), L designates the TUG-2 number (1 to 7), and M is always 0. The location of the columns in the VC-4 occupied by TU-2 (K, L, 0) is given by the formula:

$$\text{Xth column} = 10 + [K–1] + 3 \times [L–1] + 21 \times [X–1] \qquad \text{for } X = 1 \text{ to } 12.$$

Thus TU-2 (1,1,0) resides in columns 10, 31, 52, 73, 94, 115, 136, 157, 178, 199, 220 and 241 of the VC-4, and TU-2 (3,7,0) resides in columns 30, 51, 72, 93, 114, 135, 156, 177, 198, 219, 240 and 261 of the VC-4. A full listing of the location of the TU-2 columns within the VC-4 frame is given in Appendix I.

7.3.9 Numbering of TU-12s in a VC-4

Each TUG-3 can comprise seven TUG-2s which shall be numbered #1 to #7 and each TUG-2 can comprise three TU-12s which shall be numbered #1 to #3.

Thus any TU-12 can be allocated a number in the form #K, #L, #M, where K designates the TUG-3 number (1 to 3), L designates the TUG-2 number (1 to 7), and M designates the TU-12 number (1 to 3). The location of the columns in the VC-4 occupied by TU-12 (K,L,M) is given by the formula:

$$\text{Xth column} = 10 + [K–1] + 3 \times [L–1] + 21 \times [M–1] + 63 \times [X–1] \qquad \text{for } X = 1 \text{ to } 4.$$

Thus TU-12 (1,1,1) resides in columns 10, 73, 136, and 199 of the VC-4, and TU-12 (3,7,3) resides in columns 72, 135, 198 and 261 of the VC-4. A full listing of the location of the TU-12 columns within the VC-4 frame is given in Appendix II.

7.3.10 Numbering of TU-11s in a VC-4

Each TUG-3 can comprise seven TUG-2s which shall be numbered #1 to #7 and each TUG-2 can comprise four TU-11s which shall be numbered #1 to #4.

Thus any TU-11 can be allocated a number in the form #K, #L, #M, where K designates the TUG-3 number (1 to 3), L designates the TUG-2 number (1 to 7), and M designates the TU-11 number (1 to 4). The location of the columns in the VC-4 occupied by TU-11 (K,L,M) is given by the formula:

Xth column = $10 + [K–1] + 3 \times [L–1] + 21 \times [M–1] + 84 \times [X–1]$ for X = 1 to 3.

Thus TU-11 (1,1,1) resides in columns 10, 94 and 178 of the VC-4, and TU-11 (3,7,4) resides in columns 93, 177 and 261 of the VC-4. A full listing of the location of the TU-11 columns within the VC-4 frame is given in Appendix III.

7.3.11 Numbering of TU-2s in a VC-3

As shown in Figures 7-9 and 7-10, a VC-3 can comprise seven TUG-2s which shall be numbered from #1 to #7. Each TUG-2 can comprise a TU-2.

Thus any TU-2 can be allocated a two-figure address in the form #L, #M, where L designates the TUG-2 number (1 to 7) and M is always 0. The location of the columns in the VC-3 occupied by TU-2 (L, 0) is given by the formula:

Xth column = $2 + [L–1] + 7 \times [X–1]$ for X = 1 to 12.

Thus TU-2 (1,0) resides in columns 2, 9, … and 79 of the VC-3, and TU-2 (7,0) resides in columns 8, 15, …. and 85 of the VC-3. A full listing of the location of the TU-2 columns with the VC-3 frame is given in Appendix IV.

7.3.12 Numbering of TU-12s in a VC-3

Each TUG-2 can comprise three TU-12s which shall be numbered #1 to #3.

Thus any TU-12 can be allocated a two-figure address in the form #L, #M, where L designates the TUG-2 number (1 to 7) and M designates the TU-12 number (1 to 3). The location of the columns in the VC-3 occupied by TU-12 (L, M) is given by the formula:

Xth column = $2 + [L–1] + 7 \times [M–1] + 21 \times [X–1]$ for X = 1 to 4.

Thus TU-12 (1,1) resides in columns 2, 23, 44 and 65 of the VC-3, and TU-12 (7,3) resides in columns 22, 43, 64 and 85 of the VC-3. A full listing of the location of the TU-12 columns with the VC-3 frame is given in Appendix V.

7.3.13 Numbering of TU-11s in a VC-3

Each TUG-2 can comprise four TU-11s which shall be numbered #1 to #4.

Thus any TU-11 can be allocated a two-figure address in the form #L, #M, where L designates the TUG-2 number (1 to 7) and M designates the TU-11 number (1 to 4). The location of the columns in the VC-3 occupied by TU-11 (L, M) is given by the formula:

Xth column = $2 + [L–1] + 7 \times [M–1] + 28 \times [X–1]$ for X = 1 to 3.

Thus TU-11 (1,1) resides in columns 2, 30 and 58 of the VC-3, and TU-11 (7,4) resides in columns 29, 57 and 85 of the VC-3. A full listing of the location of the TU-11 columns with the VC-3 frame is given in Appendix VI.

NOTE – The time slot number contained in Figures 7-26 to 7-28 should not be interpreted as the tributary port number.

An external tributary signal may be assigned to a particular payload capacity using a connection function.

For example, at the VC-12 level:

– Tributary #1 – TU-12 (1,1,1);
– Tributary #2 – TU-12 (1,1,2);
– Tributary #3 – TU-12 (1,1,3);
– Tributary #4 – TU-12 (1,2,1);
– :
– Tributary #63 – TU-12 (3,7,3).

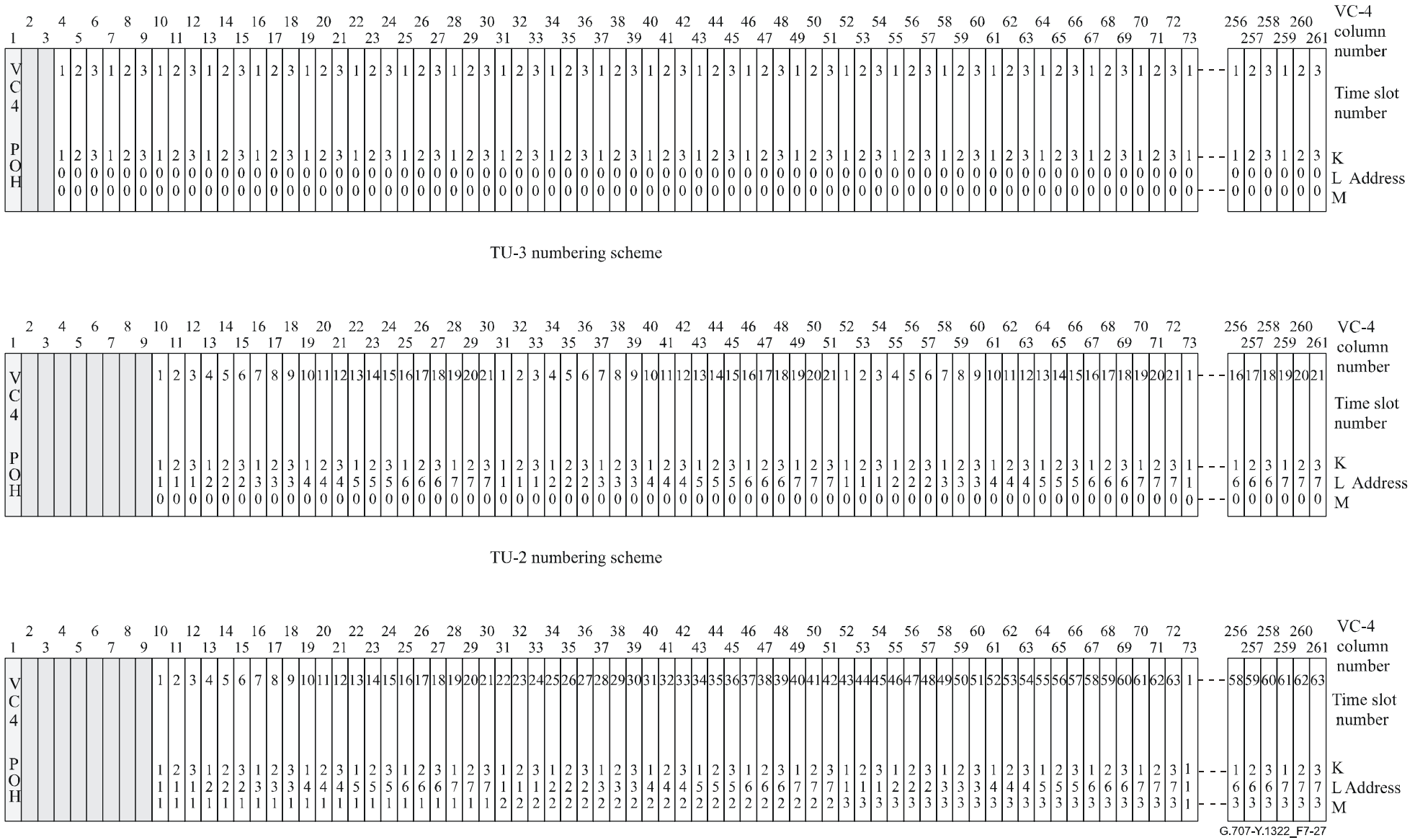


Figure 7-27 – TU-3, TU-2 and TU-12 numbering scheme within a VC-4

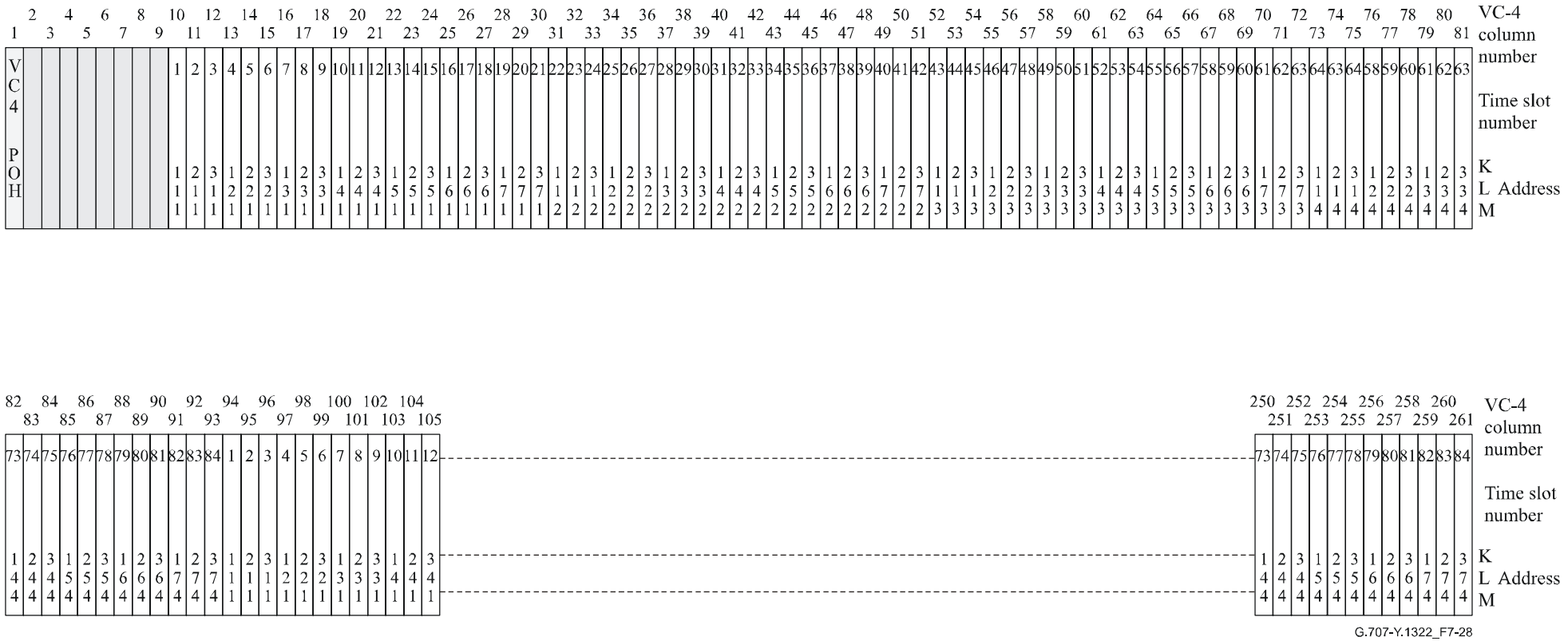


Figure 7-28 – TU-11 numbering scheme within a VC-4

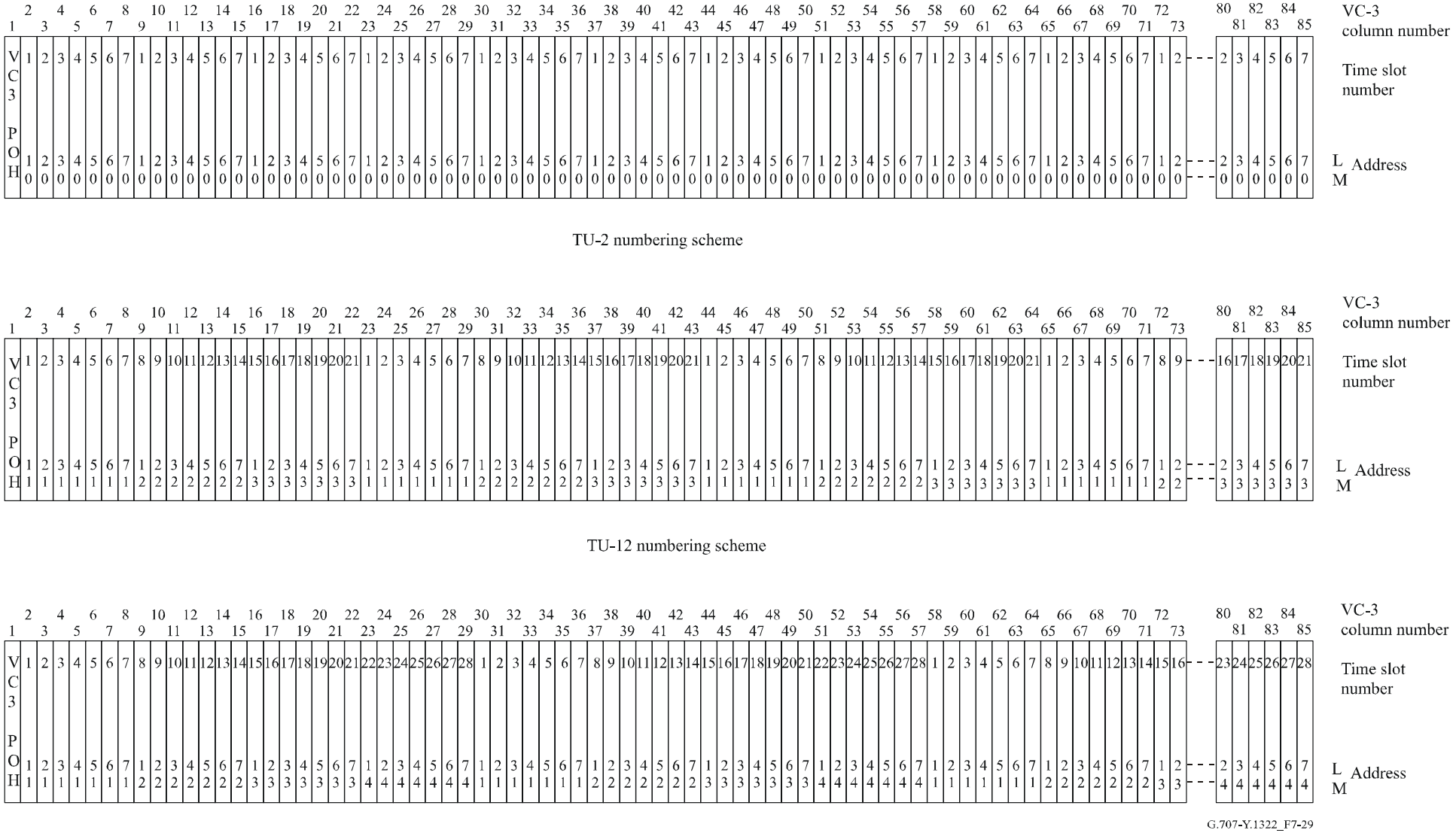


Figure 7-29 – TU-2, TU-12 and TU-11 numbering scheme within a VC-3

Table 7-1 – Allocation of TU-n capacity to time slots within a VC-4

Address #					Address #					Address #				
TU-3	TU-2	TU-12	TU-11	TS#	TU-3	TU-2	TU-12	TU-11	TS#	TU-3	TU-2	TU-12	TU-11	TS#
100	110	111	111	1	200	210	211	211	2	300	310	311	311	3
		112	112	22			212	212	23			312	312	24
		113	113	43			213	213	44			313	313	45
			114	64				214	65				314	66
	120	121	121	4		220	221	221	5		320	321	321	6
		122	122	25			222	222	26			322	322	27
		123	123	46			223	223	47			323	323	48
			124	67				224	68				324	69
	130	131	131	7		230	231	231	8		330	331	331	9
		132	132	28			232	232	29			332	332	30
		133	133	49			233	233	50			333	333	51
			134	70				234	71				334	72
	140	141	141	10		240	241	241	11		340	341	341	12
		142	142	31			242	242	32			342	342	33
		143	143	52			243	243	53			343	343	54
			144	73				244	74				344	75
	150	151	151	13		250	251	251	14		350	351	351	15
		152	152	34			252	252	35			352	352	36
		153	153	55			253	253	56			353	353	57
			154	76				254	77				354	78
	160	161	161	16		260	261	261	17		360	361	361	18
		162	162	37			262	262	38			362	362	39
		163	163	58			263	263	59			363	363	60
			164	79				264	80				364	81
	170	171	171	19		270	271	271	20		370	371	371	21
		172	172	40			272	272	41			372	372	42
		173	173	61			273	273	62			373	373	63
			174	82				274	83				374	84
Address = TUG-3#, TUG-2#, TU-1# = #K, #L, #M														

Table 7-2 – Allocation of TU-n capacity to time slots within a VC-3

Address #			
TU-2	**TU-12**	**TU-11**	**TS#**
10	11	11	1
	12	12	8
	13	13	15
		14	22
20	21	21	2
	22	22	9
	23	23	16
		24	23
30	31	31	3
	32	32	10
	33	33	17
		34	24
40	41	41	4
	42	42	11
	43	43	18
		44	25
50	51	51	5
	52	52	12
	53	53	19
		54	26
60	61	61	6
	62	62	13
	63	63	20
		64	27
70	71	71	7
	72	72	14
	73	73	21
		74	28
Address = TUG-2#, TU-1# = #L, #M			

8 Pointers

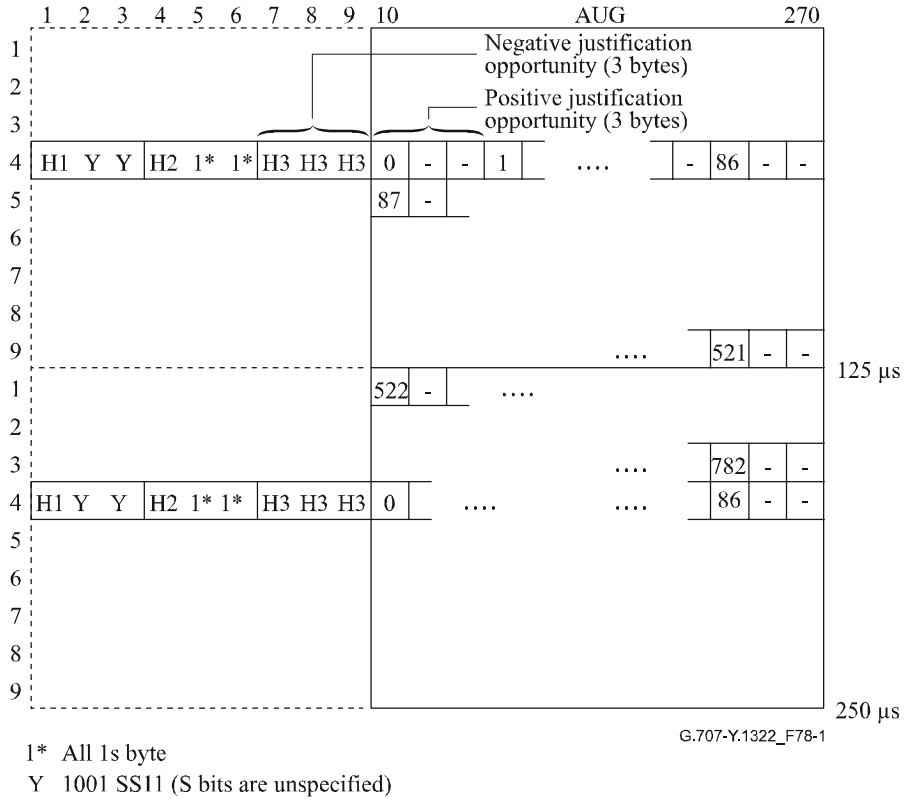
8.1 AU-n pointer

The AU-n pointer provides a method of allowing flexible and dynamic alignment of the VC-n within the AU-n frame.

Dynamic alignment means that the VC-n is allowed to "float" within the AU-n frame. Thus, the pointer is able to accommodate differences, not only in the phases of the VC-n and the SOH, but also in the frame rates.

8.1.1 AU-n pointer location

The AU-4 pointer is contained in bytes H1, H2 and H3 as shown in Figure 8-1. The three individual AU-3 pointers are contained in three separate H1, H2 and H3 bytes as shown in Figure 8-2.



1* All 1s byte
Y 1001 SS11 (S bits are unspecified)

Figure 8-1 – AU-4 pointer offset numbering

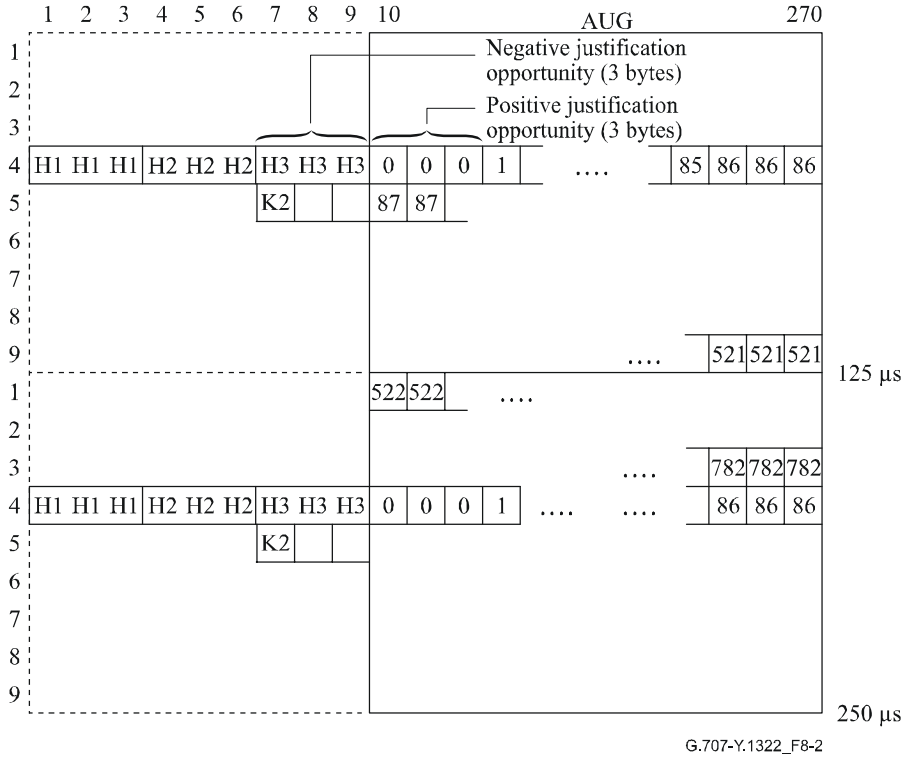


Figure 8-2 – AU-3 pointer offset numbering

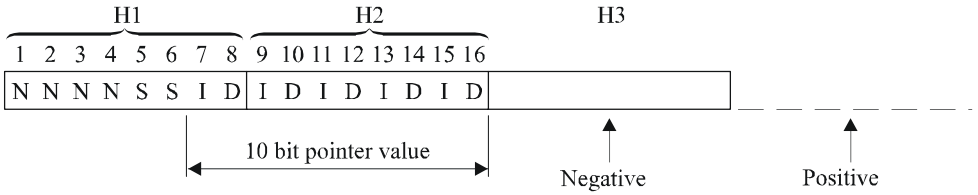
8.1.2 AU-n pointer value

The pointer contained in H1 and H2 designates the location of the byte where the VC-n begins. The two bytes allocated to the pointer function can be viewed as one word as shown in Figure 8-3. The last ten bits (bits 7-16) of the pointer word carry the pointer value.

As illustrated in Figure 8-3, the AU-4 pointer value is a binary number with a range of 0 to 782 which indicates the offset, in three-byte increments, between the pointer and the first byte of the VC-4 (see Figure 8-1). Figure 8-3 also indicates one additional valid pointer, the concatenation indication. The concatenation indication is indicated by "1001" in bits 1-4, bits 5-6 unspecified, and ten "1"s in bits 7-16. The AU-4 pointer is set to concatenation indication for AU-4 concatenation (see 8.1.7).

As illustrated in Figure 8-3, the AU-3 pointer value is also a binary number with a range of 0 to 782. Since there are three AU-3s in the AUG-1, each AU-3 has its own associated H1, H2 and H3 bytes. As shown in Figure 8-2, the H bytes are shown in sequence. The first H1, H2, H3 set refers to the first AU-3, and the second set to the second AU-3, and so on. For the AU-3s, each pointer operates independently.

In all cases, the AU-n pointer bytes are not counted in the offset. For example, in an AU-4, the pointer value of 0 indicates that the VC-4 starts in the byte location that immediately follows the last H3 byte, whereas an offset of 87 indicates that the VC-4 starts three bytes after the K2 byte.



I Increment
D Decrement
N New data flag

New data flag
– Enabled when at least 3 out of 4 bits match "1001"
– Disabled when at least 3 out of 4 bits match "0110"
– Invalid with other codes

Negative justification
– Invert 5 D-bits
– Accept majority vote

Pointer value (b7-b16)
– Normal range is:
for AU-4, AU-3: 0-782 decimal
for TU-3: 0-764 decimal

Positive justification
– Invert 5 I-bits
– Accept majority vote

Concatenation indication
– 1001SS1111111111 (SS bits are unspecified)

SS bits	AU-n/TU-n type
10	AU-4, AU-4-Xc, AU-3, TU-3

G.707-Y.1322_F8-3

Figure 8-3 – AU-n/TU-3 pointer (H1, H2, H3) coding

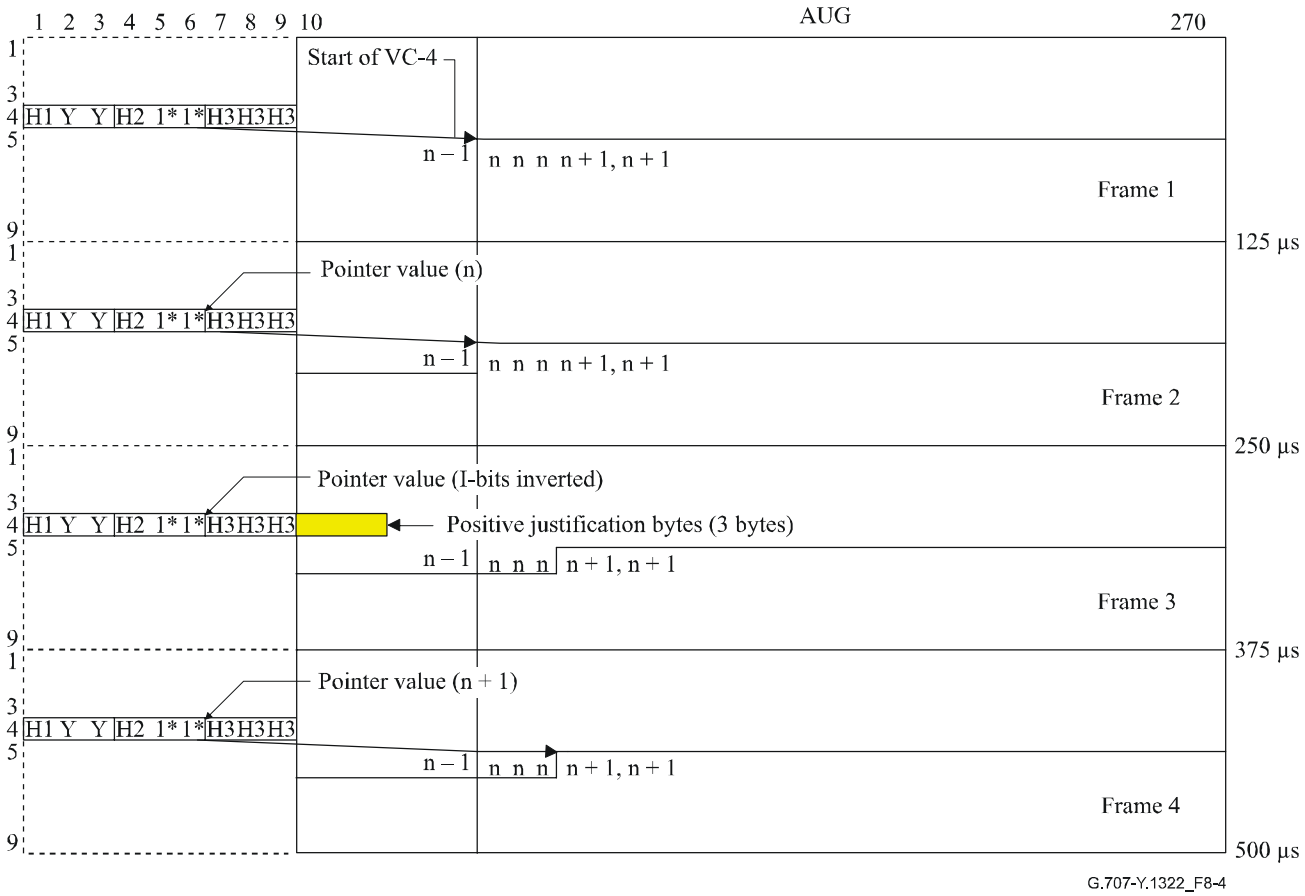
NOTE 1 – The AU-4, AU-4-Xc, AU-3 SS bits were included in the pointer detection algorithm (refer to the 1997 version of ITU-T Rec. G.783). Since the 2000 versions of ITU-T Recs G.783 and G.806, the SS bits are excluded from the AU-n pointer detection algorithm.

NOTE 2 – The pointer is set to all "1"s when AIS occurs.

8.1.3 Frequency justification

If there is a frequency offset between the frame rate of the AUG-N and that of the VC-n, then the pointer value will be incremented or decremented as needed, accompanied by a corresponding positive or negative justification byte or bytes. Consecutive pointer operations must be separated by at least three frames (i.e., every fourth frame) in which the pointer value remains constant.

If the frame rate of the VC-n is too slow with respect to that of the AUG-N, then the alignment of the VC-n must periodically slip back in time and the pointer value must be incremented by one. This operation is indicated by inverting bits 7, 9, 11, 13 and 15 (I-bits) of the pointer word to allow 5-bit majority voting at the receiver. Three positive justification bytes appear immediately after the last H3 byte in the AU-4 frame containing inverted I-bits. Subsequent pointers will contain the new offset. This is illustrated in Figure 8-4.



1* All 1s byte
Y 1001 SS11 (S bits are unspecified)

Figure 8-4 – AU-4 pointer adjustment operation – Positive justification

For AU-3 frames, a positive justification byte appears immediately after the individual H3 byte of the AU-3 frame containing inverted I-bits. Subsequent pointers will contain the new offset. This is illustrated in Figure 8-5.

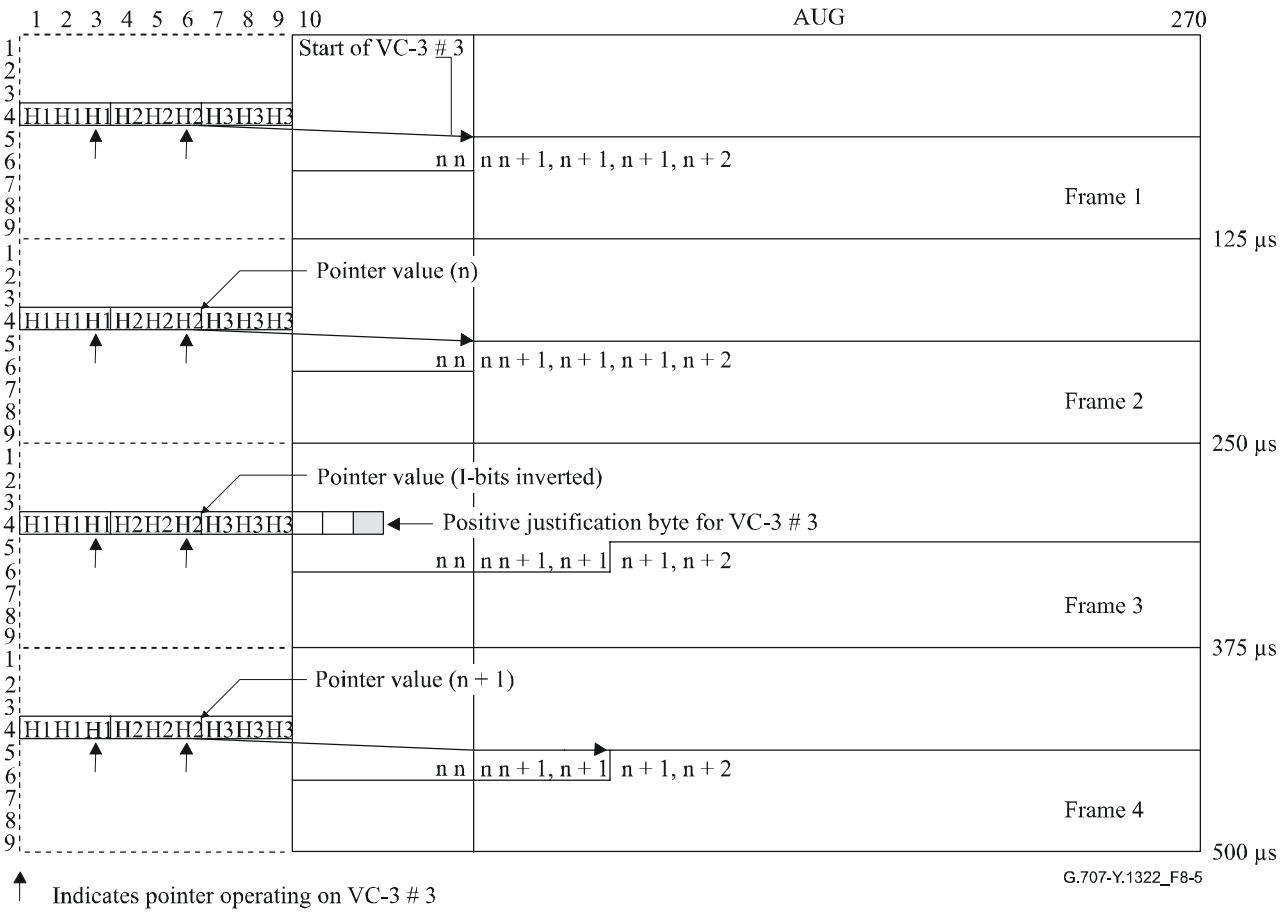
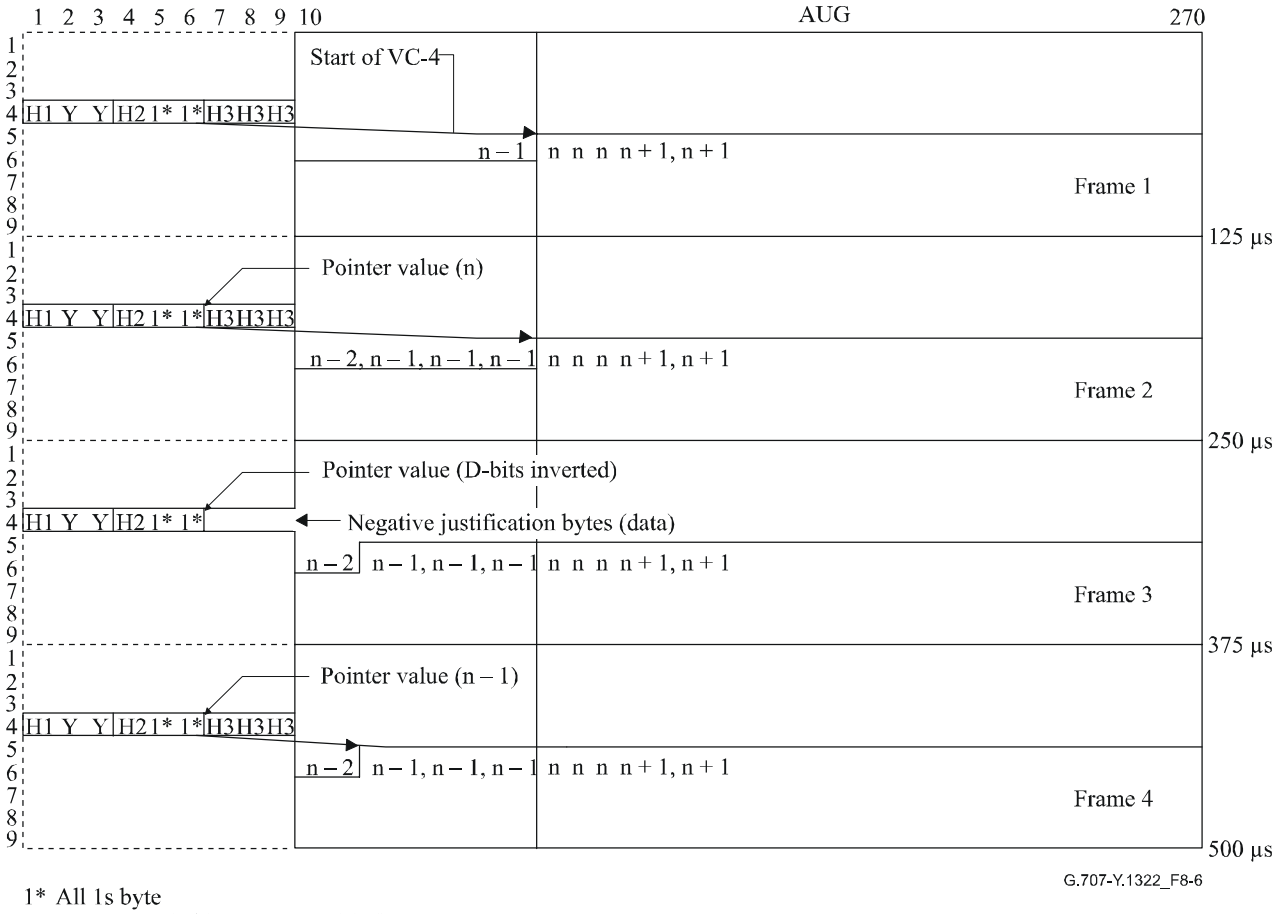


Figure 8-5 – AU-3 pointer adjustment operation – Positive justification

If the frame rate of the VC-n is too fast with respect to that of the AUG-N, then the alignment of the VC-n must periodically be advanced in time and the pointer value must be decremented by one. This operation is indicated by inverting bits 8, 10, 12, 14 and 16 (D-bits) of the pointer word to allow 5-bit majority voting at the receiver. Three negative justification bytes appear in the H3 bytes in the AU-4 frame containing inverted D-bits. Subsequent pointers will contain the new offset. This is illustrated in Figure 8-6.



1* All 1s byte
Y 1001 SS11 (S bits are unspecified)

Figure 8-6 – AU-4 pointer adjustment operation – Negative justification

For AU-3 frames, a negative justification byte appears in the individual H3 byte of the AU-3 frame containing inverted D-bits. Subsequent pointers will contain the new offset. This is illustrated in Figure 8-7.

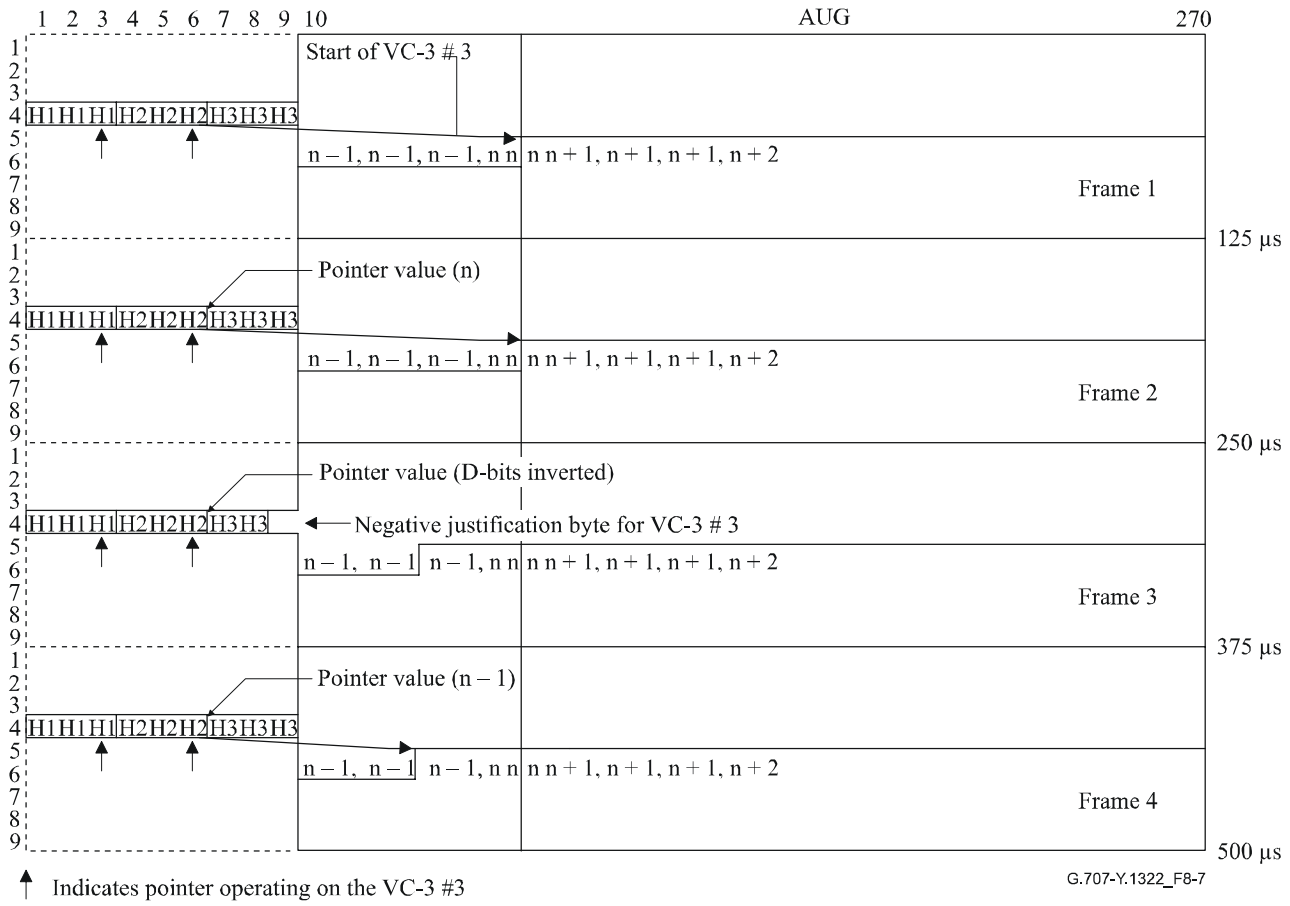


Figure 8-7 – AU-3 pointer adjustment operation – Negative justification

8.1.4 New data flag (NDF)

Bits 1-4 (N-bits) of the pointer word carry an NDF which allows an arbitrary change of the pointer value if that change is due to a change in the payload.

Four bits are allocated to the flag to allow error correction. Normal operation is indicated by a "0110" code in the N-bits. NDF is indicated by inversion of the N-bits to "1001". An NDF should be interpreted as enabled when three or more of the four bits match the pattern "1001". An NDF should be interpreted as disabled when three or more of the four bits match the pattern "0110". The remaining values (i.e., "0000", "0011", "0101", "1010", "1100" and "1111") should be interpreted as invalid. The new alignment is indicated by the pointer value accompanying the NDF and takes effect at the offset indicated.

8.1.5 Pointer generation

The following summarizes the rules for generating the AU-n pointers:

1) During normal operation, the pointer locates the start of the VC-n within the AU-n frame. The NDF is set to "0110".

2) The pointer value can only be changed by operation 3, 4 or 5.

3) If a positive justification is required, the current pointer value is sent with the I-bits inverted and the subsequent positive justification opportunity is filled with dummy information. Subsequent pointers contain the previous pointer value incremented by one. If the previous

pointer is at its maximum value, the subsequent pointer is set to zero. No subsequent increment or decrement operation is allowed for at least three frames following this operation.

4) If a negative justification is required, the current pointer value is sent with the D-bits inverted and the subsequent negative justification opportunity is overwritten with actual data. Subsequent pointers contain the previous pointer value decremented by one. If the previous pointer value is zero, the subsequent pointer is set to its maximum value. No subsequent increment or decrement operation is allowed for at least three frames following this operation.

5) If the alignment of the VC-n changes for any reason other than rules 3 or 4, the new pointer value shall be sent accompanied by NDF set to "1001". The NDF only appears in the first frame that contains the new values. The new location of the VC-n begins at the first occurrence of the offset indicated by the new pointer. No subsequent increment or decrement operation is allowed for at least three frames following this operation.

8.1.6 Pointer interpretation

The following summarizes the rules for interpreting the AU-n pointers:

1) During normal operation, the pointer locates the start of the VC-n within the AU-n frame.

2) Any variation from the current pointer value is ignored unless a consistent new value is received three times consecutively or it is preceded by one of the rules 3, 4 or 5. Any consistent new value received three times consecutively overrides (i.e., takes priority over) rules 3 or 4.

3) If the majority of the I-bits of the pointer word are inverted, a positive justification operation is indicated. Subsequent pointer values shall be incremented by one.

4) If the majority of the D-bits of the pointer word are inverted, a negative justification operation is indicated. Subsequent pointer values shall be decremented by one.

5) If the NDF is interpreted as enabled, then the coincident pointer value shall replace the current one at the offset indicated by the new pointer value unless the receiver is in a state that corresponds to a loss of pointer.

8.1.7 AU-4 concatenation

See clauses 11.1 and 11.2.

8.2 TU-3 pointer

The TU-3 pointer provides a method of allowing flexible and dynamic alignment of VC-3 within the TU-3 frame, independent of the actual content of the VC-3.

8.2.1 TU-3 pointer location

Three individual TU-3 pointers are contained in three separate H1, H2 and H3 bytes as shown in Figure 8-8.

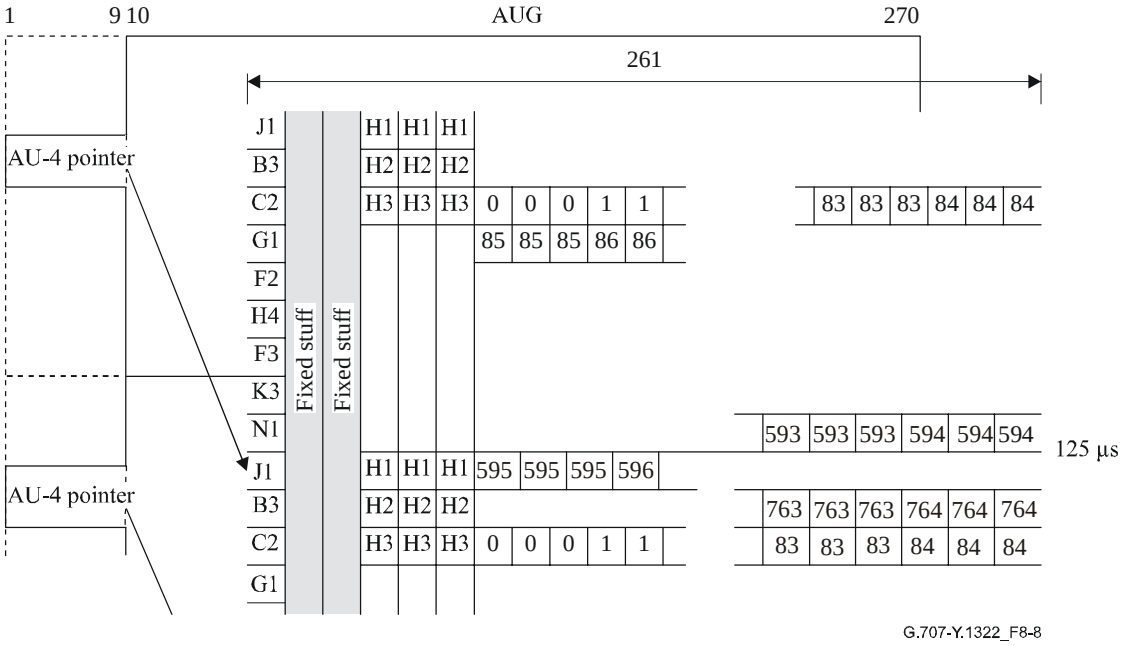


Figure 8-8 – TU-3 pointer offset numbering

8.2.2 TU-3 pointer value

The TU-3 pointer value contained in H1 and H2 designates the location of the byte where the VC-3 begins. The two bytes allocated to the pointer function can be viewed as one word as shown in Figure 8-3. The last ten bits (bits 7-16) of the pointer word carry the pointer value.

The TU-3 pointer value is a binary number with a range of 0-764 which indicates the offset between the pointer and the first byte of the VC-3 as shown in Figure 8-8.

8.2.3 Frequency justification

If there is a frequency offset between the TU-3 frame rate and that of the VC-3, then the pointer value will be incremented or decremented as needed accompanied by a corresponding positive or negative justification byte. Consecutive pointer operations must be separated by at least three frames in which the pointer value remains constant.

If the frame rate of the VC-3 is too slow with respect to that of the TU-3 frame rate, then the alignment of the VC-3 must periodically slip back in time and the pointer must be incremented by one. This operation is indicated by inverting bits 7, 9, 11, 13 and 15 (I-bits) of the pointer word to allow 5-bit majority voting at the receiver. A positive justification byte appears immediately after the individual H3 byte in the TU-3 frame containing inverted I-bits. Subsequent TU-3 pointers will contain the new offset.

If the frame rate of the VC-3 is too fast with respect to that of the TU-3 frame rate, then the alignment of the VC-3 must be periodically advanced in time and the pointer must be decremented by one. This operation is indicated by inverting bits 8, 10, 12, 14 and 16 (D-bits) of the pointer word to allow 5-bit majority voting at the receiver. A negative justification byte appears in the individual H3 byte in the TU-3 frame containing inverted D-bits. Subsequent TU-3 pointers will contain the new offset.

8.2.4 New data flag (NDF)

Bits 1-4 (N-bits) of the pointer word carry an NDF which allows an arbitrary change of the value of the pointer if that change is due to a change in the VC-3.

Four bits are allocated to the flag to allow error correction. Normal operation is indicated by a "0110" code in the N-bits. NDF is indicated by inversion of the N-bits to "1001". An NDF should be interpreted as enabled when three or more of the four bits match the pattern "1001". An NDF should be interpreted as disabled when three or more of the four bits match the pattern "0110". The remaining values (i.e., "0000", "0011", "0101", "1010", "1100" and "1111") should be interpreted as invalid. The new alignment is indicated by the pointer value accompanying the NDF and takes effect at the offset indicated.

8.2.5 Pointer generation

The following summarizes the rules for generating the TU-3 pointers:

1) During normal operation, the pointer locates the start of the VC-3 within the TU-3 frame. The NDF is set to "0110".
2) The pointer value can only be changed by operation 3, 4 or 5.
3) If a positive justification is required, the current pointer value is sent with the I-bits inverted and the subsequent positive justification opportunity is filled with dummy information. Subsequent pointers contain the previous pointer value incremented by one. If the previous pointer is at its maximum value, the subsequent pointer is set to zero. No subsequent increment or decrement operation is allowed for at least three frames following this operation.
4) If a negative justification is required, the current pointer value is sent with the D-bits inverted and the subsequent negative justification opportunity is overwritten with actual data. Subsequent pointers contain the previous pointer value decremented by one. If the previous pointer value is zero, the subsequent pointer is set to its maximum value. No subsequent increment or decrement operation is allowed for at least three frames following this operation.
5) If the alignment of the VC-3 changes for any reason other than rules 3 or 4, the new pointer value shall be sent accompanied by the NDF set to "1001". The NDF only appears in the first frame that contains the new value. The new VC-3 location begins at the first occurrence of the offset indicated by the new pointer. No subsequent increment or decrement operation is allowed for at least three frames following this operation.

8.2.6 Pointer interpretation

The following summarizes the rules for interpreting the TU-3 pointers:

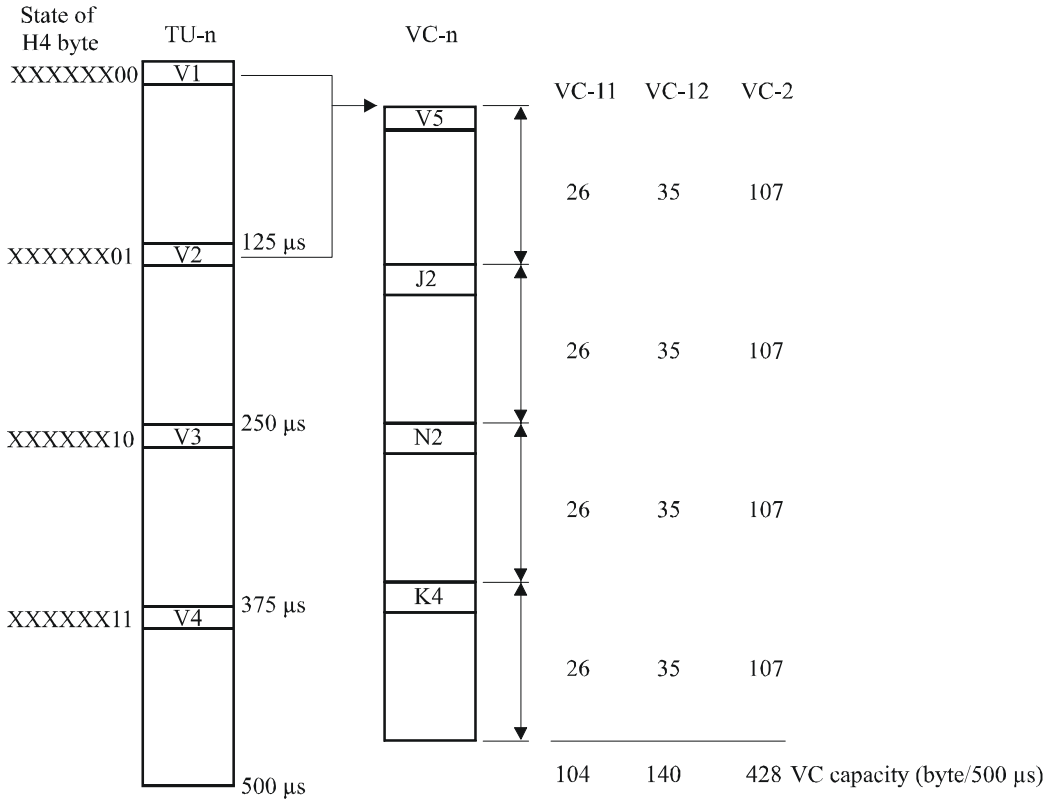
1) During normal operation the pointer locates the start of the VC-3 within the TU-3 frame.
2) Any variation from the current pointer value is ignored unless a consistent new value is received three times consecutively or it is preceded by one of rules 3, 4 or 5. Any consistent new value received three times consecutively overrides (i.e., takes priority over) rules 3 or 4.
3) If the majority of the I-bits of the pointer word are inverted, a positive justification is indicated. Subsequent pointer values shall be incremented by one.
4) If the majority of the D-bits of the pointer word are inverted, a negative justification is indicated. Subsequent pointer values shall be decremented by one.
5) If the NDF is interpreted as enabled, then the coincident pointer value shall replace the current one at the offset indicated by the new pointer value unless the receiver is in a state that corresponds to a loss of pointer.

8.3 TU-2, TU-12 and TU-11 pointers

The TU-11, TU-12 and TU-2 pointers provide a method of allowing flexible and dynamic alignment of the VC-11, VC-12 and VC-2 within the TU-11, TU-12 and TU-2 multiframes, independent of the actual contents of the VC-11, VC-12 and VC-2.

8.3.1 TU-2, TU-12 and TU-11 pointer location

The TU-2, TU-12 and TU-11 pointers are contained in the V1 and V2 bytes as illustrated in Figure 8-9.



TU Tributary Unit
VC Virtual Container
V1 TU Pointer 1
V2 TU Pointer 2
V3 TU Pointer 3 (action)
V4 Reserved

NOTE – V1, V2, V3 and V4 bytes are part of the TU-n and are terminated at the pointer processor.

Figure 8-9 – Virtual container mapping in multiframed tributary unit

8.3.2 TU-2, TU-12 and TU-11 pointer value

The tributary unit pointer word is shown in Figure 8-10. The two S bits (bits 5 and 6) indicate the tributary unit type.

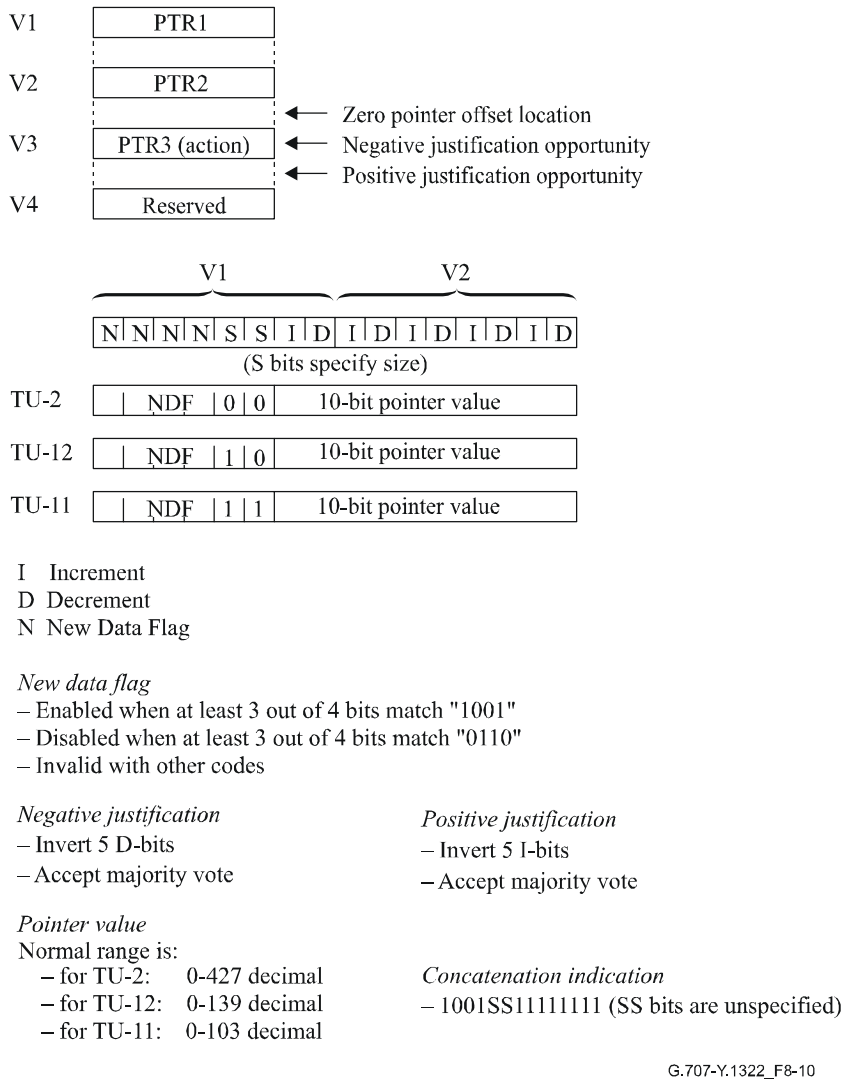


Figure 8-10 – TU-2, TU-12 and TU-11 pointer coding

The pointer value (bits 7-16) is a binary number which indicates the offset from V2 to the first byte of the VC-2, VC-12 or VC-11. The range of the offset is different for each of the tributary unit sizes as illustrated in Figure 8-11. The pointer bytes are not counted in the offset calculation.

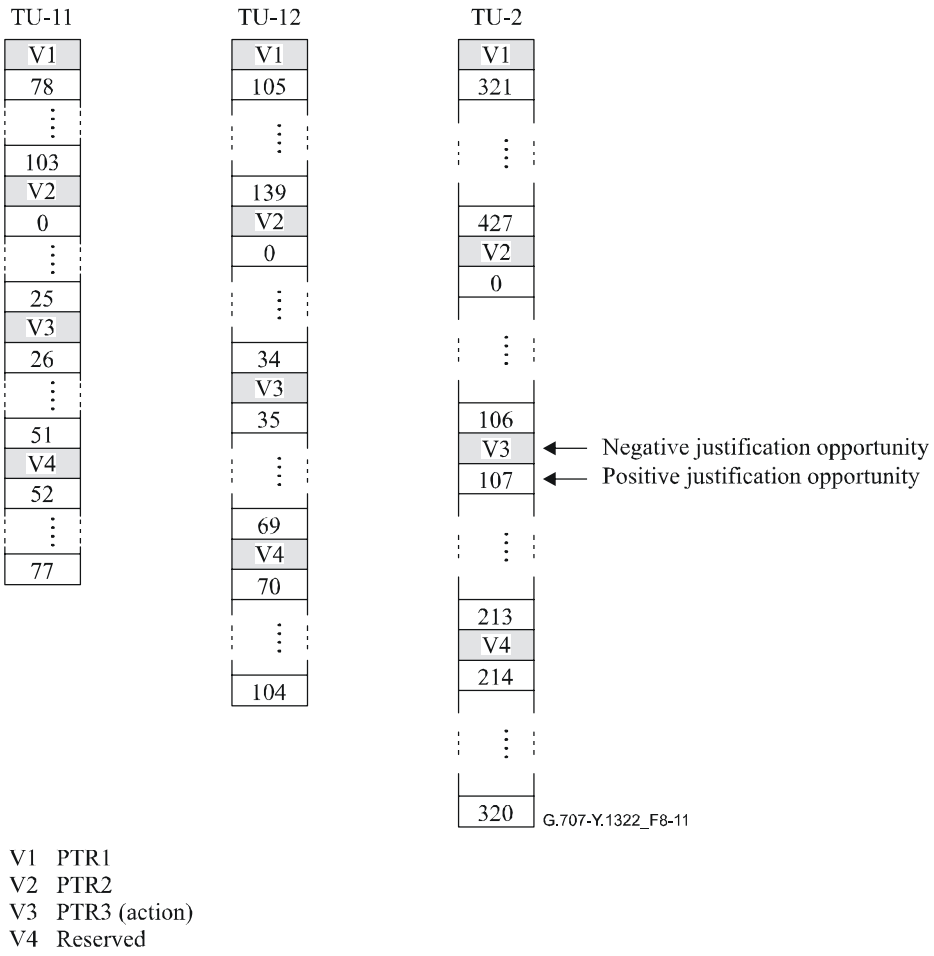


Figure 8-11 – TU-2, TU-12 and TU-11 pointer offsets

8.3.3 TU-2, TU-12 and TU-11 frequency justification

The TU-2, TU-12 and TU-11 pointers are used to frequency justify the VC-2, VC-12 and VC-11 exactly in the same way that the TU-3 pointer is used to frequency justify the VC-3. A positive justification opportunity immediately follows the V3 byte. Additionally, V3 serves as the negative justification opportunity such that when the opportunity is taken, V3 is overwritten by data. This is also shown in Figure 8-11. The indication of whether or not a justification opportunity has been taken is provided by the I- and D-bits of the pointer in the current tributary unit multiframe. The value contained in V3 when not being used for a negative justification is not defined. The receiver is required to ignore the value contained in V3 whenever it is not used for negative justification.

8.3.4 New data flag (NDF)

Bits 1-4 (N-bits) of the pointer word carry an NDF. It is the mechanism which allows an arbitrary change of the value of a pointer.

As with the TU-3 pointer NDF, the normal value is "0110", and the value "1001" indicates a new alignment for the VC-n, and possibly new size. An NDF should be interpreted as enabled when three or more of the four bits match the pattern "1001". An NDF should be interpreted as disabled when three or more of the four bits match the pattern "0110". The remaining values (i.e., "0000", "0011", "0101", "1010", "1100" and "1111") should be interpreted as invalid. The new alignment is indicated by the pointer value and size value accompanying the NDF and takes effect at the offset indicated.

8.3.5 TU-2, TU-12 and TU-11 pointer generation and interpretation

The rules for generating and interpreting the TU-2, TU-12 and TU-11 pointers for the VC-2, VC-12 and VC-11 are an extension to the rules provided in clauses 8.2.5 and 8.2.6 for the TU-3 pointer with the following modification:

– The term TU-3 is replaced with TU-2, TU-12 or TU-11 and the term VC-3 is replaced with VC-2, VC-12 or VC-11.

8.3.6 TU-2 concatenation

See clauses 11.3 and 11.4.

8.3.7 TU-2, TU-12 and TU-11 sizes

Bits 5 and 6 of TU-2, TU-12 and TU-11 pointers indicate the size of the TU-m. Three sizes are currently provided; they are defined in Table 8-1 below:

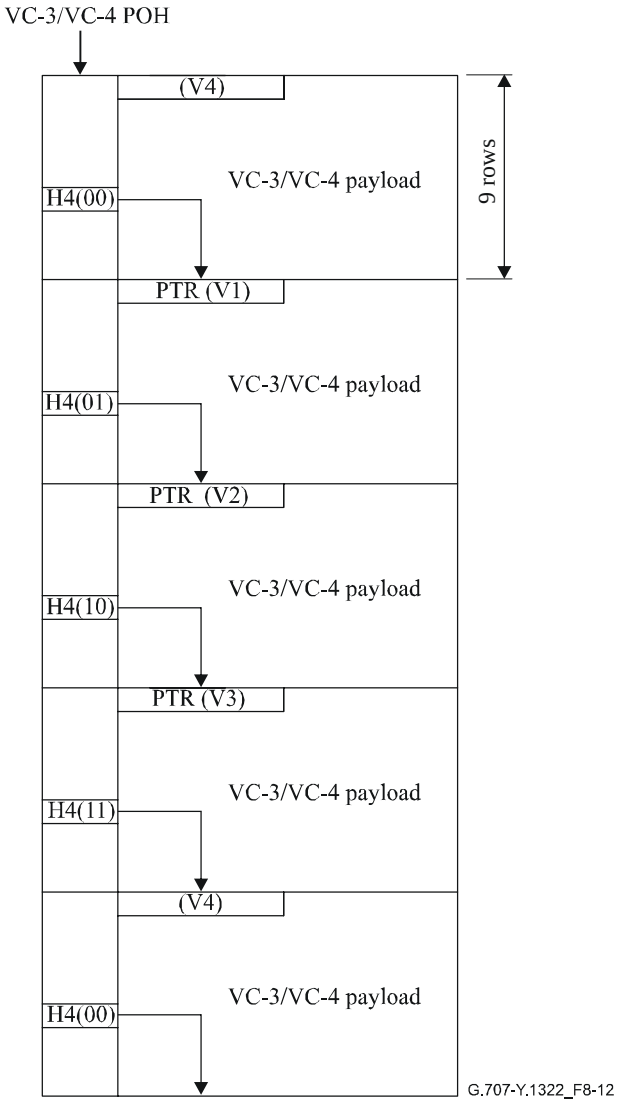
Table 8-1 – TU-2, TU-12 and TU-11 sizes

Size	Designation	TU-m pointer range (in 500 µs)
00	TU-2	0-427
10	TU-12	0-139
11	TU-11	0-103
NOTE – This technique is only used at the TU-2, TU-12 and TU-11 levels.		

8.3.8 TU-2, TU-12 and TU-11 multiframe indication byte

TU-2, TU-12 and TU-11 multiframe indication byte (H4) relates to the lowest level of the multiplexing structure and provides a 500 µs (4-frame) multiframe identifying frames containing the TU-2, TU-12 or TU-11 pointers. Figure 8-9 shows the VC-2, VC-12 and VC-11 mapping in the multiframed TU-2, TU-12 and TU-11.

The value of the H4 byte, read from the VC-4/VC-3 POH, identifies the frame phase of the next VC-4/VC-3 payload as shown in Figure 8-12. The coding of the H4 byte is illustrated in Figure 8-13.



In H4 (XY), XY represent bits 7 and 8 of H4.

Figure 8-12 – TU-2, TU-12 and TU-11 500 µs multiframe indication using H4 byte

H4 bits									
1	2	3	4	5	6	7	8	Frame No.	Time
X	X	1	1	X	X	0	0	0	0
X	X	1	1	X	X	0	1	1	
X	X	1	1	X	X	1	0	2	
X	X	1	1	X	X	1	1	3	500 µs TU-m multiframe

X Bit reserved for future international standardization. Its content shall be set to "1" in the interim.

Figure 8-13 – Tributary unit multiframe indicator byte (H4) coding sequence

9 Overhead bytes description

9.1 Types of overhead

Several types of overhead have been identified for application in the SDH.

9.1.1 SOH

SOH information is added to the information payload to create an STM-N. It includes block framing information and information for maintenance, performance monitoring and other operational functions. The SOH information is further classified into regenerator section overhead (RSOH) which is terminated at regenerator functions and multiplex section overhead (MSOH) which passes transparently through regenerators and is terminated where the AUG-Ns are assembled and disassembled.

NOTE – The FEC overhead defined in clause 9.2.4 uses both RSOH and MSOH. As the FEC is defined for the multiplex section, the FEC overhead located in the RSOH is not terminated at regenerator functions.

The rows 1-3 of the SOH are designated as RSOH while rows 5-9 are designated to be MSOH. This is illustrated in Figure 9-3 for the case of STM-1.

The SOH description is given in clause 9.2.

9.1.2 Virtual container POH

Virtual container POH provides for integrity of communication between the point of assembly of a virtual container and its point of disassembly. Two categories of virtual container POH have been identified:

– *Higher order virtual container POH (VC-4/VC-3 POH)*

  VC-3 POH is added to either an assembly of TUG-2s or a container-3 to form a VC-3. VC-4 POH is added to either an assembly of TUG-3s or a container-4 to form a VC-4. Amongst the functions included within this overhead are virtual container path performance monitoring, alarm status indications, signals for maintenance purposes and multiplex structure indications (VC-4/VC-3 composition).

– *Lower order virtual container POH (VC-3/VC-2/VC-12/VC-11 POH)*

  Lower order VC-m (m=11, 12, 2, 3) POH is added to the Container-m to form a VC-m. Among the functions included in this overhead are virtual container path performance monitoring, signals for maintenance purposes and alarm status indications.

The POH descriptions are given in clause 9.3.

9.2 SOH description

9.2.1 SOH bytes location

The location of SOH bytes within an STM-N, $N \geq 1$, frame is identified by a three-coordinate vector S (a, b, c) where a (1 to 3, 5 to 9) represents the row number, b (1 to 9) represents a multi-column number and c (1 to N) represents the depth of the interleave within the multi-column. This is illustrated in Figure 9-1.

The relationship between the row and column numbers and the coordinates is given by:

- Row = a;
- Column = N (b–1) + c.

For example the K1 byte in an STM-1 is located at S (5, 4, 1) or at [5, 4] in [row, column] notation.

For STM-0, identification of the SOH bytes by a three-coordinate vector is unnecessary since all STM-0 SOH bytes have a <letter><number> name.

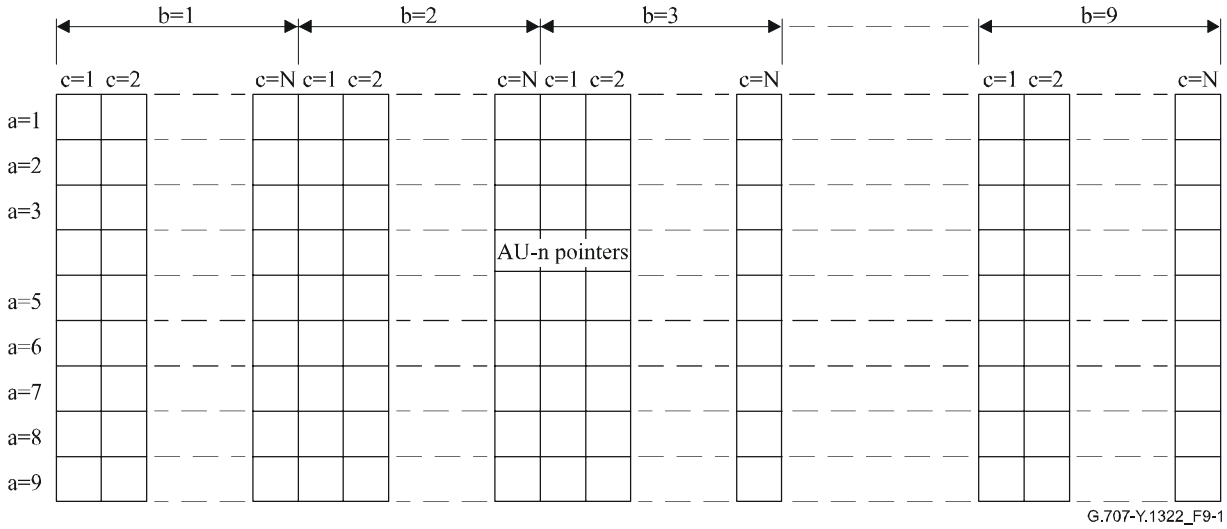


Figure 9-1 – Numbering of SOH byte locations for STM-N

The assignment of the various SOH bytes in the STM-0/1/4/16/64/256 frames is illustrated in Figures 9-2 to 9-7.

NOTE – Scrambling of the STM-N frames is described in clause 6.5.

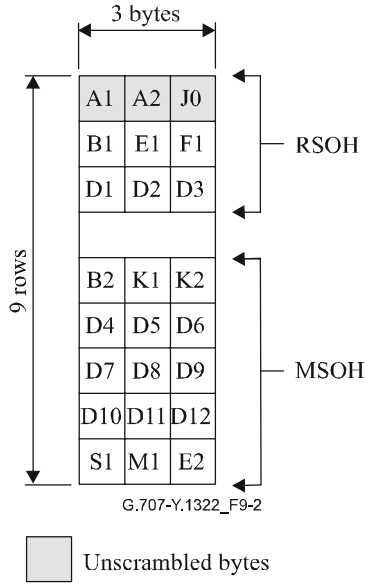
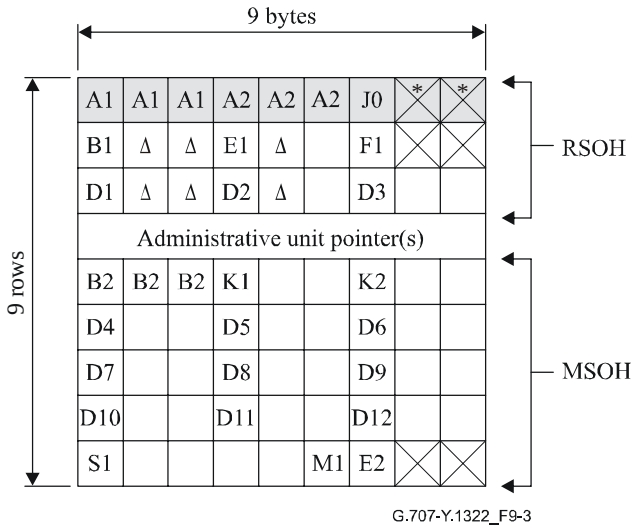


Figure 9-2 – STM-0 SOH



Unscrambled bytes

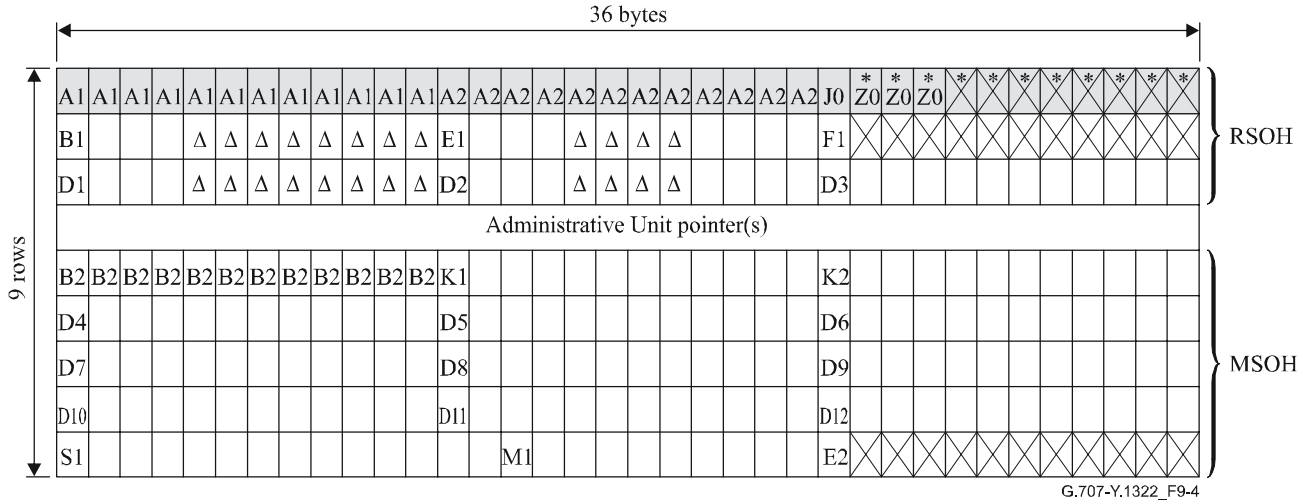
Bytes reserved for national use

* The content of these reserved bytes has to be carefully selected as they are not scrambled

Media-dependent bytes

NOTE – All unmarked bytes are reserved for future international standardization (for media-dependent, additional national use and other purposes).

Figure 9-3 – STM-1 SOH



Unscrambled bytes

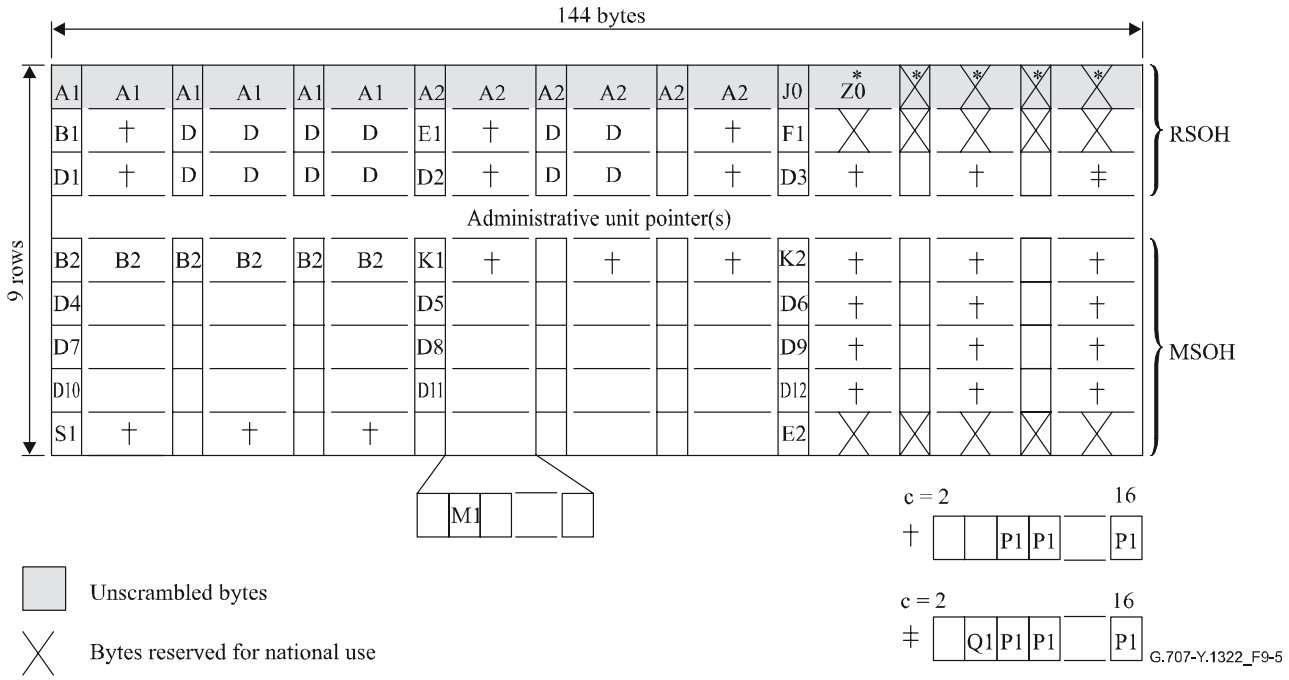
Bytes reserved for national use

* The content of these reserved bytes has to be carefully selected as they are not scrambled

Δ Media-dependent bytes

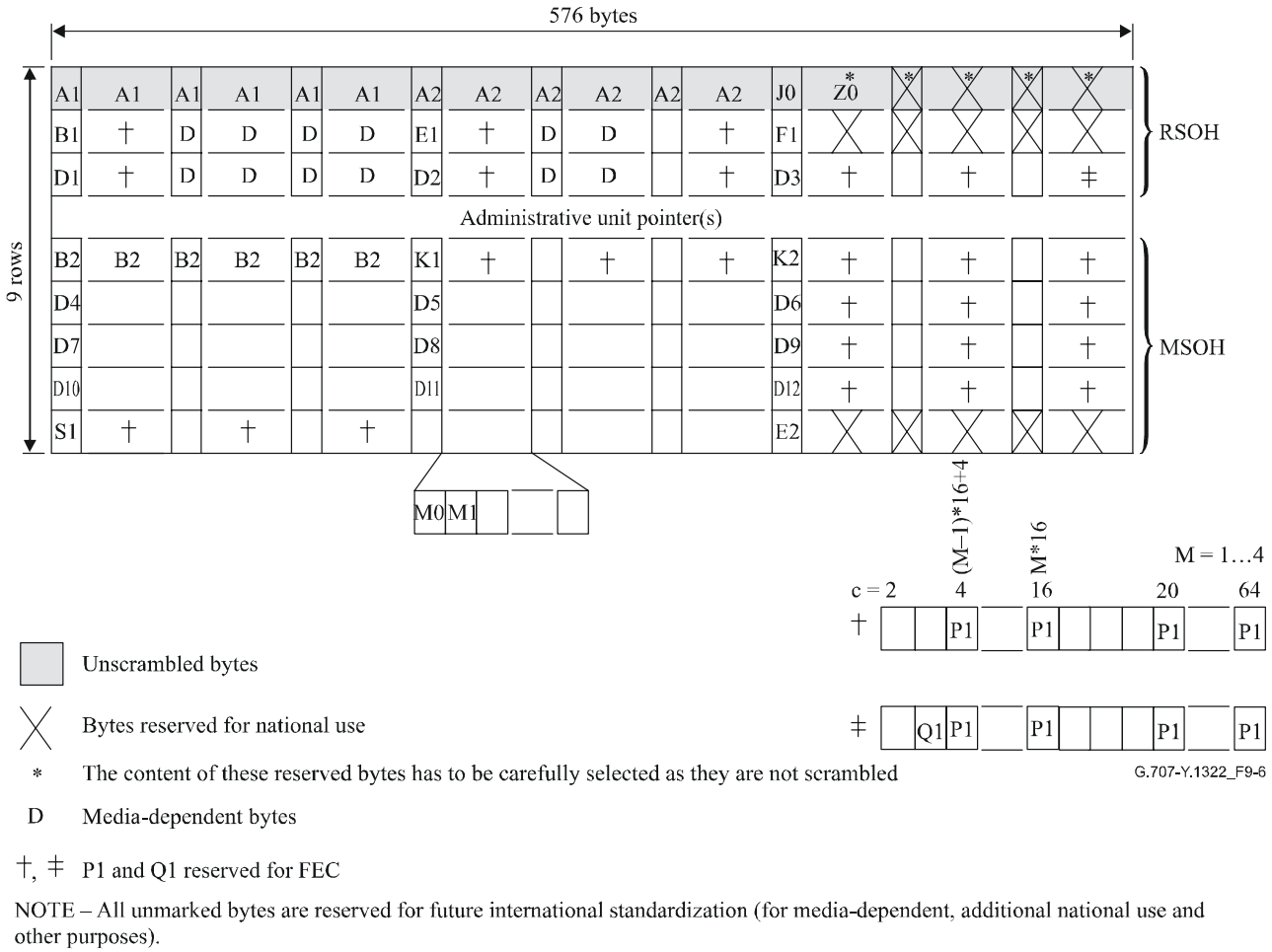
NOTE – All unmarked bytes are reserved for future international standardization (for media-dependent, additional national use and other purposes).

Figure 9-4 – STM-4 SOH



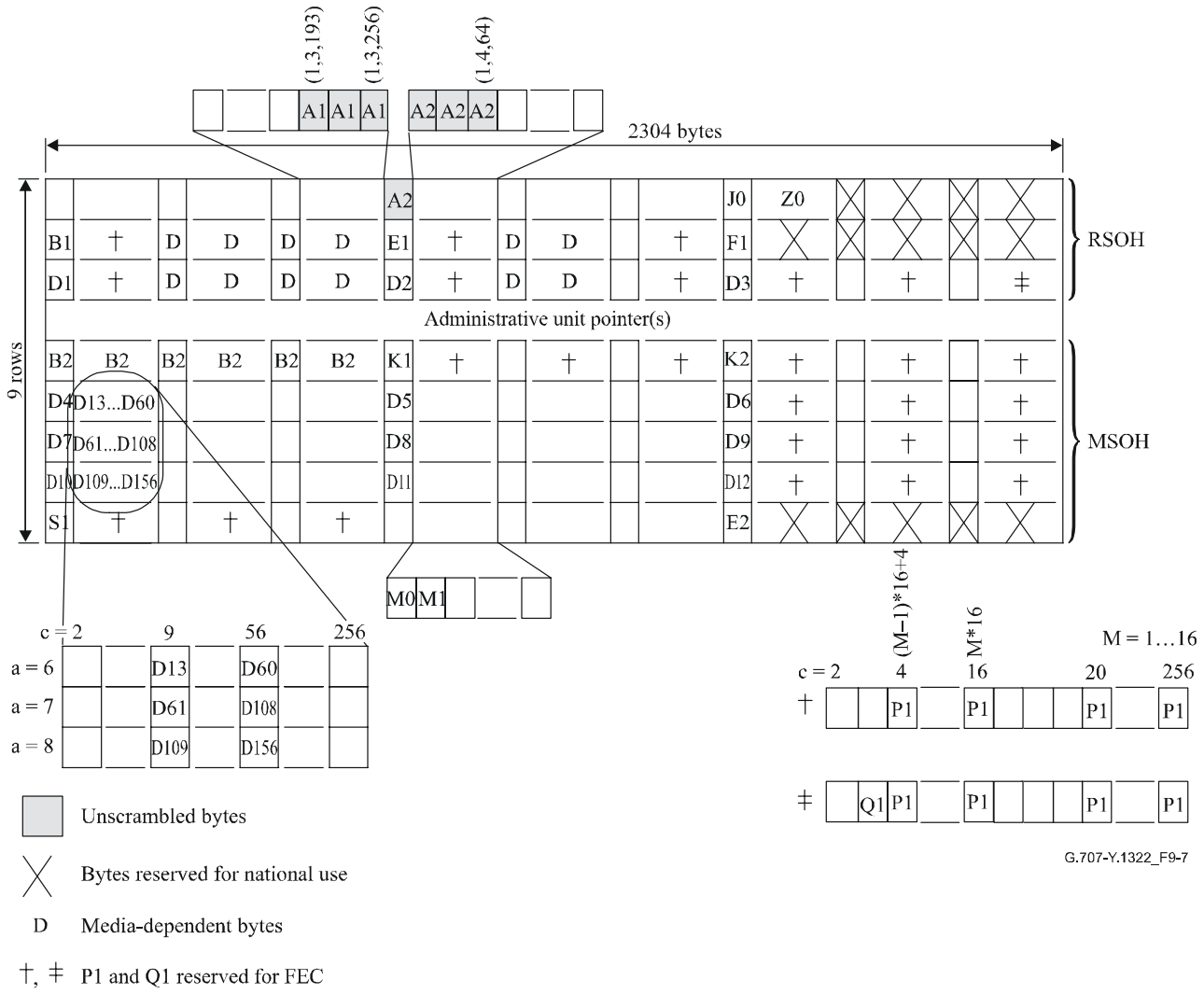
NOTE – All unmarked bytes are reserved for future international standardization (for media-dependent, additional national use and other purposes).

Figure 9-5 – STM-16 SOH



NOTE – All unmarked bytes are reserved for future international standardization (for media-dependent, additional national use and other purposes).

Figure 9-6 – STM-64 SOH



NOTE – All unmarked bytes are reserved for future international standardization (for media-dependent, additional national use and other purposes).

Figure 9-7 – STM-256 SOH

9.2.2 SOH bytes description

9.2.2.1 Framing: A1, A2

Two types of bytes are defined for framing:

– A1: 11110110

– A2: 00101000

The frame alignment word of an STM-0 frame is composed of one A1 byte followed by one A2 byte. The frame alignment word of an STM-N frame (N=1, 4, 16, 64) is composed of $3 \times N$ A1 bytes followed by $3 \times N$ A2 bytes. The frame alignment word of an STM-256 frame is composed of 64 A1 bytes in the locations S (1,3,193) [1,705] to S (1,3,256) [1,768] followed by 64 A2 bytes in the locations S (1,4,1) [1,769] to S (1,4,64) [1,832]. The bytes in locations S (1,1,1) [1,1] to S (1,3,192) [1,704] and S (1,4,65) [833] to S (1,9,256) [1,1536] are reserved for future international standardization (for media-dependent, additional national use and other purposes).

NOTE – For the reserved bytes in row 1 of the STM-256 frame, a pattern should be used that provides sufficient transitions and no significant DC unbalance after scrambling.

9.2.2.2 Regenerator section trace: J0

The J0 byte located at S (1,7,1) or [1,6N+1] in an STM-N is allocated to a regenerator section trace. This byte is used to transmit repetitively a section access point identifier so that a section receiver can verify its continued connection to the intended transmitter. Within a national network, or within the domain of a single operator, this section access point identifier may use either a single byte (containing the code 0-255) or the access point identifier format as defined in clause 3/G.831. At international boundaries, or at the boundaries between the networks of different operators, the format defined in clause 3/G.831 shall be used unless otherwise mutually agreed by the operators providing the transport.

A 16-byte frame is defined for the transmission of section access point identifiers where these conform to the definition contained in clause 3/G.831. The first byte of the 16-byte frame is a header byte and includes the result of a CRC-7 calculation over the previous frame. The following 15 bytes are used for the transport of 15 T.50 characters (international reference version) required for the section access point identifier. The 16-byte frame description is given in Table 9-1:

Table 9-1 – 16-byte frame for trail API

Byte #	**Value (bit 1, 2, …, 8)**							
1	1	C_1	C_2	C_3	C_4	C_5	C_6	C_7
2	0	X	X	X	X	X	X	X
3	0	X	X	X	X	X	X	X
:	:				:			
16	0	X	X	X	X	X	X	X

NOTE 1 – 1000 0000 0000 0000 in bit 1 of each byte is the trace identifier frame alignment signal.

NOTE 2 – $C_1C_2C_3C_4C_5C_6C_7$ is the result of the CRC-7 calculation over the previous frame. C_1 is the MSB. The description of this CRC-7 calculation is given in Annex B.

NOTE 3 – XXXXXXX represents a T.50 character.

For interworking of equipment employing the regenerator section trace function with old equipment implementing the STM identifier functionality (see Notes), the former shall be able to transmit the pattern "0000 0001" in J0.

NOTE 1 – STM identifier: C1.

NOTE 2 – In earlier versions of this Recommendation, the content of bytes located at S (1,7,1) or [1,6N+1] to S (1,7,N) or [1,7N] was defined as a unique identifier indicating the binary value of the multi-column, interleave depth coordinate, c. It may have been used to assist in frame alignment.

9.2.2.3 Spare: Z0

These bytes, which are located at positions S (1,7,2) or [1,6N+2] to S (1,7,N) or [1,7N], are reserved for future international standardization.

In case of interworking of equipment implementing the STM identifier functionality (see Note 1) and equipment employing the regenerator section trace function, these bytes shall be as defined in the note below.

NOTE 1 – STM identifier: C1.

NOTE 2 – In earlier versions of this Recommendation, the content of bytes located at S (1,7,1) or [1,6N+1] to S (1,7,N) or [1,7N] was defined as a unique identifier indicating the binary value of the multi-column, interleave depth coordinate, c. It may have been used to assist in frame alignment.

9.2.2.4 BIP-8: B1

One byte is allocated for regenerator section error monitoring. This function shall be a Bit Interleaved Parity 8 (BIP-8) code using even parity. The BIP-8 is computed over all bits of the previous STM-N frame after scrambling and is placed in byte B1 of the current frame before scrambling. (For details of the scrambling process, see clause 6.5.)

NOTE – Bit Interleaved Parity-X (BIP-X) code is defined in clause 3.13.

9.2.2.5 Orderwire: E1, E2

These two bytes may be used to provide orderwire channels for voice communication. E1 is part of the RSOH and may be accessed at regenerators. E2 is part of the MSOH and may be accessed at multiplex section terminations.

9.2.2.6 User channel: F1

This byte is reserved for user purposes (e.g., to provide temporary data/voice channel connections for special maintenance purposes).

9.2.2.7 RS data communication channel (DCC_R): D1-D3

A 192 kbit/s channel is defined using bytes D1, D2 and D3 as a regenerator section DCC.

9.2.2.8 MS data communication channel (DCC_M): D4-D12

For STM-N (N=1, 4, 16, 64, 256), a 576 kbit/s channel is defined using bytes D4 to D12 as a multiplex section DCC.

9.2.2.9 Extended MS data communication channel (DCC_{Mx}): D13-D156

For STM-256, an additional 9216 kbit/s channel is defined using bytes D13 to D156 as an extended multiplex section DCC.

– D13 to D60 are located in S (6,1,9) to S (6,1,56).

– D61 to D108 are located in S (7,1,9) to S (7,1,56).

– D109 to D156 are located in S (8,1,9) to S (8,1,56).

9.2.2.10 BIP-N × 24: B2

The B2 bytes are allocated for a multiplex section error monitoring function. This function shall be a Bit Interleaved Parity N × 24 code (BIP-N × 24) using even parity. The BIP-N × 24 is computed over all bits of the previous STM-N frame except for the first three rows of SOH and is placed in bytes B2 of the current frame.

For STM-0, N should be read as 1/3 giving a BIP-8.

9.2.2.11 Automatic protection switching (APS) channel: K1, K2 (b1-b5)

Two bytes are allocated for APS signalling for the protection of the multiplex section. The bit assignments for these bytes and the bit-oriented protocol are given in ITU-T Rec. G.841.

9.2.2.12 MS-RDI: K2 (b6-b8)

The multiplex section remote defect indication (MS-RDI) is used to return an indication to the transmit end that the received end has detected an incoming section defect or is receiving MS-AIS. MS-RDI is generated by inserting a "110" code in positions 6, 7 and 8 of the K2 byte before scrambling.

9.2.2.13 Synchronization status: S1 (b5-b8)

Bits 5 to 8 of byte S (9,1,1) or [9,1] are allocated for synchronization status messages. Table 9-2 gives the assignment of bit patterns to the four synchronization levels agreed to within ITU-T. Two additional bit patterns are assigned: one to indicate that quality of the synchronization is unknown and the other to signal that the section should not be used for synchronization. The remaining codes are reserved for quality levels defined by individual operators.

Table 9-2 – Assignment of SSM bit patterns

S1 bits b5-b8	SDH synchronization quality level description
0000	Quality unknown (existing synchronization network)
0001	Reserved
0010	ITU-T Rec. G.811
0011	Reserved
0100	SSU-A
0101	Reserved
0110	Reserved
0111	Reserved
1000	SSU-B
1001	Reserved
1010	Reserved
1011	ITU-T Rec. G.813 Option I (SEC)
1100	Reserved
1101	Reserved
1110	Reserved
1111	Do not use for synchronization (Note)
NOTE – This message may be emulated by equipment failures and will be emulated by a multiplex section AIS signal. The assignment of the "do not use for synchronization" quality level message is mandatory because the receipt of a multiplex section AIS is not necessarily interpreted as an indication of a physical failed synchronization source interface port. This assignment allows this state to be recognized without interaction with the multiplex section AIS detection process.	

9.2.2.14 MS-REI: M0, M1

For STM-N (N=0, 1, 4, 16), one byte (M1) is allocated for use as a multiplex section remote error indication (MS-REI).

For STM-N (N=64 and 256), two bytes (M0, M1) are allocated for use as a multiplex section remote error indication (MS-REI).

NOTE 1 – Interworking of equipment that supports MS-REI and equipment that does not support MS-REI cannot be achieved automatically.

NOTE 2 – STM-64 interfaces of equipment designed prior to the 2003 version of this Recommendation may support the single M1 REI only. STM-64 interfaces of new equipment has to be configurable to support the single byte M1 REI.

For STM-N levels, this byte conveys the count (in the range of [0, 255/65 536]) of interleaved bit blocks that have been detected in error by the BIP-24×N (B2). For STM-0, the count is based on a BIP-8 in B2. For the rate of STM-16, this value shall be truncated to 255.

STM-0, M1 generation: The byte shall be set to convey the count of interleaved bit blocks that have been detected in error by the BIP-8 in the range of [0, 8].

STM-0, M1 interpretation: The value in the byte shall be interpreted as follows in Table 9-3:

Table 9-3 – STM-0 M1 interpretation

M1[2-8] code, bits 234 5678	Interpretation
000 0000	0 BIP violation
000 0001	1 BIP violation
000 0010	2 BIP violations
000 0011	3 BIP violations
:	:
000 1000	8 BIP violations
000 1001	0 BIP violation
000 1010	0 BIP violation
:	:
111 1111	0 BIP violation
NOTE – Bit 1 of M1 is ignored.	

STM-1, M1 generation: The byte shall be set to convey the count of interleaved bit blocks that have been detected in error by the BIP-24 in the range of [0, 24].

STM-1, M1 interpretation: The value in the byte shall be interpreted as follows in Table 9-4:

Table 9-4 – STM-1 M1 interpretation

M1[2-8] code, bits 234 5678	Interpretation
000 0000	0 BIP violation
000 0001	1 BIP violation
000 0010	2 BIP violations
000 0011	3 BIP violations
:	:
001 1000	24 BIP violations
001 1001	0 BIP violation
001 1010	0 BIP violation
:	:
111 1111	0 BIP violation
NOTE – Bit 1 of M1 is ignored.	

STM-4, M1 generation: The byte shall be set to convey the count of interleaved bit blocks that have been detected in error by the BIP-96 in the range of [0, 96].

STM-4, M1 interpretation: The value in the byte shall be interpreted as follows in Table 9-5:

Table 9-5 – STM-4 M1 interpretation

M1[2-8] code, bits 234 5678	Interpretation
000 0000	0 BIP violation
000 0001	1 BIP violation
000 0010	2 BIP violations
000 0011	3 BIP violations
000 0100	4 BIP violations
000 0101	5 BIP violations
:	:
110 0000	96 BIP violations
110 0001	0 BIP violation
110 0010	0 BIP violation
:	:
111 1111	0 BIP violation
NOTE – Bit 1 of M1 is ignored.	

STM-16, M1 generation: The byte shall be set to convey the count of interleaved bit blocks that have been detected in error by the BIP-384 (in the range of [0, 255]) where the value conveyed is truncated at 255.

STM-16, M1 interpretation: The value in the byte shall be interpreted as follows in Table 9-6:

Table 9-6 – STM-16 M1 interpretation

M1[1-8] code, bits 1234 5678	Interpretation
0000 0000	0 BIP violation
0000 0001	1 BIP violation
0000 0010	2 BIP violations
0000 0011	3 BIP violations
0000 0100	4 BIP violations
0000 0101	5 BIP violations
:	:
1111 1111	255 BIP violations

STM-64, M0 and M1 generation: The bytes shall be set to convey the count of interleaved bit blocks that have been detected in error by the BIP-1536 (in the range of [0, 1536]). M0 bit 1 is most significant bit and M1 bit 8 is least significant bit. If interworking with old equipment supporting the single byte REI in M1, the value conveyed is truncated at 255 and inserted in M1.

STM-64, M0 and M1 interpretation: The value in M0 and M1 is interpreted as given in Table 9-7. If interworking with old equipment supporting the single byte REI in M1, the value in M1 is interpreted as given in Table 9-8.

NOTE 3 – Interworking cannot be achieved automatically. It has to be configured by the management systems.

Table 9-7 – STM-64 M0 and M1 interpretation

M0[1-8] code, bits 1234 5678	M1[1-8] code, bits 1234 5678	Interpretation
0000 0000	0000 0000	0 BIP violation
0000 0000	0000 0001	1 BIP violation
0000 0000	0000 0010	2 BIP violations
0000 0000	0000 0011	3 BIP violations
0000 0000	0000 0100	4 BIP violations
0000 0000	0000 0101	5 BIP violations
	:	:
0000 0110	0000 0000	1536 BIP violations
0000 0110	0000 0001	0 BIP violation
0000 0110	0000 0010	0 BIP violation
	:	:
1111 1111	1111 1111	0 BIP violation

Table 9-8 – STM-64 M1 interpretation

M1[1-8] code, bits 1234 5678	Interpretation
0000 0000	0 BIP violation
0000 0001	1 BIP violation
0000 0010	2 BIP violations
0000 0011	3 BIP violations
0000 0100	4 BIP violations
0000 0101	5 BIP violations
:	:
1111 1111	255 BIP violations

STM-256, M0, M1 generation: The bytes shall be set to convey the count of interleaved bit blocks that have been detected in error by the BIP-6144 (in the range of [0, 6144]). M0 bit 1 is most significant bit and M1 bit 8 is least significant bit.

STM-256, M0, M1 interpretation: The value in the byte shall be interpreted as follows in Table 9-9:

Table 9-9 – STM-256 M0 and M1 interpretation

M0[1-8] code, bits 1234 5678	M1[1-8] code, bits 1234 5678	Interpretation
0000 0000	0000 0000	0 BIP violation
0000 0000	0000 0001	1 BIP violation
0000 0000	0000 0010	2 BIP violations
0000 0000	0000 0011	3 BIP violations
0000 0000	0000 0100	4 BIP violations
0000 0000	0000 0101	5 BIP violations
	:	:
0001 1000	0000 0000	6144 BIP violations
0001 1000	0000 0001	0 BIP violation
0001 1000	0000 0010	0 BIP violation
	:	:
1111 1111	1111 1111	0 BIP violation

9.2.2.15 Media-dependant bytes

These 6N bytes, which are located at positions S (2,2,X) or [2,N+X], S (2,3,X) or [2,2N+X], S (2,5,X) or [2,4N+X], S (3,2,X) or [3,N+X], S (3,3,X) or [3,2N+X], S (3,5,X) or [3,4N+X] with X=1…N, are reserved for media-dependent applications.

The definition of these media-dependent bytes is outside the scope of this Recommendation.

NOTE – For SDH radio these bytes are defined in ITU-R Recommendation F.750.

9.2.3 Reduced SOH functionalities interface

For some applications (e.g., intra-station interface), an interface with reduced SOH functionalities can be used. The SOH bytes to be used for this interface are given in Table 9-10:

Table 9-10 – Reduced SOH functionalities interface

SOH bytes	Transmit functionality	Receive functionality
A1, A2	Required	Required
J0-Z0/C1	Optional	Optional
B1	Required	Unused
E1	Unused	Unused
F1	Unused	Unused
D1-D3	Unused	Unused
B2	Required	Required
K1, K2 (APS)	Optional	Optional
K2 (MS-AIS)	Required	Required
K2 (MS-RDI)	Required	Required
D4-D12	Unused	Unused
S1	Unused, 00001111 generated	Unused
M1	Required	Optional
E2	Unused	Unused
Other bytes	Unused	Unused

Required	These signals at the interface shall contain valid information as defined by this Recommendation.
Optional	Valid information may or may not be present in these signals. Use of these functions shall be a local matter.
Unused	This function is not defined at the interface. The contents should, if not specified otherwise, be either 00000000 or 11111111 according to regional standard.

9.2.4 Forward error correction: P1, Q1

For STM-16, STM-64 and STM-256, the P1 and Q1 bytes are reserved for an optional forward error correction (FEC) function. The FEC function and details for STM-64 and STM-256 of the usage of the P1 and Q1 bytes are given in Annex A. The FEC function and details for STM-16 of the usage of the P1 and Q1 bytes are given in Appendix IX.

NOTE – See clause A.4 regarding the functionality and transparency of regenerators.

9.3 POH descriptions

9.3.1 VC-4-Xc/VC-4/VC-3 POH

The VC-4-Xc POH is located in the first column of the 9-row by X × 261-column VC-4-Xc structure.

The VC-4 POH is located in the first column of the 9-row by 261-column VC-4 structure.

The VC-3 POH is located in the first column of the 9-row by 85-column VC-3 structure.

The VC-4-Xc/VC-4/VC-3 POH consists of 9 bytes denoted J1, B3, C2, G1, F2, H4, F3, K3 and N1 (see Figures 11-1, 7-3 and 7-4). These bytes are classified as follows:

– Bytes or bits used for end-to-end communication with independent payload function: J1, B3, C2, G1, K3 (b1-b4).

– Payload type-specific bytes: H4, F2, F3.

– Bits reserved for future international standardization: K3 (b5-b8).

– Byte which can be overwritten in an operator domain (without affecting the end-to-end performance monitoring facility of the byte B3): N1.

NOTE – Payload-dependent and payload-independent information is communicated by different codings in C2 byte and bits 5 to 7 of G1 byte.

9.3.1.1 Path trace: J1

This is the first byte in the virtual container; its location is indicated by the associated AU-n (n=3, 4) or TU-3 pointer. This byte is used to transmit repetitively a path access point identifier so that a path receiving terminal can verify its continued connection to the intended transmitter. A 16-byte frame is defined for the transmission of an access point identifier. This 16-byte frame is identical to the 16-byte frame defined in clause 9.2.2.2 for the description of the byte J0. At international boundaries, or at the boundaries between the networks of different operators, the format defined in clause 3/G.831 shall be used unless otherwise mutually agreed by the operators providing the transport. Within a national network or within the domain of a single operator, this path access point identifier may use a 64-byte frame.

9.3.1.2 Path BIP-8: B3

One byte is allocated in each VC-4-Xc/VC-4/VC-3 for a path error monitoring function. This function shall be a BIP-8 code using even parity. The path BIP-8 is calculated over all bits of the previous VC-4-Xc/VC-4/VC-3. The computed BIP-8 is placed in the B3 byte of the current VC-4-Xc/VC-4/VC-3.

9.3.1.3 Signal label: C2

One byte is allocated to indicate the composition or the maintenance status of the VC-4-Xc/VC-4/VC-3. Table 9-11, which is based on Hex code, provides codes for this byte.

Table 9-11 – C2 byte coding

MSB LSB **1 2 3 4 5 6 7 8**	**Hex code (Note 1)**	**Interpretation**
0 0 0 0 0 0 0 0	00	Unequipped or supervisory-unequipped (Note 2)
0 0 0 0 0 0 0 1	01	Reserved (Note 3)
0 0 0 0 0 0 1 0	02	TUG structure, see clause 7.2
0 0 0 0 0 0 1 1	03	Locked TU-n (Note 4)
0 0 0 0 0 1 0 0	04	Asynchronous mapping of 34 368 kbit/s or 44 736 kbit/s into the container-3, see clause 10.1.2
0 0 0 0 0 1 0 1	05	Experimental mapping (Note 9)
0 0 0 1 0 0 1 0	12	Asynchronous mapping of 139 264 kbit/s into the container-4, see clause 10.1.1.1
0 0 0 1 0 0 1 1	13	ATM mapping, see clauses 10.2.1 and 10.2.2
0 0 0 1 0 1 0 0	14	MAN DQDB [1] mapping, see clause 10.4
0 0 0 1 0 1 0 1	15	FDDI [3]-[11] mapping, see clause 10.5
0 0 0 1 0 1 1 0	16	Mapping of HDLC/PPP [12], [13] framed signal, see clause 10.3
0 0 0 1 0 1 1 1	17	Reserved for proprietary use (Note 10)
0 0 0 1 1 0 0 0	18	Mapping of HDLC/LAPS [15] framed signals, see clause 10.3
0 0 0 1 1 0 0 1	19	Reserved for proprietary use (Note 10)
0 0 1 0 0 0 0 0	20	Asynchronous mapping of ODUk (k=1,2) into VC-4-Xv (X=17,68), see clause 10.7

Table 9-11 – C2 byte coding

MSB LSB 1 2 3 4 5 6 7 8	Hex code (Note 1)	Interpretation
0 0 0 1 1 0 1 0	1A	Mapping of 10 Gbit/s Ethernet frames [14], see Annex F
0 0 0 1 1 0 1 1	1B	GFP mapping, see clause 10.6
0 0 0 1 1 1 0 0	1C	Mapping of 10 Gbit/s fibre channel frames (Note 8)
1 1 0 0 1 1 1 1	CF	Reserved (Note 7)
1 1 0 1 0 0 0 0 … … 1 1 0 1 1 1 1 1	D0 … DF	Reserved for proprietary use (Note 10)
1 1 1 0 0 0 0 1 … … 1 1 1 1 1 1 0 0	E1 … FC	Reserved for national use
1 1 1 1 1 1 1 0	FE	Test signal, O.181-specific mapping (Note 5)
1 1 1 1 1 1 1 1	FF	VC-AIS (Note 6)

NOTE 1 – There are 191 spare codes left for future use. Refer to Annex A/G.806 for the procedure to obtain one of these codes for a new payload type.

NOTE 2 – Value "0" indicates "VC-4-Xc/VC-4/VC-3 path unequipped or supervisory-unequipped". This value is originated in the case of an open connection and in the case of a supervisory-unequipped signal that contains no payload.

NOTE 3 – Value "1" should not be used in any equipment designed after the date of approval (10/2000) of version 5 of this Recommendation. In the past, this code meant "Equipped-non-specific" and has been used in cases where a mapping code is not defined in this table, see code "05" for new designs. For interworking with (old) equipment designed to transmit only the values "0" and "1", the following conditions apply:

– For backward compatibility, old equipment shall interpret any value received other than value "0" as an equipped condition.

– For forward compatibility, when receiving value "1" from old equipment, new equipment shall not generate a payload mismatch alarm.

NOTE 4 – The code "03" shall, for backward compatibility purposes, continue to be interpreted as previously defined even if the locked mode byte synchronous mappings are not defined any more.

NOTE 5 – Any mapping defined in ITU-T Rec. O.181 which does not correspond to a mapping defined in this Recommendation falls in this category.

NOTE 6 – Value "FF" indicates VC-AIS. It is generated by a TCM source if no valid incoming signal is available and a replacement signal is generated.

NOTE 7 – Previous value assigned for an obsolete mapping of HDLC/PPP framed signal [12], [13].

NOTE 8 – This mapping is under study and the signal label is provisionally allocated.

NOTE 9 – Value "05" is only to be used for experimental activities in cases where a mapping code is not defined in this table. Refer to Annex A/G.806 for more information on the use of this code.

NOTE 10 – The code value(s) will not be subject to further standardization. Refer to Annex A/G.806 for more information on the use of these codes.

9.3.1.4 Path status: G1

One byte is allocated to convey the path status and performance back to a VC-4-Xc/VC-4/VC-3 trail termination source as detected by a trail termination sink. This feature permits the status and performance of the complete duplex trail to be monitored at either end, or at any point along that trail. The allocation of bits in G1 is illustrated in Figure 9-8.

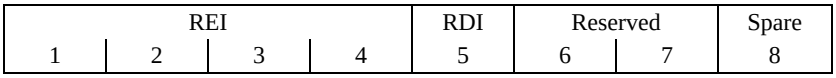


Figure 9-8 – VC-4-Xc/VC-4/VC-3 path status (G1)

Bits 1 through 4 convey the count of interleaved-bit blocks that have been detected in error by the trail termination sink using the path BIP-8 code (B3). This count has nine legal values, namely 0-8 errors. The remaining seven possible values represented by these four bits can only result from some unrelated condition and shall be interpreted as zero errors.

Bit 5 is set to 1 to indicate a VC-4-Xc/VC-4/VC-3 path remote defect indication (RDI), otherwise it is set to 0. The VC-4-Xc/VC-4/VC-3 path RDI is sent back towards the trail termination source if either an AU-4-Xc/AU-4/AU-3 or TU-3 server signal failure or trail signal failure is being detected by the trail termination sink. RDI does not indicate remote payload or adaptation defects. Connectivity and server defects are indicated by RDI; for further details, see ITU-T Rec. G.783.

Bits 6 and 7 are reserved for an optional use described in clause VII.1. If this option is not used, bits 6 and 7 shall be set to 00 or 11. A receiver is required to be able to ignore the contents of these bits. The use of the optional function is at the discretion of the owner of the trail termination source generating the G1 byte.

Bit 8 is allocated for future use. This bit has no defined value. The receiver is required to ignore its content.

NOTE – Equipment complying with the 1993 versions of the I.432.x series of ITU-T Recommendations may use bit 5 of G1 to indicate a remote loss of cell delineation (LCD).

9.3.1.5 Path user channels: F2, F3

These bytes are allocated for user communication purposes between path elements and are payload dependent.

For mapping of DQDB in VC-4, these two octets are used to carry the DQDB layer management information octets (M1 and M2) [1].

9.3.1.6 Position and sequence indicator: H4

This byte provides a multiframe and sequence indicator for virtual VC-3/VC-4 concatenation (see clause 11.2) and a generalized position indicator for payloads. In the latter case, the content is payload specific (e.g., H4 can be used as a multiframe indicator for VC-2, VC-11 and VC-12 payload as defined in clause 8.3.8).

For mapping of DQDB in VC-4, the H4 byte carries the slot boundary information and the link status signal (LSS). The bits 1 and 2 are used for the LSS code [1]. The bits 3 to 8 form the slot offset indicator. The slot offset indicator shall contain a binary number indicating the offset in octets between the H4 octet and the first slot boundary following the H4 octet. The valid range of the slot offset indicator value shall be 0 to 52. A received value of 53 to 63 corresponds to an error condition.

9.3.1.7 Automatic protection switching (APS) channel: K3 (b1-b4)

These bits are allocated for APS signalling for protection at the VC-3/VC-4 path levels.

9.3.1.8 Network operator byte: N1

This byte is allocated to provide a tandem connection monitoring (TCM) function. The details concerning the two possible implementations of the HO-TCM function are given in Annexes C and D.

9.3.1.9 Data link K3 (b7-b8)

Bits 7 and 8 of K3 are reserved for a higher order path data link. The applications and protocols are outside the scope of this Recommendation.

9.3.1.10 Spare: K3 (b5-b6)

These bits are allocated for future use. These bits have no defined value. The receiver is required to ignore their content.

9.3.2 VC-2, VC-12 and VC-11 POH

The bytes V5, J2, N2 and K4 are allocated to the VC-2, VC-12 and VC-11 POH. The V5 byte is the first byte of the multiframe and its position is indicated by the TU-2, TU-12 or TU-11 pointer. The position of these bytes in the multiframe is given in Figure 8-9.

NOTE – Payload-dependent and payload-independent information is communicated by different codings in bits 5 to 7 of V5 and 5 to 7 of K4.

9.3.2.1 V5 byte

The byte V5 provides the functions of error checking, signal label and path status of the VC-2, VC-12 and VC-11 paths. The bit assignments of the V5 byte are specified in the following clauses and are illustrated in Figure 9-9.

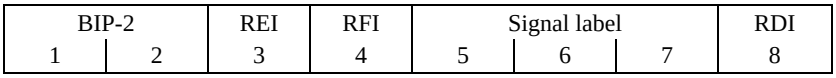


Figure 9-9 – VC-2, VC-12 and VC-11 POH V5

Bits 1 and 2 are used for error performance monitoring. A bit interleaved parity (BIP) scheme is specified. Bit 1 is set such that parity of all odd number bits (1, 3, 5 and 7) in all bytes in the previous VC-2, VC-12 or VC-11 is even and bit 2 is set similarly for the even number bits (2, 4, 6 and 8).

Note that the calculation of the BIP-2 includes the VC-2, VC-12 or VC-11 POH bytes but excludes bytes V1, V2, V3 (except when used for negative justification) and V4.

Bit 3 is a VC-2, VC-12 and VC-11 path remote error indication (REI) that is set to one and sent back towards a VC-2, VC-12 or VC-11 path originator if one or more errors were detected by the BIP-2, and is otherwise set to zero.

Bit 4 is a VC-11 byte synchronous path remote failure indication (RFI). This bit is set to one if a failure is declared, otherwise it is set to zero. The VC-11 path RFI is sent back by the VC-11 termination. The use and content of this bit are undefined for VC-2 and VC-12.

NOTE – A failure is a defect that persists beyond the maximum time allocated to the transmission system protection mechanisms.

Bits 5 through 7 provide a VC-2, VC-12 and VC-11 signal label. Eight binary values are possible in these three bits. Value 000 indicates "VC-2, VC-12 or VC-11 path unequipped or supervisory-unequipped". Value 001 is used by old equipment to indicate "VC-2, VC-12 or VC-11 path equipped-non-specific payload". Other values are used by new equipment to indicate specific mappings as shown in Table 9-12. The value 101 indicates a VC-2, VC-12 or VC-11 mapping given

by the extended signal label described in clause 9.3.2.4. Any value received, other than 000, indicates an equipped VC-2, VC-12 or VC-11 path.

Table 9-12 – VC-2, VC-12 and VC-11 V5 signal label coding

b5	b6	b7	Meaning
0	0	0	Unequipped or supervisory-unequipped
0	0	1	Reserved (Note 1)
0	1	0	Asynchronous, see clauses 10.1.3.1, 10.1.4.1 and 10.1.5.1
0	1	1	Bit synchronous, see clauses 10.1.3.2 and 10.1.5.2 (Note 2)
1	0	0	Byte synchronous, see clauses 10.1.4.2, 10.1.4.3, 10.1.5.3 and 10.1.5.4
1	0	1	Extended signal label described in 9.3.2.4 (Note 1)
1	1	0	Test signal, O.181-specific mapping (Note 3)
1	1	1	VC-AIS (Note 4)

NOTE 1 – Value "1" should not be used in any equipment designed after the date of approval of version 5 (10/2000) of this Recommendation. In the past this code meant "equipped-non-specific" and has been used in cases where a mapping code is not defined in this table, see code "101" and extended signal label "08" in Table 9-13 for new designs. For interworking with (old) equipment designated to transmit only the values "0" and "1", the following conditions apply:

– For backward compatibility, old equipment shall interpret any value received other than "0" as an equipped condition.

– For forward compatibility, when receiving value "1" from old equipment, new equipment shall not generate a payload mismatch alarm.

NOTE 2 – In the case of a VC-12, the code "3" shall, for backward compatibility purposes, continue to be interpreted as previously defined even if the bit synchronous mapping of 2048 kbit/s signal is not defined anymore.

NOTE 3 – Any non-virtually concatenated mapping defined in ITU-T Rec. O.181 that does not correspond to a mapping defined in this Recommendation falls in this category.

NOTE 4 – Value "7" indicates VC-AIS. It is generated by a TCM source if no valid incoming signal is available and a replacement signal is generated.

Bit 8 is set to 1 to indicate a VC-2, VC-12 or VC-11 path remote defect indication (RDI); otherwise it is set to zero. The VC-2, VC-12 or VC-11 path RDI is sent back towards the trail termination source if either a TU-2, TU-12 or TU-11 server signal failure or trail signal failure condition is being detected by the trail termination sink. RDI does not indicate remote payload or adaptation defects. Connectivity and server defects are indicated by RDI; for further detail see ITU-T Rec. G.783.

9.3.2.2 Path trace: J2

Byte J2 is used to transmit repetitively a lower order path access point identifier so that a path receiving terminal can verify its continued connection to the intended transmitter. This path access point identifier uses the format defined in clause 3/G.831. A 16-byte frame is defined for the transmission of path access point identifiers. This 16-byte frame is identical to the 16-byte frame defined in clause 9.2.2.2 for the description of the byte J0.

NOTE – Equipment developed prior to the adoption of the 1993 version of ITU-T Rec. G.709 may not support this functionality.

9.3.2.3 Network operator byte: N2

This byte is allocated to provide a tandem connection monitoring (TCM) function. The details concerning the implementation of the LO-TCM are given in Annex E.

9.3.2.4 Extended signal label: K4 (b1)

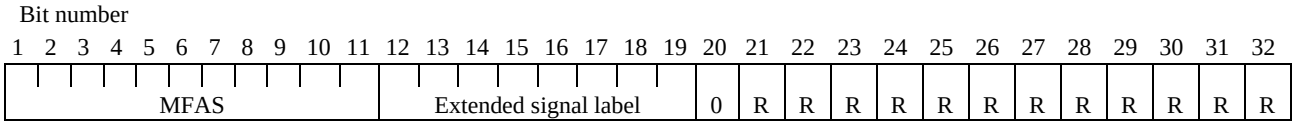
This bit is allocated to an extended signal label. If the signal label in V5 bits 5 through 7 is 101, the contents of the extended signal label is valid and is described below. For all other values of V5 bits 5 through 7, the extended signal label bit is undefined and should be ignored by the receiver.

The bit contains a 32-frame multiframe depicted in Figure 9-10. The multiframe alignment signal, MFAS, consists of "0111 1111 110". The extended signal label is contained in bits 12 to 19. Multiframe position 20 must contain "0". The remaining 12 bits are reserved for future standardization, should be set to all "0"s, and should be ignored by the receiver.

NOTE 1 – The virtual concatenation multiframe in K4 bit 2 uses the MFAS of this bit. That means that the virtual concatenation function needs to consider this bit without confirming that the V5 signal label is 101.

There are no inconsistency problems since all LO virtually concatenated payloads must have an extended signal label.

NOTE 2 – If at a later stage the bits reserved for future use are activated, care must be taken to ensure that a sequence of nine "1"s (imitating the MFAS) is avoided.



MFAS	Multiframe alignment bits
0	Zero
R	Reserved bit

Figure 9-10 – K4 bit 1 multiframe

The coding of the extended signal label is given in Table 9-13. The signal labels in Table 9-12 for the range "0" to "7" and the signal labels in Table 9-13 for the range of "08" to "FF" together forms the complete VC-11/VC-12/VC-2 signal label range of "00" to "FF".

NOTE 3 – Signal label "5" is indicated by an equipment not supporting the extended signal label receiving an extended signal label.

NOTE 4 – For interworking with equipment using the ATM mapping in clause 10.2.5 it may be necessary to accept the V5 signal label "5" without K4 bit 1 multiframe as an equipped condition.

Table 9-13 – VC-11/VC-12/VC-2 extended signal label byte coding

MSB b12 b13 b14 b15	LSB b16 b17 b18 b19	Hex code (Note 1)	Interpretation
0 0 0 0	0 0 0 0	00	Reserved (Note 2)
…	…	…	
0 0 0 0	0 1 1 1	07	
0 0 0 0	1 0 0 0	08	Experimental mapping (Note 3)
0 0 0 0	1 0 0 1	09	ATM mapping, see clauses 10.2.3 to 10.2.5
0 0 0 0	1 0 1 0	0A	Mapping of HDLC/PPP [12], [13] framed signal, see clause 10.3
0 0 0 0	1 0 1 1	0B	Mapping of HDLC/LAPS [15] framed signals, see clause 10.3
0 0 0 0	1 1 0 0	0C	Virtually concatenated test signal, O.181-specific mapping (Note 4)
0 0 0 0	1 1 0 1	0D	GFP mapping, see clause 10.6
1 1 0 1	0 0 0 0	D0	Reserved for proprietary use (Note 5)
…	…	…	
1 1 0 1	1 1 1 1	DF	
1 1 1 1	1 1 1 1	FF	Reserved

NOTE 1 – There are 225 spare codes left for future use. Refer to Annex A/G.806 for the procedure to obtain one of these codes for a new payload type.

NOTE 2 – Values "00" to "07" are reserved to give a unique name to non-extended in Table 9-12 and extended signal labels.

NOTE 3 – Value "08" is only to be used for experimental activities in cases where a mapping code is not defined in this table. Refer to Annex A/G.806 for more information on the use of this code.

NOTE 4 – Any virtually concatenated mapping defined in ITU-T Rec. O.181 or its successors which does not correspond to a mapping defined in this Recommendation falls in this category.

NOTE 5 – These 16-code values will not be subject to further standardization. Refer to Annex A/G.806 for more information on the use of these codes.

9.3.2.5 Lower order virtual concatenation: K4 (b2)

This bit is allocated for the lower order virtual concatenation string. The bit is multiframed in 32 frames to form a 32-bit string. This function is described in clause 11.4.

9.3.2.6 Automatic protection switching (APS) channel: K4 (b3-b4)

These bits are allocated for APS signalling for protection at the lower order path level. This function is for further study.

9.3.2.7 Reserved: K4 (b5-b7)

Bits 5 to 7 of K4 are reserved for an optional use described in clause VII.2. If this option is not used, these bits shall be set to "000" or "111". A receiver is required to be able to ignore the contents of these bits. The use of the optional function is at the discretion of the owner of the trail termination source generating the K4 byte.

9.3.2.8 Data link: K4 (b8)

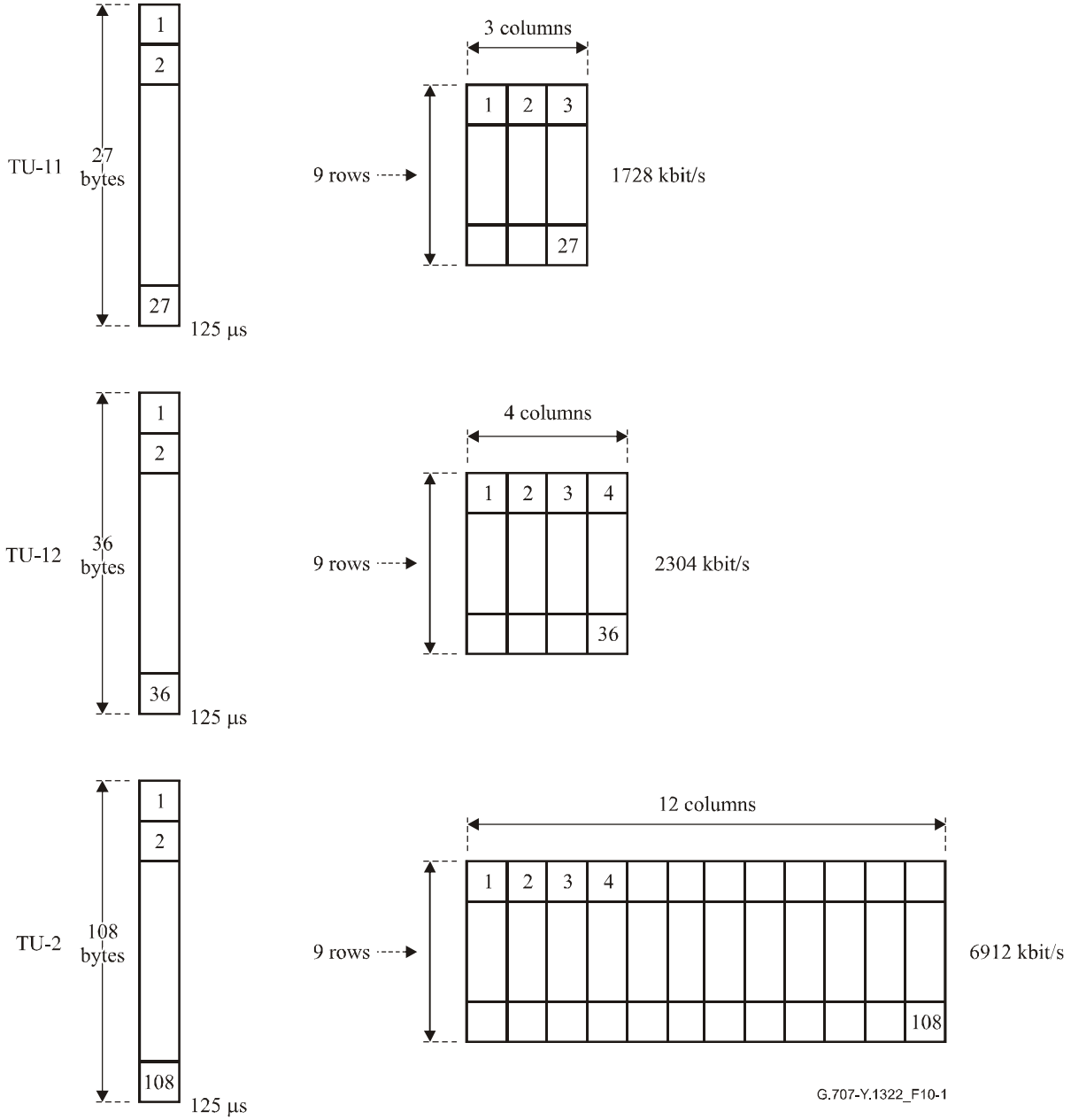
Bit 8 of K4 is reserved for a lower order path data link. The applications and protocols are outside the scope of this Recommendation.

10 Mapping of tributaries into VC-n/VC-m

10.1 Mapping of G.702 type signals

Accommodation of asynchronous and synchronous tributaries presently defined in ITU-T Rec. G.702 shall be possible.

Figure 10-1 shows TU-11, TU-12 and TU-2 sizes and formats.



NOTE – The tributary unit pointer bytes (V1-V4) are located in byte 1 (using a four frame multiframe).

Figure 10-1 – TU-11, TU-12 and TU-2 sizes and formats

10.1.1 Mapping into VC-4

10.1.1.1 Asynchronous mapping of 139 264 kbit/s

One 139 264 kbit/s signal can be mapped into a VC-4 of an STM-1 frame as shown in Figures 10-2 and 10-3.

The VC-4 consists of a 9-byte (1 column) path overhead (POH) plus a 9-row by 260-column payload structure as shown in Figure 10-2.

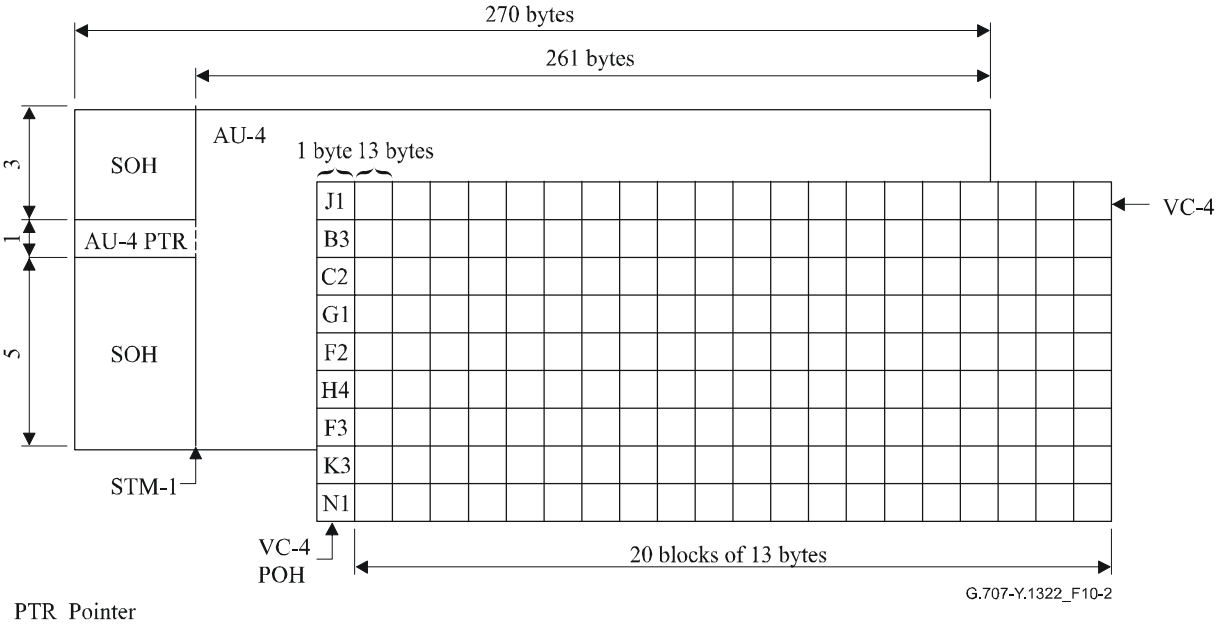


Figure 10-2 – Multiplexing of VC-4 into STM-1 and block structure of VC-4 for asynchronous mapping of 139 264 kbit/s

This payload can be used to carry one 139 264 kbit/s signal:

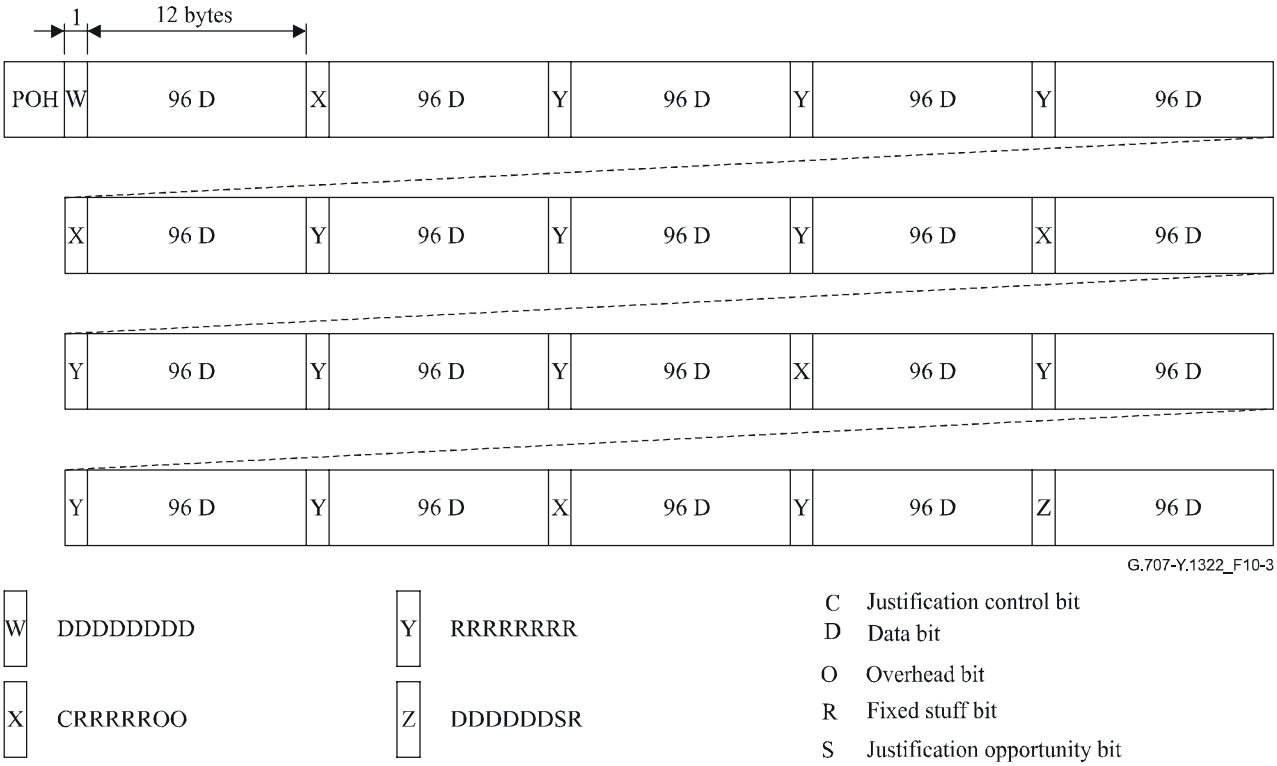
– Each of the nine rows is partitioned into 20 blocks, consisting of 13 bytes each (Figure 10-2).

– In each row, one justification opportunity bit (S) and five justification control bits (C) are provided (Figure 10-3).

– The first byte of each block consists of:
  - either eight data bits (D) (byte W); or
  - eight fixed stuff bits (R) (byte Y); or
  - one justification control bit (C) plus five fixed stuff bits (R) plus two overhead bits (O) (byte X); or
  - six data bits (D) plus one justification opportunity bit (S) plus one fixed stuff bit (R) (byte Z).

– The last 12 bytes of one block consist of data bits (D).

The sequence of all these bytes is shown in Figure 10-3.



NOTE – This figure shows one row of the nine-row VC-4 container structure.

Figure 10-3 – Asynchronous mapping of 139 264 kbit/s tributary into VC-4

The overhead bits (O) are reserved for further overhead communication purposes.

The set of five justification control bits (C) in every row is used to control the corresponding justification opportunity bit (S). CCCCC = 00000 indicates that the S bit is an information bit, whereas CCCCC = 11111 indicates that the S bit is a justification bit.

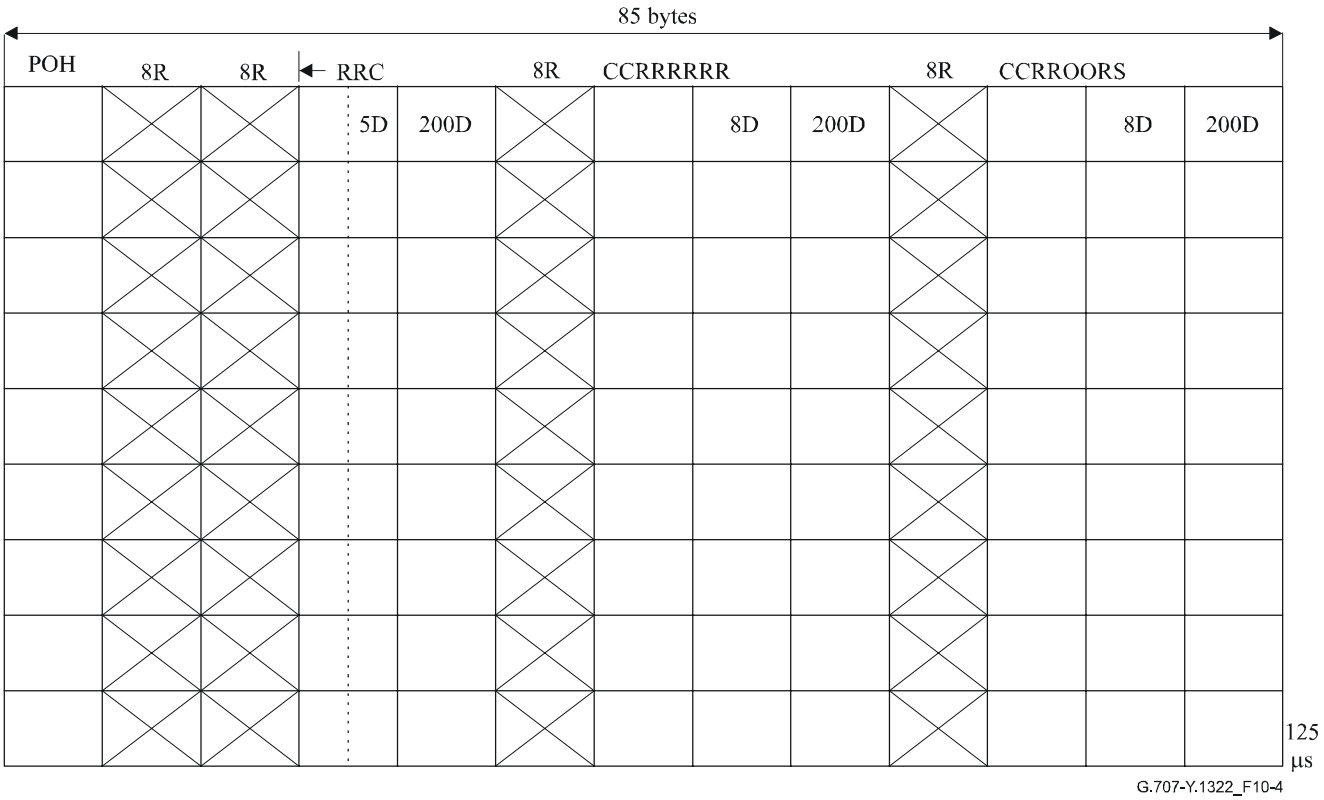
Majority vote should be used to make the justification decision in the desynchronizer for protection against single and double bit errors in the C bits.

The value contained in the S bit, when used as justification bit, is not defined. The receiver is required to ignore the value contained in this bit whenever it is used as a justification bit.

10.1.2 Mapping into VC-3

10.1.2.1 Asynchronous mapping of 44 736 kbit/s

One 44 736 kbit/s signal can be mapped into a VC-3 as shown in Figure 10-4.



C Justification control bit

D Data bit

O Overhead bit

R Fixed stuff bit

S Justification opportunity bit

Figure 10-4 – Asynchronous mapping of 44 736 kbit/s tributary into VC-3

The VC-3 consists of nine subframes every 125 µs. Each subframe consists of one byte of VC-3 POH, 621 data bits, a set of five justification control bits, one justification opportunity bit and two overhead communication channel bits. The remaining bits are fixed stuff (R) bits. The O bits are reserved for future overhead communication purposes.

The set of five justification control bits is used to control the justification opportunity (S) bit. CCCCC = 00000 indicates that the S bit is a data bit, whereas CCCCC = 11111 indicates that the S bit is a justification bit. Majority vote should be used to make the justification decision in the desynchronizer for protection against single and double bit errors in the C bits.

The value contained in the S bit, when used as justification bits, is not defined. The receiver is required to ignore the value contained in this bit whenever it is used as a justification bit.

10.1.2.2 Asynchronous mapping of 34 368 kbit/s

One 34 368 kbit/s signal can be mapped into a VC-3 as shown in Figure 10-5.

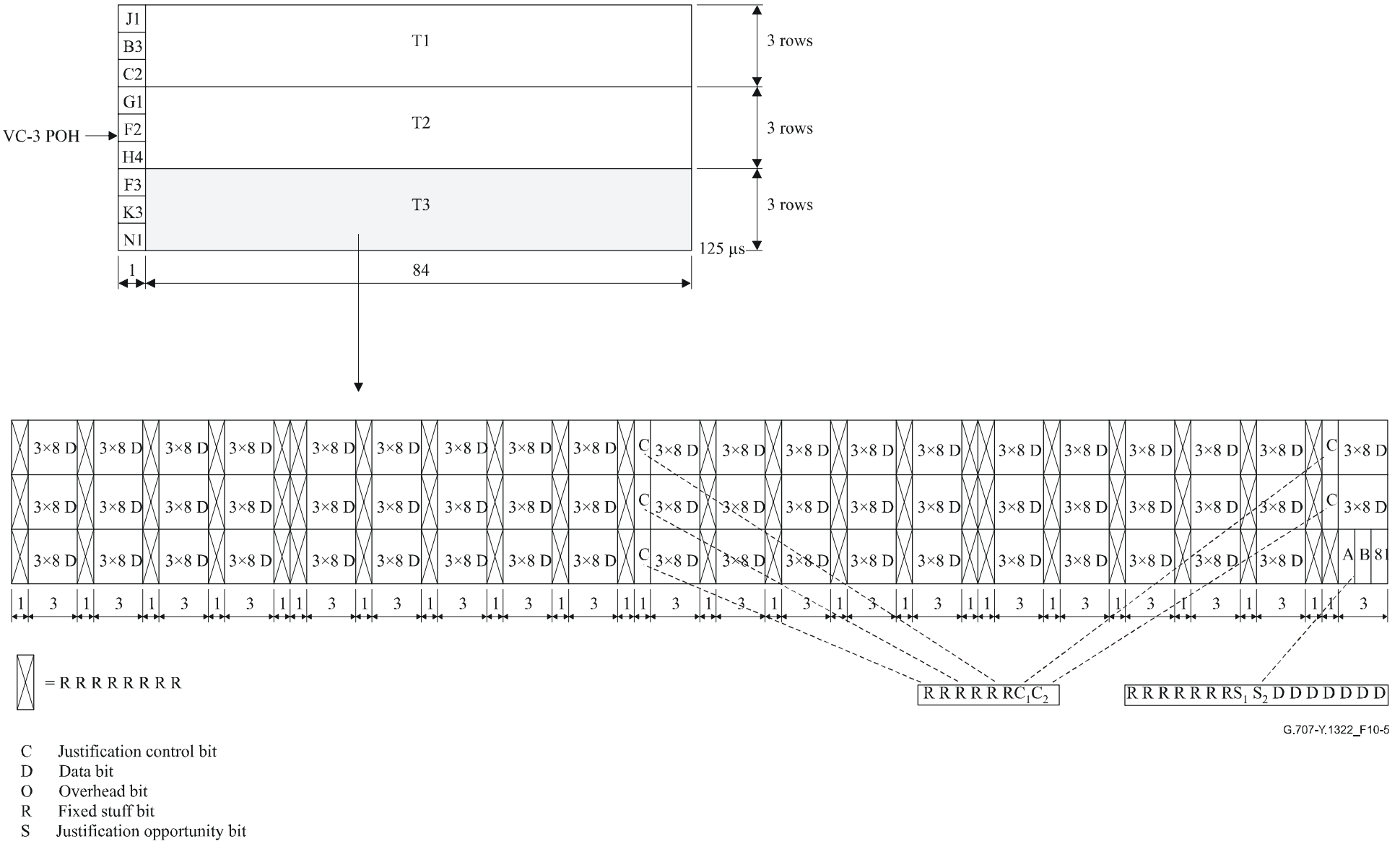


Figure 10-5 – Asynchronous mapping of 34 368 kbit/s tributary into VC-3

In addition to the VC-3 POH, the VC-3 consists of a payload of 9×84 bytes every 125 µs. This payload is divided in three subframes, each subframe consisting of:

– 1431 data bits (D);

– two sets of five justification control bits (C_1, C_2);

– two justification opportunity bits (S_1, S_2);

– 573 fixed stuff bits (R).

Two sets of five justification control bits C_1 and C_2 are used to control the two justification opportunity bits S_1 and S_2, respectively.

$C_1C_1C_1C_1C_1$ = 00000 indicates that S_1 is a data bit while $C_1C_1C_1C_1C_1$ = 11111 indicates that S_1 is a justification bit. C_2 bits control S_2 in the same way. Majority vote should be used to make the justification decision in the desynchronizer for protection against single and double bit errors in the C bits.

The value contained in S_1 and S_2, when they are justification bits, is not defined. The receiver is required to ignore the value contained in these bits whenever they are used as justification bits.

NOTE – The same mapping could be used for bit or byte synchronous 34 368 kbit/s. In these cases, S_1 bit should be a fixed stuff and S_2 bit a data bit. By setting the C_1 bits to 1 and the C_2 bits to 0, a common desynchronize could be used for both asynchronous and synchronous 34 368 kbit/s mappings.

10.1.3 Mapping into VC-2

10.1.3.1 Asynchronous mapping of 6312 kbit/s

One 6312 kbit/s signal can be mapped into a VC-2. Figure 10-6 shows this over a period of 500 µs.

V5	D D D D D D D R	(24 × 8) D	R R R R R R R R	
R R R R R R R R	C_1C_2 O O O O D R	(24 × 8) D	R R R R R R R R	
D D D D D D D D	C_1C_2 O O O O D R	(24 × 8) D	R R R R R R R R	
R R R R R R R R	C_1C_2 D D D S_1S_2 R	(24 × 8) D		125 µs
J2	D D D D D D D R	(24 × 8) D	R R R R R R R R	
R R R R R R R R	C_1C_2 O O O O D R	(24 × 8) D	R R R R R R R R	
D D D D D D D D	C_1C_2 O O O O D R	(24 × 8) D	R R R R R R R R	
R R R R R R R R	C_1C_2 D D D S_1S_2 R	(24 × 8) D		250 µs
N2	D D D D D D D R	(24 × 8) D	R R R R R R R R	
R R R R R R R R	C_1C_2 O O O O D R	(24 × 8) D	R R R R R R R R	
D D D D D D D D	C_1C_2 O O O O D R	(24 × 8) D	R R R R R R R R	
R R R R R R R R	C_1C_2 D D D S_1S_2 R	(24 × 8) D		375 µs
K4	D D D D D D D R	(24 × 8) D	R R R R R R R R	
R R R R R R R R	C_1C_2 O O O O D R	(24 × 8) D	R R R R R R R R	
D D D D D D D D	C_1C_2 O O O O D R	(24 × 8) D	R R R R R R R R	
R R R R R R R R	C_1C_2 D D D S_1S_2 R	(24 × 8) D		500 µs

C Justification control bit
D Data bit
O Overhead bit
R Fixed stuff bit
S Justification opportunity bit

Figure 10-6 – Asynchronous mapping of 6312 kbit/s tributary

In addition to the VC-2 POH, the VC-2 consists of 3152 data bits, 24 justification control bits, eight justification opportunity bits and 32 overhead communication channel bits. The remaining are fixed stuff bits (R). The O bits are reserved for future overhead communication purposes.

Two sets (C_1, C_2) of three justification control bits, are used to control the two justification opportunities S_1 and S_2, respectively.

$C_1C_1C_1 = 000$ indicates that S_1 is a data bit, while $C_1C_1C_1 = 111$ indicates that S_1 is a justification bit. C_2 bits control S_2 in the same way. Majority vote should be used to make the justification decision in the desynchronizer for protection against single bit error in the C bits.

The value contained in S_1, and S_2, when they are justification bits, is not defined. The receiver is required to ignore the value contained in these bits whenever they are used as justification bits.

10.1.3.2 Bit synchronous mapping of 6312 kbit/s

The bit synchronous mapping for 6312 kbit/s tributaries is shown in Figure 10-7.

Note that a common desynchronizer can be used for both asynchronous and bit synchronous mappings.

V5	D D D D D D D R	(24 × 8) D	R R R R R R R R	
R R R R R R R R	1 Ø O O O O D R	(24 × 8) D	R R R R R R R R	
D D D D D D D D	1 Ø O O O O D R	(24 × 8) D	R R R R R R R R	
R R R R R R R R	1 Ø D D D R D R	(24 × 8) D		125 µs
J2	D D D D D D D R	(24 × 8) D	R R R R R R R R	
R R R R R R R R	1 Ø O O O O D R	(24 × 8) D	R R R R R R R R	
D D D D D D D D	1 Ø O O O O D R	(24 × 8) D	R R R R R R R R	
R R R R R R R R	1 Ø D D D R D R	(24 × 8) D		250 µs
N2	D D D D D D D R	(24 × 8) D	R R R R R R R R	
R R R R R R R R	1 Ø O O O O D R	(24 × 8) D	R R R R R R R R	
D D D D D D D D	1 Ø O O O O D R	(24 × 8) D	R R R R R R R R	
R R R R R R R R	1 Ø D D D R D R	(24 × 8) D		375 µs
K4	D D D D D D D R	(24 × 8) D	R R R R R R R R	
R R R R R R R R	1 Ø O O O O D R	(24 × 8) D	R R R R R R R R	
D D D D D D D D	1 Ø O O O O D R	(24 × 8) D	R R R R R R R R	
R R R R R R R R	1 Ø D D D R D R	(24 × 8) D		500 µs

D Data bit
O Overhead bit
R Fixed stuff bit

Figure 10-7 – Bit synchronous mapping of 6312 kbit/s tributary

10.1.4 Mapping into VC-12

NOTE – Refer to clause 9/G.803 for recommended selection criteria on the choice of primary rate mapping.

10.1.4.1 Asynchronous mapping of 2048 kbit/s

One 2048 kbit/s signal can be mapped into a VC-12. Figure 10-8 shows this over a period of 500 µs.

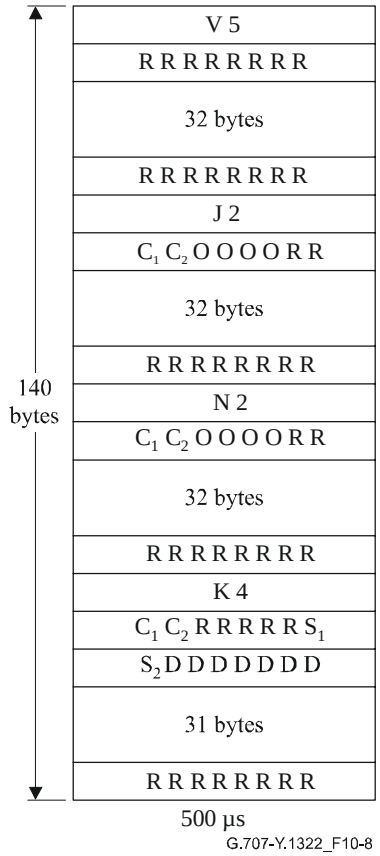


Figure 10-8 – Asynchronous mapping of 2048 kbit/s tributary

In addition to the VC-12 POH, the VC-12 consists of 1023 data bits, six justification control bits, two justification opportunity bits and eight overhead communication channel bits. The remaining are fixed stuff bits (R). The O bits are reserved for future overhead communication purposes.

Two sets (C_1, C_2) of three justification control bits are used to control the two justification opportunities S_1 and S_2, respectively. $C_1C_1C_1$ = 000 indicates that S_1 is a data bit, while $C_1C_1C_1$ = 111 indicates that S_1 is a justification bit. C_2 controls S_2 in the same way. Majority vote should be used to make the justification decision in the desynchronizer for protection against single bit errors in the C bits.

The value contained in S_1 and S_2, when they are justification bits, is not defined. The receiver is required to ignore the value contained in these bits whenever they are used as justification bits.

10.1.4.2 Byte synchronous mapping of 2048 kbit/s

Figure 10-9 shows byte synchronous mapping for G.704 structured 2048 kbit/s tributaries employing, for example, common channel signalling (CCS) or channel associated signalling (CAS).

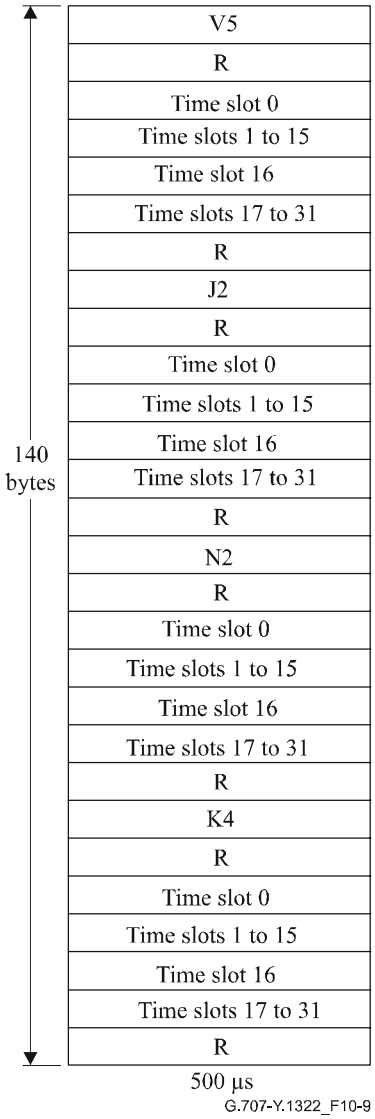
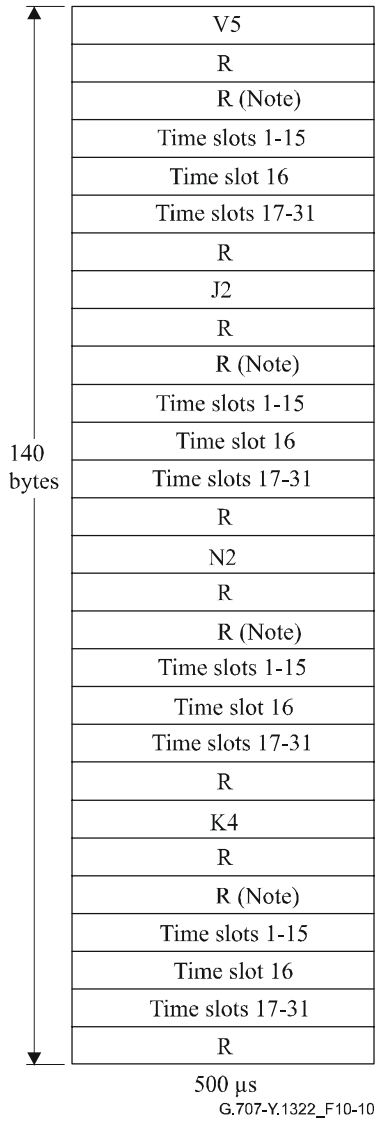


Figure 10-9 – Byte synchronous mapping for 2048 kbit/s tributary (30 channels with common channel signalling or channel associated signalling)

10.1.4.3 Byte synchronous mapping of 31 × 64 kbit/s

Byte synchronous mapping of 31 × 64 kbit/s tributaries is shown in Figure 10-10.



R Fixed stuff byte

NOTE – Inserting here a time slot 0 according to ITU-T Rec. G.704 would result in the 2048 kbit/s mapping described in Figure 10-9.

Figure 10-10 – Byte synchronous mapping for 31 × 64 kbit/s

10.1.5 Mapping into VC-11

Different structures are defined for the transport of 1544 kbit/s and 64 kbit/s client signals. To support 1544 kbit/s transport across SDH and PDH networks, the rule for interconnecting VC-11 mappings will be to use the 1544 kbit/s asynchronous mapping unless otherwise mutually agreed by the operators providing the transport. This SDH interconnection rule does not modify the mapping recommendations in ITU-T Rec. G.803. Refer to clause 9/G.803 for additional information on selection criteria and the choice of primary rate mappings.

10.1.5.1 Asynchronous mapping of 1544 kbit/s

One 1544 kbit/s signal can be mapped into a VC-11. Figure 10-11 shows this over a period of 500 µs.

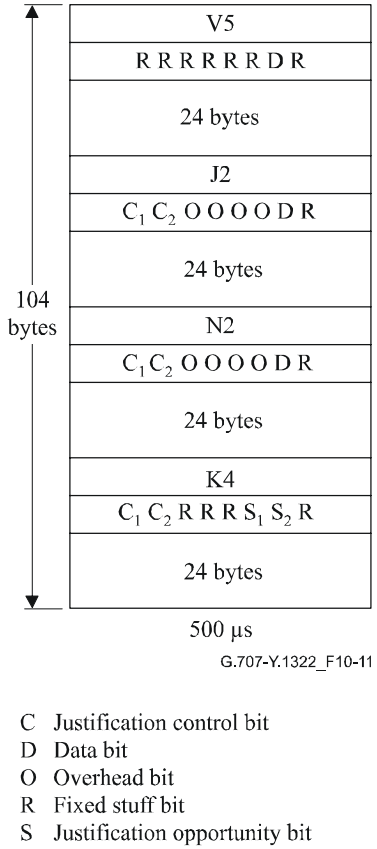


Figure 10-11 – Asynchronous mapping of 1544 kbit/s tributary

In addition to the VC-11 POH, the VC-11 consists of 771 data bits, six justification control bits, two justification opportunity bits and eight overhead communication channel bits. The remaining are fixed stuff bits (R). The O bits are reserved for future communication purposes.

Two sets (C_1,C_2) of three justification control bits are used to control the two justification opportunities, S_1 and S_2, respectively.

$C_1C_1C_1 = 000$ indicates that S_1 is a data bit while $C_1C_1C_1 = 111$ indicates that S_1 is a justification bit. C_2 controls S_2 in the same way. Majority vote should be used to make the justification decision in the desynchronizer for protection against single bit errors in the C bits.

The value contained in S_1 and S_2, when they are justification bits, is not defined. The receiver is required to ignore the value contained in these bits whenever they are used as justification bits.

10.1.5.2 Bit synchronous mapping of 1544 kbit/s

The bit synchronous mapping for 1544 kbit/s tributaries is shown in Figure 10-12.

Note that a common desynchronizer can be used for both asynchronous and bit synchronous mappings.

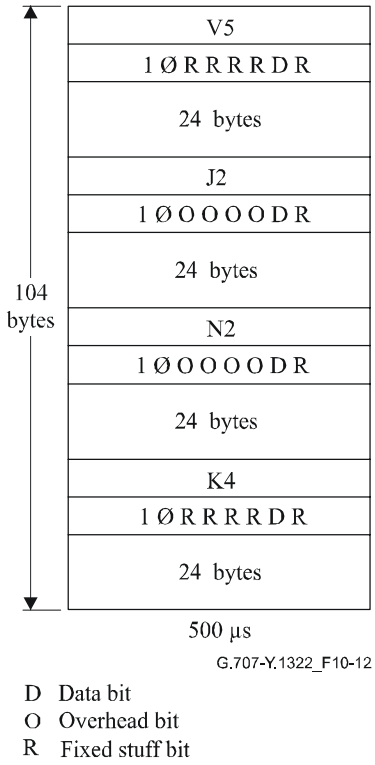
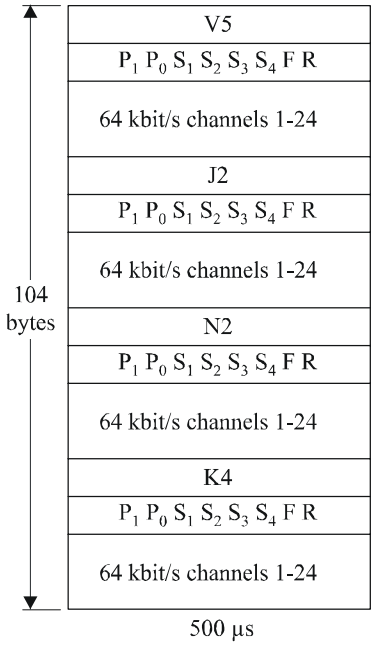


Figure 10-12 – Bit synchronous mapping for 1544 kbit/s tributary

10.1.5.3 Byte synchronous mapping of 1544 kbit/s

The byte synchronous mapping for 1544 kbit/s tributaries is shown in Figure 10-13.



F 1544 kbit/s tributary frame bit
S Signalling bits
P_1 P_0 Signalling phase indicator
P_1 P_0 00 on the first signalling byte of the multiframe

Figure 10-13 – Byte synchronous mapping for 1544 kbit/s tributary

The S_1, S_2, S_3 and S_4 bits contain the signalling for the 24×64 kbit/s channels. The F bit contains the 1544 kbit/s frame bit. The phase of the signalling bits and the F bit is indicated in the P_1 and P_0 bits. This is illustrated in Figure 10-14.

If the S or F bits are not used in an application, then they shall be set to 0.

Signalling												Formats				
2 state				4 state				16 state				24 frames	12 frames			
S_1	S_2	S_3	S_4	S_1	S_2	S_3	S_4	S_1	S_2	S_3	S_4	F_4	FAS	S	P_1	P_0
A_1	A_2	A_3	A_4	A_1	A_2	A_3	A_4	A_1	A_2	A_3	A_4	m	1	-	0	0
A_5	A_6	A_7	A_8	A_5	A_6	A_7	A_8	A_5	A_6	A_7	A_8	e_1	-	0	0	0
A_9	A_{10}	A_{11}	A_{12}	A_9	A_{10}	A_{11}	A_{12}	A_9	A_{10}	A_{11}	A_{12}	m	0	-	0	0
A_{13}	A_{14}	A_{15}	A_{16}	A_{13}	A_{14}	A_{15}	A_{16}	A_{13}	A_{14}	A_{15}	A_{16}	0	-	0	0	0
A_{17}	A_{18}	A_{19}	A_{20}	A_{17}	A_{18}	A_{19}	A_{20}	A_{17}	A_{18}	A_{19}	A_{20}	m	1	-	0	0
A_{21}	A_{22}	A_{23}	A_{24}	A_{21}	A_{22}	A_{23}	A_{24}	A_{21}	A_{22}	A_{23}	A_{24}	e_2	-	1	0	0
A_1	A_2	A_3	A_4	B_1	B_2	B_3	B_4	B_1	B_2	B_3	B_4	m	0	-	0	1
A_5	A_6	A_7	A_8	B_5	B_6	B_7	B_8	B_5	B_6	B_7	B_8	0	-	1	0	1
A_9	A_{10}	A_{11}	A_{12}	B_9	B_{10}	B_{11}	B_{12}	B_9	B_{10}	B_{11}	B_{12}	m	1	-	0	1
A_{13}	A_{14}	A_{15}	A_{16}	B_{13}	B_{14}	B_{15}	B_{16}	B_{13}	B_{14}	B_{15}	B_{16}	e_3	-	1	0	1
A_{17}	A_{18}	A_{19}	A_{20}	B_{17}	B_{18}	B_{19}	B_{20}	B_{17}	B_{18}	B_{19}	B_{20}	m	0	-	0	1
A_{21}	A_{22}	A_{23}	A_{24}	B_{21}	B_{22}	B_{23}	B_{24}	B_{21}	B_{22}	B_{23}	B_{24}	1	-	0	0	1
A_1	A_2	A_3	A_4	A_1	A_2	A_3	A_4	C_1	C_2	C_3	C_4	m	1	-	1	0
A_5	A_6	A_7	A_8	A_5	A_6	A_7	A_8	C_5	C_6	C_7	C_8	e_4	-	0	1	0
A_9	A_{10}	A_{11}	A_{12}	A_9	A_{10}	A_{11}	A_{12}	C_9	C_{10}	C_{11}	C_{12}	m	0	-	1	0
A_{13}	A_{14}	A_{15}	A_{16}	A_{13}	A_{14}	A_{15}	A_{16}	C_{13}	C_{14}	C_{15}	C_{16}	0	-	0	1	0
A_{17}	A_{18}	A_{19}	A_{20}	A_{17}	A_{18}	A_{19}	A_{20}	C_{17}	C_{18}	C_{19}	C_{20}	m	1	-	1	0
A_{21}	A_{22}	A_{23}	A_{24}	A_{21}	A_{22}	A_{23}	A_{24}	C_{21}	C_{22}	C_{23}	C_{24}	e_5	-	1	1	0
A_1	A_2	A_3	A_4	B_1	B_2	B_3	B_4	D_1	D_2	D_3	D_4	m	0	-	1	1
A_5	A_6	A_7	A_8	B_5	B_6	B_7	B_8	D_5	D_6	D_7	D_8	1	-	1	1	1
A_9	A_{10}	A_{11}	A_{12}	B_9	B_{10}	B_{11}	B_{12}	D_9	D_{10}	D_{11}	D_{12}	m	1	-	1	1
A_{13}	A_{14}	A_{15}	A_{16}	B_{13}	B_{14}	B_{15}	B_{16}	D_{13}	D_{14}	D_{15}	D_{16}	e_6	-	1	1	1
A_{17}	A_{18}	A_{19}	A_{20}	B_{17}	B_{18}	B_{19}	B_{20}	D_{17}	D_{18}	D_{19}	D_{20}	m	0	-	1	1
A_{21}	A_{22}	A_{23}	A_{24}	B_{21}	B_{22}	B_{23}	B_{24}	D_{21}	D_{22}	D_{23}	D_{24}	1	-	0	1	1

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A_n	Signalling bits	F	Frame alignment signal bits
C_n	Signalling bits	m	Data link bits
B_n	Signalling bits	e_n	CRC bits
D_n	Signalling bits	FAS	Frame alignment signal
		S	Signalling multiframe FAS

Figure 10-14 – Out slot signalling assignments (24-channel signalling operations)

10.1.5.4 Byte synchronous mapping of 384 kbit/s

The byte synchronous mapping for four-byte interleaved 384 kbit/s tributaries is shown in Figure 10-15.

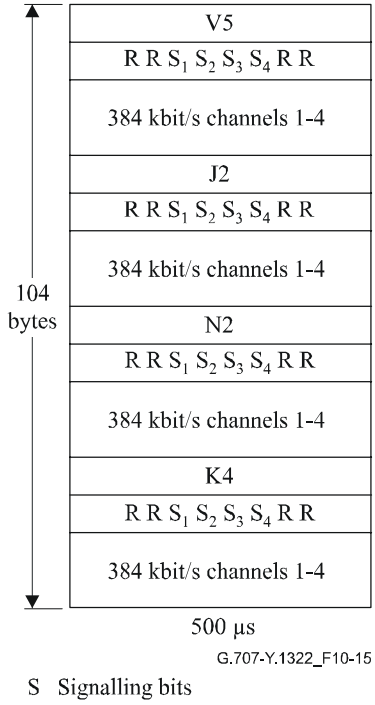


Figure 10-15 – Byte synchronous mapping for 384 kbit/s tributaries

The S_1, S_2, S_3 and S_4 bits contain the signalling for each of the four 384 kbit/s channels. The out slot signalling assignments for the channel associated signalling methods is shown in Figure 10-16.

Frame number	n	n + 1	n + 2	n + 3	n + 4	n + 5	n + 6	n + 7
Use of S_i bits (i = 1, 2, 3, 4)	F_s	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	X
(Notes 1 and 4)	(Note 2)	(Note 3)						(Note 5)

NOTE 1 – Each S_i (i = 1, 2, 3, 4) constitutes an independent signalling multiframe over eight frames. S_i includes the phase indicator in itself so that the PP bits cannot be used for the phase indicator.

NOTE 2 – The F_s bit is either alternate 0, 1 or the following 48-bit digital pattern:

A101011011 0000011001 1010100111 0011110110 10000101

For the 48-bit digital pattern, the A-bit is usually fixed to state 1 and is reserved for optional use. The pattern is generated according to the following primitive polynomial (refer to ITU-T Rec. X.50):

$$X^7 + X^4 + 1$$

NOTE 3 – Y_j bit (j = 1 to 6) carries channel associated signalling or maintenance information. When the 48-bit pattern is adopted as F_s frame alignment signal, each Y_j bit (j = 1 to 6) can be multiframed, as follows:

$$Y_{j1}, Y_{j2}, \ldots, Y_{j12}$$

Y_{j1} bit carries the following 16-bit frame alignment pattern generated according to the same primitive polynomial as for the 48-bit pattern.

A011101011011000

The A-bit is usually fixed to 1 and is reserved for optional use. Each Y_{ji} (i = 2 to 12) bit carries channel associated signalling for subrate circuits and/or maintenance information.

NOTE 4 – S_i bits (F_s, Y_1, …, Y_6 and X) all at state 1 indicate alarm indication signal (AIS) for six 64 kbit/s channels.

NOTE 5 – The X-bit is usually fixed to state 1. When backward AIS for six 64 kbit/s channels is required, the X-bit is set to state 0.

Figure 10-16 – Out slot signalling assignments

Table 10-1 – Differences between G.707 and G.704 naming

G.707	G.704
S_i	ST_i
Y_j	S_j
X	S_p

10.1.6 VC-11 to VC-12 conversion for transport by a TU-12

When transporting a VC-11 in a TU-12, the VC-11 is adapted by adding fixed stuff with even parity as shown in Figure 10-17. Thus the resulting TU-12 payload can be monitored and cross-connected in the network as though it were a VC-12 with its BIP value unchanged while preserving end-to-end integrity of the real VC-11 path.

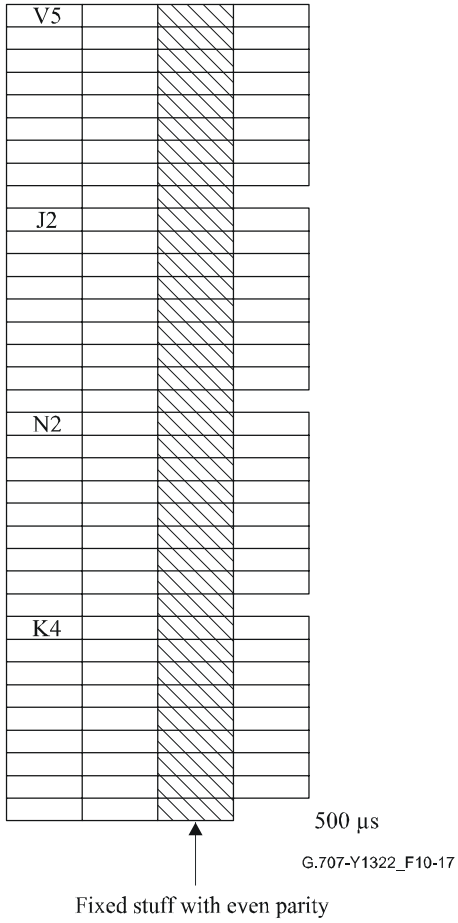


Figure 10-17 – Conversion of VC-11 to VC-12 for transport by TU-12

10.2 Mapping of ATM cells

The mapping of ATM cells is performed by aligning the byte structure of every cell with the byte structure of the virtual container used including the concatenated structure (VC-n, VC-n-X, n ≥ 1). Since the relevant container-n, container-n-Xc or container-n-Xv capacity may not be an integer multiple of the ATM cell length (53 bytes), a cell is allowed to cross the container-n, container-n-Xc or container-n-Xv frame boundary.

The ATM cell information field (48 bytes) shall be scrambled before mapping into the VC-n or VC-n-X. In the reverse operation, following termination of the VC-n or VC-n-X signal, the ATM cell information field will be descrambled before being passed to the ATM layer.

A self-synchronizing scrambler with polynomial $x^{43} + 1$ shall be used. The scrambler operates for the duration of the cell information field. During the 5-byte header the scrambler operation is suspended and the scrambler state retained. The first cell transmitted on start-up will be corrupted because the descrambler at the receiving end will not be synchronized to the transmitter scrambler. Cell information field scrambling is required to provide security against false cell delineation and cell information field replicating the STM-N frame alignment word.

When the VC-n or VC-n-X is terminated, the cell must be recovered. The ATM cell header contains a header error control (HEC) field which may be used in a similar way to a frame alignment word to achieve cell delineation. This HEC method uses the correlation between the header bits to be protected by the HEC (32 bits) and the control bit of the HEC (8 bits) introduced in the header after computation with a shortened cyclic code with generating polynomial $g(x) = x^8 + x^2 + x + 1$.

The remainder from this polynomial is then added to the fixed pattern "01010101" in order to improve the cell delineation performance. This method is similar to conventional frame alignment recovery where the alignment word is not fixed but varies from cell to cell.

More information on HEC cell delineation is given in ITU-T Rec. I.432.1.

10.2.1 Mapping into VC-4-Xc/VC-4-Xv

The ATM cell stream is mapped into a container-4-Xc or container-4-Xv with its byte boundaries aligned with the container-4-Xc or container-4-Xv byte boundaries. The container-4-Xc or container-4-Xv is then mapped into VC-4-X together with the VC-4-X POH and (X-1) columns of fixed stuff (see Figure 10-18). The ATM cell boundaries are thus aligned with the VC-4-X byte boundaries. Since the container-4-Xc or container-4-Xv capacity (X × 2340 bytes) is not an integer multiple of the cell length (53 bytes), a cell may cross a container-4-Xc or container-4-Xv frame boundary.

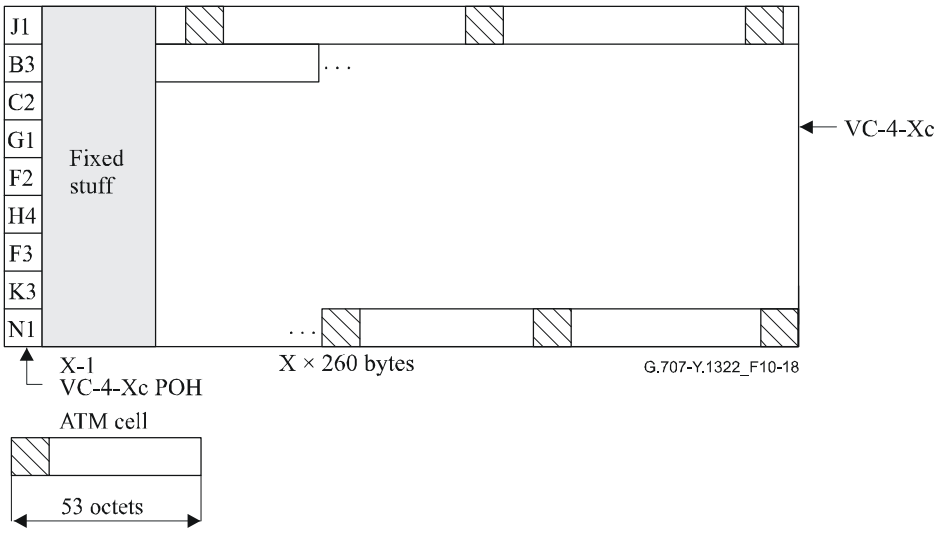


Figure 10-18 – Mapping of ATM cells into VC-4-Xc

10.2.2 Mapping into VC-4/VC-3

The ATM cell stream is mapped into container-4/container-3 with its byte boundaries aligned with the container-4/container-3 byte boundaries. The container-4/container-3 is then mapped into VC-4/VC-3 together with the VC-4/VC-3 POH (see Figure 10-19). The ATM cell boundaries are thus aligned with the VC-4/VC-3 byte boundaries. Since the C-4/C-3 capacity (2340/756 bytes respectively) is not an integer multiple of the cell length (53 bytes), a cell may cross a container-4/container-3 frame boundary.

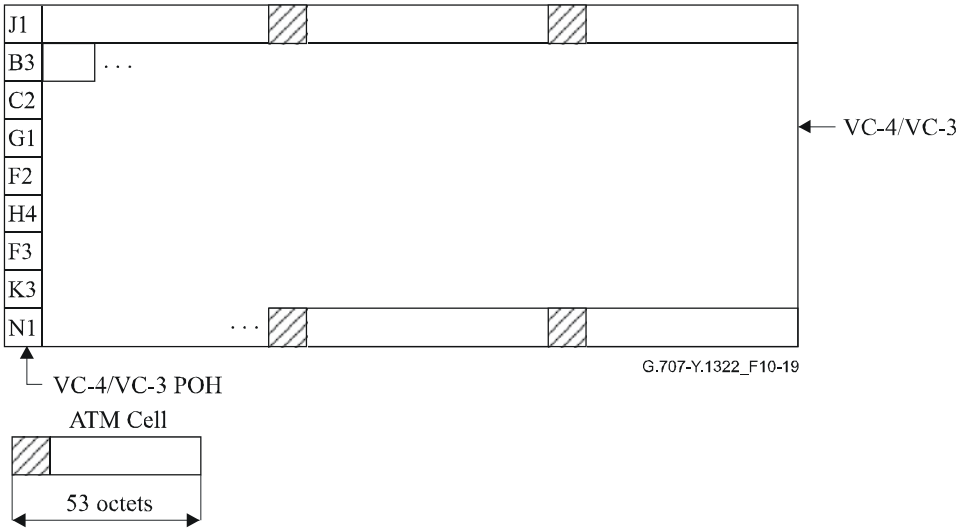
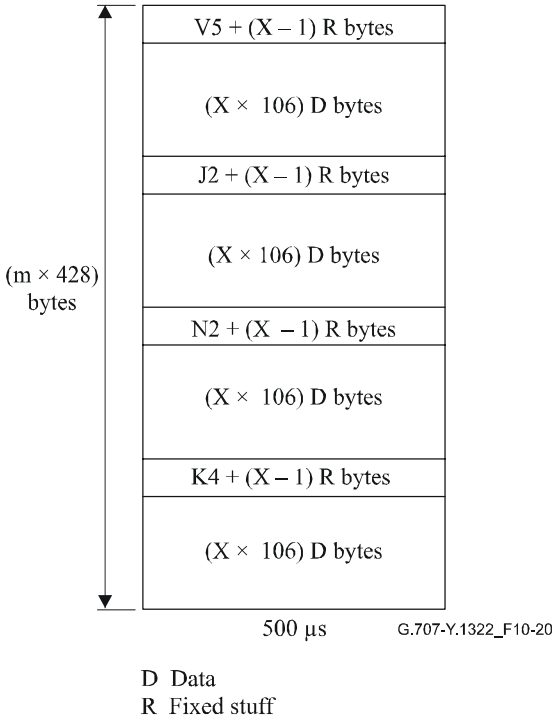


Figure 10-19 – Mapping of ATM cells into VC-4/VC-3

10.2.3 Mapping into VC-2-Xc/VC-2-Xv

Figure 10-20 shows the mapping for an ATM cell stream with a data rate of X × 6.784 Mbit/s where "X" can take any integer value between 1 and 7 inclusive for contiguous concatenation, and between 1 and 64 inclusive for virtual concatenation.

The VC-2-X structure is organized as a four-frame multiframe. The frames of the VC-2-Xc (contiguous concatenation) multiframe consist of one byte of POH, (X-1) stuff bytes and (X × 106) bytes of payload area. The frames of the VC-2-Xv (virtual concatenation), multiframe consist of X independent bytes of POH and (X × 106) bytes of payload area. ATM cells are loaded into the VC-2-X payload area with the boundaries of the cells aligned with any VC-2-X byte boundary. Because the VC-2-X payload space is equivalent of exactly (X × 2) ATM cells per 125 µs frame, the alignment between ATM cell boundaries and the VC-2-X structure will remain constant from frame to frame. Cells can cross VC-2-X frame boundaries.



NOTE – In the case of virtual concatenation, the frames contain X independent VC-2-mc POH bytes.

Figure 10-20 – Mapping of ATM cells into VC-2-Xc using contiguous concatenation

10.2.4 Mapping into VC-2

Figure 10-21 shows the mapping for an ATM cell stream with a data rate of 6.784 Mbit/s.

The VC-2 structure is organized as a four-frame multiframe. The frames of the multiframe consist of one byte of VC-2 POH and 106 bytes of payload area. ATM cells are loaded into the VC-2 payload area with the boundaries of the cells aligned with any VC-2 byte boundary. Because the VC-2 payload space is the equivalent of exactly two ATM cells per 125 µs frame, the alignment between ATM cell boundaries and the VC-2 structure will remain constant from frame to frame. Cells can cross VC-2 frame boundaries.

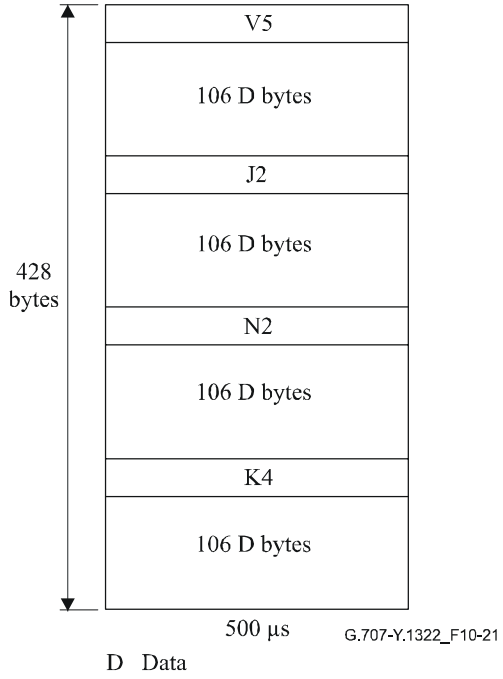


Figure 10-21 – Mapping of ATM cells into VC-2

10.2.5 Mapping into VC-12/VC-11

Figures 10-22 and 10-23 show the mapping for ATM cell streams with data rates of 2.176 Mbit/s and 1.600 Mbit/s into VC-12 and VC-11, respectively.

In floating TU-n mode, the VC-12/VC-11 structure is organized as a four-frame multiframe. The frames of the multiframe consist of one byte of VC-12/VC-11 POH and 34 or 25 bytes, respectively, of payload area. ATM cells are loaded into the VC-12/VC-11 payload area with the boundaries of the cells aligned with any VC-12/VC-11 byte boundary. Because the VC-12/VC-11 payload space is not related to the size of an ATM cell (53 bytes), the alignment between ATM cell boundaries and the VC-12/VC-11 structure will change from frame to frame in a sequence repeating every 53 frames. Cells can cross VC-12/VC-11 frame boundaries.

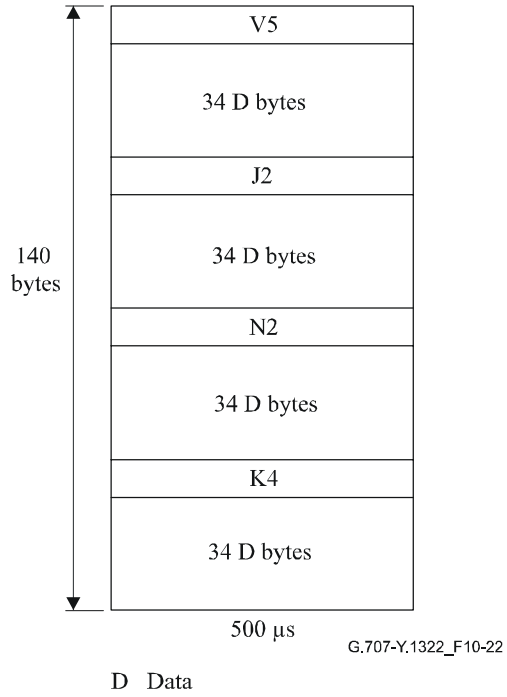


Figure 10-22 – Mapping of ATM cells into VC-12

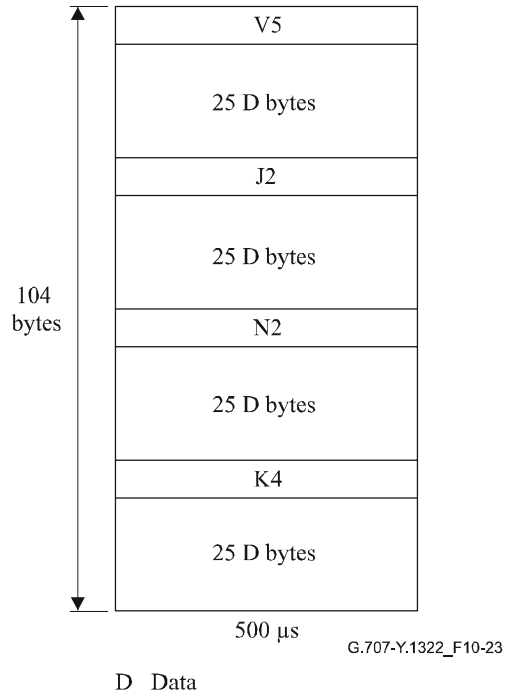


Figure 10-23 – Mapping of ATM cells into VC-11

10.3 Mapping of HDLC framed signals

The mapping of HDLC framed signals [2] is performed by aligning the byte structure of every frame with the byte structure of the virtual container used, including the concatenated structure (VC-n-Xc/VC-n-Xv/VC-n). Since the HDLC frames are of variable length (the mapping does not impose any restrictions on the maximum length), a frame may cross the container-x frame boundary.

HDLC flags (01111110) shall be used for interframe fill to buffer out the asynchronous nature of the arrival of the HDLC framed signals according to the effective payload of the virtual container used (this excludes any fixed stuff bytes).

The HDLC framed signal plus the interframe fill shall be scrambled before they are inserted as payload of the virtual container (VC-n-Xc/VC-n-Xv/VC-4/VC-3) used. In the reverse operation, following termination of the VC signal, the payload will be descrambled before it is passed on to the HDLC layer. A self-synchronizing scrambler with polynomial $x^{43}+1$ shall be used.

The $x^{43}+1$ scrambler shall operate continuously through the bytes of the VC-n-Xc/VC-n-Xv/VC-4/VC-3, bypassing bytes of SDH path overhead. The scrambling state at the beginning of a VC-n-Xc/VC-n-Xv/VC-4/VC-3 shall be the state at the end of the previous VC-n. Thus, the scrambler runs continuously and is not reset per frame. An initial seed of the scrambler is unspecified. Consequently, the first 43 transmitted bits following start-up or SDH reframe operation will not be descrambled correctly.

The $x^{43}+1$ scrambler operates on the input data stream with most significant bit (MSB) first, consistent with the bit ordering and transmission ordering defined for SDH in clause 5.

The above mapping procedure with scrambling shall be used for the mapping of HDLC framed signals (e.g., HDLC/PPP or HDLC/LAPS with IP packets) in any VC-n-Xc/VC-n-Xv/VC-4/VC-3 while scrambling is not required for VC-2/VC-12/VC-11.

There are no further specific requirements for any virtual container size, other than that the appropriate signal label for that container is inserted in the appropriate path overhead location. Path signal labels are specified in clause 9.3.

NOTE – HDLC/PPP frames [13] are also referred to as packet over SDH/SONET (PoS) frames.

10.4 Mapping of DQDB into VC-4

The mapping of distributed queue dual bus (DQDB) signals [1] should be performed according to ETSI ETS 300 216.

10.5 Asynchronous mapping for FDDI at 125 000 kbit/s into VC-4

The 125 000 kbit/s fibre distributed data interface (FDDI) physical layer signal [3]-[11] is mapped into an SDH VC-4. The VC-4 consists of 1 column (9-bytes) of path overhead (POH) plus a 9-row by 260-column payload structure. For this mapping, each row of 260 bytes is partitioned into 20 blocks of 13 bytes each, see Figure 10-24.

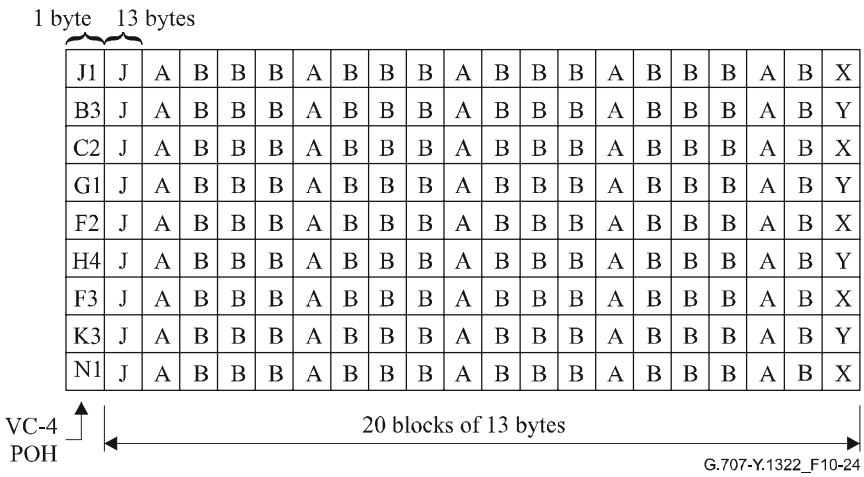


Figure 10-24 – Block structure of VC-4 for asynchronous mapping of FDDI

There are five block types: J, A, B, X and Y. The blocks consist of 13 bytes. The definitions of them are given in Figure 10-25.

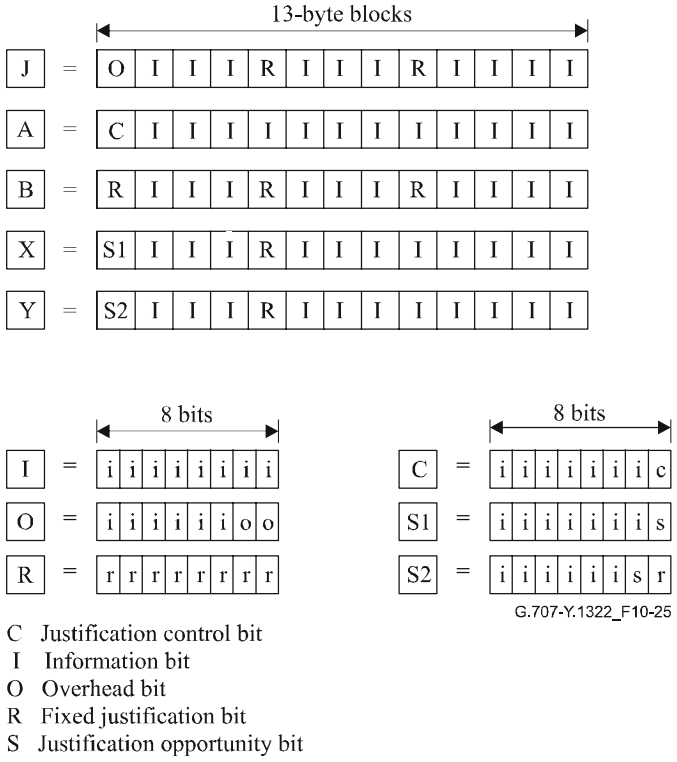


Figure 10-25 – Block contents for asynchronous mapping of FDDI

In order to accommodate the asynchronous FDDI payload (approximately 15 625 ± 1 bits per VC-4), a bit justification mechanism is utilized. The 15 620 information bits (**i**) and the 9 justification opportunity bits (**s**) within this structure carry the FDDI physical layer bits. In each row of the payload structure, five justification control bits (**c**) are used to control the corresponding justification opportunity bit (**s**) of that row.

If the **s** bit is used to carry information, the five **c** bits are set to zero {**c c c c c** = 0 0 0 0 0}. If the **s** bit is used as a justification bit, the five **c** bits are set to one {**c c c c c** = 1 1 1 1 1}. The value contained in the **s** bit when used as a justification bit is not defined. The receiver shall ignore the value contained in this bit whenever it is used as a justification bit. Majority vote should be used to make the justification decision in the desynchronizer for protection against single- and double-bit errors in the **c** bits.

The overhead bits (**o**) are reserved for future overhead communication purposes. The remaining bits are fixed stuff bits (**r**).

10.6 Mapping of GFP frames

The GFP frame stream is mapped into a container-n (n = 11, 12, 2, 3, 4, 4-Xc, 11-Xv/12-Xv/2-Xv/3-Xv/4-Xv) with its byte boundaries aligned with the byte boundaries of the container-n (see Figure 10-26). The container-n is then mapped into the VC-n respectively, together with the associated POH as specified in clause 9.3. The GFP frame boundaries are thus aligned with the VC-n byte boundaries. Since the container-n capacity is not an integer multiple of the variable length GFP Frame, a GFP frame may cross a container-n frame boundary.

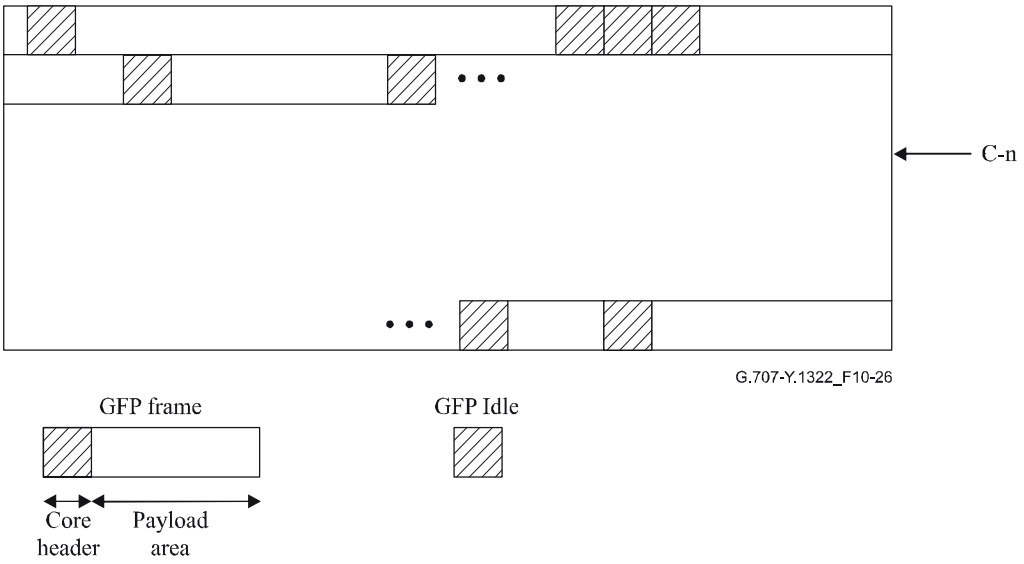


Figure 10-26 – Mapping of GFP frames into C-n

A GFP frame consists of a GFP core header and a GFP payload area. GFP frames arrive as a continuous byte stream with a capacity that is identical to the VC payload, due to the insertion of GFP Idles at the GFP adaptation stage. See also ITU-T Rec. G.7041/Y.1303.

NOTE – There is no rate adaptation or scrambling required at the mapping stage. The GFP adaptation process performs these functions.

10.7 Asynchronous mapping of ODUk into a C-4-X transported via a VC-4-Xv

The purpose of this mapping is to provide for the transport of a subset of OTN elements, as defined in ITU-T Rec. G.709/Y.1331, over existing SDH transport networks by means of VC-4 virtual concatenation.

The number of VC-4s required to transport an OTN element by means of virtual concatenation is found by dividing the bit rate of the OTN entity by the payload rate of a VC-4-Xv, the C-4-X. These are provided in Table 10-2. As this number is not an integer, it is necessary to provide both a fixed stuff to pad the C-4-X payload area and a means of mapping the client into the remainder of the payload area.

Table 10-2 – Mapping of OTN elements in SDH virtually concatenated VC-4s

OTN entity	Nominal bit rate, kbit/s ODUk	VC-4 virtual concatenation order (X)	Nominal bit rate, kbit/s VC-4-Xv
ODU1	239/238 × 2 488 320 (≈2 498 775.126)	17	2 545 920
ODU2	239/237 × 9 953 280 (≈10 037 273.924)	68	10 183 680

The ODUk signal is extended with frame alignment overhead (FAS and MFAS bytes) as specified in clauses 15.6.2.1 and 15.6.2.2/G.709/Y.1331 and an all-0's pattern in the OTUk overhead field (Figure 10-27).

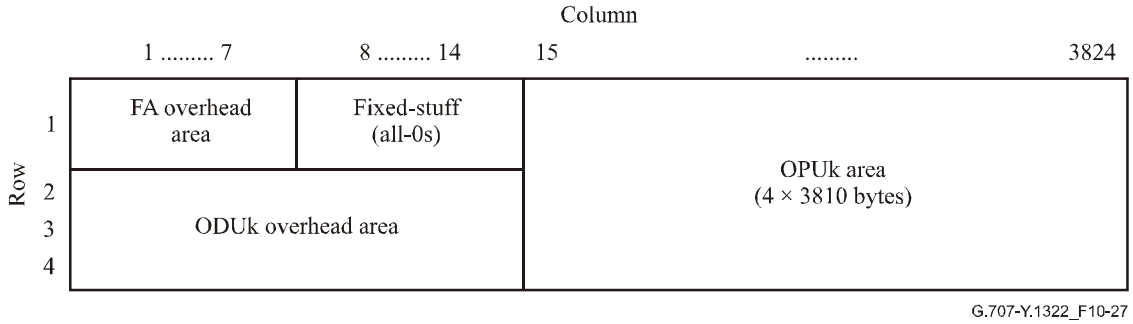


Figure 10-27 – Extended ODUk frame structure
(FA OH included, OTUk OH area contains fixed stuff)

Before the extended ODUk signal is mapped into the C-4-X, it is scrambled using a self-synchronizing scrambler with polynomial $x^{43}+1$. The scrambler operates over the whole extended ODUk frame and is not reset per frame.

10.7.1 Asynchronous mapping of ODU1 into a C-4-17 transported via a VC-4-17v

The basic C-4-17 structure is as shown in Figure 10-28. It is comprised of 9 rows by 4420 (i.e., 17 × 260) columns.

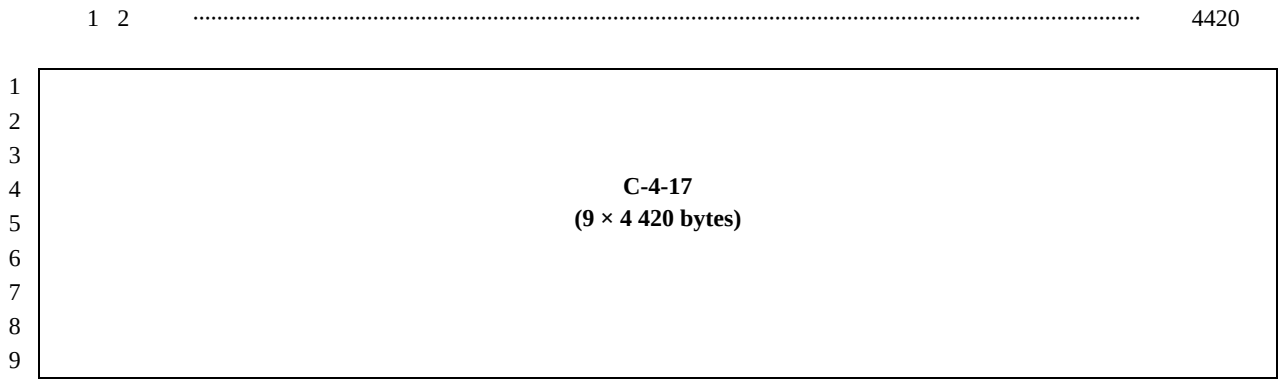


Figure 10-28 – C-4-17 structure

This C-4-17 frame is transported via a VC-4-17v. Refer to clause 11.2.

The extended ODU1 signal is asynchronously mapped into this C-4-17 with the following structure:

– Each of the nine rows is partitioned into 5 blocks, consisting of 884 octets each (Figure 10-29).

– Each block is partitioned into 17 subblocks, consisting of 52 octets each.

  • In each subblock, one negative justification opportunity octet (S) and five justification control bits (C) are provided.

- The first byte of each subblock consists of either:
  - a fixed stuff byte (R); or
  - a justification control byte (J), which consists of seven fixed stuff bits (bits R; bits 1 to 7) and a justification control bit (bit C, bit 8); or
  - a negative justification opportunity byte (S).
- The last 51 bytes of one subblock consist of data bytes (D).

NOTE 1 – Each block contains a total of (17 × 51) = 867 data bytes.

The sequence of all these bytes is shown in Figure 10-29.

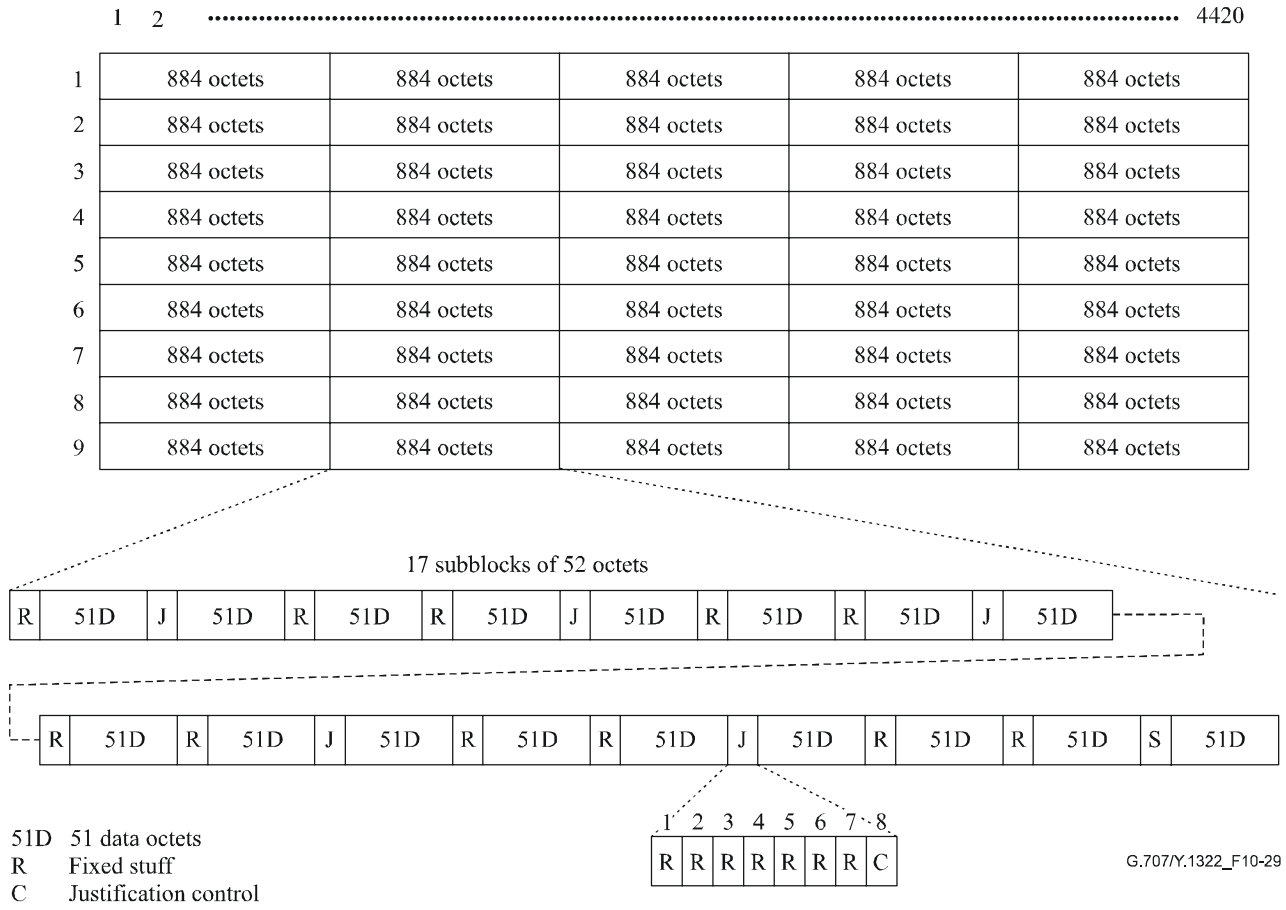


Figure 10-29 – Block structure for ODU1 mapping into C-4-17

The set of five justification control bits (C) in every subblock is used to control the corresponding negative justification opportunity byte (S). CCCCC = 00000 indicates that the S byte is an information byte, whereas CCCCC = 11111 indicates that the S byte is a justification byte.

At the synchronizer all five C bits are set to the same value. Majority vote (3 out of 5) should be used to make the justification decision at the desynchronizer for protection against single and double bit errors in the JC bits.

The value contained in the S byte when used as justification byte is all-ZEROs. The receiver is required to ignore the value contained in this byte whenever it is used as a justification byte.

The value contained in the R bits and bytes is all-ZEROs. The receiver is required to ignore the value contained in these bits/bytes.

NOTE 2 – The maximum bit-rate tolerance between C-4-17 and the ODU1 signal clock, which can be accommodated by this mapping scheme, is approximately –720 to +420 ppm. The nominal justification ratio

is 75/119, which is approximately equal to 0.630252. Here, the justification ratio is normalized to 1, i.e., it is the long-run average fraction of justification opportunities for which there is a justification.

10.7.2 Asynchronous mapping of ODU2 into a C-4-68 transported via a VC-4-68v

The basic C-4-68 structure is as shown in Figure 10-30. It is comprised of 9 rows by 17 680 (i.e., 68 × 260) columns.

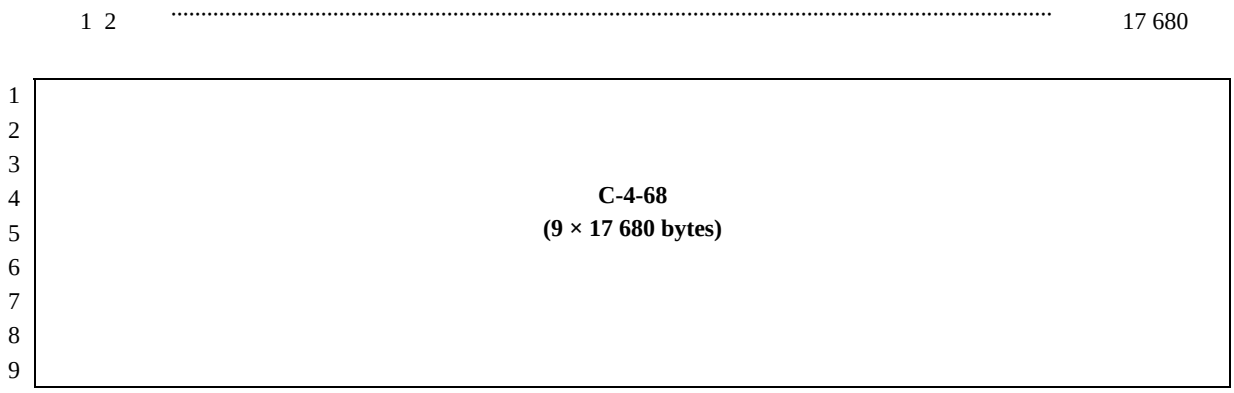


Figure 10-30 – C-4-68 structure

This C-4-68 frame is transported via a VC-4-68v. Refer to clause 11.2.

The extended ODU2 signal is asynchronously mapped into this C-4-68 with the following structure:

– Each of the nine rows is partitioned into 20 blocks, consisting of 884 octets each (Figure 10-31).

– Each block is partitioned into 13 subblocks, consisting of 68 octets each.

  • In each subblock, one negative justification opportunity octet (S) and five justification control bits (C) are provided.

  • The first byte of each subblock consists of either:

    – a fixed stuff byte (R); or

    – a justification control byte (J), which consists of seven fixed stuff bits (bits R; bits 1 to 7) and a justification control bit (bit C, bit 8); or

    – a negative justification opportunity byte (S).

  • The last 67 bytes of one subblock consist of data bytes (D).

  NOTE 1 – Each block contains a total of (13 × 67) = 871 data bytes.

The sequence of all these bytes is shown in Figure 10-31.

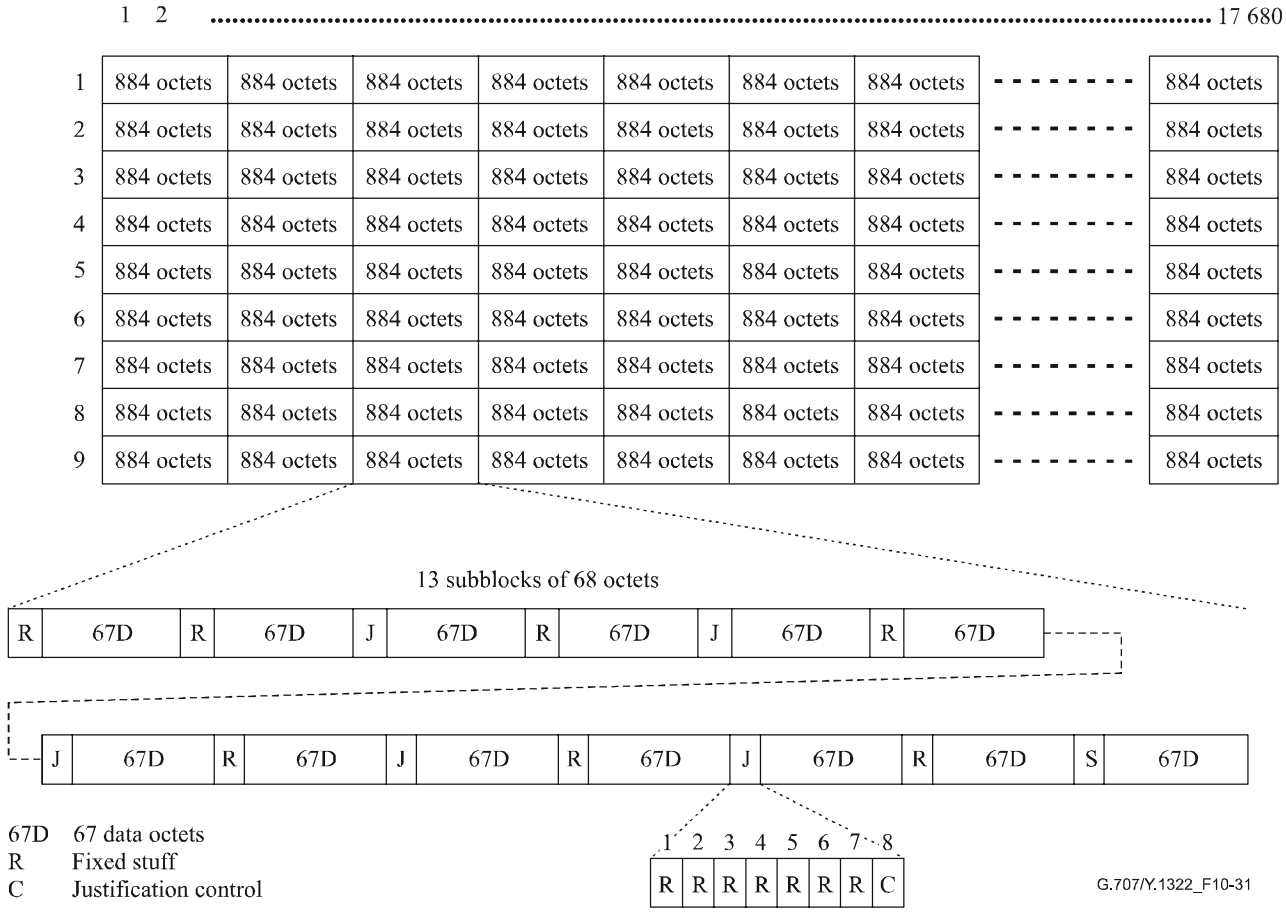


Figure 10-31 – Block structure for ODU2 mapping into C-4-68

The set of five justification control bits (C) in every subblock is used to control the corresponding negative justification opportunity byte (S). CCCCC = 00000 indicates that the S byte is an information byte, whereas CCCCC = 11111 indicates that the S byte is a justification byte.

At the synchronizer, all five C bits are set to the same value. Majority vote (3 out of 5) should be used to make the justification decision at the desynchronizer for protection against single- and double-bit errors in the JC bits.

The value contained in the S byte, when used as justification byte, is all-ZEROs. The receiver is required to ignore the value contained in this byte whenever it is used as a justification byte.

The value contained in the R bits and bytes is all-ZEROs. The receiver is required to ignore the value contained in these bits/bytes.

NOTE 2 – The maximum bit-rate tolerance between C-4-68 and the ODU2 signal clock, which can be accommodated by this mapping scheme, is approximately –330 to +810 ppm. The nominal justification ratio is 23/79, which is approximately equal to 0.291139. Here, the justification ratio is normalized to 1, i.e., it is the long-run average fraction of justification opportunities for which there is a justification.

11 VC concatenation

For the transport of payloads that do not fit efficiently into the standard set of virtual containers (VC-11, VC-12, VC-2, VC3, VC4) VC concatenation can be used. VC concatenation is defined for:

VC-4 – to provide transport for payloads that require capacity greater than one container-4;

VC-3 – to provide transport for payloads that require capacity greater than one container-3;

VC-2 – to provide transport for payloads that require capacity greater than one container-2;

VC-12 – to provide transport for payloads that require capacity greater than one container-12;

VC-11 – to provide transport for payloads that require capacity greater than one container-11.

Two methods for concatenation are defined: contiguous and virtual concatenation. Both methods provide concatenated bandwidth of X*container-n at the path termination. The difference is the transport between the path terminations. Contiguous concatenation maintains the contiguous bandwidth throughout the whole transport, while virtual concatenation breaks the contiguous bandwidth into individual VCs, transports the individual VCs and recombines these VCs to a contiguous bandwidth at the end point of the transmission. Virtual concatenation requires concatenation functionality only at the path termination equipment, while contiguous concatenation requires concatenation functionality at each network element.

It is possible to perform a conversion between the two types of concatenation. The conversion between virtual and contiguous VC-4 concatenation is defined in ITU-T Rec. G.783. The conversion between virtual and contiguous VC-2 concatenation is for further study.

11.1 Contiguous concatenation of X VC-4s (VC-4-Xc, X = 4, 16, 64, 256)

A VC-4-Xc provides a payload area of X*container-4 and is represented by a C-4-X structure as shown in Figure 11-1. One common set of POH, located in the first column, is used for the whole VC-4-Xc (e.g., the BIP-8 covers all 261*X columns of the VC-4-Xc). Columns 2 to X are fixed stuff.

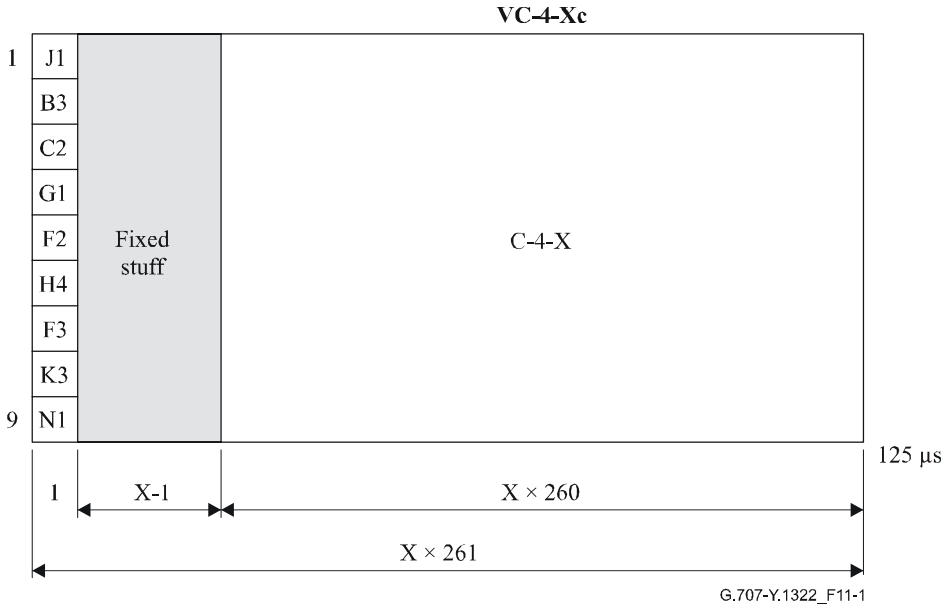


Figure 11-1 – VC-4-Xc structure

The VC-4-Xc is transported in X contiguous AU-4 in the STM-N signal. The first column of the VC-4-Xc is always located in the first AU-4. The pointer of this first AU-4 indicates the position of the J1 byte of the VC-4-Xc. The pointers of the AU-4 #2 to X are set to the concatenation indication

(see Figure 8-3) to indicate the contiguously concatenated payload. Pointer justification is performed in common for the X concatenated AU-4s and X*3 stuffing bytes are used.

A VC-4-Xc provides a payload capacity of 599'040 kbit/s for X = 4, 2'396'160 kbit/s for X = 16, 9'584'640 kbit/s for X = 64 and 38'338'560 kbit/s for X = 256.

NOTE – High rate VC-4-Xc could be used without any constraints in point-to-point connections. SDH networks may be limited to a certain bit rate of VC-4-Xc (e.g., X ≤ 64), e.g., due to rings with MS SPRING that has to reserve 50% of the STM-N bandwidth for protection.

11.2 Virtual concatenation of X VC-3s/VC-4s (VC-3-Xv/VC-4-Xv, X = 1 ... 256)

A VC-3-Xv/VC-4-Xv provides the transport capability equivalent to X*container-3/container-4, which can be represented by a C-3-X/C-4-X like structure, and has a payload capacity of X*48'384/149'760 kbit/s as depicted in Figures 11-2 and 11-3. The payload is mapped into X individual VC-3s/VC-4s which form the VC-3-Xv/VC-4-Xv, as illustrated in Appendix XIV. Each VC-3/VC-4 has its own POH as specified in clause 9.3.1. The H4 POH byte is used for the virtual concatenation-specific sequence and multiframe indication as defined below.

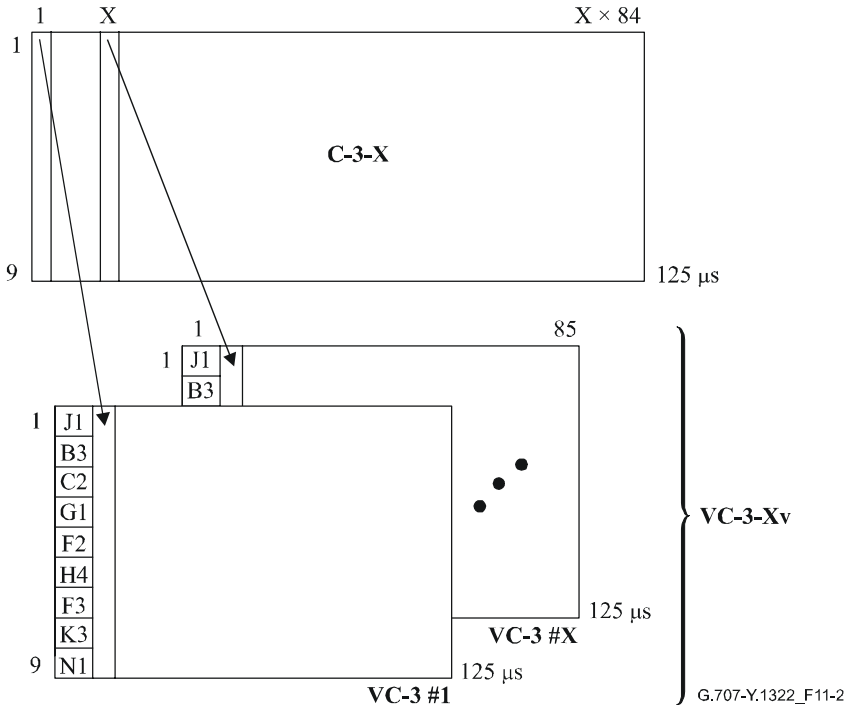


Figure 11-2 – VC-3-Xv structure

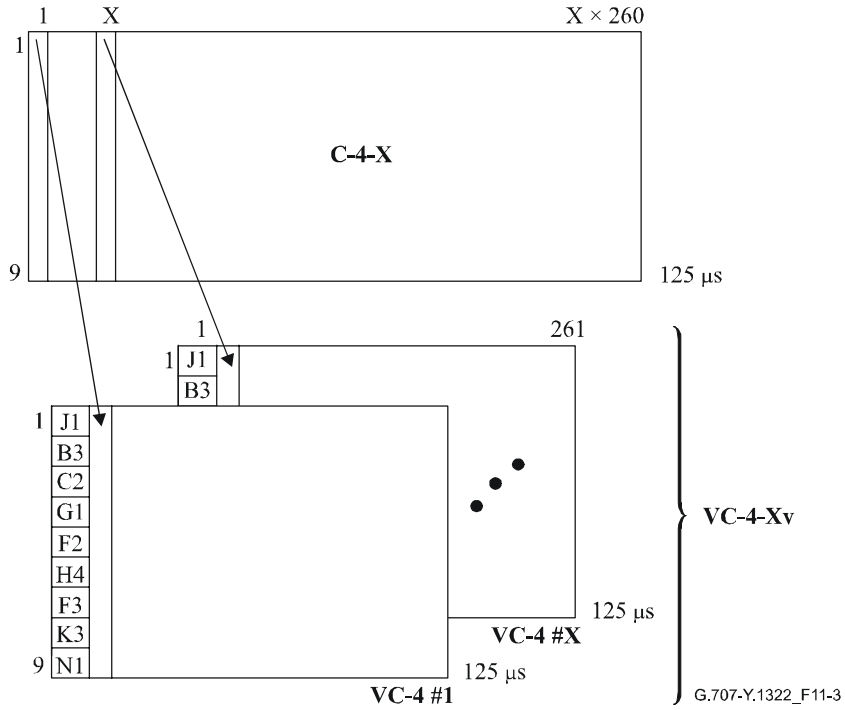


Figure 11-3 – VC-4-Xv structure

Each VC-3/VC-4 of the VC-3-Xv/VC-4-Xv is transported individually through the network. Due to the different propagation delays of the VC-3s/VC-4s, a differential delay will occur between the individual VC-3s/VC-4s. At the path termination this differential delay has to be compensated and the individual VC-3s/VC-4s have to be realigned for access to the contiguous payload area. The realignment process has to cover at least a differential delay of 125 µs.

A two-stage 512 ms multiframe is introduced to cover differential delays of 125 µs and above (up to 256 ms). The first stage uses H4, bits 5-8 for the 4-bit multiframe indicator (MFI1). MFI1 is incremented every basic frame and counts from 0 to 15. For the 8-bit multiframe indicator of the second stage (MFI2), H4, bits 1-4 in frame 0 (MFI2 bits 1-4) and 1 (MFI2 bits 5-8) of the first multiframe are used (see Table 11-1). MFI2 is incremented once every multiframe of the first stage and counts from 0 to 255. The resulting overall multiframe is 4096 frames (= 512 ms) long.

Table 11-1 – VC-3-Xv/VC-4-Xv sequence and multiframe indicator H4 coding

H4 byte								1st multi-frame number	2nd multi-frame number
Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8		
				1st multiframe indicator MFI1 (bits 1-4)					
Sequence indicator MSB (bits 1-4)				1	1	1	0	14	n–1
Sequence indicator LSB (bits 5-8)				1	1	1	1	15	
2nd multiframe indicator MFI2 MSB (bits 1-4)				0	0	0	0	0	n
2nd multiframe indicator MFI2 LSB (bits 5-8)				0	0	0	1	1	
Reserved ("0000")				0	0	1	0	2	
Reserved ("0000")				0	0	1	1	3	
Reserved ("0000")				0	1	0	0	4	
Reserved ("0000")				0	1	0	1	5	
Reserved ("0000")				0	1	1	0	6	
Reserved ("0000")				0	1	1	1	7	
Reserved ("0000")				1	0	0	0	8	
Reserved ("0000")				1	0	0	1	9	
Reserved ("0000")				1	0	1	0	10	
Reserved ("0000")				1	0	1	1	11	
Reserved ("0000")				1	1	0	0	12	
Reserved ("0000")				1	1	0	1	13	
Sequence indicator SQ MSB (bits 1-4)				1	1	1	0	14	
Sequence indicator SQ LSB (bits 5-8)				1	1	1	1	15	
2nd multiframe indicator MFI2 MSB (bits 1-4)				0	0	0	0	0	n+1
2nd multiframe indicator MFI2 LSB (bits 5-8)				0	0	0	1	1	
Reserved ("0000")				0	0	1	0	2	

The sequence indicator (SQ) identifies the sequence/order in which the individual VC-3s/VC-4s of the VC-3-Xv/VC-4-Xv are combined to form the contiguous payload C-3-X/C-4-X like structure as shown in Figure 11-4. Each VC-3/VC-4 of a VC-3-Xv/VC-4-Xv has a fixed unique sequence number in the range of 0 to (X–1).

The VC-4 transporting the:

- data from cols 1, X+1, 2X+1, .. 259X+1 of the C-4-X like structure has the sequence number 0;
- data from cols 2, X+2, 2X+2, .. 259X+2 of the C-4-X like structure has the sequence number 1;

and so on up to the VC-4 transporting the:

- data from cols X, X+X, 2X+X, ..259X+X of the C-4-X like structure has the sequence number (X–1).

The VC-3 transporting the:

- data from cols 1, X+1, 2X+1, … 83X+1 of the C-3-X like structure has the sequence number 0;
- data from cols 2, X+2, 2X+2, … 83X+2 of the C-3-X like structure has the sequence number 1;

and so on up to the VC-3 transporting the:

- data from cols X, X+X, 2X+X, … 83X+X of the C-3-X like structure has the sequence number (X–1).

For applications requiring fixed bandwidth, the sequence number is fixed assigned and not configurable. This allows the constitution of the VC-3-Xv/VC-4-Xv to be checked without using the trace. The 8-bit sequence number (which supports values of X up to 256) is transported in bits 1 to 4 of the H4 bytes, using frame 14 (SQ bits 1-4) and 15 (SQ bits 5-8) of the first multiframe stage as shown in Table 11-1.

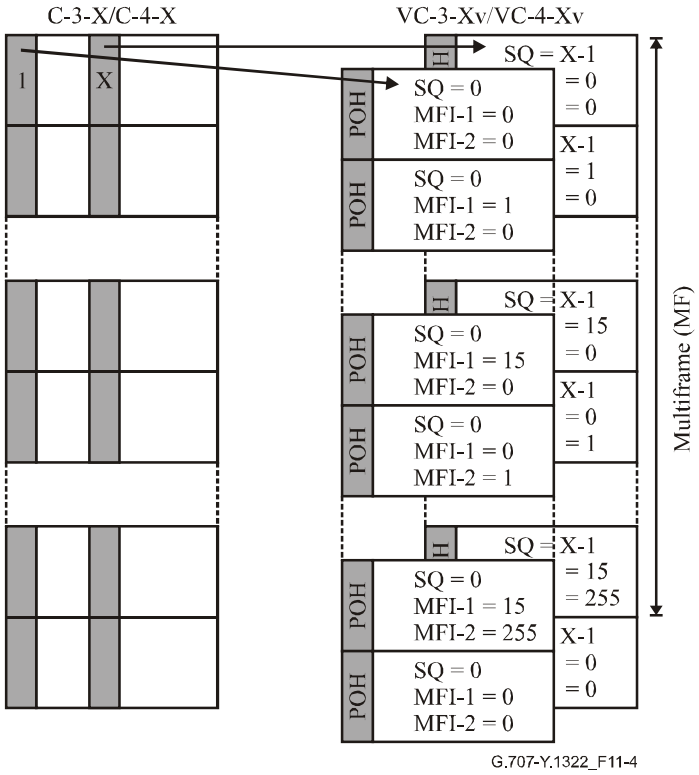


Figure 11-4 – VC-3-Xv/VC-4-Xv multiframe and sequence indicator

11.2.1 Higher order LCAS for VC-n-Xv (n = 3, 4)

Table 11-2 depicts the modified VC-3, VC-4 H4 HO virtual concatenation 1st multiframe, as defined in clause 11.2, indicating the control codes used for the support of HO LCAS. See also ITU-T Rec. G.7042/Y.1305.

– Frame indicator: A combination of the 1st multiframe and the 2nd multiframe counter [0-4095].

– Sequence indicator: Number to identify each member in the VCG [0-255].

– CTRL: LCAS control field, see Table 1/G.7042/Y.1305.

– GID: Group identification bit.

– Member status: The status report of the individual members uses the MST-multiframe as shown in Table 11-3. The status of all members (256) is transferred in 64 ms.

– RS-Ack: Re-sequence acknowledge bit.

– CRC: Eight-bit CRC check for fast acceptance of virtual concatenation OH. With this CRC-8 the probability of an undetected error is better than 1.52×10^{-16}. The CRC generator polynomial is $x^8 + x^2 + x + 1$.

Table 11-2 – VC-n-Xv sequence and multiframe indicator H4 coding

H4 byte								1st multi-frame number	2nd multi-frame number
Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8		
				1st multiframe indicator MFI1 (bits 1-4)					
Sequence indicator MSB (bits 1-4)				1	1	1	0	14	n–1
Sequence indicator LSB (bits 5-8)				1	1	1	1	15	
2nd multiframe indicator MFI2 MSB (bits 1-4)				0	0	0	0	0	n
2nd multiframe indicator MFI2 LSB (bits 5-8)				0	0	0	1	1	
CTRL				0	0	1	0	2	
GID ("000x")				0	0	1	1	3	
Reserved ("0000")				0	1	0	0	4	
Reserved ("0000")				0	1	0	1	5	
CRC-8				0	1	1	0	6	
CRC-8				0	1	1	1	7	
Member status MST				1	0	0	0	8	
Member status MST				1	0	0	1	9	
0	0	0	RS_Ack	1	0	1	0	10	
Reserved ("0000")				1	0	1	1	11	
Reserved ("0000")				1	1	0	0	12	
Reserved ("0000")				1	1	0	1	13	
Sequence indicator SQ MSB (bits 1-4)				1	1	1	0	14	
Sequence indicator SQ LSB (bits 5-8)				1	1	1	1	15	
2nd multiframe indicator MFI2 MSB (bits 1-4)				0	0	0	0	0	n+1
2nd multiframe indicator MFI2 LSB (bits 5-8)				0	0	0	1	1	
CTRL				0	0	1	0	2	
0	0	0	GID	0	0	1	1	3	
Reserved ("0000")				0	1	0	0	4	
Reserved ("0000")				0	1	0	1	5	
C_1	C_2	C_3	C_4	0	1	1	0	6	
C_5	C_6	C_7	C_8	0	1	1	1	7	
Member status MST				1	0	0	0	8	

Table 11-3 – H4 VC-n-Xv member status

2nd multiframe frame number	Member number				
0, 32, 64, 96, 128, 160, 192, 224	0	1	2	3	MST-multiframe
	4	5	6	7	
1, 33, 65, 97, 129, 161, 193, 225	8	9	10	11	
	12	13	14	15	
. . .	. . .	. . .	. . .	. . .	
30, 62, 94, 126, 158, 190, 222, 254	240	241	242	243	
	244	245	246	247	
31, 63, 95, 127, 159, 191, 223, 255	248	249	250	251	
	252	253	254	255	

NOTE 1 – There are 8 member statuses reported per VC-n-Xv frame. The 256 members require 32 frames at a frame rate of 2 ms each. This, therefore, results in the member status being refreshed every 64 ms if there is only one return channel.

NOTE 2 – The interpretation of the member status bits according to this table is based on the 2nd multiframe value at the moment the member status word is received. In the case of VC-3/VC-4 this means that first the 2nd multiframe value is read from H4[1-4][0] and H4[1-4][1], a value between 0 and 255, and, consequently, this value is used (modulo 32) as an index for this table to identify the members of which the status is received in the H4[1-4][8] and H4[1-4][9] nibbles immediately after. This is still within the same 1st multiframe, but just in the next control packet.

11.2.1.1 High order control packet

The high order control packet consists of:

- MST (member status) field (two nibbles 1st multiframe #8 and #9);
- RS-Ack (re-sequence acknowledge) bit (bit 4 of nibble 1st multiframe #10);
- SQ (sequence indicator) field (two nibbles 1st multiframe #14 and #15);
- MFI2 (2nd multiframe indicator) (two nibbles 1st multiframe #0 and #1);
- CTRL (control) field (one nibble 1st multiframe #2);
- GID (group identification) bit (bit 4 of nibble 1st multiframe #3);
- The CRC-8 field is sent with one nibble in each of frame #6 and frame #7. (Note that in this paragraph, unless otherwise indicated, the frame numbers are those indicated by the 1st multiframe number field.) The CRC-8 field, $C_1C_2C_3C_4C_5C_6C_7C_8$ is the remainder of the CRC-8 calculation over the control packet. In the example of Table 11-2, the control packet bits are contained in H4[1-4] of the frames 8…15 of multiframe *n* and H4[1-4] of the frames 0…7 of multiframe *n* + 1 (where multiframes *n* and *n* + 1 are indicated by the 2nd multiframe indicator bits). The CRC-8 remainder is calculated as follows: The first 14 nibbles of the control packet bits represent a polynomial *M(x)* of degree 55, where H4[1] of frame 8, 2nd multiframe *n* is the most significant bit and H4[4] of frame 5, 2nd multiframe *n* + 1 is the least significant bit. *M(x)* is first multiplied by x^8 and then divided (modulo 2) by generator polynomial $G(x) = x^8 + x^2 + x + 1$ to produce a remainder *R(x)* of degree 7 or less. *R(x)* is the CRC-8 code with x^7 of *R(x)* corresponding to C_1 as the most significant bit of the remainder and x^0 of *R(x)* corresponding to C_8 as the least significant bit of the remainder;
- All other 1st multiframe nibbles (#11, #12, #13, #4 and #5) are reserved and should be set to "0000".

The high order control packet starts at 1st multiframe #8 and ends at 1st multiframe #7 in the next multiframe as shown between the heavy lines in Table 11-2.

11.3 Contiguous concatenation of X VC-2s in a higher order VC-3 (VC-2-Xc, X = 1 … 7)

A VC-2-Xc provides a payload area of X*container-2 and is represented by a C-2-X structure as shown in Figure 11-5. One common set of POH, corresponding to the POH of the first VC-2, is used for the whole VC-2-Xc (e.g., the BIP-2 covers all 428*X bytes of the VC-2-Xc). The POH positions corresponding to VC-2 #2 to VC-2 #X are fixed stuff.

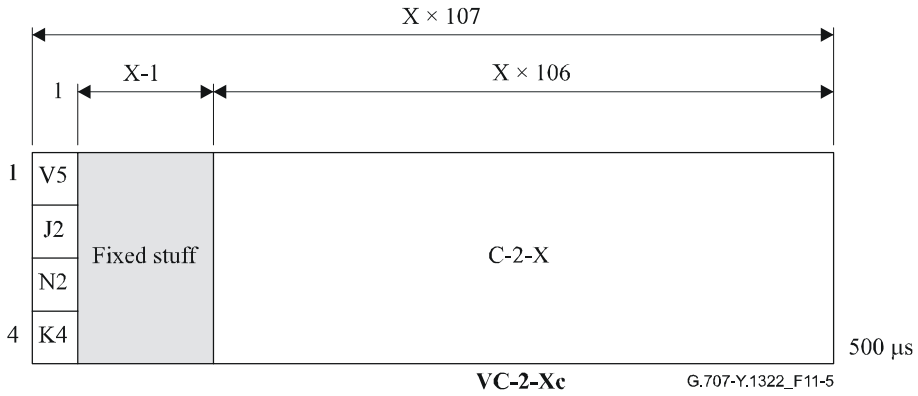


Figure 11-5 – VC-2-Xc structure

The VC-2-Xc is located in X contiguous TU-2 in a higher order VC-3. The first column of the VC-2-Xc is always located in the first TU-2. The pointer of this first TU-2 indicates the position of the V5 POH byte of the VC-2-Xc. The pointers of the TU-2 #2 to #X are set to the concatenation indication (see Figure 8-10) to indicate the contiguous concatenated payload. Pointer justification is performed in common for the X concatenated TU-2s and X stuffing bytes are used.

With allowed values of X between 1 and 7, the VC-2-Xc provides a payload capacity between 6784 kbit/s and 47 488 kbit/s in steps of 6784 kbit/s.

11.4 Virtual concatenation of X VC-11/VC-12/VC-2

A VC-11-Xv/VC-12-Xv/VC-2-Xv provides the transport capability equivalent to X*container-11/container-12/container-2, which can be represented by a C-11-X/C-12-X/C-2-X like structure and has a payload capacity of X*1600/2176/6784 kbit/s, as depicted in Figures 11-6, 11-7 and 11-8. The container is mapped in X individual VC-11s/VC-12s/VC-2s which form the VC-11-Xv/VC-12-Xv/VC-2-Xv, as illustrated in Appendix XIV. Each VC-11/VC-12/VC-2 has its own POH.

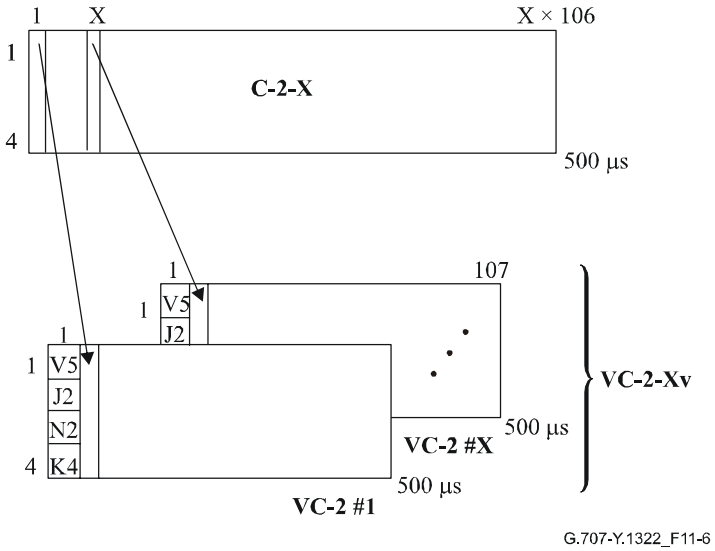


Figure 11-6 – VC-2-Xv structure

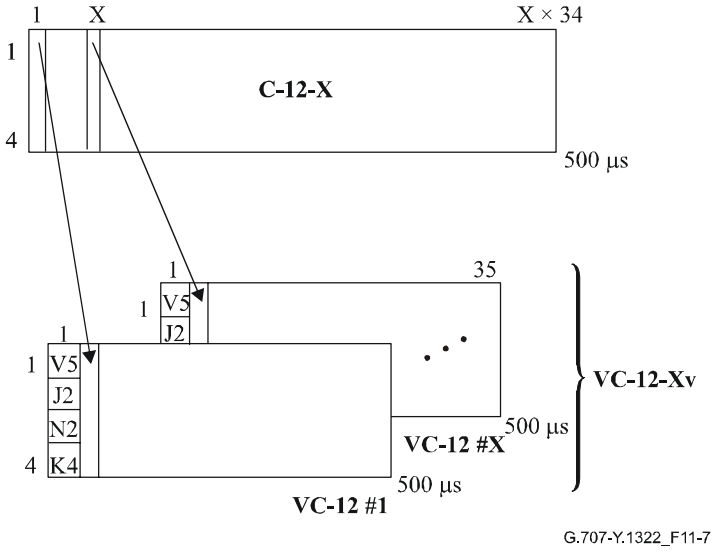


Figure 11-7 – VC-12-Xv structure

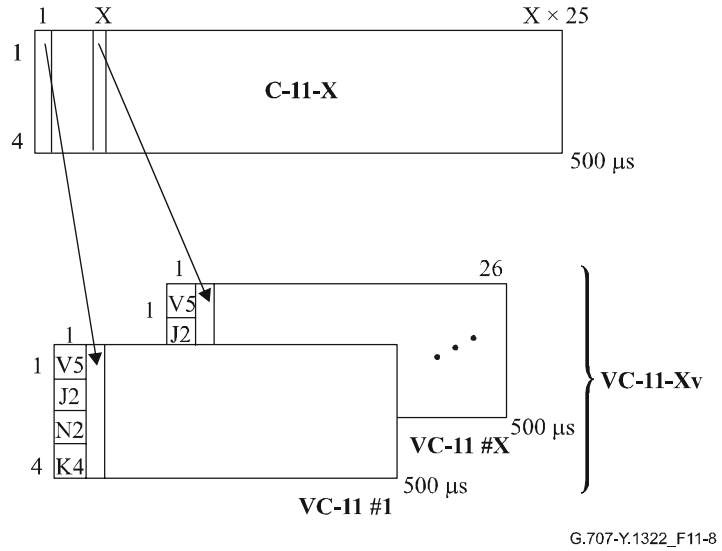


Figure 11-8 – VC-11-Xv structure

Each VC-11/VC-12/VC-2 of the VC-11-Xv/VC-12-Xv/VC-2-Xv is transported individually through the network. Due to the different propagation delays of the VC-11s/VC-12s/VC-2s, a differential delay will occur between the individual VC-11s/VC-12s/VC-2s. At the path termination, this differential delay has to be compensated and the individual VC-11s/VC-12s/VC-2s have to be realigned for access to the contiguous payload area. The realignment process has to cover at least a differential delay of 125 µs.

Payload capacities are shown in Table 11-4 for VC-11-Xv, VC-12-Xv and VC-2-Xv.

Table 11-4 – Capacity of virtually concatenated VC-11-Xv/VC-12-Xv/VC-2-Xv

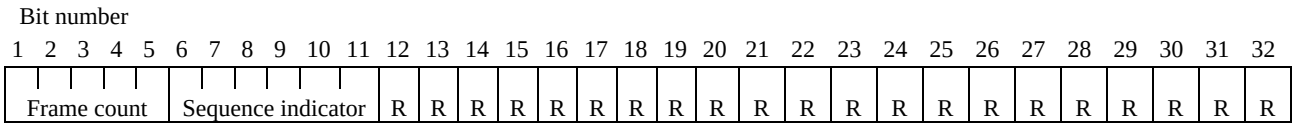
	X	Capacity	In steps of
VC-11-Xv	1 to 64 (Note)	1600 kbit/s to 102 400 kbit/s	1600 kbit/s
VC-12-Xv	1 to 64	2176 kbit/s to 139 264 kbit/s	2176 kbit/s
VC-2-Xv	1 to 64	6784 kbit/s to 434 176 kbit/s	6784 kbit/s
NOTE – Limited to 64 due to: a) six bits for sequence indicator in K4 bit 2 frame: and b) inefficient and unlikely to map more than 64 VC-11s in VC-4.			

To perform the realignment of the individual VC-ms (m = 2/12/11) that belong to a virtually concatenated group, it is necessary to:

– compensate for the differential delay experienced by the individual VC-ms;

– know the individual sequence numbers of the individual VC-ms.

Bit 2 of the K4 byte of the lower order VC-m POH is used to convey this information from the sending end to the receiving end of the virtually concatenated signal where the realignment process is performed. A serial string of 32 bits (over 32 four-frame multiframes) is arranged as in Figure 11-9. This string is repeated every 16 ms (32 bits × 500 µs/bit) or every 128 frames.



R Reserved bit

Figure 11-9 – K4 bit 2 multiframe

The LO virtual concatenation information in K4 bit 2 has a 32-bit multiframe depicted in Figure 11-9. The phase of the LO virtual concatenation information in K4 bit 2 should be the same as for the K4 bit 1 extended signal label described in clause 9.3.2.4.

NOTE – Virtually concatenated VC-11/VC-12/VC-2 must use the extended signal label. Otherwise the frame phase of the K4 bit 2 multiframe cannot be established.

The frame consists of the following fields:

The LO virtual concatenation frame count is contained in bits 1 to 5. The LO virtual concatenation sequence indicator is contained in bits 6 to 11. The remaining 21 bits are reserved for future standardization, should be set to all "0"s and should be ignored by the receiver.

The LO virtual concatenation frame count provides a measure of the differential delay up to 512 ms in 32 steps of 16 ms that is the length of the multiframe (32×16 ms = 512 ms).

The LO virtual concatenation sequence indicator identifies the sequence/order in which the individual VC-11s/VC-12s/VC-2s of the VC-11-Xv/VC-12-Xv/VC-2-Xv are combined to form the contiguous payload C-11-X/C-12-X/C-2-X as shown in Figures 11-6 to 11-8. Each VC-11/ VC-12/VC-2 of a VC-11-Xv/VC-12-Xv/VC-2-Xv has a fixed unique sequence number in the range of 0 to (X–1).

The VC-11 transporting the:

- data from cols 1, X+1, 2X+1, ….25X+1 of the C-11-X like structure has the sequence number 0;
- data from cols 2, X+2, 2X+2, … 25X+2 of the C-11-X like structure has the sequence number 1;

and so on up to the VC-11 transporting the:

- data from cols X, X+X, 2X+X, … 25X+X of the C-11-X like structure has the sequence number (X–1).

The VC-12 transporting the:

- data from cols 1, X+1, 2X+1, … 34X+1 of the C-12-X like structure has the sequence number 0;
- data from cols 2, X+2, 2X+2, … 34X+2 of the C-12-X like structure has the sequence number 1;

and so on up to the VC-12 transporting the:

- data from cols X, X+X, 2X+X, … 34X+X of the C-12-X like structure has the sequence number (X–1).

The VC-2 transporting the:

- data from cols 1, X+1, 2X+1, … 106X+1 of the C-2-X like structure has the sequence number 0;
- data from cols 2, X+2, 2X+2, … 106X+2 of the C-2-X like structure has the sequence number 1;

and so on up to the VC-2 transporting the:

- data from cols X, X+X, 2X+X, … 106X+X of the C-2-X like structure has the sequence number (X–1).

For applications requiring fixed bandwidth, the sequence number is fixed assigned and not configurable. This allows the constitution of the VC-11-Xv/VC-12-Xv/VC-2-Xv to be checked without using the trace.

11.4.1 Lower order LCAS, VC-m-Xv (m = 11, 12, 2)

Figure 11-10 depicts the modified K4[2] LO virtual concatenation multiframe, as defined in clause 11.4, indicating the control codes used for the support of LO LCAS. See also ITU-T Rec. G.7042/Y.1305.

– Frame count: The multiframe counter [0-31].

– Sequence indicator: Number to identify each member in the VCG [0-63].

– CTRL: LCAS control field, see Table 1/G.7042/Y.1305.

– GID: Group identification bit.

– Member status: The status report of the individual members uses the MST-multiframe as shown in Table 11-5. The status of all members (64) is transferred in 128 ms.

– RS-Ack: Re-Sequence Acknowledge bit.

– CRC: Three-bit CRC check for fast acceptance of virtual concatenation overhead. With this CRC-3 the probability of an undetected error in a signal with an average BER of 5.32×10^{-9}, is 4×10^{-30}. The CRC generator polynomial is $x^3 + x + 1$.

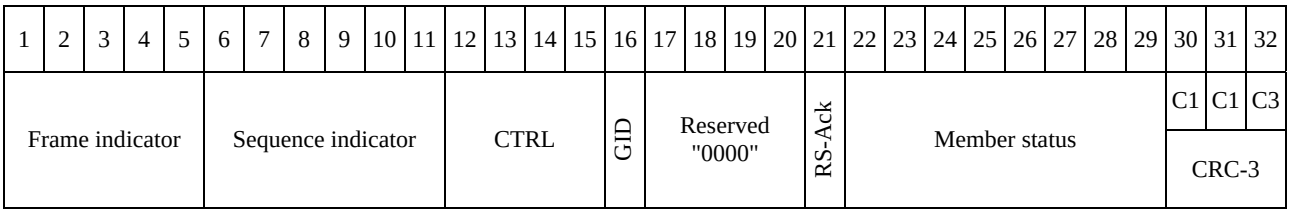


Figure 11-10 – K4[2] VC-m-Xv supporting LCAS coding

Table 11-5 – LO LCAS VC-m-Xv frame-to-member number relation

Frame number	Member number								
0, 8, 16, 24	0	1	2	3	4	5	6	7	MST-multiframe
1, 9, 17, 25	8	9	10	11	12	13	14	15	
2, 10, 18, 26	16	17	18	19	20	21	22	23	
3, 11, 19, 27	24	25	26	27	28	29	30	31	
4, 12, 20, 28	32	33	34	35	36	37	38	39	
5, 13, 21, 29	40	41	42	43	44	45	46	47	
6, 14, 22, 30	48	49	50	51	52	53	54	55	
7, 15, 23, 31	56	57	58	59	60	61	62	63	
NOTE – There are eight member statuses reported per VC-m-Xv frame. The 64 members require eight frames at a frame rate of 16 ms each. This thus results in the member status being refreshed every 128 ms if there is only one return channel.									

11.4.1.1 Lower order control packet

The lower order control packet consists of:

- Multiframe indicator (MFI) (five bits: 1 to 5);
- Sequence indicator (SQ) field (six bits: 6 to 11);
- CTRL (control) field (four bits: 12 to 15);
- GID (group identification) bit (one bit: 16);
- RS-Ack (re-sequence acknowledge) bit (one bit: 21);
- Member status (MST) field (eight bits: 22 to 29);
- CRC-3 field (three bits: 30 to 32), $C_1C_2C_3$, is the remainder of the CRC-3 calculation over the K4[2] bits 1…32. To calculate the CRC, we regard control packet bits 1-29 as a polynomial *M(x)* where K4[2] of frame 1 is the most significant bit and K4[2] of frame 29 is the least significant bit of *M(x)*. *M(x)* is first multiplied by x^3 and then divided (modulo 2) by generator polynomial $G(x) = x^3 + x + 1$ to produce a remainder *R(x)* of degree 2 or less. *R(x)* is the CRC-3 code with x^2 of *R(x)* corresponding to C_1 as the most significant bit of the remainder and x^0 of *R(x)* corresponding to C_3 as the least significant bit of the remainder;
- All other bits (#17, #18, #19 and #20) are reserved and should be set to '0'.

The lower order control packet starts and stops at the same frames as the original multiframe (see Figure 11-10).

Annex A

Forward error correction for STM-64, and STM-256

(This annex forms an integral part of this Recommendation)

A.1 Network reference model

The network reference model for in-band FEC has the following characteristics:

a) Conceptually, the FEC falls below the MS layer and provides a "correction service" to the MS layer. Correction at intermediate regenerators is possible.

b) FEC covers and provides correction for the AUG-N area, all MSOH bytes and the FSI byte located in the RSOH.

c) The FEC uses overhead bytes from the MSOH and RSOH. Regenerators have to pass through the FEC-related RSOH bytes.

d) The FEC insertion function shall compensate B2 appropriately to reflect the changes in the FEC MSOH bytes. The FEC parity covers the compensated B2 bytes.

e) The MS layer signal degrade and other performance monitoring functions based on B2 apply to the corrected data; they are thus appropriate for service-related performance measurements (e.g., as used for protection switching), but give no information about the raw performance of the line.

f) FEC performance monitoring functions can provide information about the condition of the raw performance of the multiplex section. Use of in-band FEC performance monitoring is for further study.

A.2 The FEC function

A.2.1 Code type and parameters

The code is a shortened, systematic binary-BCH code derived from a (8191, 8152) parent code. Sufficient parity bits are generated to support triple error correction.

The block size is 1 row (bit-slice) of the STM-N (see Figure A.1) ordered in $8 \times N/16$ rows, i.e., $k = 4320$ information bits plus 39 parity bits per block, i.e., $n = 4359$. The minimum code distance = 7, i.e., number of correctable errors, $t = 3$.

A.2.2 FEC encoder description and algorithm

The generator polynomial used is $G(x) = G1(x) \times G3(x) \times G5(x)$ where:

$$G1(x) = x^{13} + x^4 + x^3 + x + 1$$

$$G3(x) = x^{13} + x^{10} + x^9 + x^7 + x^5 + x^4 + 1$$

$$G5(x) = x^{13} + x^{11} + x^8 + x^7 + x^4 + x + 1$$

FEC encoding operates on a row-by-row basis. The code word is represented by the polynomial

$$C(x) = I(x) + R(x)$$

where:

$I(x) = a_{4358}x^{4358} + \ldots + a_{39}x^{39}$ where a_n ($n = 4358$ to 39) represents the information bits

and

$R(x) = a_{38}x^{38} + \ldots + a_0$ where a_n ($n = 38$ to 0) represents the parity bits

The first bit of the overhead in each code block is the first bit of the code word and is the coefficient a_{4358} of x^{4358}. The information bits not covered (see clause A.2.5) in the FEC calculations are replaced with zeros in the FEC encoder and decoder.

Since this is a systematic code, the parity bits R(x) are provided by:

$$R(x) = I(x) \bmod G(x)$$

A.2.3 Encoder and decoder locations

The encoder is always located at the transmitter side of the equipment that terminates MSOH.

There is always a decoder at the input of an in-band FEC-compliant equipment that terminates MSOH. Optionally, a regenerator equipment can decode (correct), but shall not re-encode.

A.2.4 FEC delay characteristic

The decode delay is no more than 15 µs wherever encountered. Equipment compliant with this standard shall have a FEC processing delay of no more than 15 µs. In the case of in-band FEC being supported each correcting regenerator equipment adds no more than 15 µs delay.

A.2.5 SDH and FEC check bits not included in FEC coding

The bits and bytes that are not included in the coding of the FEC are:

– All RSOH bytes including undefined RSOH bytes but not the Q1 bytes.

– All FEC parity bits.

NOTE – Although parity bits R(x) of each code-word are transported in information bits I(x) positions they are not included in I(x); they form the R(x) part of the code-word C(x). As such the R(x) can be corrected. Intermediate regenerators correcting I(x) errors must correct errors within the parity R(x). At MS terminating points, correction of errors within the parity bits R(x) is not necessary.

A.3 Mapping into the SDH frame

To minimize delay relative to maintaining RSOH/MSOH layer integrity, MSOH and RSOH for FEC parity bits are used to limit delay to 30 µs per encoder/decoder.

Figures 9-5, 9-6 and 9-7 give the allocation of P1 and Q1 parity and status bytes for STM-N, (N = 64, 256), signals.

A.3.1 Location of the information bits

Each of the 9 rows of an STM-N (N = 64, 256) is considered equal and independent. There is no difference between the SOH and AUG-N regarding the information bits I(x).

One row K of the STM-N frame is shown in Figure A.1. The transmission order is column by column. The row is divided such that every 8 × N/16 bit forms one bit-slice. The FEC information bits a_n (n = 4358 … 39) are located in the positions shown in the figure. Each subrow forms one information word I(x) of the FEC function.

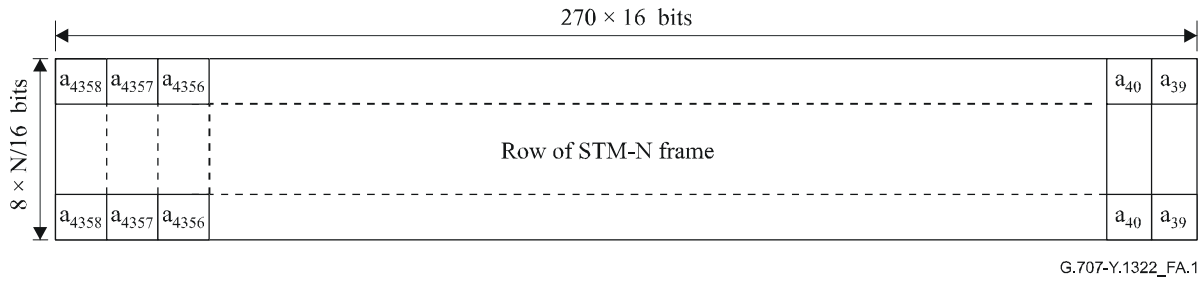


Figure A.1 – FEC information bits in row K of STM-N frame

NOTE – Some of the FEC information bits a_n are set to zero for the calculation of the parity R(x), see clause A.2.5.

The 8-way bit interleaving in conjunction with BCH-3 provides 24-bit burst error correction capability per row for STM-64 and STM-256.

A.3.2 Location of in-band FEC parity

The P1 bytes are allocated for FEC parity. There is one parity bits set a_n, (n = 0…38), for every subrow in Figure A.1 of an STM-N, i.e., $8 \times N/16$ sets. The FEC parity bit a_n, (n = 0…38), for row K is located in SOH byte:

S (x, y, $M \times 16 - n + 13 \times$ Int [n/13]);

where x, y for STM-N row K and parity bit n is obtained from Table A.1, and

M = 1,2,3,4 for STM-64

M = 1,2, …, 16 for STM-256

Table A.1 – x, y values for location of FEC parity a_n for row K

Row K	(x, y) for a_n $26 \leq n \leq 38$	(x, y) for a_n $13 \leq n \leq 25$	(x, y) for a_n $n \leq 12$
1	2,1	2,4	2,6
2	3,1	3,4	3,6
3	3,7	3,8	3,9
4	5,4	5,5	5,6
5	5,7	5,8	5,9
6	6,7	6,8	6,9
7	7,7	7,8	7,9
8	8,7	8,8	8,9
9	9,1	9,2	9,3
NOTE – The FEC parity R(x) is not necessarily located in the same row as its information bits.			

A.3.3 Location of status/control bits

The FEC FSI carrying byte is located in the first Q1 byte S (3,9,3).

FSI is a FEC status indicator. This is used at the FEC decoding point to determine whether FEC information is present to allow error correction to take place. The location of the FSI bits within the FSI byte is given in Figure A.2.

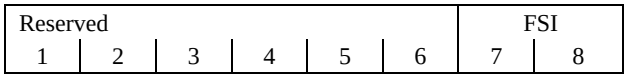


Figure A.2 – Q1 byte S (3,9,3)

A.3.4 FEC status indication (FSI)

The FEC encoder is required to generate the FEC status indication (FSI) bits to enable downstream decoders. This is to prevent downstream decoders from causing errors by miscorrection when FEC encoding is not present.

The FSI bits are bits 7 and 8 of the FSI byte, see Figure A.2. The remaining bits in the FSI bytes are reserved, but are covered by the FEC. The transmitted default value for these remaining 6 bits shall be zero. The FSI bits (7 and 8) are checked prior to FEC decoding, but the entire FSI byte is included in the FEC block for correction before retransmission by correcting regenerators. The FSI bit coding is defined in clause A.6.2.

A.3.5 B1 calculation at encoder and decoder

B1 is calculated according to clause 9.2.2.4. The FEC check bytes and FSI byte in the SOH are included in the B1 calculation.

The B1 bit errors are calculated before the FEC based on the uncorrected signal. B1 calculation gives error performance of each regenerator section before error correction.

A.3.6 B2 calculation at encoder and decoder

B2 is calculated according to clause 9.2.2.10. The FEC code bytes and FSI byte in the RSOH are not included in the B2 calculation. The FEC parity bytes in the MSOH are included in the B2 calculation. In other words, the B2 has to be compensated to include the FEC parity bytes accordingly in order to show the correct B2 parity.

NOTE – The FEC coding is performed over the compensated B2 parity.

The B2 bit errors are calculated after the FEC decoding based on the corrected signal and B2 bytes.

A.4 In-band FEC regenerator functions

A.4.1 Regenerators not supporting in-band FEC

Regenerator equipment developed prior to the adoption of FEC in this revision of this Recommendation may not transparently pass through the P1 and Q1 bytes. If this information is blocked through older regenerator equipment, downstream equipment will not attempt correction as a result of not receiving the expected FSI byte value.

A.4.2 Regenerators passing in-band FEC transparently without error correction

Regenerator equipment that permits in-band FEC but does not perform error correction shall pass through P1 and Q1 bytes unaltered.

A.4.3 Regenerators with error correction

Optionally, regenerator equipment can perform FEC decoding and correction without re-encoding. The corrected FEC parity bits plus FSI byte are forwarded.

A.5 Performance monitoring

A.5.1 FEC correctable error count

Correctable errors are those that are detected and corrected.

Raw MS layer BER can be calculated with the aid of FEC correction counts. If error correction is performed, then the FEC correctable error count reflects the raw BER from the last decoding point.

A.5.2 FEC uncorrectable error count

Uncorrectable errors are those that are detected but not corrected. The use of this is for further study.

A.5.3 Error count after FEC decoding

B2 is used to calculate the error count after the FEC decoding at an MS termination point or non-intrusive monitor.

A.6 FEC activation and deactivation

A.6.1 FEC operational states

A.6.1.1 Encoder states

There are three operational states:

a) FEC on;

b) FEC off with encoder delay;

c) FEC off without encoder delay.

The management layer controls the encoder operational state. Transitions to/from state c affect data path delay and will not be hitless.

A.6.1.2 Decoder states

There are three operational states:

a) FEC correction enabled;

b) FEC correction off with decoder delay;

c) FEC correction off without decoder delay.

The state transitions to/from state c is solely under management layer control and affects data path delay. Therefore, this transition is not hitless. State transitions between state a and state b are controlled by the received FSI.

A.6.2 FEC status indication (FSI)

A.6.2.1 FSI interaction with decoder states

Decoder state a can only be entered with received FSI "on" condition. If operating in decoder state a and FSI "off" is received then the decoder shall enter state b. The transitions between state a and state b shall occur in a hitless manner.

A.6.2.2 FEC on/off state indication generation at transmitter

When the encoder is in state a, FSI = 01 is transmitted. When the encoder is in state b or in state c, FSI = 00. FSI = 10 and 11 are not valid encoder transmission values.

In order to permit synchronized decoder switching at the receiver, the FSI is changed from 01 to 00 or (00 to 01) seven frames before the encoder is switched off (on). The encoder is turned off (on) starting with the first row of the 8th frame after the FSI change.

A.6.2.3 FEC on/off state detection at receiver

FSI On→Off transition is detected upon receipt of the 3rd consecutive non-01. FSI Off→On transition is detected upon receipt of the 9th consecutive "on" value of 01. This allows the decoder to implement an automatic on/off switch while building in robustness against erroneously performing decoding (and corrupting bits) when the encoder is off.

A.6.3 MS-AIS interaction with FEC

An MS layer termination point is required to monitor for MSF-AIS prior to FEC corrections. If MSF-AIS is detected, FEC corrections should be disabled no later than the beginning of the following frame after MSF-AIS detection.

A regenerator that performs corrections is required to monitor for MSF-AIS prior to corrections. If MSF-AIS is detected, FEC corrections should be disabled no later than the beginning of the following frame after MSF-AIS detection.

Once the MSF-AIS defect is cleared, the FEC corrections should resume no later than the following frame after the clearing of MSF-AIS, assuming that the FSI is in the correction state.

Regenerator section defects that corrupt FEC parity bits (e.g., LOS and LOF) shall disable FEC corrections. Regenerator section defects that do not corrupt FEC parity bits (e.g., J0 mismatch) shall not disable FEC corrections.

A.7 Performance of in-band FEC

The performance of the in-band FEC is discussed in Appendix X.

Annex B

CRC-7 polynomial algorithm

(This annex forms an integral part of this Recommendation)

B.1 Multiplication/division process

A particular CRC-7 word is the remainder after multiplication by X^7 and then division (modulo 2) by the generator polynomial $X^7 + X^3 + 1$, of the polynomial representation of the previous trail trace identifier multiframe (TTI).

When representing the contents of the block as a polynomial, the first bit in the block, i.e., byte 1 bit 1 should be taken as being the most significant bit. Similarly, C_1 is defined to be the most significant bit of the remainder and C_7 the least significant bit of the remainder.

B.2 Encoding procedure

Contrary to example CRC-4 procedure in 2 Mbit/s signals, the CRC-7 word is static because the data is static (the TTI represents the source address). This means that the CRC-7 checksum can be calculated *a priori* over the TTI multiframe. For consistency with existing Recommendations, the CRC-7 checksum is to be calculated over the previous multiframe. In theory, this means that the 16-byte string that is loaded in a device for repetition transmission should have the checksum as the last byte although, in practice, it does not really matter because the TTI is static.

The encoding procedure is as follows:

i) The CRC-7 bits in the TTI are replaced by binary 0s.

ii) The TTI is then acted upon by the multiplication/division process referred to in clause B.1.

iii) The remainder resulting from the multiplication/division process is inserted into the CRC-7 location.

The CRC-7 bits generated do not affect the result of the multiplication/division process because, as indicated in i above, the CRC-7 bit positions are initially set to 0 during the multiplication/division process.

B.3 Decoding procedure

The decoding procedure is as follows:

i) A received TTI is acted upon by the multiplication/division process referred to in clause B.1 after having its CRC-7 bits extracted and replaced by 0s.

ii) The remainder resulting from the division process is then compared on a bit-by-bit basis with the CRC-7 bits received.

iii) If the remainder calculated in the decoder exactly corresponds to the CRC-7 bits received, it is assumed that the checked TTI is error free.

Annex C

VC-4-Xc/VC-4/VC-3 tandem connection monitoring protocol: Option 1

(This annex forms an integral part of this Recommendation)

This annex describes the tandem connection overhead layer for SDH. The tandem connection sublayer is an optional sublayer which falls between the multiplex section and path layers defined in this Recommendation. This overhead sublayer deals with the reliable transport of path layer payload and its overhead across a network. The use of tandem connection is application-specific and at the discretion of the carrier. It is expected that the principal applications for tandem connection will be in the inter-office network and that tandem connections will generally not be used in applications such as the subscriber access network.

NOTE – The TC monitoring may have an unexpected dependence to the incoming signal. See Appendix VIII for a description of the problem.

C.1 Tandem connection overhead – Byte location

The N1 byte in the path overhead in each HOVC of the tandem connection is defined as tandem connection overhead (TCOH). Bits 1-4 of this byte in each HOVC of the tandem connection are used to provide a tandem connection incoming error count (IEC), which is defined below. The remaining four bits in byte N1 of the first VC-n within the tandem connection are used to provide an end-to-end data link.

NOTE – Applications currently under consideration may require some LAPD messages generated before the originating TCTE to be transferred through the tandem connection data link. This is for further study.

Figure C.1 shows the tandem connection overheads for an STM-1 rate tandem connection made up of a bundle of 3 VC-3 HO paths.

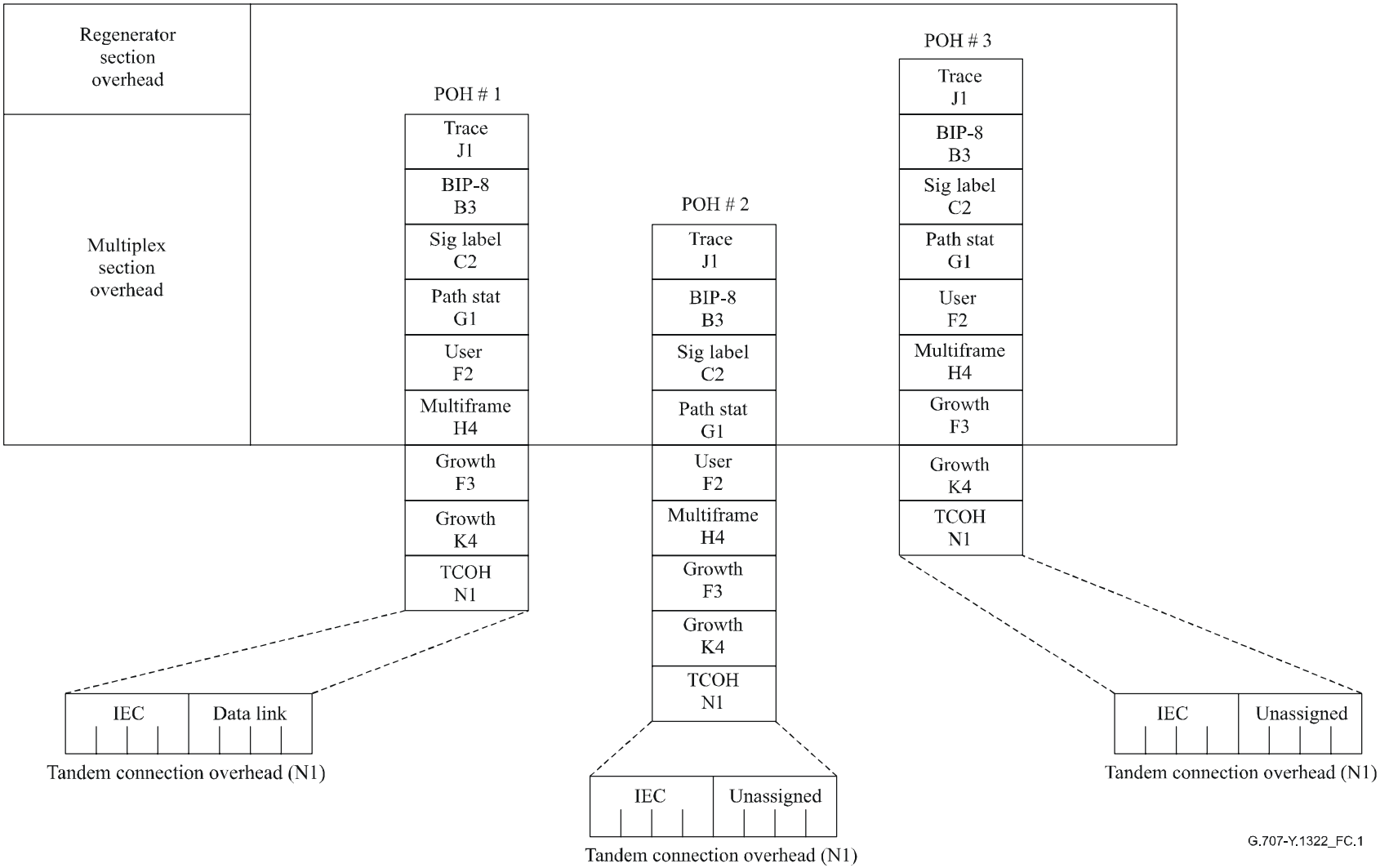


Figure C.1 – Tandem connection overhead in STM-1 rate (AU-3 based) tandem connection

C.2 Definitions

C.2.1 tandem connection (TC): A tandem connection is defined as a group of higher order VC-ns which are transported and maintained together through one or more tandem line systems, with the constituent HOVC payload capacities unaltered. Note that, in support of the layered overhead approach used in SDH, the tandem connection sublayer falls between the multiplex section and path overhead layers (i.e., the original regenerator section, multiplex section and path functional overhead layering evolves to regenerator section, multiplex section, tandem connection and path layers).

C.2.2 tandem connection terminating element (TCTE): The element which originates/terminates the tandem connection. A multiplex section terminating element (MSTE) or a path terminating element (PTE) may also be a TCTE.

C.3 Tandem connection bundling

Tandem connection maintenance may be performed on a single higher order VC-n or on a bundle with a capacity of N STM-1s where N is any of the allowed SDH hierarchy levels defined in clause 6.3. The size of bundles supported is application-specific and an equipment issue. The following clause describes how tandem connection bundling is achieved.

C.3.1 Bundling of VC-3s within an STM-1

The bytes from bundled VC-3s within an STM-1 shall be contiguous at the STM-1 level, but are not contiguous when interleaved to higher levels. The first VC-n of the bundle shall contain the tandem connection data link.

Figure C.2 illustrates this for a tandem connection at the STM-1 rate.

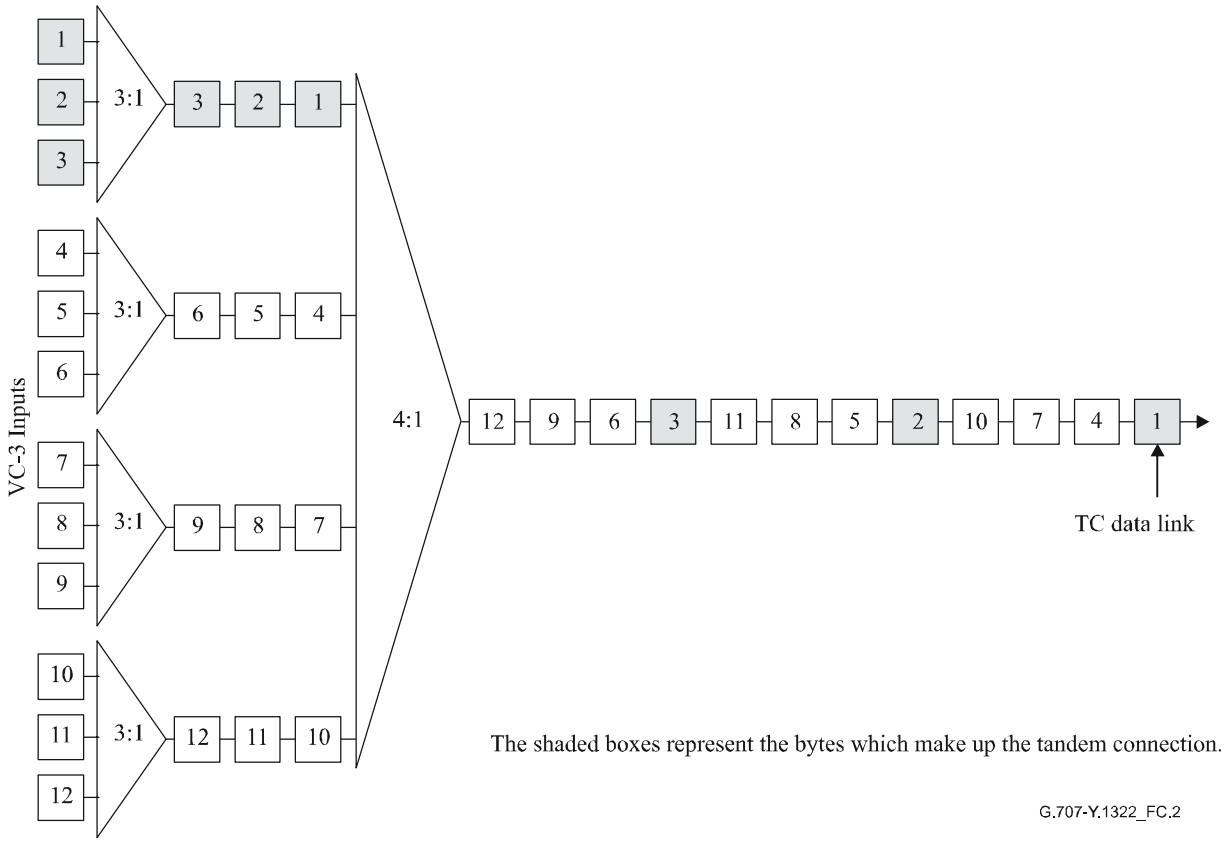


Figure C.2 – Example of an STM-1 rate tandem connection within an STM-N

C.3.2 Bundling of VC-3s within an STM-N (N>1)

Bundles of VC-3s within an STM-N (N is any of the allowed SDH hierarchy levels defined in clause 6.3) consist of multiples of STM-1s. The bytes from the constituent STM-1s shall be contiguous. The first HOVC of the tandem connection shall contain the tandem connection data link.

C.3.3 Tandem connection bundle contents

A tandem connection bundle at the STM-N rate (N is any of the allowed SDH hierarchy levels defined in clause 6.3) may carry $3 \times N$ VC-3s or combinations of VC-4-Mcs ($M \leq N$; $M = 1, 4, 16$) including one VC-4-Xc as per the concatenation mechanism defined in clause 8.1.7 (e.g., an STM-4 tandem connection could carry 12 VC-3s, or 4 VC-4s, or one VC-4-4c, or 2 VC-4s and 6 VC-3s, etc.). Note that a VC-4-Mc shall be contained wholly within a single tandem connection.

Figure C.3 illustrates this for an STM-4 rate tandem connection made up of four VC-4s.

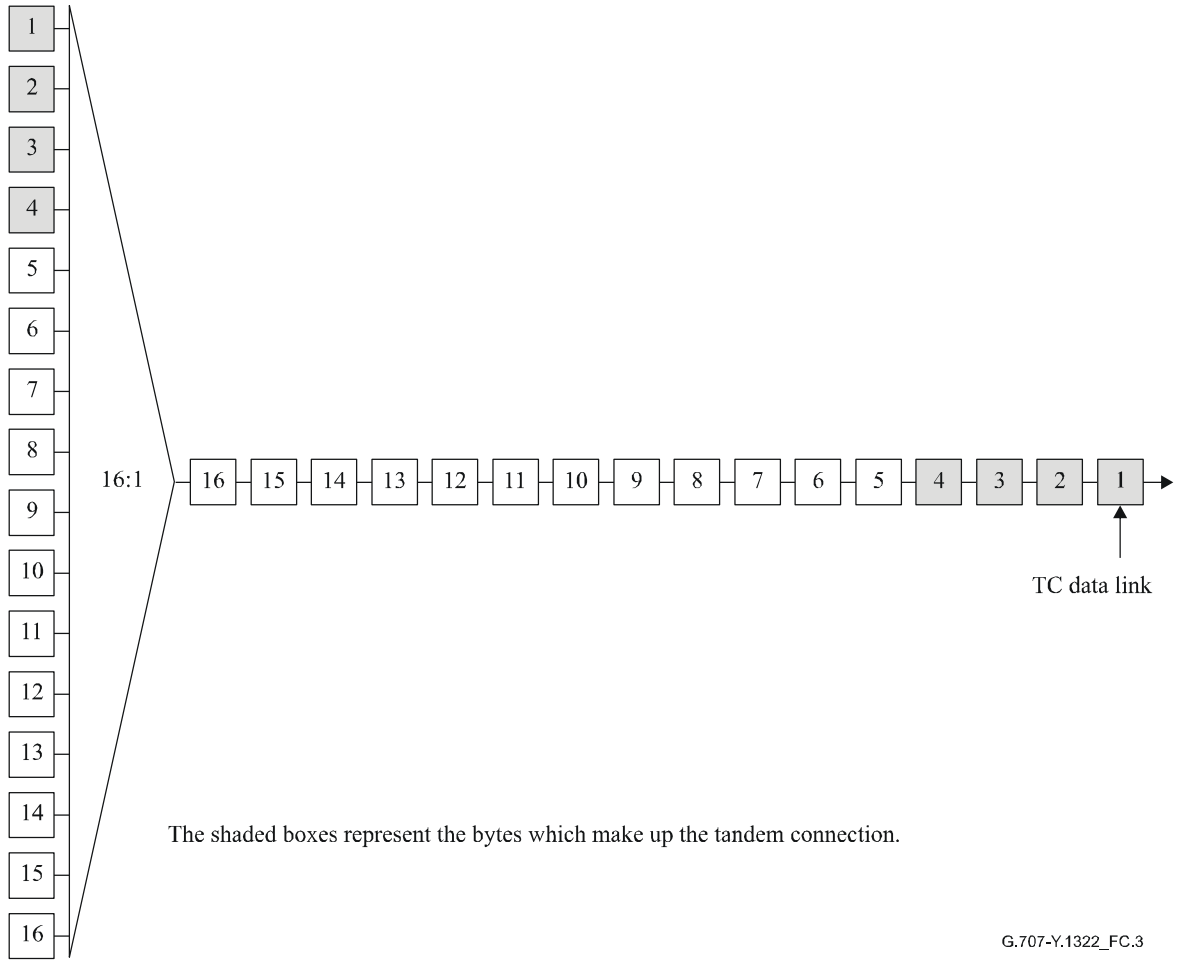


Figure C.3 – Example of an STM-4 rate tandem connection within an STM-16

C.3.4 Tandem connection bundles in higher rate signals

A bundle of HOVCs forming a tandem connection may be multiplexed into a higher rate STM-N as per the multiplexing procedure defined in this Recommendation.

C.4 Incoming error count (IEC)

In order to continually assess the tandem connection signal quality, the B3 bytes in the VC-n overhead of each of the HOVCs that make up the tandem connection signal are used to determine

the number of errors which have accumulated in the tandem connection. In order to account for any errors that may be present in a VC-n at the originating end of the tandem connection, the number of errors detected in the incoming VC-n at the originating end of the tandem connection is written into bits 1-4 of byte N1 in the next frame using the coding given in Table C.1. This procedure is carried out for each of the VC-ns that make up the tandem connection.

The tandem connection signal may then be carried through the network by STM-M SDH line system (of equal or higher transport rate), or number of SDH line systems in tandem where the tandem connection is made at the tandem connection, or higher, level (e.g., a VC-3 tandem connection may be cross-connected at the VC-3 rate or higher, and a TCB at the STM-4 rate may be cross-connected at the STM-4 rate or higher). At the terminating TCTE (far end of the tandem connection), the B3 byte in each of the constituent HOVCs is again used to calculate the number of errors which have accumulated. The magnitude (absolute value) of the difference between this calculated number of errors and the number of errors written into the IEC at the originating end is then used to determine the error performance of the tandem connection for each transmitted SDH frame. The IEC field is interpreted according to Table C.2. Note that the B3 byte data and the IEC read in the current frame both apply to the previous frame.

On the outgoing side of the terminating TCTE, the IEC (first four bits of N1 byte) of all constituent HOVCs shall be set to all 0s. As a default, the tandem connection data link (last four bits of N1 in the first HOVC) shall be set to all 0s.

NOTE – Applications currently under consideration may require some messages in the tandem connection data link to be forwarded on beyond the terminating TCTE. This is for further study.

The unassigned bits (last four bits in the remaining Z5 bytes) shall be passed through unaltered. B3 shall then be compensated as defined in clause C.5.

Table C.1 – IEC coding

b1	b2	b3	b4	Number of BIP-8 violations
1	0	0	1	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	1	1	0	Incoming AIS

NOTE – To guarantee a non-all-zeroes N1 byte independent of the incoming signal status, it is required that the IEC code field contains at least one "1". When zero errors in the BIP-8 of the incoming signal are detected, then an IEC code is inserted with "1"s in it. In this manner it is possible for the tandem connection sink at the tail end of the tandem connection link to use the IEC code field to distinguish between unequipped conditions started within or before the tandem connection.

Table C.2 – IEC code interpretation

b1	b2	b3	b4	IEC code interpretation
0	0	0	0	0 BIP violation
0	0	0	1	1 BIP violation
0	0	1	0	2 BIP violations
0	0	1	1	3 BIP violations
0	1	0	0	4 BIP violations
0	1	0	1	5 BIP violations
0	1	1	0	6 BIP violations
0	1	1	1	7 BIP violations
1	0	0	0	8 BIP violations
1	0	0	1	0 BIP violation
1	0	1	0	0 BIP violation
1	0	1	1	0 BIP violation
1	1	0	0	0 BIP violation
1	1	0	1	0 BIP violation
1	1	1	0	0 BIP violation, Incoming AIS
1	1	1	1	0 BIP violation

C.5 B3 compensation

Since the B3 parity check is taken over the VC-n payload and path overhead (including N1), writing into N1 at the originating TCTE will affect the path parity calculation. Unless this is compensated for, a device which monitors path parity within the tandem connection (e.g., a bridging monitor) may incorrectly count errors. The B3 parity byte should always be consistent with the current state of the VC-n. Therefore, whenever N1 is written, B3 shall be modified to compensate for the change in the N1 value. Since the B3 value in a given frame reflects a parity check over the previous frame (including the B3 byte in that frame), the changes made to the B3 byte in the previous frame shall also be considered in the compensation of B3 for the current frame. Therefore, the following equation shall be used for B3 compensation:

$$B3'(t) = B3(t-1) \oplus B3'(t-1) \oplus N1(t-1) \oplus N1'(t-1) \oplus B3(t)$$

where:

B3 the existing B3 value in the incoming signal

B3' the new (compensated) B3 value

N1 the existing N1 value in the incoming signal

N1' the new value written into the N1 byte (IEC plus data link at the originating TCTE, or all 0s at the terminating TCTE)

$\oplus$ exclusive OR operator

t the time of the current frame

t–1 the time of the previous frame

C.6 Data link

Bits 5-8 of the N1 byte in the first VC-n of the tandem connection are designated as a 32 kbit/s tandem connection data link. The remaining four bits in byte N1 of the remaining VC-ns are unassigned and must not be altered by the TCTE. The signal format used on the tandem connection data link is comprised of messages that use a subset of the LAPD protocol (unnumbered, unacknowledged frame).

NOTE – If future applications require LAPD messages generated and terminated outside the tandem connection to be transferred through the tandem connection data link, the above statement does not require that these messages also be unnumbered and unacknowledged.

When these LAPD messages are not being transmitted (i.e., the data link is idle), LAPD flags (01111110) shall be continuously transmitted.

Currently, four messages are defined below to support tandem connection maintenance:

- tandem connection trace;
- tandem connection idle signal ID;
- tandem connection test signal ID;
- tandem connection far end one-second performance report message.

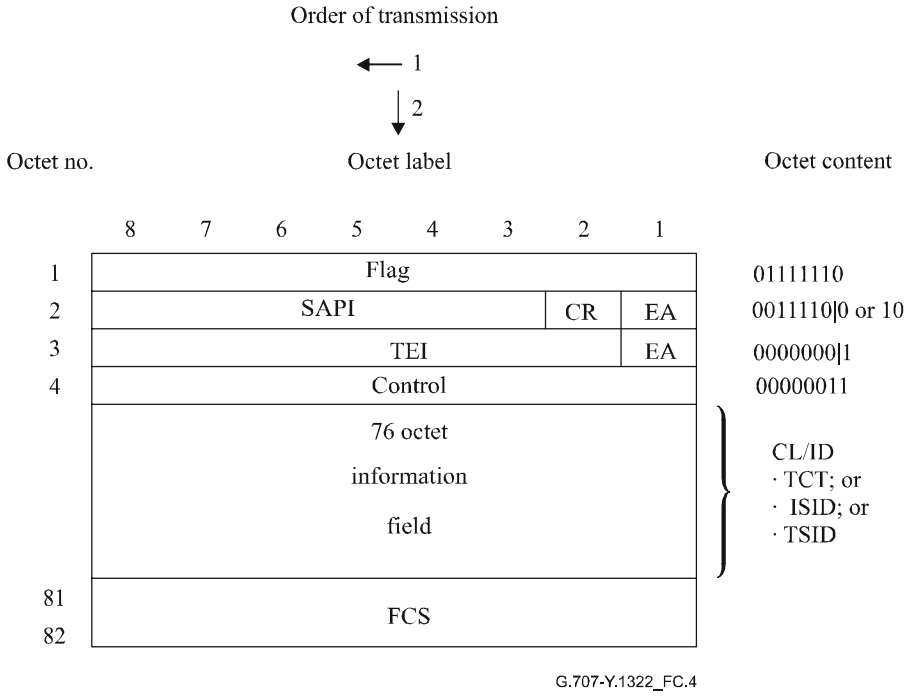
In practice, the tandem connection trace, idle signal ID or test signal ID message is transmitted continuously at a minimum rate of once per second. The tandem connection far end one-second performance report message is transmitted continuously at a rate of once per second.

Operation, administration and maintenance of the network may cause messages, other than those defined above, to appear on the tandem connection data link. Network terminal and monitoring equipment should be able to disregard any such undefined messages. Such undefined message use must not interfere with the transmission of the messages defined in this Recommendation. Use of the tandem connection data link for other terminal-to-terminal messages beyond the described set is for future study.

C.6.1 Format of the LAPD messages

The format of the LAPD messages uses a subset of the full Q.921/LAPD capabilities. The message structure is shown in Figure C.4. This message structure is that of a Q.921/LAPD, unnumbered and unacknowledged frame. The source of the LAPD messages shall generate the FCS and the zero stuffing required for transparency. Zero stuffing by a transmitter prevents the occurrence of the flag pattern (01111110) in the bits between the opening and closing flags of a Q.921/LAPD frame by inserting a zero after any sequence of five consecutive ones. A receiver removes a zero following five consecutive ones.

There is no requirement for the boundaries of the LAPD octets and the N1 byte to coincide. The bits of the LAPD octet shall be transmitted in the order shown in Figure C.4, within the N1 byte. Thus, bits n, n + 1, n + 2 and n + 3 of an arbitrary LAPD octet would be loaded into bits 5, 6, 7 and 8, respectively, of the N1 byte.



Flag	Interpretation
01111110	Interframe fill octet sequence

SAPI|CR|EA	Interpretation
00111100	SAPI=15, CR=0 (DTE), EA=0
00111110	SAPI=15, CR=1 (Carrier), EA=0

TEI|EA	Interpretation
00000001	TEI=0, EA=1

Control	Interpretation
00000011	Unacknowledged information transfer

N octet information field	Interpretation
Path ID	Common language identifier
Idle SIG. ID	
Test SIG. ID	

FCS	Interpretation
Variable	CRC-16 frame check sequence

Figure C.4 – Q.921/LAPD message structure

C.6.2 Tandem connection trace, idle signal and test signal identification messages

The tandem connection identification messages discussed below shall be transmitted a minimum of once per second and shall use only the SAPI/TEI values shown in Figure C.4. The contents of the 76-octet information field is shown in Figure C.5 and is discussed in this clause.

Tandem connection trace

Data elements	Binary value	
TYPE	0011 1000	Connection ID
EIC	XXXX XXXX..XXXX	10 octets
LIC	XXXX XXXX..XXXX	11 octets
FIC	XXXX XXXX..XXXX	10 octets
UNIT	XXXX XXXX..XXXX	6 octets
FI	XXXX XXXX..XXXX	38 octets

Idle signal identification

Data elements	Binary value	
TYPE	0011 0100	Idle ID
EIC	XXXX XXXX..XXXX	10 octets
LIC	XXXX XXXX..XXXX	11 octets
FIC	XXXX XXXX..XXXX	10 octets
UNIT	XXXX XXXX..XXXX	6 octets
PORT No.	XXXX XXXX..XXXX	38 octets

Test signal identification

Data elements	Binary value	
TYPE	0011 0010	Test ID
EIC	XXXX XXXX..XXXX	10 octets
LIC	XXXX XXXX..XXXX	11 octets
FIC	XXXX XXXX..XXXX	10 octets
UNIT	XXXX XXXX..XXXX	6 octets
GEN No.	XXXX XXXX..XXXX	38 octets

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Figure C.5 – Tandem connection trace-idle signal and test signal identification messages

NOTE – Note that the tandem connection trace message length of 76 bytes may be changed to 64 bytes to be consistent with the SDH path trace (J1 Byte), once the content of the J1 byte message (under study) has been standardized.

The tandem connection trace (TCT), idle signal identification (ISID) and test signal identification (TSID) messages all use the same 76-octet structure made up of six data elements. Each data element, except the first, is a fixed length word made up of ASCII characters. The first data element is one byte long and defines the type of identification message being transmitted. The next four data elements identify the type of terminal equipment and the equipment location that sourced the

identification message. Finally, given that terminal equipment may source more than one tandem connection signal, the final data element identifies a specific tandem connection signal.

The first five data elements have the same meaning for all three messages, and will be defined first. The sixth data element is different for each of the messages (see Figure C.5). The data elements are designed to accommodate codes that are widely used in facility networks.

The first five data elements, common to all three identification messages, are defined as follows:

TYPE The type code is a one-octet code used to identify a particular type of identification message. Specific values are shown in Figure C.5.

EIC The equipment identification code (up to 10 characters) describes a specific piece of equipment.

LIC The location identification code (up to 11 characters) describes a specific location.

FIC The frame identification code (up to 10 characters) identifies where the equipment is located within a building at a given location.

UNIT A code (up to 6 characters) that identifies the equipment location within a bay.

The final data element for the tandem connection trace message is the facility identification code:

FI The facility identification code (up to 38 characters) identifies a specific tandem connection.

The final data element for the idle signal identification message is the port number:

PORT No. The PORT number is the designation of the equipment port that initiates the idle signal.

The final data element for the test signal identification message is the generator number:

GEN No. The number of the test signal generator that initiates the test signal.

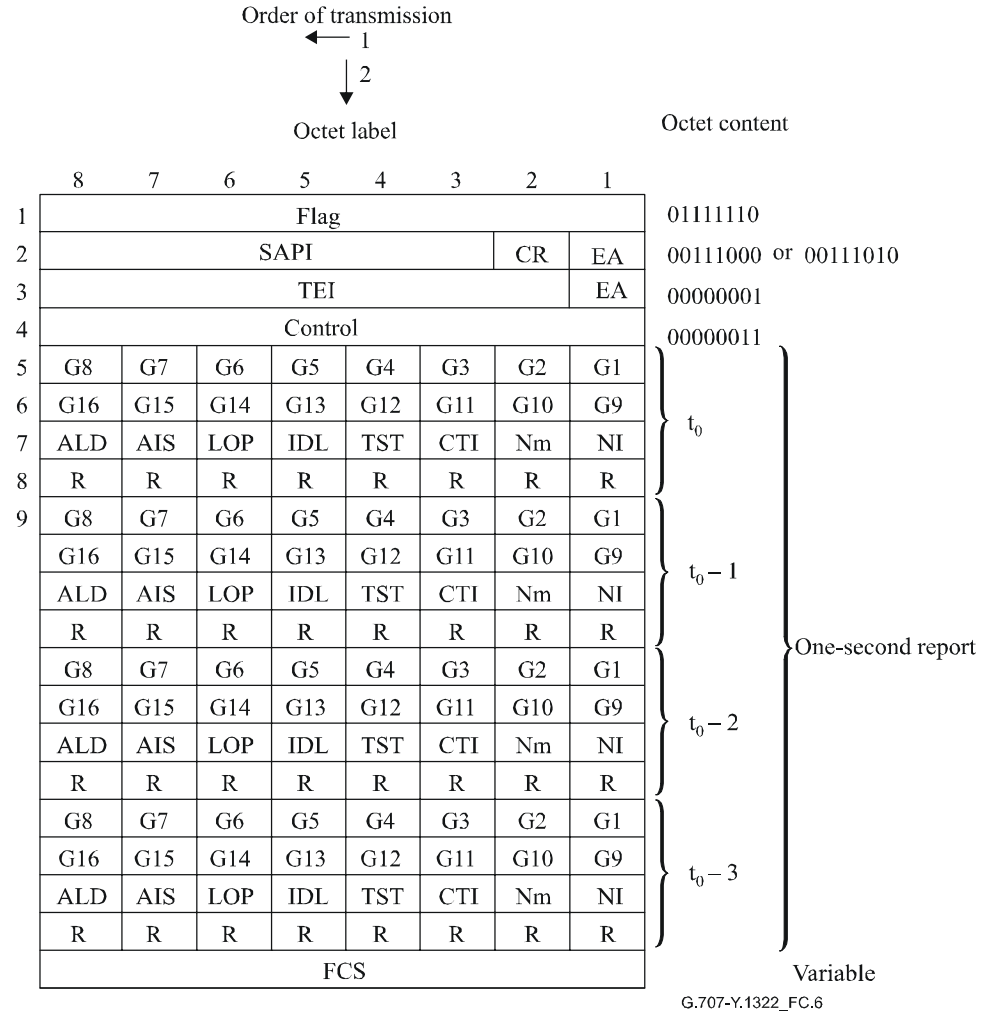
The ASCII null character shall be used to indicate the end of the string when the full length of the data element is not needed for a given word. The remaining bit positions of the data element may contain ones, zeros, or any combination of ones and zeros.

In those cases where all the data elements are not needed for a given message, the first octet of the data element shall contain the ASCII null character. The remaining bit-positions of the data element may contain ones, zeros or any combination of ones and zeros.

C.6.3 The far-end performance report message

The tandem connection far end one-second performance report message discussed below shall be transmitted once per second and shall use only the SAPI/TEI values shown in Figure C.6. The phase of the one-second report periods with respect to the occurrence of error events is arbitrary in that the one-second timing does not depend on the time of occurrence of any error event.

The performance report contains performance information for each of the four previous one-second intervals. This is illustrated in Figure C.6, octets 5 through 20, and by an example in Figure C.7. Counts of events shall be accumulated in each contiguous one-second interval. At the end of each one-second interval, a modulo-4 counter shall be incremented, and the appropriate performance bits shall be set in the t_0 octets (octets 5 through 8 in Figure C.6). These octets and the octets that carry the performance bits of the preceding three one-second intervals form the performance report message.



Address	Interpretation
00111000	SAPI=14, C/R=0 (User) EA=0
00111010	SAPI=14, C/R=1 (Carrier) EA=0
00000001	TEI=0, EA=1

Control	Interpretation
00000011	Unacknowledged information transfer

One-second report	Interpretation
G1-G8	LSB of 2-byte tandem connection error event counter
G9-G16	MSB of 2-byte tandem connection error event counter
ALD = 1	Tandem connection AIS/LOP defect
AIS = 1	Tandem connection AIS failure condition
LOP = 1	Tandem connection LOP failure condition
IDL = 1	Tandem connection idle signal received
TST = 1	Tandem connection test signal received
CTI = 0	Error event counts are bit error counts
R = 0	Reserved (default value is 0)
NmNI = 00, 01, 10, 11	One-second report modulo 4 counter

FCS	Interpretation
Variable	CRC-16 frame check sequence

Figure C.6 – SDH tandem connection far-end performance report message status

	$t = t_0$	$t = t_0 + 1$	$t = t_0 + 2$	$t = t_0 + 3$
Flag	01111110	01111110	01111110	01111110
Address Octet 1	00111000	00111000	00111000	00111000
Address Octet 2	00000001	00000001	00000001	00000001
Control	00000011	00000011	00000011	00000011
Message Octet 1	**11111111**	00000000	00000000	00000000
Message Octet 2	**00000000**	00000000	00000000	00000000
Message Octet 3	**00000000**	10000001	10000010	00100011
Message Octet 4	**00000000**	00000000	00000000	00000000
Message Octet 5	11110000	**11111111**	00000000	00000000
Message Octet 6	00000000	**00000000**	00000000	00000000
Message Octet 7	00000011	**00000000**	10000001	10000010
Message Octet 8	00000000	**00000000**	00000000	00000000
Message Octet 9	00001111	11110000	**11111111**	00000000
Message Octet 10	00000000	00000000	**00000000**	00000000
Message Octet 11	00000010	00000011	**00000000**	10000001
Message Octet 12	00000000	00000000	**00000000**	00000000
Message Octet 13	00000000	00001111	11110000	**11111111**
Message Octet 14	00000000	00000000	00000000	**00000000**
Message Octet 15	00000001	00000010	00000011	**00000000**
Message Octet 16	00000000	00000000	00000000	**00000000**
FCS Octet 1	xxxxxxxx	xxxxxxxx	xxxxxxxx	xxxxxxxx
FCS Octet 2	xxxxxxxx	xxxxxxxx	xxxxxxxx	xxxxxxxx

NOTES

$t = t_0 - 3$:	Tandem connection error count = 0;	all other parameters = 0; N(t) = 1
$t = t_0 - 2$:	Tandem connection error count = 15;	all other parameters = 0; N(t) = 2
$t = t_0 - 1$:	Tandem connection error count = 240;	all other parameters = 0; N(t) = 3
$t = t_0$:	Tandem connection error count = 255;	all other parameters = 0; N(t) = 0
$t = t_0 + 1$:	AIS/LOP defect detected;	all other parameters = 0; N(t) = 1
$t = t_0 + 2$:	AIS/LOP defect detected;	all other parameters = 0; N(t) = 2
$t = t_0 + 3$:	LOP failure detected;	all other parameters = 0; N(t) = 3

Figure C.7 – Example of an SDH tandem connection far-end performance report message status

C.6.3.1 Elements of the far-end performance report message

Occurrences of performance anomalies, defects, failures and status conditions indicate the overall quality of transmission on a tandem connection. The tandem connection anomalies, defects, failures and status conditions that shall be detected and reported are:

– tandem connection error event;

– tandem connection AIS/LOP defect;

– tandem connection AIS failure;

– tandem connection LOP failure;
– tandem connection idle signal received condition;
– tandem connection test signal received condition;
– tandem connection count type indicator (CTI).

These tandem connection events and conditions are defined in the following clauses.

C.6.3.2 Tandem connection error event

A tandem connection error event is detected by comparing the calculated number of errors received at the end of the tandem connection, using the B3 byte, with the incoming error count contained in the tandem connection overhead (i.e., bits 1-4 of the N1 byte), for each of the signals that make up the tandem connection. The IEC field is interpreted according to Table C.2.

C.6.3.3 Tandem connection AIS/LOP defect

AU-n AIS defect and AU-n LOP defect are defined in ITU-T Rec. G.783. The occurrence of either one of these defects, in at least one of the signals that make up the tandem connection, constitutes a tandem connection AIS/LOP defect.

C.6.3.4 Tandem connection AIS failure

A tandem connection AIS failure is declared if the AU-n AIS defect is present, in at least one of the signals that make up the tandem connection, for a period T, where T is 2.5 ± 0.5 s.

C.6.3.5 Tandem connection LOP failure

A tandem connection LOP failure is declared if the AU-n LOP defect is present, in at least one of the signals that make up the tandem connection, for a period T, where T is 2.5 ± 0.5 s.

C.6.3.6 Tandem connection idle signal received condition

A tandem connection idle signal received condition occurs when a valid tandem connection idle signal is detected at the end of a tandem connection.

C.6.3.7 Tandem connection test signal received condition

A tandem connection test signal received condition occurs when a valid tandem connection test signal is detected at the end of a tandem connection.

C.6.3.8 Tandem connection count type indicator

The tandem connection count type indicator is set to 0 to indicate that the tandem connection IEC contains a count of the number of bit errors (not block errors) which were detected in the previous one-second interval.

C.6.4 Special carrier applications

A carrier may require the use of the tandem connection data link for purposes related to the provisioning or maintenance of the tandem connection or SDH network. Such uses may cause interruptions, delays or reduction of throughput on the tandem connection data link, but shall not impact the timely transmission of the LAPD messages defined above.

The LAPD messages defined above should be constructed and inserted on the data link by the source terminal (TCTE) that constructs the tandem connection signal whether it is a carrier (CR=1) or a DTE (CR=0) terminal. The messages should be delivered without alteration to the TCTE that sinks the information payload of the tandem connection signal.

C.7 Treatment of incoming signal failures

AU-n (n=3, 4) AIS is specified as all 1s in the entire AU-n, including the AU-n pointer. Since the AU-n pointer is invalid during AIS, the HOVC POH cannot be accessed. Without the following changes, the tandem connection overhead would be lost during signal failures.

When there is a failure on an incoming signal at the origination point of a tandem connection (originating TCTE), the pointers should be re-established within the tandem connection (in order to locate the tandem connection overhead). A new incoming signal failure (ISF) indicator shall be set within the tandem connection to indicate that there was a signal failure before the tandem connection, and AU-n AIS shall be inserted in the appropriate signal(s) at the end of the tandem connection.

The following clauses discuss the treatment of signal failures which occur before and within the tandem connection, respectively.

C.7.1 Signal failures before the tandem connection

Figure C.8 illustrates tandem connections with incoming signal failures. For transmission from left to right, when there is a signal failure on an incoming AU-n at the originating TCTE, that TCTE will insert a valid pointer value in H1, H2 and H3. With this pointer value, the originating TCTE will locate B3 and the TCOH. An incoming error count of 14 (1110) will be written into the IEC (bits 1-4 of the TCOH) and, for the first HOVC only, the data link will be written into bits 5-8 of the TCOH. All 1s will be written into the remainder of the HOVC, except for B3. B3 shall be calculated in order to provide even parity over the previous frame.

Within the tandem connection, no special treatment is necessary. AU-ns which entered with a signal failure will have valid pointers within the tandem connection (inserted by the originating TCTE). Regenerator section and/or multiplex section terminating equipment within the tandem connection will see valid pointers and will treat the signals as if they were carrying traffic.

At the end of the tandem connection, the terminating TCTE will interpret an IEC value of 14 as an incoming signal failure (ISF) indication. When an ISF indication is received, the terminating TCTE will insert AU-n AIS on the appropriate outgoing signals. For tandem connection error calculations, ISF values of 9 through 13 and 15 will be interpreted as zero incoming errors (IEC=0).

NOTE – IEC values of 9 through 13 and 15 are reserved for future standardization.

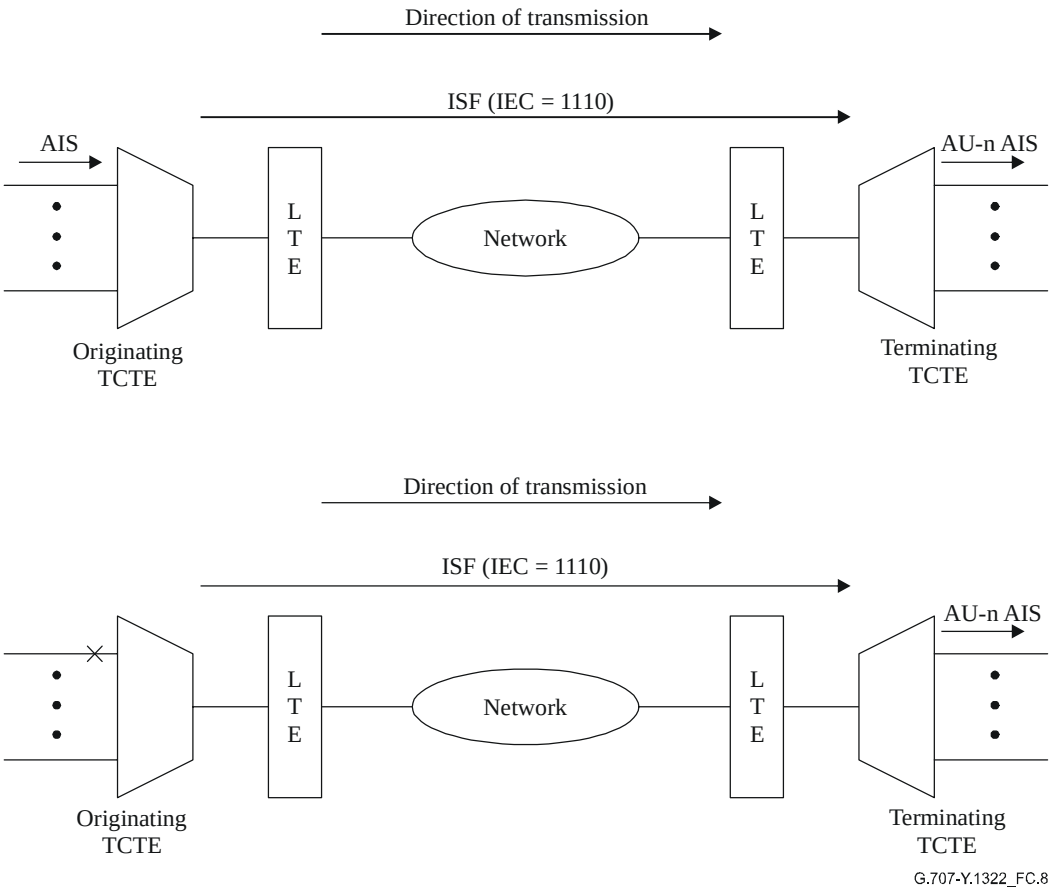


Figure C.8 – Tandem connection with incoming signal failures

C.7.2 Signal failures within the tandem connection

Figure C.9 illustrates signal failures within a tandem connection. No special treatment is required for these failures. Regenerator section and/or multiplex section terminating equipment within the tandem connection will respond to signal failures. If AU-n AIS is received at the terminating TCTE, it will indicate a signal failure within the tandem connection.

NOTE – As discussed above, signal failures before the originating TCTE will be converted to ISF by the originating TCTE. Therefore, AU-n AIS at the terminating TCTE indicates a failure inside the tandem connection.

When the terminating TCTE receives a signal failure, it will insert AIS in the appropriate outgoing AU-ns, and will return the appropriate message to the originating TCTE via the tandem connection far-end performance report message.

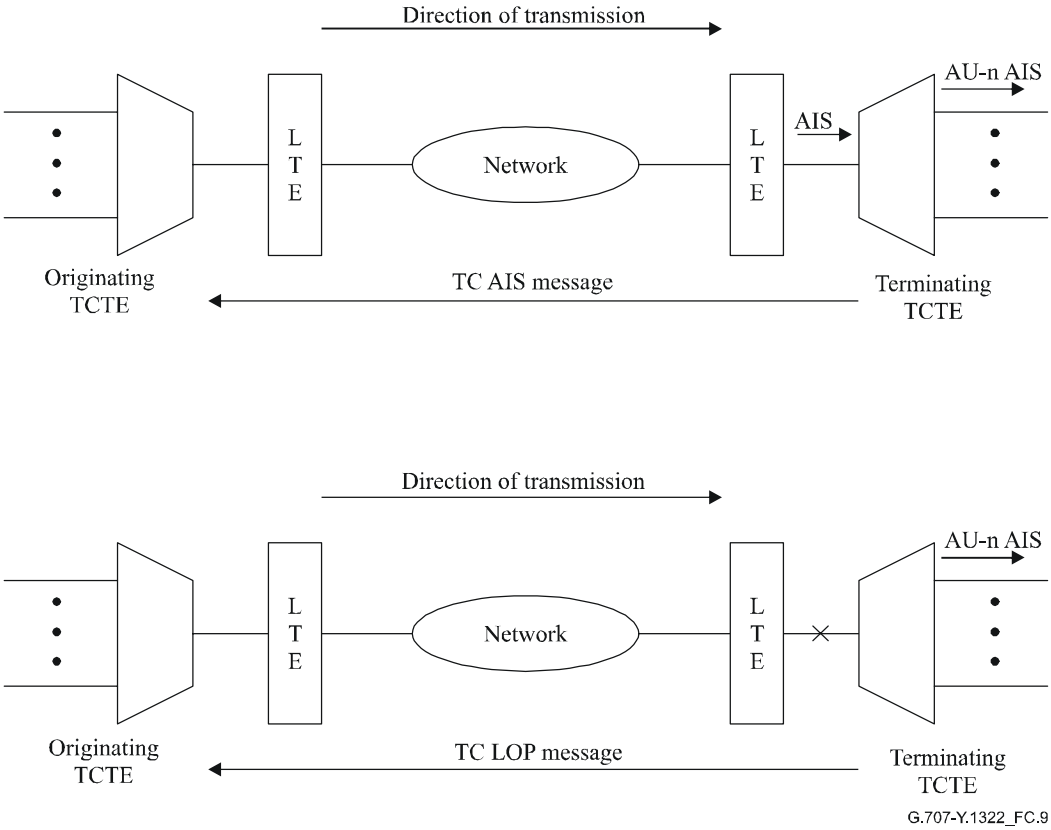


Figure C.9 – Signal failures within the tandem connection

C.8 Tandem connection idle signal

Tandem connection idle signal is defined as a tandem connection with all constituent signal labels set to "unequipped" (C2=00), and a valid idle signal ID message on the tandem connection data link (per clause C.6).

C.9 Tandem connection test signal

Tandem connection test signal is defined as any valid tandem connection signal with a valid tandem connection test signal ID.

Annex D

VC-4-Xc/VC-4/VC-3 tandem connection monitoring protocol: Option 2

(This annex forms an integral part of this Recommendation)

NOTE – The TC monitoring may have an unexpected dependence to the incoming signal. See Appendix VIII for a description of the problem.

D.1 N1 byte structure

N1 is allocated for tandem connection monitoring for contiguously concatenated VC-4, the VC-4 and VC-3 levels. The structure of the N1 byte is given in Table D.1.

- Bits 1-4 are used as an incoming error count (IEC); the coding is given in Table D.2.
- Bit 5 operates as the TC-REI of the tandem connection to indicate errored blocks caused within the tandem connection.
- Bit 6 operates as the OEI to indicate errored blocks of the egressing VC-n.
- Bits 7-8 operate in a 76 multiframe as:
  - the access point identifier of the tandem connection (TC-API); it complies with the generic 16-byte string format given in clause 9.2.2.2;
  - the TC-RDI, indicating to the far end that defects have been detected within the tandem connection at the near end tandem connection sink;
  - the ODI, indicating to the far end that AU/TU-AIS has been inserted into the egressing AU-n/TU-n at the TC-sink due to defects before or within the tandem connection;
  - reserved capacity (for future standardization).

The structure of the multiframe is given in Tables D.3 and D.4.

Table D.1 – N1 byte structure

b1	b2	b3	b4	b5	b6	b7	b8
IEC				TC-REI	OEI	TC-API, TC-RDI ODI, reserved	

Table D.2 – IEC coding

b1	b2	b3	b4	Number of BIP-8 violations
1	0	0	1	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	1	1	0	Incoming AIS

Table D.2 – IEC coding

NOTE – To guarantee a non all-zeros N1 byte independent of the incoming signal status, it is required that the IEC code field contains at least one "1". When zero errors in the BIP-8 of the incoming signal are detected, then an IEC code is inserted with "1"s in it. In this manner, it is possible for the tandem connection sink at the tail end of the tandem connection link to use the IEC code field to distinguish between unequipped conditions started within or before the tandem connection.

Table D.3 – b7-b8 multiframe structure

Frame #	Bits 7 and 8 definition
1-8	Frame alignment signal: 1111 1111 1111 1110
9-12	TC-API byte #1 [1 $C_1C_2C_3C_4C_5C_6C_7$]
13-16	TC-API byte #2 [0 X X X X X X X]
17-20	TC-API byte #3 [0 X X X X X X X]
:	:
65-68	TC-API byte #15 [0 X X X X X X X]
69-72	TC-API byte #16 [0 X X X X X X X]
73-76	TC-RDI, ODI and reserved (see Table D.4)

Table D.4 – Structure of frames Nos 73-76 of the b7-b8 multiframe

TC-RDI, ODI and reserved capacity		
Frame #	**b7 definition**	**b8 definition**
73	Reserved (default = "0")	TC-RDI
74	ODI	Reserved (default = "0")
75	Reserved (default = "0")	Reserved (default = "0")
76	Reserved (default = "0")	Reserved (default = "0")

D.2 TCM functionality at the tandem connection source

- If no valid AU-n/TU-n enters the tandem connection at the TC-source, then a valid pointer is inserted. This results in a VC-AIS signal as described in clause 6.2.4.1.4 being inserted; the IEC is set to "incoming AIS" code (see Table D.2).
- If a valid AU-n/TU-n enters the tandem connection, then an even BIP-8 is computed for each bit n of every byte of the VC-n in the preceding frame including B3 and compared with byte B3 recovered from the current frames to determine the number of BIP violations arriving at the tandem connection source. This value is coded into bits 1 to 4 as shown in Table D.2.
  - In both cases, bits 5-8 are assembled and transmitted according to Tables D.1, D.3 and D.4. The bits TC-REI, TC-RDI, OEI, ODI are set to "1" if the corresponding anomaly or defect is detected at the associated TC-sink of the reverse direction.
  - The BIP-8 is compensated according to the algorithm described in clause D.4.

NOTE – If an unequipped or supervisory unequipped signal enters a tandem connection, then the N1 and B3 bytes are overwritten with values not equal to all zeroes.

D.3 TCM functionality at the tandem connection sink

- If no valid AU-n/TU-n arrives at the TC-sink, the corresponding defect caused within the tandem connection is declared. The TC-RDI and ODI bits are set to 1 in the reverse direction and an AU/TU-AIS is inserted in the egressing AU-n/TU-n.
- If a valid AU-n/TU-n is present at the TC-sink the N1 byte is monitored:
  - An "all-zeroes" N1-byte indicates a disconnection or misconnection within the tandem connection. In this case, the TC-RDI and ODI bits are set to 1 in the reverse direction and an AU/TU-AIS is inserted in the egressing AU-n/TU-n.
  - The multiframe in bits 7 and 8 is recovered and the contents are interpreted. If the multiframe cannot be found, the TC-RDI and ODI bits are set to 1 in the reverse direction and AU/TU-AIS is inserted in the egressing AU-n/TU-n.
  - The TC-API is recovered and compared with the expected TC-API. In the case of a mismatch, the TC-RDI and ODI bits are set to 1 in the reverse direction and AU/TU-AIS is inserted in the egressing AU-n/TU-n.
  - The IEC field is interpreted according to Table D.5.

    An "incoming AIS" code indicates that a defect has already occurred before the tandem connection. In this case, only the ODI-bit is set to 1 in the reverse direction and AU/TU-AIS is inserted in the egressing AU-n/TU-n.

    The even BIP-8 parity is computed for each bit n of every byte of the VC-n in the preceding frame, including B3, and compared with byte B3 recovered from the current frames to determine the number of BIP violations. The OEI bit is set to 1 in the reverse direction if the number of determined BIP-violations is greater than zero. Furthermore, this value is compared with the number of BIP violations retrieved from IEC of the current frame. If the difference is not equal to zero, an errored block caused within the tandem connection is declared and a TC-REI bit is signalled in the reverse direction.

    If TU-n/AU-AIS is not inserted by the tandem connection sink, the N1 byte is set to all zeros and the BIP is compensated according to the algorithm described in clause D.4.

Table D.5 – IEC code interpretation

b1	b2	b3	b4	IEC code interpretation
0	0	0	0	0 BIP violation
0	0	0	1	1 BIP violation
0	0	1	0	2 BIP violations
0	0	1	1	3 BIP violations
0	1	0	0	4 BIP violations
0	1	0	1	5 BIP violations
0	1	1	0	6 BIP violations
0	1	1	1	7 BIP violations
1	0	0	0	8 BIP violations
1	0	0	1	0 BIP violation
1	0	1	0	0 BIP violation
1	0	1	1	0 BIP violation
1	1	0	0	0 BIP violation
1	1	0	1	0 BIP violation
1	1	1	0	0 BIP violation, incoming AIS
1	1	1	1	0 BIP violation

D.4 BIP-8 compensation

Since the BIP-8 parity check is taken over the VC-n (including N1), writing into N1 at the TC-source or TC-sink will affect the VC-4-Xc/VC-4/VC-3 path parity calculation. Because the BIP-8 parity should always be consistent with the current state of the VC-n, the BIP has to be compensated each time N1 byte is modified. Since the BIP-8 value in a given frame reflects the parity check over the previous frame, the changes made to BIP-8 bits in the previous frame shall also be considered in the compensation of BIP-8 in the current frame. Therefore, the following equation shall be used for compensation of the individual bits of the BIP-8:

$$B3[i]'(t) = B3[i](t–1) \oplus B3[i]'(t–1) \oplus N1[i](t–1) \oplus N1[i]'(t–1) \oplus B3[i](t)$$

where:

B3[i] the existing B3[i] value in the incoming signal

B3[i]' the new (compensated) B3[i] value

N1[i] the existing N1[i] value in the incoming signal

N1[i]' the new value written into the N1[i] bit

$\oplus$ exclusive OR operator

t the time of the current frame

t–1 the time of the previous frame

Annex E

VC-2, VC-12 and VC-11 tandem connection monitoring protocol

(This annex forms an integral part of this Recommendation)

E.1 N2 byte structure

N2 is allocated for tandem connection monitoring for the VC-2, VC-12 and VC-11 levels. The structure of the N2 byte is given in Table E.1.

- Bits 1-2 are used as an even BIP-2 for the tandem connection.
- Bit 3 is fixed to "1". This guarantees that the contents of N2 is not all zeros at the TC-source. This enables the detection of an unequipped or supervisory-unequipped signal at the tandem connection sink without the need of monitoring further OH-bytes.
- Bit 4 operates as an "incoming AIS" indicator.
- Bit 5 operates as the TC-REI of the tandem connection to indicate errored blocks caused within the tandem connection.
- Bit 6 operates as the OEI to indicate errored blocks of the egressing VC-n.
- Bits 7-8 operate in a 76 multiframe as:
  - the access point identifier of the tandem connection (TC-API); it complies with the generic 16-byte string format given in clause 9.2.2.2;
  - the TC-RDI, indicating to the far end that defects have been detected within the tandem connection at the near end tandem connection sink;
  - the ODI, indicating to the far end that TU-AIS has been inserted at the TC-sink into the egressing TU-n due to defects before or within the tandem connection;
  - reserved capacity (for future standardization).

The structure of the multiframe is given in Tables E.2 and E.3.

Table E.1 – N2 byte structure

b1	b2	b3	b4	b5	b6	b7	b8
BIP-2		"1"	Incoming AIS	TC-REI	OEI	TC-API, TC-RDI ODI, reserved	

Table E.2 – b7-b8 multiframe structure

Frame #	b7-b8 definition
1-8	Frame alignment signal: 1111 1111 1111 1110
9-12	TC-API byte #1 [1 $C_1C_2C_3C_4C_5C_6C_7$]
13-16	TC-API byte #2 [0 X X X X X X X]
17-20	TC-API byte #3 [0 X X X X X X X]
:	:
65-68	TC-API byte #15 [0 X X X X X X X]
69-72	TC-API byte #16 [0 X X X X X X X]
73-76	TC-RDI, ODI and reserved (See Table E.3)

Table E.3 – Structure of frames Nos 73-76 of the b7-b8 multiframe

TC-RDI, ODI and reserved capacity		
Frame #	**b7 definition**	**b8 definition**
73	Reserved (default = "0")	TC-RDI
74	ODI	Reserved (default = "0")
75	Reserved (default = "0")	Reserved (default = "0")
76	Reserved (default = "0")	Reserved (default = "0")

E.2 TCM functionality at the tandem connection source

- If no valid TU-n is entering the tandem connection at the TC-source, a valid pointer is inserted. This results in a VC-AIS signal as described in clause 6.2.4.1.4 being inserted and bit 4 is set to "1". Even BIP-2 parity is calculated over the inserted VC-AIS signal and written into bits 1-2 of N2.
- If a valid TU-n is entering the tandem connection at the tandem connection source, then even BIP-2 parity is calculated over the incoming valid VC-n or the inserted VC-AIS signal and written into bits 1-2 of N2.
  - In both cases, bits 3-8 are assembled and transmitted according to Tables E.1, E.2 and E.3.

    The bits TC-REI, TC-RDI, OEI, ODI are set to "1" if the corresponding anomaly or defect is detected at the associated TC-sink of the reverse direction.
  - The original BIP-2 is compensated according to the algorithm described in clause E.4.

NOTE – In an unequipped or supervisory-unequipped signal entering a tandem connection, the N2 and V5 bytes are overwritten with values not equal to all zeros.

E.3 TCM functionality at the tandem connection sink

If no valid TU-n arrives at the TC-sink, the corresponding defect caused within the tandem connection is declared and the TC-RDI and ODI conditions apply. A TU-AIS is inserted in the outgoing TU-n.

If a valid TU-n is present at the TC-sink, the N2 byte is monitored:

– An "all-zeros" N2-byte indicates a disconnection or misconnection within the tandem connection. In this case, the TC-RDI and ODI-bits are set to "1" in the reverse direction and TU-AIS is inserted in the egressing TU-n.

– Bit 4 of the received N2 set to "1" indicates that a defect has already occurred before the tandem connection. In this case, the ODI bit is set to "1" in the reverse direction and TU-AIS is inserted in the egressing TU-n.

– The multiframe in bits 7 and 8 is recovered and the contents are interpreted. If the multiframe cannot be found, the TC-RDI and ODI bits are set to "1" in the reverse direction and TU-AIS is inserted in the egressing TU-n.

– The TC-API is recovered and compared with the expected TC-API. In the case of a mismatch, the TC-RDI and ODI bits are set to "1" in the reverse direction and TU-AIS is inserted in the egressing TU-n.

The even BIP-2 is computed for each bit pair of every byte of the preceding VC-n including V5 and compared with the BIP-2 retrieved from the V5-byte. A difference not equal to zero indicates that the VC-n has been corrupted and then the OEI bit is set to "1" in the reverse direction. Furthermore, the actual BIP-2 is compared with the BIP-2 retrieved from the N2-byte. A difference not equal to

zero indicates that the VC-n has been corrupted within the tandem connection and then the TC-REI is set to "1" in the reverse direction.

If TU-AIS is not inserted at the tandem connection sink, then the N2-byte is set to all zeroes and the BIP is compensated according to the algorithm described in clause E.4.

E.4 BIP-2 compensation

Since the BIP-2 parity check is taken over the VC-n (including N2), writing into N2 at the TC-source or TC-sink will affect the VC-2/VC-12/VC-11 path parity calculation. Unless this is compensated, the error monitoring mechanism of BIP-2 is corrupted. Because the parity should always be consistent with the current state of the VC-n, the BIP has to be compensated each time N2-byte is modified. Since the BIP-2 value in a given frame reflects the parity check over the previous frame, the changes made to BIP-2 bits in the previous frame shall also be considered in the compensation of BIP-2 in the current frame. Therefore, the following equation shall be used for compensation of the individual bits of the BIP-2:

$$V5[1]'(t) = V5[1](t-1) \oplus V5[1]'(t-1) \oplus N2[1](t-1) \oplus N2[3](t-1) \oplus N2[5](t-1) \oplus N2[7](t-1) \oplus N2[1]'(t-1) \oplus N2[3]'(t-1) \oplus N2[5]'(t-1) \oplus N2[7]'(t-1) \oplus V5[1](t)$$

$$V5[2]'(t) = V5[2](t-1) \oplus V5[2]'(t-1) \oplus N2[2](t-1) \oplus N2[4](t-1) \oplus N2[6](t-1) \oplus N2[8](t-1) \oplus N2[2]'(t-1) \oplus N2[4]'(t-1) \oplus N2[6]'(t-1) \oplus N2[8]'(t-1) \oplus V5[2](t)$$

where:

V5[i]	the existing V5[i] value in the incoming signal
V5[i]'	the new (compensated) V5[i] value
N2[i]	the existing N2[i] value in the incoming signal
N2[i]'	the new value written into the N2[i] bit
$\oplus$	exclusive OR operator
t	the time of the current frame
t–1	the time of the previous frame

Annex F

Transport of 10 Gbit/s Ethernet in a VC-4-64c

(This annex forms an integral part of this Recommendation)

IEEE has defined in IEEE 802.3ae a 10 Gbit/s Ethernet WAN interface. This interface is basically an STM-64 with a VC-4-64c and the Ethernet MAC mapped into the VC-4-64c using a 64B/66B coding (see IEEE 802.3ae, sections 49 and 50). Some limitations on the use of overhead bytes apply (see IEEE 802.3ae, section 50). Furthermore, the 10 Gbit/s Ethernet WAN signal has a different clock accuracy (see Appendix XII).

F.1 Mapping of Ethernet MAC into VC-4-64c using 64B/66B coding

The Ethernet MAC data is 64B/66B coded as defined in IEEE 802.3ae, section 49.2.4. The 64B/66B coded continuous data stream is mapped into the VC-4-64c payload area as shown in Figure F.1. The mapping is independent of the Ethernet block and packet boundaries. A bit re-labelling process is used to accommodate the different bit numbering schemes used by IEEE 802.3 and SDH (see IEEE 802.3ae, sections 49.1.4.5 and 50.3.1).

The C2 path signal label shall be set to "1A" as defined in Table 9-11.

Note that this mapping is an alternative to the mapping of Ethernet MAC frames into a VC-4-64c using GFP (see 10.6 and ITU-T Rec. G.7041/Y.1303).

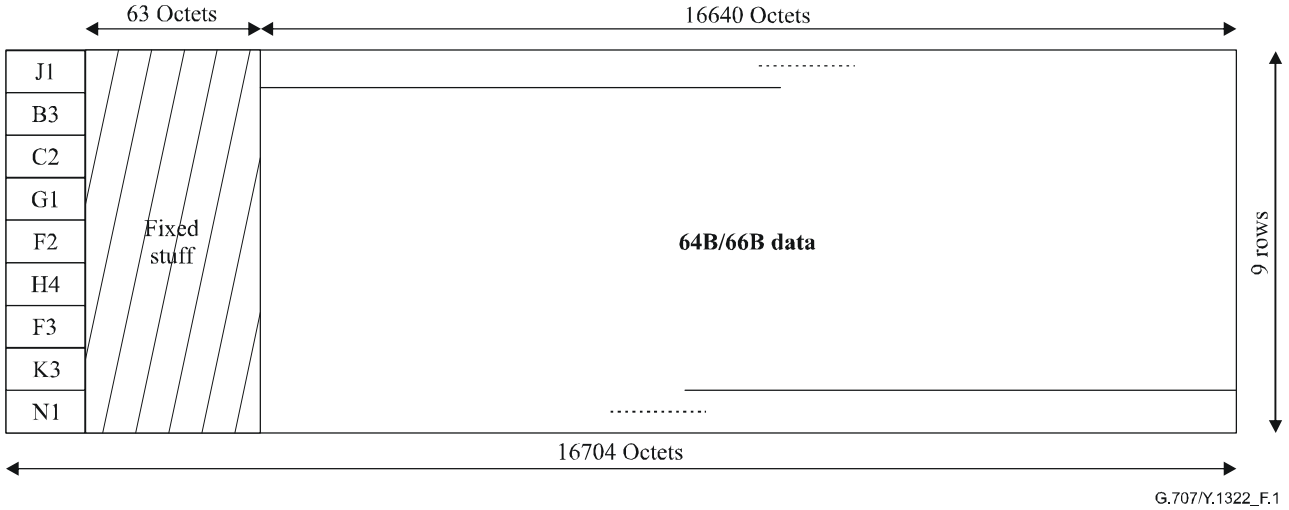


Figure F.1 – 64B/66B coded Ethernet MAC mapping into VC-4-64c

Annex G

Mapping of *N* × TU-12 in *M* virtual concatenated SHDSL pairs (dSTM-12*NMi*)

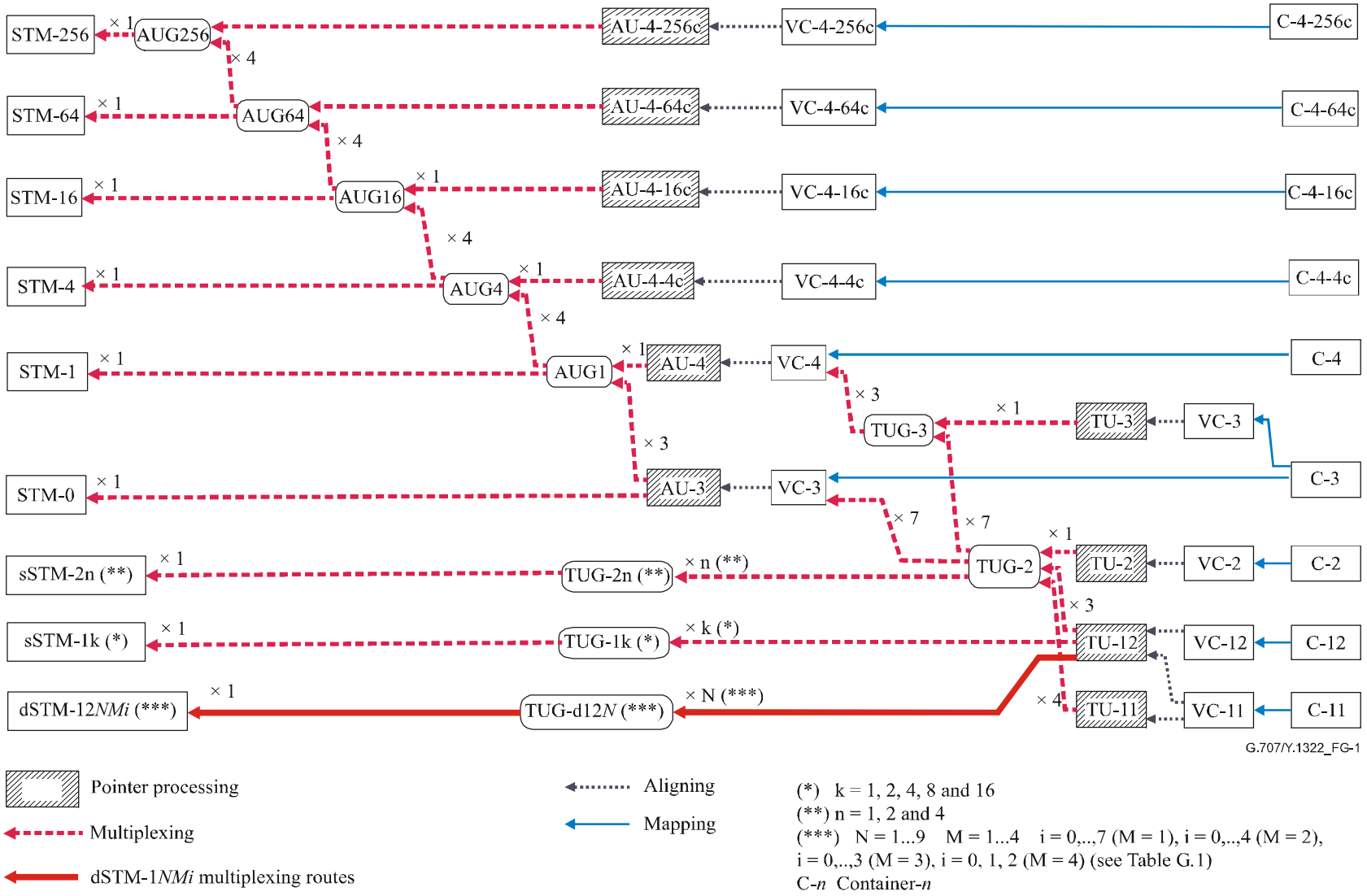
(This annex forms an integral part of this Recommendation)

Clause E.14/G.991.2 specifies the mapping of *N* × TU-12 (*N* = 1...9) into *M* (*M* = 1...4) virtual concatenated SHDSL wire pairs with an optional (*M* × *i* × 8) kbit/s DCC.

This annex specifies the associated additional multiplexing route and the SDH-related signal names.

G.1 Multiplex structure

Figure G.1 shows, within the general SDH multiplexing scheme (including the one defined in ITU-T Rec. G.708 for sub-STM-0), the additional multiplexing route provided by clause E.14/G.991.2. I.e., the multiplexing routes of specific dSTM-12*NMi* (of order *N* = 1...9, *M* = 1...4 and *i* = 0,..,7 (single-pair mode), *i* = 0,..,4 (2-pair mode), *i* = 0,..,3 (3-pair mode) and *i* = 0, 1, 2 (4-pair mode)) via a tributary unit group d12*N* (TUG-d12*N*).



NOTE – This figure is informative and shows the additional multiplexing routes added by this Recommendation (dSTM-12*NMi*).
It is adapted from ITU-T Recs G.707/Y.1322 and G.708.

Figure G.1 – Additional structure for dSTM

G.2 Mapping overview

Table G.1 provides an overview of the defined set of dSTM-12*NMi* signals. This table is based on Table E.42/G.991.2.

Table G.1 – Assignment of dSTM-12*NMi* names to *N* × TU-12/VC-12 connections over *M*-Pair SHDSL

Number (*N*) of TU-12 / VC-12 connections	**Aggregate payload bit rate [kbit/s]**	**1-Pair SHDSL** **Size 1 × k_s bits of each payload sub-block with k_s = i + n × 8 [bits]** ***M* = 1**	**2-Pair SHDSL** **Size 2 × k_s bits of each payload sub-block with k_s = i + n × 8 [bits]** ***M* = 2**	**3-Pair SHDSL** **Size 3 × k_s bits of each payload sub-block with k_s = i + n × 8 [bits]** ***M* = 3**	**4-Pair SHDSL** **Size 4 × k_s bits of each payload sub-block with k_s = i + n × 8 [bits]** ***M* = 4**
1	2304 + M × i × 8	n = 36; i = 0,..,7 dSTM-12110 to dSTM-12117	n = 18; i = 0,..,4 dSTM-12120 to dSTM-12124	n = 12; i = 0,..,3 dSTM-12130 to dSTM-12133	n = 9; i = 0,1,2 dSTM-12140 to dSTM-12142
2	4608 + M × i × 8	n = 72; i = 0,..,7 dSTM-12210 to dSTM-12217	n = 36; i = 0,..,4 dSTM-12220 to dSTM-12224	n = 24; i = 0,..,3 dSTM-12230 to dSTM-12233	n = 18; i = 0,1,2 dSTM-12240 to dSTM-12242
3	6912 + M × i × 8	–	n = 54; i = 0,..,4 dSTM-12320 to dSTM-12324	n = 36; i = 0,..,3 dSTM-12330 to dSTM-12333	n = 27; i = 0,1,2 dSTM-12340 to dSTM-12342
4	9216 + M × i × 8	–	n = 72; i = 0,..,4 dSTM-12420 to dSTM-12424	n = 48; i = 0,..,3 dSTM-12430 to dSTM-12433	n = 36; i = 0,1,2 dSTM-12440 to dSTM-12442
5	11 520 + M × i × 8	–	–	n = 60; i = 0,..,3 dSTM-12530 to dSTM-12533	n = 45; i = 0,1,2 dSTM-12540 to dSTM-12542
6	13 824 + M × i × 8	–	–	n = 72; i = 0,..,3 dSTM-12630 to dSTM-12633	n = 54; i = 0,1,2 dSTM-12640 to dSTM-12642
7	16 128 + M × i × 8	–	–	n = 84; i = 0,..,3 dSTM-12730 to dSTM-12733	n = 63; i = 0,1,2 dSTM-12740 to dSTM-12742
8	18 432 + M × i × 8	–	–	–	n = 72; i = 0,1,2 dSTM-12840 to dSTM-12842
9	20 736 + M × i × 8	–	–	–	n = 81; i = 0,1,2 dSTM-12940 to dSTM-12942
		If no data communication channel is used i = 0. If management, signalling, control and maintenance functions are to be transmitted over the Z-bits, i × 8 kbit/s per wire-pair are additionally required with i = 1,..,7 (1-pair), i = 1,..,4 (2-pair), i = 1, 2, 3 (3-pair) and i = 1, 2 (4-pair).			

Annex H

Mapping of TU-11, TU-12, TU-2 and TU-3 in G-PON GEM connections

(This annex forms an integral part of this Recommendation)

Clause I.4/G.984.3 specifies the mapping of individual TU-11, TU-12, TU-2 and TU-3 into GEM connections supported on G-PON transport systems.

This annex specifies the associated additional multiplexing routes and the SDH-related signal names.

H.1 Multiplex structure

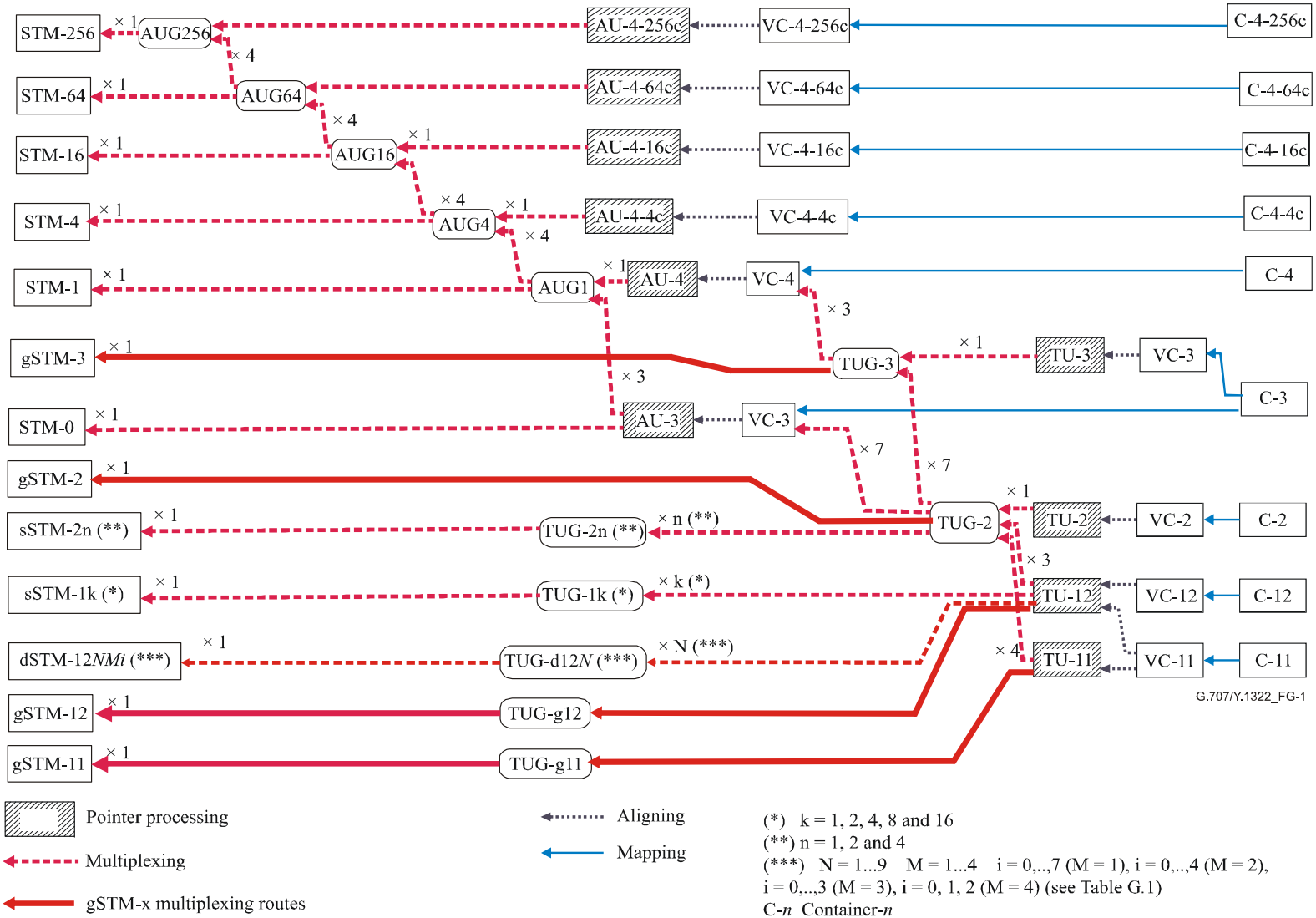
Figure H.1 shows, within the general SDH multiplexing scheme (including the one defined in ITU-T Rec. G.708 for sub STM-0), the additional multiplexing routes provided by clause I.4/G.984.3. This includes: the multiplexing route of gSTM-11 via a tributary unit group g11 (TUG-g11), multiplexing route of gSTM-12 via a tributary unit group g12 (TUG-g12), multiplexing route of gSTM-2 via a tributary unit group 2 (TUG-2), and multiplexing route of gSTM-3 via a tributary unit group 3 (TUG-3).

H.2 Mapping overview

Table H.1 provides an overview of the defined set of gSTM-11, gSTM-12, gSTM-2 and gSTM-3 signals. This table is based on the table in clause I.4/G.984.3.

Table H.1 – Assignment of gSTM-x names to TU-x connections over GEM

Type of TU-x connections	Aggregate payload bit rate [kbit/s]	Size of each GEM payload [bytes]
11	108 × 8/0.5 = 1 728	4(3 × 9) = 108
12	144 × 8/0.5 = 2 304	4(4 × 9) = 144
2	432 × 8/0.5 = 6 912	4(12 × 9) = 432
3	774 × 8/0.125 = 49 536	86 × 9 = 774



NOTE – This figure is informative and shows the additional gSTM-x multiplexing routes.

Figure H.1 – Additional structure for gSTM-x

Appendix I

Relationship between TU-2 address and location of columns within a VC-4

(This appendix does not form an integral part of this Recommendation)

Table I.1 shows the relationship between TU-2 address and location of columns within a VC-4.

Table I.1 – Relationship between TU-2 address and location of columns within a VC-4

TU-2 address			TU-2 column number											
K	**L**	**M**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**
1	1	0	10	31	52	73	94	115	136	157	178	199	220	241
1	2	0	13	34	55	76	97	118	139	160	181	202	223	244
1	3	0	16	37	58	79	100	121	142	163	184	205	226	247
1	4	0	19	40	61	82	103	124	145	166	187	208	229	250
1	5	0	22	43	64	85	106	127	148	169	190	211	232	253
1	6	0	25	46	67	88	109	130	151	172	193	214	235	256
1	7	0	28	49	70	91	112	133	154	175	196	217	238	259
2	1	0	11	32	53	74	95	116	137	158	179	200	221	242
2	2	0	14	35	56	77	98	119	140	161	182	203	224	245
2	3	0	17	38	59	80	101	122	143	164	185	206	227	248
2	4	0	20	41	62	83	104	125	146	167	188	209	230	251
2	5	0	23	44	65	86	107	128	149	170	191	212	233	254
2	6	0	26	47	68	89	110	131	152	173	194	215	236	257
2	7	0	29	50	71	92	113	134	155	176	197	218	239	260
3	1	0	12	33	54	75	96	117	138	159	180	201	222	243
3	2	0	15	36	57	78	99	120	141	162	183	204	225	246
3	3	0	18	39	60	81	102	123	144	165	186	207	228	249
3	4	0	21	42	63	84	105	126	147	168	189	210	231	252
3	5	0	24	45	66	87	108	129	150	171	192	213	234	255
3	6	0	27	48	69	90	111	132	153	174	195	216	237	258
3	7	0	30	51	72	93	114	135	156	177	198	219	240	261

Appendix II

Relationship between TU-12 address and location of columns within a VC-4

(This appendix does not form an integral part of this Recommendation)

Table II.1 shows the relationship between TU-12 address and location of columns within a VC-4.

Table II.1 – Relationship between TU-12 address and location of columns within a VC-4

TU-12 address			TU-12 column number			
K	**L**	**M**	**1**	**2**	**3**	**4**
1	1	1	10	73	136	199
1	1	2	31	94	157	220
1	1	3	52	115	178	241
1	2	1	13	76	139	202
1	2	2	34	97	160	223
1	2	3	55	118	181	244
1	3	1	16	79	142	205
1	3	2	37	100	163	226
1	3	3	58	121	184	247
1	4	1	19	82	145	208
1	4	2	40	103	166	229
1	4	3	61	124	187	250
1	5	1	22	85	148	211
1	5	2	43	106	169	232
1	5	3	64	127	190	253
1	6	1	25	88	151	214
1	6	2	46	109	172	135
1	6	3	67	130	193	256
1	7	1	28	91	154	217
1	7	2	49	112	175	238
1	7	3	70	133	196	259
2	1	1	11	74	137	200
2	1	2	32	95	158	221
2	1	3	53	116	179	242
2	2	1	14	77	140	203
2	2	2	35	98	161	224
2	2	3	56	119	182	245
2	3	1	17	80	143	206
2	3	2	38	101	164	227
2	3	3	59	122	185	248

Table II.1 – Relationship between TU-12 address and location of columns within a VC-4

TU-12 address			TU-12 column number			
K	**L**	**M**	**1**	**2**	**3**	**4**
2	4	1	20	83	146	209
2	4	2	41	104	167	230
2	4	3	62	125	188	251
2	5	1	23	86	149	212
2	5	2	44	107	170	233
2	5	3	65	128	191	254
2	6	1	26	89	152	215
2	6	2	47	110	173	236
2	6	3	68	131	194	257
2	7	1	29	92	155	218
2	7	2	50	113	176	239
2	7	3	71	134	197	260
3	1	1	12	75	138	201
3	1	2	33	96	159	222
3	1	3	54	117	180	243
3	2	1	15	78	141	204
3	2	2	36	99	162	225
3	2	3	57	120	183	246
3	3	1	18	81	144	207
3	3	2	39	102	165	228
3	3	3	60	123	186	249
3	4	1	21	84	147	210
3	4	2	42	105	168	231
3	4	3	63	126	189	252
3	5	1	24	87	150	213
3	5	2	45	108	171	234
3	5	3	66	129	192	255
3	6	1	27	90	153	216
3	6	2	48	111	174	237
3	6	3	69	132	195	258
3	7	1	30	93	156	219
3	7	2	51	114	177	240
3	7	3	72	135	198	261

Appendix III

Relationship between TU-11 address and location of columns within a VC-4

(This appendix does not form an integral part of this Recommendation)

Table III.1 shows the relationship between TU-11 address and location of columns within a VC-4.

Table III.1 – Relationship between TU-11 address and location of columns within a VC-4

TU-11 address			TU-11 column number		
K	**L**	**M**	**1**	**2**	**3**
1	1	1	10	94	178
1	1	2	31	115	199
1	1	3	52	136	220
1	1	4	73	157	241
1	2	1	13	97	181
1	2	2	34	118	202
1	2	3	55	139	223
1	2	4	76	160	244
1	3	1	16	100	184
1	3	2	37	121	205
1	3	3	58	142	226
1	3	4	79	163	247
1	4	1	19	103	187
1	4	2	40	124	208
1	4	3	61	145	229
1	4	4	82	166	250
1	5	1	22	106	190
1	5	2	43	127	211
1	5	3	64	148	232
1	5	4	85	169	253
1	6	1	25	109	193
1	6	2	46	130	214
1	6	3	67	151	135
1	6	4	88	172	256
1	7	1	28	112	196
1	7	2	49	133	217
1	7	3	70	154	238
1	7	4	91	175	259
2	1	1	11	95	179
2	1	2	32	116	200
2	1	3	53	137	221
2	1	4	74	158	242

Table III.1 – Relationship between TU-11 address and location of columns within a VC-4

TU-11 address			TU-11 column number		
K	**L**	**M**	**1**	**2**	**3**
2	2	1	14	98	182
2	2	2	35	119	203
2	2	3	56	140	224
2	2	4	77	161	245
2	3	1	17	101	185
2	3	2	38	122	206
2	3	3	59	143	227
2	3	4	80	164	248
2	4	1	20	104	188
2	4	2	41	125	209
2	4	3	62	146	230
2	4	4	83	167	251
2	5	1	23	107	191
2	5	2	44	128	212
2	5	3	65	149	233
2	5	4	86	170	254
2	6	1	26	110	194
2	6	2	47	131	215
2	6	3	68	152	236
2	6	4	89	173	257
2	7	1	29	113	197
2	7	2	50	134	218
2	7	3	71	155	239
2	7	4	92	176	260
3	1	1	12	96	180
3	1	2	33	117	201
3	1	3	54	138	222
3	1	4	75	159	243
3	2	1	15	99	183
3	2	2	36	120	204
3	2	3	57	141	225
3	2	4	78	162	246
3	3	1	18	102	186
3	3	2	39	123	207
3	3	3	60	144	228
3	3	4	81	165	249
3	4	1	21	105	189
3	4	2	42	126	210

Table III.1 – Relationship between TU-11 address and location of columns within a VC-4

TU-11 address			TU-11 column number		
K	**L**	**M**	**1**	**2**	**3**
3	4	3	63	147	231
3	4	4	84	168	252
3	5	1	24	108	192
3	5	2	45	129	213
3	5	3	66	150	234
3	5	4	87	171	255
3	6	1	27	111	195
3	6	2	48	132	216
3	6	3	69	153	237
3	6	4	90	174	258
3	7	1	30	114	198
3	7	2	51	135	219
3	7	3	72	156	240
3	7	4	93	177	261

Appendix IV

Relationship between TU-2 address and location of columns within a VC-3

(This appendix does not form an integral part of this Recommendation)

Table IV.1 shows the relationship between TU-2 address and location of columns within a VC-3.

Table IV.1 – Relationship between TU-2 address and location of columns within a VC-3

TU-2 address		**TU-2 column number**											
L	**M**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**
1	0	2	9	16	23	30	37	44	51	58	65	72	79
2	0	3	10	17	24	31	38	45	52	59	66	73	80
3	0	4	11	18	25	32	39	46	53	60	67	74	81
4	0	5	12	19	26	33	40	47	54	61	68	75	82
5	0	6	13	20	27	34	41	48	55	62	69	76	83
6	0	7	14	21	28	35	42	49	56	63	70	77	84
7	0	8	15	22	29	36	43	50	57	64	71	78	85

Appendix V

Relationship between TU-12 address and location of columns within a VC-3

(This appendix does not form an integral part of this Recommendation)

Table V.1 shows the relationship between TU-12 address and location of columns within a VC-3.

Table V.1 – Relationship between TU-12 address and location of columns within a VC-3

TU-12 address		TU-12 column number			
L	**M**	**1**	**2**	**3**	**4**
1	1	2	23	44	65
1	2	9	30	51	72
1	3	16	37	58	79
2	1	3	24	45	66
2	2	10	31	52	73
2	3	17	38	59	80
3	1	4	25	46	67
3	2	11	32	53	74
3	3	18	39	60	81
4	1	5	26	47	68
4	2	12	33	54	75
4	3	19	40	61	82
5	1	6	27	48	69
5	2	13	34	55	76
5	3	20	41	62	83
6	1	7	28	49	70
6	2	14	35	56	77
6	3	21	42	63	84
7	1	8	29	50	71
7	2	15	36	57	78
7	3	22	43	64	85

Appendix VI

Relationship between TU-11 address and location of columns within a VC-3

(This appendix does not form an integral part of this Recommendation)

Table VI.1 shows the relationship between TU-11 address and location of columns within a VC-3.

Table VI.1 – Relationship between TU-11 address and location of columns within a VC-3

TU-11 address		TU-11 column number		
L	**M**	**1**	**2**	**3**
1	1	2	30	58
1	2	3	31	59
1	3	5	33	61
1	4	7	35	63
2	1	4	32	60
2	2	12	40	68
2	3	18	46	74
2	4	24	52	80
3	1	6	34	62
3	2	13	41	69
3	3	19	47	75
3	4	25	53	81
4	1	8	36	64
4	2	14	42	70
4	3	20	48	76
4	4	26	54	82
5	1	9	37	65
5	2	15	43	71
5	3	21	49	77
5	4	27	55	83
6	1	10	38	66
6	2	16	44	72
6	3	22	50	78
6	4	28	56	84
7	1	11	39	67
7	2	17	45	73
7	3	23	51	79
7	4	29	57	85

Appendix VII

Enhanced remote defect indication (E-RDI)

(This appendix does not form an integral part of this Recommendation)

As an option, equipment may provide additional defect differentiation. Remote defect indication (RDI), as defined in clauses 9.3.1.4 and 9.3.2.1, provides back to the trail termination source an indication if either server signal defects, or connectivity defects, are being detected by the trail termination sink. RDI does not differentiate between types of defects. This appendix defines an enhanced remote defect indication which supports three types of RDI indications: E-RDI server defect, E-RDI connectivity defect and E-RDI payload defect. It provides differentiation between server signal defects (E-RDI server), connectivity defects (E-RDI connectivity) and payload or adaptation defects (E-RDI payload). If more than one of these defects occurs at the same time, the priority for the type of indication used will be in the order of:

1) E-RDI server;

2) E-RDI connectivity;

3) E-RDI payload.

The use of this option provides an operator with enhanced fault sectionalization capabilities for a trail crossing multi-operator domains. The enhanced remote defect indication option is compatible with equipment supporting RDI.

VII.1 VC-4-Xc/VC-4/VC-3 paths

As described in clause 9.3.1.4, byte G1 is allocated to convey back to a VC-4-Xc/VC-4/VC-3 trail termination source the status and performance of the complete trail. Bits 5 to 7 of byte G1 may be used to provide an enhanced remote defect indication with additional differentiation between the payload defect (PLM), server defects (AIS, LOP) and connectivity defects (TIM, UNEQ). The codes from Table VII.1 will be used.

Table VII.1 – G1 (b5-b7) coding and triggers

b5	b6	b7	Meaning	Triggers
0	0	1	No remote defect	No remote defect
0	1	0	E-RDI payload defect	PLM
1	0	1	E-RDI server defect	AIS, LOP
1	1	0	E-RDI connectivity defect	TIM, UNEQ

For the E-RDI codes, bit 7 is set to the inverse of bit 6. Table VII.2 provides the E-RDI G1 (b5-b7) code interpretation.

Table VII.2 – G1 (b5-b7) coding and E-RDI interpretation

b5	b6	b7	E-RDI Interpretation
0	0	0	No remote defect (Note 1)
0	0	1	No remote defect
0	1	0	E-RDI payload defect (Note 2)
0	1	1	No remote defect (Note 1)
1	0	0	E-RDI server defect (Note 1)
1	0	1	Remote E-RDI server defect
1	1	0	Remote E-RDI connectivity defect
1	1	1	Remote E-RDI server defect (Note 1)
NOTE 1 – These codes are generated by RDI supporting equipment and are interpreted by E-RDI supporting equipment as shown. For equipment supporting RDI (see clause 9.3.1.4), this code is triggered by the presence or absence of one of the following defects: AIS, LOP, TIM or UNEQ. Equipment conforming to an earlier version of this Recommendation may include PLM as a trigger condition. ATM equipment complying with the 1993 version of the I.432.x series of ITU-T Recommendations may include LCD as a trigger condition. Note that for some national networks, this code is triggered only by an AIS or LOP defect. NOTE 2 – ATM equipment complying with the 1996 version of ITU-T Rec. I.432.2 may include LCD as a trigger condition.			

The E-RDI G1 (b5-b7) code interpretation provides for interworking with equipment which supports RDI. It is not necessary for the interpretation to identify if the equipment supports RDI or E-RDI.

VII.2 VC-2, VC-12 and VC-11 paths

As described in clause 9.3.2.1, bits 3, 4 and 8 of byte V5 are allocated to convey back to a VC-2, VC-12 or VC-11 trail termination source the status and performance of the complete trail. Bits 5 to 7 of byte K4 may be used to provide an enhanced remote defect indication with additional differentiation between the payload defect (PLM), server defects (AIS, LOP) and connectivity defects (TIM, UNEQ). The codes from Table VII.3 will be used.

Table VII.3 – V5 b8 and K4 (b5-b7) coding and triggers

V5 b8	K4 b5	K4 b6	K4 b7	Meaning	Triggers
0	0	0	1	No remote defect	No remote defect
0	0	1	0	E-RDI payload defect	PLM
1	1	0	1	E-RDI server defect	AIS, LOP
1	1	1	0	E-RDI connectivity defect	TIM, UNEQ

For the E-RDI codes, V5 b8 is set to the same value as K4 b5. In addition, for the E-RDI codes, bit 7 is set to the inverse of bit 6. Table VII.4 provides the E-RDI K4 (b5-b7) code interpretation.

Table VII.4 – V5 b8 and K4 (b5-b7) coding and E-RDI interpretation

V5 b8	K4 b5	K4 b6	K4 b7	E-RDI Interpretation
0	0	0	0	No remote defect (Note 1)
0	0	0	1	No remote defect
0	0	1	0	E-RDI payload defect
0	0	1	1	No remote defect (Note 2)
0	1	0	0	No remote defect (Note 2)
0	1	0	1	No remote defect (Note 2)
0	1	1	0	No remote defect (Note 2)
0	1	1	1	No remote defect (Note 1)
1	0	0	0	E-RDI server defect (Note 1)
1	0	0	1	E-RDI server defect (Note 2)
1	0	1	0	E-RDI server defect (Note 2)
1	0	1	1	E-RDI server defect (Note 2)
1	1	0	0	E-RDI server defect (Note 2)
1	1	0	1	E-RDI server defect
1	1	1	0	E-RDI connectivity defect
1	1	1	1	E-RDI server defect (Note 1)

NOTE 1 – These codes are generated by RDI supporting equipment and are interpreted by E-RDI supporting equipment as shown. For equipment supporting RDI (see clause 9.3.2.1) this code is triggered by the presence or absence of one of the following defects: AIS, LOP, TIM or UNEQ. Equipment conforming to an earlier version of this Recommendation may include PLM as a trigger condition. Note, for some national networks, this code is triggered only by an AIS or LOP defect.

NOTE 2 – This code is not applicable to any known standards; it is included here for completeness.

The E-RDI V5 b8 and K4 (b5-b7) coding interpretation provides for interworking with equipment which supports RDI. It is not necessary for the interpretation to identify if the equipment supports RDI or E-RDI.

Appendix VIII

Unexpected behaviour, dependence of TC monitoring on the incoming signal

(This appendix does not form an integral part of this Recommendation)

VIII.1 Entering AIS condition (in case of VC-3/VC-4/VC-4-Xc)

Entering of the AIS condition is already critical for the VC-3/VC-4/VC-4-Xc cases; the issue here is the moment the signal is replaced by all-1s.

Assume that an all-1s signal is inserted at the moment the B3 byte would be output by the adaptation sink function (MSn/Sn_A_Sk). As such, the TC_TT_So function will detect B3=all-1s and detects a number of BIP violations. While all-1s (AIS) insertion is accompanied by SSF=true, the N1[1-4] bits will be written with IncAIS code (1110) according to our standards. It is not possible to forward the IEC count at this moment. This will cause the far-end (TC_TT_Sk) to detect BIP-8 violations in B3 and IncAIS code (or IEC=0); and consequently an errored block will be declared. Also, in this example, in the next frame, BIP-8 violations will be detected with IEC=0, and another EB is declared. The reason is that the insertion of AIS started "in the middle of the VC-n frame" (as said above at the B3 byte location). If the AIS insertion had started at the J1 byte location, or behind the B3 location, only a single frame would have been impacted.

Conclusion: at VC-3/VC-4/VC-4-Xc tandem connections it is possible to get 1 or 2 errored seconds being detected by the TC-TT_Sk function at the end of the TC as a result of the insertion of AIS in front of the TC.

VIII.2 Entering AIS condition (in case of VC-11/VC-12/VC-2)

This problem does not occur at the VC-11/VC-12/VC-2 level; there is a real BIP-2 there, not an IEC.

VIII.3 Recovery from a phase jump (valid for all VC-n)

Causes of phase jumps at the ingress of a TC that have been identified so far are:

– recovery from SSF condition (LOP, AIS);

– establishment of a different path as a result of a cross-connect change, (e.g., from B→A to C→A, from UNEQ→A to B→A, from B→A to UNEQ→A);

– recovery of a byte synchronous mapped 2 Mbit/s signal from AIS condition; VC-12 signal will follow the phase jump of the 2 Mbit/s signal (see Annex C/ETSI EN 300 417-4-1 V1.2.1);

– protection switching caused by external commands, by revertive operation, by signal degrade SD.

The phase jump of the VC-n is to be communicated towards the VC-n path termination sink via the VC-n signal itself and via the AU/TU pointer. As a consequence, such phase jump travels with different speed through the network: the VC-n bytes go much faster than the AU/TU pointer. A VC-n signal will experience a few bytes delay in each pointer processor, while the AU/TU pointer will experience between 0 and (a little bit more than) one frame delay in each pointer processor.

Consequently, the TC termination sink (and VC termination sink) will be misaligned for some frames; the last pointer processor before the TC [VC] termination sink still uses the previous pointer, which is no longer aligned with the VC-n data after the phase jump. This means that the wrong bytes are used as POH and the BIP-n calculation will be wrong.

Appendix IX

Forward error correction for STM-16

(This appendix does not form an integral part of this Recommendation)

See Annex A with N equal to 16 and M equal to 1.

Figure 9-5 gives the allocation of P1 and Q1 parity and status bytes for STM-16 signal.

The 8-way bit interleaving in conjunction with BCH-3 provides 24-bit burst error correction capability per row for STM-16.

Appendix X

Performance of in-band FEC

(This appendix does not form an integral part of this Recommendation)

A criterion for the evaluation of the intrinsic correcting performance of the in-band BCH-3 code is the theoretical relationship between the line BER after the FEC error correction (BER_{Output}, Pc) and the line BER before the FEC error correction (BER_{Input}, p).

For BCH codes, this criterion can be mathematically computed with the assumptions that errors occur independently from each other and that the decoder never fails (probability of incorrect decoding equals zero).

$$Pc = \sum_{i=4}^{N} \frac{i}{N} \cdot \binom{N}{i} \cdot p^{i} \cdot (1-p)^{N-i}$$

where N = 4359.

This theoretical intrinsic performance gain of the BCH-3 code is given in Figures X.1 and X.2 versus input BER and Q value respectively.

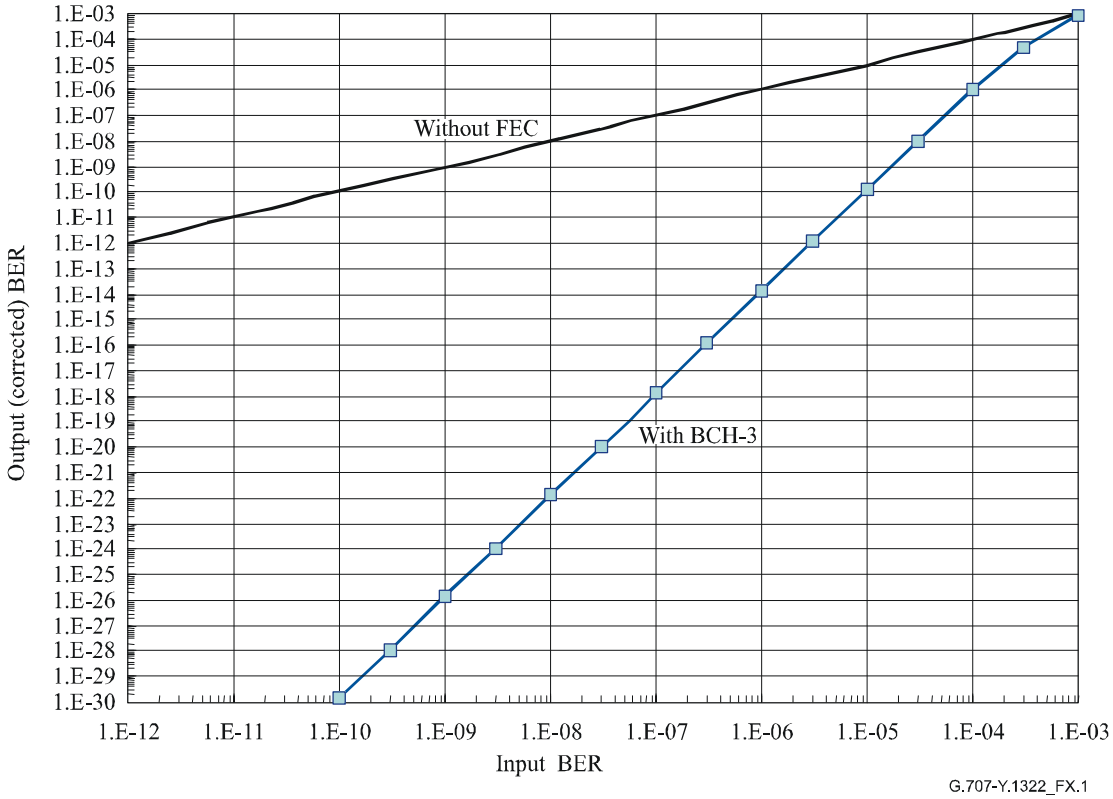


Figure X.1 – Theoretical output (corrected) BER versus input BER (BCH-3)

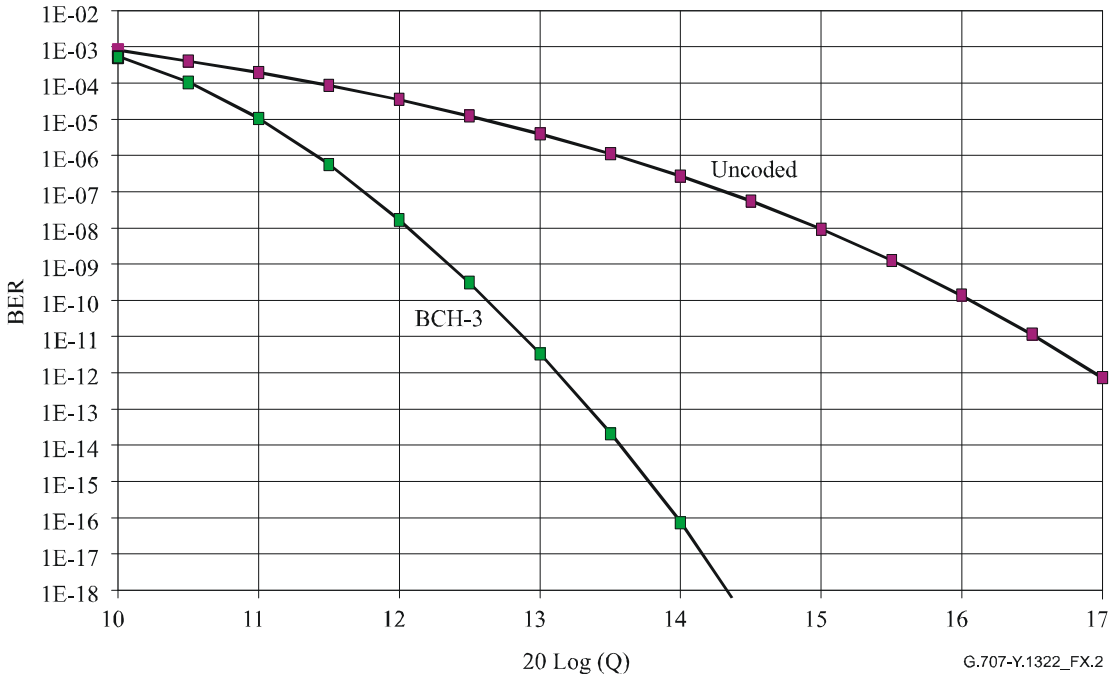


Figure X.2 – Theoretical output (corrected) BER versus Q value (BCH-3)

The FEC function performance can also be evaluated through the coding gain. In this Recommendation the coding gain is evaluated by the difference in Q-value required for coded and uncoded operation to a specified level of communication performance.

Figure X.2 gives performance curves to provide the coding gain in terms of Q-value. The Q-value in the horizontal axis is provided as 20 log (Q). For example, the gain at 10^{-12} is 3.8 dB. The coding gain in terms of 20 log (Q) is equivalent to coding gain as represented by optical signal-to-noise ratio (OSNR) when the line system uses optical amplifiers.

The FEC performance may be slightly improved when the FEC decoding is optionally performed in the regenerators as described in clause A.4.3. The performance gain of using FEC per span versus end-to-end is given in Figure X.3. Note that equally distributed raw BER among the spans are assumed. Normally BER are different span-by-span and the FEC performance is mainly given by the worst BER span. Therefore, the assumption of equal BER distribution gives the worst-case performance for the end-to-end decoding method.

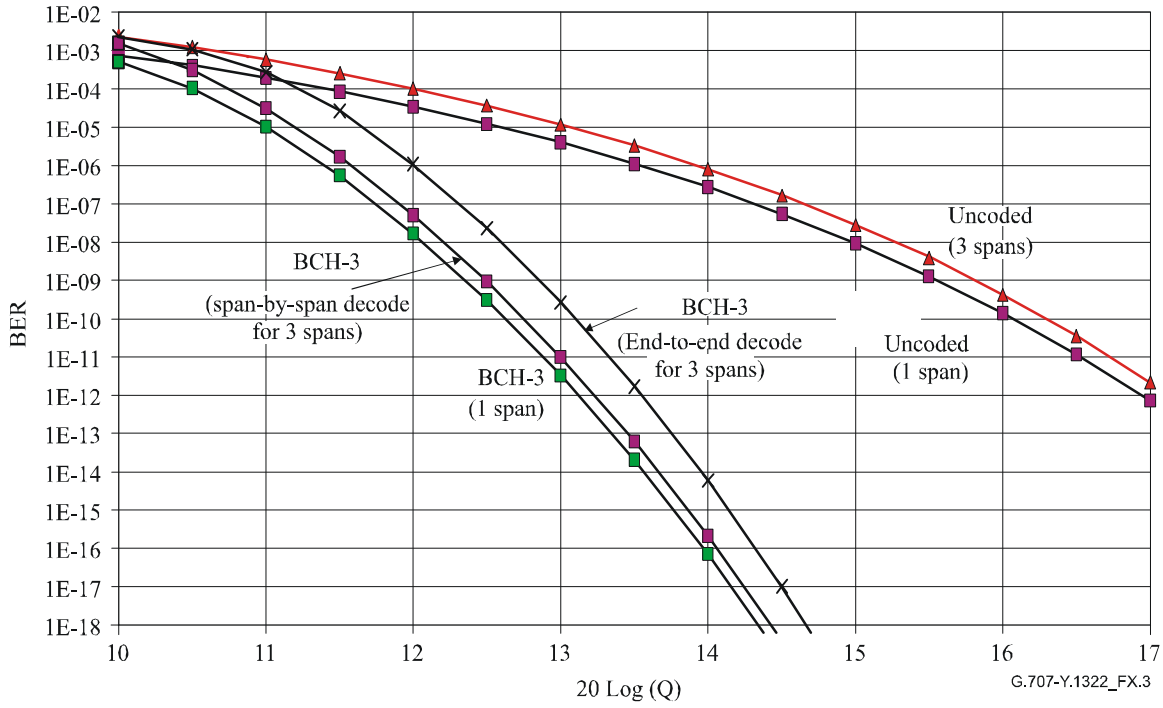


Figure X.3 – Comparison of end-to-end versus span-by-span FEC

For BER_{Input} above 10^{-3}, the probability of incorrect decoding (an incorrect decoding occurs when the decoder attempts correction but acts incorrectly because the error pattern is beyond its ability to correct) is no longer negligible and makes the previous indication of BER_{Output} inaccurate. In such cases, the BER_{Output} versus BER_{Input} curves are even located below the non-corrected curve in Figure X.1.

Appendix XI

Nominal justification ratios for asynchronous mapping of ODU1 into C-4-17 and ODU2 into C-4-68

(This appendix does not form an integral part of this Recommendation)

Appendix V/G.709/Y.1331 provides a relation between justification ratio and frequency offset, for the case of either CBRx or ODUk mapped into ODUn (n > k). Following the notation there, let α be the justification ratio, i.e., the average number of justifications per C-4-Xc frame; also, as is done there, let positive α correspond to negative justification and negative α correspond to positive justification. Then $0 \le \alpha \le 45$ for mapping ODU1 into C-4-17 and $0 \le \alpha \le 180$ for mapping ODU2 into C-4-68. In addition, as is done in Appendix V/G.709/Y.1331, define the following notation:

- N number of fixed stuff bytes in the C-4-Xc payload area
- S nominal ODUk client rate (bytes/s)
- T nominal C-4-Xc frame period(s)
- y_c client (ODUk) frequency offset (fraction)
- y_s server (C-4-Xc) frequency offset (fraction)
- N_f average number of client bytes mapped into a C-4-Xc frame, for the particular frequency offsets (averaged over a large number of frames)

(Note that in Appendix V/G.709/Y.1331, a quantity p, representing the fraction of the payload area for the client in question, was defined. Here, $p = 1$ because there is only one client being mapped; i.e., there is no possible multiplexing as there was in Appendix V/G.709/Y.1331.)

Then N_f is given by:

$$N_f = ST\frac{1+y_c}{1+y_s} \tag{XI-1}$$

For frequency offsets small compared to 1, this may be approximated

$$N_f = ST(1+y_c-y_s) \equiv ST\beta \tag{XI-2}$$

The quantity β-1 is the net frequency offset due to client and server frequency offset.

Now, the average number of client bytes mapped into a C-4-Xc frame is also equal to the total number of bytes in the payload area available to the client for data mapping (i.e., excluding any fixed stuff bytes (N)), plus the average number of bytes stuffed for this client over a very large number of frames. The latter is equal to the justification ratio. The former is equal to:

Number of data bytes in payload area for ODU1 mapped into C-4-17

(51 data bytes/subblock)(17 subblocks/block)(5 blocks/row)(9 rows/frame) = 39 015 data bytes/frame.

Number of data bytes in payload area for ODU2 mapped into C-4-68

(67 data bytes/subblock)(13 subblocks/block)(20 blocks/row)(9 rows/frame) = 156 780 data bytes/frame.

Combining the above with Equations (XI-1) and (XI-2) produces:

ODU1 mapped into C-4-17

$$ST\beta = \alpha + 39015 \tag{XI-3}$$

ODU2 mapped into C-4-68

$$ST\beta = \alpha + 156780 \tag{XI-4}$$

The nominal stuff ratio occurs when the frequency offsets are zero, i.e., when $\beta = 1$. We now set $\beta = 1$ and solve for α for each case.

ODU1 mapped into C-4-17

The quantity *ST* is the nominal number of ODU1 bytes in the nominal C-4-17 frame period. The latter is equal to 125 μs. The former is equal to (239/238)(2.48832 × 10^9 bits/s)(1 byte/8 bits). Then

$$\begin{aligned}
\alpha &= (125\times10^{-6})\left(\frac{239}{238}\right)\left(\frac{2.48832\times10^{9}}{8}\right) - 39015 \\
&= \left(\frac{239}{238}\right)(38880) - 39015 \\
&= \frac{(239)(38880) - (238)(39015)}{238} \\
&= \frac{6750}{238} \\
&= \frac{3375}{119} \\
&\approx 28.361345
\end{aligned} \tag{XI-5}$$

Then, on average, there are approximately 28.361345 negative justifications per C-4-17 frame out of a total possible 45. The long-run average fraction of justification opportunities for which there is a justification is equal to the above, divided by 45 (denote this quantity by α')

$$\alpha' = \frac{3375}{(119)(45)} = \frac{75}{119} \approx 0.630252100840 \tag{XI-6}$$

ODU2 mapped into C-4-68

The quantity *ST* is the nominal number of ODU2 bytes in the nominal C-4-68 frame period. The latter is equal to 125 μs. The former is equal to (239/237)(9.95328 × 10^9 bits/s)(1 byte/8 bits). Then

$$\begin{aligned}
\alpha &= (125\times10^{-6})\left(\frac{239}{237}\right)\left(\frac{9.95328\times10^{9}}{8}\right) - 156780 \\
&= \left(\frac{239}{237}\right)(155520) - 156780 \\
&= \frac{(239)(155520) - (237)(156780)}{237} \\
&= \frac{12420}{237} \\
&= \frac{4140}{79} \\
&\approx 52.405063
\end{aligned} \tag{XI-7}$$

Then, on average, there are approximately 52.405063 negative justifications per C-4-68 frame out of a total possible 180. The long-run average fraction of justification opportunities for which there is a justification is equal to the above, divided by 180 (denote this quantity by α')

$$\alpha' = \frac{4140}{(79)(180)} = \frac{23}{79} \approx 0.291139240506 \qquad \text{(XI-8)}$$

Appendix XII

Consideration on 10 Gbit/s Ethernet WAN clock accuracy

(This appendix does not form an integral part of this Recommendation)

In IEEE 802.3ae, IEEE has defined a 10 Gbit/s Ethernet WAN interface. This interface is basically an STM-64 with a VC-4-64c, and the Ethernet MAC mapped into the VC-4-64c using a 64B/66B coding (see Annex F).

IEEE 802.3ae defines a clock accuracy of ±20 ppm for the 10 Gbit/s WAN signal, while a clock accuracy of ±4.6 ppm is required for SDH signals (except for the MS-AIS case). A VC-4-64c with ±20 ppm clock accuracy may result in excessive AU pointer justifications, which results in alarms if pointer adjustment monitoring is active.

The IEEE 802.3ae interface can be supported by an SDH network if the clock accuracy is improved to meet the SDH ±4.6 ppm requirement. No other changes are required. Alternately, a clock alignment can be performed at the entrance to a SDH network. The 10 Gbit/s WAN signal is terminated in this case. The 64B/66B data stream is extracted and re-inserted into a new VC-4-64c (see Annex F) generated by the SDH equipment clock. Clock adaptation is performed by insertion or deletion of idle characters as defined in IEEE 802.3ae, section 49.2.4.7.

Appendix XIII

Example LCAS control packet CRC calculations

(This appendix does not form an integral part of this Recommendation)

XIII.1 Example of CRC-8 computation for LCAS and virtual concatenation carried in the H4 byte (i.e., VC-3-Xv and VC-4-Xv)

	H4[1-4] function	Most significant nibble H4[1-4]				Least significant nibble H4[5-8]				H4[5-8] value	
		bit 1	bit 2	bit 3	bit 4	bit 5	bit 6	bit 7	bit 8		
MF-2 counter = 201	Member Status [72-79]	0	1	1	0	1	0	0	0	8	LCAS control packet
		1	0	0	0	1	0	0	1	9	
	H4[1-3] = Reserved ('0') H4[4] = RS-Ack ('1')	0	0	0	1	1	0	1	0	10	
	Reserved ('0')	0	0	0	0	1	0	1	1	11	
		0	0	0	0	1	1	0	0	12	
		0	0	0	0	1	1	0	1	13	
	Sequence number	0	0	0	1	1	1	1	0	14	
	(19 = 13_{HEX})	0	0	1	1	1	1	1	1	15	
MF-2 counter = 202	MF-2 counter	1	1	0	0	0	0	0	0	0	
	(202 = CA_{HEX})	1	0	1	0	0	0	0	1	1	
	Control word ('NORM')	0	0	1	0	0	0	1	0	2	
	H4[1-3] = Reserved ('0') H4[4] = GID ('1')	0	0	0	1	0	0	1	1	3	
	Reserved ('0')	0	0	0	0	0	1	0	0	4	
		0	0	0	0	0	1	0	1	5	
	CRC-8 of previous	0	1	1	1	0	1	1	0	6	
	14 H4[1-4] nibbles	1	1	0	0	0	1	1	1	7	
	Member status [80-87]	0	0	0	0	1	0	0	0	8	LCAS control packet
		1	0	0	1	1	0	0	1	9	
	H4[1-3] = Reserved ('0') H4[4] = RS-Ack ('1')	0	0	0	1	1	0	1	0	10	
	Reserved ('0')	0	0	0	0	1	0	1	1	11	
		0	0	0	0	1	1	0	0	12	
		0	0	0	0	1	1	0	1	13	
	Sequence number	0	0	0	1	1	1	1	0	14	
	(19 = 13_{HEX})	0	0	1	1	1	1	1	1	15	
MF-2 counter = 203	MF-2 counter	1	1	0	0	0	0	0	0	0	
	(203 = CB_{HEX})	1	0	1	1	0	0	0	1	1	
	Control word ('NORM')	0	0	1	0	0	0	1	0	2	
	H4[1-3] = Reserved ('0') H4[4] = GID ('0')	0	0	0	0	0	0	1	1	3	
	Reserved	0	0	0	0	0	1	0	0	4	
		0	0	0	0	0	1	0	1	5	
	CRC-8 of previous	0	0	1	1	0	1	1	0	6	
	14 H4[1-4] nibbles	1	0	0	1	0	1	1	1	7	
	Member status [88-95]	0	0	0	0	1	0	0	0	8	
		0	0	0	0	1	0	0	1	9	

Figure XIII.1 – High order LCAS CRC calculation example

XIII.2 Example of CRC-3 computation for LCAS and virtual concatenation carried in bit 2 of the K4 byte (i.e., VC-2-Xv, VC-12-Xv and VC-11-Xv)

<table>
<tr><td>1</td><td>2</td><td>3</td><td>4</td><td>5</td><td>6</td><td>7</td><td>8</td><td>9</td><td>10</td><td>11</td><td>12</td><td>13</td><td>14</td><td>15</td><td>16</td><td>17</td><td>18</td><td>19</td><td>20</td><td>21</td><td>22</td><td>23</td><td>24</td><td>25</td><td>26</td><td>27</td><td>28</td><td>29</td><td>30</td><td>31</td><td>32</td></tr>
<tr><td colspan="32">K4[1] 32-bit multiframe structure</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td colspan="8">Signal label extension</td><td>0</td><td colspan="6">Unused</td><td>0</td><td colspan="8">Unused</td></tr>
<tr><td colspan="32">K4[2] 32-bit multiframe structure</td></tr>
<tr><td colspan="5" rowspan="2">Multiframe-2 indicator</td><td colspan="6" rowspan="2">Sequence number</td><td colspan="27">LCAS control information</td></tr>
<tr><td colspan="8">CTRL</td><td>GID</td><td colspan="6">Reserved "0000"</td><td>RS-Ack</td><td colspan="8">Member status</td><td>C_1</td><td>C_1</td><td>C_3</td></tr>
<tr><td colspan="5" rowspan="2">Example:</td><td colspan="6" rowspan="2">MF-2 = 7, sequence number = 22, CTRL = NORM, member status of members 56-63</td><td colspan="27" rowspan="2"></td><td colspan="3" rowspan="2">CRC-3</td></tr>
<tr><td colspan="8">0</td><td>0</td><td colspan="6">0</td><td>1</td><td colspan="8">0</td></tr>
<tr><td colspan="5">0</td><td colspan="6">0</td><td colspan="8">1</td><td>1</td><td colspan="6">0</td><td>1</td><td colspan="8">0</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">MF-2 = 8, sequence number = 22, CTRL = NORM, member status of members 0-7</td></tr>
<tr><td colspan="5">0</td><td colspan="6">1</td><td colspan="8">0</td><td>0</td><td colspan="6">0</td><td>1</td><td colspan="8">0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td colspan="32">MF-2 = 9, sequence number = 22, CTRL = NORM, member status of members 8-15</td></tr>
<tr><td colspan="5">0</td><td colspan="6">1</td><td colspan="8">0</td><td>0</td><td colspan="6">0</td><td>1</td><td colspan="8">0</td><td>1</td><td>0</td></tr>
<tr><td colspan="32">MF-2 = 10, sequence number = 22, CTRL = NORM, member status of members 16-23</td></tr>
<tr><td colspan="5">0</td><td colspan="6">1</td><td colspan="8">0</td><td>0</td><td colspan="6">0</td><td>1</td><td colspan="8">0</td><td>1</td><td>0</td><td>1</td></tr>
</table>

Figure XIII.2 – Lower order LCAS control packet examples including the CRC-3

Appendix XIV

Mapping serial data into a VCG

(This appendix does not form an integral part of this Recommendation)

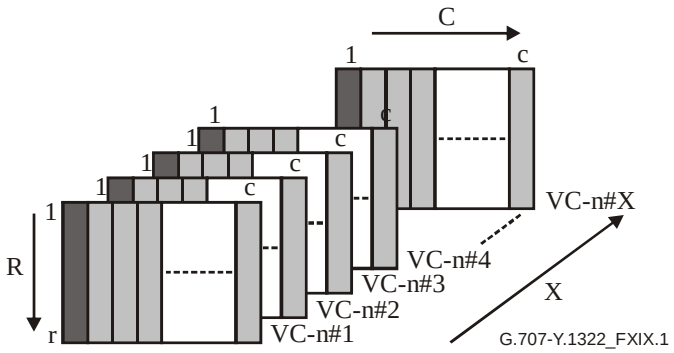


Figure XIV.1 – VCAT mapping order

Serial data is mapped into a VCG on an octet-by-octet basis in the following order:

1) Xth VC;
2) Cth column;
3) Rth row;

i.e., octet #1 maps into VC #1, column #1, row #1
octet #2 maps into VC #2, column #1, row #1
octet #3 maps into VC #3, column #1, row #1
.
.
octet #X maps into VC #X, column #1, row #1
octet #(X+1) maps into VC #1, column #2, row #1
octet #(X+2) maps into VC #2, column #2, row #1
octet #(X+3) maps into VC #3, column #2, row #1
.
.
octet #(X+X) maps into VC #X, column #2 of row #1
etc., until X*C*R octets are mapped, then the sequence is repeated.

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ITU-T Y-SERIES RECOMMENDATIONS

GLOBAL INFORMATION INFRASTRUCTURE, INTERNET PROTOCOL ASPECTS AND NEXT-GENERATION NETWORKS

GLOBAL INFORMATION INFRASTRUCTURE	
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