INTERNATIONAL TELECOMMUNICATION UNION

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DATA COMMUNICATION OVER THE TELEPHONE NETWORK

9600 BITS PER SECOND MODEM STANDARDIZED FOR USE ON POINT-TO-POINT 4-WIRE LEASED TELEPHONE-TYPE CIRCUITS

ITU-T Recommendation V.29

(Extract from the *Blue Book*)

NOTES

1 ITU-T Recommendation V.29 was published in Fascicle VIII.1 of the *Blue Book*. This file is an extract from the *Blue Book*. While the presentation and layout of the text might be slightly different from the *Blue Book* version, the contents of the file are identical to the *Blue Book* version and copyright conditions remain unchanged (see below).

2 In this Recommendation, the expression "Administration" is used for conciseness to indicate both a telecommunication administration and a recognized operating agency.

Recommendation V.29

9600 BITS PER SECOND MODEM STANDARDIZED FOR USE ON POINT-TO-POINT 4-WIRE LEASED TELEPHONE-TYPE CIRCUITS

(Geneva, 1976; amended at Geneva, 1980, Malaga-Torremolinos, 1984, and at Melbourne, 1988)

1 Introduction

This modem is intended to be used primarily on special quality leased circuits, e.g. Recommendation M.1020 [1] or M.1025 [2] circuits but this does not preclude the use of this modem over circuits of lower quality at the discretion of the Administration concerned (see Notes 1 and 2).

On leased circuits, considering that there exist and will come into being many modems with features designed to meet the requirements of the Administrations and users, this Recommendation in no way restricts the use of any other modems.

The principal characteristics of this recommended modem for transmitting data at 9600 bits per second on leased circuits are as follows:

a) fallback rates of 7200 and 4800 bits per second;

b) capable of operating in a duplex or half-duplex mode with continuous or controlled carrier;

c) combined amplitude and phase modulation with synchronous mode of operation;

d) inclusion of an automatic adaptive equalizer;

e) optional inclusion of a multiplexer for combining data rates of 7200, 4800 and 2400 bits per second (see Note 3).

Note 1 - The principal use of this recommended modem is on 4-wire leased circuits. Other applications, such as stand-by operation on the switched network, should be points for further study.

The types of special quality circuits, e.g. M.1020 [1] or M.1025 [2] should be studied.

Note 2 - The values of some circuit characteristics, for example, noise and nonlinear distortion, are subject to further study.

Note 3 - When the multiplexer option is installed, provisions in § 12 may supersede provisions given in other sections.

Note 4 - Attention should be given to the selection of appropriate equalization techniques in the modem implementation, if acceptable performance on circuits conforming to Recommendation M.1025 is desired.

2 Line signals

2.1 The carrier frequency is to be 1700 ± 1 Hz. No separate pilot frequencies are provided. The power levels used will conform to Recommendation V.2.

2.2 *Signal space coding*

2.2.1 At 9600 bits per second, the scrambled data stream to be transmitted is divided into groups of four consecutive data bits (quadbits). The first bit (Q1) in time of each quadbit is used to determine the signal element amplitude to be transmitted. The second (Q2), third (Q3) and fourth (Q4) bits are encoded as a phase change relative to the phase of the immediately preceding element (see Table 1/V.29). The phase encoding is identical to Recommendation V.27.

The relative amplitude of the transmitted signal element is determined by the first bit (Q1) of the quadbit and the absolute phase of the signal element (see Table 2/V.29). The absolute phase is initially established by the synchronizing signal as explained in § 8 below.

Figure 1/V.29 shows the absolute phase diagram of transmitted signal elements at 9600 bits per second.

At the receiver the quadbits are decoded and the data bits are reassembled in correct order.

2.2.2 At the fallback rate of 7200 bits per second, the scrambled data stream to be transmitted is divided into groups of three consecutive data bits. The first data bit in time determines Q2 of the modulator quadbit. The second and third data bits determine Q3 and Q4 respectively of the modulator quadbit. Q1 of the modulator quadbit is a data ZERO for each signal element. Signal elements are determined in accordance with § 2.2.1 above. Figure 2/V.29 shows the absolute phase diagram of the transmitted signal elements at 7200 bits per second.

2.2.3 At the fallback rate of 4800 bits per second (see Table 3/V.29), the scrambled data stream to be transmitted is divided into groups of two consecutive data bits. The first data bit in time determines Q2 of the modulator quadbit and the second data bit determines Q3 of the modulator quadbit. Q1 of the modulator quadbit is a data ZERO for each signal element. Q4 is determined by inverting the modulo 2 sum of Q2 + Q3. The signal element is then determined in accordance with § 2.2.1 above. Figure 3/V.29 shows the absolute phase diagram of transmitted signal elements at 4800 bits per second.

The phase changes are identical with Recommendation V.26 (alternative A) and the amplitude is constant with a relative value of 3.

TABLE 1/V.29

Q2	Q3	Q4	Phase change (see Note)
0	0	1	0°
0	0	0	45°
0	1	0	90°
0	1	1	135°
1	1	1	180°
1	1	0	225°
1	0	0	270°
1	0	1	315°

Note - The phase change is the actual on-line phase shift in the transition region from the centre of one signalling element to the centre of the following signalling element.

TABLE 2/V.29

Absolute phase	Q1	Relative signal element amplitude
0°, 90°, 180°, 270°	0	3
	1	5
45°, 135°, 225°, 315°	0	$\sqrt{2}$
	1	$3\sqrt{2}$

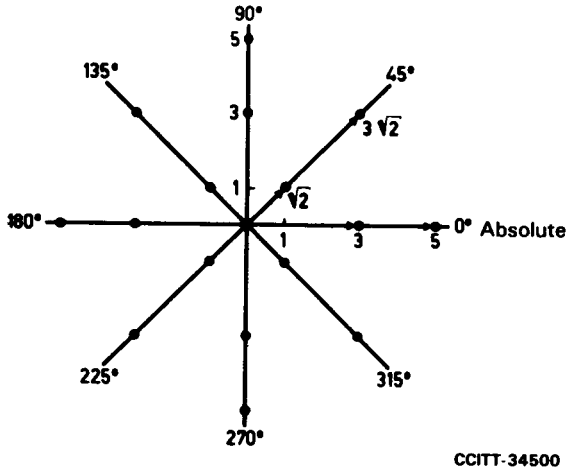

FIGURE 1/V.29

Signal space diagram at 9600 bit/s

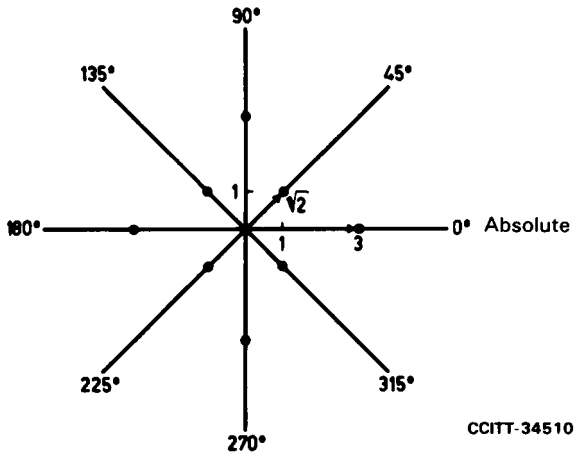

FIGURE 2/V.29

Signal space diagram at 7200 bit/s

TABLE 3/V.29

Data bits		Quadbits				Phase change
		Q1	Q2	Q3	Q4	
0	0	0	0	0	1	0°
0	1	0	0	1	0	90°
1	1	0	1	1	1	180°
1	0	0	1	0	0	270°

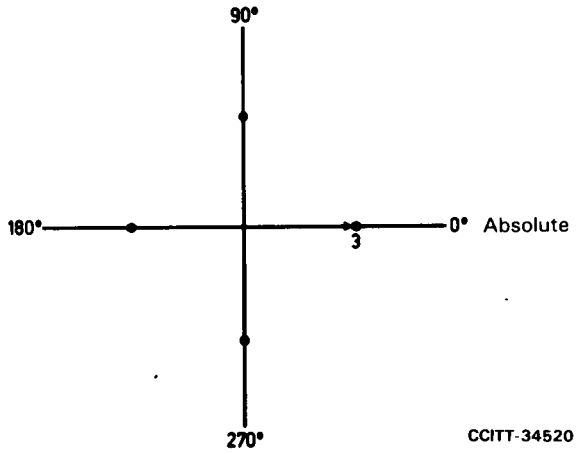

FIGURE 3/V.29

Signal space diagram at 4800 bit/s

3 Data signalling and modulation rates

The data signalling rates shall be 9600, 7200 and 4800 bits per second ± 0.01%. The modulation rate is 2400 bauds ± 0.01%.

4 Received signal frequency tolerance

The carrier frequency tolerance allowance at the transmitter is ± 1 Hz. Assuming a maximum frequency drift of ± 6 Hz in the connection between the modems, then the receiver must be able to accept errors of at least ± 7 Hz in the received signal frequency.

5 Interchange circuits

5.1 *List of interchange circuits* (Table 4/V.29)

TABLE 4/V.29

Interchange circuit (see Note 1)	
No.	Designation
102	Signal ground or common return
103	Transmitted data
104	Received data
105 (see Note 2)	Request to send
106	Ready for sending
107	Data set ready
109	Data channel received line signal detector
111 (see Note 3)	Data signalling rate selector (DTE source)
113	Transmitter signal element timing (DTE source)
114	Transmitter signal element timing (DTE source)
115	Receiver signal element timing (DCE source)
140 (see Note 4)	Loopback/Maintenance test
141 (see Note 4)	Local loopback
142	Test indicator

Note 1 - All essential interchange circuits and any others which are provided shall comply with the functional and operational requirements of Recommendation V.24. All interchange circuits provided shall be properly terminated in the data terminal equipment and in the data circuit-terminating equipment in accordance with the appropriate Recommendation for electrical characteristics (see § 6).

Note 2 - Not essential for continuous carrier operation.

Note 3 - A manual selector shall be implemented which determines the two data signalling rates selected by circuit 111. The manual selector positions shall be designated 9600/7200, 9600/4800 and 7200/4800. The ON condition of circuit 111 selects the higher data signalling rate and the OFF condition of circuit 111 selects the lower data signalling rate.

Note 4 - Interchange circuits 140 and 141 are optional.

5.2 *Threshold and response times of circuit 109*

5.2.1 *Threshold*

- greater than - 26 dBm: circuit 109 ON;
- less than -31 dBm: circuit 109 OFF.

The condition of circuit 109 for levels between -26 dBm and -31 dBm is not specified except that the signal detector shall exhibit a hysteresis action, such that the level at which the OFF to ON transition occurs is at least 2 dB greater than that for the ON to OFF transition.

5.2.2 *Response times*

- ON to OFF: 30 ± 9 ms;
- OFF to ON:

1) for initial equalization, circuit 109 must be ON prior to user data appearing on circuit 104;
2) for re-equalization during data transfer, circuit 109 will be maintained in the ON condition; during this period, circuit 104 may be clamped to the binary 1 condition;
3) after a line signal interruption that lasts more than the ON to OFF response time:
   a) when no new equalization is needed, 15 ± 10 ms,
   b) when a new equalization is needed, circuit 109 must be ON prior to user data appearing on circuit 104.

Response times of circuit 109 are the times that elapse between the connection or removal of a line signal to or from the modem receive line terminals and the appearance of the corresponding ON or OFF condition on circuit 109.

Note - Circuit 109 ON to OFF response time should be suitably chosen within the specified limits to ensure that all valid data bits have appeared on circuit 104.

5.3 *Response time for circuit 106*

The time between the OFF to ON transition of circuit 105 and the OFF to ON transition of circuit 106 shall be optionally 15 ms ± 5 ms or 253.5 ms ± 0.5 ms.

The short delay is used when circuit 105 does not control the transmitter carrier. The long delay is used when circuit 105 controls transmitter carrier and a synchronizing signal is initiated by the OFF to ON transition of circuit 105.

The time between the ON to OFF transition of circuit 105 and the ON to OFF transition of circuit 106 shall be suitably chosen to ensure that all valid signal elements have been transmitted.

5.4 *Fault condition of interchange circuits*

(See Recommendations V.28, § 7 for association of the receiver failure detection types.)

5.4.1 The DTE should interpret a fault condition on circuit 107 as an OFF condition using failure detection type 1.

5.4.2 The DCE should interpret a fault condition on circuits 105 and 108 as an OFF condition using failure detection type 1.

5.4.3 All other circuits not referred to above may use failure detection type 0 or 1.

6 Electrical characteristics of interchange circuits

Use of electrical characteristics conforming to Recommendation V.28 is recommended together with the connector pin assignment plan specified by ISO 2110.

Note - Manufacturers may wish to note that the long-term objective is to replace electrical characteristics specified in Recommendation V.28, and that Study Group XVII has agreed that the work shall proceed to develop a more efficient, all balanced, interface for the V-Series application which minimizes the number of interchange circuits.

7 Timing arrangements

Clocks should be included in the modem to provide the data terminal equipment with transmitter signal element timing, circuit 114, and receiver signal element timing, circuit 115. In this arrangement, the transmitter may either run as

an independent timing source or with loopback timing (transmit timing slaved to receive timing). Loopback timing may be desirable in some network applications. Alternatively, the transmitter signal element timing may be originated in the data terminal equipment and be transferred to the modem via interchange circuit 113.

8 Synchronizing signals

Transmission of synchronizing signals may be initiated by the modem or by the associated data terminal equipment. When circuit 105 is used to control the transmitter carrier the synchronizing signals are generated during the interval between the OFF to ON transition of circuit 105 and the OFF to ON transition of circuit 106. When the receiving modem detects a circuit condition which requires resynchronizing, it shall turn circuit 106 OFF and generate a synchronizing signal.

The synchronizing signals for all data signalling rates are divided into four segments as in Table 5/V.29.

TABLE 5/V.29

	Segment 1	Segment 2	Segment 3	Segment 4	Total of Segments 1, 2, 3 and 4
Type of line signal	No transmitted energy	Alternations	Equalizer conditioning pattern	Scrambled all binary ONEs	Total synchronizing signal
Number of symbol intervals	48	128	384	48	608
Approximate time in ms[a)]	20	53	160	20	253

a) Approximate times are provided for information only. The segment duration is determined by the exact number of symbol intervals.

8.1 Segment 2 of the synchronizing signal consists of alterations between two signal elements. The first signal element (A) transmitted has a relative amplitude of 3 and defines the absolute phase reference of 180°. The second signal element (B) transmitted depends on the data signalling rate. Figure 4/V.29 shows the B signal element at each of the data signalling rates. Segment 2 alternates ABAB...ABAB for 128 symbol intervals.

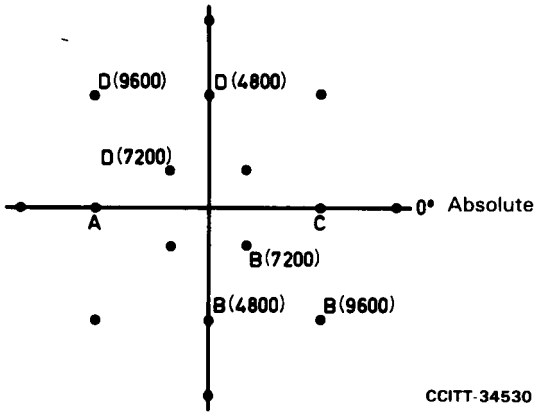

FIGURE 4/V.29

Signal space diagram showing synchronizing signal points

8.2 Segment 3 of the synchronizing signals transmits two signal elements according to an equalizer condition pattern. The first signal element (C) has a relative amplitude of 3 and absolute phase of 0°. The second signal element (D) transmitted depends on the data signalling rate. Figure 4/V.29 shows the D signal element at each of the data signalling rates. The equalizer conditioning pattern is a pseudo-random sequence generated by the polynomial:

$$1 + x^{-6} + x^{-7}$$

Each time the pseudo-random sequence contains a ZERO, point C is transmitted. Each time the pseudo-random sequence contains a ONE, the point D is transmitted. Segment 3 begins with the sequence CDCDCDC.... according to the pseudo-random sequence and continues for 384 symbol intervals. The detailed pseudo-random sequence generation is described in Appendix I.

8.3 Segment 4 commences transmission according to the encoding described in § 2.2 above with continuous binary ONEs applied to the input of the data scrambler. Segment 4 duration is 48 symbol intervals. At the end of Segment 4, circuit 106 is turned ON and user data are applied to the input of the data scrambler.

9 Scrambler

A self-synchronizing scrambler/descrambler having the generating polynomial $1 + x^{-18} + x^{-23}$, shall be included in the modem.

At the transmitter the scrambler shall effectively divide the message polynomial, of which the input data sequence represents the coefficients in descending order, by the scrambler generating polynomial to generate the transmitted sequence. At the receiver the received polynomial, of which the received data sequence represents the coefficients in descending order, shall be multiplied by the scrambler generating polynomial to recover the message sequence.

The detailed scrambling and descrambling processes are described in Appendix II.

10 Equalizer

An automatic adaptive equalizer shall be provided in the receiver.

The receiver shall incorporate a means of detecting loss of equalization and initiating a synchronizing signal sequence in its associated local transmitter.

The receiver shall incorporate a means of detecting a synchronizing signal sequence from the remote transmitter and initiating a synchronizing signal sequence in its associated local transmitter, which may be initiated at any time during the reception of the synchronizing signal sequence, regardless of the state of circuit 105.

Either modem can initiate the synchronizing signal sequence. The synchronizing signal is initiated when the receiver has detected a loss of equalization or when circuit 105 OFF to ON transition occurs in the carrier controlled mode, as described in § 5.3 above. Having initiated a synchronizing signal, the modem expects a synchronizing signal from the remote transmitter.

If the modem does not receive a synchronizing signal from the remote transmitter within a time interval equal to the maximum expected two-way propagation delay, it transmits another synchronizing signal. A time interval of 1.2 seconds is recommended.

If the modem fails to synchronize on the received signal sequence, it transmits another synchronizing signal.

If a modem receives a synchronizing signal when it had not initiated a synchronizing signal and the receiver properly synchronizes, it returns only one synchronizing sequence.

Note - Manufacturers should note that where there is a likelihood that double-hop satellite connections may be encountered, a more appropriate value for this timer may be in the range of 1.8 to 2.6 seconds.

11 The following information is provided to assist equipment manufacturers:

- The data modem should have no adjustment for send level or receive sensitivity under the control of the operator.
- The transmitter energy spectrum shall be shaped in such a way that with continuous binary ONEs applied to the input of the scrambler the resulting transmitted spectrum shall have a substantially linear phase characteristic over the band of 700 Hz to 2700 Hz and the energy density at 500 Hz and 2900 Hz shall be attenuated 4.5 dB ± 2.5 dB with respect to the maximum energy density between 500 Hz and 2900 Hz.

12 **Multiplexing** (see Table 6/V.29)

A multiplexing option may be included to combine 7200, 4800 and 2400 bits per second data subchannels into a single aggregate bit stream for transmission. Identification of the individual data subchannels is accomplished by assignment to the modulator quadbit as defined in § 2.2 above.

12.1 *List of interchange circuits concerned with multiplexer ports* (see Table 7/V.29)

12.2 *Transmit buffers*

In the transmitter of each multiplexer port, there shall be a data buffer of suitable capacity. In this way, both phase variations and, within certain limits, frequency deviations are absorbed. The buffer shall be initialized when the OFF to ON transition of circuit 105 occurs and may be repositioned in the event of the buffer overflow.

Note - The buffer may be initialized upon the DCE sending a synchronizing signal.

12.3 *Transmit port timing arrangements*

Table 8/V.29 shows all possible combinations of port and main DCE transmit timing clock arrangements.

12.4 *Port simulated circuit 105 to circuit 109 operation (optional)*

Simulated circuits 105 to 109 operation on an individual port interface may optionally be provided in accordance with Recommendation V.13.

Note - There may be equipment in the field that accomplishes simulated 105 to 109 operation in a different way. In this case the entire DCE shall operate in continuous carrier mode.

12.5 *Response times for circuit 106*

Circuit 105 to circuit 106 delays on individual ports of the multiplexer are not necessarily those specified in § 5.3. Other suitable delays may be needed to handle simulated circuit 105 to circuit 109 operations.

TABLE 6/V.29

Aggregate data rate	Multiplex configuration	Sub-channel data rate	Multiplex channel	Modulator bits			
				Q1	Q2	Q3	Q4
9600 bits/s	1	9600	A	X	X	X	X
	2	7200 2400	A B	X	X	X	X
	3	4800 4800	A B	X	X	X	X
	4	4800 2400 2400	A B C	X	X	X	X
	5	2400 2400 2400 2400	A B C D	X	X	X	X
7200 bit/s	6	7200	A		X	X	X
	7	4800 2400	A B		X	X	X
	8	2400 2400 2400	A B C		X	X	X
4800 bit/s	9	4800	A		X	X	
	10	2400 2400	A B		X	X	

Note - When more than one modulator bit is assigned to a sub-channel, the first bit in time of the sub-channel is assigned to the first bit in time (Q1) of the modulator.

TABLE 7/V.29

Interchange circuits (see Note 1)		Port A	Ports B, C, D
No.	Designation		
102	Signal ground or common return	X	X
103	Transmitted data	X	X
104	Received data	X	X
105	Request to send	X (see Note 2)	X (see Note 2)
106	Ready for sending	X (see Note 3)	X (see Note 3)
107	Data set ready	X	X
109	Data channel received line signal detector	X	X
111	Data signalling rate selector (DTE source)	X (see Note 4)	
113	Transmitter signal element timing (DTE source)	X	X
114	Transmitter signal element timing (DCE source)	X	X
115	Receiver signal element timing (DCE source)	X	X
140	Loopback/Maintenance test	X (see Note 5)	X (see Note 5)
141	Local loopback	X (see Notes 5 and 6)	
142	Test indicator	X (see Note 7)	X (see Note 7)

Note 1 - All essential interchange circuits and any others which are provided shall comply with the functional and operational requirements of Recommendation V.24. All interchange circuits indicated by X shall be properly terminated in the data terminal equipment and in the data circuit-terminating equipment in accordance with the appropriate Recommendation for electrical characteristics (see § 6).

Note 2 - Circuit 105 is not necessary for continuous carrier transmission. The transmitted line signal will not be controlled by this interchange circuit. If needed, circuit 105 (when the multiplexer is present) is used to control circuit 109 at the remote DCE. See § 12.4 below.

Note 3 - During the synchronization process of the main DCE, the OFF condition of circuit 106 is signalled at all port interfaces.

Note 4 - Circuit 111 is optionally present on Port A. If present, circuit 111 is activated in multiplexer configurations 1, 6 and 9 in the same way as if no multiplexer were present.

Note 5 - Circuits 140 and 141 are optional.

Note 6 - Circuit 141 is present only on Port A. When used in multiplexer configurations other than configurations 1, 6 or 9, the looping occurs on all ports.

Note 7 - Circuit 142 is present on all ports of the multiplexer, but may be activated on an individual port basis for individual port tests. All are activated simultaneously for entire DCE tests.

TABLE 8/V.29

Source of port transmitter signal element timing (used to clock in circuit 103)	Source of DCE internal transmitter element timing (internal transmit clock)	Port transmit buffer
114 (DCE source)	Internal (Independent timing)	Not required
	External[a] (Circuit 113 of selected port)	Not required
	Receiver timing (Loopback timing)	Not required
113 (DTE source)[a]	Internal (Independent timing)	Required
	External[a] (Circuit 113 of selected port)	Required for all ports except port supplying circuit 113 to DCE
	Receiver timing (Loopback timing)	Required

[a] In these applications a source could also be another DCE.

APPENDIX I

(to Recommendation V.29)

Details of the pseudo-random sequence generator

The equalizer conditioning pattern is determined by a pseudo-random sequence generated by the polynomial $1 + x^{-6} + x^{-7}$. Figure I-1/V.29 shows a suitable implementation.

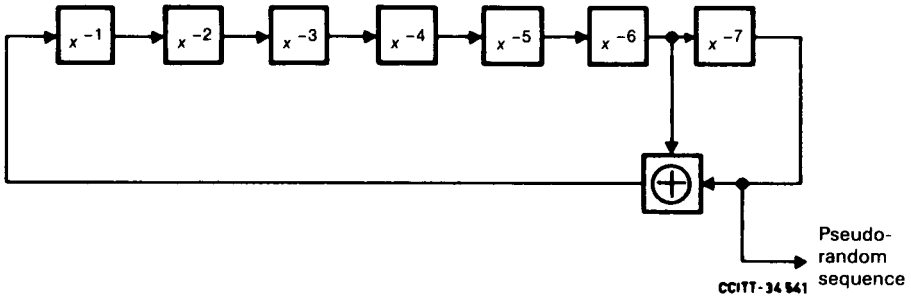

FIGURE I-1/V.29

The initial condition of the generator is 0101010. The generator clock is at the symbol rate (2400 symbols per second). The first four conditions of the generator are:

- initial condition: 0101010
- after first shift: 1010101
- after second shift: 1101010
- after third shift: 1110101

APPENDIX II

(to Recommendation V.29)

Detailed scrambling and descrambling process

II.1 *Scrambling*

The message polynomial is divided by the generating polynomial $1 + x^{-18} + x^{-23}$ (see Figure II-1/V.29). The coefficients of the quotient of this division taken in descending order form the data sequence to be transmitted. In order to ensure that proper starting sequence is generated, the shift register is fed with "0" during segments 1, 2 and 3. During segment 4 and normal data transmission it is fed with scrambled data D_s (input data D_i being "1" during segment 4).

$$D_s = D_i \oplus D_s x^{-18} \oplus D_s x^{-23}$$

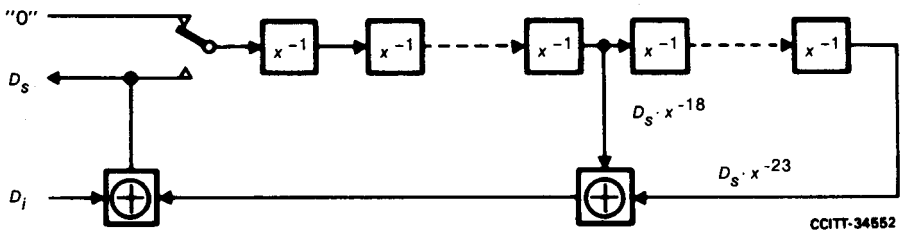

FIGURE II-I/V.29

II.2 *Descrambling*

The polynomial represented by the received sequence is multiplied by the generating polynomial (Figure II-2/V.29) to form the recovered message polynomial. The coefficients of the recovered polynomial, taken in descending order, form the output data sequence D_o.

$$D_o = D_i = D_s (1 \oplus x^{-18} \oplus x^{-23})$$

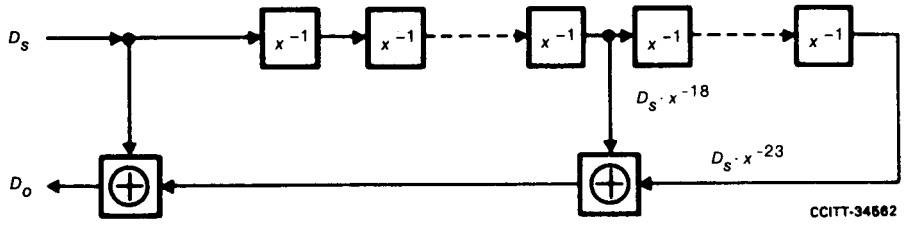

FIGURE II-2/V.29

II.3 *Elements of the scrambling process*

The polynomial $1 + x^{-18} + x^{-23}$ generates a pseudo-random sequence of length $2^{23} - 1 = 8{,}388{,}607$. This long sequence does not require the use of a guard polynomial to prevent the occurrence of repeat patterns and is particularly simple to implement with integrated circuits.

References

[1] CCITT Recommendation *Characteristics of special quality international leased circuits with special bandwidth conditioning,* Vol. IV, Rec. M.1020.

[2] CCITT Recommendation *Characteristics of special quality international leased circuits with basic bandwidth conditioning,* Vol. IV, Rec. M.1025.