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O.172
Amendment 2
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SERIES O: SPECIFICATIONS OF MEASURING EQUIPMENT

Equipment for the measurement of digital and analogue/digital parameters

Jitter and wander measuring equipment for digital systems which are based on the synchronous digital hierarchy (SDH)

Amendment 2: Alternative clock and jitter generation and a new verification method for STM-256 reference transmitter intrinsic jitter

Recommendation ITU-T O.172 (2005) – Amendment 2

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Alternative clock and jitter generation and a new verification method for STM-256 reference transmitter intrinsic jitter

Summary

Amendment 2 to Recommendation ITU-T O.172 contains an alternative implementation of clock and jitter generation for Appendix VII and a new verification method for the reference transmitter intrinsic jitter for STM-256, as Appendix IX.

History

Edition	Recommendation	Approval	Study Group
1.0	ITU-T O.172	1999-03-26	4
2.0	ITU-T O.172	2001-03-15	4
2.1	ITU-T O.172 (2001) Amend. 1	2003-03-29	4
3.0	ITU-T O.172	2005-04-13	4
3.1	ITU-T O.172 (2005) Amend. 1	2008-06-29	4
3.2	ITU-T O.172 (2005) Amend. 2	2010-07-29	15

FOREWORD

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As of the date of approval of this Recommendation, ITU had not received notice of intellectual property, protected by patents, which may be required to implement this Recommendation. However, implementers are cautioned that this may not represent the latest information and are therefore strongly urged to consult the TSB patent database at http://www.itu.int/ITU-T/ipr/.

CONTENTS

Page

Recommendation ITU-T O.172

Jitter and wander measuring equipment for digital systems which are based on the synchronous digital hierarchy (SDH)

Amendment 2

Alternative clock and jitter generation and a new verification method for STM-256 reference transmitter intrinsic jitter

1)   Clause 8.5, minimum jitter/wander generation capability

Replace Table 3 of clause 8.5 with the following table:

Table 3 – Minimum amplitude for adjustable generated jitter/wander amplitude versus jitter/wander frequency for SDH line signals

Signal	Minimum peak-to-peak jitter/wander amplitude [UIpp]					Jitter/wander frequency breakpoints [Hz]									
	A_0	A_1	A_2	A_3	A_4	f_0	f_{12}	f_{11}	f_{10}	f_9	f_8	f_1	f_2	f_3	f_4
STM-0e, STM-0	*	*	20	2	0.2	*	*	*	*	10	30	300	2 k	20 k	400 k
STM-1e, STM-1	3600	400	50	2	0.2	12 μ	178 μ	1.6 m	15.6 m	125 m	19.3	500	6.5 k	65 k	1.3 M
STM-4	14400	1600	200	2	0.2	12 μ	178 μ	1.6 m	15.6 m	125 m	9.65	1 k	25 k	250 k	5 M
STM-16	57600	6400	800	2	0.2	12 μ	178 μ	1.6 m	15.6 m	125 m	12.1	5 k	100 k	1 M	20 M
STM-64	230400	25600	3200	2	0.2	12 μ	178 μ	1.6 m	15.6 m	125 m	12.1	20 k	400 k	4 M	80 M
STM-256	FFS	FFS	12800	8	0.2	FFS	FFS	FFS	FFS	10	50	80 k	400 k	16 M	320 M
NOTE 1 – Values denoted by "*" are undefined.															
NOTE 2 – Values are based on the requirements of Rec. ITU-T G.825 [13].															
NOTE 3 – Values for STM-0 are based on the requirements of ANSI T1.105.03 [21].															
NOTE 4 – FFS denotes that the value is for further study.															

2)   Clause VII.1

a)   Replace the second paragraph of clause VII.1 with the following text:

The scheme uses a high-quality optical transmitter and pattern generator with minimal pattern dependent jitter at the line rate under test. A target would be less than 10 mUI peak-peak measured in bandwidth f_1-f_4. A generic jitter modulator is also described with the capability to generate pulse sinusoidal jitter. Both techniques can be verified with general purpose test equipment. The method described in Appendix VIII or that of Appendix IX may be used to verify the intrinsic jitter of the optical pattern generator for STM-16/64. In the case of STM-256, the method described in Appendix IX may be used to verify the intrinsic jitter of the reference transmitter.

b)   Replace Note 1 of the paragraph below Table VII.1 with the following text:

NOTE 1 – The error associated with the intrinsic jitter of the reference transmitter for STM-16/64 is verified as described in Appendix VIII or Appendix IX. The error associated with the intrinsic jitter of the reference transmitter for STM-256 is verified as described in Appendix IX.

3)   Clause VII.2

a)   Replace the second and third paragraphs of clause VII.2 with the following text:

Figures VII.2, VII.2a, VII.3 and VII.4 are example implementations of the generic test system in Figure VII.1. These illustrate potential means to produce independently verifiable bursts of clock jitter and a means of eliminating data jitter from an optical pattern, these do not restrict other implementation methods.

One example block diagram of the clock section is shown in Figure VII.2. This is implemented using two high quality synthesizers, Oscillator 1 and Oscillator 2, to generate the line rate clock and sinusoidal jitter phase modulation. The relative amplitude levels of these oscillators will determine the jitter amplitude generated, while the relative frequencies determine the jitter modulation. For example, if Oscillator 1 is set to the line rate clock, and Oscillator 2 to the line rate plus (or minus) an offset, the sinusoidal phase modulation will be generated at the offset frequency, on the line clock.

b)   Add the following new paragraph and figure in clause VII.2, below Figure VII.2:

Figure VII.2a below shows an alternative implementation of the clock and jitter generation. The pulse generator and oscillator 2 in Figure VII.2 could be replaced by an arbitrary waveform generator (AWG) supporting sinusoidal pulses corresponding to Table VII.1.
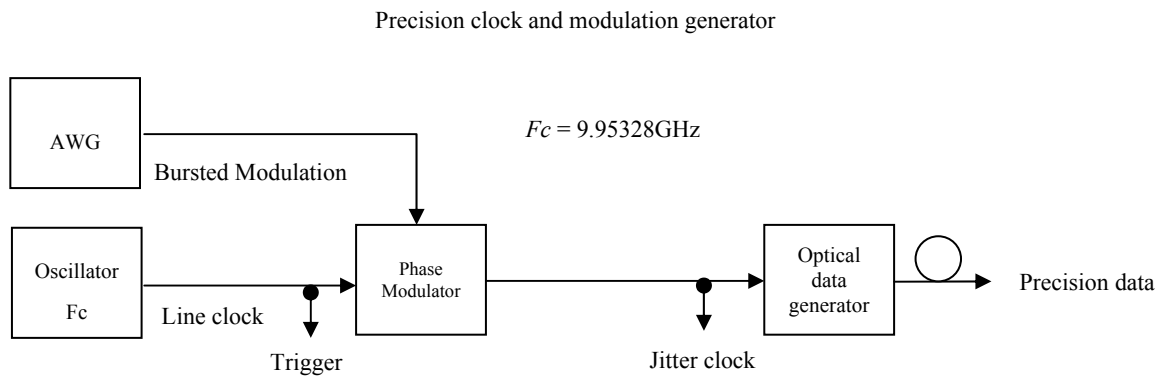
Precision clock and modulation generator

Figure VII.2a – Alternative clock and jitter generation block diagram

4)   New Appendix IX

Add the following new appendix:

Appendix IX

Method for characterization of STM-256 reference transmitter intrinsic jitter

(This appendix does not form an integral part of this Recommendation)

This appendix describes the intrinsic jitter verification method for the reference transmitter described in Appendix VII, and is especially suitable for STM-256 but can be used for STM-16/64. Appendix VIII is suitable for the intrinsic jitter verification method for the reference transmitter for only STM-16/64.

IX.1 Method

This verification method estimates the intrinsic jitter of the reference transmitter assuming that the pattern dependent jitter (PDJ) and random jitter (RJ) of the reference transmitter and the intrinsic jitter of the jitter measurement device are not correlated with each other.

The verification method consists of two steps. In step 1, the RJ and PDJ suppression ratio of the reference transmitter are evaluated by a spectrum analyser or a phase noise measurement device. In step 2, the intrinsic jitter including the PDJ and the RJ of the reference transmitter are estimated from the measurement result of the jitter measurement device.

IX.1.1 Step 1: Measurement of RJ and PDJ suppression ratio

1)   The set-up is shown in Figure IX.1. Here, the block diagram of the reference transmitter to be verified is based on the block diagram shown in Figure VII.3. The oscillator in Figure IX.1 outputs the 40-GHz line clock. This oscillator corresponds to Oscillator 1 in Figure VII.2. The clock modulator in Figure IX.1 corresponds to the other modulation functions of Figure VII.2. Note that the following two internal connections of the reference transmitter in Figure IX.1 are changed from those in Figure VII.3 in order to evaluate the reference transmitter intrinsic jitter. The input of Phase adjust is just connected with the oscillator output. The output of the data modulator is an external output shown in Optical data (B).
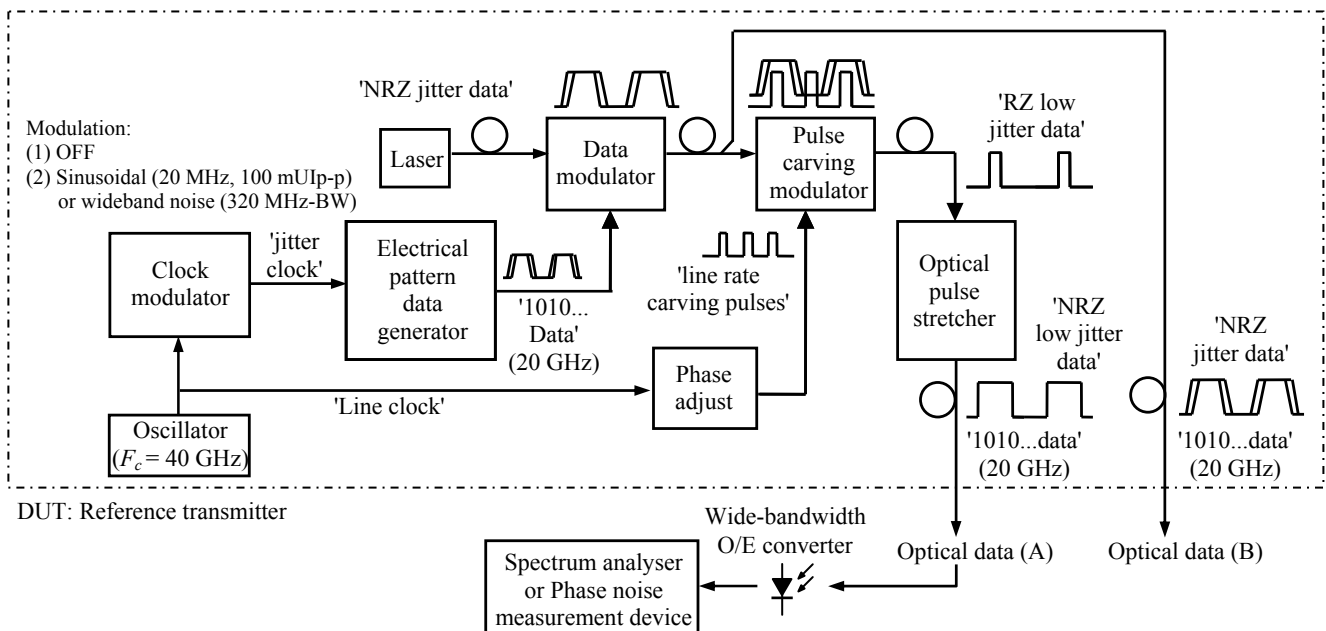

Figure IX.1 – Example reference transmitter verification block diagram (Step 1)

2)   Turn off the modulation of the clock modulator, and set the electrical pattern data generator to produce a 1010...data sequence (20-GHz clock). Since the 1010...data sequence without clock modulation does not generate PDJ, the dominant jitter component of the intrinsic jitter of optical data (A) is RJ due to the oscillator.

Apply Optical data (A) to the spectrum analyser through the wide-bandwidth O/E converter. A phase noise measurement device can be used instead of the spectrum analyser. Use the SSB noise at the centre frequency of 20 GHz to determine the RMS jitter, σ_{RJ}, of Optical data (A) for the jitter measurement bandwidth f_1-f_4. Here, refer to steps 2) to 4) of clause VIII.2.2 to determine the RMS jitter from the SSB noise.

Table IX.1 shows an example of the SSB phase noise performance, which is suitable for the STM-256 reference transmitter, at the centre frequency of 20 GHz. This phase noise achieves the RJ of 2 mUIpp for a measurement interval of $T = 60$ s in the bandwidth 80 kHz to 320 MHz.

NOTE – The error associated with the wide-bandwidth O/E converter, spectrum analyser and phase noise measurement device is for further study.

Table IX.1 – Example of phase noise performance at centre frequency of 20 GHz suitable for STM-256 reference transmitter (RJ = 2 mUIpp for bandwidth 80 kHz to 320 MHz)

Offset frequency	Phase noise (dBc/Hz)
10 kHz	−151
100 kHz	−154
1 MHz	−154
10 MHz	−154
100 MHz	−154
320 MHz	−154

3)   Set the clock modulator to turn on sinusoidal modulation to generate pseudo-PDJ on the 1010...data sequence. For example, set a sinusoidal modulation with modulation frequency $f_m = 20$ MHz and an amplitude of 100 mUIpp.

Apply Optical data (A) to the spectrum analyser or the phase noise measurement device and measure the modulation spectral intensity, P_A (in dB), at the frequency of 20 GHz $+ f_m$. In the same way, apply Optical data (B) to the spectrum analyser or the phase noise measurement device and measure the spectral intensity, P_B (in dB), at the frequency of 20 GHz $+ f_m$. Determine the PDJ suppression ratio, $z = 10^{(P_A - P_B)/20}$, using the measured P_A and P_B. The PDJ suppression ratio z represents the input-to-output RMS jitter transfer ratio of the pulse carving modulator. For example, for $P_A = -38$ dB and $P_B = -15$ dB, $z = 10^{(-38+15)/20} \cong 0.07$.

Wideband noise modulation with a bandwidth exceeding 320 MHz can be used instead of sinusoidal modulation to verify the PDJ suppression ratio, not in a specific modulation frequency, but in the entire jitter measurement bandwidth. In this case, measure the integrated SSB noise power of Optical data (A) and Optical data (B) for bandwidth f_1-f_4 and determine the PDJ suppression ratio by calculating the difference of the measured integrated SSB noise for Optical data (A) and Optical data (B). If the PDJ suppression performance of the pulse carving modulator is independent of the jitter modulation frequency f_m, the calculated value of z will be the same regardless of sinusoidal or wideband noise modulation.

IX.1.2 Step 2: Estimating intrinsic jitter

1)   Prepare the set-up shown in Figure IX.2. The difference from Figure IX.1 is that the spectrum analyser (or phase noise measurement device) is replaced by the jitter measurement device. Turn off modulation of the clock modulator, and set the electrical pattern data generator to produce a test pattern sequence (e.g., unframed PRBS-31). Optical data (A) includes low PDJ suppressed by the pulse carving modulator and RJ due to the oscillator.
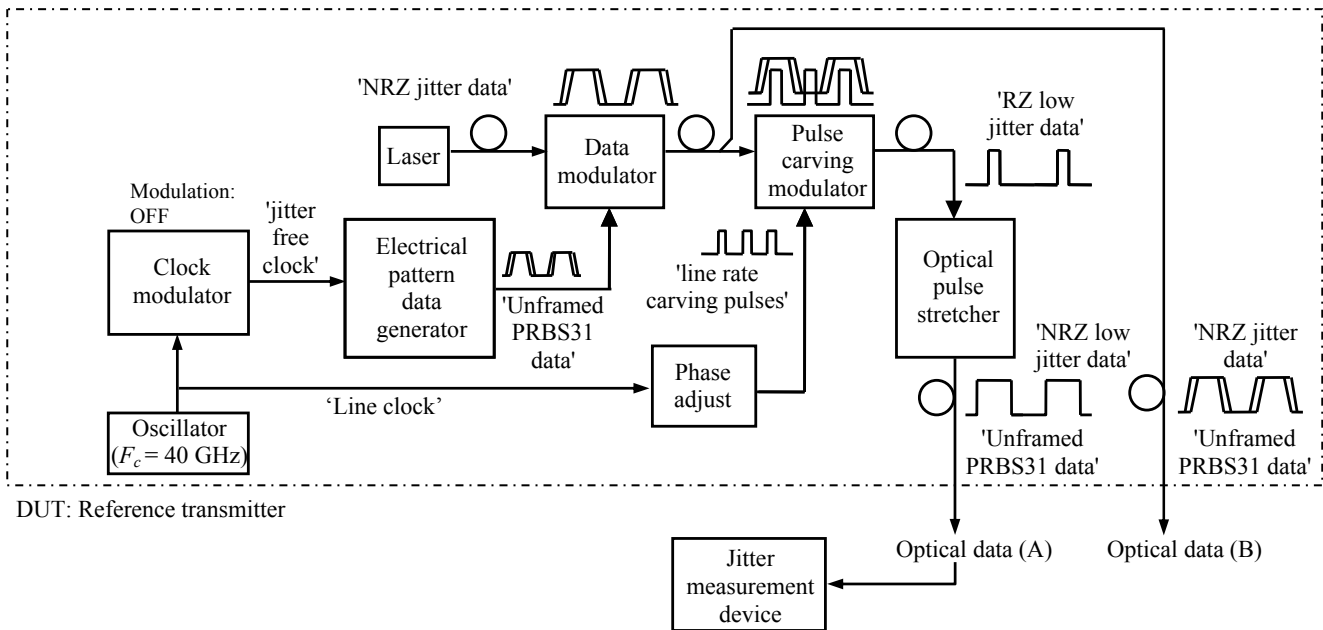
Figure IX.2 – Example reference transmitter verification block diagram (Step 2)

2)   Measure the RMS jitter, σ_{meas_A}, of Optical data (A) using the jitter measurement device. Similarly, measure the RMS jitter, σ_{meas_B}, of Optical data (B). The results σ_{meas_A} and σ_{meas_B} are represented by the following equations:

$$\sigma_{meas\_A}^2 = \sigma_A^2 + \sigma_{RXJ}^2$$

$$\sigma_{meas\_B}^2 = \sigma_B^2 + \sigma_{RXJ}^2$$

$$\sigma_A^2 = z^2\sigma_B^2 + \sigma_{RJ}^2$$

where, σ_A and σ_B represent the true RMS jitter of Optical data (A) and Optical data (B), respectively. σ_{RXJ} represents the intrinsic jitter of the jitter measurement device. σ_{RJ} and z are the RJ and PDJ suppression ratio of the reference transmitter determined in Step 1, respectively. The following equation is derived from the above three equations.

$$\sigma_A = \sqrt{\frac{z^2(\sigma_{meas\_B}^2 - \sigma_{meas\_A}^2) + \sigma_{RJ}^2}{1 - z^2}}$$

3)   Determine σ_A by substituting the measured results, σ_{meas_A}, σ_{meas_B}, σ_{RJ} and z into the above equation. σ_A is the estimated RMS value of the reference transmitter intrinsic jitter. If the PDJ component has been suppressed adequately by the pulse carving modulator, the PDJ component might be observed as Gaussian noise along with the RJ component. In this case, the peak-to-peak value of the estimated intrinsic jitter for measurement interval $T = 60$ s can be estimated as $13.3 \times \sigma_A$.

4)   Determine the estimated peak-to-peak intrinsic jitter as $13.3 \times \sigma_A$. This value should be lower than 10% of the nominal jitter amplitude of the reference transmitter in Appendix VII. In other words, the intrinsic jitter should be less than 10 mUIpp at a nominal jitter amplitude of 100 mUIpp.

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