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ITU-T

TELECOMMUNICATION
STANDARDIZATION SECTOR
OF ITU

O.172
Amendment 1
(06/2008)

SERIES O: SPECIFICATIONS OF MEASURING EQUIPMENT

Equipment for the measurement of digital and analogue/digital parameters

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Jitter and wander measuring equipment for digital systems which are based on the synchronous digital hierarchy (SDH)

Amendment 1

Recommendation ITU-T O.172 (2005) – Amendment 1

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ITU-T O-SERIES RECOMMENDATIONS

SPECIFICATIONS OF MEASURING EQUIPMENT

For further details, please refer to the list of ITU-T Recommendations.

Recommendation ITU-T O.172

Jitter and wander measuring equipment for digital systems which are based on the synchronous digital hierarchy (SDH)

Amendment 1

Summary

Amendment 1 to Recommendation ITU-T O.172 includes changes to the measurement bandwidth, measurement accuracy, jitter transfer measurement accuracy, Appendices VII and VIII.

Source

Amendment 1 to Recommendation ITU-T O.172 (2005) was approved on 29 June 2008 by ITU-T Study Group 4 (2005-2008) under Recommendation ITU-T A.8 procedure.

FOREWORD

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Recommendation ITU-T O.172

Jitter and wander measuring equipment for digital systems which are based on the synchronous digital hierarchy (SDH)

Amendment 1

1) Introduction

This amendment contains extensions to the 2005 version of Recommendation ITU-T O.172.

2) Additions

2.1) Clause 9.3, Measurement bandwidths

Replace Table 7 with the following table, which adds the measurement bandwidth for f_{12} high-pass filter for STM-64 rate.

Table 7/O.172 – Jitter measurement function bandwidth for SDH line signals

Signal	Jitter measurement bandwidth (–3 dB cut-off frequencies)			
	f_1 (Hz) high-pass	**f_{12} (Hz) high-pass**	**f_3 (Hz) high-pass**	**f_4 (Hz) low-pass**
STM-0e, STM-0	100	–	20 k	400 k
STM-1e	500	–	65 k	1.3 M
STM-1	500	12 k	65 k	1.3 M
STM-4	1 k	12 k	250 k	5 M
STM-16	5 k	12 k	1 M	20 M
STM-64	20 k	50 k	4 M	80 M
STM-256	80 k	–	16 M	320 M

NOTE 1 – Values for STM-0 are based on the requirements of ANSI T1.105.03 [21].

NOTE 2 – Values for STM-256 are to be considered provisional, since network requirements are not yet defined in ITU-T Rec. G.825 [13].

NOTE 3 – The f_{12} high-pass filter is optional.

2.2) Clause 9.4, Measurement accuracy

Replace Table 8 with the following table, which adds the fixed error for structured signal in the f_{12} - f_4 band for STM-64 rate.

Table 8/O.172 – Fixed error (W) of SDH line jitter measurements

Signal	Maximum peak-to-peak jitter error (UIpp) for given digital signals					
	Structured signal			Clock signal		
	f_1-f_4	f_{12}-f_4	f_3-f_4	f_1-f_4	f_{12}-f_4	f_3-f_4
STM-0e	FFS	–	FFS	FFS	–	FFS
STM-0	0.07	–	0.035	0.05	–	0.03
STM-1e	0.07	–	0.025	0.05	–	0.02
STM-1	0.07	0.035	0.035	0.05	0.03	0.03
STM-4	0.1	0.035	0.035	0.05	0.03	0.03
STM-16	0.1	0.035	0.035	0.05	0.03	0.03
STM-64	0.1	0.035	0.035	0.05	–	0.03
STM-256	0.15	–	0.05	0.05	–	0.03

Replace paragraph b) in clause 9.4.1 with the following:

b) An optical signal in conformance with ITU-T Rec. G.957 [14] or G.691 [1] and with a nominal power in the range –10 dBm to –12 dBm. Operation at higher input power levels may be permitted in accordance with the minimum mean launch powers specified in ITU-T Rec. G.957 [14] or G.691 [1] or G.693 [2].

2.3) Clause 9.5, Jitter transfer measurement accuracy

Add the following underlined part to the text of clause 9.5:

The total measurement error in the jitter frequency range $f_L = 0.01 \cdot f_C$ and $f_H = 100 \cdot f_C$ or f_4, if f_4 is lower than $100 \cdot f_C$, when using input jitter amplitude equal to the applicable jitter tolerance masks, shall be less than:

$$\pm 0.05 \text{ dB} \pm 0.12 \cdot g$$

where g is the measured jitter transfer gain at the jitter frequency f_m in dB<u>, and f_L, f_C, and f_H are according to Table 15-2 of ITU-T Rec. G.783</u>. This measurement error applies for g greater than or equal to –45 dB. No accuracy is specified for g less than –45 dB.

2.4) Appendix VII, Method for verification of measurement result accuracy and intrinsic fixed error

2.4.1) Clause VII.2, System implementation

a) *Replace the following text in clause VII.2*:

It is recommended the relative oscillator amplitudes be adjusted up to 100 mUI phase modulation, this can be calibrated using the spectrum analyser using normal FM theory techniques. The operation of the pulse generator is used to gate the Oscillator 2 clock, thus directly controlling the modulation burst time.

~~The synchronization of the modulation burst relative to the frame structure is for further study.~~

To minimize potential phase discontinuities, the modulation burst shall be either synchronized to the zero crossings of the sinusoidal modulation signal or alternatively shall have a maximum on/off transition time given approximately by the following relation.

b) Add the following text to the end of clause VII.2:

The synchronization of the modulation burst relative to the "SDH" frame structure is for further study.

2.4.2) Clause VII.3, Results and interpretation

Replace Table VII.1 with the following table, which adds new Note 5.

Table VII.1/O.172 – Combinations of modulation frequency, burst width and repetition rate

Signal	Modulation frequency f_m	Minimum burst width t_{min}	Burst widths > t_{min}				
STM-1	1 kHz[a)]	2 ms	–	–	–	–	–
	65 kHz[a)]	31 µs	–	–	–	100 µs	1 ms
	300 kHz	6.7 µs	–	–	–	100 µs	1 ms
	1.3 MHz	1.5 µs	–	–	10 µs	100 µs	1 ms
STM-4	10 kHz[a)]	200 µs	–	–	–	–	1 ms
	250 kHz[a)]	8 µs	–	–	–	100 µs	1 ms
	1 MHz	2 µs	–	–	10 µs	100 µs	1 ms
	5 MHz	400 ns	–	–	10 µs	100 µs	1 ms
STM-16	50 kHz[a)]	40 µs	–	–	–	100 µs	1 ms
	1 MHz a)	2 µs	–	–	10 µs	100 µs	1 ms
	5 MHz	400 ns	–	–	10 µs	100 µs	1 ms
	20 MHz	100 ns	–	1 µs	10 µs	100 µs	1 ms
STM-64	200 kHz[a)]	10 µs	–	–	–	100 µs	1 ms
	3 MHz[a)]	667 ns	–	–	10 µs	100 µs	1 ms
	20 MHz	100 ns	–	1 µs	10 µs	100 µs	1 ms
	80 MHz	25 ns	100 ns	1 µs	10 µs	100 µs	1 ms

[a)] The burst repetition rate shall be in the range from 10 Hz to 10 kHz.

NOTE 1 – Applicable only when high-pass f_1 is used for the jitter measurement.

NOTE 2 – The measurement period should be 60 seconds.

NOTE 3 – Minimum burst repetition rate of 10 Hz is chosen for measurement repeatability and is based on test pattern PRBS repetition.

NOTE 4 – Burst widths of 100 µs and 1 ms can only be used with burst repetitions less than 10 kHz and 1 kHz respectively.

NOTE 5 – STM-256 is for further study, because achieving reference transmitter for STM-256 by using current technology may be difficult.

2.5) Appendix VIII, Method for characterization of transmit intrinsic jitter

2.5.1) Clause VIII.2, Method

Replace item 4) of clause VIII.2.1 with the following:

4) If there is no corresponding SDH signal edge for a particular i, assign to $x_i = 0$. Measure x_i to cover one period of the SDH frame, i.e., the size of the dataset, $[x_1 .. x_N]$ is $N = 125 \times 10^{-6} \times f_0$, where f_0 is the corresponding bit rate. Then generate mathematically a new sequence by using the following Formula VIII-1.

$$x_i' = \frac{\sum_{n=1}^{24} x_{i-n}}{\sum_{n=1}^{24} p_{i-n}} \tag{VIII-1}$$

where p_i represents the pattern density information. Assign $p_i = 1$ when an SDH edge exists, assign $p_i = 0$ when no transition data is present. See Figure VIII.2.

Substitute x_i' values into series x_i where no measured SDH edge value exists.

For the long test pattern like PRBS-23 described in clause VIII.3, generate mathematically a new sequence by using following Formula VIII-2, instead of using Formula VIII-1.

$$x_i' = \frac{\sum_{n=1}^{64} h_n x_{i-n}}{\sum_{n=1}^{64} h_n p_{i-n}} \tag{VIII-2}$$

where h_n series (n = 1, 2, ... , 64) is the coefficient of an LPF with a cut-off frequency of $0.032f_o$. For example, half of the coefficients, $h_{1\text{-}32}$, are given as follows; the other remaining coefficients, $h_{33\text{-}64}$, are symmetrical with $h_{1\text{-}32}$.

$h_{1\text{-}32}$ =

```
4.406e-05,     -9.982e-04,    -3.215e-03,    -4.628e-03,
-1.399e-04,    -1.447e-03,    -3.817e-03,    -4.237e-03,
-3.595e-04,    -1.982e-03,    -4.315e-03,    -3.342e-03,
-6.391e-04,    -2.584e-03,    -4.619e-03,    -1.852e-03,

3.087e-04,     1.614e-02,     4.031e-02,     6.207e-02,
3.189e-03,     2.171e-02,     4.650e-02,     6.560e-02,
6.809e-03,     2.771e-02,     5.233e-02,     6.803e-02,
1.114e-02,     3.397e-02,     5.759e-02,     6.927e-02.
```

NOTE 2 – The errors associated with these phase insertion algorithms are less than 4%. This is an estimation from ten samples which is evaluated in clause VIII.5.

2.5.2) Clause VIII.3, Diagnostic test pattern

Replace the whole clause VIII.3 including Figures VIII.4 and VIII.5 with the following:

1) Figures VIII.4 and VIII.5 below define diagnostic SDH test patterns. These are suitable for use at STM-64 and STM-16. The remainder of the SDH frame is an all 00_H scrambled $2^7–1$ pattern or a PRBS-23 scrambled $2^7–1$ pattern for each test pattern. When using an all 00_H scrambled $2^7–1$ pattern, the test pattern simulates short periodic patterns. Here, the scrambler shall be reset to "1111111" at the last byte of the first row of SOH for every SDH frame. On the other hand, when using a PRBS-23 scrambled $2^7–1$ pattern, the test pattern simulates long periodic patterns. Here, the scrambler and the shift registers to generate the PRBS-23 bit stream shall be reset simultaneously to "1111111" and "1111111111 1111111111 111", respectively, at the last byte of the first row of SOH for every SDH frames.

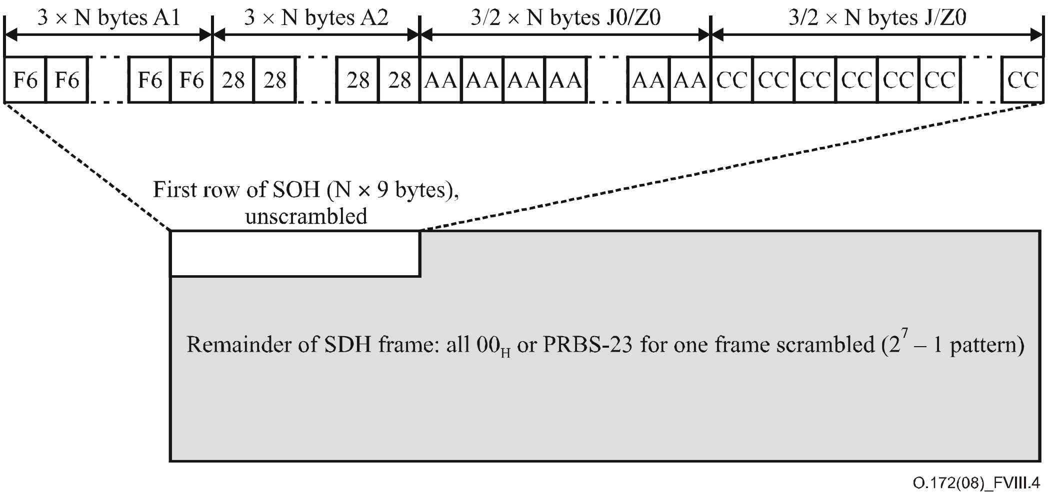


Figure VIII.4/O.172 – Test pattern 1

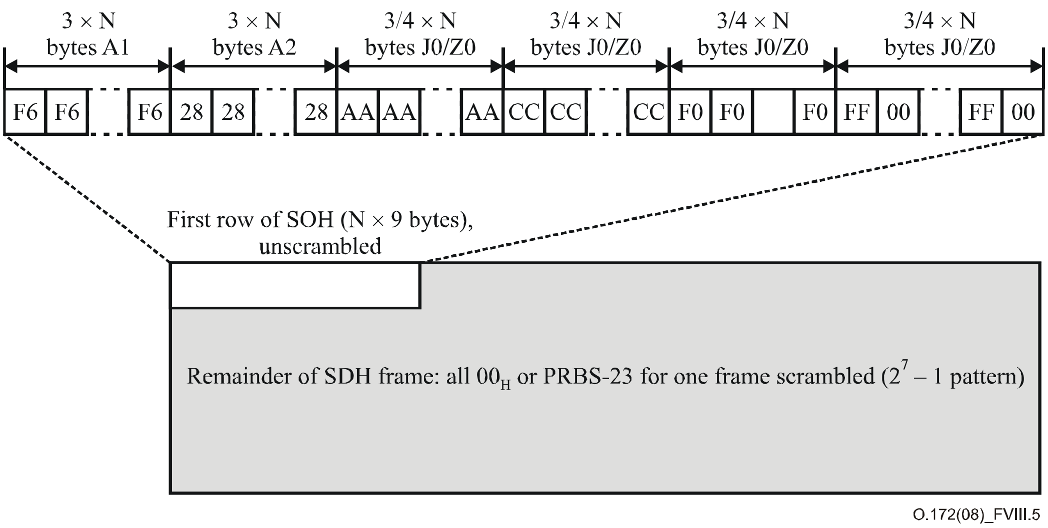


Figure VIII.5/O.172 – Test pattern 2

2) STM-256 pattern is for further study.

2.5.3) New clause VIII.5

VIII.5 Evaluation of the error associated with the phase insertion algorithm

The phase insertion methods of item 4) in clause VIII.2.1 were designed considering the characteristics of wideband clock recovery (WCR) used in traditional jitter measurement equipment that satisfies this Recommendation. Although these insertion methods are easy and effective, they have algorithm error for the phase insertion values obtained by real WCR output. This clause verifies the algorithm error. First, how to obtain the phase insertion values by using an ideal WCR is explained as follows:

This WCR phase insertion algorithm consists of the following three steps. Refer to Figure VIII.7 for the signal form in each step.

1) Measure the pattern-dependent phase values, x_i, with a resolution of 1 mUI at the SDH signal edges, according to items 1) through 3) in clause VIII.2.1.

2) Make a simplified SDH signal sequence, s_k, by using x_i. Here, the amplitude value of s_k is 0 or 1, and the sampling interval of s_k is 1/1000 times the corresponding SDH bit rate. Assign x_i to the phase error value at the corresponding data edges of s_k.

3) Input the sequence s_k to the ideal WCR achieved by the digital signal processing shown in Figure VIII.8. The clock signal sequence, c_k, is output from the WCR. Detect the phase error sequence, x_i', at every rising edge of c_k.

Use sequence x_i' for sequence x_i in item 5) in clause VIII.2.1.

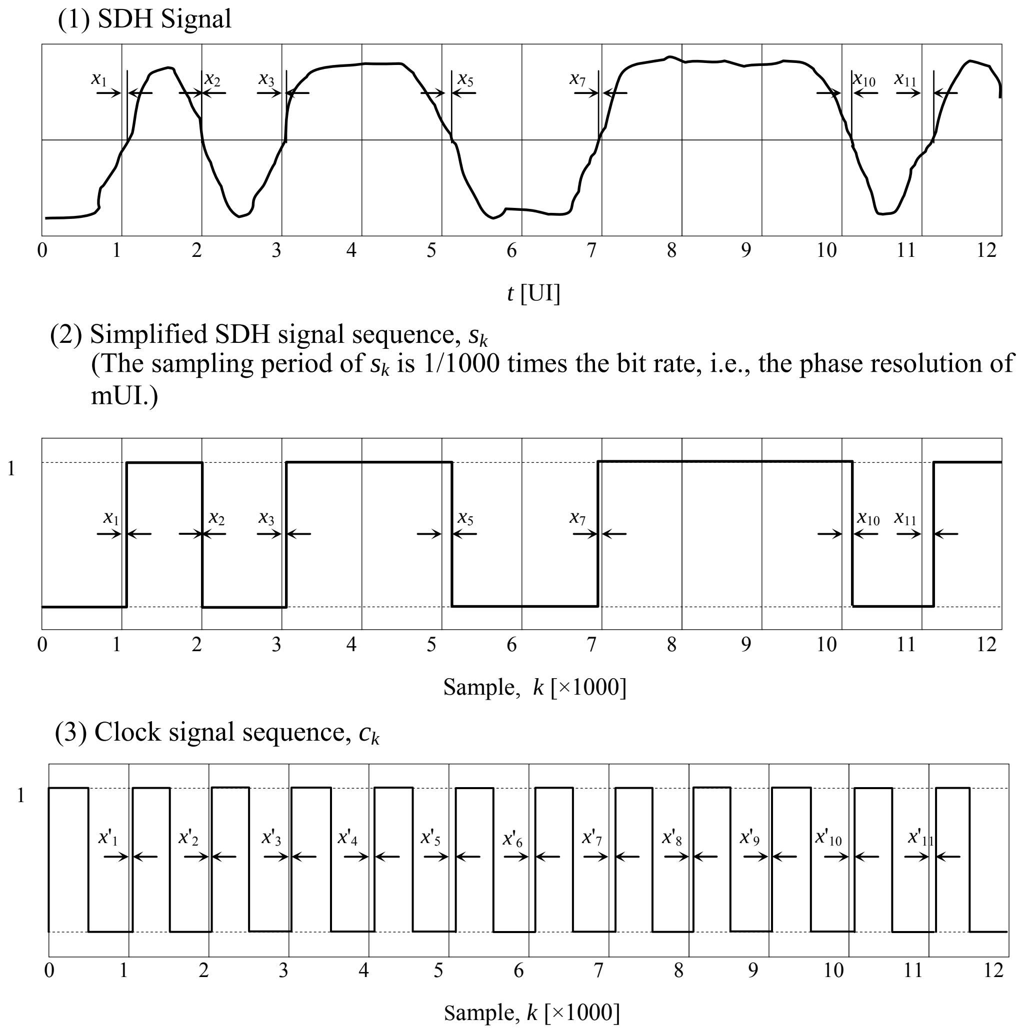


Figure VIII.7/O.172 – Phase insertion algorithm using wideband clock recovery

Figure VIII.8 shows an example of the block diagram of the ideal WCR achieved by digital signal processing. The delay outputs the delayed sequence, s_{k-500}, which is delayed by the half cycle of the SDH bit rate. The XOR outputs exclusive-OR between s_k and s_{k-500}. The BPF is a digital filter in which the centre frequency is the SDH bit rate; its pass-band width should be at least four times the cut-off frequency f_4 of the jitter measurement low-pass filter. For example, the pass-band is 10 GHz ±320 MHz for STM-64 (f_4 = 80 MHz). The Limiter outputs c_k = 1 when the input is a positive value, and c_k = 0 when the input is a negative value.

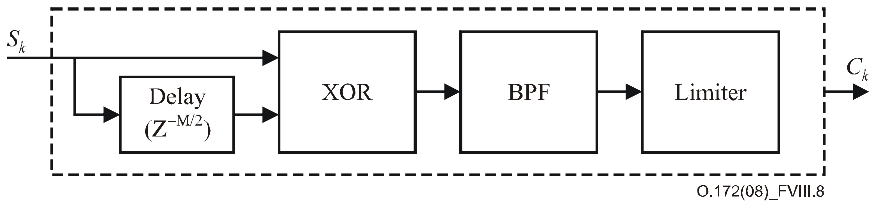


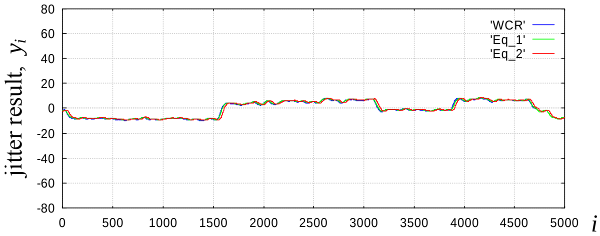
Figure VIII.8/O.172 – Example of block diagram of wideband clock recovery

The criterial jitter result y_i is obtained by using x_i' generated by the WCR algorithm mentioned above.

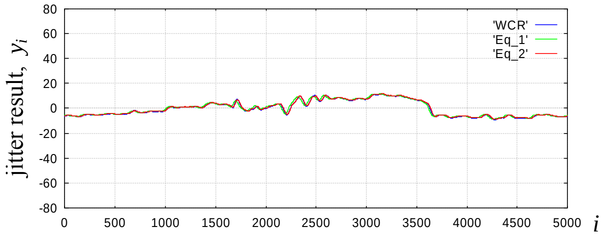
Table VIII.1 shows the verified differences between jitter results y_i obtained from the phase insertion methods in item 4 in clause VIII.2.1 and jitter results y_i obtained from the above-mentioned WCR model. Here, the pattern-dependent phase values of the actual STM-64 signals (Example 1-10) observed by an oscilloscope were used as the input sequence x_i. The algorithm errors of the phase insertion methods are less than 4% or less than 2% when using Formula VIII-1 or Formula VIII-2, respectively. The series of the jitter results y_i of Example 1-10 are shown in Figure VIII.9. All graphs are extracted at the SOH sections with a large peak-peak.

Table VIII.1/O.172 – Algorithm error of phase insertion method

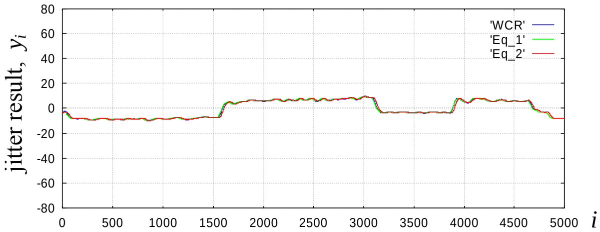
Transmission signal (STM-64)	Jitter result of WCR model [mUIpp]	Difference of Jitter results [%]	
		Formula VIII-1	Formula VIII-2
		$x_i' = \frac{\sum_{n=1}^{24} x_{i-n}}{\sum_{n=1}^{24} p_{i-n}}$	$x_i' = \frac{\sum_{n=1}^{64} h_n x_{i-n}}{\sum_{n=1}^{64} h_n p_{i-n}}$
Example 1	18	0	0
Example 2	20	0	0
Example 3	19	0	1
Example 4	23	–4	–2
Example 5	35	0	1
Example 6	60	–2	0
Example 7	99	–1	0
Example 8	98	–1	0
Example 9	120	0	1
Example 10	49	–2	–1



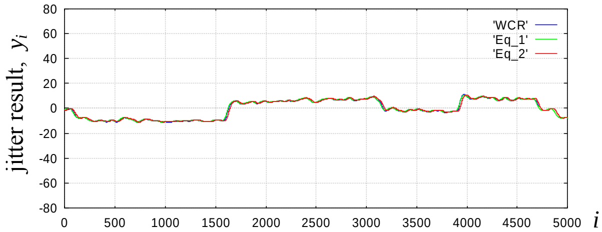
a) Example 1



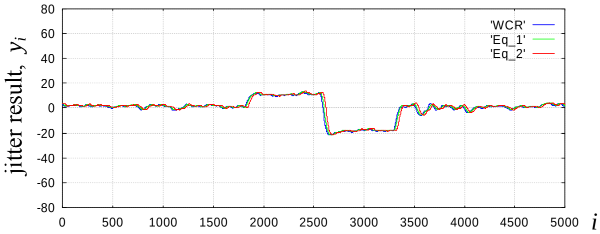
b) Example 2



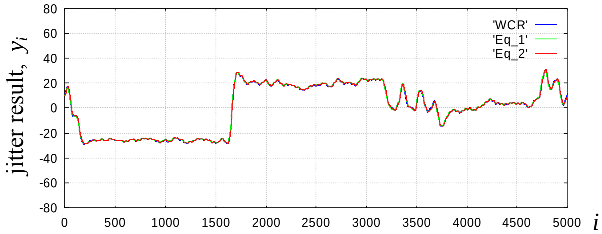
c) Example 3



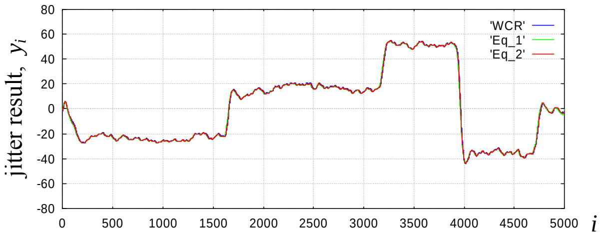
d) Example 4



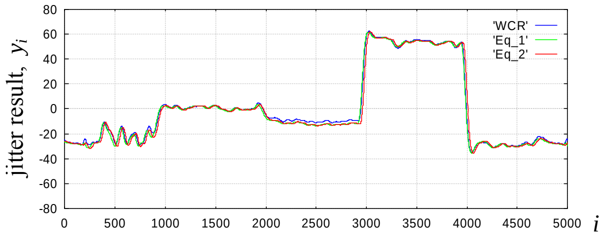
e) Example 5



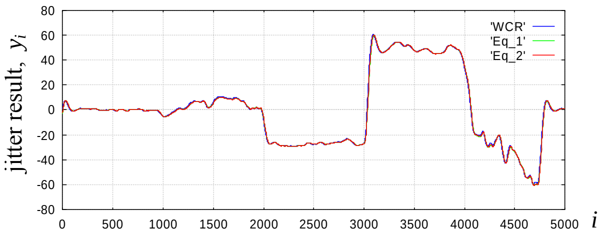
f) Example 6



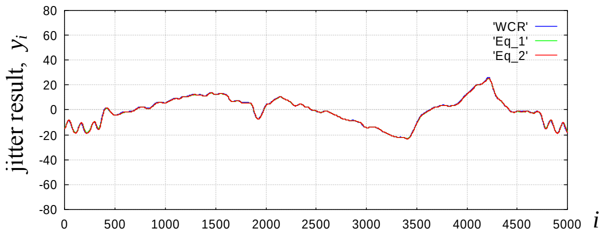
g) Example 7



h) Example 8



i) Example 9



j) Example 10

Figure VIII.9/O.172 – Example of jitter results, y_i, with each phase insertion algorithm

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