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THE INTERNATIONAL
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O.151

(11/1988)

SERIES O: SPECIFICATIONS FOR MEASURING EQUIPMENT

Equipment for the measurement of digital and analogue/ digital parameters

ERROR PERFORMANCE MEASURING EQUIPMENT FOR DIGITAL SYSTEMS AT THE PRIMARY BIT RATE AND ABOVE

Reedition of CCITT Recommendation O.151 published in the Blue Book, Fascicle IV.4 (1988)

NOTES

1 CCITT Recommendation O.151 was published in Fascicle IV.4 of the *Blue Book*. This file is an extract from the *Blue Book.* While the presentation and layout of the text might be slightly different from the *Blue Book* version, the contents of the file are identical to the *Blue Book* version and copyright conditions remain unchanged (see below).

2 In this Recommendation, the expression "Administration" is used for conciseness to indicate both a telecommunication administration and a recognized operating agency.

Recommendation O.151

ERROR PERFORMANCE MEASURING EQUIPMENT FOR DIGITAL SYSTEMS AT THE PRIMARY BIT RATE AND ABOVE[1]

(Geneva, 1976; amended Geneva, 1980, Malaga-Torremolinos, 1984 and Melbourne, 1988)

The requirements for the characteristics of bit-error performance measuring equipment which are described below must be adhered to in order to ensure compatibility between equipments standardized by the CCITT, and produced by different manufacturers.

1 General

The equipment is designed to measure the bit-error performance of digital transmission systems by the direct comparison of a pseudorandom test pattern with an identical locally generated test pattern. In addition the capability to measure errored time intervals is provided.

2 Test patterns

2.1 *Pseudorandom pattern for systems using a $2^{15} - 1$ pattern length*

This pattern is to be produced by means of a shift register incorporating appropriate feedback (see Figure 1/O.151 and Table 1/O.151):

Number of shift register stages	15
Pattern length	$2^{15} - 1 =$ 32 767 bits
Feedback	taken from the 14th and 15th stage via an exclusive-OR-gate to the first stage
Longest sequence of zeros	15 (inverted signal)

2.2 *Pseudorandom pattern for systems using $2^{23} - 1$ pattern length*

This pattern is to be produced by means of a shift register incorporating appropriate feedback (see Figure 2/O.151):

Number of shift register stages	23
Pattern length	$2^{23} - 1 =$ 8 388 607 bits
Feedback	taken from the 18th and 23rd stages via an exclusive-OR-gate to the first stage
Longest sequence of zeros	23 (inverted signal)

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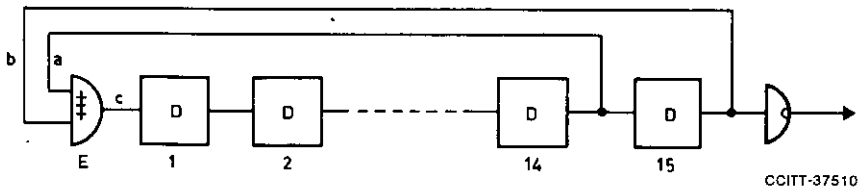
1 This Recommendation is the joint responsibility of Study Groups IV, XVII and XVIII.

TABLE 1/O.151

Status of the shift register stages during the transmission of the first 47 bits

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
2	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
3	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0
																0
																0
14	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
15	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
16	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
17	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1
																1
																1
29	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1
30	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
31	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1
32	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1
																1
																1
43	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1
44	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
45	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0
46	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1
47	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	1
																1



Note – The clock pulse connection is not shown.

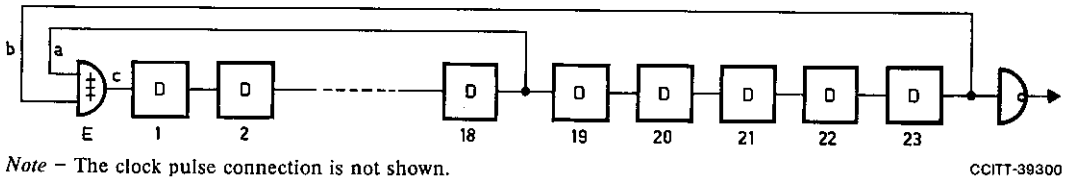
a	b	c
1	0	1
0	1	1
0	0	0
1	1	0

Truth table for exclusive OR-gate (E):

a and b: gate inputs
c: gate output

FIGURE 1/O.151

Circuit example for a 15-stage shift register with D-flipflops and an exclusive-OR-gate



a	b	c
1	0	1
0	1	1
0	0	0
1	1	0

Truth table for exclusive OR-gate (E):

a and b: gate inputs
c: gate output

FIGURE 2/O.151

Circuit example for a 23-stage shift register with D-flipflops and an exclusive-OR-gate

2.3 *Pseudorandom pattern for systems using $2^{20} - 1$ pattern length*

This pattern may be generated by a twenty stage shift register with feedback taken from the seventeenth and twentieth stages. The output signal is taken from the twentieth stage, and an output bit is forced to be a "one" whenever the next 14 bits are all "zero".

The quasi-random sequence satisfies the following:

$$Q_{n+1}\ (k+1) = Q_n(k),\ n = 1, 2, \ldots, 19,$$

$$Q_1\ (k+1) = Q_{17}(k) \oplus Q_{20}(k), \text{ and}$$

$$RD(k) = Q_{20}\ (k) + \overline{Q_6(k) + \ldots + Q_{19}(k)}$$

where

$Q_n(k)$ = Present state for nth stage

$Q_n(k+1)$ = Next state for nth stage

$RD(k)$ = Present value of output

$+$ = a logic OR operation

$\oplus$ = a logic EXCLUSIVE OR operation

$\overline{(\ )}$ = a logic NEGATION operation.

2.4 *Fixed patterns (optional)*

Fixed patterns of all ones and alternating ones and zeros may be provided.

3 Bit rate

The bit rates in accordance with CCITT Recommendations are indicated in Table 2/O.151.

TABLE 2/O.151

Bit rates, pertinent Recommendations and pseudo random test patterns

Bit rates (kbit/s)	Recommendations corresponding to multiplex system	Recommendations corresponding to digital line section/line system	Bit rate tolerance	Test pattern
1 554	G.733 [1]	G.911 [8], G.951 [9], G.955 [10]	$\pm 50 \cdot 10^{-6}$	$2^{15}-1$, $2^{20}-1$
2 048	G.732 [2]	G.921 [11], G.952 [12], G.956 [13]	$\pm 50 \cdot 10^{-6}$	$2^{15}-1$
6 312	G.743 [3]	G.912 [14], G.951 [9], G.955 [10]	$\pm 30 \cdot 10^{-6}$	$2^{15}-1$, $2^{20}-1$
8 448	G.742 [4], G.745 [5]	G.921 [11], G.952 [12], G.956 [13]	$\pm 30 \cdot 10^{-6}$	$2^{15}-1$
32 064	G.752 [6]	G.913 [15], G.953 [16], G.955 [10]	$\pm 10 \cdot 10^{-6}$	$2^{15}-1$, $2^{20}-1$
34 368	G.751 [7]	G.921 [11], G.954 [17], G.956 [13]	$\pm 20 \cdot 10^{-6}$	$2^{23}-1$
44 736	G.752 [6]	G.914 [18], G.953 [16], G.955 [10]	$\pm 20 \cdot 10^{-6}$	$2^{15}-1$, $2^{20}-1$
139 264	G.751 [7]	G.921 [11], G.954 [17], G.956 [13]	$\pm 15 \cdot 10^{-6}$	$2^{23}-1$

Note – Normally only the appropriate combination of bit rates – either 2048 kbit/s, 8448 kbit/s, etc. or 1544 kbit/s, 6312 kbit/s, etc. – will be provided in a given instrumentation.

4 Interfaces

The interface characteristics (impedances, levels, codes, etc.) should be in accordance with Recommendation G.703 [19].

In addition to providing for terminated measurements the instrumentation shall also be capable of monitoring at protected test points on digital equipment. Therefore, a high impedance and/or additional gain should be provided to compensate for the loss at monitoring points already provided on some equipments.

5 Error-ratio measuring range

The receiving equipment of the instrumentation should be capable of measuring bit-error ratios in the range 10^{-3} to 10^{-8}. In addition, it should be possible to measure bit-error ratios of 10^{-9} and 10^{-10}; this can be achieved by providing the capability to count cumulative errors.

6 Mode of operation

The mode of operation should be such that the signal to be tested is first converted into a unipolar (binary) signal in the error measuring instrument and subsequently the bit comparison is made also with a reference signal in binary form.

Facilities may *optionally* be provided to allow the direct comparison at line code (e.g. AMI or HDB-3) with correspondingly coded reference signals. In the case of such measurements polarity distinction is possible, so that errors caused by the injection or omission of positive or negative pulses can be determined separately.

7 Measurement of errored time intervals

The instrument shall be capable of detecting errored seconds and other errored or error-free time intervals as defined in § 1.4 of Recommendation G.821 [20] and of deriving error performance reduced to 64 kbit/s in accordance

with Annex D to Recommendation G.821 [20][2]. The number of errored or error-free time intervals in a selectable observation period from 1 minute to 24 hours, or continuous, shall be counted and displayed.

For this measurement the error detection circuits of the instrument shall be controlled by an internal timer which sets intervals of equal length and which operates independently of the occurrence of errors.

8 Operating environment

The electrical performance requirements shall be met when operating at the climatic conditions as specified in Recommendation O.3, § 2.1.

References

[1] CCITT Recommendation *Characteristics of primary PCM multiplex equipment operating at 1544 kbit/s*, Vol. III, Rec. G.733.

[2] CCITT Recommendation *Characteristics of primary PCM multiplex equipment operating at 2048 kbit/s*, Vol. III, Rec. G.732.

[3] CCITT Recommendation *Second-order digital multiplex equipment operating at 6312 kbit/s and using positive justification*, Vol. III, Rec. G.743.

[4] CCITT Recommendation *Second-order digital multiplex equipment operating at 8448 kbit/s and using positive justification*, Vol. III, Rec. G.742.

[5] CCITT Recommendation *Second-order digital multiplex equipment operating at 8448 kbit/s and using positive/zero/negative justification*, Vol. III, Rec. G.745.

[6] CCITT Recommendation *Characteristics of digital multiplex equipments based on a second-order bit rate of 6312 kbit/s and using positive justification*, Vol. III, Rec. G.752.

[7] CCITT Recommendation *Digital multiplex equipments operating at the third-order bit rate of 34 368 kbit/s and the fourth-order bit rate of 139 264 kbit/s and using positive justification*, Vol. III, Rec. G.751.

[8] CCITT Recommendation *Digital line sections at 1544 kbit/s*, Vol. III, Rec. G.911.

[9] CCITT Recommendation *Digital line systems based on the 1544 kbit/s hierarchy on symmetric pair cables,* Vol. III, Rec. G.951.

[10] CCITT Recommendation *Digital line systems based on the 1544 kbit/s hierarchy on optical fibre cables*, Vol. III, Rec. G.955.

[11] CCITT Recommendation *Digital sections based on the 2048 kbit/s hierarchy*, Vol. III, Rec. G.921.

[12] CCITT Recommendation *Digital line systems based on the 2048 kbit/s hierarchy on symmetric pair cables*, Vol. III, Rec. G.952.

[13] CCITT Recommendation *Digital line systems based on the 2048 kbit/s hierarchy on optical fibre cables*, Vol. III, Rec. G.956.

[14] CCITT Recommendation *Digital line sections at 6312 kbit/s*, Vol. III, Rec. G.912.

[15] CCITT Recommendation *Digital line sections at 32 064 kbit/s*, Vol. III, Rec. G.913.

[16] CCITT Recommendation *Digital line systems based on the 1544 kbit/s hierarchy on coaxial pair cables*, Vol. III, Rec. G.953.

[17] CCITT Recommendation *Digital line systems based on the 2048 kbit/s hierarchy on coaxial pair cables*, Vol. III, Rec. G.954.

[18] CCITT Recommendation *Digital line sections at 44 736 kbit/s*, Vol. III, Rec. G.914.

[19] CCITT Recommendation *Physical/electrical characteristics of hierarchical digital interfaces*, Vol. III, Rec. G.703.

[20] CCITT Recommendation *Error performance on an international digital connection forming part of an integrated services digital network*, Vol. III, Rec. G.821.

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[2] Error performance evaluation at bit rates other than 64 kbit/s is under study.

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