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Information of semiconductor devices required for the design of telecommunication equipment applying soft error mitigation measures

Recommendation ITU-T K.150

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Information of semiconductor devices required for the design of telecommunication equipment applying soft error mitigation measures

Summary

Recommendation ITU-T K.150 describes characteristic parameters and functions of semiconductor devices that a telecommunication equipment designer needs when implementing soft error mitigation measures. This Recommendation describes the kinds of information expected to be supplied from semiconductor device vendors to designers for telecommunication equipment.

The definition of expected information and objective for collecting it are first described. The Recommendation then describes which semiconductor devices are targeted for information collection. Finally, the details of the information expected to be collected are described for each target semiconductor device.

History

Edition	Recommendation	Approval	Study Group	Unique ID*
1.0	ITU-T K.150	2020-12-14	5	11.1002/1000/14563

Keywords

Neutron irradiation test, soft error, SRAM, telecommunication equipment.

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Introduction

When implementing soft error mitigation measures, it is necessary both to understand the characteristics of semiconductor devices regarding soft errors and to implement soft error mitigation measures at the equipment design level.

Recommendation ITU-T K.131 provides a design methodology for soft error mitigation measures. In order to apply this design methodology to the telecommunication equipment, it is necessary to obtain information related to soft error mitigation measures on semiconductor devices to be mounted. However, the information is not always supplied from manufacturers of devices through documents such as a datasheet or a report of semiconductor devices for equipment manufacturers. Even if the information is supplied, the information may not be applied correctly, as the method to obtain the data of the semiconductor device and the format for supplying the information have not been standardized. Therefore, it is important to inform semiconductor device vendors what kind of information telecommunication equipment designers expect to receive.

This Recommendation clarifies characteristic parameters necessary for the design of soft error mitigation measures in telecommunication equipment, and which are expected to be supplied by semiconductor device vendors.

Recommendation ITU-T K.150

Information of semiconductor devices required for the design of telecommunication equipment applying soft error mitigation measures

1 Scope

This Recommendation clarifies the kinds of characteristic parameters necessary for the design of soft error mitigation measures in telecommunication equipment, and which are expected to be supplied by semiconductor device vendors. The method for obtaining the characteristic parameter is also specified. Note that this Recommendation assumes that the design methodology provided in [ITU-T K.131] is applied.

2 References

The following ITU-T Recommendations and other references contain provisions which, through reference in this text, constitute provisions of this Recommendation. At the time of publication, the editions indicated were valid. All Recommendations and other references are subject to revision; users of this Recommendation are therefore encouraged to investigate the possibility of applying the most recent edition of the Recommendations and other references listed below. A list of the currently valid ITU-T Recommendations is regularly published. The reference to a document within this Recommendation does not give it, as a stand-alone document, the status of a Recommendation.

[ITU-T K.124] Recommendation ITU-T K.124 (2016), *Overview of particle radiation effects on telecommunication systems.*

[ITU-T K.131] Recommendation ITU-T K.131 (2018), *Design methodologies for telecommunication systems applying soft error measures.*

[ITU-T K.139] Recommendation ITU-T K.139 (2018), *Reliability requirements for telecommunication systems affected by particle radiation.*

[JESD89A] JEDEC standard JESD89A (2012), *Measurement and Reporting of Alpha Particle and Terrestrial Cosmic Ray-Induced Soft Errors in Semiconductor Devices.*

3 Definitions

3.1 Terms defined elsewhere

This Recommendation uses the following terms defined elsewhere:

3.1.1 ECC correction [ITU-T K.131]: Identifies the erroneous bit then outputs data automatically corrected by logical processing using an error correction code (ECC).

3.1.2 failure in time (FIT) [ITU-T K.131]: The unit that indicates the number of failures that can be expected in one billion (10^9) hours of operation.

3.1.3 soft error [ITU-T K.131]: A phenomenon in which one or more bits within the data on the device have their values reversed. A soft error does not constitute damage to the actual device.

3.1.4 soft error rate (SER) [ITU-T K.131]: Occurrences of soft errors in a unit of time.

3.2 Terms defined in this Recommendation

This Recommendation defines the following terms:

3.2.1 correctable error: An error which can be corrected by an error correction code (ECC).

3.2.2 un-correctable error: An error which cannot be corrected by an error correction code (ECC).

3.2.3 frame: A set of memory bits to which an error correction code is applied.

3.2.4 required information (RI): Information that is expected to be provided by semiconductor vendors.

3.2.5 real-time test: Test whereby results are obtained during actual operation in an assumed operational environment.

3.2.6 accelerated test: Test whereby results are obtained in a short time by intentionally creating an analogous environment.

4 Abbreviations and acronyms

This Recommendation uses the following abbreviations and acronyms:

ASIC Application Specific Integrated Circuit

ASSP Application Specific Standard Product

BRAM Block Random Access Memory

CPLD Complex Programmable Logic Device

CPU Central Processing Unit

CRAM Configuration Random Access Memory

DRAM Dynamic Random Access Memory

ECC Error Correction Code

EUT Equipment Under Test

FIT Failure in Time

FPGA Field-Programmable Gate Array

RAM Random Access Memory

RI Required Information

SER Soft Error Rate

SRAM Static Random Access Memory

5 Conventions

None.

6 Provision of required information for soft error mitigation measures in telecommunication equipment

This clause addresses the details for the provision of information required for soft error mitigation measures. The type of information expected to be provided by semiconductor device vendors that is necessary for designing soft error mitigation measures in telecommunication equipment are specified. The information expected to be provided is referred to as "Required Information (RI)" and telecommunication equipment designers expect semiconductor device vendors to provide RI as publicly disclosed or private information. The conceptual diagram is shown in Figure 6-1.

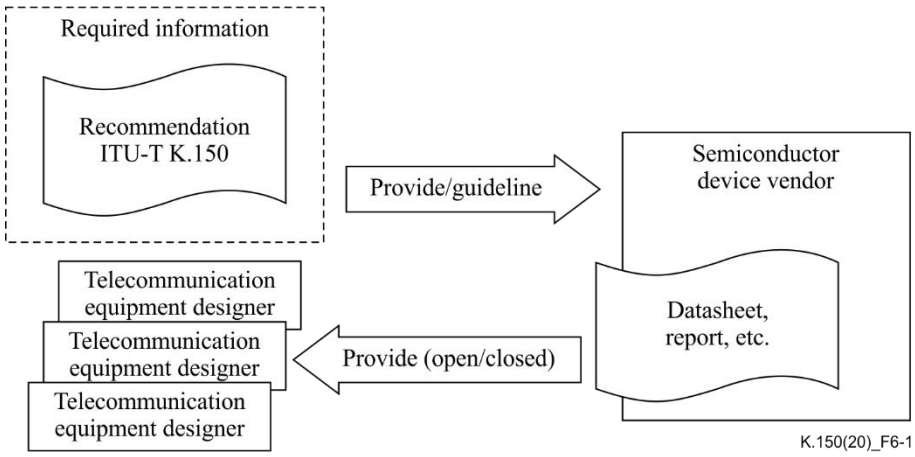

Figure 6-1 – Conceptual diagram of requested information for soft error mitigation measures

The background requiring the information is given below.

Basic recommendations for soft error mitigation measures in telecommunication equipment were given [ITU-T K.124]; then details of the techniques such as design methodologies, and reliability estimation methods and requirement were established. These recommendations address soft errors caused by the effects of neutrons and alpha particles. [ITU-T K.131] provides design methodologies to apply soft error mitigation measures effectively to equipment consisting of semiconductor devices that may be affected by particle radiation. To apply mitigation measures according to this design methodology, it is necessary to obtain essential information from a datasheet or report of the semiconductor devices that are to be mounted on equipment. This Recommendation assumes that [ITU-T K.131] is applied; the outline of procedures for implementation of soft error mitigation measures is shown in Figure 6-2.

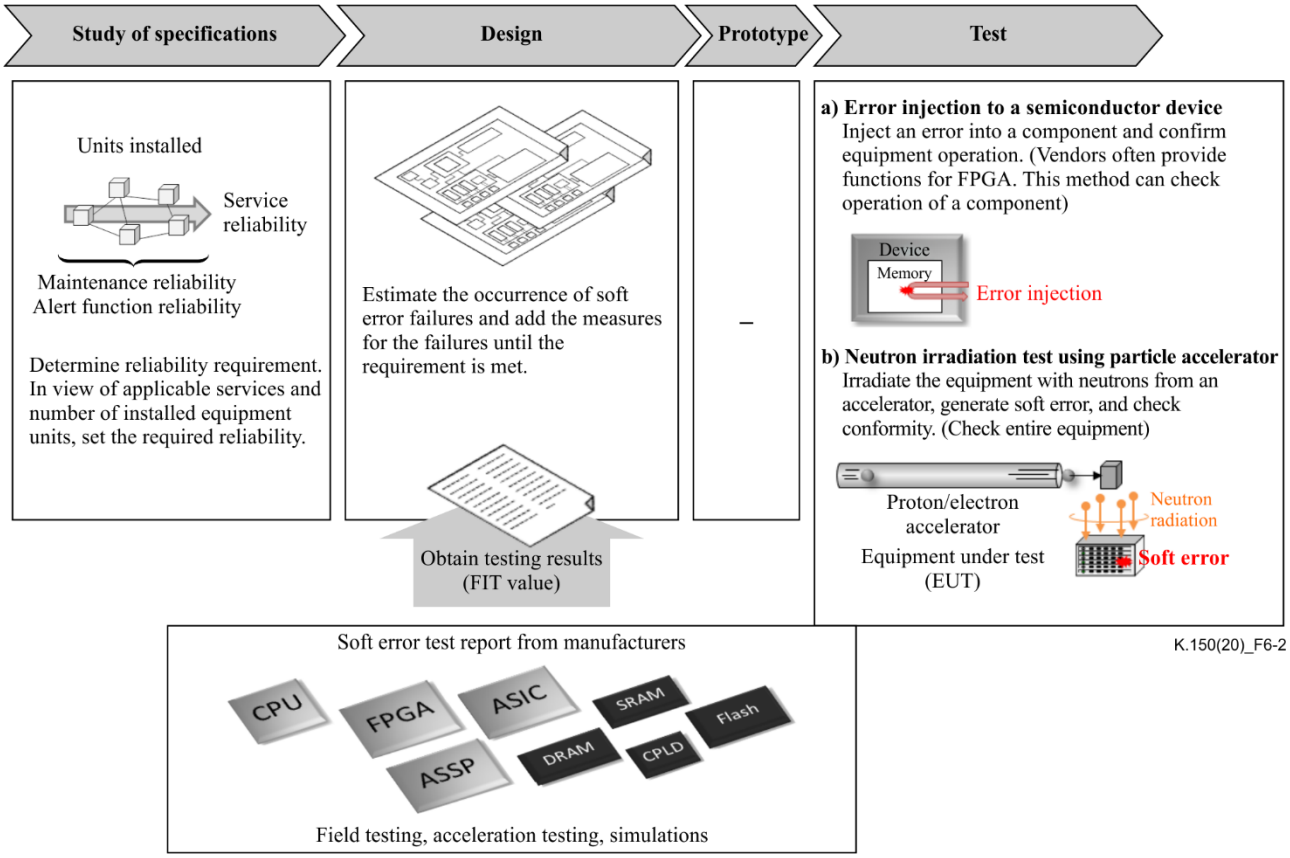

Figure 6-2 – Procedures for implementation of soft error mitigation measures in development of equipment

7 Justification for the provision of required information (RI)

This clause details the objective of getting RI, which is essential information of semiconductor devices related to soft error mitigation measures.

Semiconductor devices generally conform to the JEDEC standards, and information related to soft error is described in [JESD89A]. The measurement methods of soft errors caused by particle radiation are described in [JESD89A]. However, the range of information relating to measurement results provided from a device vendor depends on the vendor. Therefore, for designers of equipment intending to implement soft error mitigation measures, it is not easy to obtain and use the information.

There are cases that the information is not supplied, and design for soft error mitigation measures cannot be performed. Even if measurement results are provided, soft error rate (SER) may not be estimated correctly when the details of test method are not provided, as it would be difficult to know how to apply the values to the estimation of SER.

The objectives of this Recommendation are to suggest semiconductor device vendors to provide essential information that designers of telecommunication equipment need to correctly estimate SER, and appropriately design soft error measures. This Recommendation specifies what kind of information is to be provided by semiconductor device vendors, and methods to obtain the data as RI. This Recommendation aims to encourage vendors to provide standardized RI for telecommunication equipment designers in order to support appropriate selection of devices.

8 Target semiconductor devices

8.1 Semiconductor devices producing soft errors

Among semiconductor devices in telecommunication equipment, semiconductor memories and logic circuits are particularly impacted by particle radiation. Semiconductor memories are classified into static random access memory (SRAM), dynamic random access memory (DRAM) and flash memory. The soft error rate in logic circuits is so low that it does not cause problems in operational environment. Therefore, logic circuits are out of the scope of this Recommendation. Consequently, semiconductor memory devices and semiconductor devices with embedded memories are subject to this Recommendation. The kinds of memory circuits deployed in semiconductor devices under this Recommendation are classified in Table 8.1, and described in detail in clauses 8.2 to 8.3.

Table 8-1 – Semiconductor devices and their memory use

Semiconductor device type		Memory circuits		
		SRAM	**DRAM**	**Flash memory**
Generic memory		✓	✓	✓
Semiconductor devices with embedded memory	FPGA (incl. CPLD)	✓	✓	✓
	CPU	✓		
	ASSP/ASIC	✓	✓	

8.2 Generic memory devices

Soft error rate (SER) is required as RI for soft error mitigation design for generic memories. This Recommendation does not distinguish the memory circuit type because equipment designers require only the soft error rate of the memory, and the design method does not depend on the memory circuit type, such as SRAM, DRAM and flash memory, whereas the SER of each device is different from each other.

8.3 Semiconductor devices with embedded memory

As shown in Table 8-1, memories are embedded in some semiconductor devices, such as field-programmable gate array (FPGA) (including a complex programmable logic device (CPLD)), central processing unit (CPU), application specific standard product (ASSP) and application specific integrated circuit (ASIC), used for telecommunication equipment. Because there are cases that a device embeds multiple memories for different purposes, RI for each purpose is specified separately.

Some kinds of semiconductor devices connect to external memory devices and have memory controller circuits for external memories. Required information for soft error mitigation for external memory controllers is also specified in this Recommendation.

9 Overview of RI for soft error mitigation measures

The items that are included in the RI, and the objectives of including them are as follows:

1) SER (FIT/Mbit)

   Needed to confirm the frequency of occurrence and validity of errors.

2) Memory capacity (Mbit)

   Needed to estimate SER in memory units.

3) Specification of error detection/correction function and procedure to apply the function

   Needed to apply an effective design for soft error measures as a system.

4) Error notification function

Needed for equipment designers to know how to check the occurrence of a soft error in a device with an embedded memory.

5) Error recovery function

Needed for equipment designers to know how to use a recover function available to the user in devices with embedded memory.

10 RI recommended for each type of semiconductor device

This clause describes RI for each semiconductor device for which it is necessary to correctly estimate the impact of soft errors. The RI provided is used to estimate whether the telecommunication equipment where the device is installed satisfies the soft error reliability target.

10.1 Generic memory

Many of the generic memory devices, SRAM, DRAM and flash memory circuits in Table 8-1 do not have soft error mitigation functions, but some of them do. Therefore, RI is separately described depending on the presence of soft errors.

10.1.1 Generic memory without error correction function

For generic memory, soft error rate per memory capacity (SER in FIT/Mbit) shall be included in RI. It is recommended that types of SER shall be supplied with its measurement method. There are two types of classification. One is SER by measurement method (Table 10-1) and the other is error bits by measurement unit and the number of simultaneous errors (Table 10-2).

Detailed information for each classification is described as follows:

1) Measurement method

Table 10-1 shows classification of SER by measurement methods. Semiconductor vendors shall measure SER of the component by either a real-time test or an accelerated test. In the latter case, vendors shall provide SER for each radiation source (alpha particle and fast neutron beam).

Table 10-1 – Classification of SER

SER test method	Radiation source	Description in the report
Real-time test	–	Real-time SER
Accelerated test	Alpha particle	SER by Alpha particle
	Fast neutron beam	SER by fast neutron beam

Semiconductor vendors shall provide information regarding the measurement method.

This Recommendation does not define measurement methods in detail because they are already defined in [JESD89A].

2) Measurement unit and the number of simultaneous errors

Table 10-2 shows classification of error bits by measurement unit and the number of simultaneous errors. Semiconductor vendors should classify SER by the number of simultaneous errors, i.e., SER of single-bit error and SER of multiple-bit errors. A single-bit error can be neglected if it is corrected by error correction code (ECC) during the estimation of system error rate, such as service reliability (SR) or maintenance reliability (MR) in [ITU-T K.139].

Table 10-2 – Classification of error bits

Measurement unit	Number of simultaneous errors	Description in the report
A whole memory	1 bit	Single-bit error
	2 or more bits	Multiple-bit errors
An address	1 bit	Single-bit error per address
	2 or more bits	Multiple-bit errors per address

This classification is described as follows:

The occurrence rate of simultaneous errors, not in a whole device but in an address, is taken into account when error correction is applied at the time data are read from the memory address. Even if simultaneous multiple-bit errors occur in different addresses in a memory device, all errors can be corrected by ECC without impacting the operation of the equipment, provided that they all are single-bit errors in an address. Therefore, it is important to distinguish the number of errors in an address from the number of errors in the whole memory device.

Device vendors shall provide SER per address by using the labels "single-bit error per address" or "multiple-bit errors per address" to distinguish "single-bit errors" from "multiple-bit errors" in the whole memory device.

An example of simultaneous single-bit errors in multiple addresses is presented in Figure 10-1. The figure shows two single-bit simultaneous errors (red) in the physical layout, but which are single-bit errors in different addresses of the logical layout, and these can be corrected. So, these errors shall be classified as two single-bit errors per address, rather than one multiple-bit error.

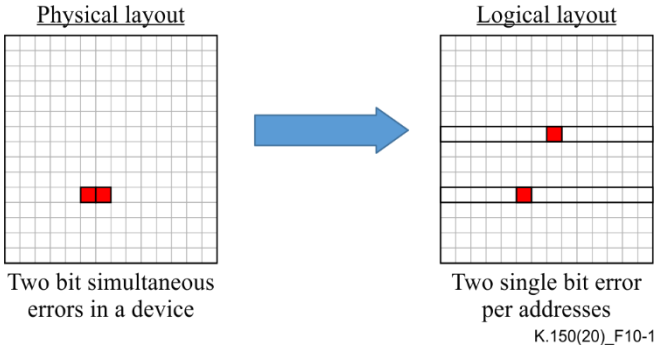

Figure 10-1 – Bit error location in physical and logical layout

10.1.2 Generic memory with error correction function

As shown in clause 9, the followings are specified as RI.

1) Soft error rate (FTI/Mbit)

   Both SERs, when the correction function is enabled and disabled, shall be presented.

2) Memory capacity (Mbit)

   The size of the target memory corresponding to the provided SER value.

3) Specification of error detection/correction function and procedure to apply the function

   Type and detail of embedded soft error detection/correction function. Description of restrictions such as reduction of performance when enabling the function.

   Procedure to enable those functions should be provided as RI.

4) Error notification function

The methods to identify the occurrence of soft errors should be provided as RI. It should include all methods, such as notification of error occurrence and representation of the data recorded in a register. It is desirable that the error notification can determine whether the error is correctable or un-correctable. In addition, if the error is correctable, the error notification should indicate whether an error has occurred or has been corrected already.

5) Error recovery function

RI about error recovery function includes all methods to recover from the situation where self-recovery is not successfully done.

Detailed information of 1) Soft error rate (FIT/Mbit) to be provided as RI is as follows:

1) Measurement method: Refer to 1) Measurement method in clause 10.1.1. The same as that for memories without error correction in the measurement method.

2) Error correction capability: SER shall be classified into "correctable error" or "un-correctable error", as shown in Table 10-3. The SER for each error depends on the error correction capability of the installed function. For example, in the case of ECC using Hamming code, single-bit errors are classified as "correctable error" and multiple-bit errors are classified as "un-correctable error".

The reason to classify the error is as follows:

– Only SER for un-correctable error is required if the error classified as correctable error can be surely corrected without any system failure, since the designer of the system can concentrate only on measures relating to un-correctable error.

– If a system failure can be caused by errors classified as correctable error, SERs for both correctable error and un-correctable error are required. For example, there is a time difference between the generation and the correction of an error, and system failure can happen in between.

In the case of memories with error correction function, it is recommended to count errors for each frame, and the number of frames classified by the number of errors in each frame should be counted. Here, "frame" is defined as a set of memory bits to which an error correction code is applied.

Table 10-3 – Classification of error type

Error correction unit	Error correction capability	Description in the report
Per frame	Correctable	Correctable error
	Un-correctable	Un-correctable error

10.2 Semiconductor devices with embedded memory

10.2.1 FPGA

10.2.1.1 Embedded memories in FPGA

Block random access memory (RAM) and configuration RAM are embedded in FPGA as shown in Figure 10-2. Where, the block RAM is user designed memory used in logic circuits and configuration RAM is memory that stores configuration information of logic circuits mounted on FPGA. When a soft error occurs, incorrect bit data is transmitted from the block random access memory (BRAM) to USER logic or incorrect configuration random access memory (CRAM) bit data may change the circuit on USER Logic. The RI for each type of memory for estimating the soft error reliability is described in clauses 10.2.1.1.1 and 10.2.1.1.2.

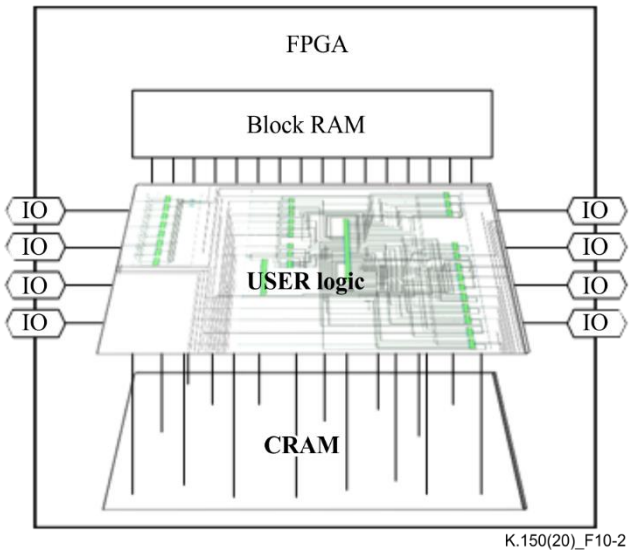

Figure 10-2 – Schematic of the embedded memory in FPGA

10.2.1.1.1 Block RAM (user RAM)

RI presented in clause 10.1.2 are expected to be supplied by device vendors.

If there are documents such as a procedure manual, it is better to clarify the name of the documents.

10.2.1.1.2 Configuration RAM

In addition to the RIs in clause 10.1.2, the following should be included in 3) Specification of error detection/correction function:

The method to calculate the maximum time from error occurrence to error detection and time for correction of soft error.

10.2.2 CPU

10.2.2.1 Cache memory

RI for CPU includes the method to estimate the soft error reliability of the cache memory.

The cache memory is a high-speed memory that operates between CPU and the main memory. Generally, cashe memories are composed of multiple memories, so information for each memory should be provided.

For a description of the RI, refer to clause 10.1.2.

10.2.3 ASSP

10.2.3.1 Embedded memories in ASSP

Three kinds of memories are embedded in ASSP as shown in Figure 10-3. Each kind of memory operates as follows:

1) Setting data storage memory. After data are written, only data retention and readout operations can be performed.
2) Operation control memory. Read and write operations can be performed depending on the operation state, such as switching of the client signal path.
3) Data buffer memory. Read and write operations are continuous, with client signals and control signals passing through.

RI for each kind memory are described in clauses 10.2.3.1.1 to 10.2.3.1.3:

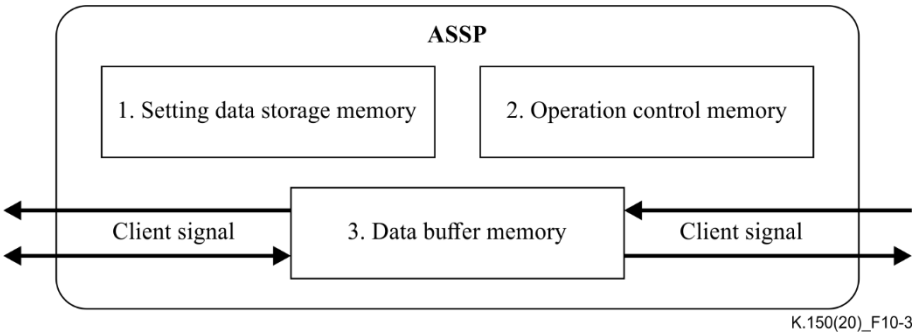

Figure 10-3 – Embedded memories in ASSP

10.2.3.1.1 Setting data storage memory

The impact of soft errors is large as data in the setting data storage memory is usually not overwritten once the setting is completed. Information regarding the functions deployed in the device is very important because the equipment designer cannot add mitigation measures in the device. In particular, information about detection, correction and notification is required for design.

For a description of the required information, refer to clause 10.1.2.

10.2.3.1.2 Operation control memory

The operation control memory is periodically overwritten, and soft errors is corrected in the period. However, a fatal problem may be caused by errors such as an error occurring in a counter that holds statistical information. If the value changes suddenly and exceeds the threshold value, then a function may be triggered and the client signal may be significantly impacted. Therefore, the information is as important as the setting data memory.

For a description of the required information, refer to clause 10.1.2.

10.2.3.1.3 Data buffer memory

Soft errors occurring in the data buffer memory are continuously overwritten with correct data. Therefore, the design is set to 0 FIT because these are correctable errors. However, it is desirable to provide information regarding detection and notification of errors in order to identify the cause of the bit or frame loss of the main signal.

For a description of the required information, refer to clause 10.1.2.

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