Superseded by a more recent version

INTERNATIONAL TELECOMMUNICATION UNION

ITU-T

I.432

TELECOMMUNICATION
STANDARDIZATION SECTOR
OF ITU

(03/93)

INTEGRATED SERVICES DIGITAL NETWORK (ISDN)

ISDN USER-NETWORK INTERFACES

B-ISDN USER-NETWORK INTERFACE – PHYSICAL LAYER SPECIFICATION

ITU-T Recommendation I.432
Superseded by a more recent version

(Previously "CCITT Recommendation")

FOREWORD

The ITU Telecommunication Standardization Sector (ITU-T) is a permanent organ of the International Telecommunication Union. The ITU-T is responsible for studying technical, operating and tariff questions and issuing Recommendations on them with a view to standardizing telecommunications on a worldwide basis.

The World Telecommunication Standardization Conference (WTSC), which meets every four years, established the topics for study by the ITU-T Study Groups which, in their turn, produce Recommendations on these topics.

ITU-T Recommendation I.432 was revised by the ITU-T Study Group XVIII (1988-1993) and was approved by the WTSC (Helsinki, March 1-12, 1993).

NOTES

1 As a consequence of a reform process within the International Telecommunication Union (ITU), the CCITT ceased to exist as of 28 February 1993. In its place, the ITU Telecommunication Standardization Sector (ITU-T) was created as of 1 March 1993. Similarly, in this reform process, the CCIR and the IFRB have been replaced by the Radiocommunication Sector.

In order not to delay publication of this Recommendation, no change has been made in the text to references containing the acronyms "CCITT, CCIR or IFRB" or their associated entities such as Plenary Assembly, Secretariat, etc. Future editions of this Recommendation will contain the proper terminology related to the new ITU structure.

2 In this Recommendation, the expression "Administration" is used for conciseness to indicate both a telecommunication administration and a recognized operating agency.

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B-ISDN USER-NETWORK INTERFACE – PHYSICAL LAYER SPECIFICATION

(Geneva, 1991; revised Helsinki, 1993)

1 Introduction

This Recommendation defines the physical layer interface to be applied to the S_B and T_B reference points of the reference configurations of the B-ISDN user-network interface (UNI) at 155 520 kbit/s and 622 080 kbit/s. It addresses separately the physical media and the transmission system used at these interfaces and addresses also the implementation of the UNI related OAM functions.

The selection of the physical medium for the interfaces at the S_B and T_B reference points should take into account that optical fibre is agreed as the preferred medium to be used to cable customer equipment. However, in order to accommodate existing cabling of customer equipment, other transmission media (e.g. coaxial cables) should not be precluded. Also, implementations should allow terminal interchangeability.

This Recommendation reflects in its structure and content the desire to take care of such early configurations and introduces a degree of freedom when choosing a physical medium at the Physical Layer.

The goal is to have maximum commonality between physical layer functions at the UNI described in this Recommendation and any functions which may be defined in the future at the (network-node interface) NNI.

1.1 Interface location with respect to reference configuration

An interface point I_a is adjacent to the B-TE or the B-NT2 on their network side; interface point I_b is adjacent to the B-NT2 and to the B-NT1 on their user sides (see Figure 1).

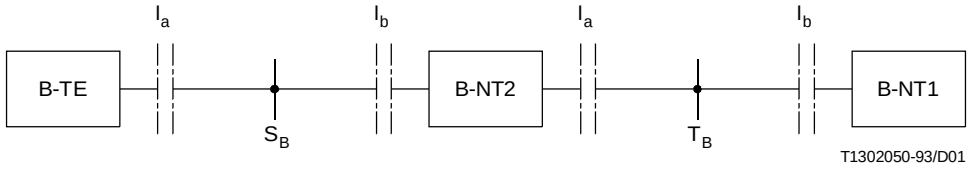


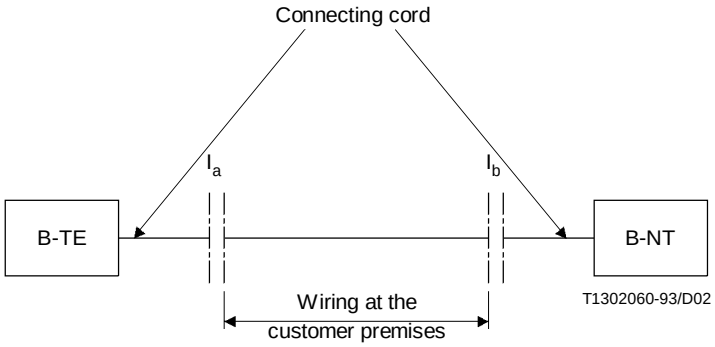
FIGURE 1/I.432

Reference configuration at reference point S_B /T_B

1.2 Interface location with respect to the wiring configuration

The interface points are located between the socket and the plug of the connector attached to the B-TE, B-NT2 or B-NT1. The location of the Interface point is shown in Figure 2.

In this Recommendation, the term “B-NT” is used to indicate network terminating layer 1 aspects of B-NT1 and B-NT2 functional groups, and the term “TE” is used to indicate terminal terminating layer 1 aspects of B-TE1, B-TA and B-NT2 functional groups, unless otherwise indicated.



NOTE – The length of the connecting cord can be zero.

FIGURE 2/I.432

Wiring configuration

2 Physical medium characteristics of the UNI at 155 520 kbit/s

2.1 Characteristics of the interface at the T_B reference point

2.1.1 Bit rate and interface symmetry

The bit rate of the interface is 155 520 kbit/s. The interface is symmetric, i.e. it has the same bit rate in both transmission directions.

The nominal bit rate in free running clock mode shall be 155 520 kbit/s with a tolerance of ± 20 ppm.

2.1.2 Physical characteristics

Both optical and electrical interfaces are recommended. The implementation selected depends on the distance to be covered and user requirements arising from the details of the installation.

2.1.2.1 Electrical interface

2.1.2.1.1 Interface range

The maximum range of the interface depends on the specific attenuation of the transmission medium used. For example a maximum range of about 100 metres for microcoax (4mm diameter) and 200 metres for CATV type (7mm diameter) will be achieved.

2.1.2.1.2 Transmission medium

Two coaxial cables, one for each direction, are recommended. The wiring configuration is point-to-point.

The impedance shall be 75 Ohms with a tolerance of ± 5% in the frequency range 50 MHz to 200 MHz.

The attenuation of the electrical path between the interface points I_a and I_b shall be assumed to follow an approximate sqrt (f) law and to have a maximum insertion loss of 20 dB at a frequency of 155 520 kHz.

2.1.2.1.3 Electrical parameters at interfaces points I_a and I_b

The digital signal presented at the output port and the port impedance should conform to Table 11/G.703 and Figures 24/G.703 and 25/G.703 for the interface at 155.520 Mbit/s.

The digital signal presented at the input port and the port impedance should conform to Table 11/G.703 and Figures 24/G.703 and 25/G.703 for the interface at 155.520 Mbit/s modified by the characteristics of the interconnecting coaxial pair.

2.1.2.1.4 Electrical connectors

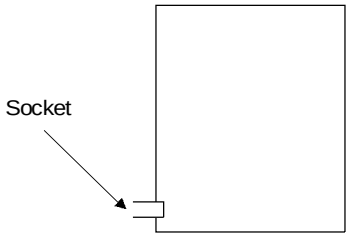
The presentation of interface point I_b at B-NT1 or B-NT2 is via a socket.

The presentation of interface point I_a at B-TE or B-NT2 is using either

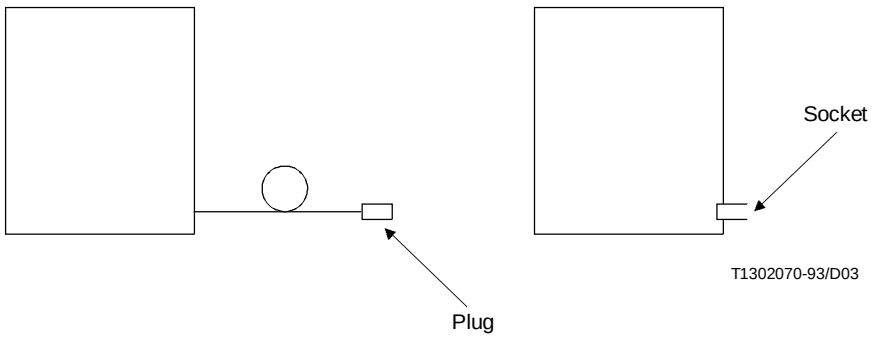
a) a socket, i.e. the connection is to be made to the equipment toward the network with a cable with plugs on both ends; or

b) an integral connecting cord with plug on the free end.

See Figure 3.



Presentation of interface point I_b at B-NT1 and B-NT2



Presentation of interface point I_a at B-TE and B-NT2

FIGURE 3/I.432

Connector types

2.1.2.1.5 Line coding

The line coding shall be coded mark inversion (CMI), see 12.1/G.703).

2.1.2.1.6 EMC/EMI requirements

Shielding properties of connectors and cables are defined by the specification of the respective values for the surface transfer impedance (STI). The template indicating the maximum STI values for CATV cables is given in Figure 4. The applicability of these values for microcoax cables remains for further study. For connectors, these template values shall be multiplied by 10 (20 dB).

The immunity of the interface against induced noise on the transmission medium should be specified by means of a terminal failure voltage (TFV) which is overlaid to the digital signal at the output port. Figure 5 shows a possible measurement configuration.

The receiver should tolerate a sinusoidal TFV with the values defined in Figure 6 and Table 1 without degradation of the bit error ratio (BER) performance.

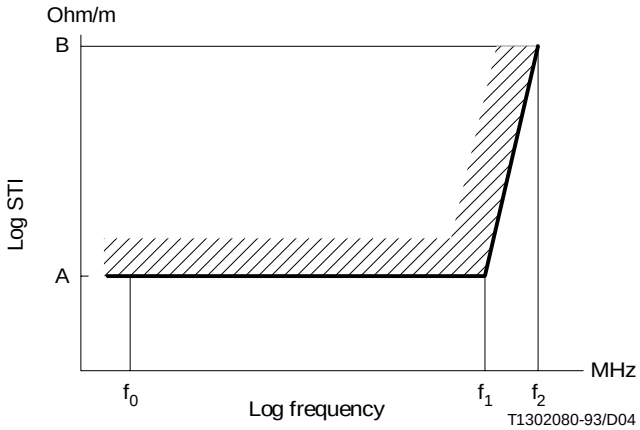


FIGURE 4/I.432

Maximum STI values as function of frequency

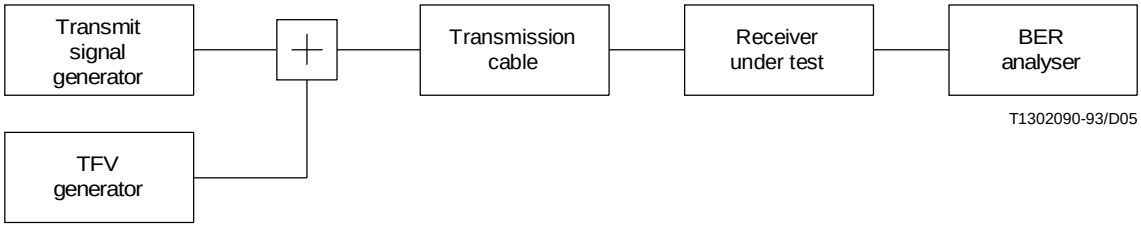


FIGURE 5/I.432

Measurement configuration

2.1.2.2 Optical interface

2.1.2.2.1 Attenuation range

The attenuation of the optical path between the specification points I_a S and I_b R shall be in the range of 0 dB to 7 dB (see 2.1.2.2.3.3).

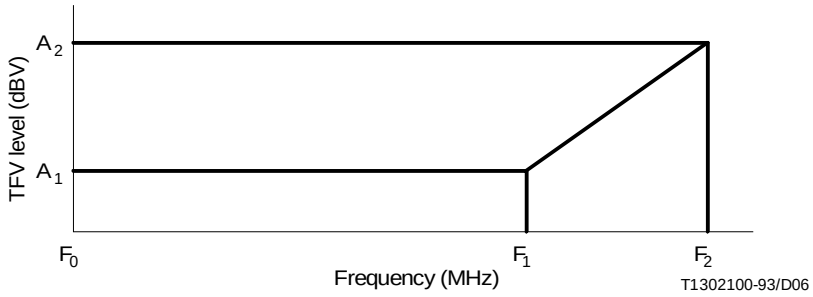


FIGURE 6/I.432

Terminal failure voltage frequency response

TABLE 1/I.432

Terminal failure voltage values

Frequency (MHz)	TFV amplitude (dBV) (0 dBV = 1 V_{op})
F0 = 1	
F1 = 200	A1 ≥ –17
F2 = 400	A2 ≥ –11

2.1.2.2.2 Transmission medium

The transmission medium shall consist of two single mode fibres one for each direction, according to Recommendation G.652 .

Some national applications may use multimode fibres.

2.1.2.2.3 Optical parameters

2.1.2.2.3.1 Line coding

The line coding shall be non return to zero (NRZ).

The convention used for optical logic level is:

- emission of light for a binary ONE;
- no emission of light for a binary ZERO.

The extinction ratio must be in accordance with I.1/G.957.

2.1.2.2.3.2 Operating wavelength

The operating wavelength shall be around 1310 nm (second window).

2.1.2.2.3.3 Input and output port characteristics

The optical parameters will be in accordance with I.1/G.957. Some national application may use optical parameters for multimode fibres.

The specification points associated with interface points I_a and I_b correspond to measurement "reference points" S and R as defined in Recommendation G.957. The optical parameters are specified for the transmitter and receiver at these specification points and for the optical path between these specification points, i.e. the connector at the interface is considered to be part of the equipment and not part of the fibre installation.

2.1.2.2.4 Optical connectors

The presentation of interface point I_b at B-NT1 or B-NT2 is via a socket. The presentation of interface point I_a at B-TE or B-NT2 is using either

a) a socket, i.e. the connection is to be made to the equipment toward the network with a cable with plugs on both ends; or

b) an integral connecting cord with a plug on the free end.

See Figure 3.

2.1.2.2.5 Safety requirements

For safety reasons the parameters for IEC 825 class 1 devices shall not be exceeded even under failure conditions.

2.2 Characteristics of the interface at the S_B reference point

For further study.

3 Physical medium characteristics of the UNI at 622 080 kbit/s

3.1 Characteristics of the interface at the T_B reference point

3.1.1 Bit rate and interface symmetry

The bit rate of the interface in at least one direction is 622 080 kbit/s. The symmetry of the interface is for further study. The following possible interfaces have been identified:

a) an asymmetrical interface with 622 080 kbit/s in one direction and 155 520 kbit/s in the other direction;

b) a symmetrical interface with 622 080 kbit/s in both directions.

NOTE – Other solutions are for further study.

If option a) is chosen, then the 155 520 kbit/s component should comply with the characteristics of indicated in 2.

The nominal bit rate in free running clock mode shall be 622 080 kbit/s with a tolerance of ± 20 ppm.

3.1.2 Physical characteristics

3.1.2.1 Electrical interface

The feasibility of an electrical interface is for further study.

3.1.2.2 Optical interface

3.1.2.2.1 Attenuation range

The attenuation of the optical path between the specification points I_a S and I_b R shall be in the range of 0 dB to 7 dB (see 3.1.2.2.3.3).

3.1.2.2.2 Transmission medium

The transmission medium shall consist of two single mode fibres one for each direction, according to Recommendation G.652 .

3.1.2.2.3 Optical parameters

3.1.2.2.3.1 Line coding

The line coding shall be non return to zero (NRZ)

The convention used for optical logic level is:

– emission of light for a binary ONE;

– no emission of light for a binary ZERO.

The extinction ratio shall be in accordance with I.4/G.957 .

3.1.2.2.3.2 Operating wavelength

The operating wavelength shall be around 1310 nm (second window).

3.1.2.2.3.3 Input and output port characteristics

The optical parameters will be in accordance with I.4/G.957. Some national application may use optical parameters for multimode fibres.

The specification points associated with interface points I_a and I_b correspond to measurement "reference points" S and R as defined in Recommendation G.957. The optical parameters are specified for the transmitter and receiver at these specification points and for the optical path between these specification points, i.e. the connector at the interface is considered to be part of the equipment and not part of the fibre installation.

3.1.2.2.4 Optical connectors

The presentation of interface point I_b at B-NT1 or B-NT2 is via a socket. The presentation of interface point I_a at B-TE or B-NT2 is using either

a) a socket, i.e. the connection is to be made to the equipment toward the network with a cable with plugs on both ends; or

b) an integral connecting cord with a plug on the free end.

See Figure 3.

3.1.2.2.5 Safety requirements

For safety reasons the parameters for IEC 825 class 1 devices should not be exceeded even under failure conditions.

3.2 Characteristics of the interface at the S_B reference point

For further study.

4 Functions provided by the transmission convergence sublayer

4.1 Transfer capability

4.1.1 Interface at 155 520 kbit/s

At the physical level at the interface at the T_B reference point the bit rate is 155 520 kbit/s. The maximum bit rate available for user information cells, signalling cells and ATM and higher layers OAM information cells, excluding physical layer frame structure octets or physical layer cells, transported in bytes or cells, is 149 760 kbit/s.

4.1.2 Interface at 622 080 kbit/s

At the physical level at the interface at the T_B reference point, the bit rate is 622 080 kbit/s in at least one direction (see 3.1.1). The maximum bit rate available for user information cells, signalling cells and ATM and higher layers OAM information cells, excluding physical layer frame structure octets or physical layer cells, is 599 040 kbit/s.

4.2 Transmission frame adaptation

The ATM cell structure is defined in Recommendation I.361. ATM cells may be carried in one of two formats; as a continuous stream of cells in a cell based format or as cells carried in an SDH-based frame structure.

4.2.1 Physical layer for the cell-based interface

4.2.1.1 Timing

At the customer side of the interface at the T_B reference point, the cell-based physical layer may derive its timing from the signal received across the interface or provide it locally by the clock of the customer equipment.

4.2.1.2 Interface structure for 155 520 kbit/s and 622 080 kbit/s

The interface structure consists of a continuous stream of cells. Each cell contains 53 octets.

The maximum spacing between successive physical layer cells is 26 ATM layer cells, i.e. after 26 contiguous ATM layer cells have been transmitted a physical layer cell is inserted in order to adapt the transfer capability to the interface rate. Physical layer cells are also inserted when no ATM layer cells are available.

The physical layer cells which are inserted can be either “idle cells” (see 4.4) or physical layer OAM cells (see 4.2.1.3), depending on the OAM requirements.

4.2.1.3 OAM implementation

4.2.1.3.1 Transmission overhead allocation

Physical layer OAM cells are used for the conveyance of the physical layer OAM information. How often OAM cells are inserted should be determined by OAM requirements. However, there can be no more than one PL-OAM cell every 27 cells and not be less than one PL-OAM cell every 513 cells per flow in operational status. It is recognized that during some phases, for example start-up, it would be desirable to increase the insertion rate of the PL-OAM cell for improving the system response. The functional requirements for increasing the PL-OAM insertion rate requires further study. These spacings would apply only when the flow is actually implemented; it is recognized that not all applications will require implementations of all flows.

4.2.1.3.2 OAM cell identification

Recommendation I.610 identifies three types of PL-OAM flows carried by maintenance cells using a specific pattern in the header.

F1 Regenerator level;

F2 Digital section level;

F3 Transmission path level.

The F1 cell carries the OAM functions for the regenerator level.

This flow is inserted in the cell flow on a recurrent basis. If these PL-OAM cells have to take priority over an ATM cell, this has to be done without restricting ATM layer transfer capability. The minimum periodicity of the cell is provisionally defined by the requirements on availability of the section as one F1 cell in 513 cells.

The OAM flow F2 is not used and the corresponding functions are supported by the F3 OAM flow because there is no transmission frame passed across the cell based UNI.

The F3 cell carries the OAM functions for the transmission path level.

These flows are inserted in the cell flow on a recurrent basis. If these PL-OAM cells have to take priority over an ATM cell, this has to be done without restricting ATM layer transfer capability. The minimum periodicity of the cell is provisionally defined by the requirements on availability of the path as one F3 cell in 513 cells.

The physical layer OAM cells must have a unique header so that they can be properly identified by the physical layer at the receiver. The patterns to be used are shown in Table 2. The header patterns shown are given prior to scrambling.

The possible need to identify other header values among those reserved for the use of the physical layer (see 2.2.1/I.361) to accommodate future identified OAM flows is for further study.

TABLE 2/I.432

Header pattern for OAM cell identification (Note)

Flow	Octet 1	Octet 2	Octet 3	Octet 4	Octet 5
F1	00000000	00000000	00000000	00000011	HEC = Valid code 01011100
F3	00000000	00000000	00000000	00001001	HEC = Valid code 01101010
NOTE – There is no significance to any of these individual fields from the point of view of the ATM layer, as physical layer OAM cells are not passed to the ATM layer.					

4.2.1.3.3 Allocation of OAM functions in information field

A provisional octet allocation for the F1 PL-OAM and F3 PL-OAM cells is shown in Figure 7.

The following fields are identified for the F3 flow:

- PL-OAM sequence number (PSN) – It is designed so as to have a sufficiently large cycle compared with the duration of cell loss and insertion, 8 bits are allocated to PSN. The counting is then done modulo 256.

- Number of included cells (NIC) – Gives the number of cells included between the previous and the present F3 PL-OAM cell. The length of this field is proposed to monitor 512 cells (provisionally). It includes the number of ATM cells and idle cells but not the PL-OAM cells.

- Transmission path error monitoring and reporting which includes the fields defined below:

  a) Monitoring block size (MBS) – It is selected by balancing efficiency and monitoring accuracy. MBS = 64 cells excluding PL-OAM cells is proposed as an upper limit, but the entire octet is allocated.

  b) Number of monitored blocks (NMB-EDC) – Gives the number of blocks included between this cell and the previous F3 OAM cell. This means the number of blocks for which error detection codes are contained in the following octets NMB-EDC = 8 is proposed. The entire octet is allocated.

  c) Error detection code (EDC) – this code is a BIP-8 calculated on a block of MBS cells repeated for each monitored block. An octet is allocated for each block.

  d) Number of monitored blocks at the far end (NMB-EB) – Gives the number of transmission path far end block errors carried in the following octets, NMB-EB = 8 is proposed. The entire octet is allocated.

  e) Transmission path far end block error (TP-FEBE), (EB1, EB2, …, EB8): This reports the number of parity violations in each block. Four bits are necessary to indicate the number of parity violations in a BIP-8. With NMB-EB = 8, a total of 4 octets are necessary.

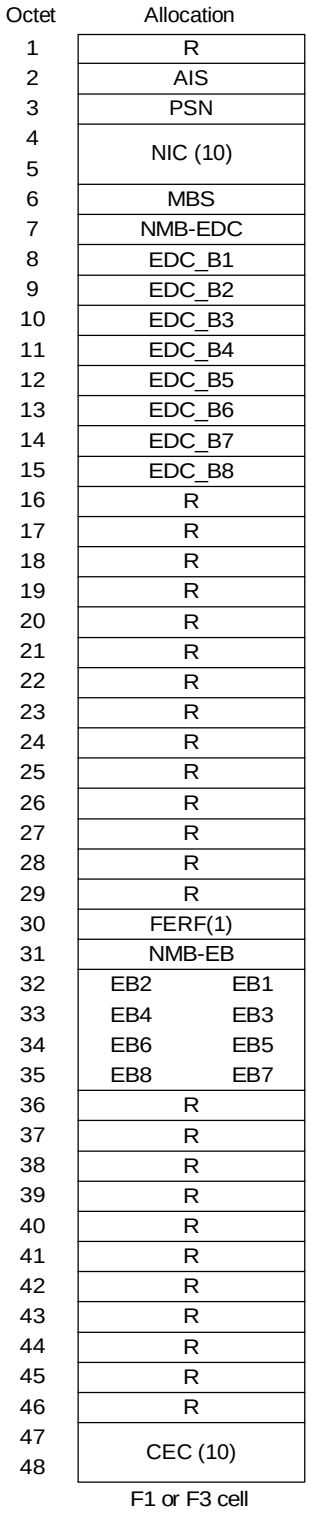


FIGURE 7/I.432

Allocation of OAM functions in information field

– Transmission path alarm indication signal (TP-AIS) – One octet is allocated (the proposed coding is all "1").

– Transmission path far end received failure (TP-FERF) – A bit is allocated. It is set when one of the defects (LOC, LOM) or AIS (see 4.2.1.3.4) is detected.

– Cell error control (CEC) – Is used to detect errors in the cell payload. A CRC 10 is proposed.

– Reserved field (R) – Contains the octet pattern of "01101010", which is the same as that of the idle cell.

The following fields are identified for the F1 flow:

– PL-OAM sequence number (PSN) – It is designed so as to have a sufficiently large cycle compared with the duration of cell loss and insertion, 8 bits are allocated to PSN. The counting is then done modulo 256.

– Number of included cells (NIC) – Gives the number of cells included between the previous and the present F1 PL-OAM cell. The length of this field is proposed to monitor 512 cells (provisionally). It includes the number of ATM cells and idle cells but not the PL-OAM cells.

– Section error monitoring and reporting which includes the fields defined below:

1) Monitoring block size (MBS) – It is selected by balancing efficiency and monitoring accuracy. MBS = 64 cells is proposed as an upper limit, but the entire octet is allocated.

2) Number of monitored blocks (NMB-EDC) – Gives the number of blocks included between this cell and the previous F1 OAM cell. This means the number of blocks for which error detection codes are contained in the following octets NMB-EDC = 8 is proposed. The entire octet is allocated.

3) Error detection code (EDC) – This code is a BIP-8 calculated on a block of MBS cells repeated for each monitored block. An octet is allocated for each block.

4) Number of monitored blocks at the far end (NMB-EB) – Gives the number of transmission path far end block errors carried in the following octets, NMB-EB = 8 is proposed. The entire octet is allocated.

5) Section far end block error (S-FEBE), (EB1, EB2, …, EB8) – This reports the number of parity violations in each block. Four bits are necessary to indicate the number of parity violations in a BIP-8. With NMB-EB = 8, a total of 4 octets are necessary.

– Section alarm indication signal (S-AIS) – One octet is allocated (the proposed coding is all "1").

– Section far end received failure (S-FERF) – A bit is allocated. It is set when one of the defects (LOC, LOM, Unacceptable error performance) is detected.

– Cell error control (CEC) – Is used to detect errors in the cell payload. A CRC 10 is proposed.

– Reserved field (R) – Contains the pattern of the octet of the idle cells (see 4.4).

Other fields such as activation/deactivation or switch-on/switch-off status of the NT2 are for further study.

4.2.1.3.4 Maintenance signals

The following maintenance signals are defined:

– Transmission path alarm indication signal (TP-AIS) – It is used to alert associated termination point in the direction of transmission that a failure has been detected and alarmed.

– Transmission path far end received failure (TP-FERF) – It is provided to alert the equipment in the opposite direction of transmission that a defect has been detected along the path. It is set when an LOC, LOM or AIS signal has been detected at the path level. The time to set this signal must be as short as possible but long enough to filter intermittent defect informations. This time has to be defined. Loss of cell delineation (LOC) is provided by the cell delineation algorithm. The time to indicate this state has to be defined. Loss of OAM cell (LOM) is detected when no F3 OAM cell is received when the maximum space between two F3 OAM cells is exceeded. This defect is declared when n (n to be defined) successive anomalies are detected. The method of detection of the AIS condition is for further study.

– Section alarm indication signal (S-AIS) – It is used to alert the equipment in the direction of transmission that a failure has been detected and alarmed.

– Section far end received failure (S-FERF) – It is provided to alert the equipment in the opposite direction of transmission that a defect has been detected along the path. It is set when an LOC, LOM or unacceptable error performance has been detected at the regenerator section level. The time to set this signal must be as short as possible but long enough to filter intermittent defect informations: it has to be defined. Loss of cell delineation (LOC) is provided by the cell delineation algorithm. The time to indicate this state has to be defined. Loss of OAM cell (LOM) is detected when no F1 OAM cell is received and the maximum space between F1 OAM cells is exceeded. This defect is declared when n (to be defined) successive anomalies are detected. The method of detection of unacceptable error performance requires further study.

4.2.1.3.5 Transmission performance monitoring

Transmission performance monitoring across the UNI is performed to detect and report transmission errors. This function is performed on the ATM layer cells and idle cells, not on the PL-OAM cells. It is calculated on a block of cells. An F3 OAM cell carries the result for the monitoring of a certain number of blocks.

– Error performance reporting – This function reports to the equipment in the opposite direction of transmission, the results of the path error monitoring carried out (FEBE); for a BIP it gives the number of parity violations in each block, calculated at the receiving end by comparison with the result carried by the cell.

4.2.1.3.6 Control communication

The provision of a data communication channel is for further study.

4.2.1.3.7 OAM procedures

For further study.

4.2.2 Physical layer for SDH-based interface

4.2.2.1 Timing

In normal operation, timing for the transmitter is locked to the timing received from the network clock. The tolerance under fault conditions is 155 520 kbit/s ± 20 ppm.

4.2.2.2 Interface structure at 155.520 kbit/s

The bit stream of the interface has an external frame based on the synchronous digital hierarchy (SDH) as described in Recommendations G.707, G.708, and G.709. Specifically, the frame is given in Recommendation G.709, and illustrated in Figure 8, the application of the SDH frame synchronous scrambler is described in 2.4/G.709.

The ATM cell stream is first mapped into the C-4 and then mapped in the VC-4 container along with the VC-4 path overhead (see Figure 8). The ATM cell boundaries are aligned with the STM-1 octet boundaries. Since the C-4 capacity (2340 octets) is not an integer multiple of the cell length (53 octets), a cell may cross a C-4 boundary.

The AU-4 point (octets H1 and H2 in the SOH) is used for finding the first octet of the VC-4. Path overhead (POH) octets J1, B3, C2 and G1 are utilized. Use of the remaining POH octets is for further study.

For all representations shown in this Recommendation in binary format, bits are numbered within the octet as shown in Figure 9 with the order of transmission being from left to right.

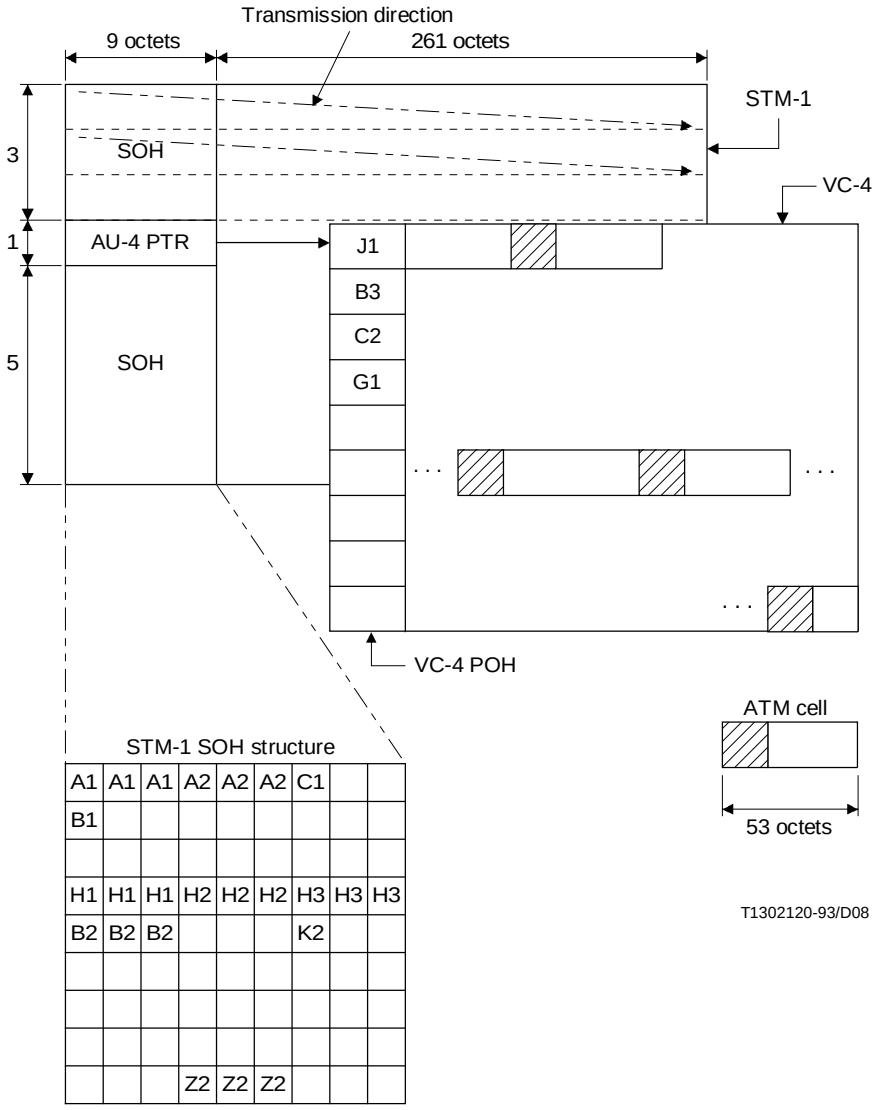
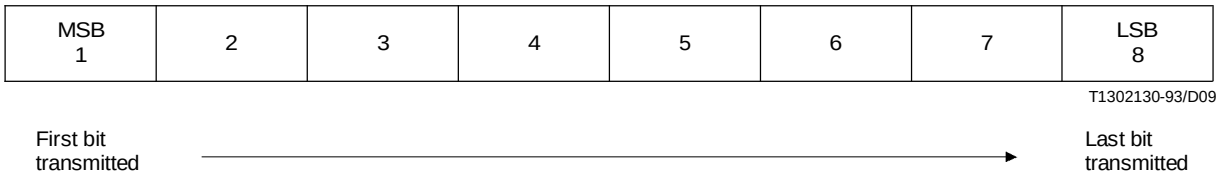


FIGURE 8/I.432

155 520 kbit/s frame structure for SDH based UNI



NOTE – The bit numbering used in this figure is different from the convention used in Recommendation I.361 but in accordance with Recommendation G.709.

FIGURE 9/I.432

Order of transmission of bits within a byte

4.2.2.3 Interface structure at 622 080 kbit/s

The bit stream of the interface has an external frame based on the synchronous digital hierarchy (SDH) as described in Recommendations G.707, G.708, G.709. Specifically, the AU-4-4c structure as given in 3.1.7/G.709 is specified, and is illustrated in Figure 10, the application of the SDH frame synchronization scrambler is described in 2.4/G.709.

The ATM cell stream is first mapped into the C-4-4c and then packed in the VC-4-4c container along with the VC-4-4c path overhead (see Figure 10). The ATM cell boundaries are aligned with the STM-4 octet boundaries. Since the C-4-4c capacity (9360 octets) is not an integer multiple of the cell length (53 octets), a cell may cross a C-4-4c boundary.

The AU-pointers are used for finding the first octet of the VC-4-4c. Path overheads octets J1, B3, C2 and G1 are utilized. Use of the remaining POH octets is for further study.

4.2.2.4 OAM implementation

4.2.2.4.1 Transmission overhead allocation

Transmission overhead allocation for the SDH physical layer functions (listed in Table 1/I.610) is given in Table 3. Use of these overheads (e.g. for frame alignment, AU-pointer generation/interpretation, bit interleaved parity (BIP) code calculation, etc.) shall be in accordance with specifications in Recommendations G.708 and G.709 for the SDH network node interface.

4.2.2.4.2 Maintenance signals

Two types of maintenance signals are defined for the physical layer to indicate the detection and location of a transmission failure. These signals are:

- alarm indication signal (AIS);
- far end receive failure (FERF),

which are applicable at both the SDH section and path layers of the physical layer.

AIS is used to alert associated termination point in the direction of transmission that a failure has been detected and alarmed.

Far end receive failure (FERF) is used to alert associated termination point in the opposite direction of transmission that a failure has been detected. Path FERF alerts the path termination point in the opposite direction of transmission that a failure has occurred along the path. Path FERF should be also used to indicate loss of cell delineation.

Generation and detection of section and path AIS or FERF shall be in accordance with Recommendation G.709.

4.2.2.4.3 Transmission performance monitoring

Transmission performance monitoring across the UNI is performed to detect and report transmission errors. Performance monitoring is provided for the SDH section and for the path corresponding respectively to maintenance flows F2 and F3 in Figure 4/I.610.

At the SDH section (F2 flow), monitoring of the incoming signal is performed using the BIP-24 or BIP-96 inserted into the B2 field (for the 155 520 kbit/s bit rates and 622 080 kbit/s, respectively). Monitoring of the outgoing signal is performed using the far end block error (FEBE). This error count, obtained from comparing the calculated BIP and the B2 value of the incoming signal at the far end, is inserted in a Z2 field and sent back: it reports to the near end section termination point about the error performance of its outgoing signal as FEBE.

Similar to the SDH section, at the SDH path (F3 flow), monitoring of the incoming signal is performed using the BIP-8 of the B3 octet. Monitoring of the outgoing signal is performed using the path FEBE of bits 1-4 of the G1 octet.

Regenerator section monitoring (F1 flow) across the UNI is optional. If required, the incoming signal is monitored using the BIP-8 of the B1 octet. Capabilities in the SDH section overhead for monitoring the outgoing signal are not provided.

Further definitions are stated in Recommendation G.708.

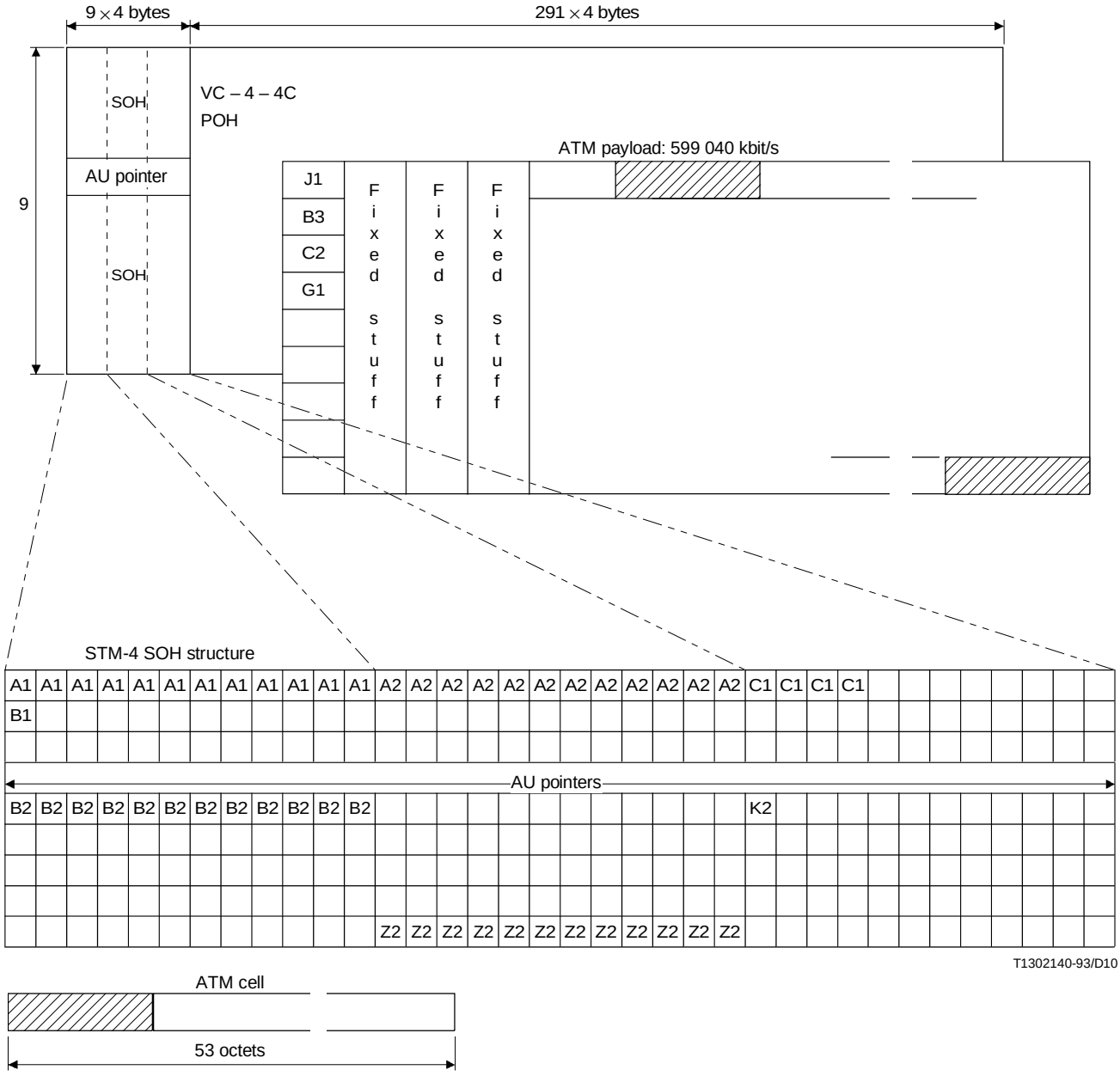


FIGURE 10/I.432

622 080 kbit/s frame structure for SDH based UNI

4.2.2.4.4 Control communication

Section layer communication channels and orderwires across the UNI are not required and are not provided.

Additional functions such as loopbacks (or their functional equivalent) or path layer communication channels are for further study.

The use of octets K1 and K2 (bits 1-5) for automatic protection switching across the UNI is for further study.

4.2.2.4.5 OAM procedures

For further study.

TABLE 3/I.432

SDH overhead octets allocation at B-UNI

Octet	Function	Coding (Note 1)
STM section overhead		
A1, A2	Frame alignment	
C1	STM-1 identifier	
B1	Regenerator section error monitoring (Note 2)	BIP-8
B2	Multiplex section error monitoring	BIP-24 (155 520 kbit/s) BIP-96 (622 080 kbit/s)
H1, H2	AU pointer, Path AIS	All 1s
H3	Pointer action	
K2 (bits 6 to 8)	Multiplex section AIS (Note 6) multiplex section FERF	111/110
Z2 (Note 4)	Section error reporting (FEBE)	B2 error count
VC path overhead		
J1	Path ID/verification	
B3	Path error monitoring	BIP-8
C2	Path signal label	ATM cells (Note 3)
G1(bits 1 to 4)	Path error reporting (FEBE)	B3 error count
G1(bit 5)	Path FERF (Note 5)	1

NOTES

1 Only octet coding relevant to OAM function implementation is listed.

2 The use of B1 for regenerator section error monitoring across the UNI is application dependent and is therefore optional.

3 Signal label code for ATM cell payload is 0001 0011.

4 Using the notation of Recommendation G.708, the bits to be used are bits (2 to 8) of octet S (9, 6, 1) in the case of the interface at 155 520 kbit/s and bits (2 to 8) of octet S (9, 4, 3) in the case of the interface at 622 080 kbit/s.

5 Path FERF should also be used to indicate loss of cell delineation.

6 The applicability of multiplex section AIS (MS-AIS) at the B-UNI is for further study.

7 The bit numbering of this table is different from the conventions used in Recommendation I.361, but in accordance with Recommendation G.709.

4.3 Header error control

4.3.1 Header error control functions

The header error control (HEC) covers the entire cell header. The code used for this function is capable of either

– single-bit error correction, or

– multiple-bit error detection.

The detailed description of the HEC procedure is given in 4.3.2. Briefly, the transmitting side computes the HEC field value. The receiver has two modes of operation as shown in Figure 11. The default mode provides for single-bit error correction. Each cell header is examined and, if an error is detected, one of two actions takes place. The action taken depends on the state of the receiver. In “correction mode” only single-bit errors can be corrected and the receiver switches to “detection mode”. In “detection mode”, all cells with detected header errors are discarded. When a header is examined and found not to be in error, the receiver switches to “correction mode”. The term “no action” in Figure 11 means no correction is performed and no cell is discarded.

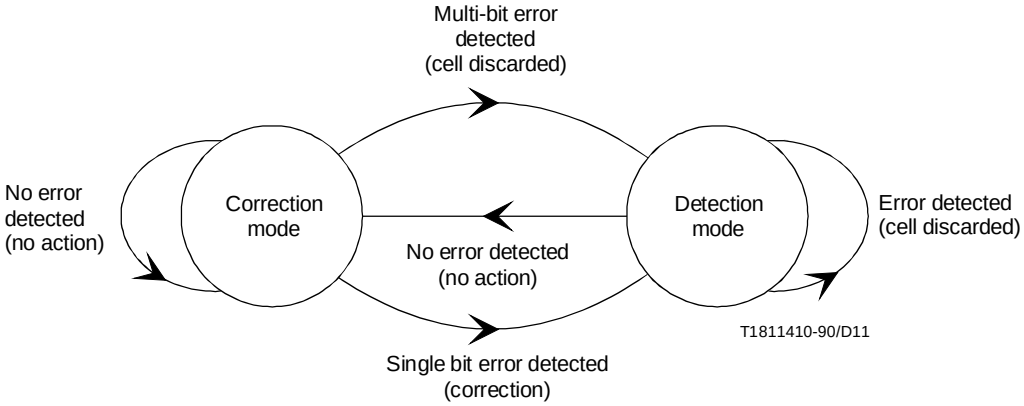


FIGURE 11/I.432

HEC: Receiver modes of operation

The flow chart in Figure 12 shows the consequence of errors in the ATM cell header. The error protection function provided by HEC provides both recovery from single-bit header errors, and a low probability of the delivery of cells with errored headers under bursty error conditions. The error characteristics of fibre-based transmission systems appear to be a mix of single-bit errors and relatively large burst errors. For some transmission systems the error correction capability might not be invoked.

Annex A gives information on how random bit errors impact the probability of occurrence of discarded cells and valid cells with errored headers.

4.3.2 Header error control (HEC) sequence generation

The transmitter calculates the HEC value for the first four octets of the ATM header and inserts the result in the HEC octet.

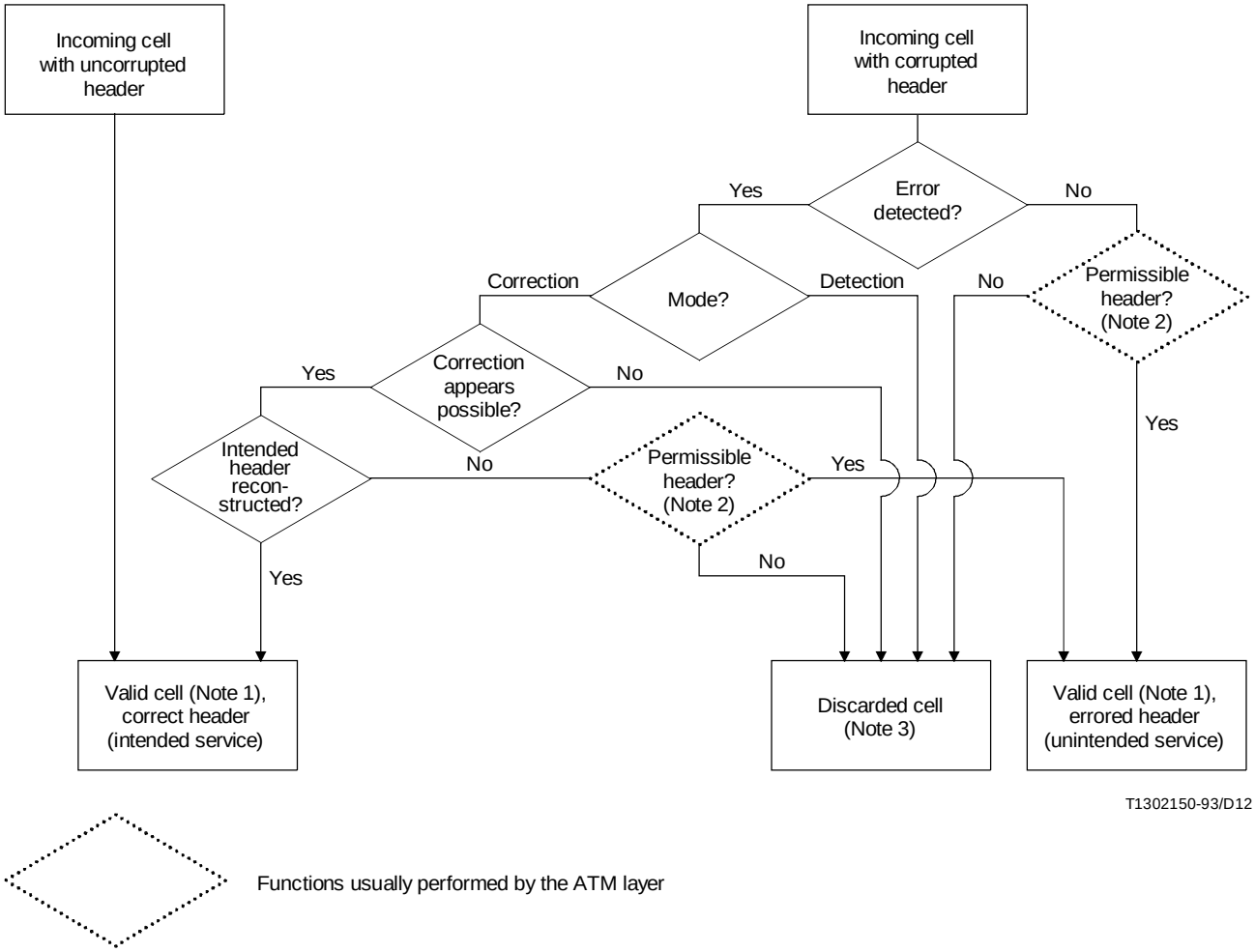
The notation used to describe the header error control is based on the property of cyclic codes. [For example a code vector such as 1000000100001 can be represented by a polynomial $P(x) = x^{12} + x^5 + 1$.] The elements of an n-element code word are thus the coefficients of a polynomial of order $n - 1$. In this application, these coefficients can have the value 0 or 1 and the polynomial operations are performed using modulo 2 operations. The polynomial representing the content of a header excluding the HEC field is generated using the first bit of a header as the coefficient of the highest order term.

The HEC field shall be an 8-bit sequence. It shall be the remainder of the division (modulo 2) by the generator polynomial $x^8 + x^2 + x + 1$ of the product x^8 multiplied by the content of the header excluding the HEC field.

At the transmitter, the initial content of the register of the device computing the remainder of the division is preset to all 0s and is then modified by division of the header excluding the HEC field by the generator polynomial (as described above); the resulting remainder is transmitted as the 8-bit HEC.

To significantly improve the cell delineation performance in the case of bit-slips the following is recommended:

- the check bits calculated by the use of the check polynomial are added (modulo 2) to an 8-bit pattern before being inserted in the last octet of the header;
- the recommended pattern is “01010101” (the left bit is the most significant bit);
- the receiver must subtract (equal to add modulo 2) the same pattern from the 8 HEC bits before calculating the syndrome of the header.



NOTES

1 Definition of “valid cell”: A cell where the header is declared by the header error control process to be free of errors (Recommendation I.113).

2 An example of an impermissible header is a header whose VPI/VCI is neither allocated to a conneciton nor pre-assigned to a particular function (idle cell, OAM cell, etc.). In many instances, the ATM layer will decide if the cell header is permissible.

3 A cell is descarded if its header is declared to be invalid; or if the header is declared to be valid and the resulting header is impermissible.

FIGURE 12/I.432

Consequences of errors in ATM cell header

This operation in no way affects the error detection/correction capabilities of the HEC.

As an example if the first 4 octets of the header were all zeros the generated header before scrambling would be "00000000 00000000 00000000 00000000 01010101". The starting value for the polynomial check is all "0"s.

4.4 Idle cells

Idle cells cause no action at a receiving node except for cell delineation including HEC verification. They are inserted and discarded for cell rate decoupling.

Idle cells are identified by the standardized pattern for the cell header[1)] shown in Table 4.

TABLE 4/I.432

Header pattern for idle cell identification

	Octet 1	Octet 2	Octet 3	Octet 4	Octet 5
Header pattern	00000000	00000000	00000000	00000001	HEC = Valid code 01010010

The content of the information field is "01101010" repeated 48 times.

4.5 Cell delineation and scrambling

4.5.1 Cell delineation and scrambling objectives

Cell delineation is the process which allows identification of the cell boundaries.

The ATM cell header contains a header error control (HEC) field which is used to achieve cell delineation.

The ATM signal is required to be self-supporting in the sense that it has to be transparently transported on every network interface without any constraints from the transmission systems used.

Scrambling will be used to improve the security and robustness of the HEC cell delineation mechanism as described in 4.5.1.1. In addition, it helps randomizing the data in the information field for possible improvement of the transmission performance.

Any scrambler specification must not alter the ATM header structure (as described in Recommendation I.361), header error control (as described in 4.3), and cell delineation algorithm (as described in 4.5.1.1).

4.5.1.1 Cell delineation algorithm

Cell delineation is performed by using the correlation between the header bits to be protected (32 bits) and the relevant control bits (8 bits) introduced in the header by the HEC (header error control) using a shortened cyclic code with generating polynomial $x^8 + x^2 + x + 1$.

Figure 13 shows the state diagram of the HEC cell delineation method.

NOTE – The "correct HEC" means the header has no bit error (syndrome is zero) and has not been corrected.

1) There is no significance to any of these individual fields from the point of view of the ATM Layer, as idle cells are not passed to the ATM Layer.

The details of the state diagram are described below:

1) In the HUNT state, the delineation process is performed by checking bit by bit for the correct HEC (i.e. syndrome equals zero) for the assumed header field. For the cell based Physical Layer, prior to scrambler synchronization, only the last six bits of the HEC are to be used for cell delineation checking. For the SDH-based interface, all 8 bits are used for acquiring cell delineation. Once such an agreement is found, it is assumed that one header has been found, and the method enters the PRESYNCH state. When octet boundaries are available within the receiving Physical Layer prior to cell delineation as with the SDH-based interface, the cell delineation process may be performed octet by octet.

2) In the PRESYNCH state, the delineation process is performed by checking cell by cell for the correct HEC. The process repeats until the correct HEC has been confirmed DELTA times consecutively. If an incorrect HEC is found, the process returns to the HUNT state.

3) In the SYNCH state the cell delineation will be assumed to be lost if an incorrect HEC is obtained ALPHA times consecutively.

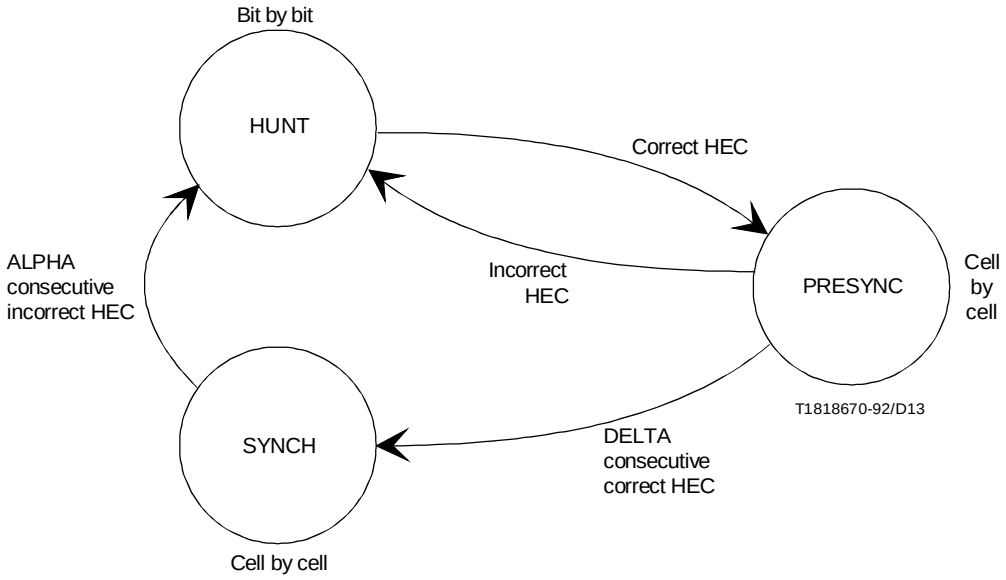


FIGURE 13/I.432

Cell delineation state diagram

The parameters ALPHA and DELTA are to be chosen to make the cell delineation process as robust and secure as possible while satisfying the performance specified in 4.5.2.

Robustness against false misalignments due to bit errors depends on ALPHA.

Robustness against false delineation in the resynchronization process depends on the value of DELTA.

For the SDH-based physical layer, values of ALPHA = 7 and DELTA = 6 are suggested.

For the cell-based physical layer, values of ALPHA = 7 and DELTA = 8 are suggested.

4.5.2 Cell delineation performance

This subclause is for further study. Figures B.1 and B.2 give provisional information on the performance of the cell delineation algorithm described in 4.5.1.1 in the presence of random bit errors, for various values of ALPHA and DELTA.

4.5.3 Scrambler operation

4.5.3.1 ATM cell level scrambler for the SDH-based Physical Layer

The following polynomial has been identified for the SDH-based physical layer.

Self synchronizing scrambler $x^{43} + 1$

This self synchronizing scrambler polynomial has been selected to minimize the error multiplication (two) introduced by the self synchronized scrambler (avoiding error multiplication in the header).

The operation of this scrambler in relation to the HEC cell delineation state diagram is as follows:

- the scrambler randomizes the bits of the information field only;
- during the five octet header the scrambler operation is suspended and the scrambler state retained;
- in the HUNT state the descrambler is disabled;
- in the PRESYNCH and SYNC states the descrambler is enabled for a number of bits equal to the length of the information field, and again disabled for the following assumed header.

4.5.3.2 Scrambler for the cell-based physical layer

The distributed sample scrambler is recommended for the cell based UNI.

4.5.3.2.1 Distributed sample scrambler (31st order)

The distributed sample scrambler is an example of a class of scrambler in which randomization of the transmitted data stream is achieved by modulo addition of a pseudo random sequence. Descrambling at the receiver is achieved by modulo addition of an identical locally generated pseudo random sequence having phase synchronization with the first in respect of the transmitted cells. The scrambler does not affect the performance of the 8 bit HEC mechanism during steady state operation.

Phase synchronization of a receiver PRBS with polynomial generator order r is achieved by sending r linearly independent source PRBS samples through the transmission channel as conveyed data samples. When received without error these r samples are sufficient to synchronize the phase of the PRBS generator at the receiver to that of the transmitter PRBS generator. A simple timing skew between the source PRBS samples and the conveyed PRBS samples serves as a means of decoupling the sample times of the source PRBS samples from the conveyed PRBS samples. This enables linear independence of PRBS samples to be simply achieved by taking samples at equal intervals of half an ATM cell from the source PRBS generator.

4.5.3.2.2 Transmitter operation

The transmitter pseudo random binary sequence is added (modulo-2) to the complete cell bit by bit excepting the HEC field. The pseudo random sequence polynomial is:

$$x^{31} + x^{28} + 1$$

The CRC octet for each cell is then modified by modulo-2 addition of the CRC calculated on the 32 bit of the scrambler sequence co-incident with the first 32 header bits. This is equivalent to calculation of the CRC on the first 32 bits of the scrambled header. The first two bits of the HEC field are then modified as follows by two bits from the PRBS generator. The two bits from the PRBS generator will be referred to as the PRBS source bits and the two bits of the CRC onto which they are mapped will be referred to as the PRBS transport bits.

To the first HEC bit (HEC_8) is added (modulo-2) the value of PRBS generator that was added (modulo-2) 211 bits earlier to the previous cell payload. To the second bit of the HEC field is added (modulo-2) the current value of the PRBS generator. These samples are exactly half a cell apart and the first ($U_{t\text{-}211}$) is delayed by 211 bits before conveyance (requiring one D-type latch for storage) (211 bits is 1 bit less than half a cell).

PRBS phase (as added to payload and all header except HEC)

U_{t-1}	U_t	U_{t+1}	U_{t+2}	U_{t+3}	U_{t+4}	U_{t+5}	U_{t+6}	U_{t+7}	U_{t+8}	U_{t+9}

Resultant transmitted data element

CLP + U_{t-1}	HEC_8 + U_{t-211}	HEC_7 + U_{t+1}	HEC_6	HEC_5	HEC_4	HEC_3	HEC_2	HEC_1	1st Pay-bit + U_{t+8}	2nd Pay-bit + U_{t+9}

4.5.3.2.3 Receiver operation

Three basic states of receiver operation are defined (see Figure 14):

I) Acquisition of scrambler synchronization (following cell delineation);

II) Verification of scrambler synchronization;

III) Steady state operation.

Receiver state I): Acquisition of scrambler synchronization (following cell delineation)

The principle of operation is as follows:

– *Cell delineation*

The cell delineation mechanism is independent from the scrambler synchronization acquisition mechanism. Cell delineation is determined using the last six bits of the HEC field (only). The first two bits have been modified by the modulo addition of the conveyed data samples and cannot therefore be used for delineation or CRC evaluation until the scrambler is synchronized.

– *Acquisition of scrambler synchronization*

The conveyed bits are extracted by modulo addition of the predicted values for HEC_8 and HEC_7 from the received values. Scrambler synchronization may for example be achieved by applying the conveyed samples at half cell intervals to a recursive descrambler (Figure C.1). In order to ensure the samples are added into the recursive descrambler at the same interval they were extracted from the source PRBS, the second sample U_{t+1} (derived from HEC_7) is stored for 211 bits before it is used.

Additionally, because both samples are applied to the recursive descrambler 211 bits behind their point of modulo addition to the transmitted data sequence, the recursive descrambler feedforward taps are chosen to generate a sequence that is advanced by 211 samples. Similarly, the verification comparison made in the recursive descrambler between the conveyed bits and their prediction is delay equalized using one bit stores as illustrated in Figure C.1.

– *Time to achieve scrambler synchronization*

Two bits of information are conveyed per cell which are linearly independent. The number of consecutive error free conveyed samples needed to synchronize the descrambler will be equal to the length of the scrambler, therefore 16 cells provides the 31 samples necessary to synchronize the scrambler.

The scrambler synchronization process is not disabled during cell delineation, however the descrambler will not begin to converge until the cell delineation mechanism has located the true position of the HEC sequence in the header and is no longer in its hunt state. Therefore the start of scrambler synchronization acquisition convergence will be coincident with the final transition from the hunt state to the presync state of the cell delineation mechanism.

Receiver state II): Verification of scrambler synchronization

The verification state differs from the acquisition state in that the recursive descrambler is no longer modified with synchronizing samples. Verification is needed because undetectable errors in the conveyed bits may have occurred during the acquisition phase. Verification tests the predicted PRBS in the receiver against the remote reference sequence given by the conveyed samples. To verify scrambler acquisition phase overall such that the probability of false synchronization is less than 10^{-6} requires 16 verifications where the transmission error ratio is better than 10^{-3}.

Receiver state III): Steady state operation (synchronized scrambler)

In this state the HEC_8 and HEC_7 bits can both be returned to normal use following their descrambling. Properties of error detection and correction are not affected by this process. Both cell delineation and scrambler synchronization are in this state reliably monitored by the existing cell delineation state machine.

HEC regeneration and header scrambling

The HEC bits in the transmitted cell were modified prior to transmission to correspond to the HEC for the scrambled header. To reverse this process where required and regenerate an HEC that corresponds to the unscrambled header, the HEC bits may be modified by modulo-2 addition of the CRC calculated on the 32 bits of the descrambler sequence coincident with the first 32 header bits.

Automatic scrambling detection

If scrambling is not used, then the conveyed PRBS samples derived from the corresponding HEC_7 and HEC_8 bits will have value zero. Thus these bits used to derive the phase of the descrambler will seed the descrambler with zeros inhibiting the PRBS of the descrambler automatically. Therefore, the absence of scrambling by the transmitter can be detected automatically by the receiver and correctly handled.

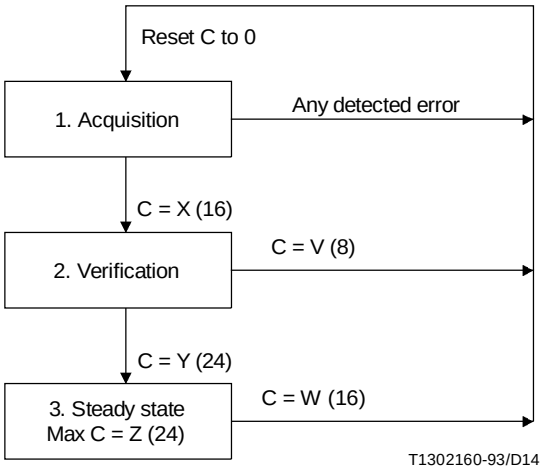


FIGURE 14/I.432

State transition diagram

4.5.3.2.4 State transition diagram and mechanism

The three states of the scrambler are Acquisition, Verification and Steady state.

The transition between these states may be determined by reference to the value of a single confidence counter (C) as follows:

Initial state = Acquisition, Confidence counter initial value = 0.

State 1: Acquisition: Confidence counter range 0 to X – 1

For every cell received correctly with no errors detected in HEC bits 1 to 6 the confidence counter is incremented by one and the two conveyed bits used to drive the recursive descrambler into synchronization.

Any error detected in the cell header results in a return to the initial state (the confidence counter being reset to zero).

Transition to the verification state occurs when the counter reaches X (Proposed value of X = 16).

State 2: Verification: Confidence counter range X to Y – 1

For every cell received without detected errors, the two conveyed bits are compared to their predicted values. For each cell with two correct predictions received, the confidence counter is incremented. If one or two incorrect predictions are made then the counter is decremented. If the counter falls below V (proposed value 8) the system returns to the acquisition initial state 1 and the confidence counter is reset.

Transition to the steady state occurs when the counter reaches Y (Proposed value of Y = 24).

State 3: Steady state: Confidence counter range Y to Z

The rules for incrementing and decrementing the confidence counter are as for state 2. The acquisition state is returned to automatically should the counter drop below W(= 16). The confidence counter has an upper limit of Z (proposed value 24).

4.6 Cell availability performance

For further study.

5 Power feeding

5.1 Provision of power

The provision of power to the B-NT1 via the user network interface is optional. When the power is provided, the following conditions should be considered.

A separate pair of wires shall be used for the provision of power to the B-NT1 via the T_B reference point.

The power sink shall be fed by either

- a source under the responsibility of the user when requested by the network provider;
- a power supply unit under the responsibility of the network provider connected to the mains electric supply in the customer premises.

The capability of the provision of power by the user side shall be available either

- as an integral part of the B-NT2/B-TE; and/or
- physically separated from the B-NT2/B-TE as an individual power supply unit.

A power source capable to feed more than one B-NT1 shall meet the requirements at each individual B-NT1 power feeding interface at the same point in time.

A short circuit or overload condition in any B-NT1 shall not affect the power feeding interface of the other B-NT1s.

5.2 Power available at B-NT1

The power available at the B-NT1 via the user-network interface shall be at least 15 watts.

5.3 Feeding voltage

The feeding voltage at the B-NT1 shall be in the range of –20 V to –57 V relative to ground.

5.4 Safety requirements

In principle, safety requirements are outside the scope of this Recommendation. However, in order to harmonize power source and sink requirements the following is required:

i) the power source shall be protected against short circuits and overload;

ii) the power sink of B-NT1 shall not be damaged by an interchange of wires.

With respect to the feeding interface of the power source, which is regarded as a touchable part in the sense of IEC Publication 950, the protection methods against electric shock specified in IEC Publication 950 may be applied.

6 Operational functions

The applicability of this paragraph to the cell based interface is for further study.

6.1 Definition of signals

The following signals related to maintenance are defined below:

Indication of LOS, LOF, LOP and LOC are generated within the functional equipment.

Path-AIS, multiplex section FERF and Path FERF are signals transmitted/received across the B-UNI (see Note 6, Table 3).

Loss of signal (LOS) – LOS is considered to have occurred when the amplitude of the relevant signal has dropped below prescribed limits for a prescribed period.

Loss of frame (LOF) – The interface detects a LOF when (TBD) or more consecutive errored framing patterns have been received.

Loss of pointer (LOP) – The interface detects a LOP when a valid pointer cannot be obtained using the pointer interpretation rules described in Recommendation G.783.

Loss of cell delineation (LOC) – The interface detects a LOC when ALPHA (7) (see 4.5.1.1) consecutive incorrect HEC have been detected.

MULTIPLEX-SECTION alarm indication signal (MS-AIS) – MS AIS is an STM-1 signal containing valid section overhead and a scrambled all-ones pattern for the remainder of the signal. On detecting LOS or LOF on the incoming signal, MS-AIS is generated by a regenerator within (TBD) μs. MS-AIS is detected as an all ones in bits 6, 7 and 8 of the K2 byte after descrambling.

PATH alarm indication signal (P-AIS) – P-AIS is sent to alert equipment in the direction of transmission that a failure has been detected. P-AIS is an all ones signal in H1, H2 and H3 octets, as well as in the entire payload. On detecting a failure or MS-AIS, P-AIS is generated within (TBD) μs.

MULTIPLEX-SECTION far end receive failure (MS-FERF) – MS-FERF alerts equipment in the opposite direction of transmission that a failure has been detected. On detecting LOS, LOF, or an MS-AIS on the incoming signal, MS-FERF is sent within (TBD) μs by inserting the code "110" in bit positions 6, 7 and 8 of the K2 byte.

PATH far end receive failure (P-FERF) – P-FERF alerts the associated path terminating equipment that a failure in the direction of transmission has been declared along the STM Path. If LOS, LOF, LOP, LOC, MS-AIS or P-AIS are detected, P-FERF is generated within (TBD) μs by setting bit 5 in the path status byte G1 to one.

6.2 Definitions of state tables at network and user sides

The user side and network side of the interface have to inform each other of the layer 1 states in relation to the different defects that could be detected.

For the purpose, two state tables are defined, one at the user side and one at the network side. States at the user side (F states) are defined in 6.2.1 and states at the network side (G states) are defined in 6.2.2. The state tables are defined in 6.2.4.

Fault conditions FC1 to FC4 that could occur at the network side or between the network side and user side are defined in Figure 15. These fault conditions directly affect the F and G states. Information on these fault conditions is exchanged between the user and network sides in the form of signals defined in 6.1.

NOTES

1 Only stable states needed for operation and maintenance of the user and the network side of the interface (system reactions, user and network relevant information) are defined. The transient states relative to the detections of the error information are not taken into account, except for power on/off transient states F7 and G13.

2 The user does not need to know where a failure is located in the network. The user must be informed on the availability and the continuity of the layer 1 service.

3 The user has all information relative to the performance associated with each direction of its adjacent section. The supervision of the quality of this section is the user's responsibility.

6.2.1 Layer 1 states on the user side of the interface

F0 state: Loss of power on the user side

– In general, the TE can neither transmit nor receive signals.

F1 state: Operational state

– Network timing and layer 1 service is available.

– The user side transmits and receives operational frames.

F2 state: Fault condition No. 1

– This fault state corresponds to the fault condition FC1.

– Network timing is available at the user side.

– The user side transmits operational frames.

– The user side receives frames containing P FERF indication.

F3 states: Fault condition No. 2

– This fault state corresponds to any combination of FC2 with FC1, FC3 and FC4.

– Network timing may not be available at the user side.

– The user side detects LOS, LOF, LOP, LOC.

– The user side transmits frames with associated MS-FERF and P-FERF.

F4 state

– This fault state corresponds to fault condition FC3 or FC1 and FC3.

– Network timing may not be available at the user side.

– The user side detects P-AIS, LOP or LOC.

– The user side transmits frames containing P-FERF indication.

F5 state: Fault condition No. 4

– This fault state corresponds to the fault condition FC4 or FC1 and FC4.

– Network timing is available at the user side.

– The user side transmits operational frames.

– The user side receives frames containing MS-FERF and P-FERF indications.

F6 state

– This fault corresponds to fault condition FC3 + FC4 or FC3 + FC4 + FC1.

– Network timing may not be available at the user side.

– The user side receives frames containing MS-FERF and P-AIS.

– The user side transmits frames containing P-FERF.

F7 state: Power on state

– This is a transient state and the user side may change the state after detection of the signal received.

6.2.2 Layer 1 states at the network side of the interface

G0 state: Loss of power on the network side

– In general, the B-NT1 can neither transmit nor receive any signal.

G1 state: Operational state

– The network timing and layer 1 service is available.

– The network side transmits and receives operational frames.

G2 state: Fault condition No. 1

– This fault state corresponds to the fault condition FC1.

– Network timing is provided to the user side.

– The path terminating equipment within the access network detects LOS, LOF, LOP, LOC or P-AIS or MS-AIS.

– The network side transmits frames containing P-FERF indication.

G3 state: Fault condition No. 2

– This fault state corresponds to the fault condition FC2.

– Network timing is not available to the user side.

– The network side transmits operational frames.

– The network side receives frames containing MS-FERF and P-FERF indications.

G4 state: Fault condition No. 3

– This fault state corresponds to the fault condition FC3.

– Network timing is not provided to the user side.

– The B-NT1 detects LOS/LOF or MS-AIS from the access network.

– The network side transmits P-AIS.

– The network side receives frames containing P-FERF.

G5 state

– This fault state corresponds to the fault condition FC4 or FC2 and FC4.

– the network side transmits frames containing MS-FERF and P-FERF indication to the user side.

G6 state

– This fault state corresponds to fault conditions FC1 and FC2.

– Network timing is not available at the user side.

– The network side transmits frames containing P-FERF indication.

– The B-NT1 receives MS-FERF and P-FERF indications from the user side and the PATH terminating equipment detects LOS, LOF, LOP, LOC or P-AIS or MS-AIS.

G7 state

– This fault state corresponds to fault conditions FC1 and FC3.

– Network timing is not available at the user side.

– The network side transmits frames containing P-AIS indication.

– The network side receives frames containing P-FERF.

G8 state

– This fault state corresponds to fault conditions FC1 and FC4 or FC1 and FC2 and FC4.

– The network side transmits frames containing MS-FERF and P-FERF indications to the user side.

G9 state

– This fault state corresponds to fault conditions FC2 and FC3.

– Network timing is not available at the user side.

– The network side transmits frames containing P-AIS.

– The network side receives frames containing MS-FERF and P-FERF indications.

G10 state

– This fault state corresponds to fault conditions FC3 and FC4 or FC2 and FC3 and FC4.

– The network side transmits frames containing P-AIS and MS-FERF indication to the user side.

– Network timing is not provided to the user side.

G11 state

– This fault state corresponds to fault conditions FC1 and FC2 and FC3.

– Network timing is not available at the user side.

– The network side transmits P-AIS to the user side.

– The network side receives frames containing MS-FERF.

G12 state

– This fault state corresponds to fault conditions FC1 and FC3 and FC4 or FC1 and FC2 and FC3 and FC4.

– Network timing is not available at the user side.

– The network side transmits frames containing P-AIS and MS-FERF to the user side.

G13 state: Power on state

– This is a transient state and the network side may change the state after detection of the signal received.

6.2.3 Definition of primitives

The following primitives should be used between the physical media dependent layer and the management entity (management physical header (MPH) primitives):

MPH-AI	MPH-ACTIVATE INDICATION (is used as error recovery and initialization information)
MPH-DI	MPH Deactivate Indication
MPH-EIn	MPH ERROR INDICATION with parameter n (n defines the failure condition relevant to the reported error)
MPH-CIn	MPH Correction Indication with parameter n (n defines the failure condition relevant to the reported recovery).

6.2.4 State tables

Operational functions are defined in Table 5 for the layer 1 states at the user side of the interface and in Table 6 for the network side.

TABLE 5/I.432

F-state table: Physical layer 1 state matrix at the user side (Note 1)

	Initial state →	F0	F1	F2	F3	F4	F5	F6	F7
Definition of the states	Operational condition or fault condition	Power off at user side	Operational	FC1	FC2 fault conditions (Note 4)	FC3 or FC3 + FC1	FC4 or FC4 + FC1	FC3 + FC4 or FC3 + FC4 + FC1	Power on at user side
	Signal transmitted by user towards interface	No signal	Normal operational frames	Normal operational frames	Frames with MS-FERF and P-FERF	Frames with P-FERF	Normal operational frames	Frames with P-FERF	No signal
New event detected at receiving side	Loss of power at user side	/	PH-DI MPH-EI0 F0	MPH-EI0 F0	MPH-EI0 F0	MPH-EI0 F0	MPH-EI0 F0	MPH-EI0 F0	MPH-EI0 F0
	Return of power to user side	F7	/	/	/	/	/	/	/
	Normal operational frames from network side	/	–	PH-AI MPH-AI F1	PH-AI MPH-AI F1	PH-AI MPH-AI F1	PH-AI MPH-AI F1	PH-AI MPH-AI F1	PH-AI MPH-AI F1
	P-FERF (FC1)	/	PH-DI MPH-EI1 F2	–	n.d.p.	–	–	–	MPH-EI1 F2
	LOS or LOF (FC2) (Note 2)	/	PH-DI MPH-EI2 F3	MPH-EI2 F3	–	MPH-EI2 F3	MPH-EI2 F3	MPH-EI2 F3	MPH-EI2 F3
	LOC or LOP or P-AIS (FC3) or (FC1 + FC3) (Note 3)	/	PH-DI MPH-EI3 F4	MPH-EI3 F4	n.d.p.	–	MPH-EI3 F6	–	MPH-EI3 F4
	P-FERF and MS-FERF (FC4)	/	PH-DI MPH-EI4 F5	MPH-EI4 F5	n.d.p.	MPH-EI4 F6	–	–	MPH-EI4 F5
	P-AIS and MS-FERF or LOC, MS-FERF and P-FERF or LOP, MS-FERF (FC3 + FC4)	/	PH-DI MPH-EI3 MPH-EI4 F6	MPH-EI3 MPH-EI4 F6	n.d.p.	MPH-EI4 F6	MPH-EI3 F6	–	MPH-EI3 MPH-EI4 F6

NOTES

1 If the path trace is used, the path trace mismatch will be a path related failure as LOP or LOC. In this table “LOC” will be substituted by “LOC or path trace mismatch”.

2 When FC2 occurs, other fault conditions (FC1 or FC3 or FC4) can not be detected but they may occur simultaneously.

3 When FC3 occurs, FC1 (P-FERF) can not be detected but it may occur simultaneously.

4 The user side cannot distinguish among FC2, FC2+FC1, FC2+FC3, FC2+FC4, FC2+FC1+FC3, FC2+FC1+FC4, FC2+FC3+FC4 or FC2+FC1+FC3+FC4.

TABLE 6/I.432

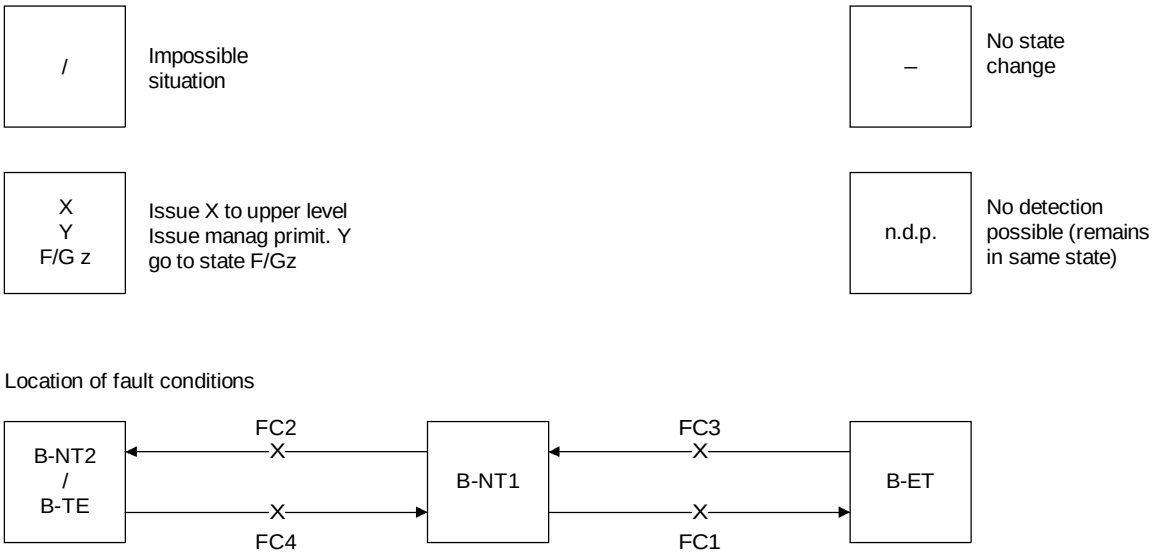
G-state table: Physical layer 1 state matrix at the network side

		Initial state →	G0	G1	G2	G3	G4	G5	G6	G7	G8	G9	G10	G11	G12	G13
Definition of the states		Operation condition or failure condition	Power off at NT1	Operational	FC1	FC2	FC3	FC4 or FC2 & FC4	FC1 & FC2	FC1 & FC3	FC1 & FC4 or FC1 & FC2 & FC4	FC2 & FC3	FC3 & FC4 or FC2 & FC3 & FC4	FC1 & FC2 & FC3	FC1 & FC3 & FC4 or FC1 & FC2 & FC3 & FC4	Power on at NT1
		Signal transmitted towards interface	No signal	Normal operational signal	Signal with P-FERF	Normal operational signal	Signal with P-AIS	Signal with MS&P-FERF	Signal with P-FERF	Signal with P-AIS	Signal with MS&P-FERF	Signal with P-AIS	Signal with P-AIS and MS-FERF	Signal with P-AIS	Signal with P-AIS and MS-FERF	No signal
New detected event		Loss of power or power down mode at NT1	–	PH-DI MPH-EI0 G0	MPH-EI0 G0	MPH-EI0 G0	MPH-EI0 G0	MPH-EI0 G0	MPH-EI0 G0	MPH-EI0 G0	MPH-EI0 G0	MPH-EI0 G0	MPH-EI0 G0	MPH-EI0 G0	MPH-EI0 G0	MPH-EI0 G0
		Return of power at NT1	MPH-CI0 G13	/	/	/	/	/	/	/	/	/	/	/	/	/
		Normal operational trames	/	–	PH-AI MPH-AI G1	PH-AI MPH-AI G1	PH-AI MPH-AI G1	PH-AI MPH-AI G1	PH-AI MPH-AI G1	PH-AI MPH-AI G1	PH-AI MPH-AI G1	PH-AI MPH-AI G1	PH-AI MPH-AI G1	PH-AI MPH-AI G1	PH-AI MPH-AI G1	PH-AI MPH-AI G1
	New appearing event	Internal network failure FC1	/	PH-DI MPH-EI1 G2	–	MPH-EI1 G6	MPH-EI1 G7	MPH-EI1 G8	–	–	–	MPH-EI1 G11	MPH-EI1 G12	–	–	MPH-EI1 G2
		Reception of MS & P-FERF (FC2)	/	PH-DI MPH-EI2 G3	MPH-EI2 G8	–	MPH-EI2 G9	n.d.p.	–	MPH-EI2 G11	n.d.p.	–	n.d.p.	–	n.d.p.	MPH-EI2 G3
		Internal network failure (FC3) (Note)	/	PH-DI MPH-EI3 G4	MPH-EI3 G7	MPH-EI9 G9	–	MPH-EI3 G10	MPH-EI3 G11	–	MPH-EI3 G12	–	–	–	–	MPH-EI3 G4
		LOS or LOF (FC4)	/	PH-DI MPH-EI4 G5	MPH-EI4 G8	MPH-EI4 G5	MPH-EI4 G10	–	MPH-EI4 G8	MPH-EI4 G12	–	MPH-EI4 G10	–	MPH-EI4 G12	–	MPH-EI4 G5
	Dis-appearing FC	FC1	/	/	MPH-CI1 G1	/	/	/	MPH-CI1 G3	MPH-CI1 G4	MPH-CI1 G5	/	/	MPH-CI1 G9	MPH-CI1 G10	/
		FC2	/	/	/	MPH-CI2 G1	/	–	MPH-CI2 G2	/	–	MPH-CI2 G4	–	MPH-CI2 G7	–	/
		FC3	/	/	/	/	MPH-CI3 G1	/	/	MPH-CI3 G2	/	MPH-CI3 G3	MPH-CI3 G5	MPH-CI3 G6	MPH-CI3 G8	/
		FC4	/	/	/	/	/	MPH-CI4 G3	/	/	MPH-CI4 G6	/	MPH-CI4 G9	/	MPH-CI4 G11	/

NOTE – If FC3 represents a path related fault condition (e.g. LOC), the consequent reaction is not applicable for the G-state table, because this failure can not be recognized at the network side. Therefore no state change will occur.

6.2.4.1 General information for the state table matrix consideration

Explanations of the symbols used in Tables 5 and 6 are given in Figure 15.:



Fault condition	Definition
FC4	Fault in the upstream direction of the interface
FC2	Fault in the downstream direction of the interface
FC3	Fault in the downstream direction in access digital section
FC1	Fault in the upstream direction in access digital section

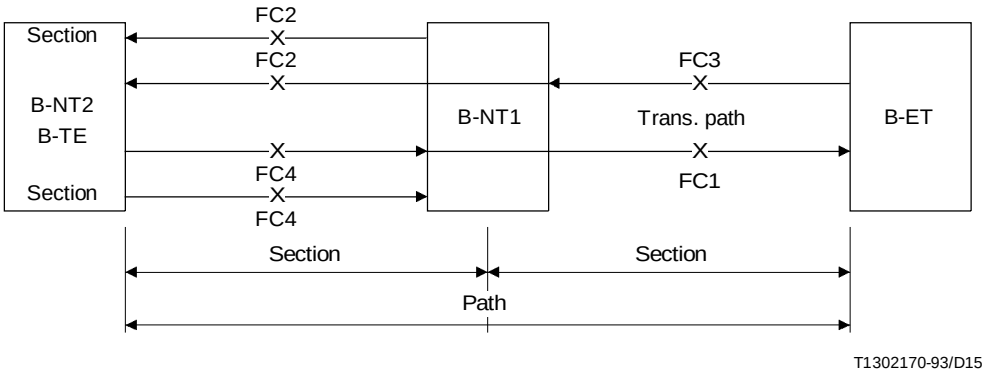


FIGURE 15/I.432

Fault conditions and operational span of section path maintenance signals

Annex A

Impact of random bit errors on HEC performance

(This annex forms an integral part of this Recommendation)

A.1 Figure A.1 gives an example of discarded cell probability and probability of valid cells with errored headers as a function of random bit error probability.

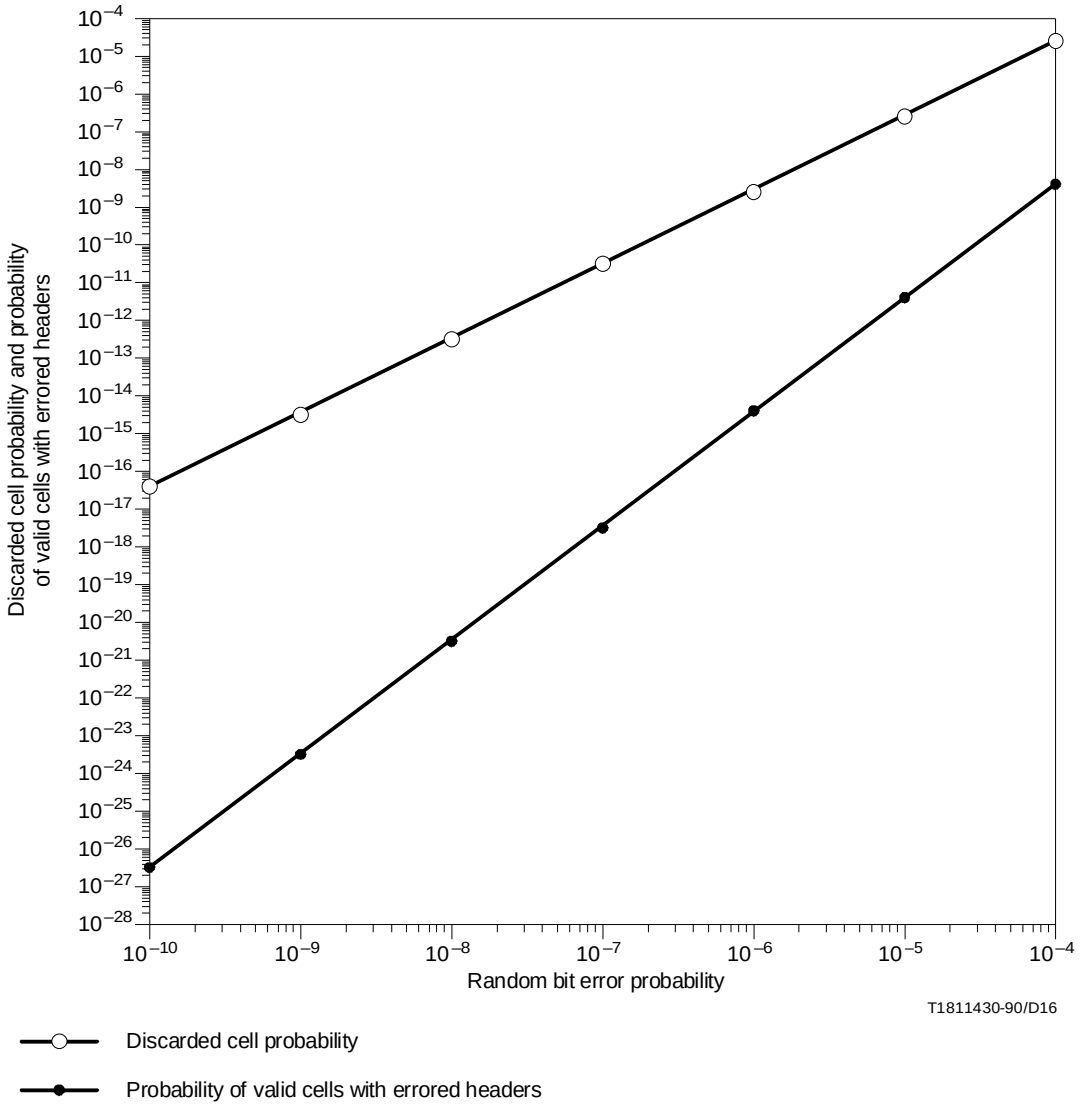


FIGURE A.1/I.432

Annex B

Impact of random bit errors on cell delineation performance

(This annex forms an integral part of this Recommendation)

B.1 Figures B.1 and B.2 show In-Sync time and acquisition time as a function of bit error probability.

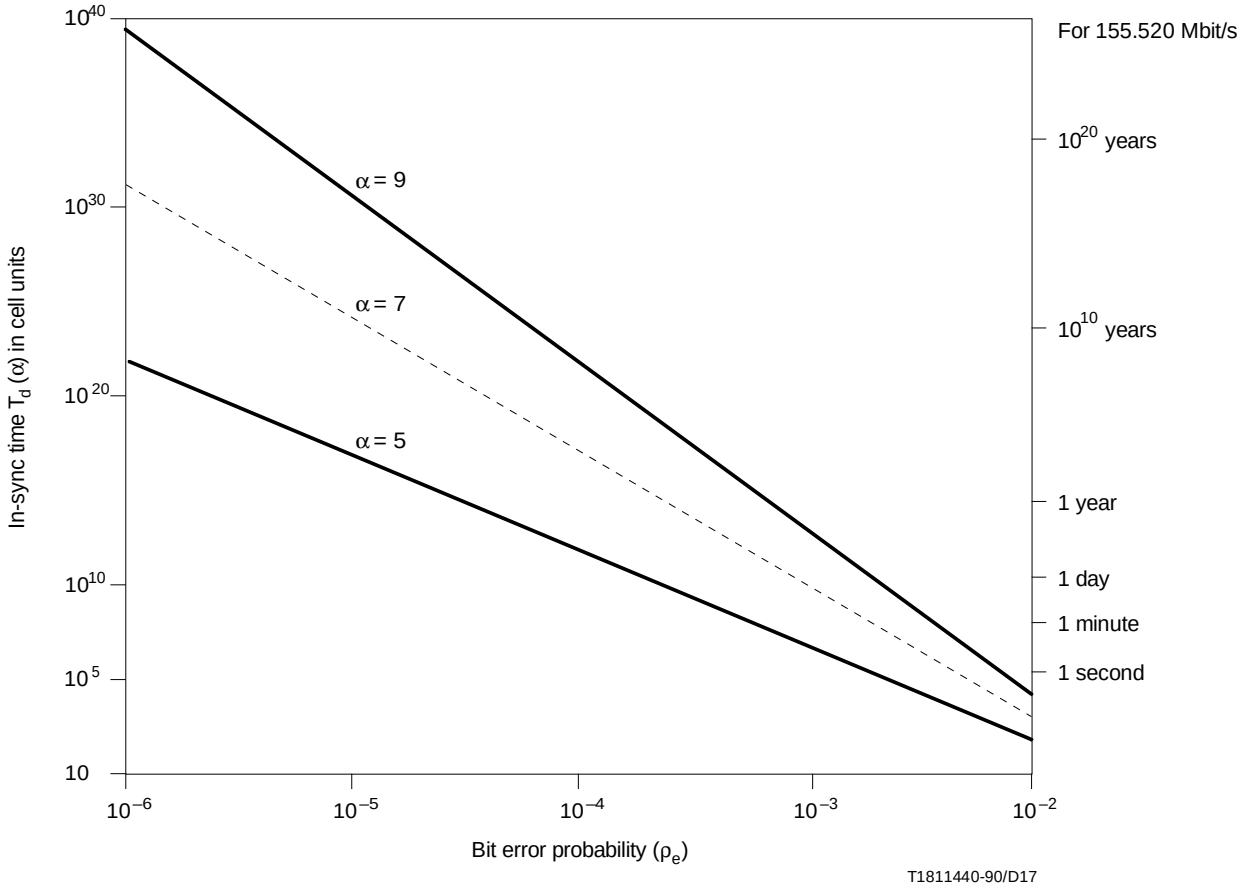


FIGURE B.1/I.432

In-sync time versus bit error probability
[T_d (α) vs. ρ_e]

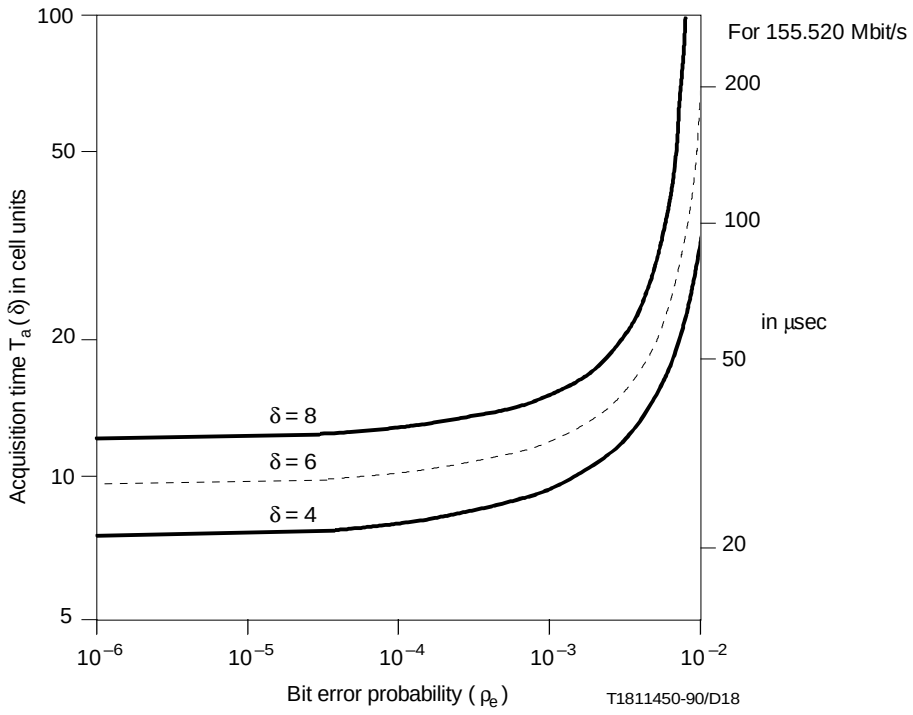


FIGURE B.2/I.432

Acquisition time versus bit error probability
[T_a (δ) vs. ρ_e]

Annex C

Distributed sample scrambler descrambler implementation example

(This annex forms an integral part of this Recommendation)

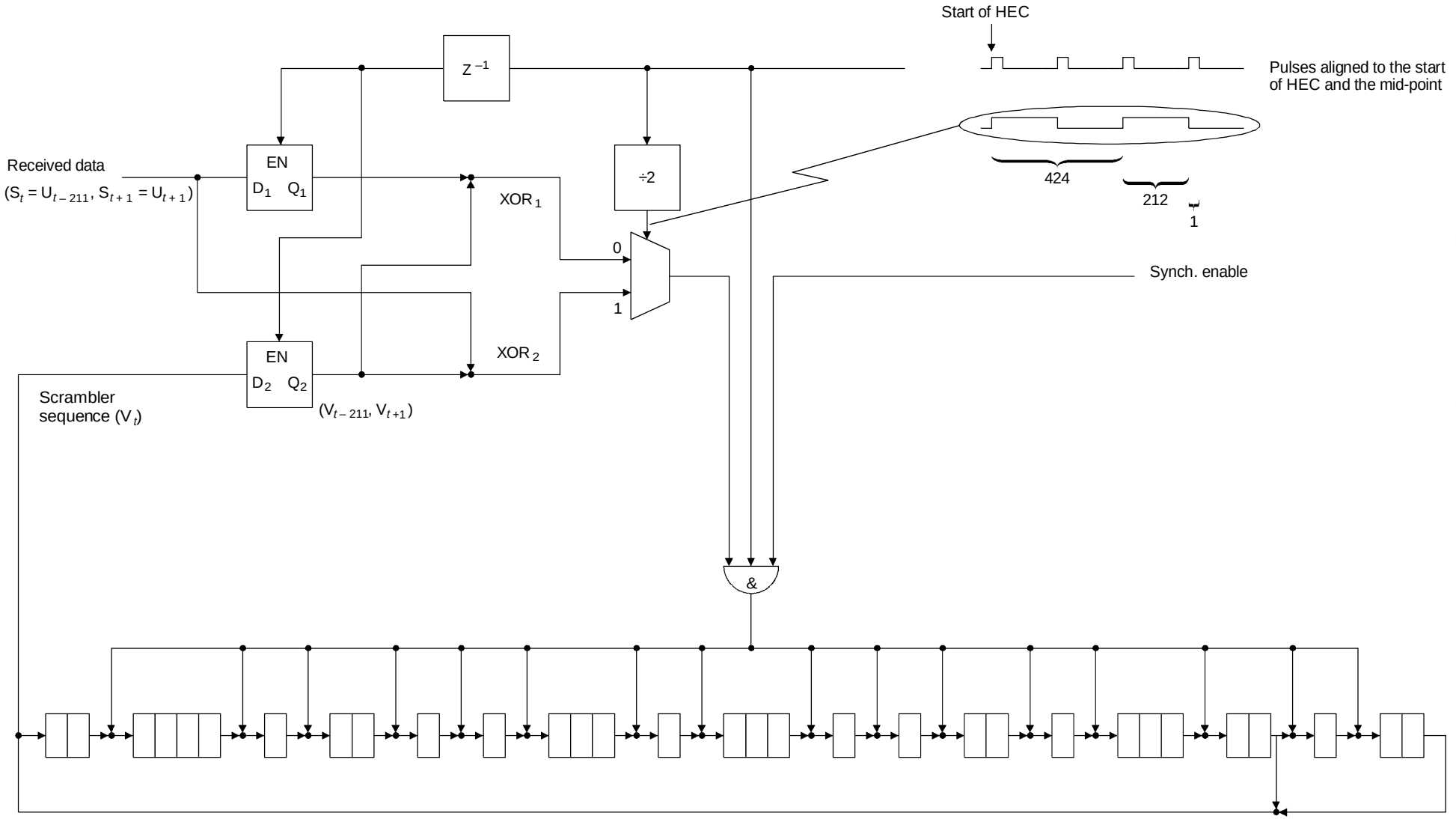
C.1 Acquisition of scrambler synchronization

The conveyed bits are extracted by modulo addition of the predicted values for HEC_8 and HEC_7 from the received values. Scrambler synchronization may for example be achieved by applying the conveyed samples at half cell intervals to a recursive descrambler (Figure C.1). In order to ensure the samples are added into the recursive descrambler at the same interval they were extracted from the source PRBS, the second sample $U_{(t+1)}$ (derived from HEC_7) is stored for 211 bits before it is used.

Additionally, because both samples are applied to the recursive descrambler 211 bits behind their point of modulo addition to the transmitted data sequence, the recursive descrambler feedforward taps are chosen to generate a sequence that is advanced by 211 samples. Similarly, the verification comparison made in the recursive descrambler between the conveyed bits and their prediction is delay equalized using one bit stores as illustrated in Figure C.1.

Example: Implementation – The recursive descrambler.

Figure C.1 illustrates the recursive descrambler implementation. Notation of sample values indicates the important sample values in each cell, time being referenced to the conveyed PRBS sample being received with HEC_8.



NOTE – All D-types clocked at the data bit rate.

FIGURE C.1/I.432

$X^{31} + X^{28} + 1$ Polynomial recursive descrambler

At time *t*:

– the receiver PRBS generator sample V_t is at the input to the lower D-type D_2;

– the source PRBS sample $S_t = U_{t–211}$ conveyed via HEC_8 is at input D_1;

– the sample previously stored at the output of the lower D-type is $D_2 = V_{t–211}$

$$EXOR_2 = S_t + D_2 = U_{t–211} + V_{t–211}$$

The multiplexer selects this output and it is applied to the feedforward taps of the recursive descrambler.

At time $t + 1$:

– the receiver sample V_{t+1} is at the input to D_2;

– the sample $S_{t+1} = U_{t+1}$ is at the input to D_1.

These values are latched on the following clock edge such that:

At time $t + 2$ through until $t + 212$:

– $EXOR_1 = V_{t+1} + U_{t+1}$ which is applied via MUX at time $t + 212$ to the feedforward taps.

At time $t + 213 = L + t – 211$ (L being the duration of a cell):

– $D_2 = V_{t+213} = V_{t–211 + L}$ (held until the next cell cycle).