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Amendment 1
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SERIES G: TRANSMISSION SYSTEMS AND MEDIA, DIGITAL SYSTEMS AND NETWORKS

Digital networks – Quality and availability targets

The control of jitter and wander within the optical transport network (OTN)

Amendment 1

ITU-T Recommendation G.8251 (2001) – Amendment 1

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ITU-T Recommendation G.8251

The control of jitter and wander within the optical transport network (OTN)

Amendment 1

Summary

This amendment contains extensions to the first version of ITU-T Rec. G.8251 (11/2001) related to the addition of ODUk multiplexing.

Source

Amendment 1 to ITU-T Recommendation G.8251 was prepared by ITU-T Study Group 15 (2001-2004) and approved under the WTSA Resolution 1 procedure on 13 June 2002.

FOREWORD

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NOTE

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ITU-T Recommendation G.8251

The control of jitter and wander within the optical transport newtork (OTN)

Amendment 1

1) Introduction

This amendment contains extensions to the first version (2001) of ITU-T Rec. G.8251, related to the addition of ODUk multiplexing.

2) Additions

2.1) Clause 1 (Scope)

Replace paragraph 3 with the following, to reflect the fact that G.8251 now has requirements for cases involving ODUk multiplexing:

The network limits given in clause 5, OTN interface tolerance specifications given in 6.1, and OTN equipment interface specifications given in Annex A apply at or refer to the OTUk interface. The relevant bit rates for these specifications are the OTUk bit rates. Note that some of the other requirements in this Recommendation, e.g. the demapper clock (ODCp), asynchronous mapper clock (ODCa), and bit-synchronous mapper clock (ODCb) requirements in Annex A, apply to other interfaces and other bit rates (i.e. the demapper resides in the sink adaptation function between the ODUkP and CBR and ODUj[/i] client, while the asynchronous and bit-synchronous mapper clocks reside in the source adaptation function between the ODUkP and client). In this Recommendation the term *clock*, when used in ODU clock (ODC), refers to a frequency source. Note that ITU-T Rec. G.8251 contains requirements for both non-OTN CBRx clients mapped into ODUk and ODUj[/i] clients multiplexed into ODUk (k > j).

2.2) Annex A – Clause A.1 (Scope)

a) Replace paragraph 1 with the following, to reflect the fact that the ODCa and ODCp clocks now also can be used for ODUk multiplexing and demultiplexing:

This annex contains the requirements for the ODUk Clock (ODC). Here, the term *clock* refers to a clock filtering and/or generating circuit. Four ODC types are defined, for different applications (see A.2):

1) ODCa for asynchronous mapping of constant bit rate (CBR) clients (e.g. generic CBRx client, RS client, etc.) and variable bit rate (VBR) clients (e.g. VP client, GFP client, etc.) into ODUk, asynchronous multiplexing of ODUj[/i] clients into ODUk (k > j), generation of Test/NULL signals and for AIS and OCI generation;
2) ODCb for bit-synchronous mapping of CBRx clients into ODUk;
3) ODCr for 3R regeneration of the ODUk signal; and
4) ODCp for demapping of constant bit rate (CBR) clients and demultiplexing of ODUj[/i] clients from ODUk (k > j).

The ODCa and ODCb generate the timing signal for the ODUk and OTUk signals produced by an OTN network element. The ODCr generates the timing signal for the OTUk produced by a 3R regenerator. The ODCp generates the timing signal for a demapped CBRx client signal or demultiplexed ODUj[/i] signal.

b) *Replace Table A.1 with the following, to:*

1) *add the atomic functions for ODUk multiplexing and demultiplexing;*

2) *make clear that the ODCp is now used for both demapping of non-OTN CBRx clients and multiplexed ODUks:*

Table A.1/G.8251 – Summary of ODUk Clock (ODC) types

	ODCa	ODCb	ODCr	ODCp
Atomic function	ODUkP/CBRx-a_A_So ODUkP/GFP_A_So ODUkP/NULL_A_So ODUkP/PRBS_A_So ODUkP/RSn-a_A_So ODUkP/VP_A_So ODUkP/ODU[i]j_A_So ODUkP/ODUi[j]_A_Sk (AIS clock) OTUk/ODUk_A_Sk (AIS clock) OTUkV/ODUk_A_Sk (AIS clock) ODUk_C (OCI clock)	ODUkP/CBRx-b_A_So ODUkP/RSn-b_A_So	OTUk/ODUk_A_So and OTUk/ODUk_A_Sk (i.e. the clocks of these atomic functions are concentrated in a single ODCr; see ITU-T Rec. G.798)	ODUkP/CBRx_A_Sk ODUkP/ODU[i]j_A_Sk
Frequency accuracy	±20 ppm	±20 ppm	±20 ppm	±20 ppm
Free-run mode supported	Yes	Yes	Yes	Yes
Locked mode supported	No	Yes	Yes	Yes
Holdover mode supported	No	No	No	No
Pull-in range	NA	±20 ppm	±20 ppm	±20 ppm
Pull-out range	NA	±20 ppm	±20 ppm	±20 ppm
Jitter generation	Table A.2/G.8251	Table A.2/G.8251	Table A.2/G.8251	Table A.3/G.8251
Wander generation	NA	NA (Note 1)	NA	NA (Note 2)
Jitter tolerance	NA	ITU-T Rec. G.825	Table 2/G.8251, Figure 1/G.8251 (OTU1) Table 3/G.8251, Figure 2/G.8251 (OTU2) Table 4/G.8251, Figure 3/G.8251 (OTU3)	Table 2/G.8251, Figure 1/G.8251 (OTU1) Table 3/G.8251, Figure 2/G.8251 (OTU2) Table 4/G.8251, Figure 3/G.8251 (OTU3)

Table A.1/G.8251 – Summary of ODUk Clock (ODC) types

	ODCa	ODCb	ODCr	ODCp
Wander tolerance	NA	ITU-T Rec. G.825	Clause 6.1/G.8251	Clause 6.1/G.8251
Jitter transfer	NA	Maximum Bandwidth: ODU1: 1 kHz ODU2: 4 kHz ODU3: 16 kHz Maximum Gain Peaking: 0.1 dB for ODU1, 2, and 3 (see Table A.4/G.8251 and Figure A.1/G.8251)	Maximum Bandwidth: OTU1: 250 kHz OTU2: 1000 kHz OTU3: 4000 kHz Maximum Gain Peaking: 0.1 dB for OTU1, 2, and 3 (see Table A.5/G.8251 and Figure A.1/G.8251)	Maximum Bandwidth: 300 Hz Maximum Gain Peaking: 0.1 dB (see A.7.3/G.8251)
Output when input signal is lost	AIS (CBRx client) OTUk: no frame hit OTUk frequency unchanged	AIS (CBRx client) OTUk: no frame hit OTUk initial frequency change ≤ 9 ppm	AIS (OTUk) OTUk: frame hit allowed Temporary OTUk frequency offset > 20 ppm allowed	AIS (CBRx client), AIS (ODUj[/i] client) Frequency offset ≤ 20 ppm

NA No requirement because not applicable

NOTE 1 – The wander generation of ODCb is expected to be negligible compared to the wander on the input CBR (e.g. SDH) client signal, because the ODCb bandwidth is relatively wide band.

NOTE 2 – The intrinsic wander generation of the ODCp is negligible compared to the wander generated by the demapping process.

c) Replace the Note at the end of clause A.1 with the following, to reflect the fact that ODUk multiplexing may now occur:

NOTE – In the case of asynchronous mapping or multiplexing, there is no requirement for a single master clock, i.e. single ODCa, in OTN equipment. Within OTN equipment there may be multiple, independent ODCa clocks for each outgoing wavelength (i.e. for the source of each OCh, OTUk, and ODUk). In the case of bit-synchronous mapping, 3R regeneration, and demapping there cannot be a single master clock for multiple OCh's, i.e. an ODCb, ODCr, or ODCp supplies timing for a single ODUk, OTUk, or CBR client, respectively.

2.3) Clause A.2 (Applications)

a) Replace paragraphs 1 and 2 with the following, to reflect the fact that the ODCa and ODCp clocks now also can be used for ODUk multiplexing and demultiplexing, respectively:

The ODCa and ODCb are used for the mapping of payload to the ODUk signal; the ODCr is used for the 3R regeneration; the ODCp is used in the CBR demapper and ODU[i]j demultiplexer.

The ODCa, used for asynchronous mapping and ODU[i]j multiplexing, is free running and the bit rate offset is accommodated by appropriately controlled stuffing. The ODCa is also the AIS and OCI clock.

b) Replace paragraph 5 with the following, to reflect the fact that the ODCp clock now also can be used for ODUk demultiplexing:

The ODCp, used for the CBR demapper and the ODU[i]j demultiplexer, is locked to the bit rate of the gapped OPUk clock (i.e. the timing of the signal that results from taking the OPUk payload and applying the justification control). If the incoming signal fails, the ODCp enters a free-run condition.

2.4) Subclause A.5.1.2 (ODCp jitter generation)

a) Replace paragraph 1 with the following, to reflect the fact that the ODCp clock now also can be used for ODUk demultiplexing:

In the absence of input jitter, jitter of the ODCp output, i.e. the CBR/RS_CI_CK signal or the ODUj[/i]_CI_Ck signal, shall not exceed the values specified in Table A.3/G.8251 when measured over a 60-second interval with the measurement filters specified in that table. Note that the output is at the CBRx/RSn_CP interface or the ODUj[/i]_CP interface. The requirements shall be met when the input frequency of the CBRx or ODUj[/i] client is constant within the limits –20 ppm to +20 ppm from the nominal frequency.

NOTE – The CBR_CP and ODUk[/i]_CP are internal to a network element, and are therefore generally not accessible to testing. Compliance with the requirement may be verified by varying the frequency of the client input at the OS_CP or OCh_CP within the limits –20 ppm to +20 ppm from nominal frequency and verifying that, for jitter-free input, the jitter on the demapped client output of the ODCp is within the limits specified in Table A.3/G.8251.

b) Replace Table A.3/G.8251 with the following, to reflect that:

1) *the requirements for demultiplexing ODU1 from ODU2 or ODU3 are the same as those for demapping CBR2G5 from ODU1; and*
2) *the requirements for demultiplexing ODU2 from ODU3 are the same as those for demapping CBR10G from ODU2:*

Table A.3/G.8251 – ODCp jitter generation requirements

Interface	Measurement bandwidth, –3 dB frequencies (Hz)	Peak-to-peak amplitude (UIpp) (Note 2)
CBR2G5 ODU1	5 k to 20 M	1.0
	1 M to 20 M	0.1
CBR10G ODU2	20 k to 80 M	1.0
	4 M to 80 M	0.1
CBR40G	80 k to 320 M (Note 1)	1.0
	16 M to 320 M	0.1

NOTE 1 – Values for STM-256 are provisional and are not present in G.825 at the time of publication of G.8251.

NOTE 2 – CBR2G5 $1\ UI = \frac{1}{2.48832}$ [ns] = 401.9 ps

CBR10G $1\ UI = \frac{1}{9.95328}$ [ns] = 100.5 ps

CBR40G $1\ UI = \frac{1}{39.81312}$ [ns] = 25.12 ps

ODU1 $1\ UI = \frac{238}{(239)(2.48832)}$ [ns] = 400.2 ps

ODU2 $1\ UI = \frac{237}{(239)(9.95328)}$ [ns] = 99.63 ps

2.5) Subclause A.7.3 (Jitter transfer for ODCp)

Replace paragraph 1 with the following, to reflect the fact that the ODCp clock now also can be used for ODUk demultiplexing:

The jitter transfer requirements for ODCp are, essentially, the transfer requirements for a CBR (e.g. SDH) demapper (i.e. a desynchronizer) or ODU[i]j demultiplexer. The demapper function, including the ODCp, is contained in the ODUkP/CBRx_A_Sk and ODUkP/RSn_A_Sk atomic function. The demultiplexer functions, including the ODCp, is contained in the ODUkP/ODU[i]j_A_Sk atomic function. The ODCp performs filtering, which is necessary to control the mapping/demapping jitter and wander accumulation over multiple OTN islands.

2.6) Appendix VI (OTN atomic functions)

Replace Figure VI.1/G.8251 by the figure below, to include the new atomic functions needed for ODUk multiplexing, and also to include all atomic functions in Table A.1/G.8251 in a simplified manner. Replace the atomic function descriptions in G.8251 with the descriptions below, which include the new atomic functions for ODUk multiplexing and are also consistent with the simplified figure.

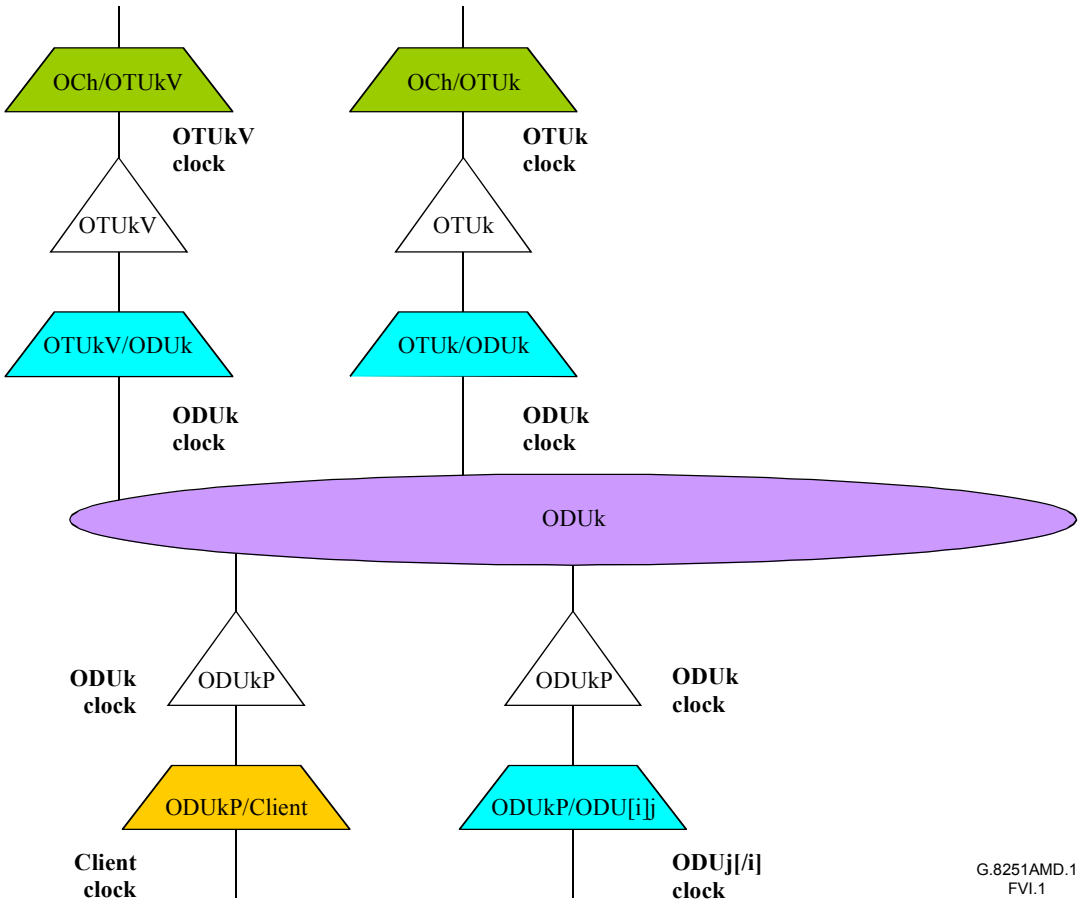

Figure VI.1/G.8251 – Atomic functions used for OTN timing

OCh/OTUk_A_Sk: Clock recovery for the OTUk clock.

OTUk/ODUk_A_Sk: Generates ODUk clock from OTUk clock (239:255 ratio). In the case of OTUk defects including signal fail, AIS is generated with an AIS clock. The ODUk clock has to be within the limits even in case of a loss of signal.

OTUk/ODUk_A_So: Generates OTUk clock from ODUk clock (255:239 ratio). As the ODUk signal is always available no AIS clock is required. A switch between several ODUk signals with different clock phases and different frequencies shall not harm the OTUk clock.

OCh/OTUkV_A_Sk: Clock recovery for the OTUkV clock.

OTUkV/ODUk_A_Sk: Generates ODUk clock, either from the OTUkV clock with a fixed ratio (synchronous mapping) or based on the OTUkV clock and stuffing (asynchronous mapping)

OTUkV/ODUk_A_So: Generates OTUkV clock, either from the ODUk clock with a fixed ratio (synchronous mapping) or free running (asynchronous mapping) with stuffing of the ODUk into the OTUk.

ODUkP/Client_A_So: Generates ODUk clock, either free-running (asynchronous mapping) with stuffing of the client signal into the ODUk if necessary or from the client clock with a fixed ratio (synchronous mapping).

ODUkP/Client_A_Sk: Generates client clock based on the ODUk clock, and stuffing decisions if applicable.

ODUk_C: Generates free running ODUk clock for OCI.

ODUkP/ODU[i]j_A_So: Generates free-running ODUk clock. Stuffing of ODUj[/I] into ODUk.

ODUkP/ODU[i]j_A_Sk: Generates ODUj[/I] clock based on ODUk clock and stuffing decision. AIS clock on incoming signal fail.

2.7) New Appendices VII and VIII

Add new Appendix VII, which documents the two Hypothetical Reference Models (HRMs) used for the payload jitter and short-term wander (TDEV) accumulation studies for ODUk multiplexing cases. Add new Appendix VIII, which documents the jitter and short-term wander accumulation studies.

Appendix VII

Hypothetical Reference Models (HRMs) for CBRx and ODUj[/i] payload jitter and short-term wander accumulation

VII.1 Discussion

This appendix describes the Hypothetical Reference Models (HRM) used to obtain the ODCp (desynchronizer) jitter transfer requirements in A.7.3 and the ODCp jitter generation requirements in A.5.1.2. These requirements, together with the HRM, are consistent with the CBRx payload jitter network limits and jitter tolerance requirements, expressed by the requirements for SDH signals in ITU-T Rec. G.825. These requirements are also consistent with the ODUj[/i] payload jitter network limits and jitter tolerance requirements, expressed by the requirements for OTUk signals in 5.1/G.8251 and 6.1.1/G.8251 (and their subclauses). In addition, these requirements are consistent with the CBRx payload short-term wander TDEV requirements, expressed by the Option 1 and Option 2 TDEV masks in ITU-T Rec. G.813 (see Figure 6/G.813, Input wander tolerance (TDEV) for option 1, and Figure I.1/G.813, Synchronization network limit to maintain 1544 kbit/s slip performance as defined in ITU-T Rec. G.822, respectively). The details of the payload jitter and short-term wander (TDEV) accumulation analyses leading to the above requirements and the HRMs are given in Appendix VIII.

Appendix II/G.8251 describes an HRM for the transport of synchronization over OTN via SDH clients. That HRM contains a total of 100 mapping or multiplexing OTN network elements (and for each mapping or multiplexing network element there is a corresponding demapping or demultiplexing network element). The specific example of Figure II.1/G.8251 has 10 "OTN islands", where each island[1] consists of one mapping/demapping and 9 multiplexing/demultiplexing network elements and is separated from each adjacent island by an SSU. However, Appendix II is considered only with long-term wander accumulation, which depends mainly on total buffer storage of all the OTN network elements. In fact, the distribution of the mapping/demapping or multiplexing/demultiplexing elements is not important for long-term wander accumulation (this is effectively stated in clause II.2) and, in the worst case, there can be up to 100 mapping/demapping or multiplexing/demultiplexing elements between two adjacent SSUs or SECs. The total long-term wander accumulation is bounded by the total mapper or multiplexer buffer capacity of 100 network elements (wherever they are in the HRM). This consideration gave rise to the maximum buffer hysteresis requirements described in clause II.5/G.8251 and specified in ITU-T Rec. G.798.

While long-term wander accumulation can be bounded by the total buffer storage of all the network elements, jitter accumulation and short-term wander accumulation do depend more heavily on the distribution of the mapping/demapping and multiplexing/demultiplexing elements in the HRM. If there is no ODUk multiplexing, i.e. if there is only mapping and demapping of a CBRx payload,

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[1] This use of the term "island" differs from other usage, where an island is taken to be a single mapper/demapper or multipexer/demultiplexer pair.

then the worst case is that of 100 mapping/demapping operations between adjacent SECs or SSUs. If there is ODUk multiplexing, then the worst case is still that of 100 mapping/demapping or multiplexing/demultiplexing operations between adjacent SECs or SSUs, but now one must also consider the relative numbers and placement of the CBRx to ODU1 mappings, ODU1 to ODU2 multiplexings, and ODU2 to ODU3 multiplexings.

Two HRMs were developed for the jitter and short-term wander accumulation studies described in Appendix VIII/G.8251. These HRMs, denoted *HRM* 1 and *HRM* 2, respectively, are:

HRM 1: (CBR2G5→ODU1→CBR2G5) + (33 identical tandem of CBR2G5→ODU1→ODU2→ODU3→ODU2→ODU1→CBR2G5).

HRM 2: (33 CBR2G5→ODU1→ CBR2G5) + [CBR2G5→ODU1+ (33 ODU1→ODU2→ODU1) + {ODU1→ODU2 + (33 ODU2→ODU3→ODU2) + ODU2→ODU1} + ODU1→ CBR2G5]

These HRMs were chosen to:

1) bound the types of scenarios that occur in practice regarding the distribution of the higher levels of ODUk multiplexing within the OTN islands; and

2) bound the jitter and short-term wander accumulation that occurs in a network of OTN islands.

The HRMs were meant to be bounding scenarios, rather than to represent actual network configurations that will occur in practice. HRM 1 represents one extreme, where the higher levels of ODUk multiplexing (higher level ODUk islands) are distributed uniformly among the lower level ODUk islands. In HRM 1, each ODU1 island (OTN island where CBR2G5 is mapped into ODU1) except the first one contains exactly one ODU2 island (island where ODU1 is multiplexed into ODU2), and each ODU2 island contains exactly one ODU3 island (OTN island where ODU2 is multiplexed into ODU3). HRM 2 represents the other extreme, where the higher levels of ODUk multiplexing are concentrated on one of the lower level ODUk islands. In HRM 2, all the ODU2 islands are concentrated in the final ODU1 island, and all the ODU3 islands are concentrated in the final ODU2 island.

The results in Appendix VIII/G.8251 show that these two HRMs bound the jitter accumulation and short-term wander accumulation, both on the CBRx payloads and ODUj[/i] payloads, that occurs in a network of OTN islands.

Appendix VIII

CBRx and ODUj[/i] payload jitter and short-term wander accumulation analyses

VIII.1 Introduction

This appendix describes the details of the CBRx and ODUj[/i] payload jitter and short-term wander accumulation analyses that led to the ODCp jitter transfer requirements of A.7.3 and the HRM of Appendix VII. A time-domain simulation model for payload mapping jitter and wander and jitter and wander due to ODUk multiplexing was developed. The details of the simulator are described in VIII.2, and jitter and short-term wander simulation results are given in VIII.3. These analyses do not include the effects of any 3R regenerators between the mapper/multiplexer and demapper/demultiplexer. This jitter is of high frequency compared to the maximum ODCp bandwidth of 300 Hz, and is therefore easily filtered by the ODCp.

VIII.2 Simulation model

A time domain simulator was developed to evaluate phase and jitter accumulation over a network of OTN islands. The term *OTN island* denotes a mapping of a CBRx or ODUj[/i] client signal into an ODUkP, transport of the ODUkP with possible multiple multiplexing to ODUm (m > k) and subsequent demultiplexing, and demapping of the client from the ODUkP with a desynchronizer or demultiplexer of specified bandwidth and gain peaking. As indicated in the introduction, the effect of 3R regenerators is ignored because 3R regenerator jitter generation is of high frequency and easily filtered by the ODCp. It is assumed that this operation can be repeated a number of times; i.e. there may be multiple OTN islands. In addition, the operation is recursive in the sense that one OTN island may contain multiple, higher-level OTN islands. A schematic of the model is shown in Figure VIII.1-1[2].

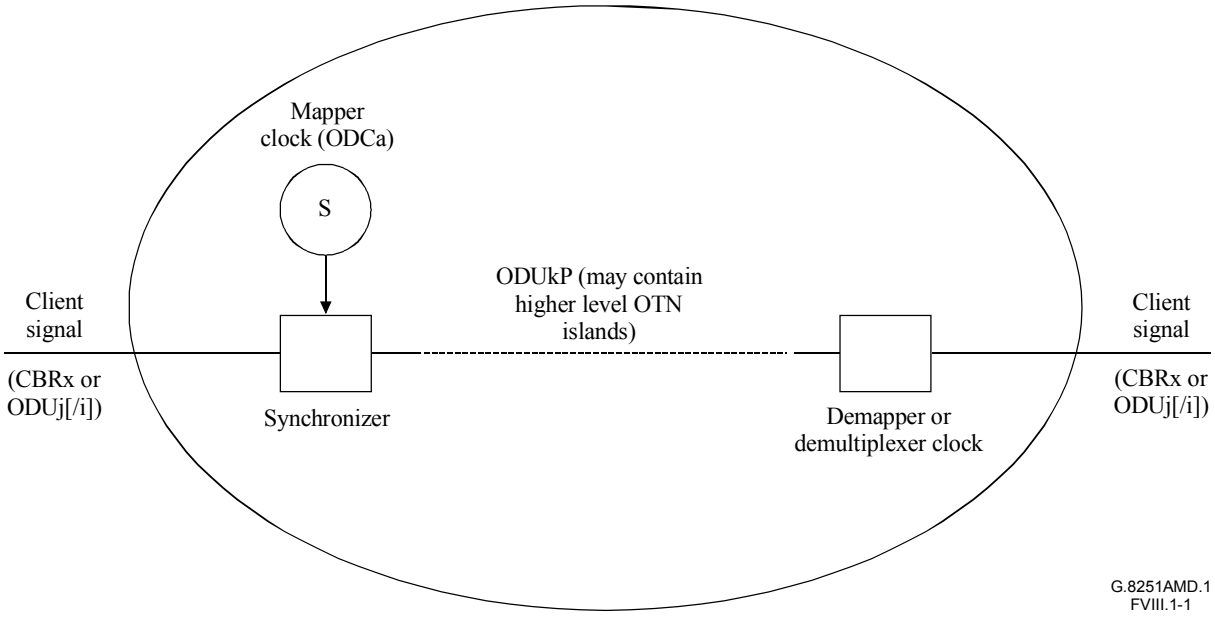
The following subclauses describe the different portions of the model. These include:

– first-order high-pass jitter measurement filter;

– second-order filter with gain peaking and 20 dB/decade rolloff (used in demapper (desynchronizer) and demultiplexer);

– +1/0/–1 byte justification scheme for CBRx mapper or +2/+1/0/–1 byte justification scheme for ODUj[/i] mapper, including the possibility of unequally-spaced justification opportunities when multiplexing ODU2 into ODU3;

– overall model (combining of mapper and demapper, and accumulation over multiple islands).



NOTE – This OTN island may contain one or more higher level OTN islands.

Figure VIII.1-1/G.8251 – Schematic of model for 1 OTN island

[2] Note that the use of the term *OTN island* here is different from the usage in Appendices II and VII. Here, an island is taken to be a single mapper/demapper or multiplexer/demultiplexer pair; therefore, and island here may contain one or more higher-level islands. In Appendices II and VII, an OTN island consists of the CBRx mapper/demapper and all multiplexing/demultiplexing pairs between the mapper and demapper.

VIII.2.1 First-order, high-pass jitter measurement filter

This model is needed to evaluate jitter accumulated in the client signal at the egress of an OTN island. The input to the filter is the client phase accumulated up to that point; the output is the jitter. The filter is typically a first-order, high-pass filter whose 3 dB bandwidth depends on the particular client. For CBRx clients, the jitter measurement filter is specified in Table 1/G.825; for ODUj[/i] clients, the jitter measurement filter is specified in Table 1/G.8251. Actually, the jitter measurement filter is a bandpass filter with both upper (low-pass) and lower (high-pass) cutoff frequencies depending on the particular rate (and increasing with increasing rate)[3]. However, the low-pass jitter measurement cutoff frequencies 20 MHz, 80 MHz, and 320 MHz for the approximately 2.5, 10, and 40 Gbit/s clients, respectively. It will turn out that these frequencies correspond to time constants that are small compared to the time step of the simulation. Therefore, it is unnecessary to model the low-pass portion of the jitter measurement filter. The high-pass portion of the jitter measurement filter depends on whether one is simulating wideband jitter or high-band jitter. The first-order, high-pass filter model covers both cases as long as the appropriate bandwidth is specified.

The transfer function for a first-order, high-pass filter, is:

$$H(s) = \frac{s}{s+a} = 1 - \frac{a}{s+a} \tag{VIII-1}$$

where $a = 2\pi f_0$ and f_0 is the filter 3 dB cutoff frequency. One may obtain a discrete-time model by first obtaining a model for the low-pass filter represented by the $a/(s + a)$ term in Eq. (VIII-1), and then subtracting the result from the input. A first-order, linear differential equation corresponding to the low-pass filter is:

$$\frac{dy}{dt} + ay(t) = au(t) \tag{VIII-2}$$

where $y(t)$ is the filter output and $u(t)$ is the filter input. Now, let T be the time step in the numerical implementation of this filter, with $t = 0$ the beginning of a time step and $t = T$ be the end of the time step. Then, the above may be converted to discrete-time form by multiplying by the integrating factor e^{at} and integrating from 0 to T. The result is:

$$e^{aT} y(T) - y(0) = \int_0^T ae^{at} u(t)\, dt \tag{VIII-3}$$

Finally, assume that the input $u(t)$ can be modelled as a constant equal to $u(0)$ over the time step from 0 to T. Then:

$$y(T) = e^{-aT} y(0) + (1 - e^{-aT}) u(0) \tag{VIII-4}$$

Eq. (VIII-4) is the discrete-time model for the low-pass filter represented by the $a/(s + a)$ term in Eq. (VIII-1). A discrete-time model for the high-pass filter is obtained by subtracting Eq. (VIII-4) from $u(0)$. The result is:

$$y(T) = -e^{-aT} y(0) + e^{-aT} u(0) \tag{VIII-5}$$

Eq. (VIII-5) is the discrete-time model for the high-pass jitter measurement filter.

VIII.2.2 Second-order, low-pass filter with gain peaking and 20 dB/decade rolloff

This model is needed for the CBRx demapper (desynchronizer) and the ODUj[/i] demultiplexer. The transfer function for a second-order, low pass filter with 20 dB/decade rolloff is:

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[3] In addition, the low-pass portion of the jitter measurement filter has a 60 dB/decade rolloff and is maximally flat (Butterworth).

$$H(s) = \frac{2\varsigma\omega_n s + \omega_n^2}{s^2 + 2\varsigma\omega_n s + \omega_n^2} \tag{VIII-6}$$

where ω_n is the undamped natural frequency and ζ is the damping ratio. In the cases of interest here $\zeta > 1$, i.e. the system is overdamped. The damping ratio is related to the gain peaking by (see Eq. (IV.2-31) of ITU-T Rec. G.8251):

$$H_p \approx 1 + \frac{1}{4\zeta^2} \tag{VIII-7}$$

where H_p is the gain peaking expressed as a pure gain (the gain peaking in dB is 20 $\log_{10} H_p$). The damping ratio and undamped natural frequency are related to the 3 dB bandwidth by (see Eq. (IV.2-30) of ITU-T Rec. G.8251):

$$f_{3dB} = \frac{\omega_n}{2\pi}\left[2\zeta^2 + 1 + \sqrt{\left(2\zeta^2 + 1\right)^2 + 1}\right]^{1/2} \tag{VIII-8}$$

where f_{3dB} is the 3 dB bandwidth in Hz. Using Eqs. (VIII-7) and (VIII-8), the damping ratio and undamped natural frequency may be determined using the respective 3 dB bandwidth and gain peaking.

Eq. (VIII-6) is equivalent to the following second-order, linear differential equation:

$$\frac{d^2y}{dt^2} + 2\varsigma\omega_n \frac{dy}{dt} + \omega_n^2 y(t) = 2\varsigma\omega_n \frac{du}{dt} + \omega_n^2 u(t) \tag{VIII-9}$$

where, as in the previous clause, $y(t)$ is the filter output and $u(t)$ is the filter input. Eq. (VIII-9) may be converted to a discrete time model using the standard state variable approach (see [1]). Consider a second-order equation with the same left-hand side as Eq. (VIII-9) but right-hand side equal to the input $u(t)$. For this equation, define state variables x_1 and x_2, where x_1 is equal to the output of this equation and x_2 is the derivative of the output. The output $y(t)$ of Eq. (VIII-9) is then easily obtained as a linear combination of x_1 and x_2 due to the linearity of Eq. (VIII-9). The resulting equations, written in standard matrix notation, are:

$$\begin{aligned} \dot{\mathbf{x}} &= \mathbf{A}\mathbf{x} + \mathbf{B}u \\ y &= \mathbf{C}\mathbf{x} \end{aligned} \tag{VIII-10}$$

where:

$$\mathbf{A} = \begin{bmatrix} 0 & 1 \\ -\omega_n^2 & -2\varsigma\omega_n \end{bmatrix} \qquad \mathbf{B} = \begin{bmatrix} 0 \\ 1 \end{bmatrix} \qquad \mathbf{C} = \begin{bmatrix} \omega_n^2 & 2\varsigma\omega_n \end{bmatrix}$$

Therefore, obtaining a discrete-time model for Eq. (VIII-6) is equivalent to obtaining a discrete-time model for the first of Eq. (VIII-10); the output y is easily obtained from the state $\mathbf{x}$ at a time step using the second of Eq. (VIII-10).

The solution $\mathbf{x}(t)$ to the first of Eq. (VIII-10) may be obtained in the same manner as the solution to the corresponding first-order equation, Eq. (VIII-3). However, the integrating factor is now a matrix-exponential $e^{\mathbf{A}t}$. The matrix exponential is defined using the usual power series representation for e^x, and it can be shown to converge for all matrices whose entries are complex

numbers (and therefore for all systems of interest here)[4]. The result, where as before one integrates from 0 to T where T is the time step, is:

$$\mathbf{x}(T) = e^{\mathbf{A}T}\mathbf{x}(0) + \int_0^T e^{\mathbf{A}(T-t)}\mathbf{B}u(t)\,dt \tag{VIII-11}$$

At this point, the derivation departs from the first-order analysis in that it is necessary to approximate the input $u(t)$ as a first-order expression in t in evaluating the integral in Eq. (VIII-11), rather than a zeroth-order expression as was done in going from Eq. (VIII-3) to (VIII-4). The reason for this is that the input to the desynchronizer filter is typically an "irregular" sawtooth-type function, i.e. the function, to lowest-order neglecting clock and regenerator noise, looks like a linear function of time with jumps occurring at stuffs. Since it is desired to eventually use a time step corresponding to the time between stuff opportunities or, at least, not much smaller than this (so that run times will be reasonable), a linear approximation in the integral is necessary to adequately represent the unfiltered phase (which is input to the desynchronizer filter). Note that one could, in principle, use higher-order approximations (the linear approximation is essentially a trapezoidal rule approximation).

A linear interpolation of the input $u(t)$ between 0 and T is:

$$u(t) \approx u(0) + \frac{u(T) - u(0)}{T}t \tag{VIII-12}$$

Inserting Eq. (VIII-12) into Eq. (VIII-11) and integrating (and noting that matrix exponential functions may be integrated like ordinary exponential functions provided the order of non-commuting matrices (in this case **A** and **B**) is preserved) produces:

$$\mathbf{x}(t) = e^{\mathbf{A}T}\mathbf{x}(0) + \left(e^{\mathbf{A}T} - \mathbf{I}\right)\mathbf{A}^{-1}\mathbf{B}u(0) + \left(e^{\mathbf{A}T} - \mathbf{I}\right)\mathbf{A}^{-2}\mathbf{B}\frac{u(T) - u(0)}{T} - \left[u(T) - u(0)\right]\mathbf{A}^{-1}\mathbf{B} \tag{VIII-13}$$

where **I** is the identity matrix (and is 2 × 2). Note that the first two terms of Eq. (VIII-13) are what would arise from a zeroth-order approximation for the input; the final two terms arise from the linear term in the approximation.

To complete the discretization of Eq. (VIII-10), an explicit expression for the matrix exponential $e^{\mathbf{A}t}$ is needed. This may be obtained by noting that the Laplace transform of $e^{\mathbf{A}t}$ is given by:

$$\mathsf{L}(e^{\mathbf{A}t}) = (s\mathbf{I} - \mathbf{A})^{-1} \tag{VIII-14}$$

where L denotes the Laplace transform. The matrix exponential $e^{\mathbf{A}t}$ may now be evaluated by calculating the inverse of the matrix $s\mathbf{I} - \mathbf{A}$ and then evaluating the inverse Laplace transform of each of the entries (it can be shown that the Laplace transform of a matrix exponential function is equal to the matrix of Laplace transforms of each of the entries). The result is:

$$e^{\mathbf{A}T} = \begin{bmatrix} e^{-aT}\cosh bT + \dfrac{a}{b}e^{-aT}\sinh bT & \dfrac{1}{b}e^{-aT}\sinh bT \\ -\dfrac{a^2 - b^2}{b}e^{-aT}\sinh bT & e^{-aT}\cosh bT - \dfrac{a}{b}e^{-aT}\sinh bT \end{bmatrix} \tag{VIII-15}$$

[4] The proof of this is particularly simple for the case where the matrix **A** is diagonalizable.

where:

$$a = \varsigma\omega_n$$
$$b = \omega_n\sqrt{\varsigma^2 - 1} \qquad \text{(VIII-16)}$$
$$a^2 - b^2 = \omega_n^2$$

The discrete-time filter is given by Eqs. (VIII-13), (VIII-15), and the second of Eq. (VIII-10). Given the state **x**(0) and input $u(0)$ at the beginning of a time step, Eqs. (VIII-13) and (VIII-15) are used to obtain the state **x**(T) at the end of the time step. The second of Eq. (VIII-10) is then used to obtain the filter output $y(t)$.

VIII.2.3 Mapper/multiplexer model

A +1/0/–1 or +2/+1/0/–1 byte justification (stuffing) scheme is modelled for the mapper or multiplexer, respectively. To determine whether to do a positive justification at a justification opportunity, the buffer fill and total number of justifications up to that point are kept track of (separately for the mapper/multiplexer of each island). Let $\phi_r(t)$ be the read clock phase (in UI) at time t, $\phi_w(t)$ be the write clock phase (in UI) at time t, $B(t)$ the synchronizer buffer fill (in UI) at time t, B_0 the initial buffer fill (in UI) at time zero, $n_{stuff}(t)$ the algebraic sum of the byte justifications up to (but not including) time t, and U the number of unit intervals in one byte (i.e. 8). Then:

$$B(t) = \phi_w(t) - \phi_r(t) + B_0 + Un_{stuff}(t) \qquad \text{(VIII-17)}$$

If $B(t)$ exceeds in the positive direction the upper mapper/multiplexer buffer threshold, a negative justification is performed[5]. In doing this, n_{stuff} is decremented by 1. Conversely, if $B(t)$ exceeds in the negative direction the lower mapper/multiplexer buffer threshold, a positive justification is performed. In doing this, n_{stuff} is incremented by 1. Note that n_{stuff} is needed to calculate the phase input to the desynchronizer (described shortly).

The write clock phase is equal to the phase output from the previous island at this level (i.e. if the current island is an ODUk island, this is the phase output from the previous ODUk island in the current chain) with any accumulated jitter from that island. The write clock phase for the first island in the current chain is equal to the client signal phase input to that island. If phase is measured with respect to the nominal client signal rate f_0 (in UI/s), which is input, and if the client is allowed to have a frequency offset y_{client} relative to this (in ppm), then the write clock phase for the first island in the current chain is:

$$\phi_{w,island\ 1}(t) = (1.0\times10^{-6})Uf_0 y_{client} t \qquad \text{(VIII-18)}$$

The simulation model allows the client frequency offset to be set on input or chosen randomly from a uniform distribution between $\pm y_{client,max}$, where $y_{client,max}$ is set on input.

In calculating the read clock phase, server layer fixed overhead is neglected. In addition, in the multiplexing case the read clock refers only to the portion of the server payload available for the client in question (and not the portion used for other clients multiplexed with this one). Then, the client and server effective nominal rates are the same. However, the server clock (read clock) is allowed to have a frequency offset y_{clock} relative to its nominal rate. Then, the read clock phase is:

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[5] Here, the sign convention is used where the transmission of an additional byte, which occurs when $B(t)$ goes above the upper threshold, is referred to as a positive justification, and the transmission of one less byte, which occurs when $B(t)$ goes below the lower threshold, is referred to as a positive justification.

$$\phi_{read}(t) = (1.0 \times 10^{-6}) f_0 y_{clock} t \quad \text{(VIII-19)}$$

The unfiltered phase input to the desynchronizer is equal to the read clock phase, plus the phase due to any multiplexing/demultiplexing of the server into higher level signals, plus the phase due to byte justifications:

$$\phi_{unfilt}(t) = \phi_{read}(t) - Un_{stuff}(t) + \phi_{mux/demux}(t) \quad \text{(VIII-20)}$$

Note that the term $Un_{stuff}(t)$, which accounts for the justifications, enters in Eqs. (VIII-17) and (VIII-20) with opposite signs. This is because the effect of a positive justification is one extra byte on the output and one less byte in the buffer, and vice versa for a negative justification.

The unfiltered phase given by Eq. (VIII-20) is input to the desynchronizer model. This is a second order filter with gain peaking, as described in the previous clause. The time step chosen for this model will be discussed shortly.

To obtain the phase due to any multiplexing/demultiplexing of the server into higher level signals, $\phi_{mux/demux}$, consider first the simple case of CBR2G5 mapped into ODU1, which is then multiplexed (mapped) into ODU2, which is then multiplexed into ODU3. At the CBR2G5 to ODU1 mapper, the stuff decisions are based on the difference between the CBR2G5 clock and mapper clock. Therefore, these stuff decisions are independent of any jitter due to the ODU1 to ODU2 or ODU2 to ODU3 mappings. At the ODU1 to CBR2G5 demapper, the recovered ODU1 clock includes any jitter due to the ODU1 to ODU2 and ODU2 to ODU3 mappings; this phase is added to the phase due to the stuff decisions that were made at the CBR2G5 to ODU1 mapper, and the sum is filtered by the CBR2G5 desynchronizer. Next, looking at the recovered ODU1 clock at the ODU1 to CBR2G5 demapper, it can be argued analogously that this has jitter due to the ODU1 to ODU2 stuffing process at the ODU1 to ODU2 mapper, plus any ODU2 jitter due to its being mapped into ODU3. Both processes are filtered by the ODU2 to ODU1 desynchronizer (demultiplexer). Finally, the ODU2 recovered clock at the ODU2 to ODU1 demapper has jitter due to the ODU2 to ODU3 stuffing process; these stuffs are filtered by the ODU3 to ODU2 desynchronizer.

Therefore, each level of multiplexing may be treated independently of the levels below it (e.g. ODU1 multiplexing into ODU2 is independent of CBR2G5 into ODU1 multiplexing). The simulator must represent the order of the multiplexing operations, i.e. the layout of the islands (this is easy to do using the C language, for example). In any island, the stuff decisions are made based on the phase difference between the client and mapper clocks. Phase is accumulated within the island in going from the mapper to demapper if there are any higher levels of mapping/demapping. This phase is added to the phase due to the stuffs at the demapper, and the total is filtered by the desynchronizer. The whole process is implemented at each level.

Since the simulation is implemented in discrete time, it is desirable for the times of stuff opportunities to occur at integral numbers of time steps. However, achieving this is complicated by the fact that the times between stuff opportunities for the different levels of mapping are not integral multiples of each other. This is because the OTU1/ODU1/OPU1 frame time of 48.971 µs (see ITU-T Rec. G.709/Y.1331) is slightly more than 4 times the OTU2/ODU2/OPU2 frame time of 12.191 µs, which is slightly more than 4 times the OTU3/ODU3/OPU3 frame time of 3.035 µs. These frame times are not in exact ratios of 4 because, when multiplexing 4 ODUk's into ODUm (m = k+1), each ODUk has its OPU and ODU overhead and, in addition, the ODUm has its OPU and ODU overhead. But, the main interest here is the effect of waiting-time jitter and short-term wander, i.e. the variable stuffs due to the stuff decisions at the mappers/multiplexers. The effect of the fixed overhead is of lesser interest; this overhead gives rise to high-frequency phase variation that is easily filtered by the desynchronizers. The mapping processes at all levels can be normalized to a common time base based on the OTU1/ODU1/OPU1 frame time by neglecting the ODU and OPU overhead (except for the actual stuffs). If this is done, it is then only necessary to adjust the maximum positive and negative frequency offsets (i.e. the allowable range of frequency offsets) for

the ODU1, ODU2, and ODU3 mapper clocks such that the ranges of stuff ratios for mapping CBRx into ODU1, ODU1 into ODU2, and ODU2 into ODU3 come out correctly. These calculations may be done using the relations in Appendix V/G.709/Y.1331 (Amendment 1) (see Eq. (V-3)/G.709/Y.1331).

With the above approximation, the "effective" ODU2 frame time in the simulator becomes one-fourth the ODU1 frame time. An ODU1 multiplexed into an ODU2 gets a stuff opportunity every 4 ODU2 frames, and the time between stuff opportunities for this process is equal to that for the mapping of CBR2G5 into ODU1 (namely, the ODU1 frame time, or 48.971 μs). Similarly, the "effective" ODU3 frame time is one-fourth the "effective" ODU2 frame time. An ODU2 multiplexed into ODU3 gets 4 stuff opportunities every 16 ODU3 frames. Therefore, the basic time unit in the simulator must be chosen as the "effective" ODU3 frame time, which is 1/16 the ODU1 frame time, or (48.971)/(16) μs = 3.06069 μs. The time step of the simulation can be no larger than this, but may need to be smaller if any of the filters (desynchronizer or jitter measurement filters) have time constants that are shorter. If the time step needs to be smaller than the "effective" ODU3 frame time, it is taken to be an integral sub-multiple of this frame time. Specifically, the simulation time step is chosen to be the largest submultiple of the "effective" ODU3 frame time that is no more than 0.1 times the smallest filter time constant. Stuffs for mapping CBR2G5 into ODU1 and ODU1 into ODU2 are allowed every 16 of the basic ("effective") ODU3 frame times. Stuffs for mapping ODU2 into ODU3 are allowed every four out of 16 of these basic times.

In multiplexing ODU2 into ODU3, the stuff opportunities need not be equally-spaced. The mapping is described in detail in ITU-T Rec. G.709/Y.1331. When an ODU2 is multiplexed into an ODU3, the ODU2 gets four of every 16 stuff opportunities in 16 successive ODU3 frames. The other 12 stuff opportunities go to the other ODU1s and/or ODU2s being multiplexed. However, the specific 4 frames that a particular ODU2 gets may not be equally spaced, and most likely will not be if ODU1 to ODU3 multiplexing is allowed. This is because the ODU1 client only requires 1 stuff opportunity out of every 16 ODU3 frames. The ODU1 and ODU2 client connections will not necessarily be set up at the same time; therefore, there is no guarantee that, when an ODU2 connection is desired (and the bandwidth is available) that the 4 ODU3 frames that have stuff opportunities will be equally spaced. It is essential that the bandwidth be usable in cases where the stuff opportunities are not equally spaced. Therefore, the possibility of unequally-spaced stuff opportunities is modelled by associating with every island (mapper) an array of length 16. Each array element indicates whether a stuff is or is not allowed on that particular effective ODU3 frame out of each set of 16. For each island, the simulator initializes at the start of the run the particular (effective) ODU3 frames that correspond to stuff opportunities. The initialization may be done in one of three ways:

1) randomly chosen;

2) concentrated; and

3) equally-spaced.

If the stuff opportunities are randomly chosen, then each island will likely have stuff opportunities on different ODU3 frames (even for CBR2G5 into ODU1 or ODU1 into ODU2 mappings, for which there is one stuff opportunity every 16 "effective" ODU3 frames; the particular one will be different for each island).

VIII.2.4 Overall model

The models described in VIII.2.1-VIII.2.3 were combined into an overall model for jitter and wander accumulation in a network of OTN islands. The client signal input to the first island is assumed to be unjittered, but may have a frequency offset from nominal (which may be chosen randomly within a range). The phase output, filtered by the demapper/demultiplexer, from each island is the input phase to the next island at the same level (the write clock for that island). The output of each island can also be separately input to a high-pass jitter measurement filter to evaluate

jitter for that island. Both peak-to-peak and RMS (actually, standard deviation) of phase and jitter are calculated for the outputs of each island. These calculations are performed after an initial time interval has elapsed (specified on input) so that any initial transient may decay (this time may be determined from knowledge of the filter time constants and verified with an initial test run where sample waveforms are examined). In addition, it is possible to save all the phase (filtered and unfiltered) and jitter waveforms output from all the islands into files, though this is not normally done for runs with a large number of islands and appreciable simulation time as the disk storage requirements can be considerable.

The peak-to-peak phase and jitter are evaluated by saving at each time step, after the initialization period, the maximum and minimum phase and jitter samples up to that point. The standard deviation (RMS) is evaluated as the square root of the sample standard variance, which is given by (it is assumed in this calculation that the number of time steps is sufficiently large that the difference between the number of samples and the number of samples minus one (the number of degrees of freedom) can be neglected):

$$\sigma_\phi^2 = \frac{1}{n-n_0}\sum_{j=n_0+1}^{n}\phi^2(jT) - \left(\frac{1}{n-n_0}\sum_{j=n_0+1}^{n}\phi(jT)\right)^2 \qquad \text{(VIII-21)}$$

In Eq. (VIII-21), $\phi(jT)$ is the phase or jitter at the *jth* time step, σ_ϕ^2 is the sample variance, n is the number of time steps, and n_0 is the number of time steps in the initialization period.

The simulation model requires a random number generator. For the simulation cases performed here, a random number generator based on a combination of a linear congruential and a shift register algorithm was used. The period of this generator is of order $(2^{32} - 1)(2^{48} - 1) = 1.2 \times 10^{24}$. In all cases, multiple independent replications were run by saving the state of the random number generator in a file and using this state to initialize the generator for the subsequent replication. The number of random samples, i.e. the number of invocations of the generator, was counted (using 2 32-bit integer variables) so it could always be checked that the supply of random samples was not exhausted.

The simulation model was implemented in a C program.

VIII.3 Jitter and short-term wander simulation results

Simulations were run for each of the two HRMs documented in Appendix VII. It was indicated in the previous clause that the justification opportunities for the multiplexing of ODU2 into ODU3 need not be equally spaced. Three types of cases were considered:

- Stuff opportunities chosen randomly in each ODU2→ODU3 mapping.
- Stuff opportunities concentrated together for each ODU2→ODU3 mapping (i.e. in a set of 16 ODU3 frames, an ODU2 gets 4 stuff opportunities in a row, followed by 12 frames with no stuff opportunity).
- Stuff opportunities equally spaced (one every 4 ODU3 frames).

The first case is the most realistic, the second the most conservative, and the third the least conservative.

Next, a worst-case condition when using a positive/zero/negative justification scheme, for purposes of jitter and wander accumulation, can occur when the frequency offset between the client and mapper clocks is small but non-zero, and sufficiently small that the resulting stuff rate is small compared to the desynchronizer bandwidth. Therefore, the following two types of cases were considered:

- Client and mapper clocks free-running with frequency offsets within their required frequency tolerances (i.e. ± 20 ppm, but adjusted to account for the fact that ODUk fixed overhead is neglected).
- Client and mapper clocks free-running with frequency offsets of ± 0.05 ppm.

In the latter case, the maximum frequency offset between client and server is 0.1 ppm. For mapping CBR2G5 into ODU1 (and therefore approximately for ODU1 into ODU2) this gives rise to a maximum mean stuff rate of 31 Hz, which is well within the 300 Hz desynchronizer bandwidth. To show this, let y be the frequency offset between the client and OPU1 clocks (for a particular mapper), and f_0 be the nominal OPU1 rate. Then the rate at which excess phase (positive or negative) is accumulated is yf_0. Since the stuff unit is 1 byte, or 8 UI (positive or negative), the mean time between stuffs is approximately $8/yf_0$, and the mean rate of stuffs is $yf_0/8$. If the maximum frequency offset magnitude between client and OPU1 is $y_{\max} = 0.1$ ppm, the maximum mean stuff rate is given by:

$$f_{stuff,\max} = (0.1\times10^{-6})(2.488320\times10^{9})/8 = 31\,\text{Hz} \qquad \text{(VIII-22)}$$

For mapping ODU2 into ODU3, in the best case the rate would be 4 times this, or 124 Hz, which is still within the 300 Hz desynchronizer bandwidth.

Then, considering that there are 2 HRMs, 3 sets of assumptions on stuff opportunities, and 2 sets of assumptions on clock accuracies, a total of 12 cases can be considered. These are summarized in Table VIII.1 (designated Cases 1-12).

Also indicated in Table VIII.1 is the number of independent replications of the simulation run for each case. If 300 independent replications are run, a good level of statistical confidence for the 95th percentile of a distribution can be obtained (i.e. if 300 independent samples of a population are placed in ascending order, a 99% confidence interval for the 95th percentile of the distribution for this population is given by the interval between the 275th and 294th samples (the 7th and 26th largest samples). This result follows from the fact that if the samples are selected independently and all have the same distribution, then reasonably tight confidence intervals for a percentile of the distribution are obtained from a binomial distribution (see [2] for details). However, due to constraints on computational resources, only Cases 9-12 had 300 replications completed. For the other cases, it is still possible to obtain 99% confidence intervals for the 95th percentile of the respective distribution; however, the intervals will be larger than those with 300 replications because the number of replications is smaller (see Table VIII.3).

Table VIII.1/G.8251 – Summary of simulation cases

Simulation case	Hypothetical reference model	Stuff opportunities	Clock offsets	Number of independent replications of simulation
1	HRM 1	Randomly Selected	Random within free-run accuracies	271
2	HRM 2	Randomly Selected	Random within free-run accuracies	271
3	HRM 1	Randomly Selected	Random within ±0.05 ppm	271
4	HRM 2	Randomly Selected	Random within ±0.05 ppm	271
5	HRM 1	Concentrated	Random within free-run accuracies	191

Table VIII.1/G.8251 – Summary of simulation cases

Simulation case	Hypothetical reference model	Stuff opportunities	Clock offsets	Number of independent replications of simulation
6	HRM 2	Concentrated	Random within free-run accuracies	191
7	HRM 1	Concentrated	Random within ±0.05 ppm	255
8	HRM 2	Concentrated	Random within ±0.05 ppm	255
9	HRM 1	Equally Spaced	Random within free-run accuracies	300
10	HRM 2	Equally Spaced	Random within free-run accuracies	300
11	HRM 1	Equally Spaced	Random within ±0.05 ppm	300
12	HRM 2	Equally Spaced	Random within ±0.05 ppm	300

Table VIII.2 shows remaining parameters for the simulation cases. These are common to all the cases. Note that the initialization time indicated in Table VIII.2 is the time needed for initial transients to decay before beginning any peak-to-peak jitter or TDEV calculation.

Table VIII.2/G.8251 – Parameters common to all simulation cases

Parameter	Value
Stuffing mechanism	+/–/0 byte stuffing
Desynchronizer/demultiplexer order	2nd order, with 20 dB/decade roll-off
Desynchronizer/demultiplexer 3 dB bandwidth	300 Hz
Desynchronizer/demultiplexer gain peaking	0.1 dB
Desynchronizer/demultiplexer damping ratio	4.6465 (corresponds to 0.1 dB gain peaking)
Mapper buffer initial conditions	Random
Time step	3.0607×10^{-6} s
Simulation time	31 s
Initialization time	1.0 s

VIII.3.1 Results for wide-band jitter accumulation

Results are given in this clause for peak-to-peak wide-band jitter accumulation for the CBR2G5 client and, for Model 2, the ODU1 client. The ODU1 jitter accumulation results in Model 2 are for the final ODU1 island; here, the ODU1 is transported over 33 ODU2 islands followed by a single ODU2 island containing 33 ODU3 islands.

A 99% confidence interval for the 95th percentile is obtained for each case by ordering the peak-to-peak jitter results from smallest to largest. A 99% confidence interval for the 95th percentile of the distribution then falls between the samples whose indices (after ordering) are given in Table VIII.3. As indicated earlier, this result follows from the fact that the confidence intervals may be obtained from a binomial distribution; see [2] for more details (the same result is applied to obtaining confidence intervals for MTIE in clause II.5/G.810).

Table VIII.3/G.8251 – Extent of 99% confidence interval for 95th percentile of a distribution, for various numbers of samples

Number of samples	Index of sample for lower end of 99% confidence interval	Index of sample for lower end of 99% confidence interval
300	275	294
271	248	266
255	234	251
191	174	189
NOTE – Samples are assumed to have been ordered from smallest to largest.		

VIII.3.1.1 CBR2G5 client wide-band jitter accumulation results

Results for CBR2G5 client wide-band jitter accumulation for Cases 1-12 are given in Figures VIII.3-1 through VIII.3-12, respectively. The accumulation is shown over 34 ODU1 islands (this is the number of ODU1 islands for each case; the remaining islands are ODU2 and ODU3 islands).

The first thing to note is that the peak-to-peak jitter accumulation is within the 1.5 UIpp network limit of ITU-T Rec. G.825 in all cases. The worst case appears to be Case 7, where the largest upper extent of the peak-to-peak jitter (largest upper extent of the 99% confidence interval for the 95th percentile) is approximately 1.08 UIpp. Some general trends in the results are now discussed.

On examining first the Model 1 cases (Figures VIII.3-1, VIII.3-3, VIII.3-5, VIII.3-7, VIII.3-9, and VIII.3-11), note that the peak-to-peak jitter increases over the first few ODU1 islands, and then remains at a generally constant level for the remaining islands. There is some fluctuation around the generally constant level, but the amplitude of the fluctuation is less than the initial increase. Next, comparing the loose clock tolerance cases (Cases 1, 5, and 9, in Figures VIII.3-1, VIII.3-5 and VIII.3-9, respectively) with the tight clock tolerance cases (Cases 3, 7, and 11, in Figures VIII.3-3, VIII.3-7 and VIII.3-11, respectively), note that the peak-to-peak jitter is larger in the tight clock tolerance cases, and the amount of fluctuation is less. In addition, the increase to the roughly constant level occurs faster in the tight clock tolerance cases, in approximately 3 islands versus 4-10 islands in the loose clock tolerance cases (in these latter cases the fact that the increase is more gradual makes it more subjective in defining when the constant level is reached).

The jitter is larger in the tight clock tolerance cases because in these cases the stuffs are occurring at low enough frequency that they are filtered independently by the desynchronizer. In these cases, the maximum jitter occurs when jitter peaks at successive levels line up. This maximum value is approximately 1.22 UIpp, which may be obtained as follows. First, the zero-to-peak jitter due to a justification of 8 UI for the CBR2G5 to ODU1 mapping, filtered by a 300 Hz low-pass filter desynchronizer and a 5 kHz high-pass jitter measurement filter, is evaluated. Next, the zero-to-peak jitter due to a justification of 8 UI for the ODU1 to ODU2 mapping, filtered by two 300 Hz low-pass desynchronizers (ODU2 to ODU1 and ODU1 to CBR2G5) and a 5 kHz high-pass jitter measurement filter is evaluated. This result is added to the previous result, under the assumption that in the worst case the two peaks line up. The result for ODU2 to ODU3 mapping is obtained, using three desynchronizer filters and recognizing that the UI here is approximately one-fourth that of the CBR2G5 UI. Finally, the entire result is multiplied by 2 to obtain peak-to-peak jitter from zero-to-peak jitter.

It appears that two islands are required in order to have a reasonable probability of obtaining this jitter (the peak-to-peak jitter is around 0.6 UI after 2 islands in Figures VIII.3-3, VIII.3-7 and VIII.3-11). A third island is required to get a jitter peak in the opposite direction. Even so, the theoretical maximum of 1.22 UIpp is not obtained; apparently there is always some overlap of the peaks in the positive and negative directions. In the loose clock tolerance cases (Figures VIII.3-1,

VIII.3-5 and VIII.3-9), the maximum peak-to-peak jitter level is lower and there is more fluctuation. This is because, for these cases, the stuffs can occur at higher frequency and, when this frequency is of the same order as the desynchronizer bandwidth or larger, they interfere with each other.

Next, consider the effect of whether the ODU2 stuff opportunities are concentrated, random, or evenly spaced. In the tight clock tolerance cases (Figures VIII.3-3, VIII.3-7 and VIII.3-11), the maximum peak-to-peak jitter is similar in all three cases (1.08 UIpp for the concentrated stuff opportunities versus 1.06 UIpp for the other two cases). This is because the stuffs tend to be widely separated in these cases (i.e. by more than 16 ODU3 frames). In the loose clock tolerance cases there is slightly more dependence; the maximum peak-to-peak jitter in Case 9 (equally-spaced stuff opportunities, Figure VIII.3-9) is approximately 0.77 UIpp, versus 0.81 UIpp for the other 2 cases (Figures VIII.3-1 and VIII.3-5). In any case, the impact of the stuff opportunity spacing is small in all cases because it affects only the ODU2 to ODU3 mapping, for which the unit interval is only one-fourth as large as that for CBR2G5 to ODU1 or ODU1 to ODU2.

Next, consider the Model 2 cases (Figures VIII.3-2, VIII.3-4, VIII.3-6, VIII.3-8, VIII.3-10 and VIII.3-12), and note that for the initial ODU1 islands that do not contain any ODU2 or ODU3 islands (islands 1-33), the peak-to-peak jitter increases over the first few ODU1 islands and then stays roughly at this level, fluctuating. The behaviour is roughly analogous to the Model 1 cases, except that the steady-state level is less than in the Model 1 cases because it reflects only one level of mapping. There is also less fluctuation in the Model 2 cases compared to the corresponding Model 1 cases (i.e. comparing Cases 1 and 2, 3 and 4, 5 and 6, 7 and 8, 9 and 10, and 11 and 12). Then, the Model 2 cases all show an increase in jitter at the 34th ODU1 island. This is due to the higher levels of mapping in this island (33 ODU1 to ODU2 mapping/demappings, followed by an ODU2 island with 33 ODU3 islands). This increase in jitter in the final island brings the peak-to-peak jitter to approximately the level in the corresponding Model 1 case (it brings it to a slightly lower level in the tight clock tolerance cases and slightly higher level in the loose clock tolerance cases).

The results here indicate that, for consideration of CBR2G5 wide-band jitter accumulation:

- the G.825 network limit of 1.5 UIpp is met;
- the peak-to-peak jitter accumulation increases relatively quickly to a maximum value and remains at this value; the ordering of the types of islands (i.e. ODU1, ODU2, and ODU3) is of secondary importance;
- there is little dependence on the locations of the stuff opportunities;
- the jitter accumulation is higher for smaller clock tolerances.

VIII.3.1.2 ODU1 client wide-band jitter accumulation results

Results for ODU1 client wide-band jitter accumulation for Cases 2, 4, 6, 8, 10, and 12 are given in Figures VIII.3-13 through VIII.3-18, respectively. The accumulation is shown over 33 ODU2 islands, which are numbered from 35 through 67 (this is the number of ODU2 islands in the final ODU1 island for each case; note that the final ODU2 island contains 33 ODU3 islands).

The peak-to-peak jitter accumulation is within the 1.5 UIpp network limit of 5.1/G.8251 in all cases. The maximum peak-to-peak jitter is largest in the tight clock tolerance cases (Figures VIII.3-14, VIII.3-16, and VIII.3-18), where it reaches 0.84 UIpp.

The results are qualitatively similar to the results for CBR2G5 clients. The impact of the location of the stuff opportunities is small. The peak-to-peak jitter increases over the first few islands to a roughly constant level, about which it fluctuates for the remaining islands. The increase is faster and the fluctuations smaller for the tight clock tolerance cases compared to the loose clock tolerance cases. The overall jitter accumulation is larger for the tight clock tolerance cases. Finally, there is an increase in jitter in the final ODU2 island due to the ODU3 islands in this ODU2 island (the previous ODU2 islands do not contain any higher levels of multiplexing).

VIII.3.1.3 STM-16 client short-term wander (TDEV) accumulation results

Results are given in this clause for CBR2G5 client short-term wander accumulation over all the islands. The results are presented in the form of TDEV for the CBR2G5 client emerging from the final ODU1 island. TDEV is displayed for integration times ranging from 3.06 μs (the simulation time step) to approximately 10 s (one-third the total simulated time of 30 s following the 1 s initialization time; note that TDEV involves a second difference calculation, and therefore can be obtained for integration times up to one-third the extent of the data). Note that it is mainly integration times of 0.05 s or larger that are of interest, because TDEV characterizes wander.

For each value of integration time the square root of mean TVAR (mean taken over all the replications) and square root of standard deviation of TVAR (i.e. fourth root of variance of TVAR, taken over all the replications) is obtained. The former is a point estimate of the expected value of TDEV. The latter is an approximation to the standard deviation of TDEV. The 95th percentile of TVAR is approximated as the value 2 standard deviations from the mean TVAR, and the 95th percentile of TDEV is approximated as the square-root of this.

CBR2G5 TDEV results for Cases 1-12 are given in Figures VIII.3-19 to VIII.3-30, respectively. First, note that TDEV is within the 10 ns limit for SDH Option 2 and the 12 ns limit for SDH Option 1 (for the integration times less than 10 s, which are the ones of interest here; see ITU-T Rec. G.813). The maximum TDEV is approximately 1 ns in the loose clock tolerance cases, which occurs for integration time of approximately 0.01 s. The maximum TDEV is approximately 3 ns in the tight clock tolerance cases, which occurs for integration time of approximately 0.3 s. TDEV is larger in the tight clock tolerance cases for longer integration times, but larger in the loose clock tolerance cases for shorter integration times. This is most likely due to the fact that the phase variation in the loose clock tolerance cases has higher frequency.

VIII.3.1.4 Conclusions

The results above indicate that:

- the G.825 network limit of 1.5 UIpp is met for CBR2G5 clients;
- the G.8251 network limit of 1.5 UIpp is met for ODU1 clients;
- the maximum peak-to-peak jitter accumulation increases relatively quickly (over the initial islands) to a maximum value; the ordering of the island types (ODU1, ODU2, ODU3) is of secondary importance;
- there is little dependence on the locations of the stuff opportunities;
- the jitter accumulation is higher for smaller clock tolerances;
- the G.813 wander TDEV limits of 10 ns for SDH Option 2 and 12 ns for SDH option 1 is met for CBR2G5 clients.

The third bullet item is significant; it means that as long as the number of islands exceeds a sufficient number, it does not matter how many there are or what their order is, because the jitter accumulation saturates. In fact, the jitter accumulation saturates for all the CBR2G5 and ODU1 client cases here. This means that there is no need to consider more islands for the ODU1 multiplexing cases (the longest ODU1 client chain was 33 islands), because the jitter has already saturated.

While jitter on ODU2 clients was not considered, this is expected to be similar to the mapping of STM-64 into ODU2. This is because the maximum justification rate is approximately the same for both cases. Jitter for such cases will be smaller than CBR2G5 into ODU1 mapping jitter due to the wider bandwidth jitter measurement high-pass filter.

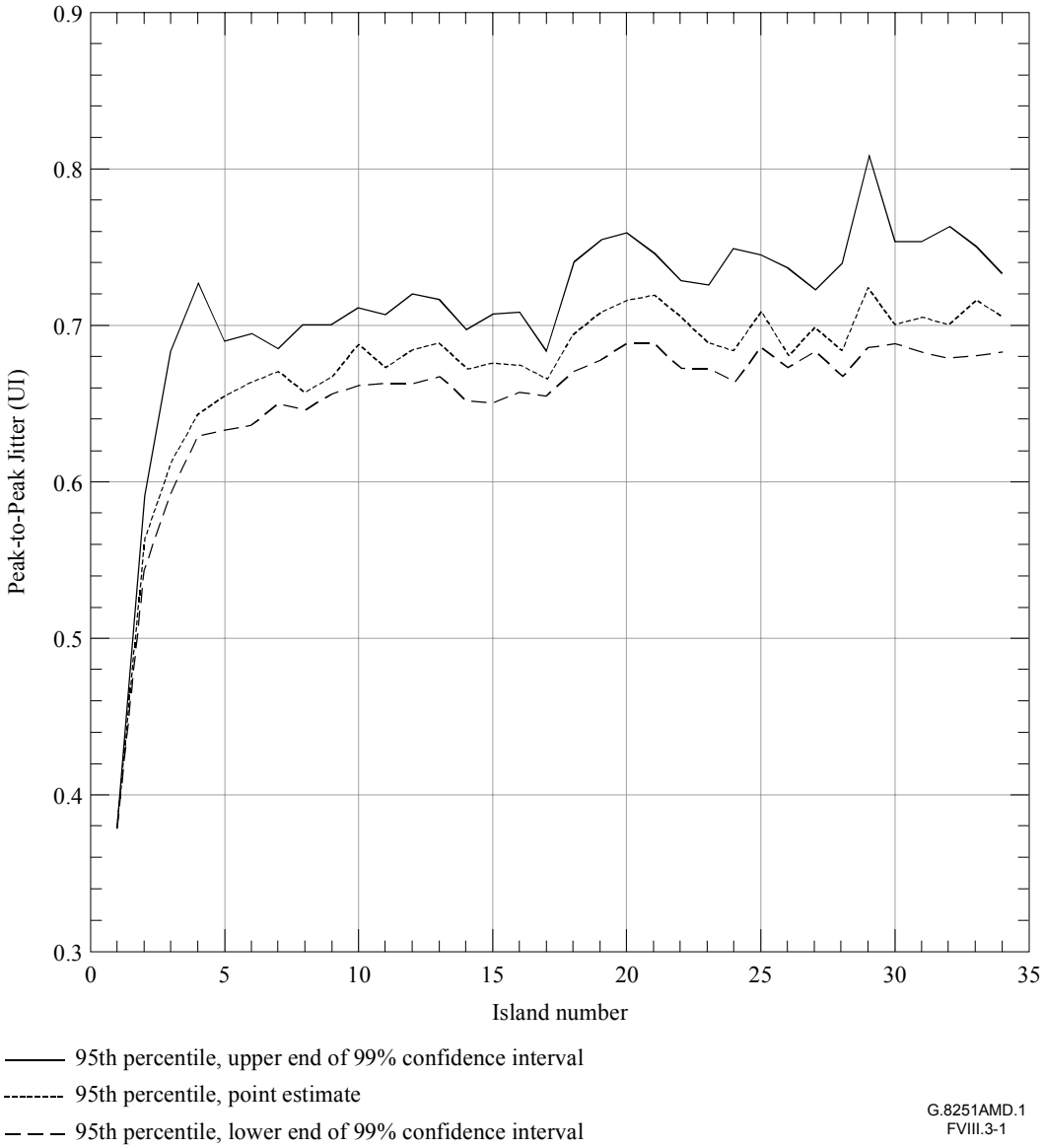
The above simulation cases do not consider high-band jitter. This is because the high-band jitter measurement high-pass filter bandwidth exceeds the wide-band high-pass filter bandwidth by a factor of approximately 200, while the high-band jitter network limit is less than the wide-band

jitter network limit by a factor of 10. The result is that the high-band jitter accumulation will be well below the network limit – by a factor of 20 or more (this result may be obtained by considering the jitter due to an isolated 8 UI justification).

VIII.4 Bibliography

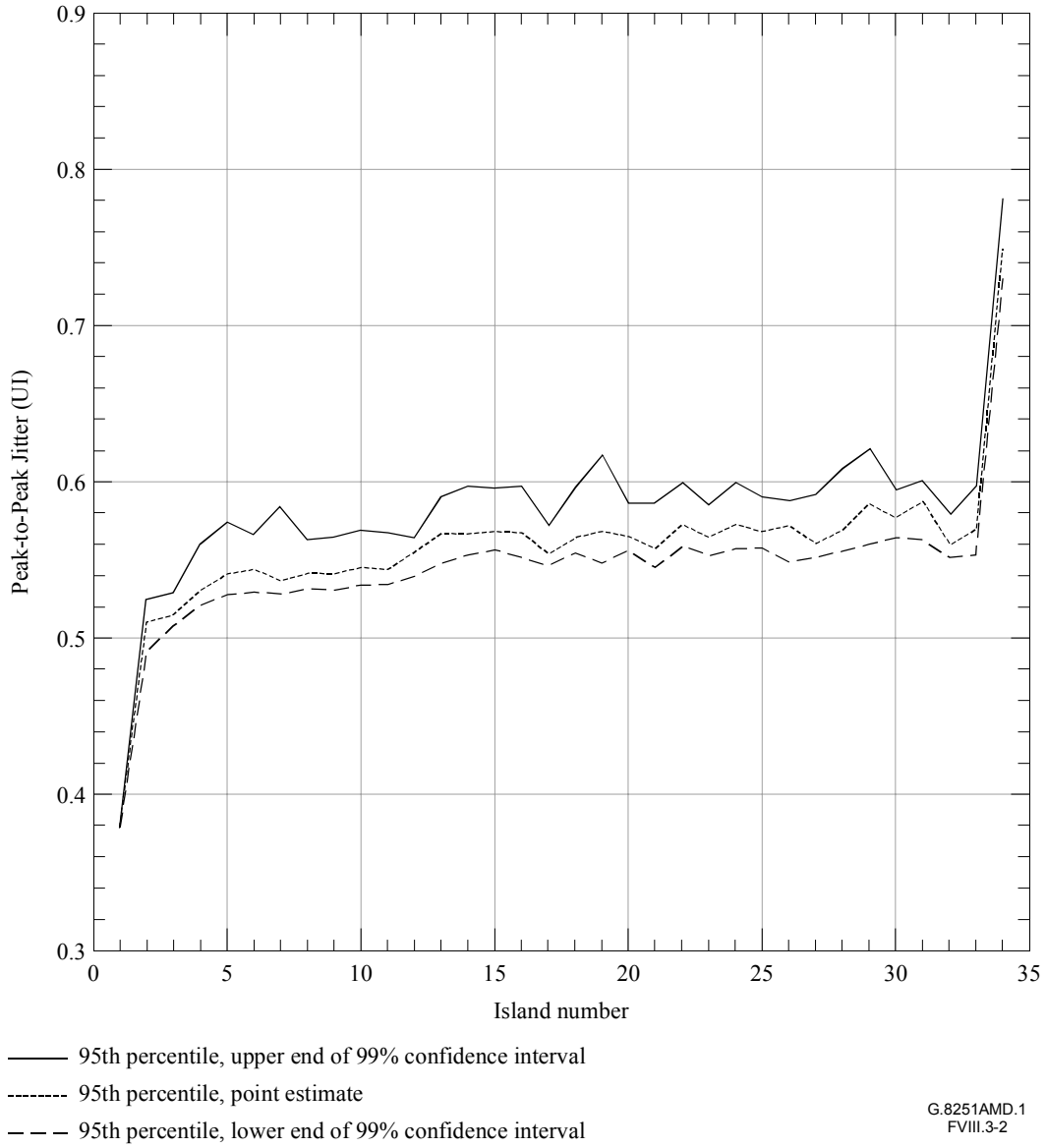
[1] SCHULTZ (Donald G.), MELSA (James L.): State Functions and Linear Control Systems, *McGraw-Hill*, New York 1967.

[2] PAPOULIS (Athanasios): Probability, Random Variables, and Stochastic Processes, Third Edition, *McGraw-Hill*, p.254 (Eq. (9-25)), New York, 1991.



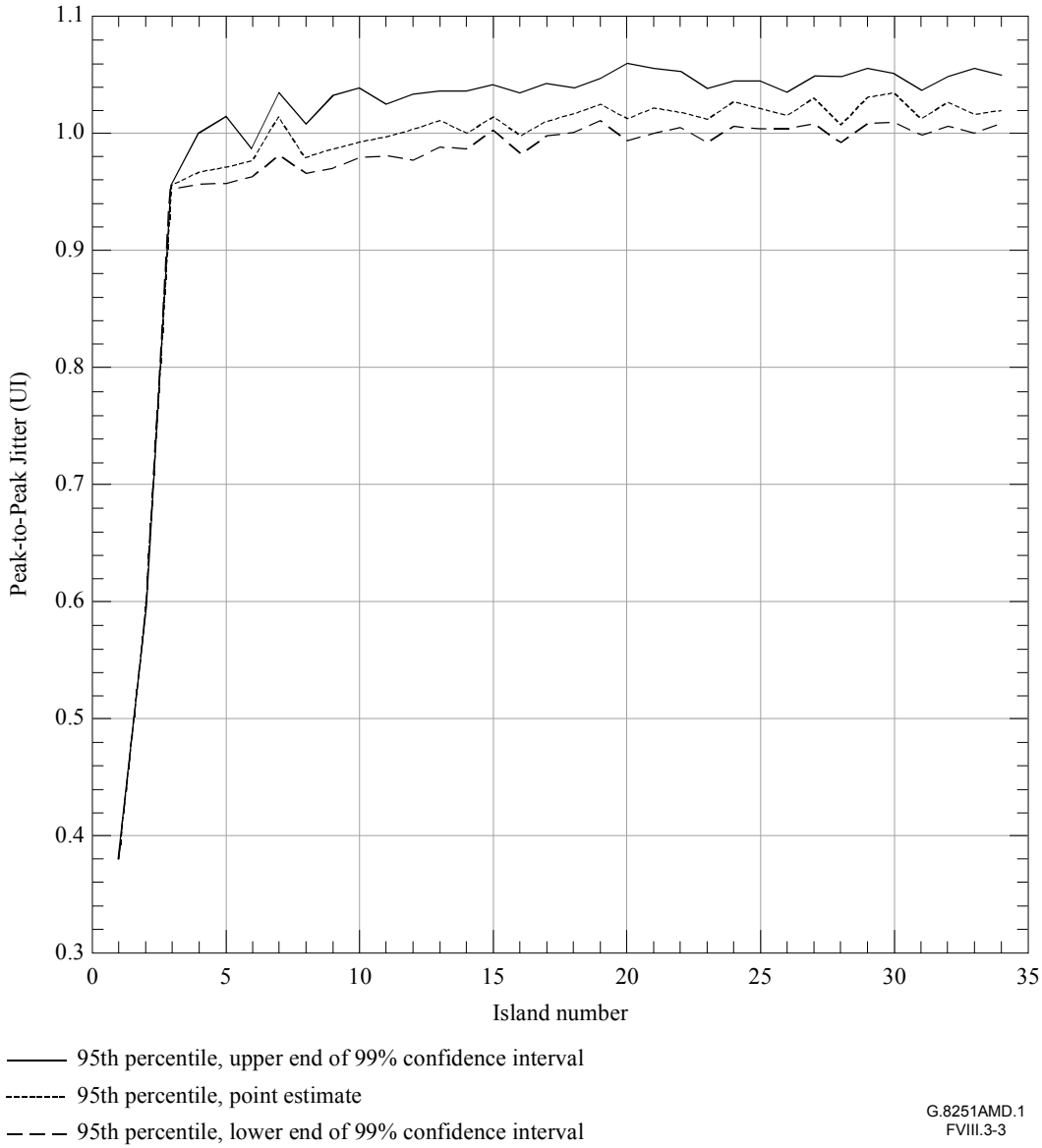
NOTE – ODU1 islands numbered from 1 to 34. 300 Hz desynchronizer at all levels (with 0.1 dB gain peaking). 5 kHz jitter measurement filter. Other assumptions in Tables VIII.1 and VIII.2.

Figure VIII.3-1/G.8251 – CBR2G5 client peak-to-peak wide-band jitter results for Case 1 (Model 1)



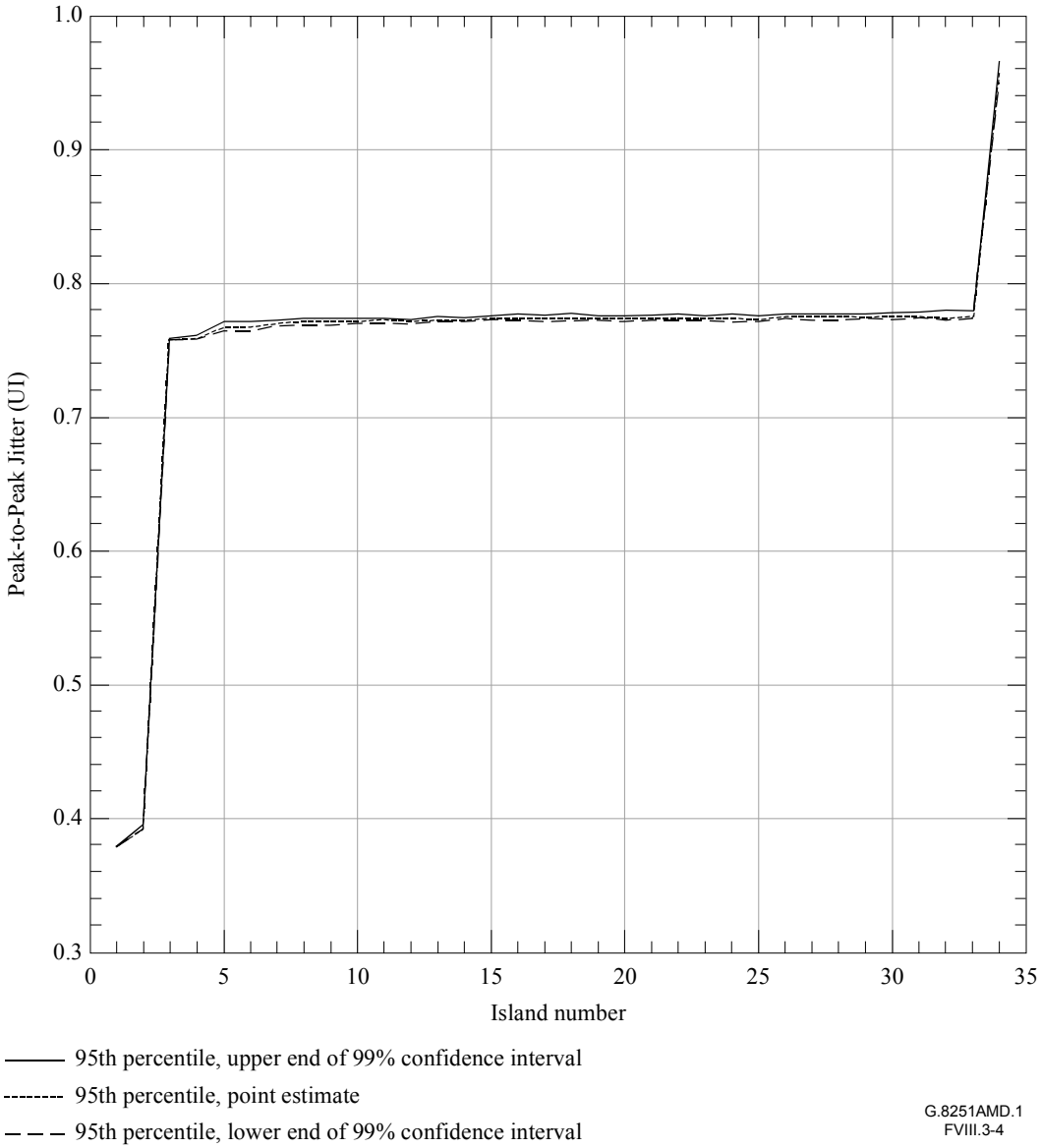
NOTE – ODU1 islands numbered from 1 to 34. 300 Hz desynchronizer at all levels (with 0.1 dB gain peaking). 5 kHz jitter measurement filter. Other assumptions in Tables VIII.1 and VIII.2.

Figure VIII.3-2/G.8251 – CBR2G5 client peak-to-peak wide-band jitter results for Case 2 (Model 2)



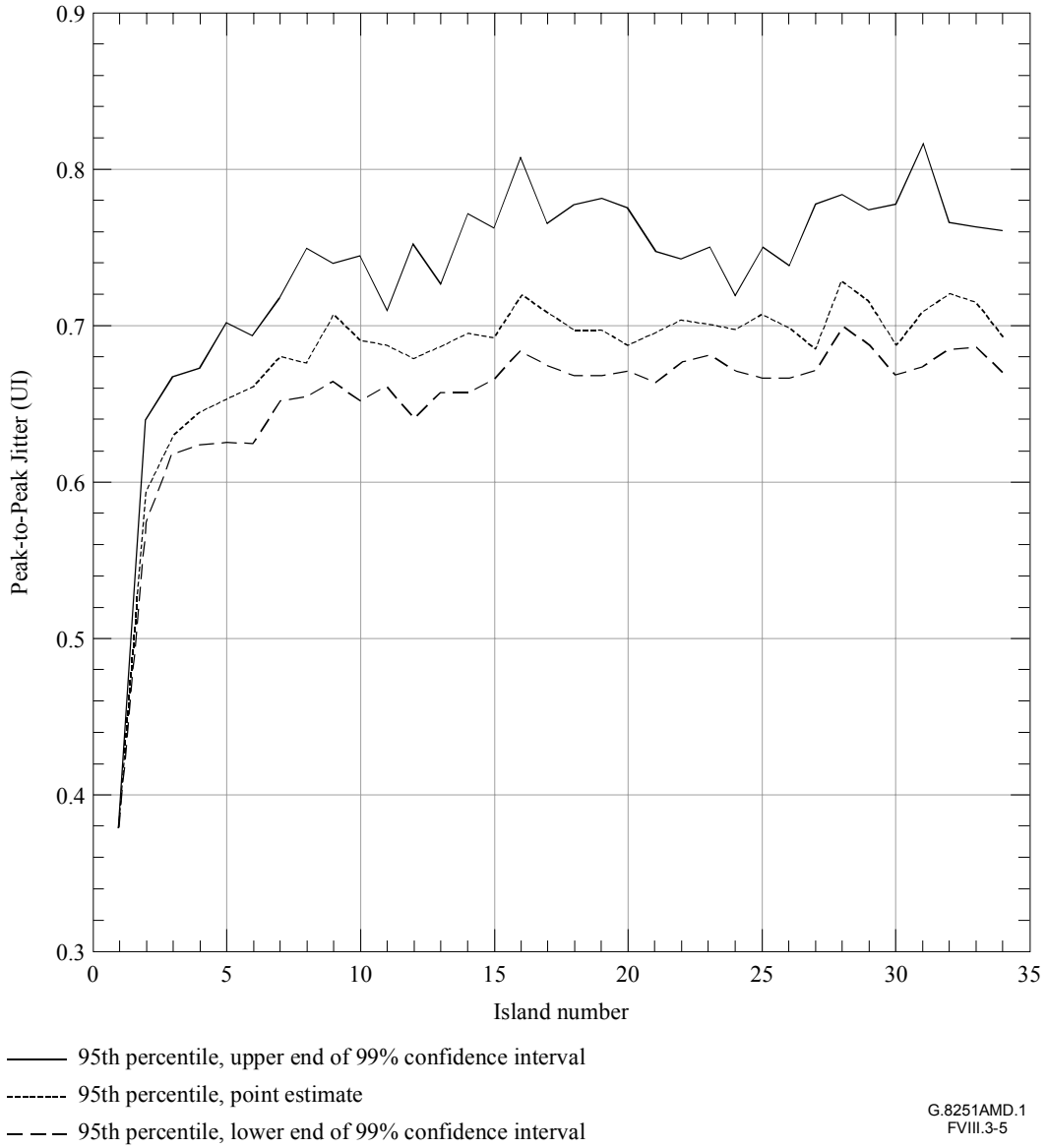
NOTE – ODU1 islands numbered from 1 to 34. 300 Hz desynchronizer at all levels (with 0.1 dB gain peaking). 5 kHz jitter measurement filter. Other assumptions in Tables VIII.1 and VIII.2.

Figure VIII.3-3/G.8251 – CBR2G5 client peak-to-peak wide-band jitter results for Case 3 (Model 1)



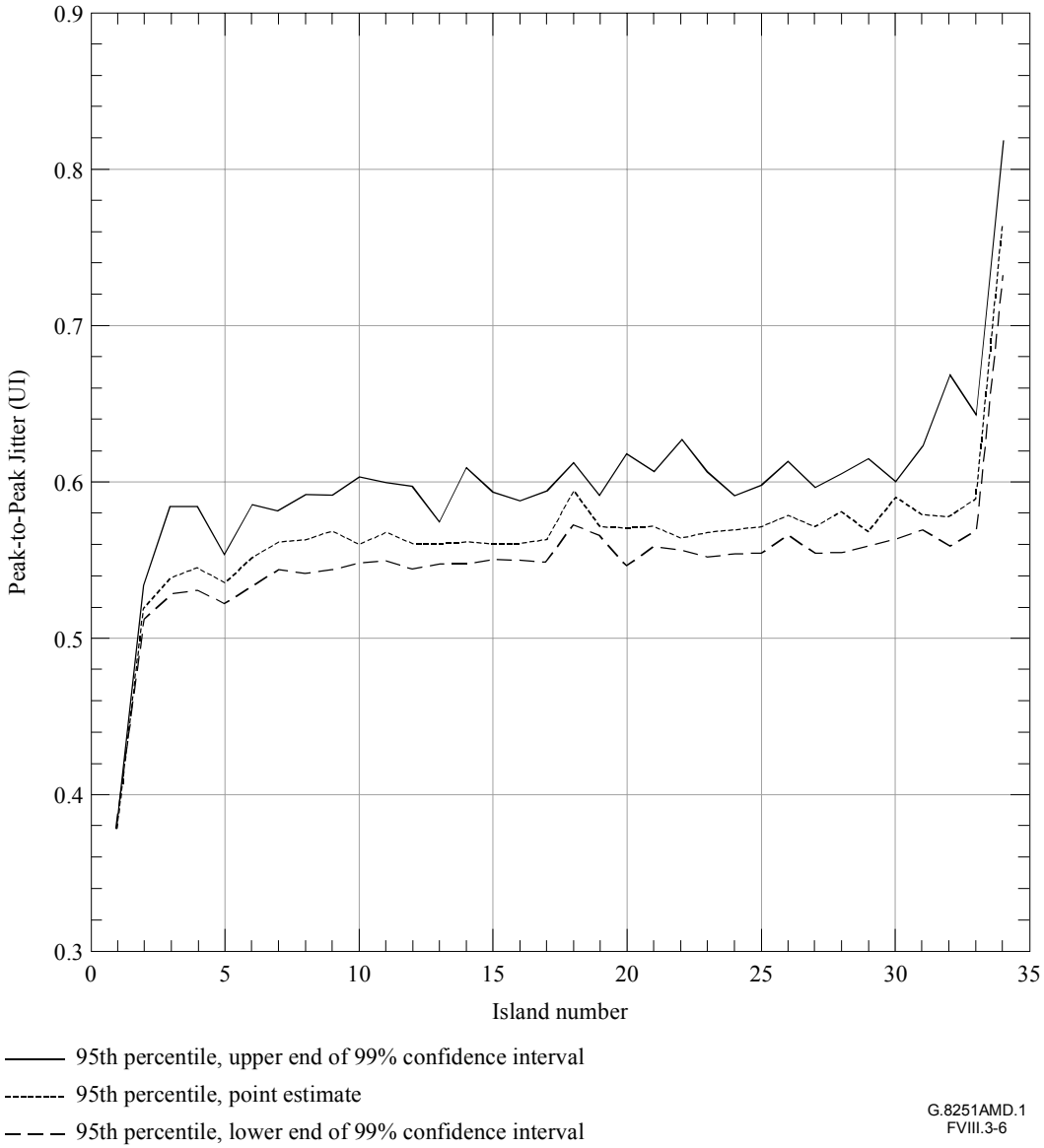
NOTE – ODU1 islands numbered from 1 to 34. 300 Hz desynchronizer at all levels (with 0.1 dB gain peaking). 5 kHz jitter measurement filter. Other assumptions in Tables VIII.1 and VIII.2.

Figure VIII.3-4/G.8251 – CBR2G5 client peak-to-peak wide-band jitter results for Case 4 (Model 2)



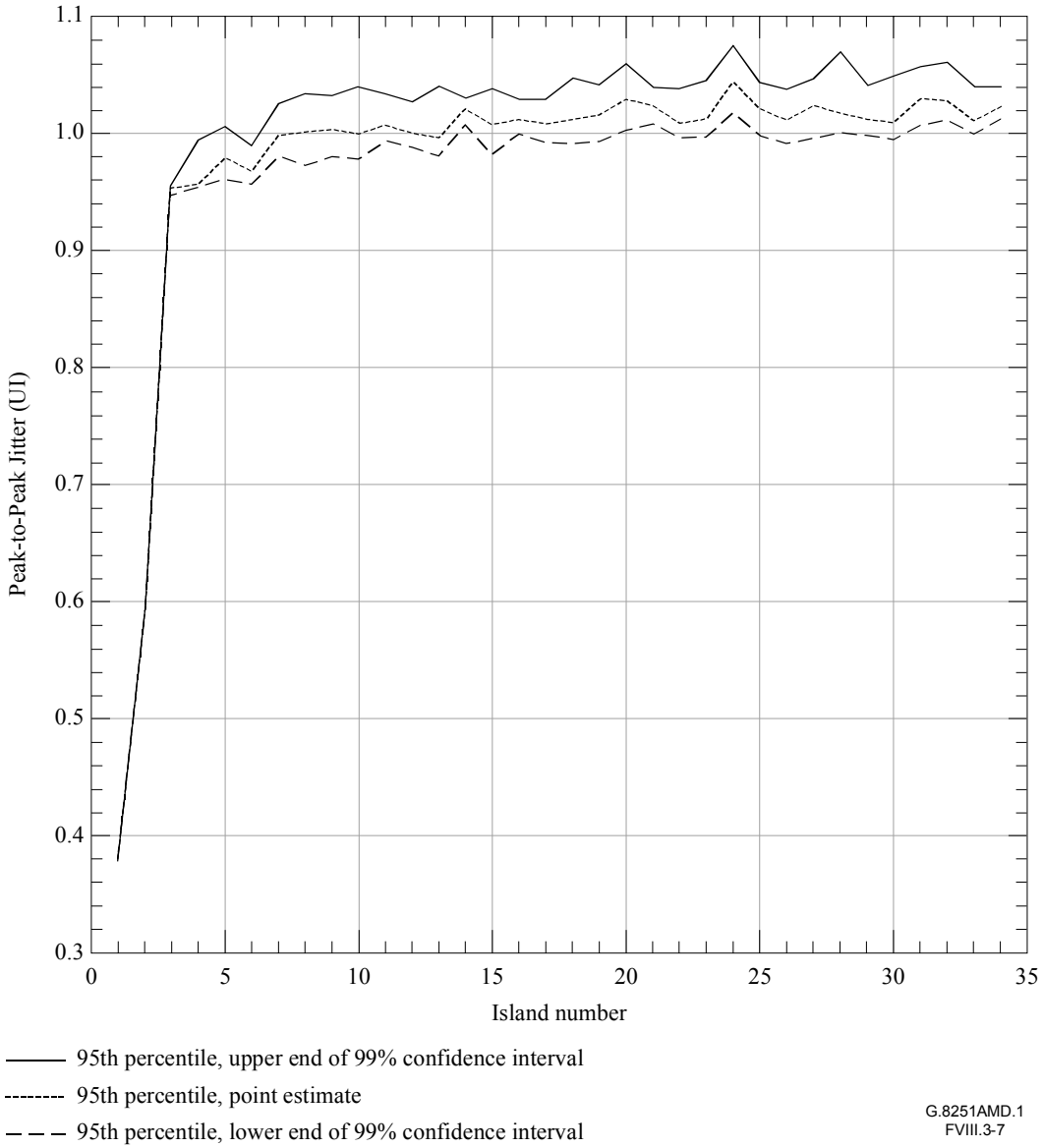
NOTE – ODU1 islands numbered from 1 to 34. 300 Hz desynchronizer at all levels (with 0.1 dB gain peaking). 5 kHz jitter measurement filter. Other assumptions in Tables VIII.1 and VIII.2.

Figure VIII.3-5/G.8251 – CBR2G5 client peak-to-peak wide-band jitter results for Case 5 (Model 1)



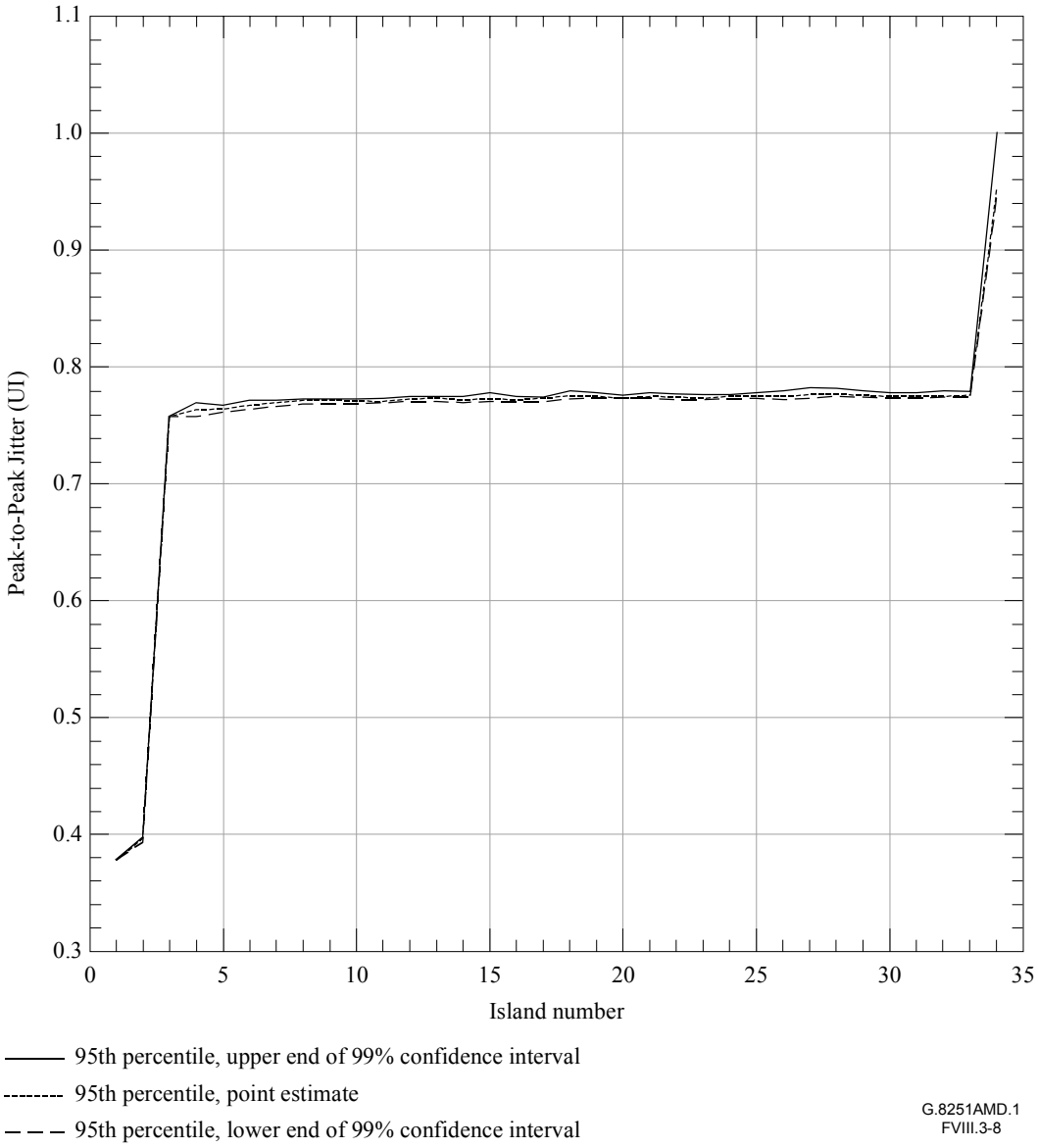
NOTE – ODU1 islands numbered from 1 to 34. 300 Hz desynchronizer at all levels (with 0.1 dB gain peaking). 5 kHz jitter measurement filter. Other assumptions in Tables VIII.1 and VIII.2.

Figure VIII.3-6/G.8251 – CBR2G5 client peak-to-peak wide-band jitter results for Case 6 (Model 2)



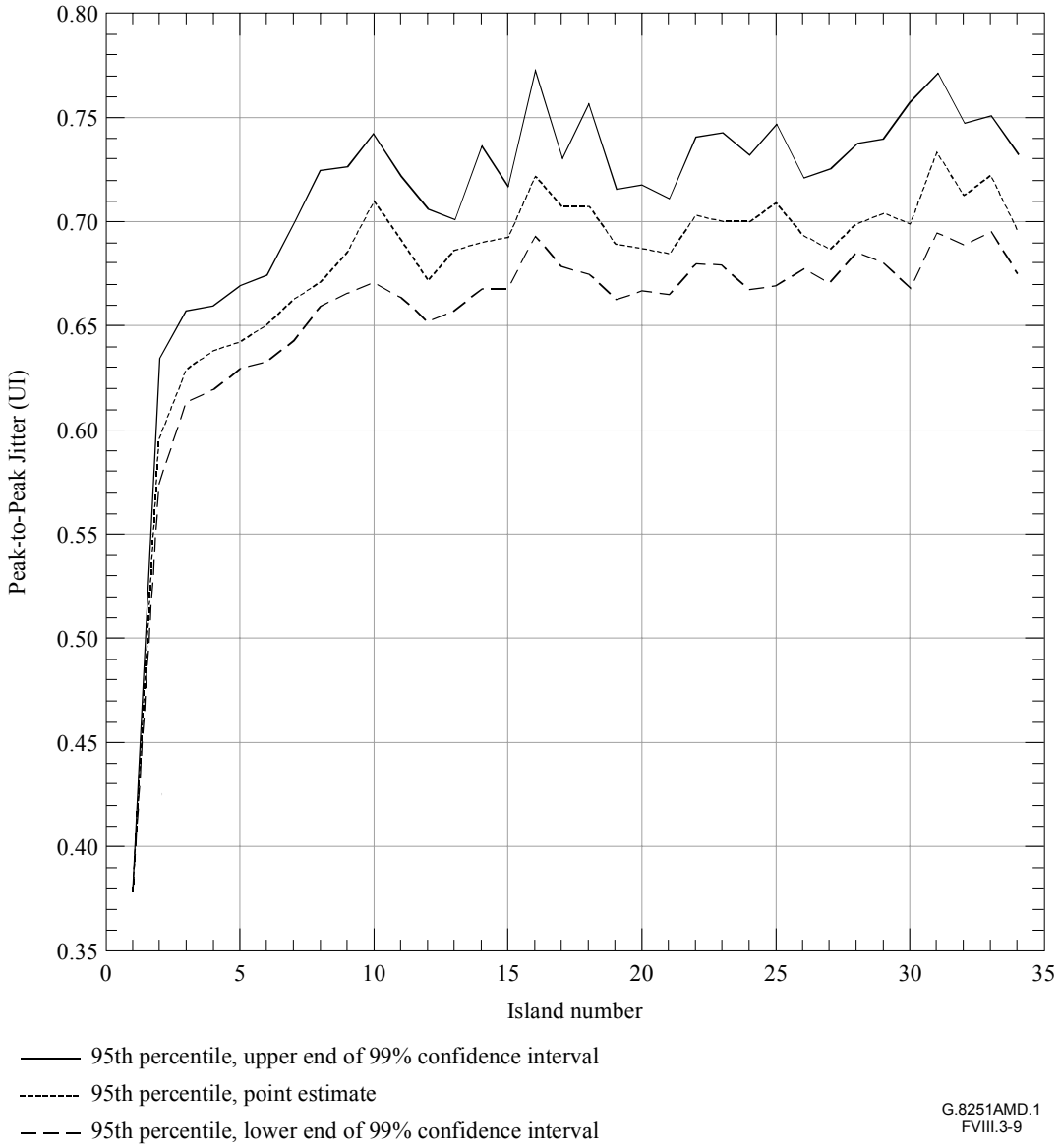
NOTE – ODU1 islands numbered from 1 to 34. 300 Hz desynchronizer at all levels (with 0.1 dB gain peaking). 5 kHz jitter measurement filter. Other assumptions in Tables VIII.1 and VIII.2.

Figure VIII.3-7/G.8251 – CBR2G5 client peak-to-peak wide-band jitter results for Case 7 (Model 1)



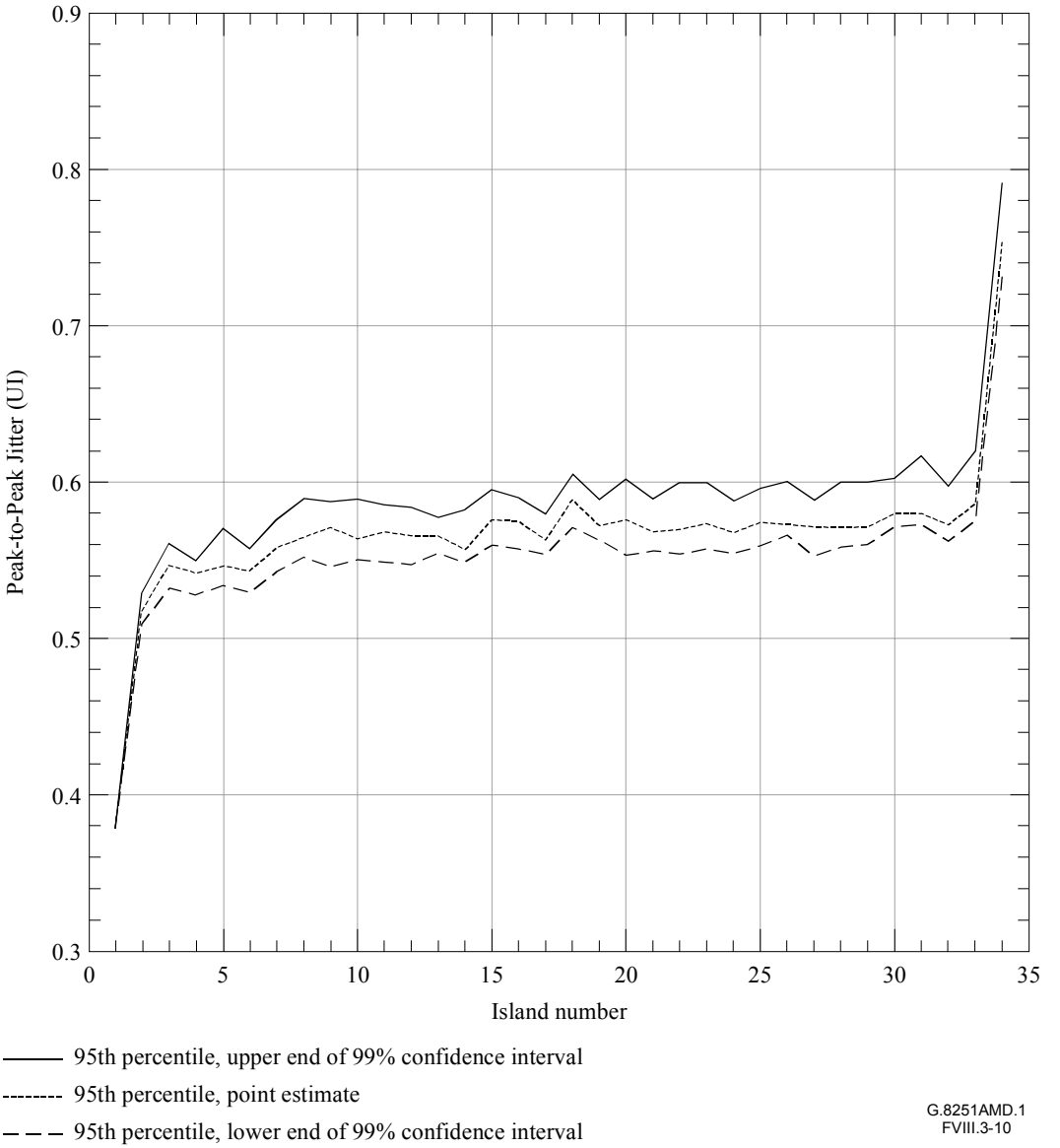
NOTE – ODU1 islands numbered from 1 to 34. 300 Hz desynchronizer at all levels (with 0.1 dB gain peaking). 5 kHz jitter measurement filter. Other assumptions in Tables VIII.1 and VIII.2.

Figure VIII.3-8/G.8251 – CBR2G5 client peak-to-peak wide-band jitter results for Case 8 (Model 2)



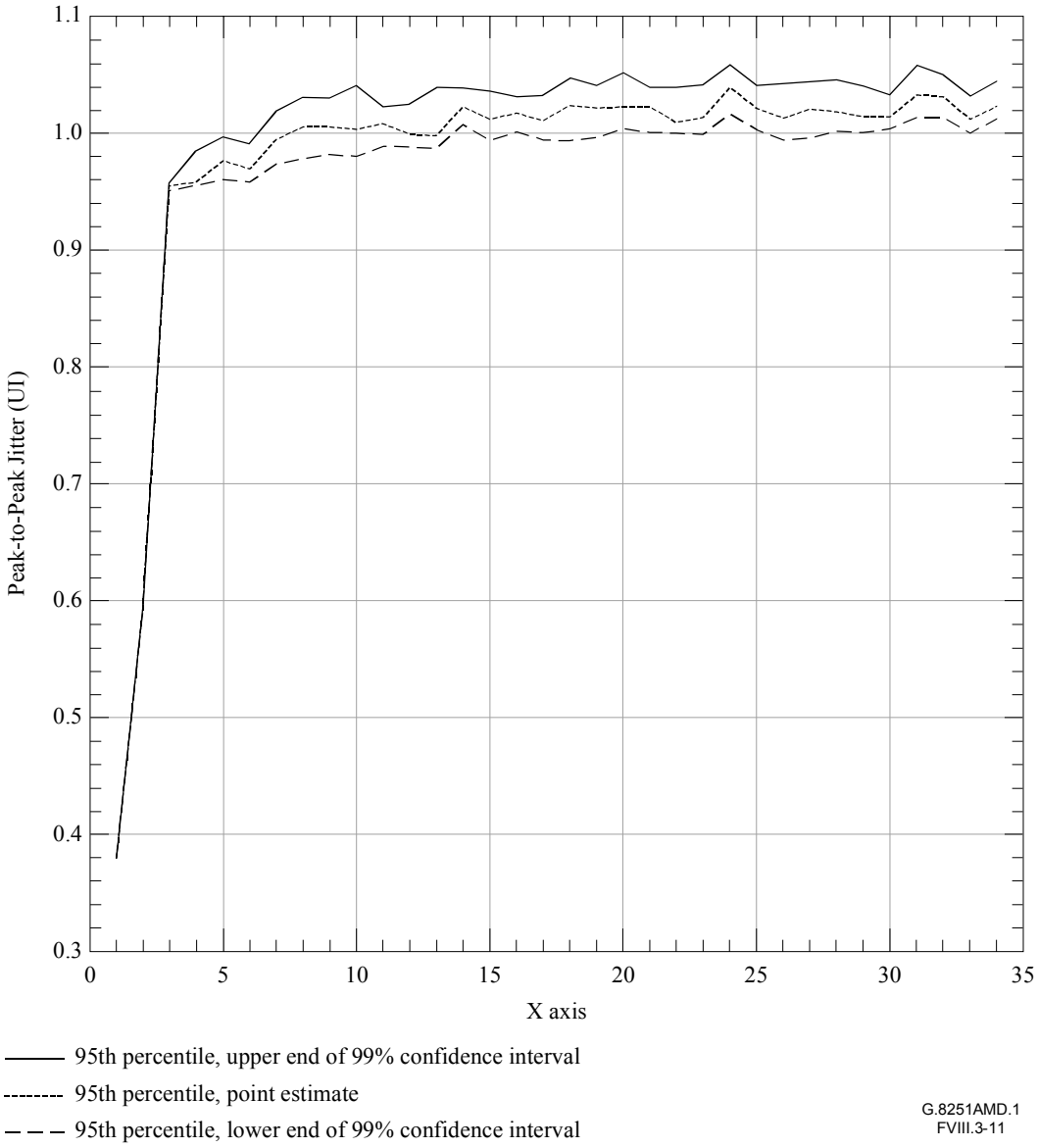
NOTE – ODU1 islands numbered from 1 to 34. 300 Hz desynchronizer at all levels (with 0.1 dB gain peaking). 5 kHz jitter measurement filter. Other assumptions in Tables VIII.1 and VIII.2.

Figure VIII.3-9/G.8251 – CBR2G5 client peak-to-peak wide-band jitter results for Case 9 (Model 1)



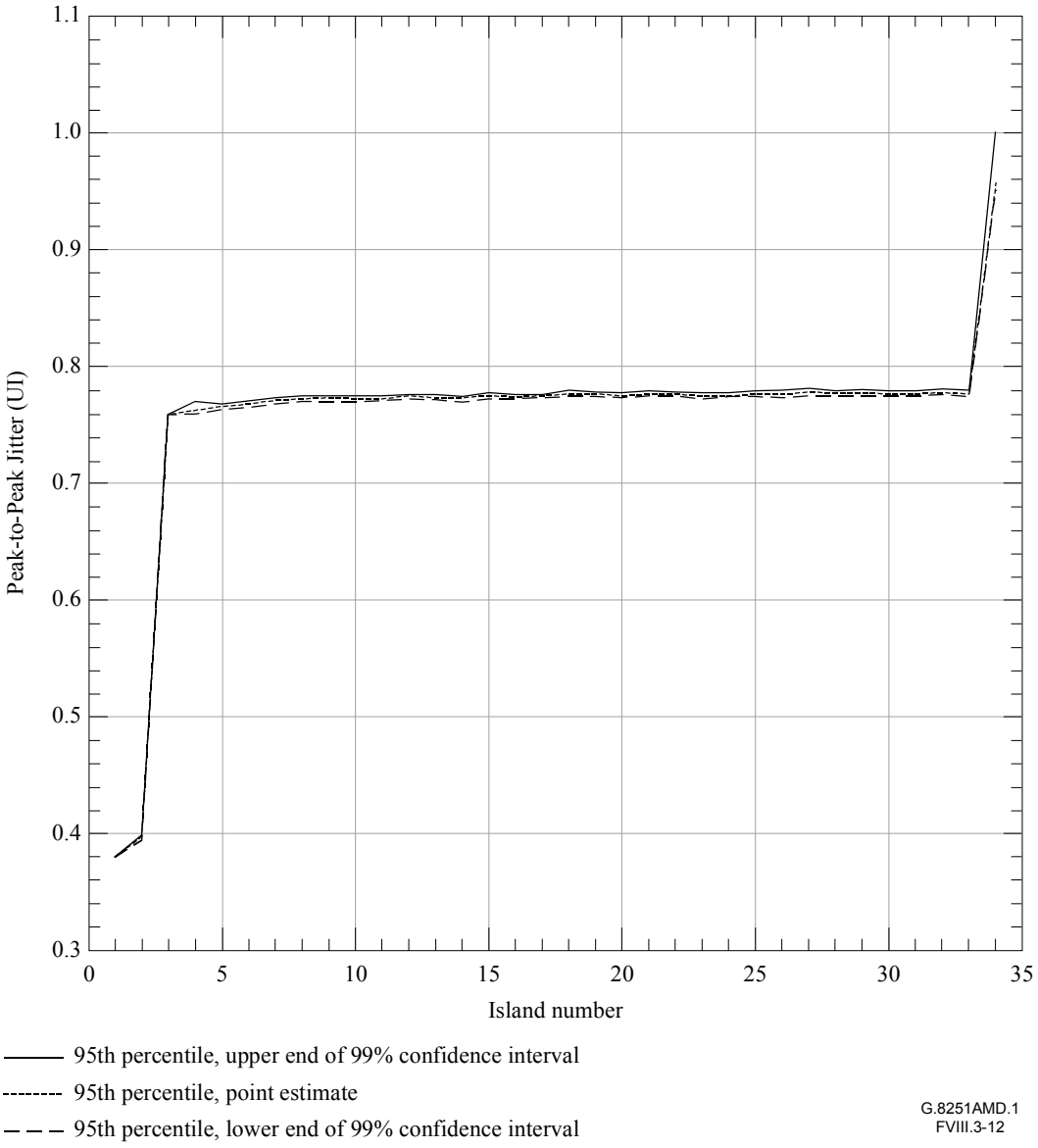
NOTE – ODU1 islands numbered from 1 to 34. 300 Hz desynchronizer at all levels (with 0.1 dB gain peaking). 5 kHz jitter measurement filter. Other assumptions in Tables VIII.1 and VIII.2.

Figure VIII.3-10/G.8251 – CBR2G5 client peak-to-peak wide-band jitter results for Case 10 (Model 2)



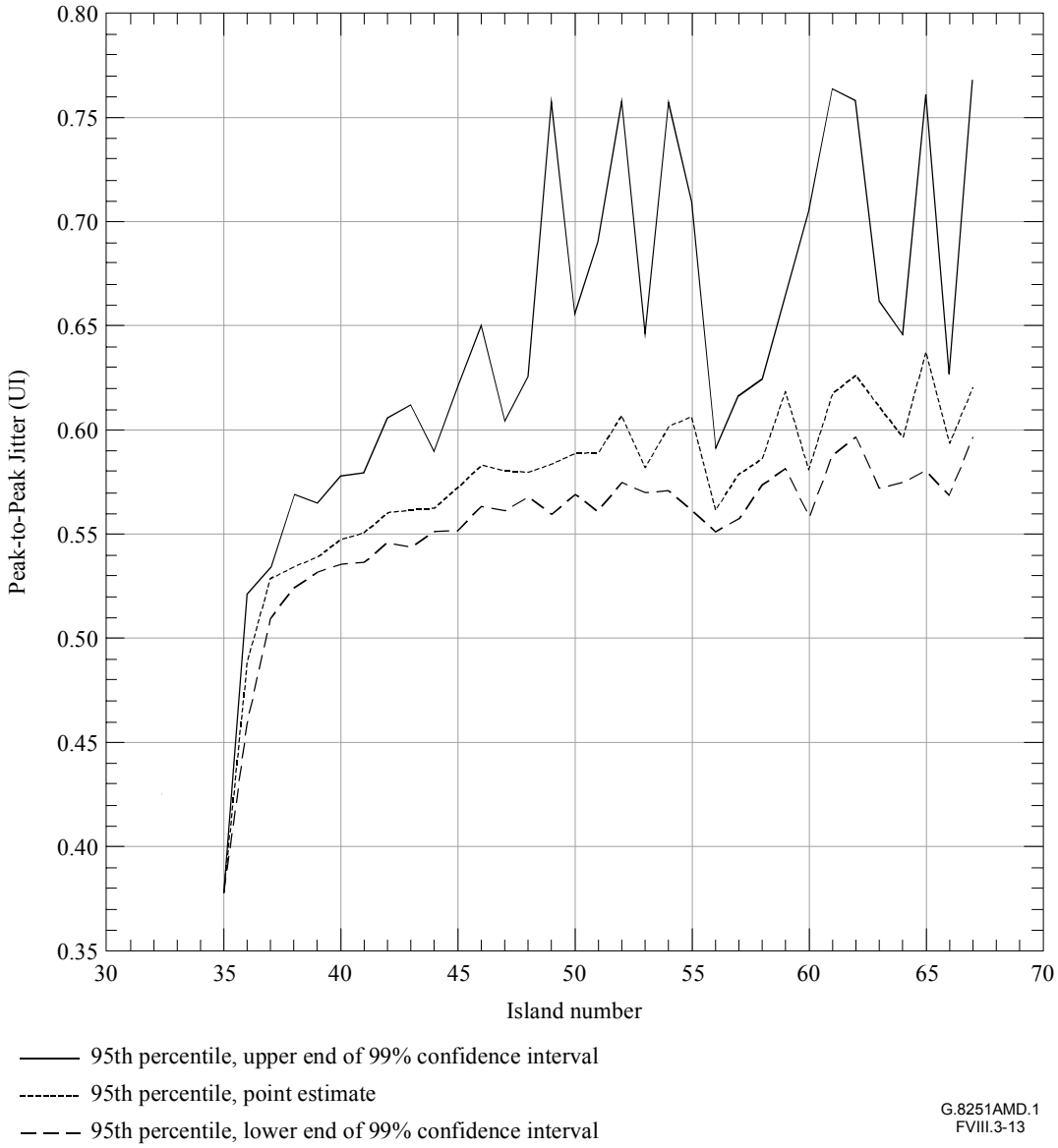
NOTE – ODU1 islands numbered from 1 to 34. 300 Hz desynchronizer at all levels (with 0.1 dB gain peaking). 5 kHz jitter measurement filter. Other assumptions in Tables VIII.1 and VIII.2.

Figure VIII.3-11/G.8251 – CBR2G5 client peak-to-peak wide-band jitter results for Case 11 (Model 1)



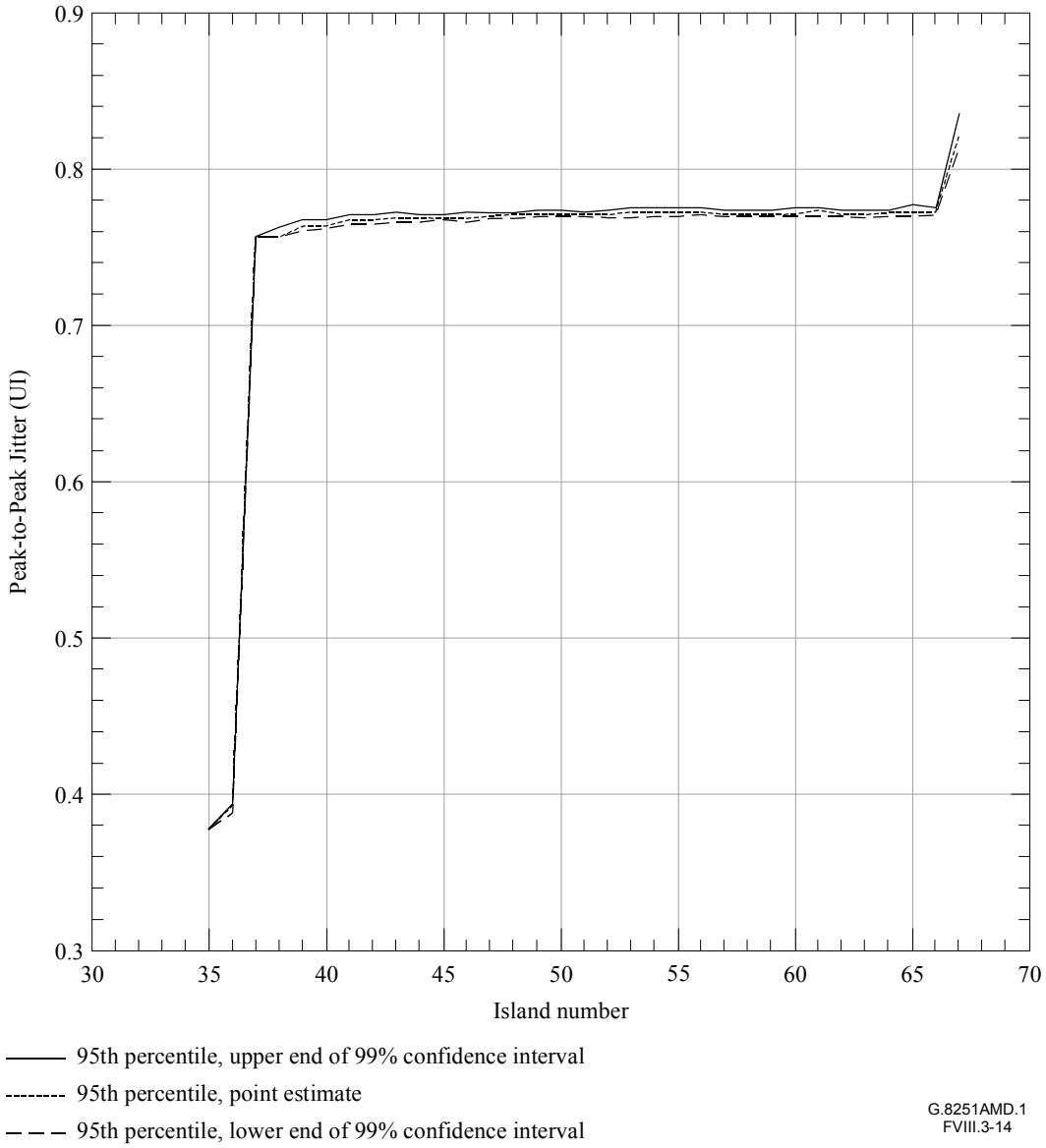
NOTE – ODU1 islands numbered from 1 to 34. 300 Hz desynchronizer at all levels (with 0.1 dB gain peaking). 5 kHz jitter measurement filter. Other assumptions in Tables VIII.1 and VIII.2.

Figure VIII.3-12/G.8251 – CBR2G5 client peak-to-peak wide-band jitter results for Case 12 (Model 2)



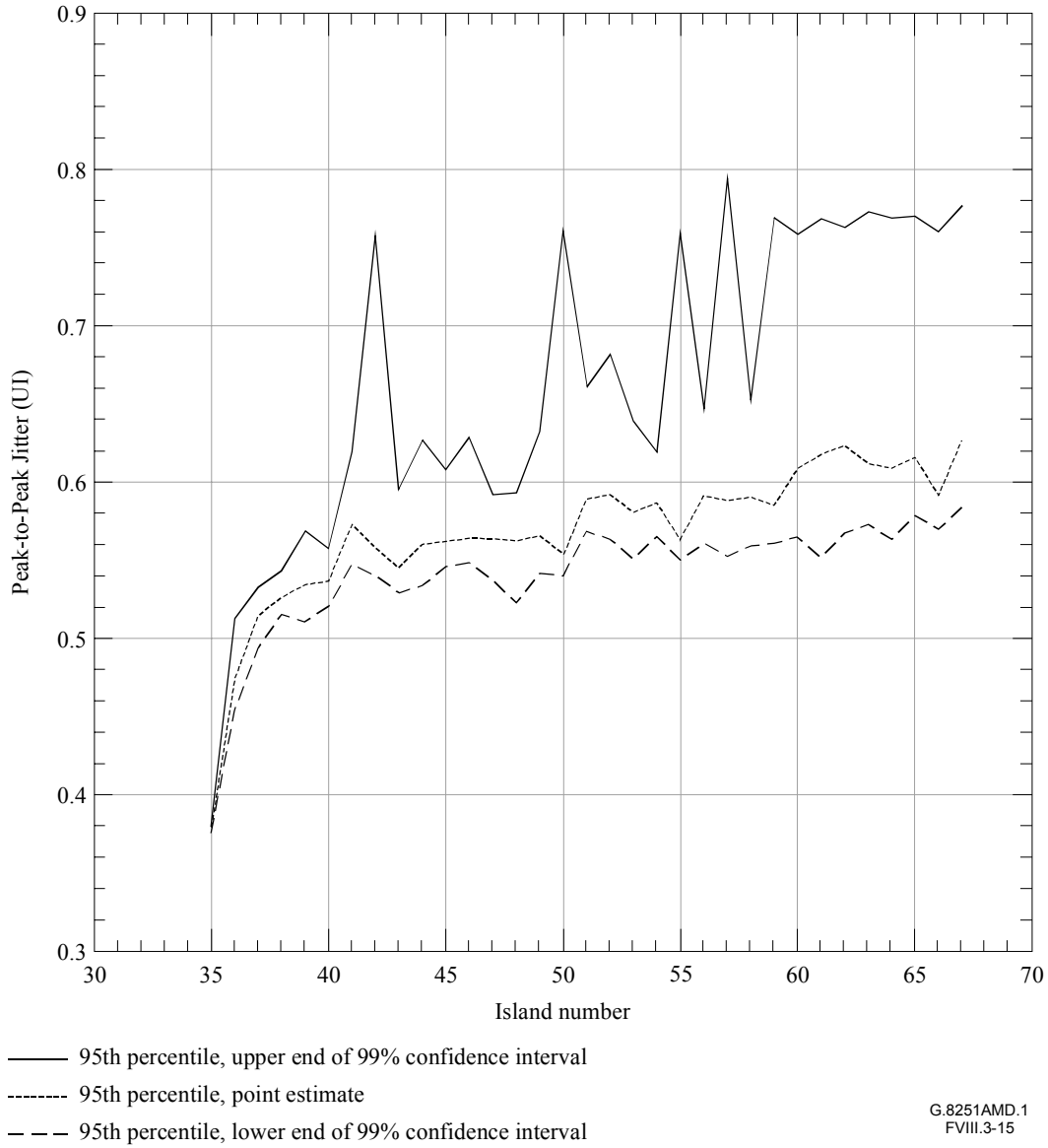
NOTE – ODU2 islands numbered from 35 to 67. 300 Hz desynchronizer at all levels (with 0.1 dB gain peaking). 5 kHz jitter measurement filter. Other assumptions in Tables VIII.1 and VIII.2.

Figure VIII.3-13/G.8251 – ODU1 client peak-to-peak wide-band jitter results for Case 2 (Model 2)



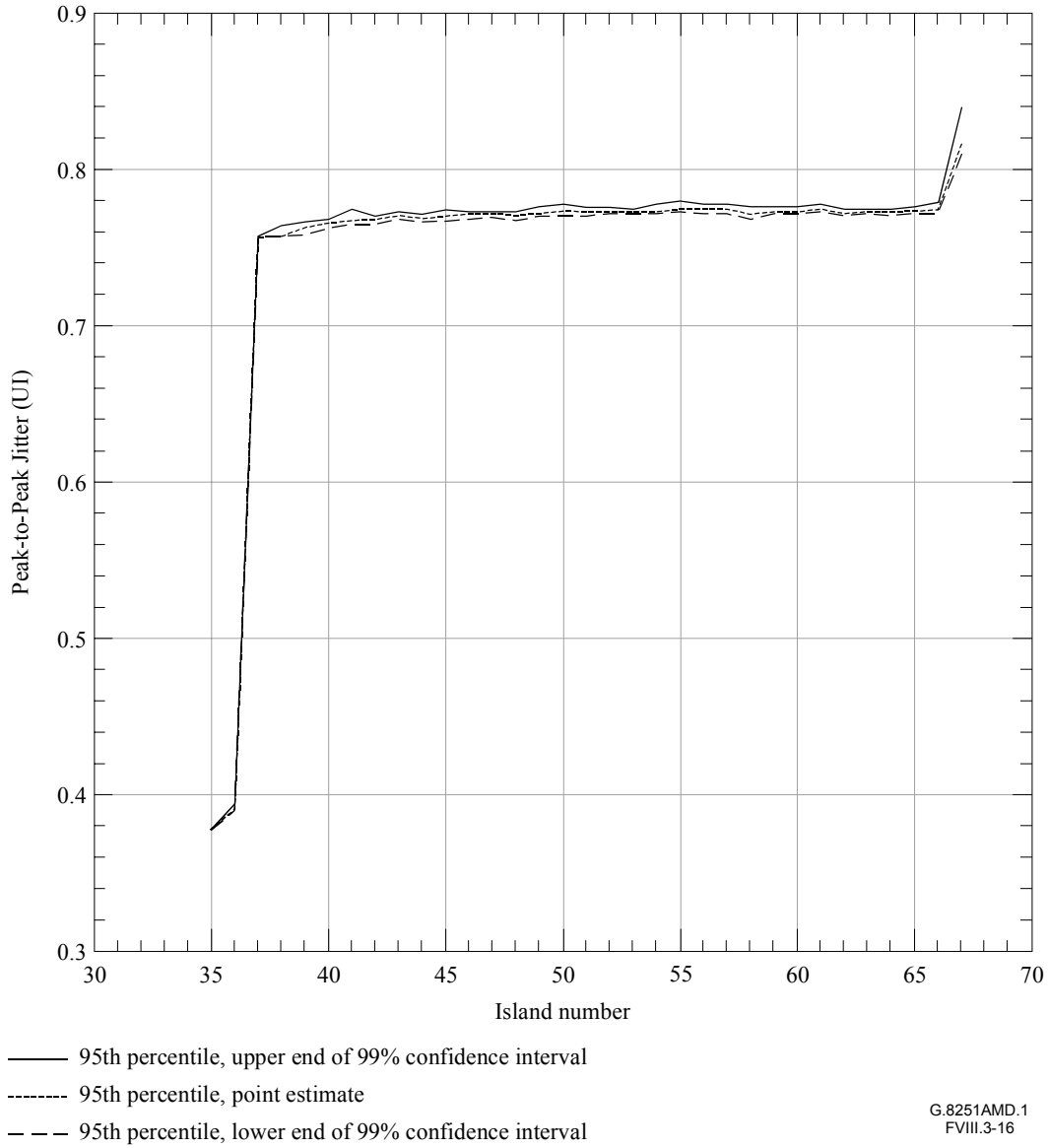
NOTE – ODU2 islands numbered from 35 to 67. 300 Hz desynchronizer at all levels (with 0.1 dB gain peaking). 5 kHz jitter measurement filter. Other assumptions in Tables VIII.1 and VIII.2.

Figure VIII.3-14/G.8251 – ODU1 client peak-to-peak wide-band jitter results for Case 4 (Model 2)



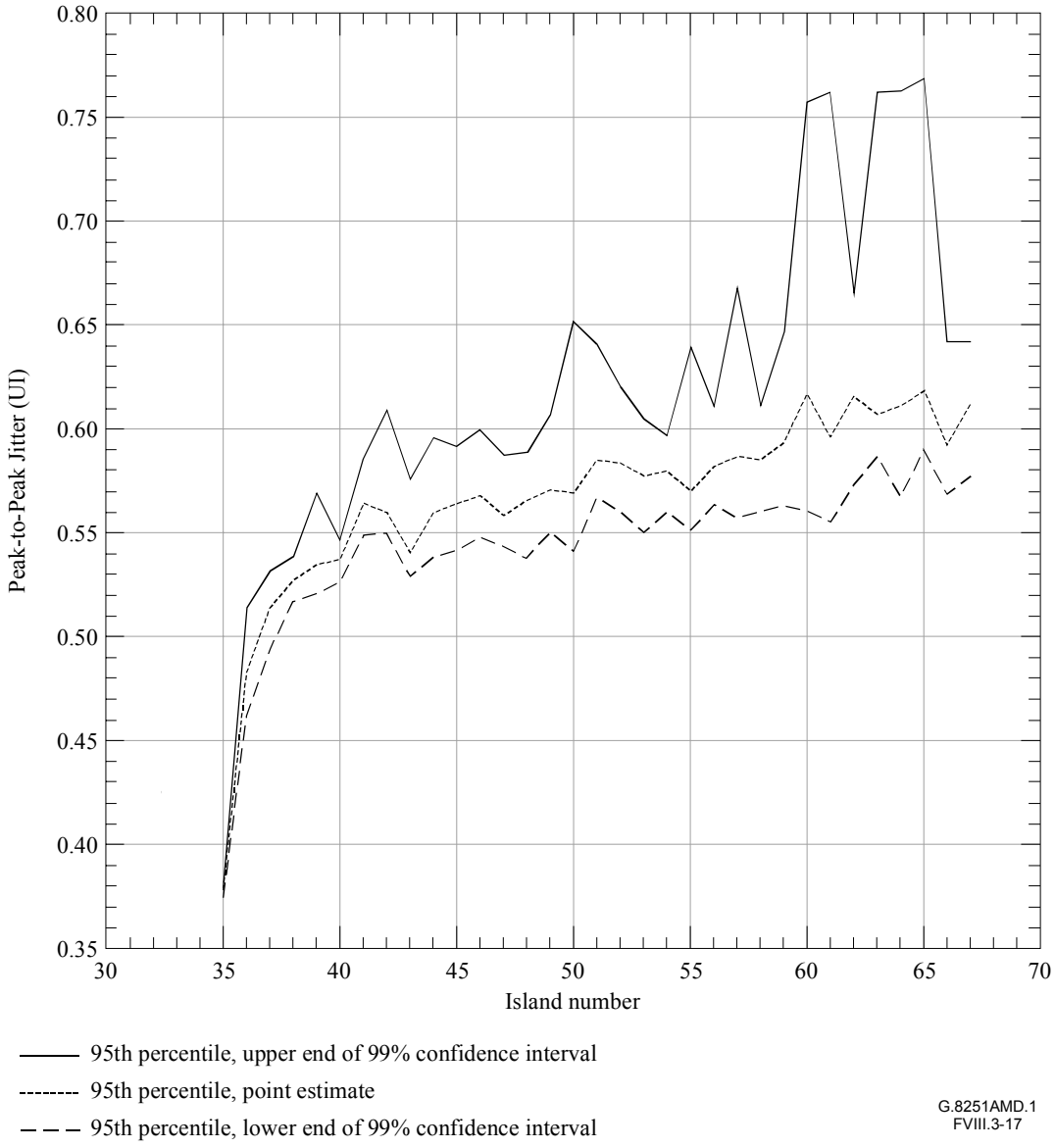
NOTE – ODU2 islands numbered from 35 to 67. 300 Hz desynchronizer at all levels (with 0.1 dB gain peaking). 5 kHz jitter measurement filter. Other assumptions in Tables VIII.1 and VIII.2.

Figure VIII.3-15/G.8251 – ODU1 client peak-to-peak wide-band jitter results for Case 6 (Model 2)



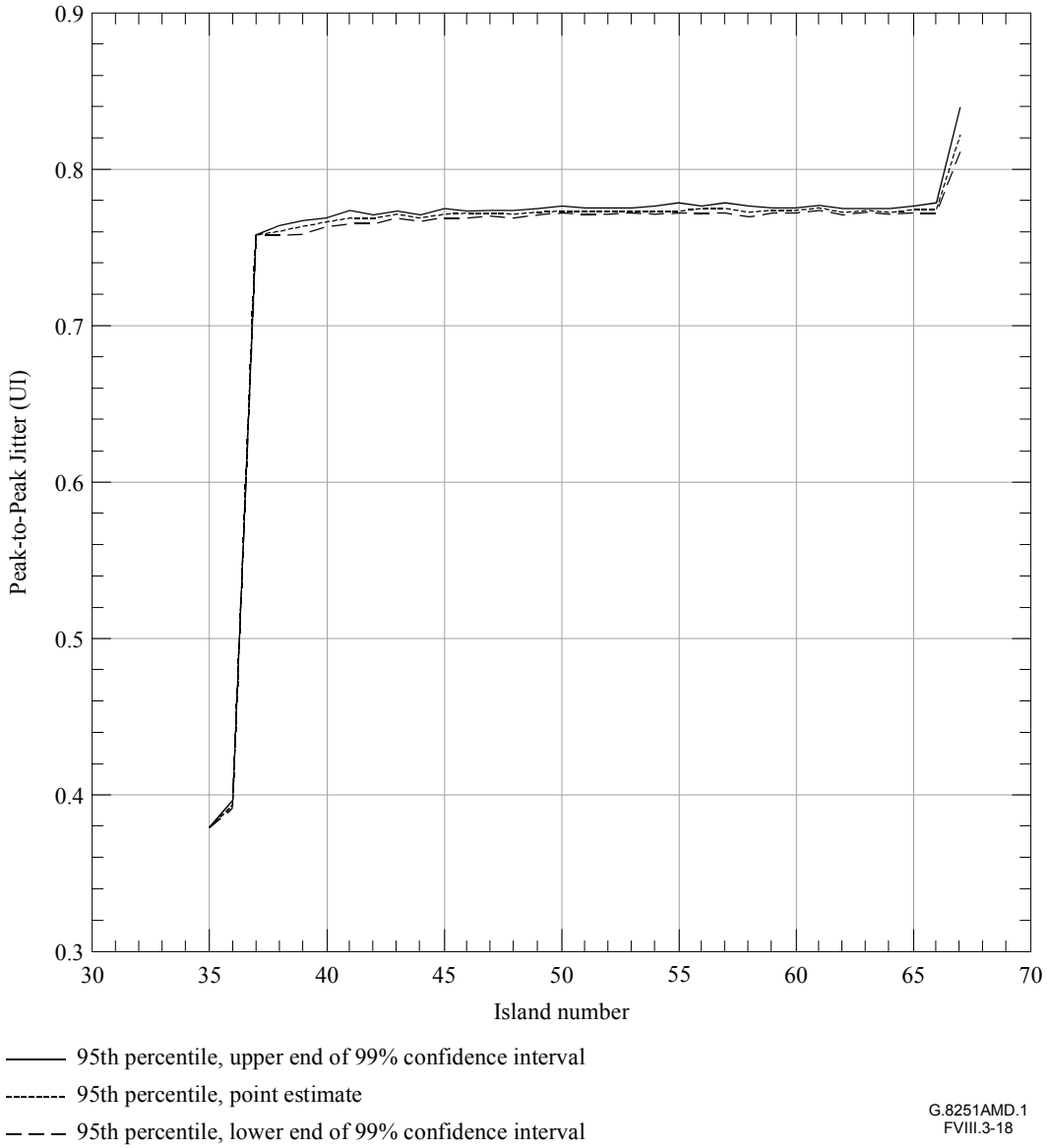
NOTE – ODU2 islands numbered from 35 to 67. 300 Hz desynchronizer at all levels (with 0.1 dB gain peaking). 5 kHz jitter measurement filter. Other assumptions in Tables VIII.1 and VIII.2.

Figure VIII.3-16/G.8251 – ODU1 client peak-to-peak wide-band jitter results for Case 8 (Model 2)



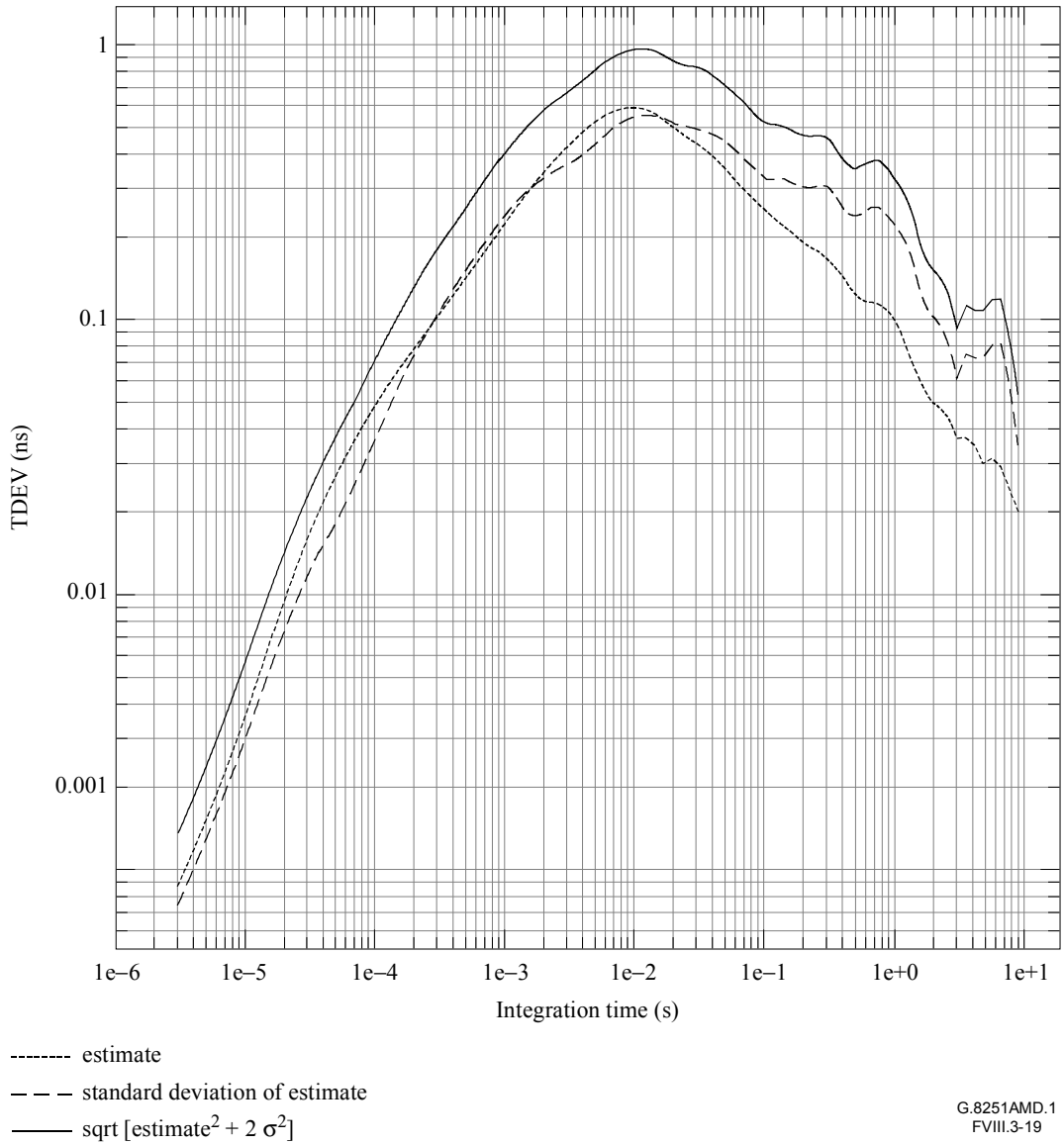
NOTE – ODU2 islands numbered from 35 to 67. 300 Hz desynchronizer at all levels (with 0.1 dB gain peaking). 5 kHz jitter measurement filter. Other assumptions in Tables VIII.1 and VIII.2.

Figure VIII.3-17/G.8251 – ODU1 client peak-to-peak wide-band jitter results for Case 10 (Model 2)



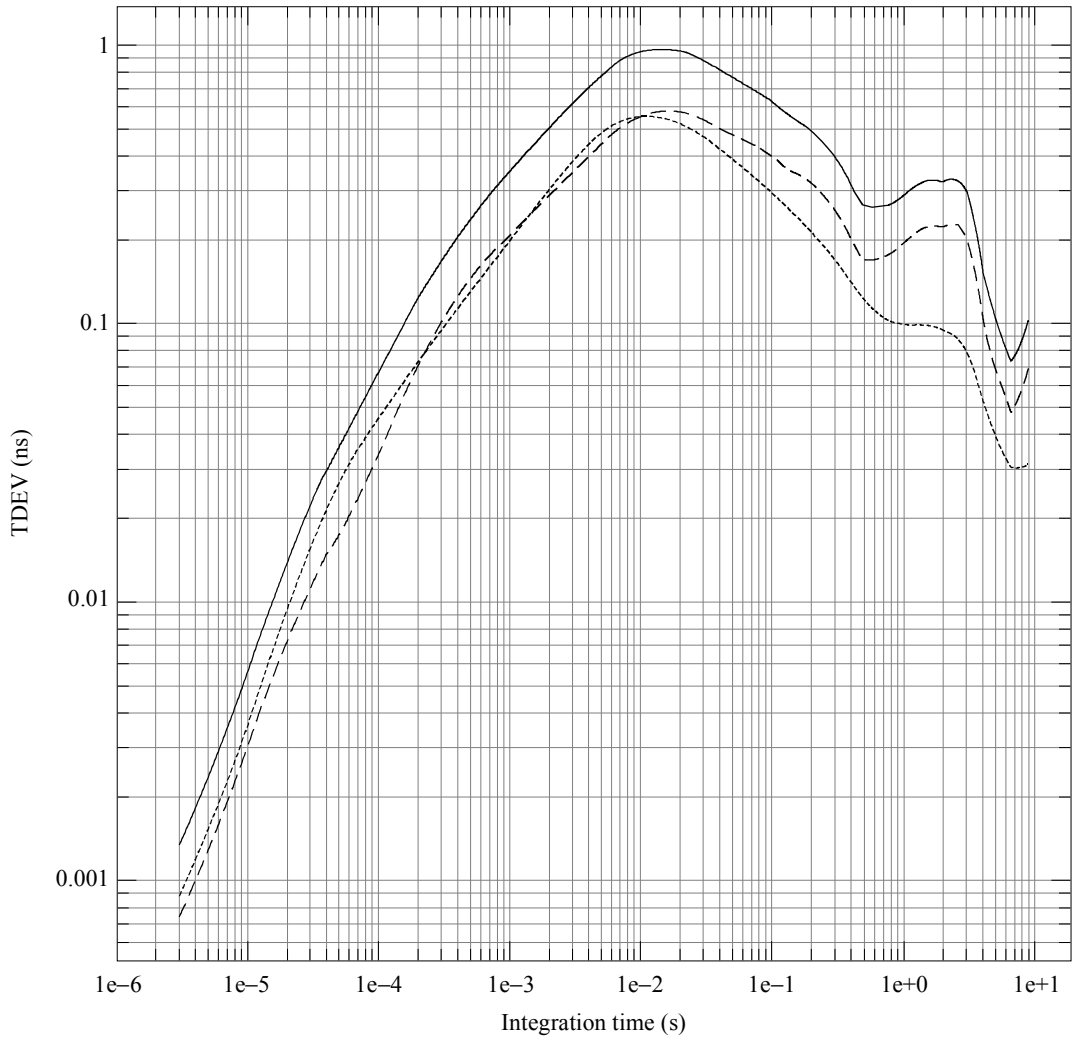
NOTE – ODU2 islands numbered from 35 to 67. 300 Hz desynchronizer at all levels (with 0.1 dB gain peaking). 5 kHz jitter measurement filter. Other assumptions in Tables VIII.1 and VIII.2.

Figure VIII.3-18/G.8251 – ODU1 client peak-to-peak wide-band jitter results for Case 12 (Model 2)



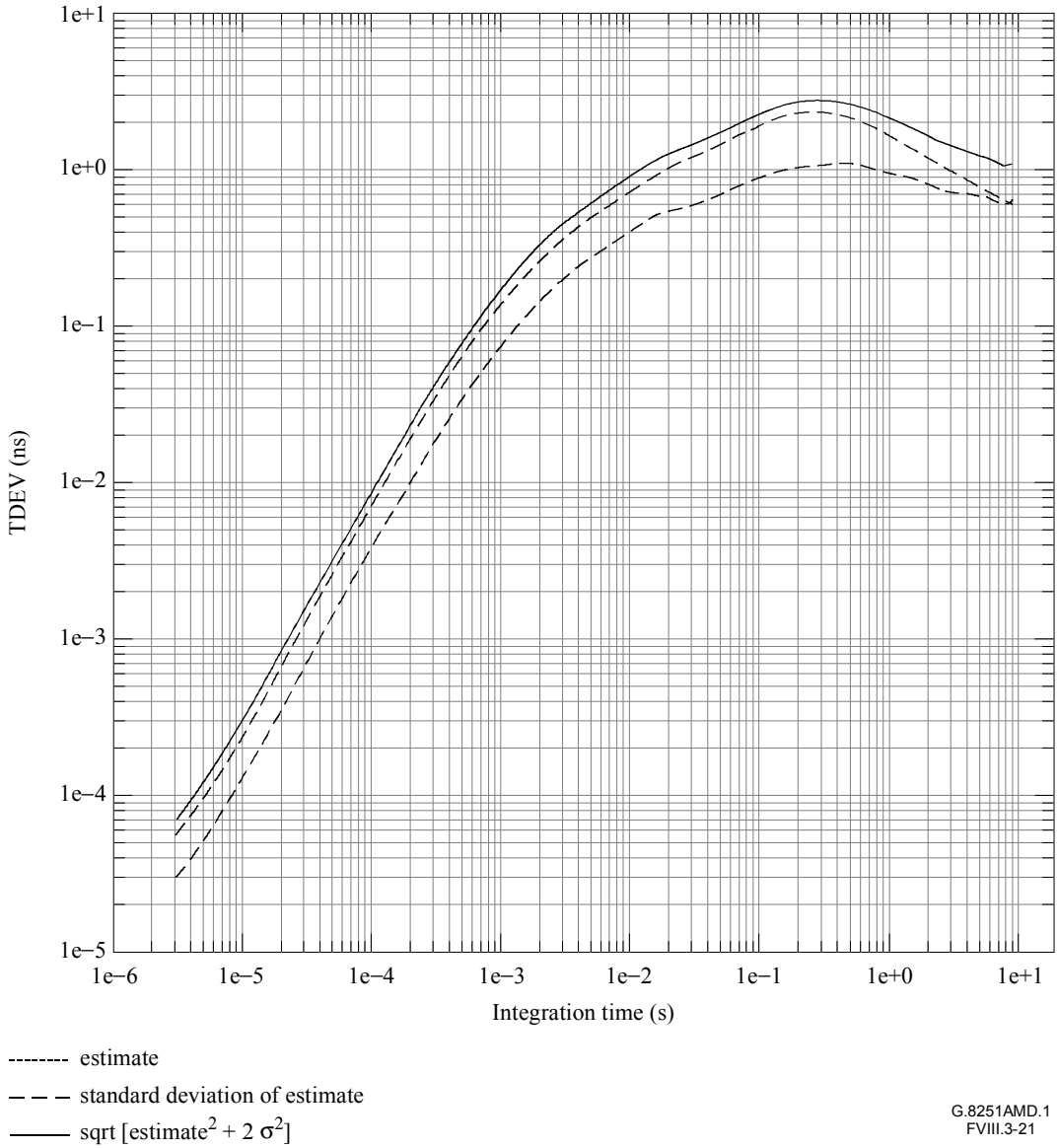
NOTE – ODU1 islands numbered from 1 to 34. 300 Hz desynchronizer at all levels (with 0.1 dB gain peaking). Other assumptions in Tables VIII.1 and VIII.2.

Figure VIII.3-19/G.8251 – CBR2G5 client short-term wander (TDEV) results for Case 1 (Model 1)



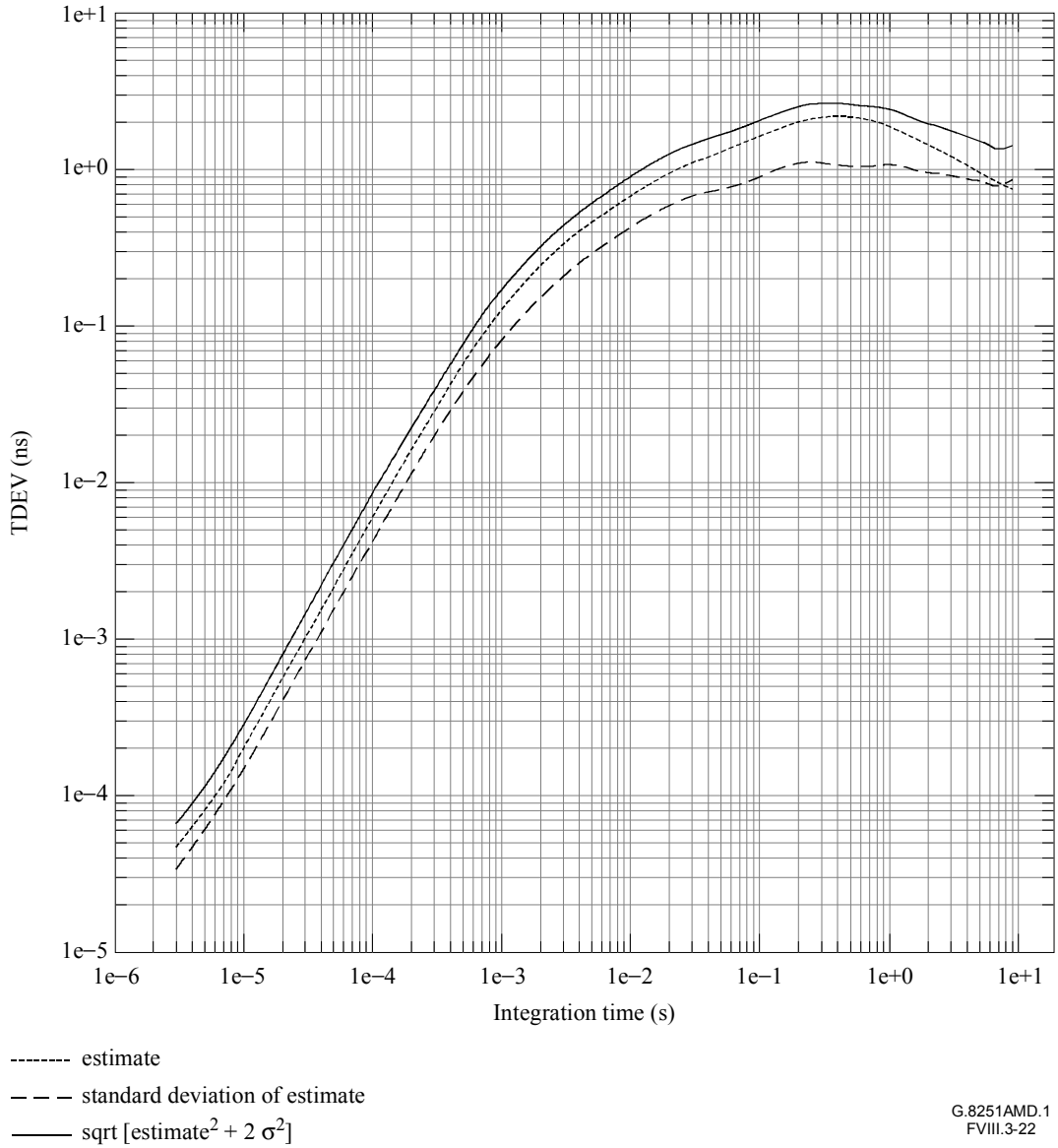
NOTE – ODU1 islands numbered from 1 to 34. 300 Hz desynchronizer at all levels (with 0.1 dB gain peaking). Other assumptions in Tables VIII.1 and VIII.2.

Figure VIII.3-20/G.8251 – CBR2G5 client short-term wander (TDEV) results for Case 2 (Model 2)



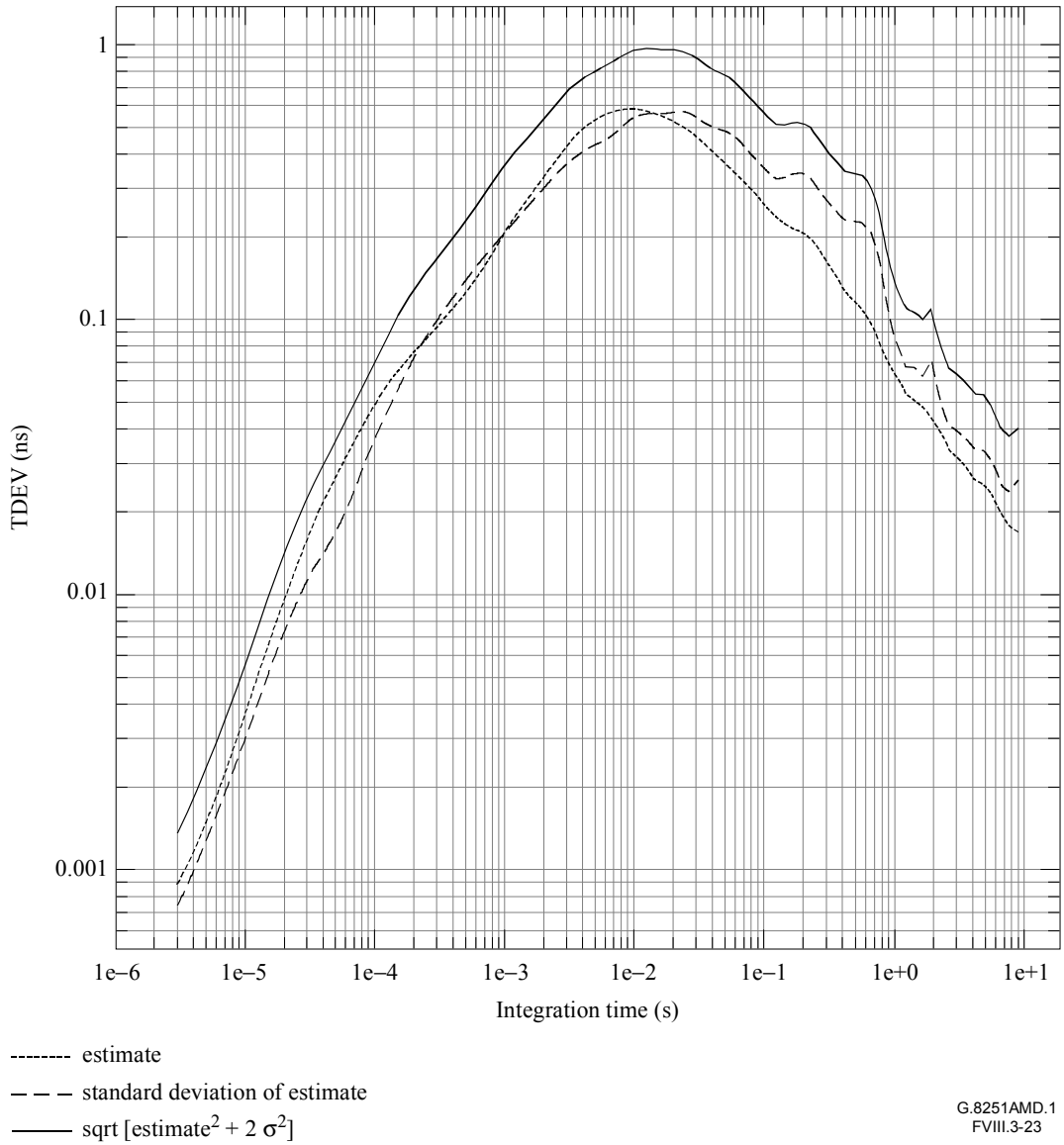
NOTE – ODU1 islands numbered from 1 to 34. 300 Hz desynchronizer at all levels (with 0.1 dB gain peaking). Other assumptions in Tables VIII.1 and VIII.2.

Figure VIII.3-21/G.8251 – CBR2G5 client short-term wander (TDEV) results for Case 3 (Model 1)



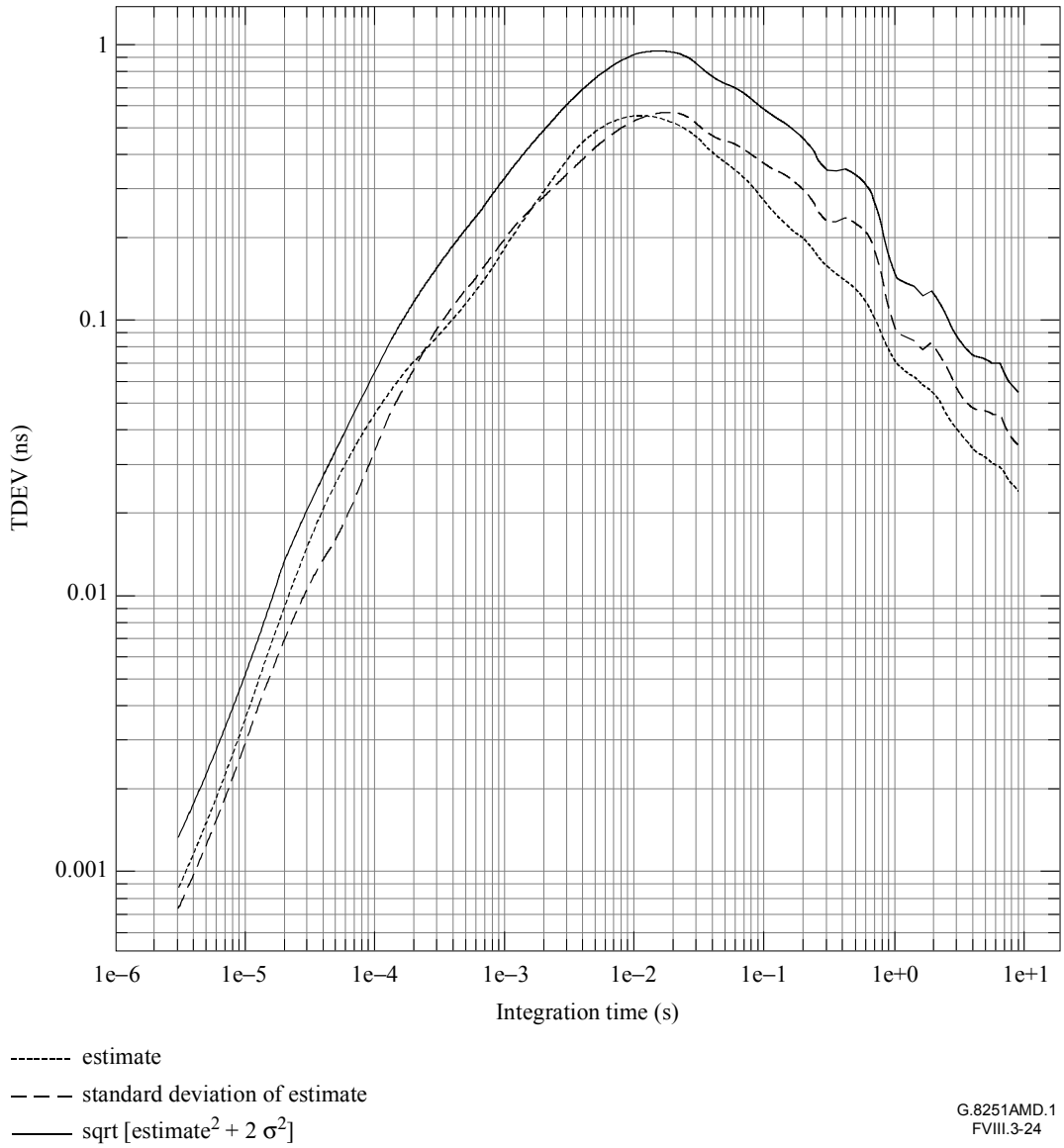
NOTE – ODU1 islands numbered from 1 to 34. 300 Hz desynchronizer at all levels (with 0.1 dB gain peaking). Other assumptions in Tables VIII.1 and VIII.2.

Figure VIII.3-22/G.8251 – CBR2G5 client short-term wander (TDEV) results for Case 4 (Model 2)



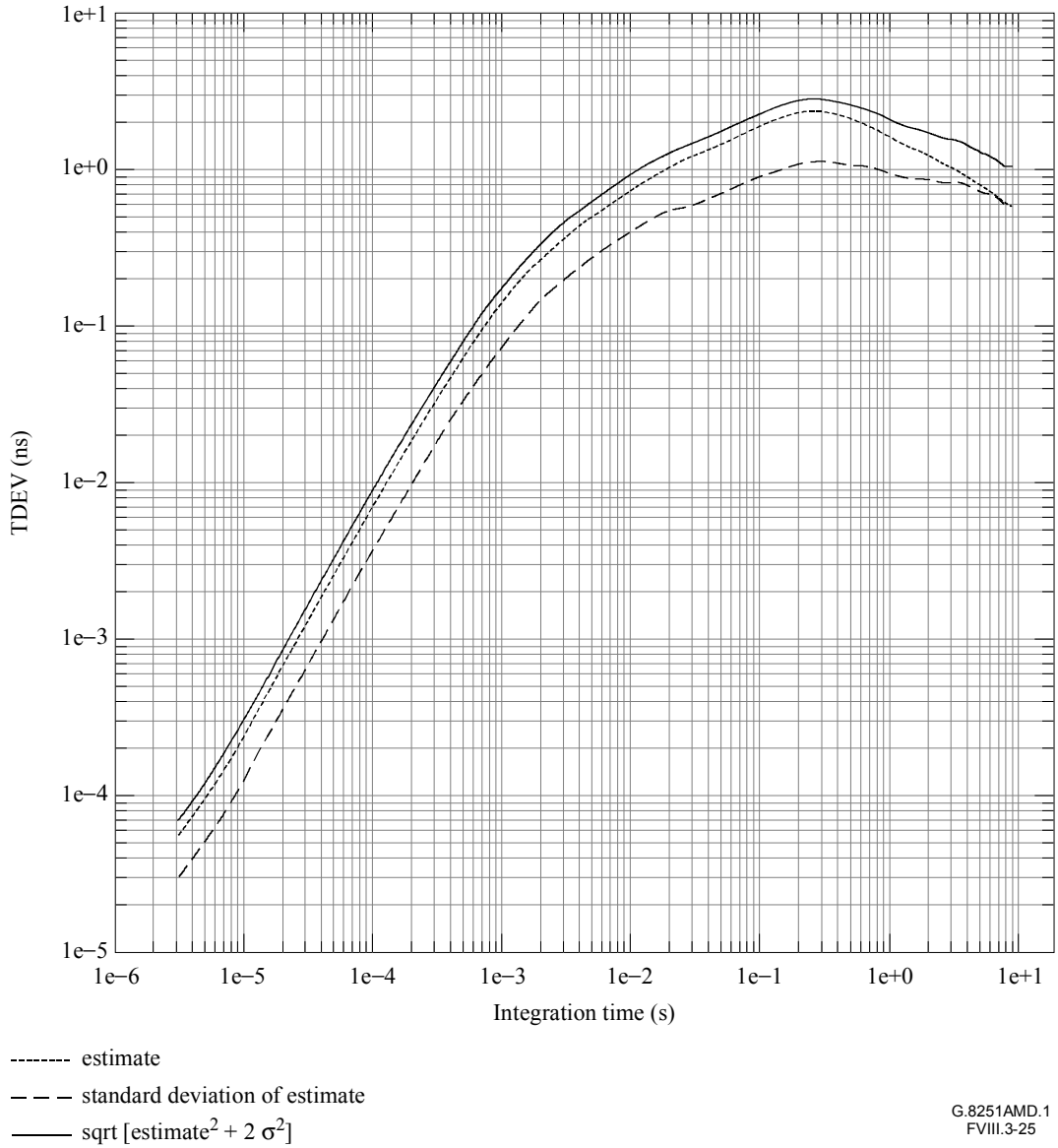
NOTE – ODU1 islands numbered from 1 to 34. 300 Hz desynchronizer at all levels (with 0.1 dB gain peaking). Other assumptions in Tables VIII.1 and VIII.2.

Figure VIII.3-23/G.8251 – CBR2G5 client short-term wander (TDEV) results for Case 5 (Model 1)



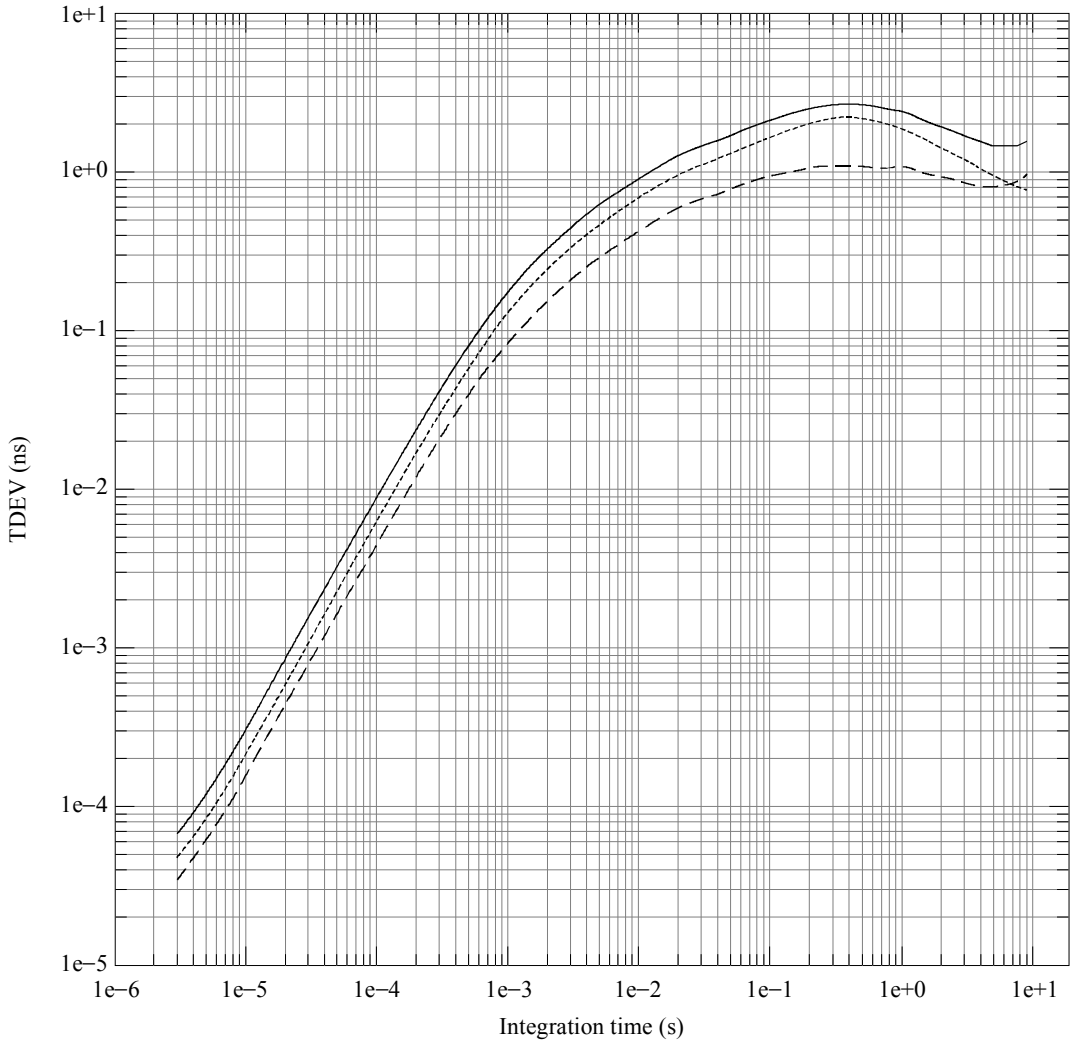
NOTE – ODU1 islands numbered from 1 to 34. 300 Hz desynchronizer at all levels (with 0.1 dB gain peaking). Other assumptions in Tables VIII.1 and VIII.2.

Figure VIII.3-24/G.8251 – CBR2G5 client short-term wander (TDEV) results for Case 6 (Model 2)



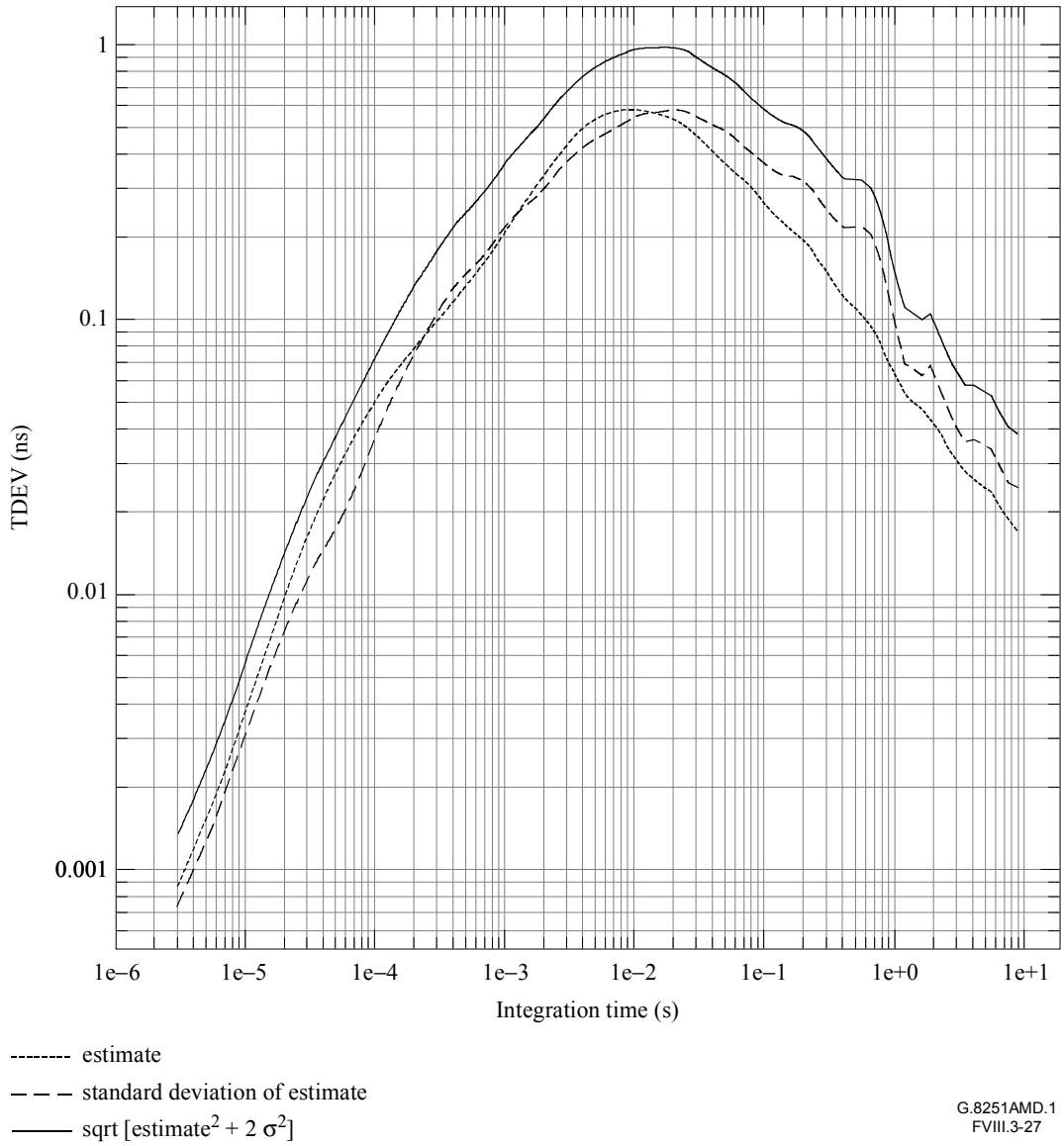
NOTE – ODU1 islands numbered from 1 to 34. 300 Hz desynchronizer at all levels (with 0.1 dB gain peaking). Other assumptions in Tables VIII.1 and VIII.2.

Figure VIII.3-25/G.8251 – CBR2G5 client short-term wander (TDEV) results for Case 7 (Model 1)



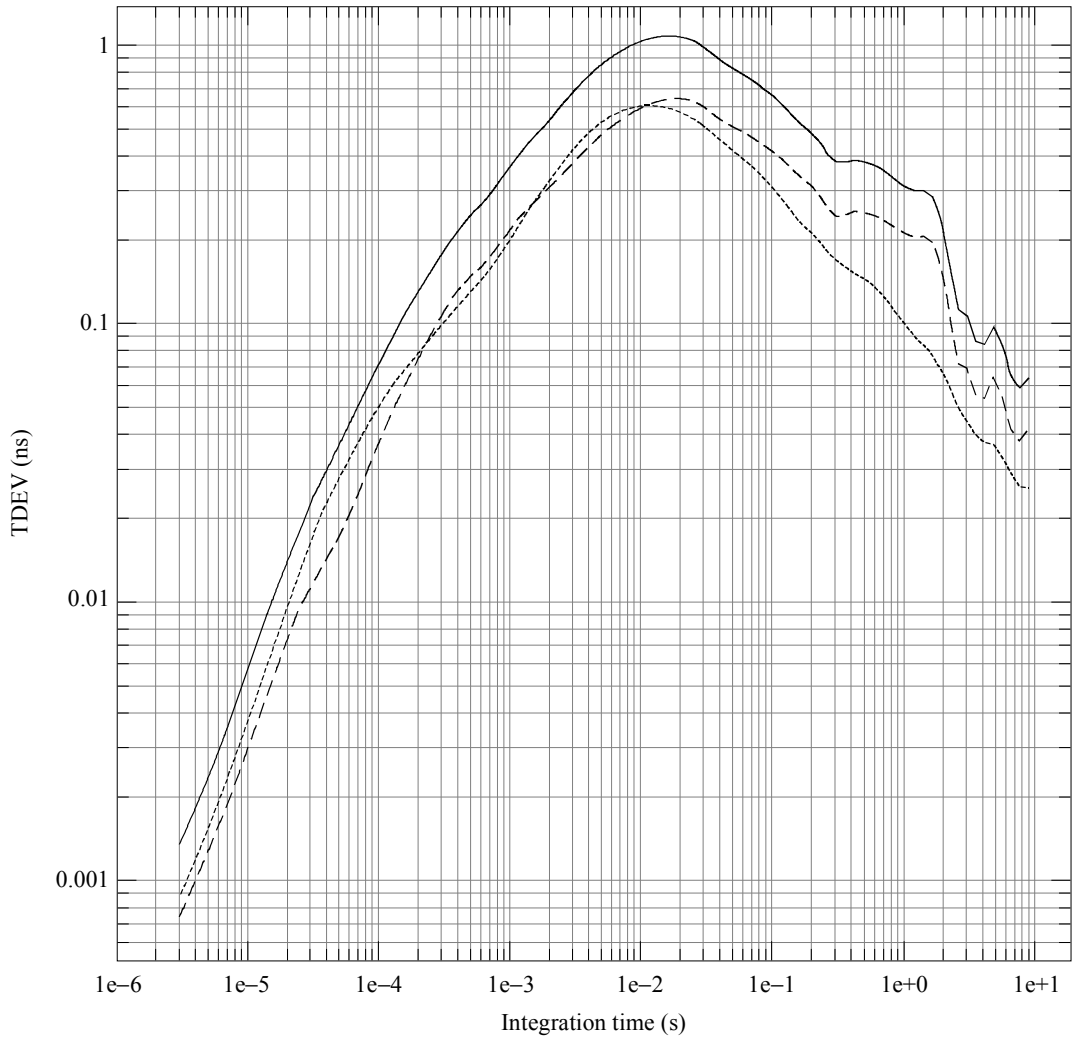
NOTE – ODU1 islands numbered from 1 to 34. 300 Hz desynchronizer at all levels (with 0.1 dB gain peaking). Other assumptions in Tables VIII.1 and VIII.2.

Figure VIII.3-26/G.8251 – CBR2G5 client short-term wander (TDEV) results for Case 8 (Model 2)



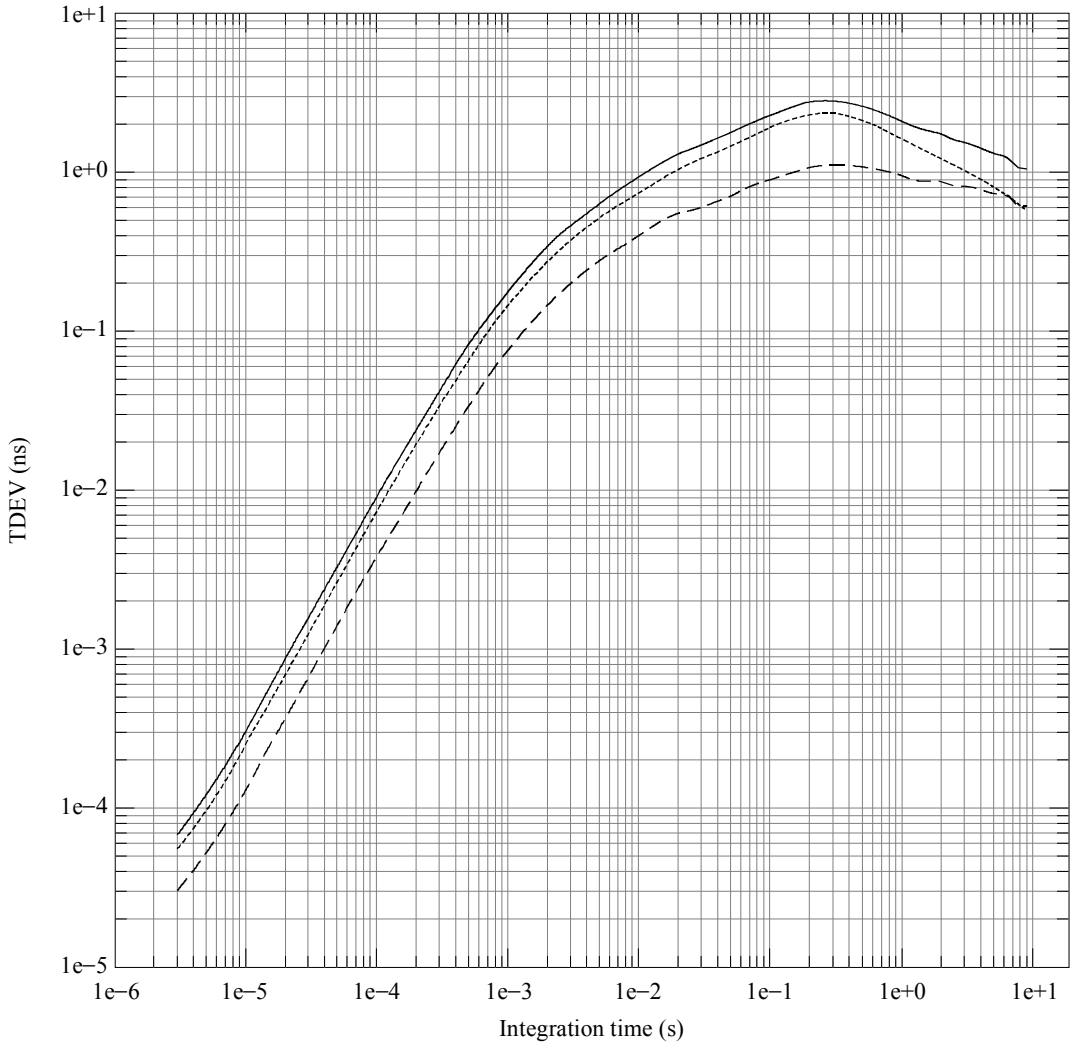
NOTE – ODU1 islands numbered from 1 to 34. 300 Hz desynchronizer at all levels (with 0.1 dB gain peaking). Other assumptions in Tables VIII.1 and VIII.2.

Figure VIII.3-27/G.8251 – CBR2G5 client short-term wander (TDEV) results for Case 9 (Model 1)



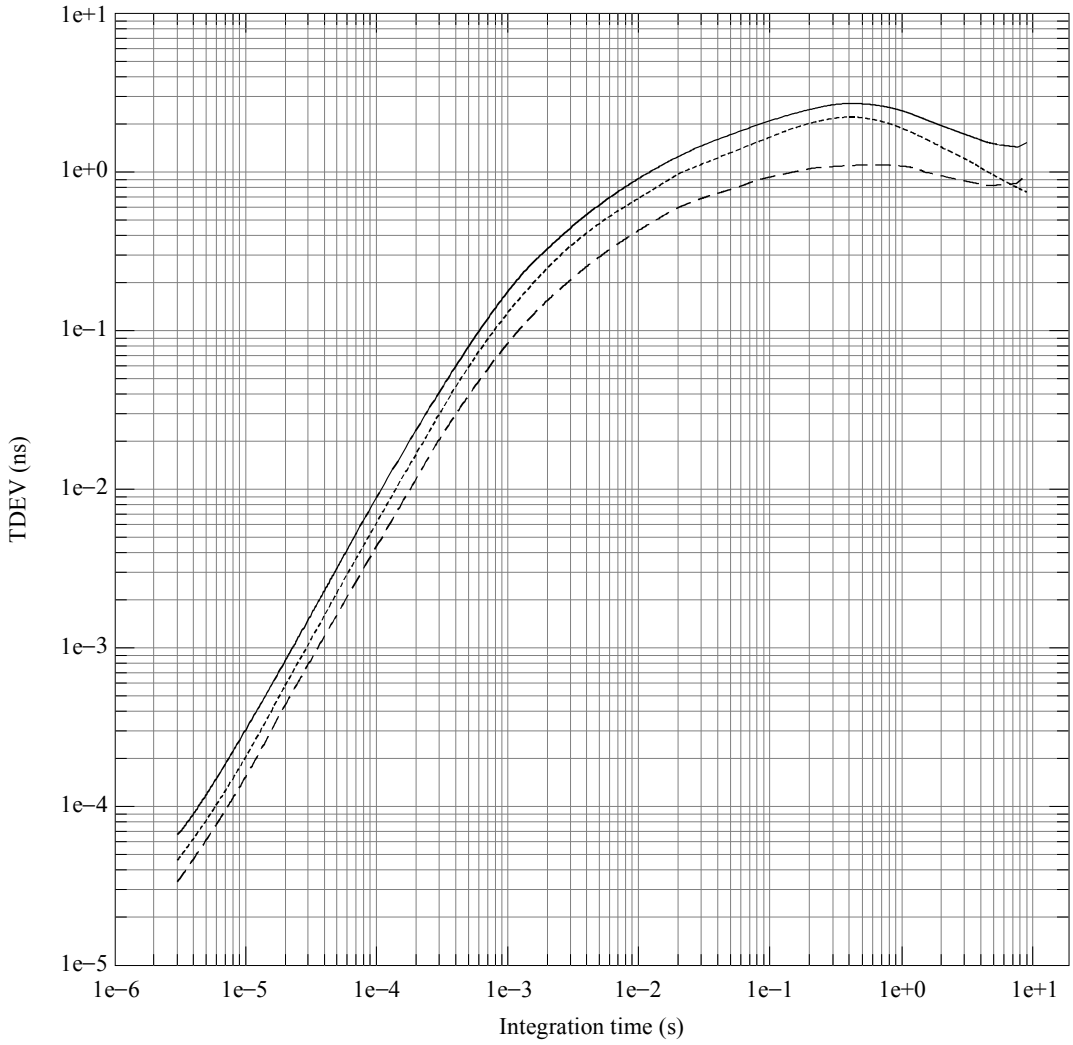
NOTE – ODU1 islands numbered from 1 to 34. 300 Hz desynchronizer at all levels (with 0.1 dB gain peaking). Other assumptions in Tables VIII.1 and VIII.2.

Figure VIII.3-28/G.8251 – CBR2G5 client short-term wander (TDEV) results for Case 10 (Model 2)



NOTE – ODU1 islands numbered from 1 to 34. 300 Hz desynchronizer at all levels (with 0.1 dB gain peaking). Other assumptions in Tables VIII.1 and VIII.2.

Figure VIII.3-29/G.8251 – CBR2G5 client short-term wander (TDEV) results for Case 11 (Model 1)



NOTE – ODU1 islands numbered from 1 to 34. 300 Hz desynchronizer at all levels (with 0.1 dB gain peaking). Other assumptions in Tables VIII.1 and VIII.2.

Figure VIII.3-30/G.8251 – CBR2G5 client short-term wander (TDEV) results for Case 12 (Model 2)

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