International Telecommunication Union

ITU-T

TELECOMMUNICATION
STANDARDIZATION SECTOR
OF ITU

G.783

Amendment 2
(03/2010)

SERIES G: TRANSMISSION SYSTEMS AND MEDIA, DIGITAL SYSTEMS AND NETWORKS

Digital terminal equipments – Principal characteristics of multiplexing equipment for the synchronous digital hierarchy

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Characteristics of synchronous digital hierarchy (SDH) equipment functional blocks

Amendment 2: Support for optical modules transporting 40 Gigabit/s signals via a multilane interface

Recommendation ITU-T G.783 (2006) – Amendment 2

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Recommendation ITU-T G.783

Characteristics of synchronous digital hierarchy (SDH) equipment functional blocks

Amendment 2

Support for optical modules transporting 40 Gigabit/s signals via a multilane interface

Summary

Amendment 2 to Recommendation ITU-T G.783 adds to the Recommendation the optical multilane interface of four optical lanes for STM-256.

History

Edition	Recommendation	Approval	Study Group
1.0	ITU-T G.783	1990-12-14	XV
2.0	ITU-T G.783	1994-01-20	15
3.0	ITU-T G.783	1997-04-08	15
4.0	ITU-T G.783	2000-10-06	15
4.1	ITU-T G.783 (2000) Cor. 1	2001-03-15	15
4.2	ITU-T G.783 (2000) Amend. 1	2002-06-13	15
4.3	ITU-T G.783 (2000) Cor. 2	2003-03-16	15
5.0	ITU-T G.783	2004-02-06	15
5.1	ITU-T G.783 (2004) Cor. 1	2004-06-13	15
5.2	ITU-T G.783 (2004) Amend. 1	2005-07-14	15
6.0	ITU-T G.783	2006-03-29	15
6.1	ITU-T G.783 (2006) Amend. 1	2008-05-22	15
6.2	ITU-T G.783 (2006) Amend. 2	2010-03-09	15

FOREWORD

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Recommendation ITU-T G.783

Characteristics of synchronous digital hierarchy (SDH) equipment functional blocks

Amendment 2

Support for optical modules transporting 40 Gigabit/s signals via a multilane interface

1) Scope

This amendment contains material to be added to Recommendation ITU-T G.783, for the support of optical modules for the transport of 40 Gigabit/s signals implementing a multilane interface, consisting of four optical 10 Gigabit/s signals.

2) Changes to Recommendation ITU-T G.783

The following clauses contain changes to be made to Rec. ITU-T G.783.

2.1) Clause 2, References

a) *Add the following references to clause 2:*

[ITU-T G.695] Recommendation ITU-T G.695 (2009), *Optical interfaces for coarse wavelength division multiplexing applications*.

[ITU-T G.709] Recommendation ITU-T G.709/Y.1331 (2009), *Interfaces for the optical transport network (OTN)*.

b) *Update ITU-T G.707/Y.1322 as follows:*

[ITU-T G.707] Recommendation ITU-T G.707/Y.1322 (2007), *Network node interface for the synchronous digital hierarchy (SDH)*.

2.2) Clause 4, Abbreviations

Add the following abbreviations to clause 4:

OSMn.m Optical Section Multilane, n = 256, m = 4

STL-n.m Synchronous Transport Lane of STM-n (n = 256) mapped over m (m = 4) parallel lanes (see [ITU-T G.707]).

2.3) New clauses 6.2.5.6 and 6.2.5.7

Add the following clauses subsequent to clause 6.2.5.5:

6.2.5.6 STL loss of lane alignment defect (dLOL)

STL-n.m dLOL is generated for interfaces of OSMn.m based on the state of the lane alignment process of the multilane STL-n.m signals defined in clause 8.2.7.

If the multilane alignment process is in the out-of-alignment (OLA) state for 3 ms, dLOL shall be declared. To provide for the case of intermittent OLA, the integrating timer shall not be reset to zero until an in-lane alignment (ILA) condition persists continuously for 3 ms. dLOL shall be cleared when the ILA state persists continuously for 3 ms.

6.2.5.7 Loss of frame defect of STL (dLOFSTL)

The lost of frame defect of a lane on a multilane signal dLOFSTL is generated based on the state of the frame alignment process defined in clause 8.2.6.

If the frame alignment process is in the out-of-frame (OOF) state for 3 ms, dLOFSTL shall be declared. To provide for the case of intermittent OOFs, the integrating timer shall not be reset to zero until an in-frame (IF) condition persists continuously for 3 ms. dLOFSTL shall be cleared when the IF state persists continuously for 3 ms.

2.4) New clauses 8.2.6 and 8.2.7

Add the following clauses subsequent to clause 8.2.5.2:

8.2.6 STL-256.4 frame alignment of STM-256 multilane interface

The frame alignment shall be found by searching for the 16 A1 followed by 15 A2 bytes (see Annex I of [ITU-T G.707]) contained in each lane of the STL-256.4 signal. The framing pattern searched for may be a subset of the A1 and A2 bytes contained on the STL-256.4 signal. The frame signal shall be continuously checked with the presumed frame start position for the alignment. If in the in-frame state (IF), the maximum out-of-frame (OOF) detection time shall be 625 µs for a random unframed signal. The algorithm used to check the alignment shall be such that, under normal conditions, a 10^{-3} (Poisson type) error ratio will not cause a false OOF more than once per 6 minutes. If in the OOF state, the maximum frame alignment time shall be 250 µs for an error-free signal with no emulated framing patterns. The algorithm used to recover from the OOF state shall be such that the probability for false frame recovery with a random unframed signal shall be no more than 10^{-5} per 250 µs time interval.

8.2.7 STL-256.4 lane alignment of STM-256 multilane interface

The STL-256.4 lane alignment process is used in re-establishing alignment of the lanes of the STM-256 multilane signal. The process has two sub-processes:

– STL-256.4 logical lane marker recovery (per lane);
– STL-256.4 multi-lane alignment.

The bytes of the STM-256 signal are distributed to the lanes in 16-byte increments.

The lane alignment signal per-lane is encoded in the byte following the 15th A2 byte.

An STL-256.4 logical lane marker recovery process is present per logical lane to recover the logical lane marker value and frame alignment number. A new value of the STL-256.4 logical lane marker and frame alignment number are accepted when in five consecutive 155'520-byte periods the same value is present in bits 7-8 of the byte following the 15th A2 byte, and consecutive incrementing values are present in bits 1-6 of the byte following the 15th A2 byte. When these conditions are met, the recovery process will enter the in-recovery (IR) state. In the IR state, recovery will be lost and the out-of-recovery (OOR) state be entered, when in each of five consecutive 155'520-byte periods a value is received in bits 7-8 that is not the same as the accepted logical lane marker value, or the value received in bits 1-6 does not match a locally incremented frame alignment number.

The STL-256.4 multi-lane alignment process has two states: out-of-lane alignment (OLA) and in-lane alignment (ILA).

The lane data for each lane is written into an elastic store, together with an indication of the start of frame boundary and frame alignment number. If all lanes are in the IR state and have unique lane marker values, and data is present in the elastic store for realignment with respect to creating consistent data of consecutive STM-256 frames with respect to the lane alignment signal, the ILA state shall be entered. In the case that lane identification for all lanes is not detected in a consistent way, the OLA state shall be entered.

2.5) New clause 9.2.3

Add the following clauses subsequent to clause 9.2.2.2:

9.2.3 OSM256.4_TT trail termination function

The OSM256.4_TT functions are responsible for the end-to-end termination of the OSM256.4 trail. Figure 9b shows the combination of the unidirectional sink and source functions to form a bidirectional function.

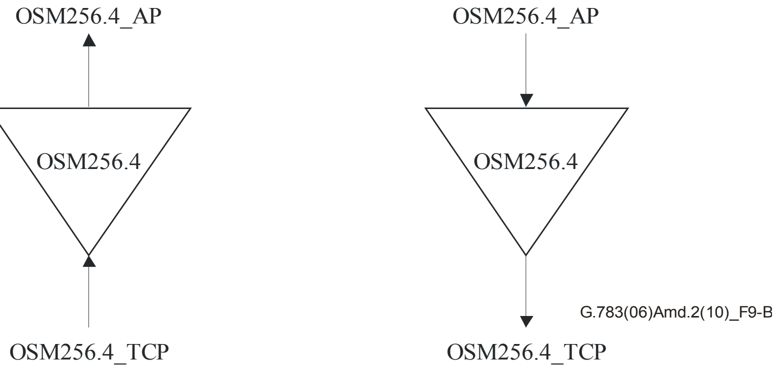

Figure 9b – OSM256.4_TT

9.2.3.1 OSM256.4_TT trail termination source function

The information flow and processing of the OSM256.4_TT_So function is defined with reference to Figure 9c.

The OSM256.4_TT_So function conditions the data for transmission over the optical medium using the multilane format. For this, the OSM256.4_TT_So generates the STL-256.4 signal within the physical specifications of [ITU-T G.695].

Symbol

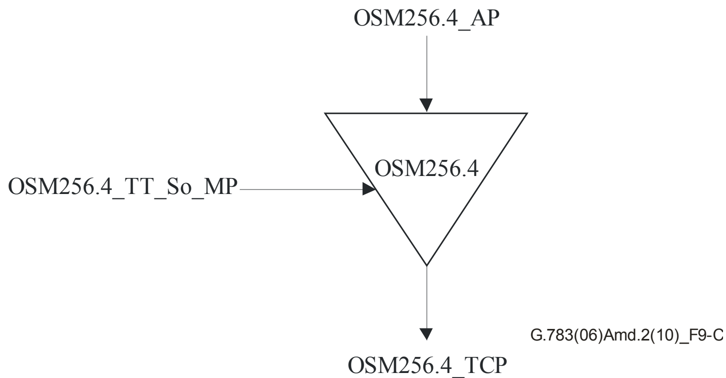

Figure 9c – OSM256.4_TT_So function

Interfaces

Table 9b – OSM256.4_TT_So inputs and outputs

Input(s)	Output(s)
OSM256.4_AP OSM256.4_AI OSM256.4_CK OSM256.4_AI_FS	OSM256.4_TCP OSM256.4_CI

Processes

The processes associated with the OSM256.4_TT function are specific processes for each lane signal of the OSM256.4 and common processes for the compound signal as depicted in Figure 9d.

Common processes

PN-11 detection: The process shall detect the generic AIS signal as described in [ITU-T G.709].

16-byte block distributer: The function shall, round robin, distribute the STM-256 signal as defined in Annex I of [ITU-T G.707] to the related lane structure of four logical lanes. The distribution is aligned to the STM-256 frame. In the event that no frame start signal is present due to the presence of an unframed generic AIS signal, the serial stream shall be arbitrarily distributed in 16-byte blocks to the lanes.

Lane specific processes

Multilane identifier insertion: The function shall insert the multilane identifier as defined in Annex I of [ITU-T G.707]. The multilane identifier replaces the 16th A2 byte position in the STL framing pattern (resulting from the STM-256 FAS signal after it has been distributed in 16-byte increments across the lanes). In the case that no STM-256 frame is present (no FS indication), no identifier shall be inserted.

STLAIS generation and insertion: The process shall insert the STLAIS indication by replacing 32 bytes on each lane after every 155'488th byte of the unstructured PN-11 pattern (distributed in 16-byte increments across the lanes) with 16 A1 bytes, followed by 15 A2 bytes, followed by a 0xFF fixed value.

Optical carrier modulation and wavelength assignment (MOD/WA): For the parameters on the optical lanes (STL-256.4), see [ITU-T G.695].

Common processes

Optical multiplexing (OM): See [ITU-T G.709].

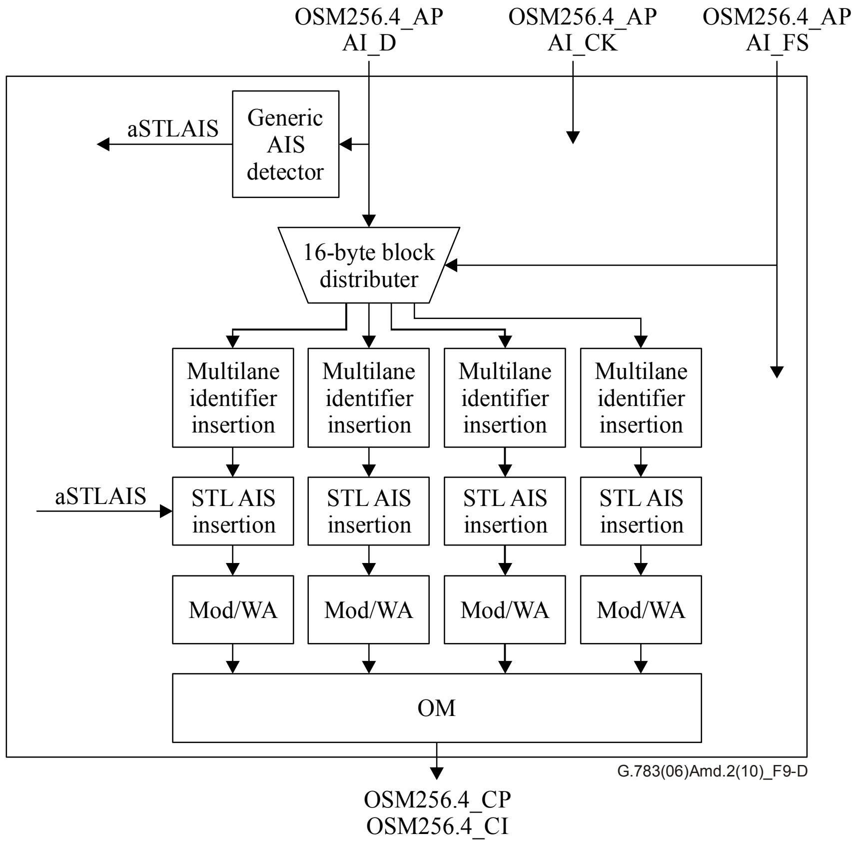

Figure 9d – OSM256.4_TT_So processes

Defects

dAIS (see clause 6.2.6.1).

Consequent actions

aSTLAIS ← dAIS

Defect correlations

None.

Performance monitoring

None.

9.2.3.2 OSM256.4_TT trail termination sink function

The information flow and processing of the OSM256.4_TT_Sk function is defined with reference to Figure 9e.

The OSM256.4_TT_Sk terminates the OSM256.4 trail. The OSM256.4_TT_Sk accepts an OSM256.4 signal with physical parameters according to [ITU-T G.695] after transport over an optical path.

Symbol

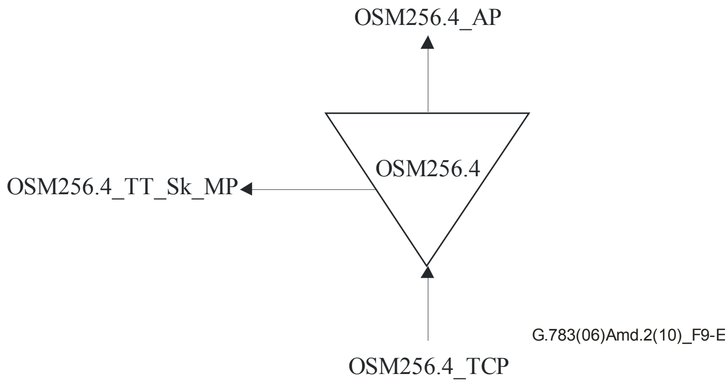

Figure 9e – OSM256.4_TT_Sk function

Interfaces

Table 9c – OSM256.4_TT_Sk inputs and outputs

Input(s)	Output(s)
OSM256.4_TCP OSM256.4_CI	OSM256.4_AP OSM256.4_AI_D OSM256.4_AI_TSF OSM256.4_TT_Sk_MP OSM256.4_TT_Sk_MI_cLOS OSM256.4_TT_Sk_MI_cLOL

Processes

The processes associated with the OSM256.4_TT_Sk function are specific processes for each lane of the STL-256.4 signal and common processes for the compound signal as depicted in Figure 9f.

Common processes

Optical demultiplexing wavelength selection, and demodulation (ODM/WS/Dmod): See [ITU-T G.709].

STL reception process: Recovers the STL-256.4 payload signal and reports the state of the STL-256.4 signal. It detects LOS of the payload signal.

Payload recovery: This function shall recover the STL-256.4 payload signals. The physical characteristics of the signals are defined in [ITU-T G.695].

Lane clock recovery: The process shall recover the clock of the STL-256.4 lane signals from the incoming data. The function shall introduce no errors in case of jitter and wander as defined in clause 6 of [ITU-T G.825].

STL frame alignment of the multilane signals: The process shall recover the STL-256.4 multilane frame start per lane as described in clause 8.2.6.

STL AIS dSTLAIS detection of multilane signals: This process shall detect the STLAIS signal by detecting a fixed value of 0xFF in the byte following the STL framing pattern (16 A1 bytes followed by 15 A2 bytes).

Lane alignment recovery: The function shall recover the lane alignment signals of the STL-256.4 lane signals from the incoming data according to clause 8.2.7.

Marker removal and STM-256 FAS recreation: The process shall re-establish the STM-256 FAS by replacing the multilane identifier in each lane with A2 while reconstructing the STM-256 frame.

Lane deskew process: The process shall compensate the differential delay between the STL-256.4 lane signals as given in Annex I of [ITU-T G.707]. The compensation between the data lanes is achieved by an elastic store per lane, writing the lane data under control of the marker processing at the correct time into the 16-byte data block multiplexer.

The elastic store shall be capable of compensating at least 180 ns of absolute differential delay between the lanes, consistent with the 802.3 specification, when used to transport STM-256 over interfaces using the C4S1-2D1 application code of [ITU-T G.695].

NOTE – IEEE 802.3 specifies limits on total skew (differential delay) and skew variation, which is limited to 4 ns.

STL-256.4 AIS generation: The process provides a generic AIS signal of PN-11 sequence toward the OSM256.4_AP.

16-byte block data signal multiplexer: The function shall multiplex the 16-byte increments of the lane signal buffers into the original order according to the lane alignment signal and rules as given in Annex I of [ITU-T G.707]. The processing of the delay compensation is given in Annex I of [ITU-T G.707].

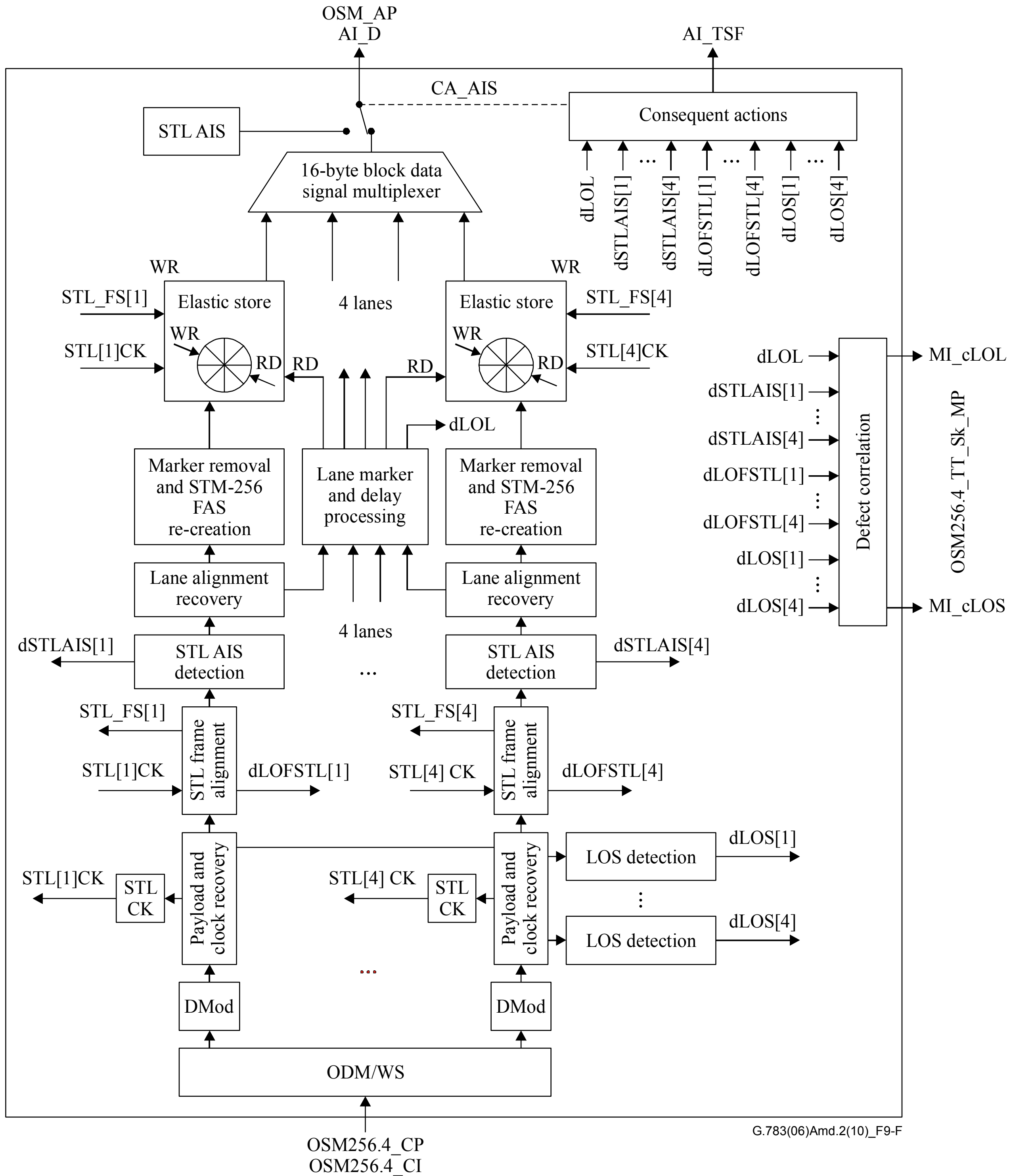

Figure 9f – OSM256.4_TT_Sk processes

Defects

The function shall detect dLOS[1..4] (for each lane), dSTLAIS, dLOFSTL, and dLOL.

dLOS[1..4]: See clause 6.2.1.1.

dSTLAIS[1..4]: See related process.

dLOL: See clause 6.2.5.6.

dLOFSTL[1..4]: See clause 6.2.5.7.

Consequent actions

The function shall perform the following consequent actions:

aTSF ← ΣdLOS[1..4] or dLOL or ΣdLOFSTL[1..4]

aAIS ← (ΠdSTLAIS[1..4]) or (ΣdLOFSTL[1..4]) or (ΣdLOS[1..4])

Defect correlations

The function shall perform the following defect correlations to determine the most probable fault cause:

cLOS ← ΣdLOS[1..4]

cLOL ← dLOL or ΣdLOFSTL[1..4] and (not ΠdSTLAIS[1..4]) and (not ΣdLOS[1..4])

Performance monitoring

For further study.

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