ITUPublications
Recommendations

International Telecommunication Union
Standardization Sector

Recommendation

ITU-T G.709.1/Y.1331.1 (2018) Amd. 4 (08/2023)

SERIES G: Transmission systems and media, digital systems and networks

Digital terminal equipments – General

SERIES Y: Global information infrastructure, Internet protocol aspects, next-generation networks, Internet of Things and smart cities

Internet protocol aspects – Transport

Flexible OTN short-reach interfaces
Amendment 4

ITU-T G-SERIES RECOMMENDATIONS

Transmission systems and media, digital systems and networks

INTERNATIONAL TELEPHONE CONNECTIONS AND CIRCUITS	G.100-G.199
GENERAL CHARACTERISTICS COMMON TO ALL ANALOGUE CARRIER-TRANSMISSION SYSTEMS	G.200-G.299
INDIVIDUAL CHARACTERISTICS OF INTERNATIONAL CARRIER TELEPHONE SYSTEMS ON METALLIC LINES	G.300-G.399
GENERAL CHARACTERISTICS OF INTERNATIONAL CARRIER TELEPHONE SYSTEMS ON RADIO-RELAY OR SATELLITE LINKS AND INTERCONNECTION WITH METALLIC LINES	G.400-G.449
COORDINATION OF RADIOTELEPHONY AND LINE TELEPHONY	G.450-G.499
TRANSMISSION MEDIA AND OPTICAL SYSTEMS CHARACTERISTICS	G.600-G.699
DIGITAL TERMINAL EQUIPMENTS	G.700-G.799
General	**G.700-G.709**
Coding of voice and audio signals	G.710-G.729
Principal characteristics of primary multiplex equipment	G.730-G.739
Principal characteristics of second order multiplex equipment	G.740-G.749
Principal characteristics of higher order multiplex equipment	G.750-G.759
Principal characteristics of transcoder and digital multiplication equipment	G.760-G.769
Operations, administration and maintenance features of transmission equipment	G.770-G.779
Principal characteristics of multiplexing equipment for the synchronous digital hierarchy	G.780-G.789
Other terminal equipment	G.790-G.799
DIGITAL NETWORKS	G.800-G.899
DIGITAL SECTIONS AND DIGITAL LINE SYSTEM	G.900-G.999
MULTIMEDIA QUALITY OF SERVICE AND PERFORMANCE – GENERIC AND USER-RELATED ASPECTS	G.1000-G.1999
TRANSMISSION MEDIA CHARACTERISTICS	G.6000-G.6999
DATA OVER TRANSPORT – GENERIC ASPECTS	G.7000-G.7999
PACKET OVER TRANSPORT ASPECTS	G.8000-G.8999
ACCESS NETWORKS	G.9000-G.9999

For further details, please refer to the list of ITU-T Recommendations.

Recommendation ITU-T G.709.1/Y.1331.1

Flexible OTN short-reach interfaces

Amendment 4

Summary

Amendment 4 adds definitions for FlexO frames using 800 Gb/s physical interfaces, including mapping of Ethernet directly to FlexO (without defining an associated FEC frame), modifications related to 100 Gb/s per lane signalling for FlexO-1 and FlexO-4, (i.e., FOIC1.1, FOIC4.4), editorial clarifications related to renaming Pad overhead as Extended overhead, reorganization of the FlexO frame description to enable potential use of different types of FEC frames for beyond 400G interfaces, and additional overhead to support new FlexO applications.

History *

Edition	Recommendation	Approval	Study Group	Unique ID
1.0	ITU-T G.709.1/Y.1331.1	2017-01-12	15	11.1002/1000/13082
2.0	ITU-T G.709.1/Y.1331.1	2018-06-22	15	11.1002/1000/13521
2.1	ITU-T G.709.1/Y.1331.1 (2018) Amd. 1	2019-04-06	15	11.1002/1000/13743
2.2	ITU-T G.709.1/Y.1331.1 (2018) Cor. 1	2020-05-07	15	11.1002/1000/14200
2.3	ITU-T G.709.1/Y.1331.1 (2018) Amd. 2	2020-12-22	15	11.1002/1000/14519
2.4	ITU-T G.709.1/Y.1331.1 (2018) Amd. 3	2022-11-13	15	11.1002/1000/15135
2.5	ITU-T G.709.1/Y.1331.1 (2018) Amd. 4	2023-08-22	15	11.1002/1000/15561

* To access the Recommendation, type the URL https://handle.itu.int/ in the address field of your web browser, followed by the Recommendation's unique ID.

FOREWORD

The International Telecommunication Union (ITU) is the United Nations specialized agency in the field of telecommunications, information and communication technologies (ICTs). The ITU Telecommunication Standardization Sector (ITU-T) is a permanent organ of ITU. ITU-T is responsible for studying technical, operating and tariff questions and issuing Recommendations on them with a view to standardizing telecommunications on a worldwide basis.

The World Telecommunication Standardization Assembly (WTSA), which meets every four years, establishes the topics for study by the ITU-T study groups which, in turn, produce Recommendations on these topics.

The approval of ITU-T Recommendations is covered by the procedure laid down in WTSA Resolution 1.

In some areas of information technology which fall within ITU-T's purview, the necessary standards are prepared on a collaborative basis with ISO and IEC.

NOTE

In this Recommendation, the expression "Administration" is used for conciseness to indicate both a telecommunication administration and a recognized operating agency.

Compliance with this Recommendation is voluntary. However, the Recommendation may contain certain mandatory provisions (to ensure, e.g., interoperability or applicability) and compliance with the Recommendation is achieved when all of these mandatory provisions are met. The words "shall" or some other obligatory language such as "must" and the negative equivalents are used to express requirements. The use of such words does not suggest that compliance with the Recommendation is required of any party.

INTELLECTUAL PROPERTY RIGHTS

ITU draws attention to the possibility that the practice or implementation of this Recommendation may involve the use of a claimed Intellectual Property Right. ITU takes no position concerning the evidence, validity or applicability of claimed Intellectual Property Rights, whether asserted by ITU members or others outside of the Recommendation development process.

As of the date of approval of this Recommendation, ITU had received notice of intellectual property, protected by patents/software copyrights, which may be required to implement this Recommendation. However, implementers are cautioned that this may not represent the latest information and are therefore strongly urged to consult the appropriate ITU-T databases available via the ITU-T website at http://www.itu.int/ITU-T/ipr/.

Table of Contents

Recommendation ITU-T G.709.1/Y.1331.1

Flexible OTN short-reach interfaces

Amendment 4

Editorial note: This is a complete-text publication. Modifications introduced by this Amendment are shown in revision marks relative to Recommendation ITU-T G.709.1/Y.1331.1 (2018) and its Amendments 1, 2 and 3, and Corrigendum 1.

1 Scope

This Recommendation specifies a set of flexible-bandwidth interoperable short-reach optical transport network (OTN) interfaces, the so called FlexO-x-RS-m interface group, over which an aggregate OTUCn (n ≥ 1) can be transferred using bonded FlexO short-reach interfaces as lower bandwidth elements.

The types of FlexO short-reach interfaces that can serve as FlexO-x-RS-m group members are covered by application codes which are at the time of publication 4I1-9D1F, 4L1-9C1F, C4S1-9D1F, 4L1-9D1F, C4S1-4D1F, 8R1-4D1F, 4I1-4D1F and 8I1-4D1F. These application codes are presented in [ITU-T G.695] and [ITU-T G.959.1].

The definition of a FlexO-x-RS-m interface group complements the existing ~~B100G~~ functions specified in [ITU-T G.709], such as OTUCn frame, ODUk/flex, with new functions such as physical interface bonding, forward error correction (FEC) coding, group management, ~~and~~ OTUCn (de)mapping.

This FlexO-x-RS Recommendation complements [ITU-T G.709] and [ITU-T G.798] and provides specifications for new functions that are specific to the processing of FlexO-x-RS-m interface group. In addition, some introduction material for the addressed application is included.

This Recommendation also contains common elements and definitions that may be used by interfaces that are outside the scope of this short reach interface Recommendation. Such definitions include FlexO frame definitions, FlexO-x interleaving, Ethernet optimized mapping procedures and frame alignment methods.

2 References

The following ITU-T Recommendations and other references contain provisions which, through reference in this text, constitute provisions of this Recommendation. At the time of publication, the editions indicated were valid. All Recommendations and other references are subject to revision; users of this Recommendation are therefore encouraged to investigate the possibility of applying the most recent edition of the Recommendations and other references listed below. A list of the currently valid ITU-T Recommendations is regularly published. The reference to a document within this Recommendation does not give it, as a stand-alone document, the status of a Recommendation.

[ITU-T G.695] Recommendation ITU-T G.695 (2018), *Optical interfaces for coarse wavelength division multiplexing applications*.

[ITU-T G.709] Recommendation ITU-T G.709/Y.1331 (2020), *Interfaces for the optical transport network*.

[ITU-T G.709.3] Recommendation ITU-T G.709.3/Y.1331.3 (2020), *Flexible OTN long-reach interfaces*.

[ITU-T G.798] Recommendation ITU-T G.798 (2017), *Characteristics of optical transport network hierarchy equipment functional blocks*.

[ITU-T G.870] Recommendation ITU-T G.870/Y.1352 (2016), *Terms and definitions for optical transport networks*.

[ITU-T G.872] Recommendation ITU-T G.872 (2019), *Architecture of the optical transport network*.

[ITU-T G.959.1] Recommendation ITU-T G.959.1 (2018*), Optical transport network physical layer interfaces*.

[ITU-T G.7041] Recommendation ITU-T G.7041/Y.1303 (2016*), Generic framing procedure*.

[ITU-T G.8260] Recommendation ITU-T G.8260 (2022), *Definitions and terminology for synchronization in packet networks*.

[IEEE 802.3] IEEE Std. 802.3-2022, IEEE Standard for Ethernet.

[NIST SP 800-38D] National Institute of Standards and Technology (2007), Recommendation for Block Cipher Modes of Operation: Galois/Counter Mode (GCM) and GMAC.

[OIF FlexE] Optical Interworking Forum, OIF (~~2017~~2021), *FlexEthernet Implementation Agreement ~~1~~2.~~1~~2*.

3 Definitions

3.1 Terms defined elsewhere

This Recommendation uses the following terms defined elsewhere:

3.1.1 Terms defined in [ITU-T G.870]:

– completely standardized OTUCn (OTUCn)

– optical data unit (ODUCn)

– optical payload unit (OPUCn)

– optical transport network (OTN)

3.1.2 cipher text [b-ITU-T X.800]: Data produced through the use of encipherment. The semantic content of the resulting data is not available.

3.1.3 confidentiality [b-ITU-T X.800]: The property that information is not made available or disclosed to unauthorized individuals, entities, or processes.

3.1.4 encryption [b-ITU-T X.800]: The cryptographic transformation of data to produce ciphertext.

3.1.5 integrity [b-ITU-T X.800]: The property that data has not been altered or destroyed in an unauthorized manner.

3.1.6 key [b-ITU-T X.800]: A sequence of symbols that controls the operations of encipherment and decipherment.

3.1.7 plaintext [b-ISO/IEC 18033-3]: Unenciphered information.

3.2 Terms defined in this Recommendation

This Recommendation defines the following terms:

3.2.1 FlexO: Information structure with a specific bit rate and frame format, consisting of overhead and payload, intended to be used in a group with n ($n \geq 1$) instances for the transport of ~~an~~ OTUCn ~~signal~~and Ethernet clients.

3.2.2 ~~FlexO-x~~FlexO-x(e): Information structure consisting of x ($x \geq 1$) ~~10-bit~~ interleaved FlexO instances, intended to be used in a group with m ($m = \lceil n/x \rceil$) instances for the transport of ~~an~~ client signals such as OTUCn ~~signal~~or Ethernet. The order x signifies the ~~FlexO-x~~FlexO-x(e) interface rate in units of 100G. Specific variants are 100G FlexO-1, 200G FlexO-2, ~~and~~ 400G FlexO-4(e) and 800G FlexO-8(e). FlexO-xe represents a FlexO-x information structure, with rate and mapping optimized for Ethernet clients.

3.2.3 FlexO-x-RS: Information structure consisting of a FlexO-x plus Reed-Solomon FEC parity.

3.2.4 FlexO-x-RS interface: Refers to an individual member interface that is part of a FlexO-x-RS-m interface group.

NOTE – The terms "member" and "PHY" are often used to refer to a FlexO-x interface.

3.2.5 FlexO-x-RS-m interface group: Refers to the group of m * FlexO-x-RS interfaces.

NOTE – The text may use "FlexO group" as short-hand for FlexO-x-RS-m interface group.

3.2.6 FOICx.k-RS: Refers to a FlexO-x-RS interface using k parallel FOICx.k-RS lanes.

NOTE – "FOICx.k" is the FlexO equivalent of "OTLk.m" for OTUk as defined in [ITU-T G.709].

3.2.7 FOICx.k-RS lane: Refers to an electrical/optical lane of a FlexO-x-RS interface.

4 Abbreviations and acronyms

This Recommendation uses the following abbreviations and acronyms:

AAD	Additional Authenticated Data
AIS	Alarm Indication Signal
AMi	Alignment Marker of index i
AM	Alignment Mechanism
AT	Authentication Tag
AVAIL	Available
~~B100G~~	~~Beyond 100G~~
BMP	Bit-synchronous Mapping Procedure
BOH	Basic Overhead Area
CAUI	(Chip to) 100 Gb/s Attachment Unit Interface
CFP2	C (100G) Form-factor Pluggable Optical Module, form factor type 2
CM	Common Marker
CRC	Cyclic Redundancy Check
CSF	Client Signal Fail
CST	Cipher Suite Type
CSTAT	Client Status
EOH	Extended Overhead Area
FA	Frame Alignment

FAS	Frame Alignment Signal
FCC0/1	FlexO Communications Channel 0 or 1
FEC	Forward Error Correction
FlexE	Flexible Ethernet
FlexO	Flexible Optical Transport Network
FN	Frame Number
FOIC-RS	FlexO-x-RS Interface
FS	Fixed Stuff
GFP	Generic Framing Procedure
GID	Group Identification
GMP	Generic Mapping Procedure
IA	Implementation Agreement
IID	FlexO Instance Identification
IV	Initialization Vector
JC	Justification Control
KCC	Key exchange Communication Channel
KI	Key Index
LCK	Locked
LD	Local Degrade
LF	Local Fault
LSB	Least Significant Bit
MAP	FlexO Map field
MFAS	Multi-Frame Alignment Signal
MNT	Maintenance
MS	Multiplexed Section
MSB	Most Significant Bit
MSI	Mutltiplex Structure Identifier
ODU	Optical Data Unit
OH	Overhead
OPU	Optical Payload Unit
OSMC	OTN Synchronization Messaging Channel
OTL	Optical Transport Lane
OTN	Optical Transport Network
OTU	Optical Transport Unit
PCS	Physical Coding Sublayer
PHY	Physical Layer
PRBS	Pseudo Random Binary Sequence

PT Payload Type

PTP Precision Time Protocol

QSFP28 Quad (100G) Small Form-factor Pluggable

RD Remote Degrade

RES Reserved for Future International Standardization

RF Remote Fault

RPF Remote Physical Layer Fault

RS Reed-Solomon

RMFAS Remote Multi-Frame Alignment Signal

RSTAT Regen Status

SM Section Monitoring

SSM Synchronization Status Message

STAT Status

RTTI Regen Trail Trace Identifier

UM Unique Marker

UP Unique Padding

5 Conventions

This Recommendation uses the following conventions:

k: The index "k" is used to represent a supported bit rate and the different versions of OPUk, ODUk and OTUk. Examples for k are "1" for an approximate bit rate of 2.5 Gbit/s, "2" for an approximate bit rate of 10 Gbit/s, and "3" for an approximate bit rate of 40 Gbit/s.

Cn: The index Cn is used for n×100G (C=100G).

m: The index "m" is used to represent ~~the bit rate or set of bit rates supported on the interface. This is one or more digits "k", where each "k" represents a particular bit rate. For example, valid values for m are (1, 2, 3, 12, 123, 23).~~the number of interfaces in a FlexO group. m is also used to represent the number of bits in a block of data/stuff in client mappings.

n: The index "n" is used to represent ~~the order of the OTM, OTS, OMS, OPS, OCG, OMU. n represents the maximum number of wavelengths that can be supported at the lowest bit rate supported on the wavelength. It is possible that a reduced number of higher bit rate wavelengths are supported. n = 0 represents the case of a single channel without a specific colour assigned to the channel~~the number of FlexO instances that are in a FlexO group.

~~**r**: The index "r", if present, is used to indicate a reduced functionality OTM, OCG, OCC and OCh (non-associated overhead is not supported). Note that for n = 0 the index r is not required as it implies always reduced functionality.~~

x: The index "x" is used to represent the bit rate of the FlexO interface, in 100G increments. For example, x=1 for 100G, x=2 for 200G, x=4 for 400G, etc.

(e): when used as FlexO-x(e) is short-hand for "or" (e.g., FlexO-x or FlexO-xe), with the "e" meaning— optimized for Ethernet payloads.

Transmission order: The order of transmission of information in all the diagrams in this Recommendation is first from left to right and then from top to bottom. Within each byte the most

significant bit is transmitted first. The most significant bit (bit 1) is illustrated on the left side of all diagrams.

Value of reserved bit(s): The value of an overhead bit, which is reserved for future international standardization, shall be set to "0".

Value of non-sourced bit(s): Unless stated otherwise, any non-sourced bits shall be set to "0".

6 Introduction and applications

A FlexO-x-RS-m (Flexible OTN short reach) interface group is defined for interoperable multi-vendor applications. It complements ~~B100G (~~beyond 100G~~)~~ [ITU-T G.709], by providing an interoperable interface for OTUCn transport signals. A FlexO-x-RS-m interface group provides modularity by bonding standard-rate interfaces (e.g., m × 100G), over which the OTUCn ($n \geq 1$) signal is adapted. The value of m is not standardized. The specification of OTUCn in [ITU-T G.709] excludes interface specific functions such as FEC, scrambling and bit alignment. A FlexO-x-RS interface or a FlexO-x-RS-m group wraps OTUCn, abstracting the transport signal from the interface. FlexO-x-RS-m enables ODUflex services >100Gbit/s to be supported across multiple interfaces, ahead of next generation interface standards such as 400GE [IEEE 802.3].

FlexO-x-RS provides OTN interfaces with comparable functionality to what was introduced in [OIF FlexE] for Ethernet interfaces.

Example applications are provided in Appendix I.

6.1 FlexO-x-RS-m interface group considerations

Considerations and capabilities for a FlexO-x-RS-m interface group:

– provides an interoperable system interface for OTUCn transport signals;

– enables higher capacity ODUflex and OTUCn, by means of bonding m standard-rate interfaces;

– provides interface rate modularity and flexibility;

– provides a frame, alignment, deskew, group management, management communication channel and such functions that are not associated with the OTUCn transport signal; and

– reuses 100G modules (e.g., CFP2, QSFP28) by matching the interface rate to OTU4 as specified in [ITU-T G.709].

The rate-specific FlexO-x-RS interfaces specified in this Recommendation are located at a system external reference point.

NOTE – The logical signal format FOICx.k-RS can be reused on a system internal interface (module framer interface). Related requirements and any optimizations to the FlexO-x-RS-m groups when used as intra-system interface (e.g., lower latency by removing FEC) are beyond the scope of this Recommendation and covered in [b-ITU-T G-Sup.58].

7 Structure and processes

This clause introduces the functions associated with a FlexO-x-RS-m interface group and the basic signal structure, processes and atomic functions.

7.1 Basic signal structure

The FlexO-x-RS-m interface group in this Recommendation is only specified for short-reach applications. The FlexO-x-RS-m interface group functional model is specified in [ITU-T G.872]. The physical optical interface specifications are beyond the scope of this Recommendation.

The information structure for FlexO-x-RS-m interface group is represented by information containment relationships and flows. The principal information containment relationship is described in Figure 7-1.

One OTUCn signal is mapped into n FlexO signals, each FlexO signal containing one OTUC instance. The n FlexO instances are mapped into m ($m \leq n$) FlexO-x-RS interfaces, each FlexO-x-RS interface containing one FlexO instance or multiple, interleaved FlexO instances plus FEC. Each FlexO-x-RS interface is split into k FlexO-x-RS lane signals. Each lane signal is modulated onto one OTSi and the k OTSi's are transported as an OTSiG via one media element.

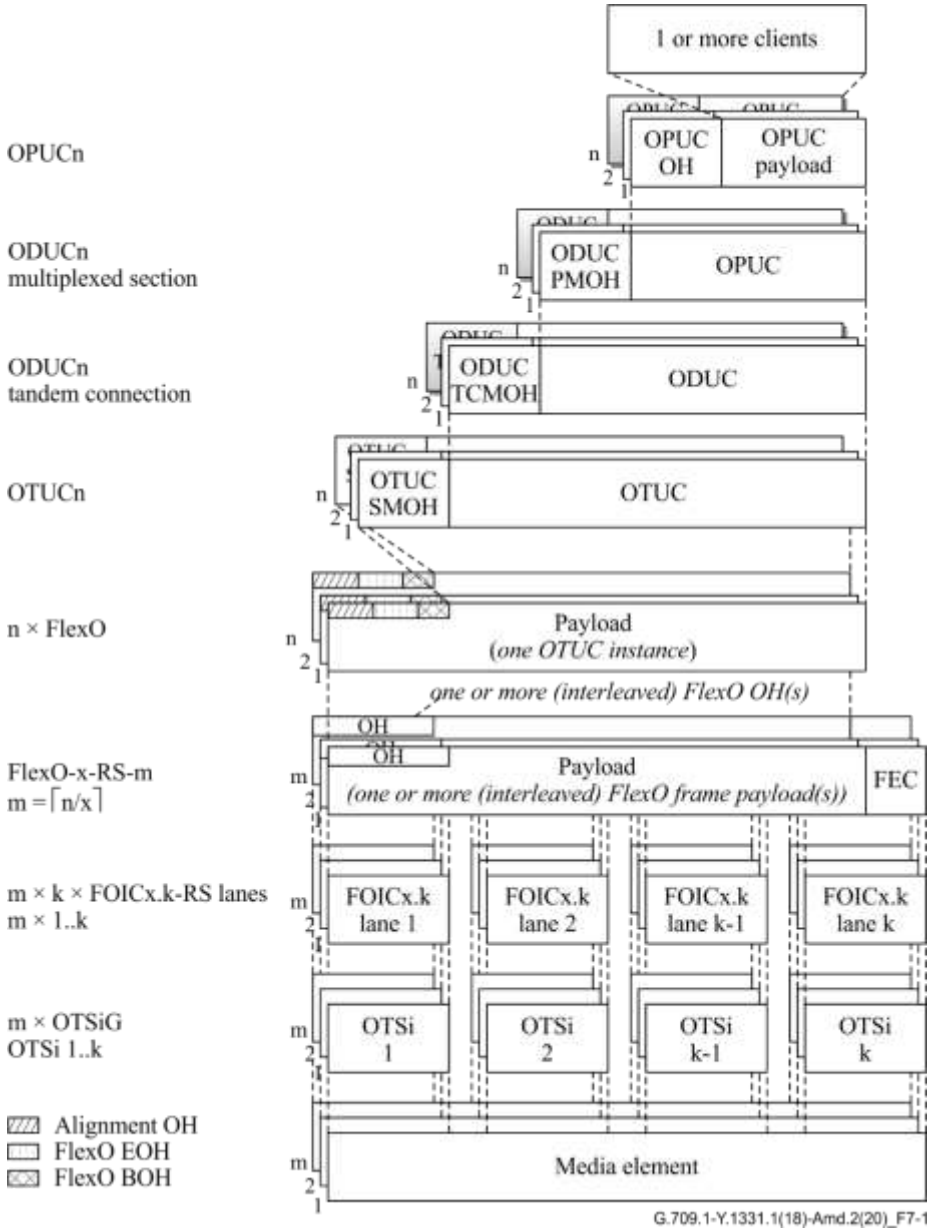

Figure 7-1 – FlexO-x-RS-m interface group principal information containment relationship

7.2 Processing and information flow

Functions, processes and information flows are more formally specified in [ITU-T G.798].

8 FlexO frame

A FlexO frame is associated with a ~~FlexO-x~~FlexO-x(e)-<fec> interface and is independent of client payload~~an OTUCn frame boundary and transport unit, the latter being specified in [ITU-T G.709]~~. A FlexO frame structure can be used for FlexO-x or Ethernet optimized FlexO-xe interfaces.

~~NOTE – The OTUCn is the transport unit over OTN interfaces and consists of n OTUC frames. It is specified in [ITU-T G.709].~~

A FlexO frame consists of frame alignment ~~marker~~ mechanism (AM) field, extended overhead area (EOH), basic overhead area (BOH) and payload area.

The FlexO frames carried over m interfaces of a ~~FlexO-x~~FlexO-x(e)-<fec>-m interface group are frame/multi-frame aligned at the source.

8.1 Frame structure

The FlexO frame structure is shown in Figure 8-1 and consists of 128 rows by 5,140 1-bit columns. It contains a frame alignment ~~marker group area~~ mechanism (AM) field in row 1, columns 1 to 480, an extended overhead area (EOH) in row 1, columns 481 to 960 per 100G instance, a basic overhead area (BOH) in row 1 columns 961 to 1280 and a (128 × 5140 – 1280 = 656640 bit) payload area in the remainder of the frame.

NOTE – The FlexO frame structure is derived from 100Gbit/s Ethernet clause 91 [IEEE 802.3] FEC alignment and lane architecture, without any 66b alignment or 256b/257b transcoding functions.

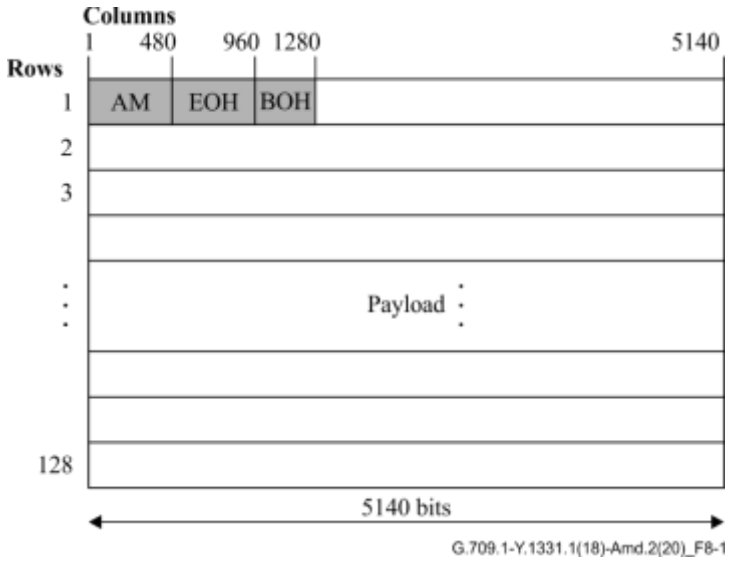

Figure 8-1 – FlexO frame structure

8.2 Multi-frame structure

In order to provide space for additional OH fields, an 8-frame FlexO multi-frame structure is defined. It uses the three least significant bits of the multi-frame alignment signal (MFAS) overhead to identify the eight frames within the multi-frame.

The multi-frame payload structure definition has been moved to the ~~OTUC~~ mapping specific clause~~s , such as 10.2 and 10.3~~10.

Figure 8-2 – Blank figure (deleted by Amd.2)

8.3 Bit rates and frame periods

The bit rates and tolerances of the FlexO signal interfaces ~~is~~ are defined in Table 8-1.

Table 8-1 – FlexO bit rates

Interface type	FlexO instance nominal bit rate	FlexO bit-rate tolerance
FlexO-x	491384/462961 × 99 532 800 kbit/s	±20 ppm
FlexO-xe	21845/25984 × 766 × 156 250 kbit/s	±20 ppm
NOTE 1 – The nominal FlexO instance bit rate used with FlexO-x is approximately: 105 643 510.782 kbit/s. The FlexO instance bit rate can be derived from the OTUC bit rate as follows: 4112/4097 × OTUC bit rate = 4112/4097 × 239/226 × 99 532 800 kbit/s. NOTE 2 – The nominal FlexO instance bit rate used with FlexO-xe is approximately: 100 622 438.327 kbit/s. The FlexO instance bit rate can be derived from 156M Ethernet clock multiple as follows: 514/544 × 1445/1624 × 766 × 156 250 kbit/s. NOTE 3 – The nominal FlexO-x(e) frame signal bit rate is x × FlexO instance nominal bit rate, so approximately x × 105 643 510.782 kbit/s for FlexO-x and x × 100 622 438.327 kbit/s for FlexO-x.		

~~FlexO nominal bit rate~~	~~FlexO bit-rate tolerance~~
~~491384/462961 × 99 532 800 kbit/s~~	~~±20 ppm~~
~~NOTE 1 – The nominal FlexO bit rate is approximately: 105 643 510.782 kbit/s.~~ ~~NOTE 2 – The FlexO bit rate can be based on the OTUC bit rate as follows: 4112/4097 × OTUC bit rate = 4112/4097 × 239/226 × 99 532 800 kbit/s.~~	

The frame and multi-frame periods of the FlexO signal interfaces are defined in Table 8-2.

Table 8-2 – FlexO frame and multi-frame periods

Interface type	Frame period (Note)	Multi-frame period (Note)
FlexO-x	~6.228 µs	49.822 µs
FlexO-xe	~6.539 µs	52.310 µs
NOTE – The period is an approximated value, rounded to 3 decimal places.		

~~Frame period (Note)~~	~~Multi-frame period (Note)~~
~~6.228 µs~~	~~49.822 µs~~
~~NOTE – The period is an approximated value, rounded to 3 decimal places.~~	

FlexO maintenance signals (AIS, LCK) are generated using a local clock.

8.4 Flex~~O-x~~O-x(e) frame structure

The 100G FlexO-1 frame structure is equal to the 100G FlexO instance frame structure as shown in Figure 8-1.

NOTE 1 – There is no Ethernet optimized frame structure at this 100G rate.

The 200G FlexO-2 frame structure is shown in Figure 8-3 and consists of 128 rows by 10280 1-bit columns. Columns 1 to 10280 contain two 10-bit interleaved 100G FlexO frame structures (#A, #B) as defined in clause 8.1. FlexO instances #1 and #2 are 10-bit interleaved into the FlexO-2 frame in the order #A, #B, #A, #B, #A, etc.

NOTE 2 – There is no Ethernet optimized frame structure at this 200G rate.

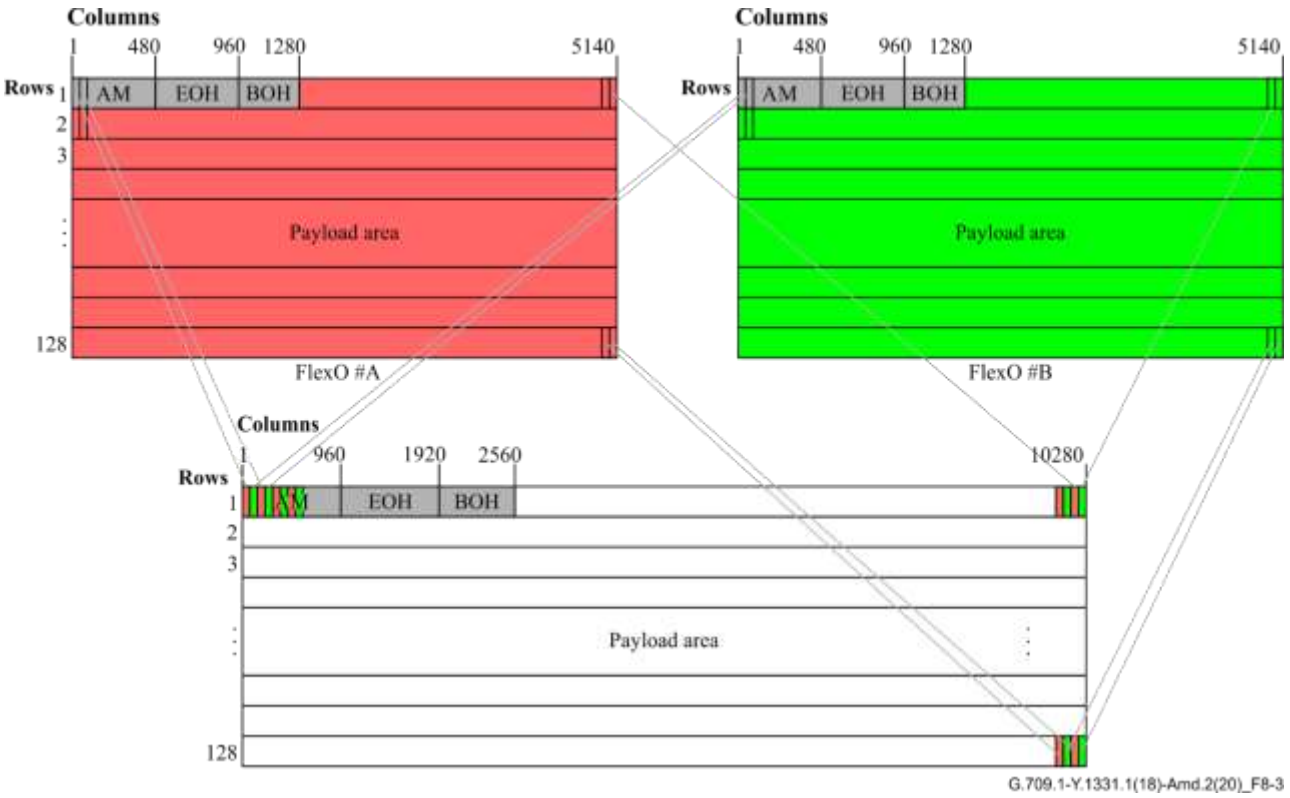

Figure 8-3 – 200G FlexO-2 frame structure

The 400G FlexO-4(e) frame structure is shown in Figure 8-4 and consists of 256 rows by 10280 1-bit columns. Columns 1 to 10280 contain four ~~10~~z-bit interleaved 100G FlexO instances (#A, #B, #C, #D) as defined in clause 8.1. FlexO instances #A, #B, #C and #D are z-bit interleaved into the FlexO-4(e) frame in the order #A, #B, #C, #D, #A, #B, etc.

For short reach FlexO-4-RS interface z=10.

For long reach FlexO-4 (16QAM) interface z=10, for FlexO-4(e) (QPSK) interface z=128.

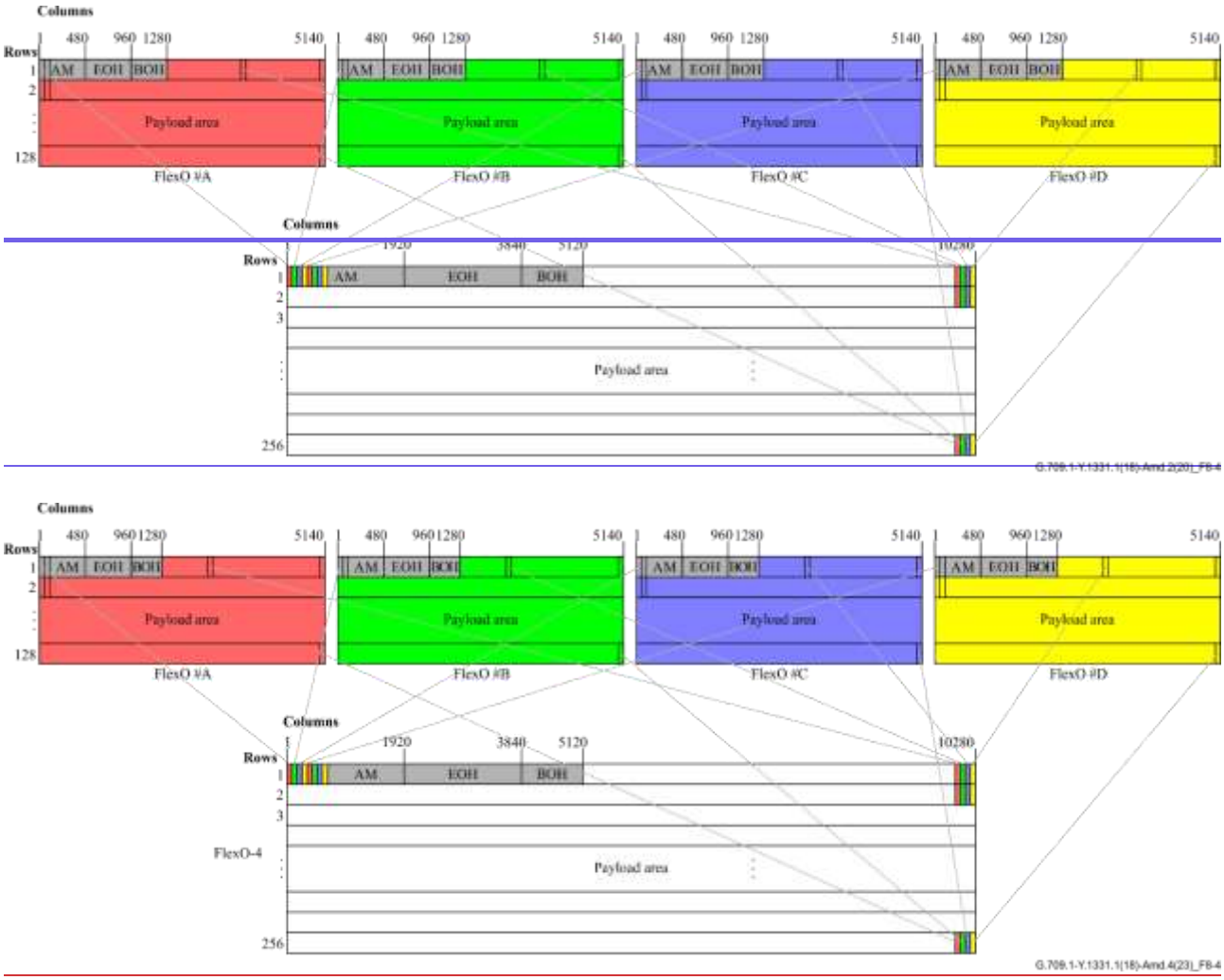

Figure 8-4 – 400G FlexO-4(e) frame structure

The 800G FlexO-8(e) frame structure is shown in Figure 8-5 and consists of 512 rows by 10280 1-bit columns. Columns 1 to 10280 contain eight z-bit interleaved 100G FlexO instances (#A, #B, #C, #D, #E, #F, #G, #H) as defined in clause 8.1. FlexO instances #A, #B, #C … #H are z-bit interleaved into the FlexO-8(e) frame in the order #A, #B, #C, #D, #E, #F, #G, #H, #A, #B, etc.

For short reach FlexO-8-RS interface z=10.

For long reach FlexO-8(e) (16QAM) interface z=128.

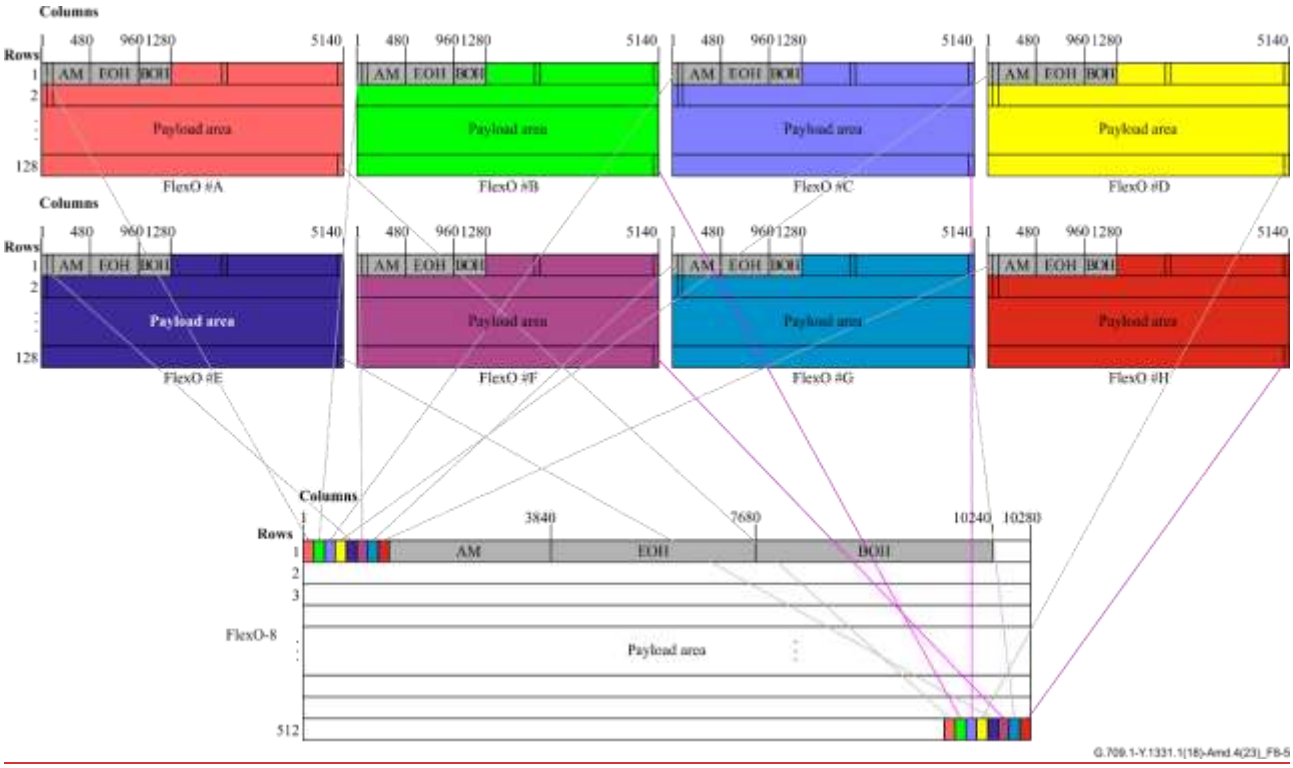

Figure 8-5 – 800G FlexO-8(e) frame structure

9 Alignment mechanism field ~~markers~~ and overhead

The FlexO frame overhead consists of alignment ~~markers~~ mechanism field~~(AM)~~, basic overhead (BOH) and extended overhead (EOH). FlexO total overhead areas in an elementary FlexO frame consist of 1,280 bits per 100G FlexO instance, 480 bits for AM~~s~~, 480 bits for EOH and 320 bits for BOH. ~~The FlexO frame overhead is terminated where the FlexO frame is assembled and disassembled.~~

The aggregate frame of a higher rate ~~FlexO-x~~FlexO-x-<fec> interface is constructed by interleaving multiple FlexO frame instances.

An overview of FlexO frame overhead areas is presented in Figure 9-1.

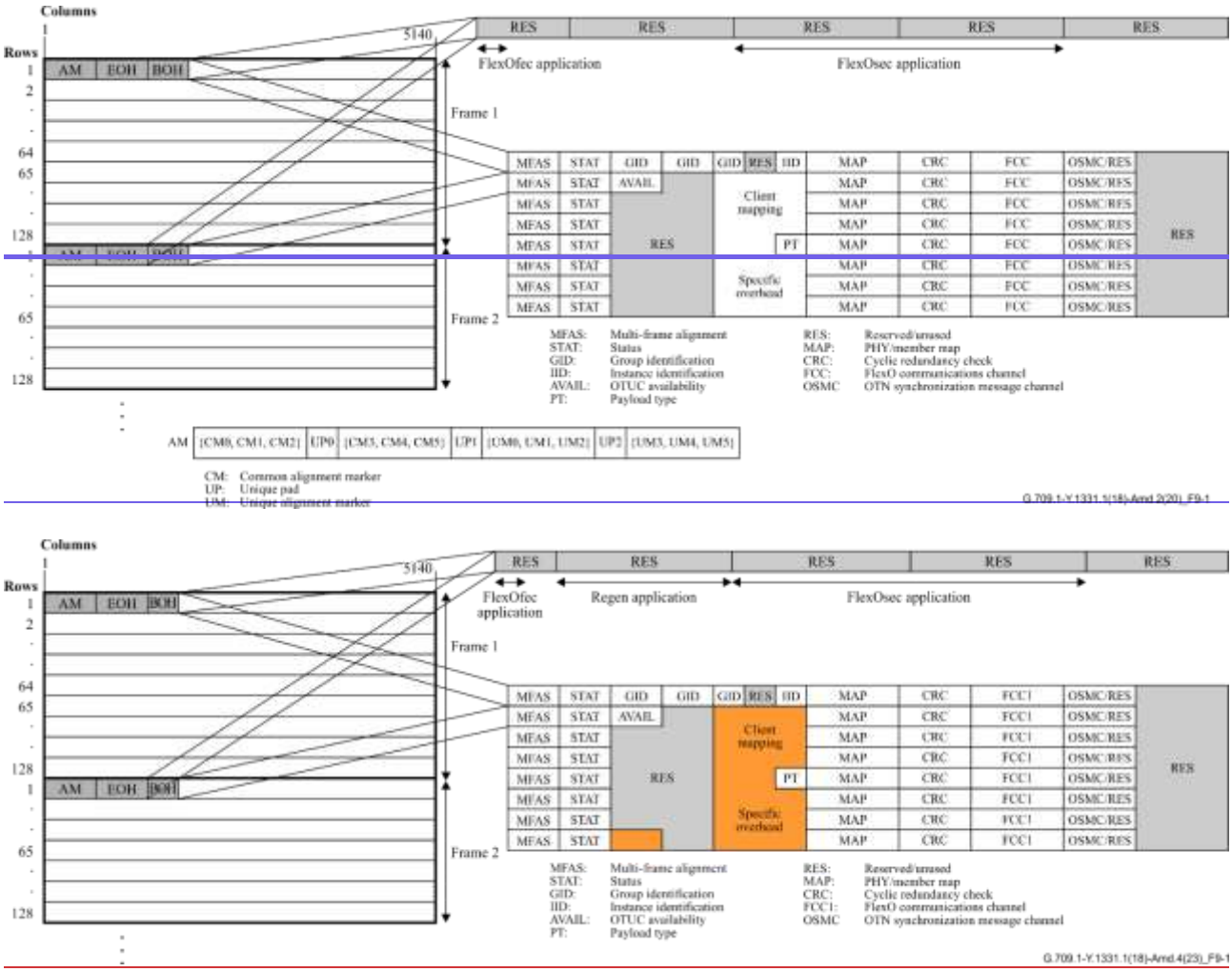

Figure 9-1 – Overhead overview

9.1 Lane alignment markers

Lane alignment markers in the alignment mechanism (AM) are used for lane alignment, lane delineation, lane ordering and lane deskewing.

~~The alignment marker (AM) area length for a FlexO frame is defined as 480 bits, which holds f~~Four 120-bit lane alignment markers fit in the AM field.

A lane alignment marker, as shown in Figure 9-2, consists of a common portion across all lanes, a unique portion per lane and some pad bits.

– CMx = 8-bit common marker field (common across lanes) – used for aligning lanes;

– ~~Umx~~ UMx = 8-bit unique marker field – used for identifying lanes;

– ~~Upx~~ Upx = 8-bit unique pad field – used for providing a DC balance when multiplexing lanes.

NOTE – Alignment marker area length specified by clause 91 [IEEE 802.3] for 100 Gbit/s Ethernet interfaces, is 1285-bit per ~~AM~~ alignment marker FEC frame period (every 4096 FEC codewords). It consists of 20 ~~AM~~ alignment marker blocks of 64-bit, plus 5-bit extra padding required for 257b block alignment. ~~Since the FlexO adaptation method described in this document does not rely on 257b blocks, the five padding bits are unnecessary.~~

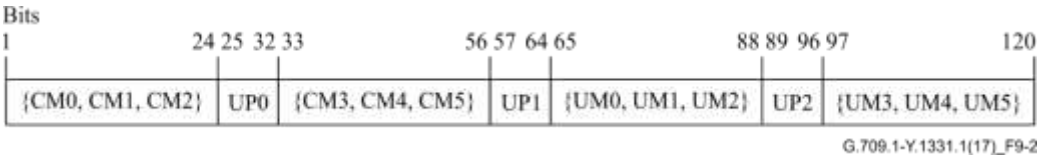

Figure 9-2 – FOICx.k lane alignment marker format

9.1.1 FlexO-1 alignment markers

The 100G FlexO-1 frame signal supports subsequent distribution into four logical lanes, numbered 0, 1, 2 and 3. Each lane carries a 120-bit lane alignment marker (am_i, i = 0,1,2,3) as specified in Table 9-1. Rows of Table 9-1 give the values of am_i transmitted over logical lane i.

The 480-bit FlexO-1 ~~alignment marker area~~AM contains 10-bit interleaved parts of am_0, am_1, am_2 and am_3 as illustrated in Figure 9-3. The 480 bits contain the 10-bit interleaved parts of am_0 to am_3 in the order am_0, am_1, am_2, am_3, am_0, am_1, etc.

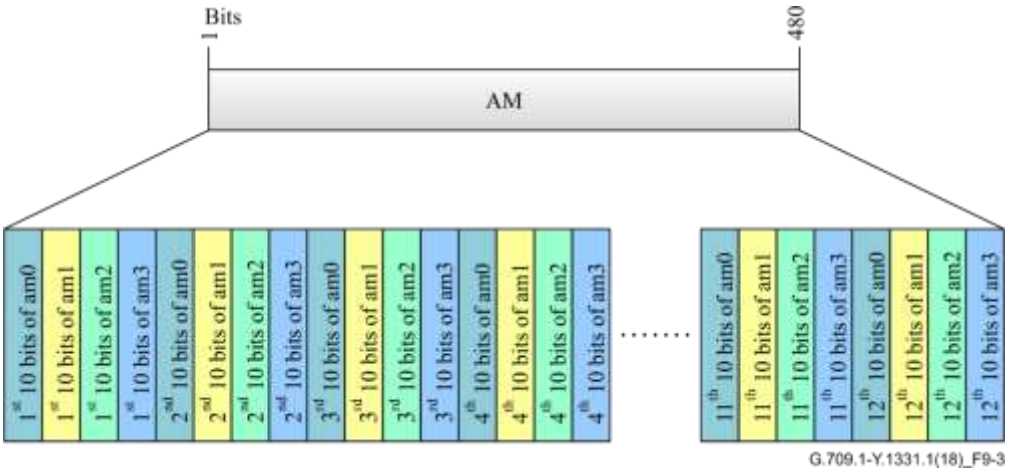

Figure 9-3 – 100G FlexO ~~alignment marker area~~AM with four interleaved lane alignment markers

Table 9-1 – FlexO-1 alignment marker encodings

logical lane	Encoding														
	{CM0, CM1, CM2, UP0, CM3, CM4, CM5, UP1, UM0, UM1, UM2, UP2, UM3, UM4, UM5}														
0	59	52	64	6D	A6	AD	9B	9B	80	8E	CF	64	7F	71	30
1	59	52	64	20	A6	AD	9B	E6	5A	7B	7E	19	A5	84	81
2	59	52	64	62	A6	AD	9B	7F	7C	CF	6A	80	83	30	95
3	59	52	64	5A	A6	AD	9B	21	61	01	0B	DE	9E	FE	F4
NOTE – The value in each byte of this ~~T~~table is in MSB-first transmission order. Note that this per-byte bit ordering is the reverse of AM values found in [IEEE 802.3], which uses an LSB-first bit transmission format.															

9.1.2 100G FlexO PAD

FlexO PAD has been repurposed as extended overhead. This clause is superseded and left blank, including Figure 9-4, which is not used.

Figure 9-4 –Blank figure (deleted by Amd.2)

9.1.3 FlexO-2 alignment markers

The 200G FlexO-2 frame signal supports subsequent distribution into eight logical lanes, numbered 0, 1, 2 to 7. Each lane carries a 120-bit lane alignment marker (am_i, i = 0,1,2 to 7) as specified in Table 9-2. Rows of Table 9-2 give the values of am_i transmitted over logical lane i.

The 960-bit FlexO-2 ~~alignment marker group area~~AM contains 10-bit interleaved parts of am_0, am_1, am_2, am_3, am_4, am_5, am_6 and am_7 as illustrated in Figure 9-5. The 480 bits of the first 100G FlexO-1 instance contain the 10-bit interleaved parts of am_0 to am_7 in the order am_0, am_2, am_4, am_6, am_1, am_3, am_5, am_7, etc. The 480 bits of the second 100G FlexO-1 instance contain the 10-bit interleaved parts of am_0 to am_7 in the order am_1, am_3, am_5, am_7, am_0, am_2, am_4, am_6, etc.

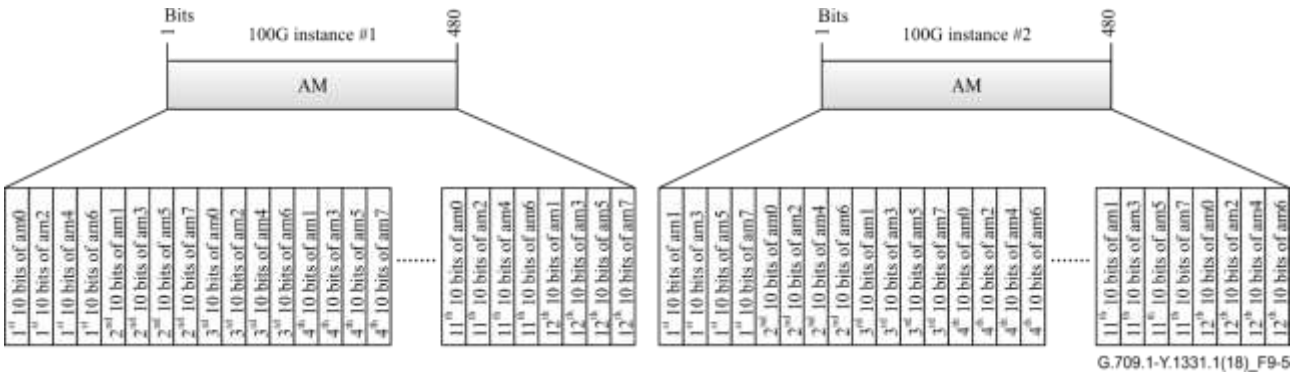

Figure 9-5 – 200G FlexO ~~alignment marker area~~AM with eight interleaved lane alignment markers

Table 9-2 – FlexO-2 alignment marker encodings

logical lane	Encoding														
	{CM0, CM1, CM2, UP0, CM3, CM4, CM5, UP1, UM0, UM1, UM2, UP2, UM3, UM4, UM5}														
0	59	52	64	A0	A6	AD	9B	6B	CD	03	31	94	32	FC	CE
1	59	52	64	20	A6	AD	9B	E6	5A	7B	7E	19	A5	84	81
2	59	52	64	62	A6	AD	9B	7F	7C	CF	6A	80	83	30	95
3	59	52	64	5A	A6	AD	9B	21	61	01	0B	DE	9E	FE	F4
4	59	52	64	87	A6	AD	9B	98	54	8A	4F	67	AB	75	B0
5	59	52	64	4F	A6	AD	9B	72	48	F2	8B	8D	B7	0D	74
6	59	52	64	BC	A6	AD	9B	77	42	39	85	88	BD	C6	7A
7	59	52	64	44	A6	AD	9B	4C	6B	6E	DA	B3	94	91	25
NOTE – The value in each byte of this table is in MSB-first transmission order. Note that this per-byte bit ordering is the reverse of ~~AM~~ alignment marker values found in [IEEE 802.3], which uses an LSB-first bit transmission format.															

9.1.4 FlexO-2 PAD

FlexO PAD has been repurposed as extended overhead. This clause is superseded and left blank.

9.1.5 FlexO-4 alignment markers

The 400G FlexO-4 frame signal supports subsequent distribution into sixteen logical lanes, numbered 0, 1, 2 to 15. Each lane carries a 120-bit lane alignment marker (am_i, i = 0,1,2 to 15) as specified in Table 9-3. Rows of Table 9-3 give the values of am_i transmitted over logical lane i.

The 1920-bit FlexO-4 ~~alignment marker group area~~AM contains 10-bit interleaved parts of am_0, am_1, am_2, am_3, am_4, am_5, am_6, am_7, am_8, am_9, am_{10}, am_{11}, am_{12}, am_{13}, am_{14} and am_{15} as illustrated in Figure 9-6. The 960 bits of the first 200G FlexO-2 instance contain the 10-bit interleaved parts of am_0 to am_{15} in the order am_0, am_2, am_4, am_6, am_8, am_{10}, am_{12}, am_{14}, am_1, am_3, am_5, am_7, am_9, am_{11}, am_{13}, am_{15}, etc. The 960 bits of the second 200G FlexO-2 instance contain the 10-bit interleaved parts of am_0 to am_{15} in the order am_1, am_3, am_5, am_7, am_9, am_{11}, am_{13}, am_{15}, am_0, am_2, am_4, am_6, am_8, am_{10}, am_{12}, am_{14}, etc.

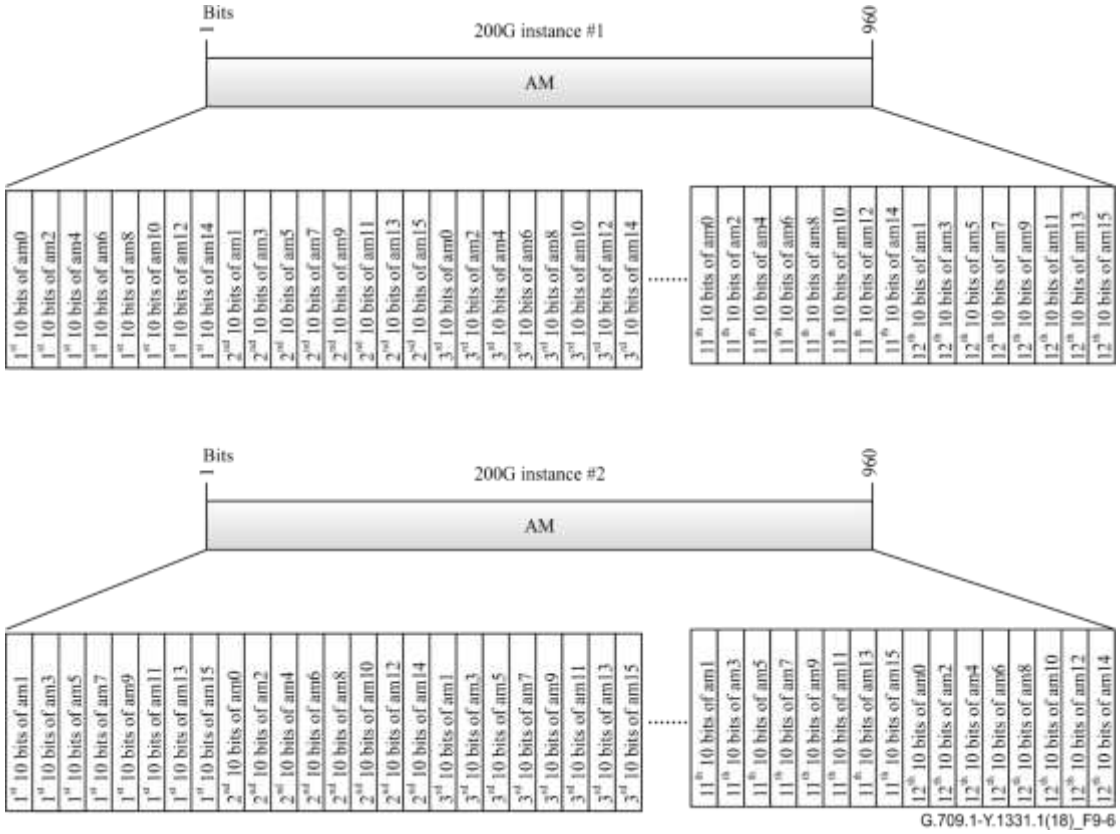

Figure 9-6 – 400G FlexO ~~alignment marker area~~AM with sixteen interleaved lane alignment markers

Table 9-3 – FlexO-4 alignment marker encodings

logical lane	Encoding														
	{CM0, CM1, CM2, UP0, CM3, CM4, CM5, UP1, UM0, UM1, UM2, UP2, UM3, UM4, UM5}														
0	59	52	64	6D	A6	AD	9B	9B	80	8E	CF	64	7F	71	30
1	59	52	64	20	A6	AD	9B	E6	5A	7B	7E	19	A5	84	81
2	59	52	64	62	A6	AD	9B	7F	7C	CF	6A	80	83	30	95
3	59	52	64	5A	A6	AD	9B	21	61	01	0B	DE	9E	FE	F4
4	59	52	64	87	A6	AD	9B	98	54	8A	4F	67	AB	75	B0
5	59	52	64	4F	A6	AD	9B	72	48	F2	8B	8D	B7	0D	74
6	59	52	64	BC	A6	AD	9B	77	42	39	85	88	BD	C6	7A
7	59	52	64	44	A6	AD	9B	4C	6B	6E	DA	B3	94	91	25
8	59	52	64	06	A6	AD	9B	F9	87	CE	AE	06	78	31	51
9	59	52	64	D6	A6	AD	9B	45	8E	23	3C	BA	71	DC	C3

Table 9-3 – FlexO-4 alignment marker encodings

logical lane	Encoding														
	{CM0, CM1, CM2, UP0, CM3, CM4, CM5, UP1, UM0, UM1, UM2, UP2, UM3, UM4, UM5}														
10	59	52	64	5F	A6	AD	9B	20	A9	D7	1B	DF	56	28	E4
11	59	52	64	36	A6	AD	9B	8E	44	66	1C	71	BB	99	E3
12	59	52	64	18	A6	AD	9B	DA	45	6F	A9	25	BA	90	56
13	59	52	64	28	A6	AD	9B	33	8C	E9	C3	CC	73	16	3C
14	59	52	64	0B	A6	AD	9B	8D	53	DF	65	72	AC	20	9A
15	59	52	64	2D	A6	AD	9B	6A	65	5D	9E	95	9A	A2	61
NOTE – The value in each byte of this Table is in MSB-first transmission order. Note that this per-byte bit ordering is the reverse of ~~AM~~ alignment marker values found in [IEEE 802.3], which uses an LSB-first bit transmission format.															

9.1.6 FlexO-4 PAD

FlexO PAD has been repurposed as extended overhead. This clause is superseded and left blank.

9.2 Basic overhead (BOH) description

The FlexO BOH area is contained in the 320 bits following the FlexO frame EOH area. The BOH structure amounts to 2,560 bits (320 bytes) and is distributed across an 8-frame multi-frame, as shown in Figure 9-7a. Each frame contains 40 BOH bytes.

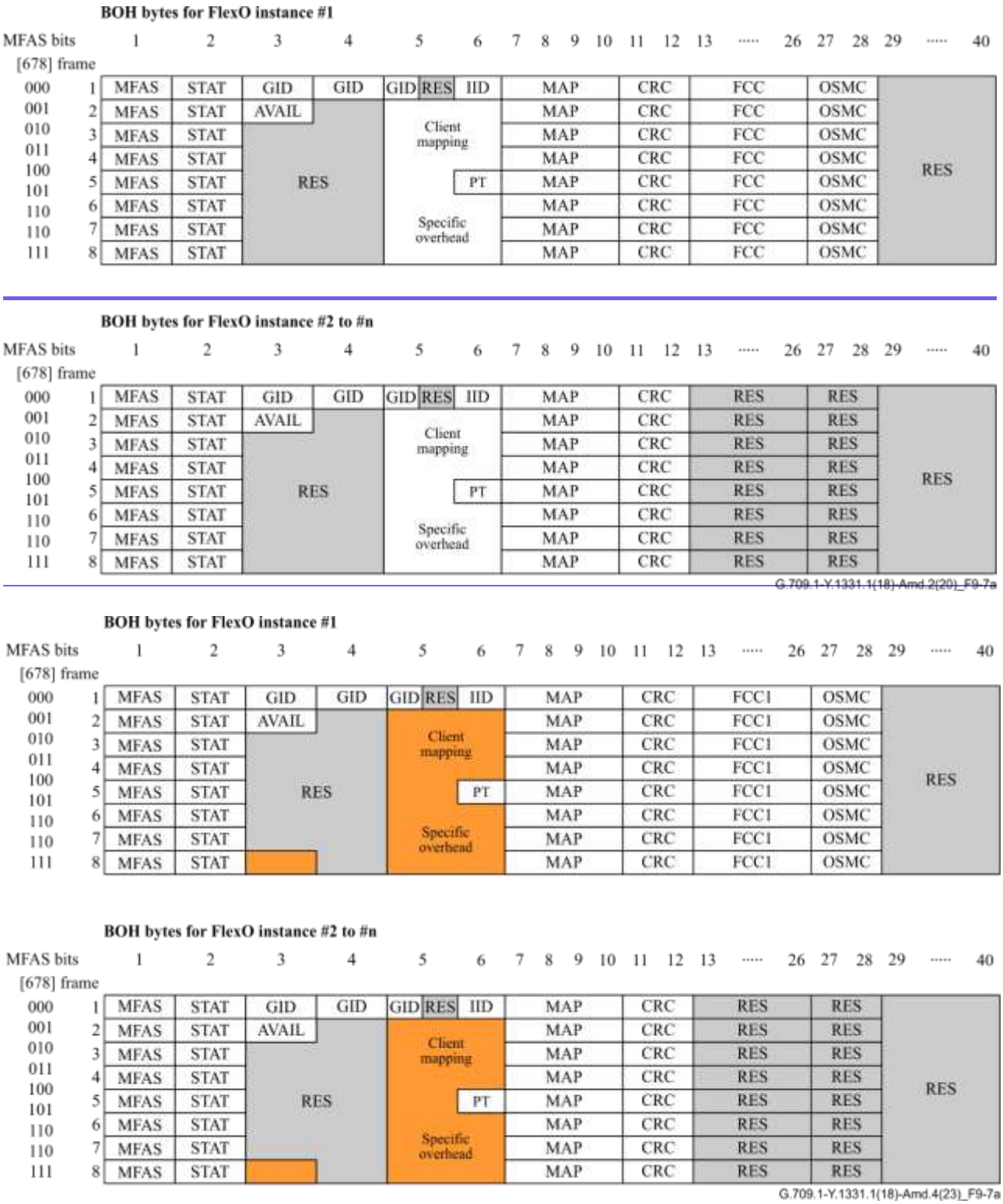

Figure 9-7a – FlexO BOH structure

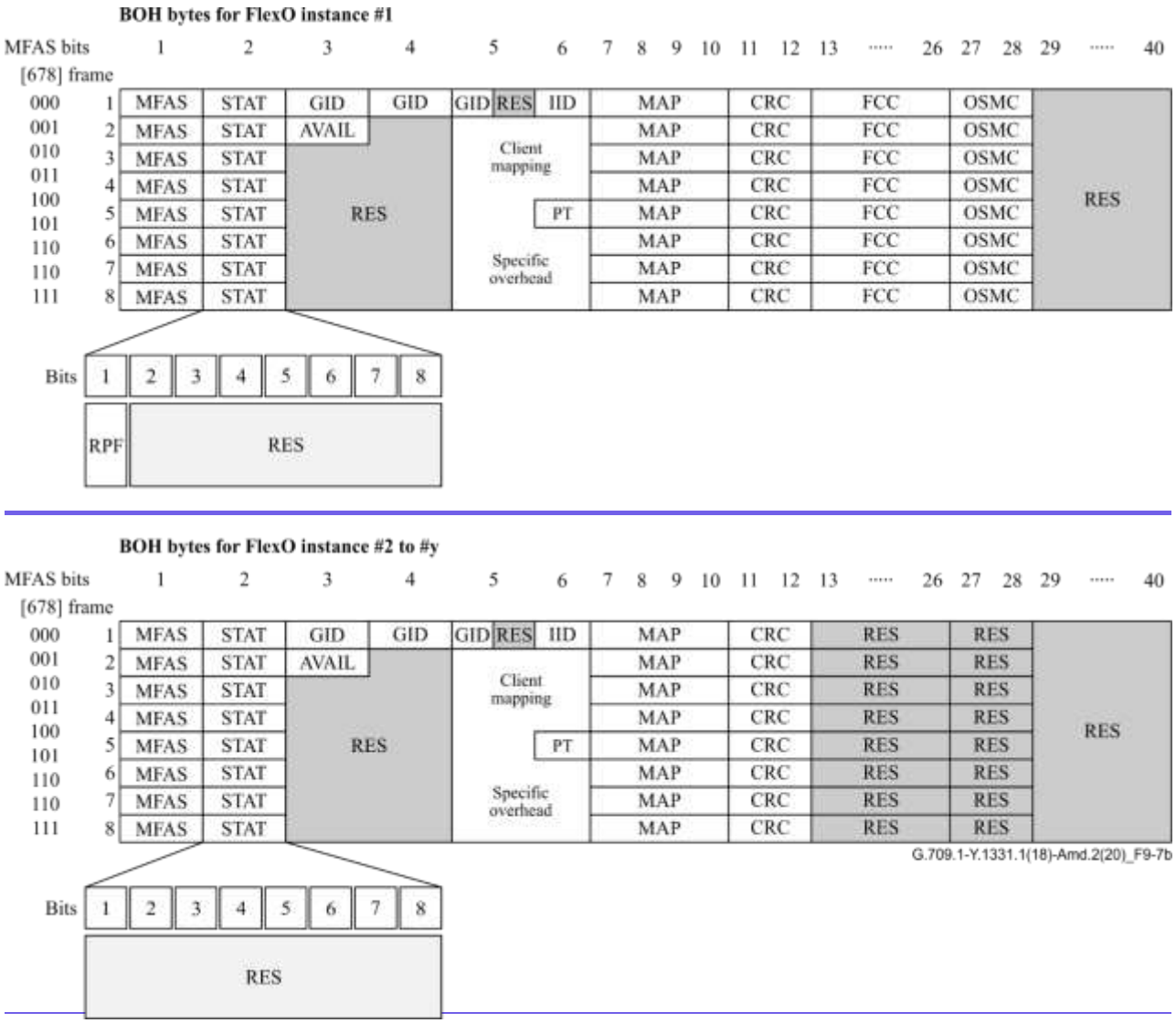

Figure 9-7b – Blank figure (deleted by Amd.4)~~FlexO OH structure of the y equipped FlexO instances of a FlexO-x <fec> interface (x = {2,4} and y ≤ x)~~

The FlexO BOH area contains the following subfields (see Figure 9-7a):

- multi-frame alignment signal (MFAS)
- status (STAT) ~~– RPF is present only in the first FlexO instance of each FlexO-x <fec> interface~~
- group management overhead including:
  - group identification (GID)
  - FlexO instance identification (IID)
  - FlexO map (MAP)
- payload overhead including:
  - payload type (PT)
  - client mapping specific
  - OTUC availability (AVAIL) – defined in clause 9.2.6.1~~Unused and only required for 100G interfaces.~~
- cyclic redundancy check (CRC)

– FlexO management communication channel (FCC1) – Present only in the first FlexO instance of each FlexO-x(e)-<fec> interface

– bits reserved for future international standardization (RES)

– OTN synchronisation message channel (OSMC)

9.2.1 Multi-frame alignment signal (MFAS)

An 8-bit (1 byte) multi-frame alignment signal field is provided and incremented in every FlexO frame. This MFAS field counts 0x00 to 0xFF and provides a 256-frame FlexO multi-frame. This central multi-frame is used to lock 2-frame, 4-frame, 8-frame, 16-frame, 32-frame, etc. multi-frame structures of overhead and payload structure to the principal frame. The MFAS sequence is shown in Figure 9-8.

Figure 9-8 – Multi-frame alignment signal overhead

The MFAS field is located in all FlexO frames, in overhead byte 1 immediately following the AM.

9.2.2 Group management overhead

9.2.2.1 Group identification (GID)

A 20-bit (2.5 bytes) FlexO group identification (GID) field is provided to indicate the interface group instance that the FlexO-x(e)-<fec> interface is a member of. The GID provides the ability to check at the receive side that the interface belongs to the intended FlexO group.

The GID field is located in frame 1, in overhead bytes 3, 4 and 5.

The same FlexO group identification value is used in both directions of transport.

Non-zero values for GID are valid and the val~~u~~"e-"of "0" is reserved for this field.

A FlexO-x(e)<fec> interface that is not part of any group has its GID value set to "0".

9.2.2.2 FlexO instance identification (IID)

A FlexO-x(e)-<fec>-m interface group is composed of m FlexO-x(e)-<fec> interfaces, also referred to as members. An 8-bit (1 byte) IID field is provided to uniquely identify each FlexO instance of a group and the order of each instance and member in the group. This information is required in the reordering process.

The IID values of the interfaces in a FlexO group are not necessarily arranged consecutively. The IID values indicate the order of the interfaces within the FlexO group, from low to high. The first FlexO-x(e)-<fec> interface in the group is the one with the lowest IID value(s).

The FlexO instances identification value(s) (IID) within a ~~FlexO-x~~FlexO-x(e)-<fec> interface shall all be larger than the IID value(s) within the~~-~~ FlexO-x(e)-<fec> interface in the group, and shall all be smaller than the IID value(s) within the next FlexO-x(e)-<fec> interface in the group.

The IID field is located in frame 1, in overhead byte 6. The values "0" and "255" are reserved for this field.

The same FlexO instance identification value is used in both directions of transport.

A ~~FlexO-x~~FlexO-x(e)-<fec> interface that is not part of any group has its FlexO IID value(s) default to "0".

9.2.2.3 FlexO map (MAP)

A 256-bit (32 bytes) field is provided to indicate the members belonging to the group. Each bit in the field, is set to "1" indicating that an instance is part of the group. The bit position of the MAP corresponds to the IID set for the member ~~FlexO-x~~FlexO-x(e)-<fec> interface, with the most significant bit (MSB) corresponding to lowest numbered IID. The remaining unused fields in the MAP are set to "0". The full MAP is sent and received on all members of the group.

The MAP field is located in all frames of all FlexO instances in a group, in overhead bytes 7, 8, 9 and 10. As shown in Figure 9-9, bit 2 of overhead byte 7 in frame 1 is associated with IID#1 and bit 7 of overhead byte 10 in frame 8 is associated with IID #254. Additionally, bit 1 of overhead byte 7 in frame 1, and bit 8 of overhead byte 10 in frame 8 are reserved.

MAP bytes																															
Frame	7								8								9								10							
1	RES	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
2	32	33	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·
3	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·
4	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·
5	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·
6	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·
7	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·
8	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	·	245	246	247	248	249	250	251	252	253	254	RES

G.709.1-Y.1331.1(18)-Amd.1(19)_F9-9

Figure 9-9 – FlexO MAP field

9.2.3~~-~~ Clause intentionally left blank

9.2.4 Clause intentionally left blank

9.2.5 Status (STAT)

An 8-bit (1 byte) field, as shown in Figure 9-10, is provided for general purpose status indication for the FlexO instance.

– Remote ~~PHY Fault~~fault (RF)

– Maintenance (MNT)

– Reserved (RES)

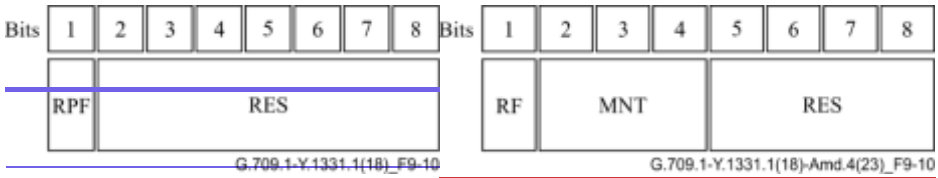

Figure 9-10 – FlexO BOH STAT field

The STAT field is located in all frames, in overhead byte 2 as shown in Figure 9-7a.

NOTE – Implementations developed prior to Edition 2.5 of this Recommendation do not support the maintenance (MNT) field; those bits are Reserved. Previous editions also only have RPF field in the first instance, and this has been repurposed in Edition 2.5 to the RF field in all instances.

9.2.5.1 Remote ~~PHY~~ fault (R~~P~~F)

For section monitoring, a single bit remote ~~PHY~~ fault (R~~P~~F) indication conveys the signal fail status detected at the remote FlexO sink function in the upstream direction.

R~~P~~F is set to "1" to indicate a remote ~~PHY~~ fault/defect indication; otherwise, it is set to "0".

NOTE – Editions prior to 2.5 of this Recommendation referred to this field as remote PHY fault (RPF).

~~The RPF field is located in bit 1 of the STAT field as shown in Figure 9-10.~~

9.2.5.2 Reserved (RES)

~~Seven~~ Four bits of the STAT byte are reserved for future international standardization as shown in Figure 9-10. These bits are set to "0".

9.2.5.3 Maintenance (MNT)

Three bits of the STAT byte are used for signalling maintenance states.

– 000 – Normal operation

– 111 – AIS

– 101 – LCK

NOTE – 100 value is reserved due to FlexOsec squelch pattern.

LCK and AIS definitions and behaviour are the same as [ITU-T G.709]. An alarm indication signal (AIS) is a signal sent downstream as an indication that an upstream defect has been detected. An AIS signal is generated in an adaptation sink function. An AIS signal is detected in a trail termination sink function to suppress defects or failures that would otherwise be detected as a consequence of the interruption of the transport of the original signal at an upstream point. A locked (LCK) is a signal sent downstream as an indication that upstream the connection is "locked", and no signal has passed through.

LCK is specified as a repeating "0101 0101" pattern and AIS is specified as a repeating “1111 1111” in the entire FlexO payload and BOH, which excludes the AM and EOH fields (see Figure 9-10a).

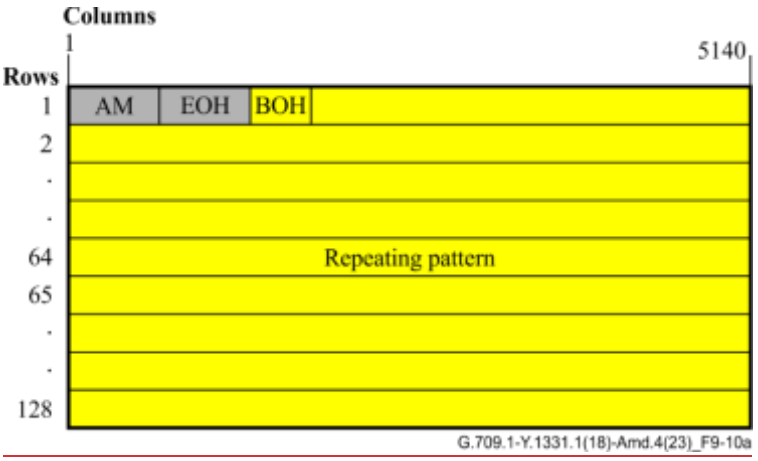

Figure 9-10a – AIS/LCK squelch for FlexO

In addition, the LCK and AIS for FlexO signals are extended with BOH such as MFAS, GID, IID, MAP, AVAIL, STAT, OSMC, FCC1 and/or the CRC overhead before it is presented at the OTN interface. This is dependent on the functionality between the LCK and AIS insertion points, and the OTN interface. The presence of LCK and AIS is detected by monitoring the MNT bits in the STAT overhead field.

9.2.6 Payload overhead

The FlexO payload overhead consists of: OTUC availability (AVAIL), payload type (PT) and client mapping specific overhead as shown in Figure 9-7a~~The FlexO payload overhead consists of: OTUC availability (AVAIL), payload type (PT) and overhead associated with the mapping of client signals into the FlexO payload. The FlexO PT and client mapping related overhead locations are shown in Figure 9-7~~.

9.2.6.1 OTUC availability (AVAIL)

The AVAIL field is unused and should be set to a value of 1 for FlexO-1-RS 100G interfaces. For other ~~x ≠ 1 interface rates,~~cases it is reserved.

The AVAIL field is located in frame 2, in overhead byte 3.

9.2.6.2 Payload type (PT)

A one-byte FlexO payload type signal is defined to indicate the composition of the FlexO payload signal. The PT field is located in frame 5, in basic overhead byte 6 in all n FlexO instances. The code points are defined in Table 9-4.

Table 9-4 – FlexO payload type code points

MSB 1 2 3 4	LSB 5 6 7 8	Hex code (Note 1)	Interpretation
0 0 0 0	0 0 0 0	00	Bit synchronous OTUC mapping, see clause 10
0 0 0 0	0 0 0 1	01	Experimental mapping (Note 2)
0 0 0 0	0 0 1 0	02	GMP based OTUC mapping for OTUCn multiplexing for FlexO-x-<fec> interfaces, see [ITU-T G.709.3]
0 0 0 0	0 1 0 0	04	Reserved for FlexOsec SquelchText value
0 0 0 0	0 1 0 1	05	GMP based Ethernet mapping for FlexO-xe-<fec> interfaces
0 1 0 0	0 0 0 0	40	Reserved OIF 800ZR mapping and multiplexing of Ethernet clients
0 1 0 0	0 0 0 1	41	Reserved OIF 800ZR PRBS test pattern
0 1 0 1	0 1 0 1	55	Reserved for STAT LCK maintenance signal
1 0 0 0	x x x x	80-8F	Reserved codes for proprietary use (Note 3)
1 1 1 1	1 1 1 0	FE	PRBS test pattern, see clause 10.3
1 1 1 1	1 1 1 1	FF	Reserved for ~~future~~ STAT AIS maintenance signal~~s~~

NOTE 1 – There are 235 spare codes left for future international standardization. Refer to Annex A of [b-ITU-T G.806] for the procedure to obtain one of these codes for a new payload type.

NOTE 2 – Value "01" is only to be used for experimental activities in cases where a mapping code is not defined in this table. Refer to Annex A of [b-ITU-T G.806] for more information on the use of this code.

NOTE 3 – These 16 code values will not be subject to further standardization. Refer to Annex A of [b-ITU-T G.806] for more information on the use of these codes.

9.2.6.3 Client specific overhead allocation

~~Thirteen~~ Fourteen bytes are reserved in the FlexO basic overhead for the client mapping specific overhead. These bytes are located in rows 2 to 8, basic overhead byte 5; rows 2 to 4 and 6 to 8, basic overhead byte 6; and row 8, basic overhead byte 3.~~These bytes are located in rows 2 to 8, basic overhead byte 5 and rows 2 to 4 and 6 to 8, basic overhead byte 6.~~

The use of these bytes depends on the specific client signal mapping and is activated per PT configuration (see clause 10 and [ITU-T G.709.3]). ~~There are no ITU-T G.709.1 mappings that make use of these bytes.~~

9.2.7 Cyclic redundancy check (CRC)

The CRC-16 (2 bytes) is located in overhead bytes 11 and 12 of each FlexO frame. The CRC protects the integrity of the OH fields in bytes 2 to 10 and excludes the MFAS, OSMC and FCC1 fields. The CRC-16 uses the $G(x) = x^{16} + x^6 + x^5 + x^3 + 1$ generator polynomial and is calculated as follows:

1) The overhead bytes 2 to 10 of the OH frame are taken in network byte order, most significant bit first, to form a 72-bit pattern representing the coefficients of a polynomial $M(x)$ of degree 71.
2) $M(x)$ is multiplied by x^{16} and divided (modulo 2) by $G(x)$, producing a remainder $R(x)$ of degree 15 or less.
3) The coefficients of $R(x)$ are considered to be a 16-bit sequence, where x^{15} is the most significant bit.
4) This 16-bit sequence is the CRC-16 where the first bit of the CRC-16 to be transmitted is the coefficient of x^{15} and the last bit transmitted is the coefficient of x^0.

The demapper process performs steps 1-3 in the same manner as the mapper process, except that here, the $M(x)$ polynomial of step 1 includes the CRC-16 bits in received order and has degree 87. In the absence of bit errors, the remainder shall be 0.

9.2.8 FlexO management communications channel (FCC1)

An 896-bit (112 bytes) field per multi-frame is provided for a ~~FlexO-x~~FlexO-x(e)-<fec> interface management communications channel. As shown in Figure 9-11, these fields are allocated across all 8 frames of the multi-frame. This provides a clear channel. Format and content of the management channel is outside the scope of this recommendation.

NOTE – The FCC1 is intended for interface management functions and is not a generic communications channel.

The FCC1 field is located in all frames, in overhead bytes 13 to 26. If unused, the management channel shall be filled with all-0s prior to scrambling. The FCC1 bytes provide a communication channel per ~~FlexO-x~~FlexO-x(e)-<fec> interface with an approximate bandwidth of ~1~~7.9~~8 Mbit/s.

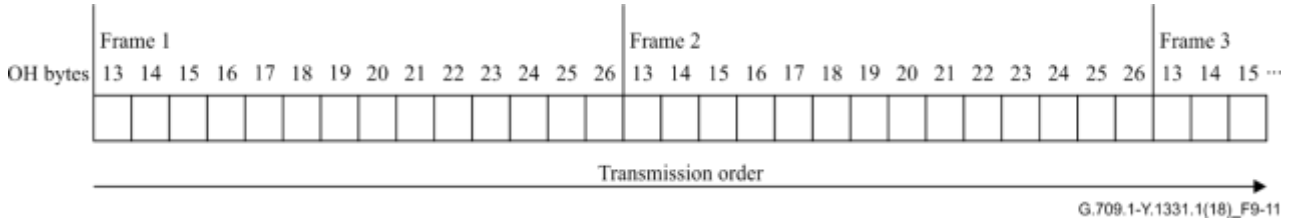

Figure 9-11 – FCC1 transmission order

NOTE – Editions prior to 2.5 of this Recommendation referred to this field as FCC.

9.2.9 FlexO reserved overhead (RES)

~~115~~112.5 bytes of the FlexO basic overhead area in the FlexO multi-frame structure are reserved for future international standardization. These bytes/bits are located in frame 1/byte 5, frame 2/byte 4, frames 3 to ~~8~~7/bytes 3 to 4, frame 8 byte 4 and frames 1 to 8/bytes 29 to 40. These bytes/bits are set to all-0s prior to scrambling.

9.2.10 OTN synchronization message channel (OSMC)

A 128-bit (16 bytes) field per multi-frame is provided for an OTN synchronization message channel (OSMC). As shown in Figure 9-7a, these are allocated across all eight frames of the multi-frame. This field provides a clear channel, to transport synchronization status message (SSM) and precision time protocol (PTP) messages.

The OSMC is only defined on the first FlexO instance (lowest IID value) of a ~~FlexO-x~~FlexO-x(e)-<fec>-m interface group.

The OSMC field is located in all frames, in overhead bytes 27 and 28. If unused, the OTN synchronization message channel bytes shall be filled with all-0s prior to scrambling. The OSMC bytes are combined to provide a messaging channel, as illustrated in Figure 9-12, with an approximate bandwidth of 2.56 Mbit/s per 100G interface.

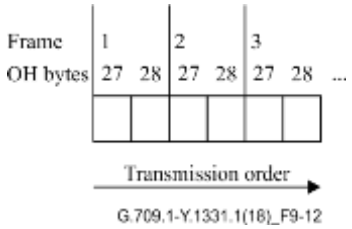

Figure 9-12 – OSMC transmission order

The SSM and PTP messages within a FlexO instance are encapsulated into GFP-F frames as specified in [ITU-T G.7041]. PTP event messages are timestamped and after encapsulation into GFP-F frames, they are inserted into the OSMC as specified in this clause. GFP-F encapsulated SSM messages (and PTP non-event messages) are inserted into the OSMC at the earliest opportunity. GFP idle frames may be inserted between successive generic framing procedure (GFP) frames.

The mapping of GFP frames is performed by aligning the byte structure of every GFP frame with the byte of the OSMC overhead field. Since the GFP frames are of variable length and may be longer than 16 bytes, a GFP frame may cross the FlexO multi-frame boundary.

9.2.10.1 Generation of event message timestamp

The message timestamp point [ITU-T G.8260] for a PTP event message transported over the OSMC shall be the 32-frame multi-frame event (corresponding to MFAS[4:8] = 00000) preceding the beginning of the GFP frame, in which the PTP event message is carried. Since the GFP frames may be longer than 64 bytes, a frame may cross the FlexO 32-frame multi-frame boundary. Figure 9-13 shows a timestamp diagram example and the relationship to the GFP frames (PTP message).

All PTP event messages are timestamped on egress and ingress interfaces. The timestamp shall be the time at which the event message timestamp point passes the reference plane [ITU-T G.8260] marking the boundary between the PTP node (i.e., OTN node) and the network.

Event message timestamps are generated at the FlexO Access Point. The message timestamp point is specified below as the 32-frame FlexO multi-frame event corresponding to MFAS[4:8] = 00000. For this application, the FlexO multi-frame event is defined as when the first bit of the first

alignment marker, corresponding to MFAS[4:8] = 00000 frame, on a lane crosses between the PTP node (i.e., OTN node) and the network (i.e., the analogous point to Ethernet MDI). In the case of a multi-lane PHY, the PTP path data delay is measured from the beginning of the alignment marker at the reference plane, which is equivalent to Ethernet MDI of the lane with the maximum media propagation delay. In practice:

– On egress interfaces, since the alignment markers for all lanes are transmitted at the same time conceptually, any alignment marker can be used for timestamping.

– On ingress interfaces, alignment markers are present in all the lanes, but different lanes may be skewed from each other. The last received alignment marker across all the lanes shall be used for timestamping.

NOTE 1 – The first byte of a GFP (PTP event message) frame is inserted into the FlexO OSMC between 4 and 31 frames after the 32-frame multi-frame boundary.

NOTE 2 – The guard band of four frames is defined to simplify implementation.

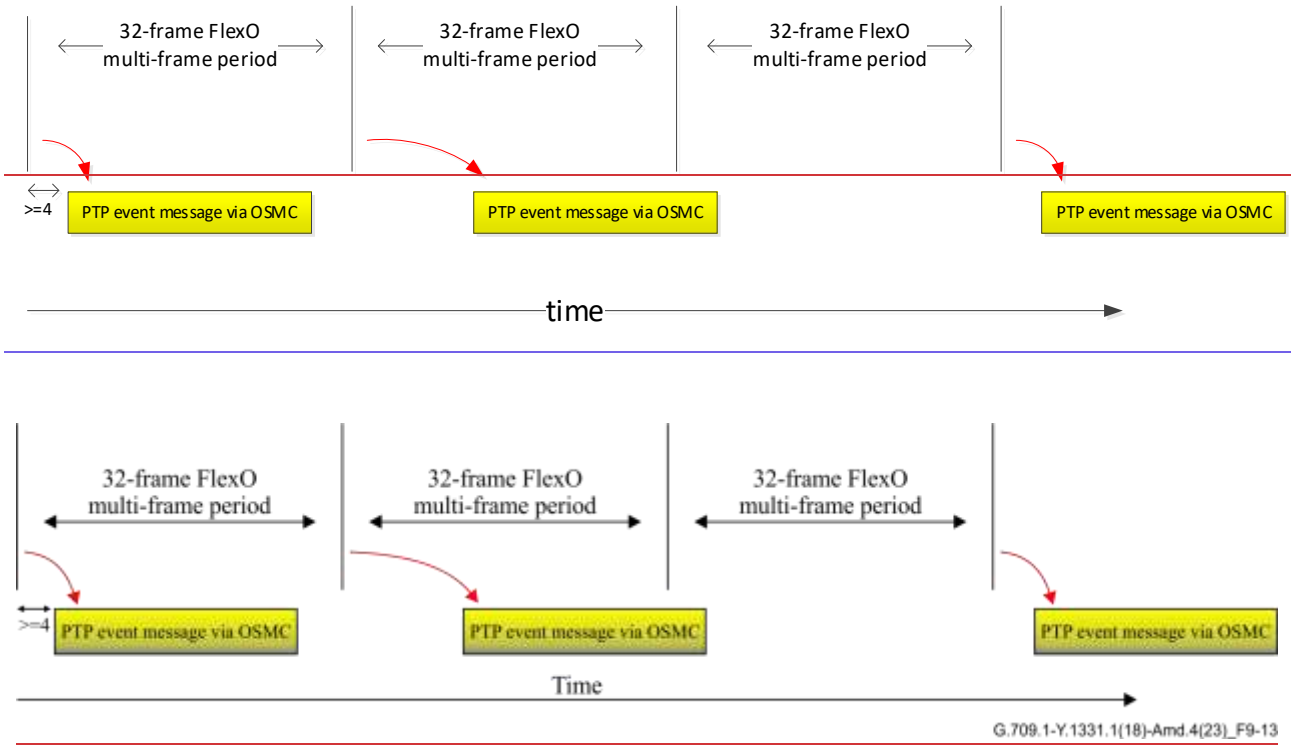

Figure 9-13 – Timing diagram example for OSMC

NOTE 3 – This time synchronization over FlexO-x-RS interface implementation does not generate event message timestamps using a point other than the message timestamp point [ITU-T G.8260].

In this time synchronization over FlexO-x-RS interface implementation, the timestamps are generated at a point removed from the reference plane. Furthermore, the time offset from the reference plane is likely to be different for inbound and outbound event messages. To meet the requirement of this clause, the generated timestamps should be corrected for these offsets. Figure 19 in [b-IEEE 1588] illustrates these offsets. Based on this model, the appropriate corrections are as follows:

<egressTimestamp> = <egressMeasuredTimestamp> + egressLatency

<ingressTimestamp> = <ingressMeasuredTimestamp> – ingressLatency

where the actual timestamps <egressTimestamp> and <ingressTimestamp> measured at the reference plane are computed from the detected, i.e., measured, timestamps by their respective

latencies. Failure to make these corrections results in a time offset between the slave and master clocks.

The PTP timestamp is associated with the first FlexO instance (lowest IID value) of a ~~FlexO-x~~FlexO-x(e)-<fec>-m interface group.

9.3 Extended overhead (EOH) description

The FlexO EOH area is contained in the 480 bits (60 bytes) following the FlexO frame AM area. The EOH overhead does not use the 8-frame multi-frame. The EOH structure is shown in Figure 9-14.

NOTE – FlexO extended overhead was specified as FlexO PAD in Editions 1.0 to 2.2 of this Recommendation.

Extended overhead that is not used for a specific application contains the all-0's pattern.

FlexO extended overhead applications include FlexOfec~~ and~~, FlexOsec and regen. Further applications may be defined in future editions of this Recommendation.

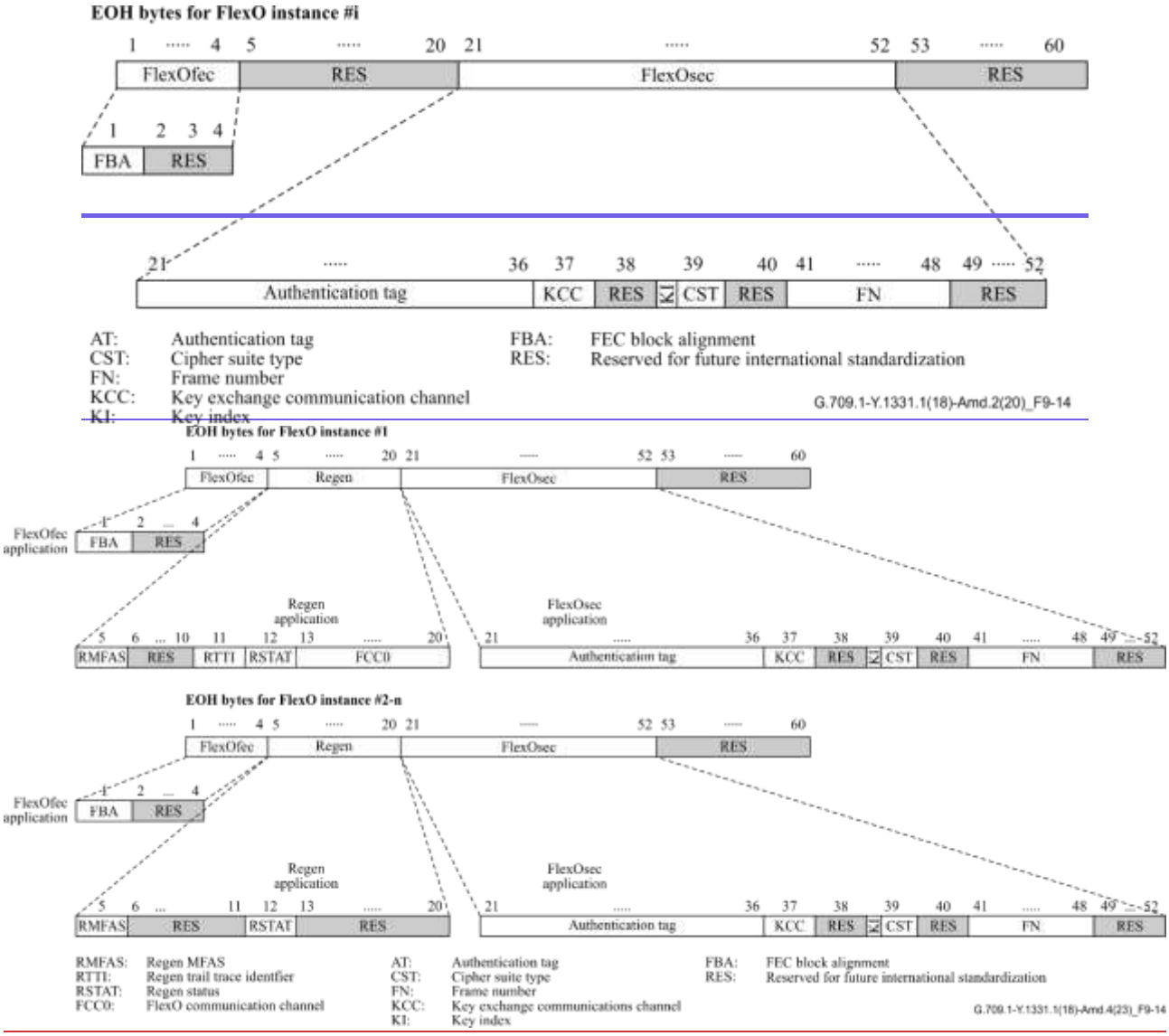

Figure 9-14 – FlexO extended overhead

9.3.1 FlexOfec overhead

FlexOfec overhead application in this Edition is associated with the staircase FEC (SC FEC) specified in [ITU-T G.709.3].

9.3.1.1 Staircase FEC block alignment (FBA) field

Figure 9-14 shows the "FBA" overhead byte in byte 1 of the extended overhead area. Refer to [ITU-T G.709.3] for the FBA specification.

9.3.2 FlexOsec overhead

FlexOsec provides secure communications between two FlexO interfaces which are interconnected by an unsecured fibre, a point-to-point optical line system or an optical network. An authenticated and authorized FlexO security entity within each FlexO interface uses the unsecured transmission through the fibre, point-to-point optical line system or optical network to provide the secure transmission to its FlexO client.

The FlexOsec overhead is specific and defined for all FlexO instances within a FlexO group interface. The FlexOsec overhead is illustrated in Figure 9-14 and contains the following fields:

– Authentication tag (AT)

– Frame number (FN)

– Key index (KI)

– Cipher suite type (CST)

– Key exchange communication channel (KCC)

– Bits reserved for future international standardization (RES)

9.3.2.1 Authentication tag (AT)

A 128-bit (16 byte) authentication tag field is provided to secure the integrity of transport of the bits in a FlexO frame. The cryptographic algorithms used to generate the integrity value and the various portions of the authenticated FlexO frame depend on the cipher suite type used. Additional details can be found in Annex B.

The AT overhead field is used individually per FlexO instance within a group interface. An authentication tag calculated over (portions of) a FlexO instance #i frame #j is inserted in the following FlexO instance #i frame #j+1.

The AT field is located in bytes 21 to 36 of the extended overhead area.

9.3.2.2 Frame number (FN)

A 64-bit (8 byte) frame number field is provided to synchronize the invocation counters on both ends of a FlexOsec connection. The use of FN as invocation counter and initialization vector (IV) construction is specific to the cipher suite type and further defined in Annex B. An IV is a nonce that is associated with an invocation of authenticated encryption on a particular plaintext and additional authenticated data (AAD).

The FlexOsec frame number is also used to create a 4-frame FlexOsec multi-frame which is separate to the FlexO MFAS multi-frame. FN is applicable to the current FlexO frame. FN increments by 1 on every FlexO frame, however on key change events FN is assumed to be reset to 0.

The FN field is located in bytes 41 to 48 of the extended overhead area.

9.3.2.3 Key index (KI)

A 2-bit key index field is provided for an in-band mechanism to coordinate use of keys on both ends. At the source, the KI value increments on key change/roll events. The value of KI is constant across 4-frame FlexOsec multi-frames and increments on multi-frame boundaries as defined by FN [63 ,64] = 00. The value of KI in the current multi-frame #k indicates the key to be used starting at the next multi-frame #k+1.

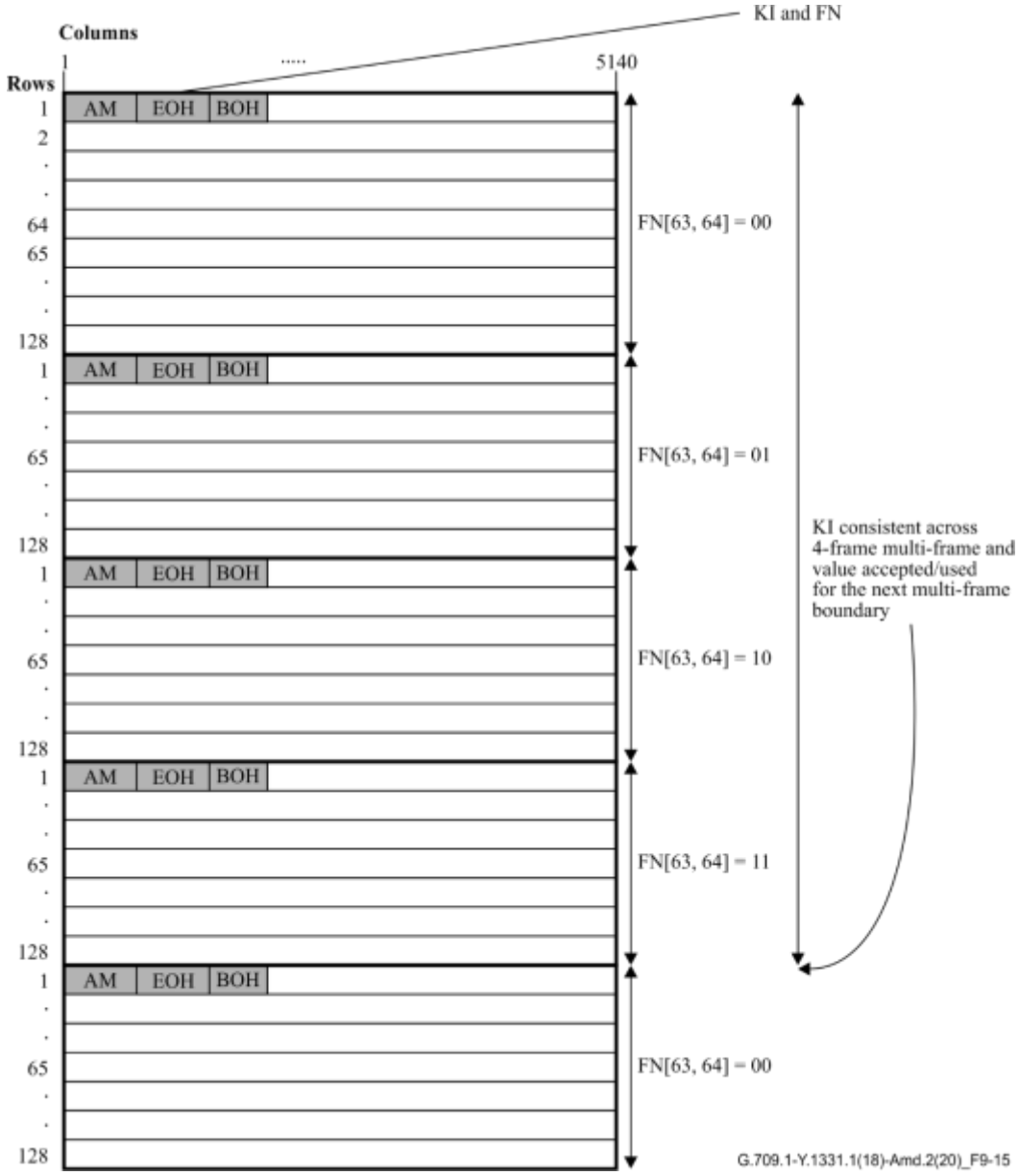

Figure 9-15 – Key index boundaries

The key index is used to select among 4 possible keys as shown in Table 9-5.

Table 9-5 – Key index coding

KI bits [12]	Interpretation
00	Key #0
01	Key #1
10	Key #2
11	Key #3

The KI field is located in bits 1 and 2 of byte 39 of the extended overhead area.

9.3.2.4 Cipher suite type (CST)

A 6-bit cipher suite type field is provided to identify and distinguish different types of ciphers (including absence of cipher), profiles or applications. The code points are defined in Table 9-6. Code point value 000000 indicates that there is no source FlexOsec.

The CST field is located in bits 3 to 8 of byte 39 of the extended overhead area.

Table 9-6 – Cipher suite type code points

CST bits [123456]	Interpretation
0 0 0 0 0 0	*No source FlexOsec*
0 0 0 0 0 1	GCM-AES-256 FlexOsec without OH encryption. Refer to Annex B.1.
0 0 0 0 1 0 – 1 1 0 1 1 1	Codepoints reserved for future standardized cryptographic cipher suites (defined by national or international standards bodies or government agencies) for use with FlexO.
1 1 1 0 0 0 – 1 1 1 1 1 0	*Reserved codes for proprietary use (Note-)*
1 1 1 1 1 1	*Reserved for future maintenance signal*
NOTE – These 7 code values will not be subject to further standardization.	

9.3.2.5 Key exchange communication channel (KCC)

An optional 8-bit (1 byte) key exchange communication channel field is provided to exchange key agreement protocols in-band using FlexO overhead.

The KCC field is located in byte 37 of the extended overhead area.

NOTE 1 – Key agreement protocols may be vendor, operator or user specific for the case that multi-vendor, multi-operator or multi-user interoperability is not required.

NOTE 2 – KCC is only present in the first FlexO instance of each ~~FlexO-x~~FlexO-x(e)-<fec> interface.

9.3.2.6 Reserved (RES)

6 bytes of the FlexOsec overhead area are reserved for future international standardization. These bytes/bits are located in bytes 38, 40, 49, 50, 51 and 52. These bytes/bits are set to all-0s.

9.3.3 FlexO regen overhead

Regen overhead is used to enable FlexO regen functions and is terminated on every interface.

NOTE – Implementations developed prior to Edition 2.5 of this Recommendation do not support the regen overhead and associated functions.

The regen overhead is illustrated in Figure 9-14 and contains the following fields:

– Regen multi-frame alignment signal (RMFAS)

– Regen status (RSTAT)

– Regen trail trace identifier (RTTI)

– FlexO regen communication channel (FCC0)

9.3.3.1 Regen multi-frame alignment signal (RMFAS)

An 8-bit (1 byte) regen multi-frame alignment signal field is provided and incremented in every FlexO frame. This RMFAS field counts 0x00 to 0xFF and provides a 256-frame FlexO multi-frame. This multi-frame is used to lock 2-frame, 4-frame, 8-frame, 16-frame, 32-frame, etc. multi-frame structures of overhead to the FlexO frame. The RMFAS sequence is identical to what is shown in Figure 9-8 for the MFAS. The RMFAS (EOH) and MFAS (BOH) increment independently.

9.3.3.2 Regen status (RSTAT)

An 8-bit (1 byte) field, as shown in Figure 9-16, is provided for general purpose status indication.

– Remote fault indication (RF)

– Local and remote degrades (LD, RD)

– Reserved (RES)

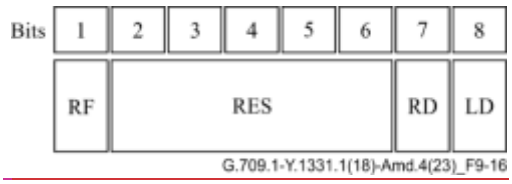

Figure 9-16 – FlexO EOH RSTAT field

The RSTAT field is located in all frames, in EOH byte 12 as shown in Figure 9-14.

9.3.3.2.1 Remote fault indication (RF)

For regen section monitoring, a single bit remote fault indication (RF) conveys the signal fail status detected at the remote FlexO sink function in the upstream direction.

RF is set to "1" to indicate a remote defect indication; otherwise, it is set to "0".

9.3.3.2.2 Degrade indication (LD/RD)

The 2-bit link degrade indication field is defined to indicate the quality of the FlexO-x(e)-<fec> interface. Local and remote degrade (LD and RD) fields are asserted and set to "1" on detection of terminated FlexO-x(e)-<fec> FEC degrade; otherwise they are set to "0". LD is propagated in the forward direction in a similar manner as indicated in Annex K of [ITU-T G.709]. RD is propagated in the backwards direction and only covers a single FlexO-x(e)-<fec> interface span, which differs from Annex K of [ITU-T G.709].

9.3.3.2.3 Reserved (RES)

Five bits of the STAT byte are reserved for future international standardization as shown in Figure 9-16. These bits are set to "0".

9.3.3.3 Regen trail trace identifier (RTTI)

For FlexO section monitoring, a one byte trail trace identifier (RTTI) overhead is defined to transport the 64-byte RTTI signal specified in clause 15.2 and Figure 15-4 of [ITU-T G.709].

The FlexO-x(e)-<fec> interface contains one RTTI overhead in the first instance as shown in Figure 9-14.

The 64-byte RTTI signal shall be aligned with the FlexO regen multi-frame (RMFAS). Byte 0 of the 64-byte RTTI signal shall be present at FlexO regen 64 multi-frame using RMFAS 6 MSBs xx00 0000.

9.3.3.4 FlexO regen communication channel (FCC0)

A 64-bit (8 bytes) field per frame is provided for a FlexO-x(e)-<fec> interface regen management communications channel. As shown in Figure 9-14, these fields are located in the EOH in byte locations 13 to 20.

NOTE – The FCC0 is intended for interface management functions and is not a generic communications channel.

The FCC0 bytes provide a communication channel per FlexO-x(e)-<fec> interface with an approximate bandwidth of ~10 Mbit/s.

9.4 Frame alignment (FA)

The frame alignment word is used for long reach FlexO-8(e)-DO and FlexO-4(e) (QPSK). The role of the FA is to find the FlexO frame boundary. It is located in bit columns 1-480 of the first row of each frame and is protected by the line-side FEC.

Figure 9-17 illustrates the structure of the frame alignment word and encoding within each AM field of FlexO instance. The 480-bit field consists of 16 octets of FA1 in bit columns 1 to 128, 16 octets of FA2 in bit columns 129 to 256, and 224 reserved bits in bit columns 257 to 480. The FA1 and FA2 octets are shown in Table 9-7. Each of the FA1 and FA2 octets shall be transmitted most significant bit (MSB) first. The reserved bits are transmitted as all-zeros and ignored upon receipt. Frame alignment can be done across a subset of the alignment area.

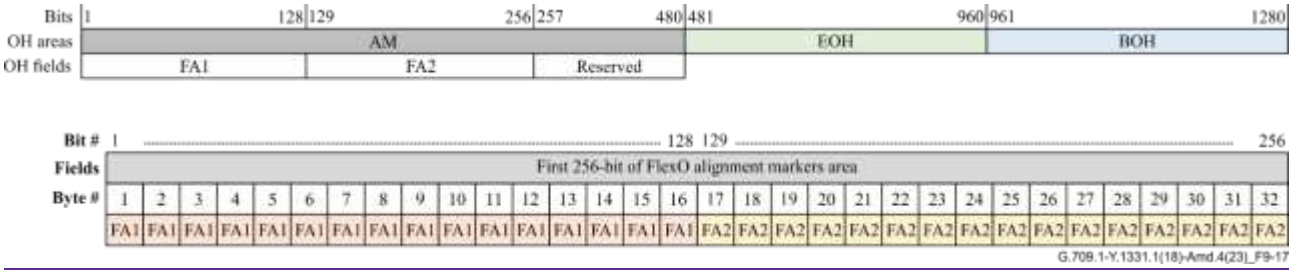

Figure 9-17 – Frame alignment word

Table 9-7 – FA encodings

Field	Value
FA1	0x09
FA2	0xD7

10 FlexO ~~Mapping~~ mapping ~~of OTUCn signal into n FlexO instances~~procedures

FlexO payload can be mapped with different clients, such as OTUCn, Ethernet and pseudo random binary sequence (PRBS).

10.1 BMP mapping of OTUCn client into FlexO-x

In the most general case, the n OTUC instances of an OTUCn are mapped to a FlexO-x-<fec>-m group of m FlexO-x-<fec> interfaces, each with a FlexO-x-<fec> interface bandwidth of ceiling (n/m) *100G.

~~In the most general case, the n OTUC instances of an OTUCn are mapped to a FlexO-x-<fec>-m group of m FlexO-x-<fec> interfaces, each with a FlexO-x-<fec> interface bandwidth of ceiling (n/m) *100G.~~

10.1.1 Distributing OTUCn and combining OTUC instances

An OTUCn frame structure is specified in clause 11.3 [ITU-T G.709] and contains n ~~synchronous~~ instances of OTUC frame structures. As shown in Figure 10-1, the FlexO source adaptation consists of splitting the OTUCn frame into n × OTUC instances. Similarly, the sink adaptation combines n × OTUC instances into an OTUCn. A single OTUC instance is then associated to a FlexO instance, and multiple FlexO instances are associated to a FlexO-x-<fec> interface depending on interface rate. Alignment and deskewing are performed on the OTUC instances.

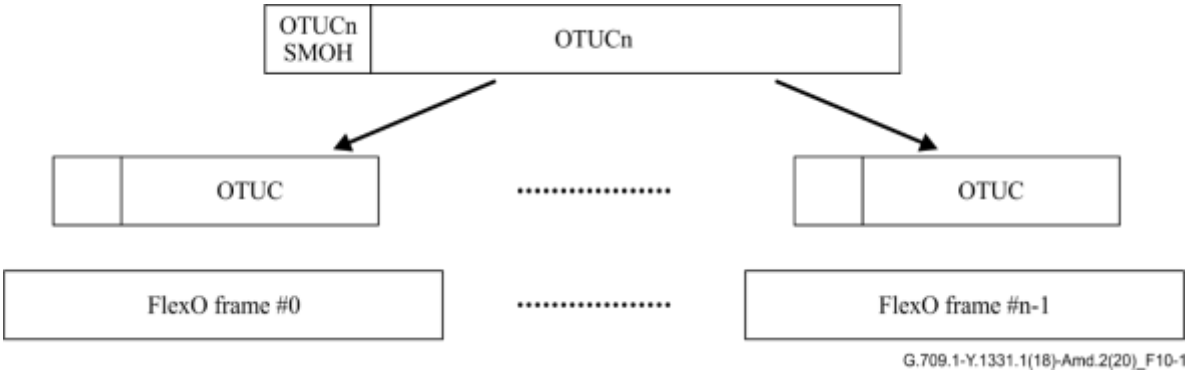

Figure 10-1 – OTUCn distributed onto n × FlexO frame instances

10.1.2 FlexO multi-frame payload

For BMP mapping procedure, fixed stuffing is used to pad the OTUCn up to a FlexO-x rate. In order to pad the payload area, an 8-frame FlexO multi-frame structure is defined. It uses the three least significant bits of the multi-frame alignment signal (MFAS) overhead to identify the eight frames within the multi-frame.

The FlexO multi-frame structure is shown in Figure 10-2. The multi-frame contains seven fixed stuff (FS) locations in the payload area of FlexO frames, each containing 1,280 bits. These fixed-stuff locations are located in row 65, columns 1 to 1,280 of the first seven frames within the multi-frame. The last frame within the multi-frame does not contain fixed stuff.

The fixed stuff bits are filled with all-0s and not checked at the receiver sink function.

The FlexO multi-frame payload, excluding the fixed stuff FS locations, consists of 5,244,160 bits (655,520 bytes) out of the total 5,263,360 bits (657,920 bytes) per FlexO multi-frame.

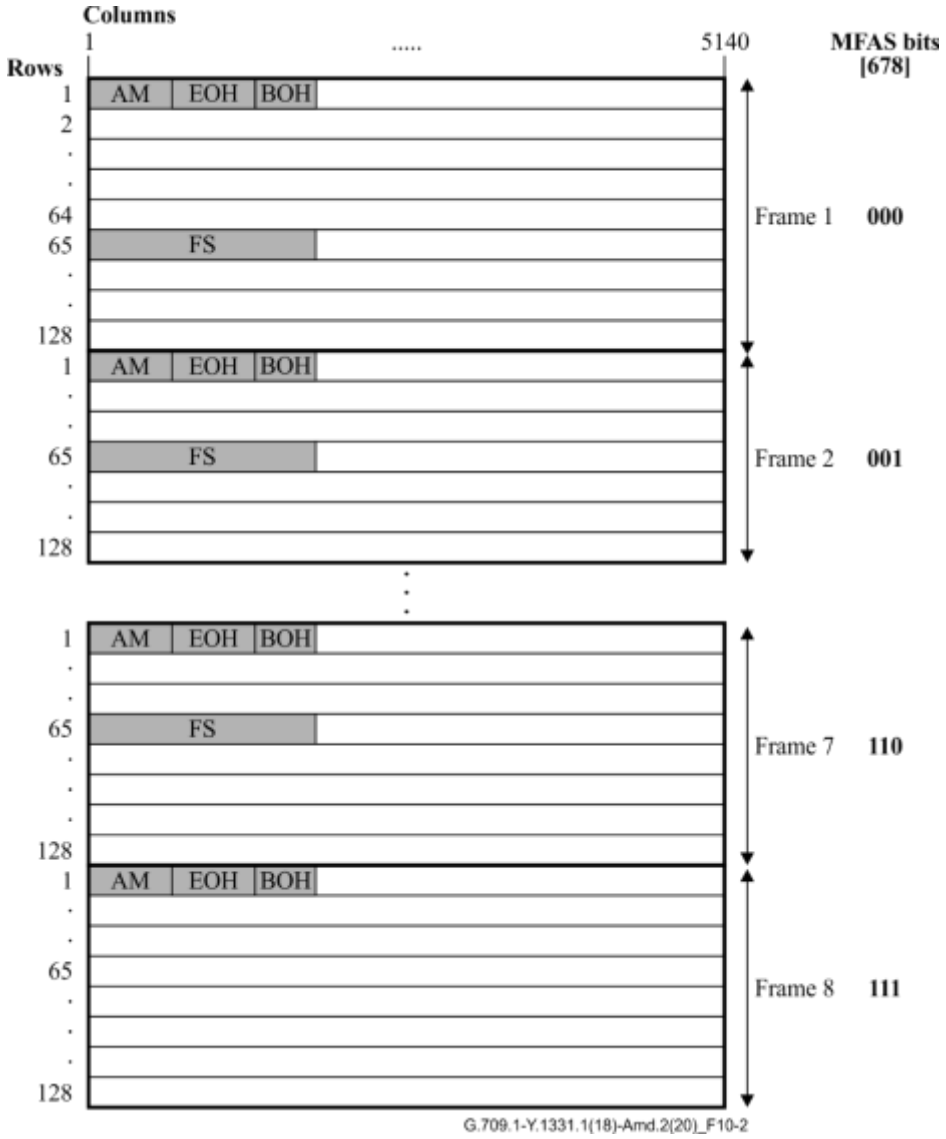

Figure 10-2 – FlexO BMP multi-frame structure

The FlexO multi-frame payload area is divided in 128-bit blocks. The 128-bit blocks are aligned to the start of a FlexO payload area (following AM, EOH and BOH). The FlexO frame payload consists of 5,120 blocks (frame #1-7 of the multi-frame, with fixed stuff payload) and 5,130 blocks (frame eight of the multi-frame, without fixed stuffing).

NOTE – This 128-bit (16-byte) word/block alignment of the 100G OTUC is analogous to the 66b block alignment of a 100G Ethernet PCS stream that is kept through the clause 91 [IEEE 802.3] adaptation process.

10.1.3 Mapping of OTUC into FlexO multi-frame payload

Groups of 128 successive bits (16 bytes) of the OTUC signal are mapped into a 128-bit block of the FlexO frame payload area using a bit-synchronous mapping procedure (BMP) control mechanism as specified in clause 17 of [ITU-T G.709]. The 128-bit group of OTUC is aligned to the OTUC frame structure.

The OTUC frame structure is floating in respect to the FlexO frame.

The serial bit stream of an OTUC signal is inserted into the FlexO frame payload so that the bits will be transmitted on the FlexO-x-<fec> interface in the same order that they were received at the input of the mapper function.

In clause 8.3, the shown bit rate ratio between FlexO frame and the OTUC client is 4112/4097.

10.1.3.1 Mapping of OTUC into FlexO frame

There exists a one-to-one relationship between an OTUC and a 100G FlexO instance. The FlexO payload area is segmented in 128-bit blocks. The OTUC is mapped in contiguous 128-bit segments.

There are (5,140*128*8 – 1,280*15) / (239*16*8*4) = 42.85 OTUC frames per FlexO multi-frame. This results in ~5 OTUC frames per FlexO frame, or a new OTUC frame every ~24 FlexO frame rows, as shown in Figure 10-3.

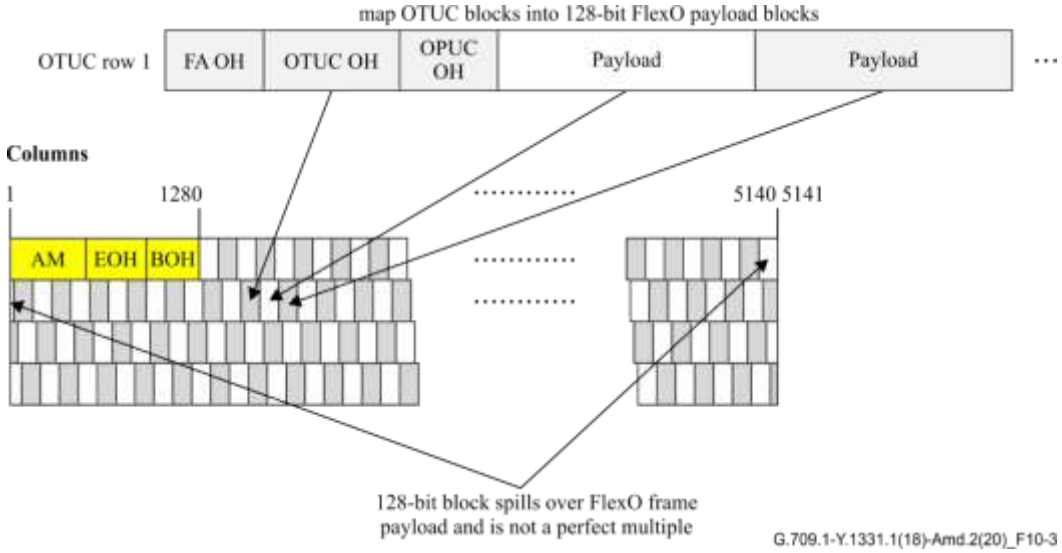

Figure 10-3 – OTUC mapped into 100G FlexO frame payload

The FlexO frame payload does not divide elegantly into 128-bit blocks in a single row. The block will spill over and cross row boundaries as shown in Figure 10-3. The 128-bit alignment is always consistent across FlexO frames and the first 128-bit block starts immediately following the overhead area.

~~The AVAIL field indicates whether an OTUC is mapped into the FlexO frame payload (set to "1") or if the FlexO payload is empty (set to "0"). Other AVAIL values are not valid for 100G FlexO-x-RS interfaces.~~

10.41.4 FlexO-x-<fec>-m group alignment and deskewing

FlexO members are identified within a FlexO-x-<fec>-m group and reordered using GID, MAP and IID FlexO BOH field. The IID sequence is used to recreate an OTUCn in proper OTUC instance order. For example, OTUC_#1 is mapped into a FlexO frame with the minimum IID number and so on.

Deskewing in the sink process is performed between OTUC frames within the group, using OTUC FAS as specified in [ITU-T G.709].

The OTUC frame skew requirements are intended to account for variations due to digital mapping and cable lengths. The skew tolerance requirement is 300 ns.

NOTE – These requirements are in line with [OIF FlexE] Low Skew applications.

10.1.5 Client mapping specific overhead

The client mapping specific overhead shown in Figure 9-7a is not used for OTUCn BMP mapping and is reserved.

10.2 GMP mapping of Ethernet client into FlexO-xe

One or more Ethernet clients can be mapped directly to n FlexO instances using generic mapping procedure (GMP). The n FlexO frames are phase-locked and multi-frame aligned. The characteristic information of each Ethernet client is a sequence of 257b blocks.

For each Ethernet client and prior to mapping, the FEC is decoded and the codewords are re-interleaved to form a stream of 257b blocks with the alignment markers removed. For 100GBASE-R clients, the BIP counters in the AMs are discarded. Because 100GBASE-R does scrambling prior to 257b transcoding, there is no descrambling performed for these clients. For 200GBASE-R and 400GBASE-R clients, the am_sf<2:0> bits are extracted from the alignment markers prior to their removal and the 257b blocks are descrambled per clause 119.2.4.3 of [IEEE 802.3].

At the demapper, the inverse processes are performed. For 200GE/400GE client types, the 257b blocks are scrambled following the procedures in clause 119.2.4.3 of [IEEE 802.3] and the am_sf<2:0> fields extracted from the received FlexO frame overhead fields are processed as described in CSTAT clause 10.2.3.3 and inserted in the appropriate locations in the AM fields. For 100GE clients the BIP counters are recomputed and inserted. For 100GE clients, no scrambling is performed (the blocks are intrinsically scrambled).

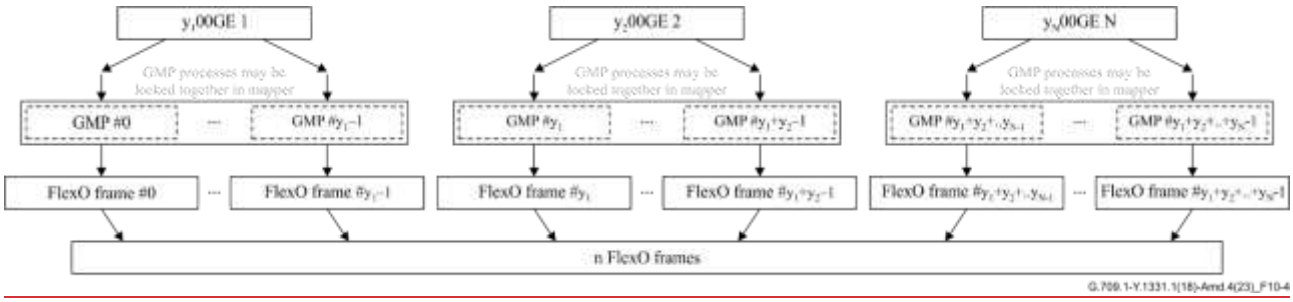

Figure 10-4 – Mapping of Ethernet clients using GMP

For 100GBASE-R (100GE) clients, the 257b stream is mapped directly into the payload area of the corresponding FlexO instance.

For 200GBASE-R (200GE) clients, the 257b stream is split on a 257b block basis, in a round-robin fashion into two 100G 257b streams which are mapped into the payload areas of the corresponding two FlexO instances.

For 400GBASE-R (400GE) clients, the 257b stream is split on a 257b block basis, in a round-robin fashion into four 100G 257b streams which are mapped into the payload areas of the corresponding four FlexO instances.

Refer to Annex C for additional Ethernet GMP procedures.

10.2.1 FlexO frame and 4-frame multi-frame payload structure

The FlexO frame payload area is divided in 257-bit payload blocks (see Figure 10-5a). A 5b padding (following AM, EOH and BOH) is used to align to 257-bit multiples. The 257-bit payload blocks are aligned to the start of a FlexO payload following the 5b padding area. The FlexO frame payload ~~consists~~contains of 2555 257-bit blocks.

NOTE – There is no fixed stuff in frames 1 to 7 of the FlexO 8-frame multi-frame in this mapping.

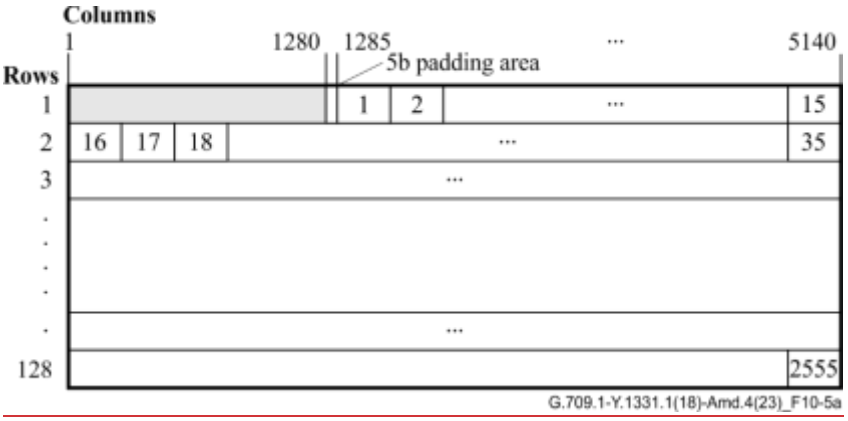

Figure 10-5a – FlexO frame showing payload with 257b blocks

The FlexO payload 4-frame multi-frame structure with 257-bit payload blocks in the payload area for the mapping of Ethernet client signals is illustrated in Figure 10-5b. This per instance server payload area consists of 10,220 257-bit blocks for Ethernet client mapping. Note that a y00GE client is GMP mapped over y phase-locked and multi-frame aligned FlexO instances, so its server payload area actually consists of 10,220 × [y × 257]-bit blocks.

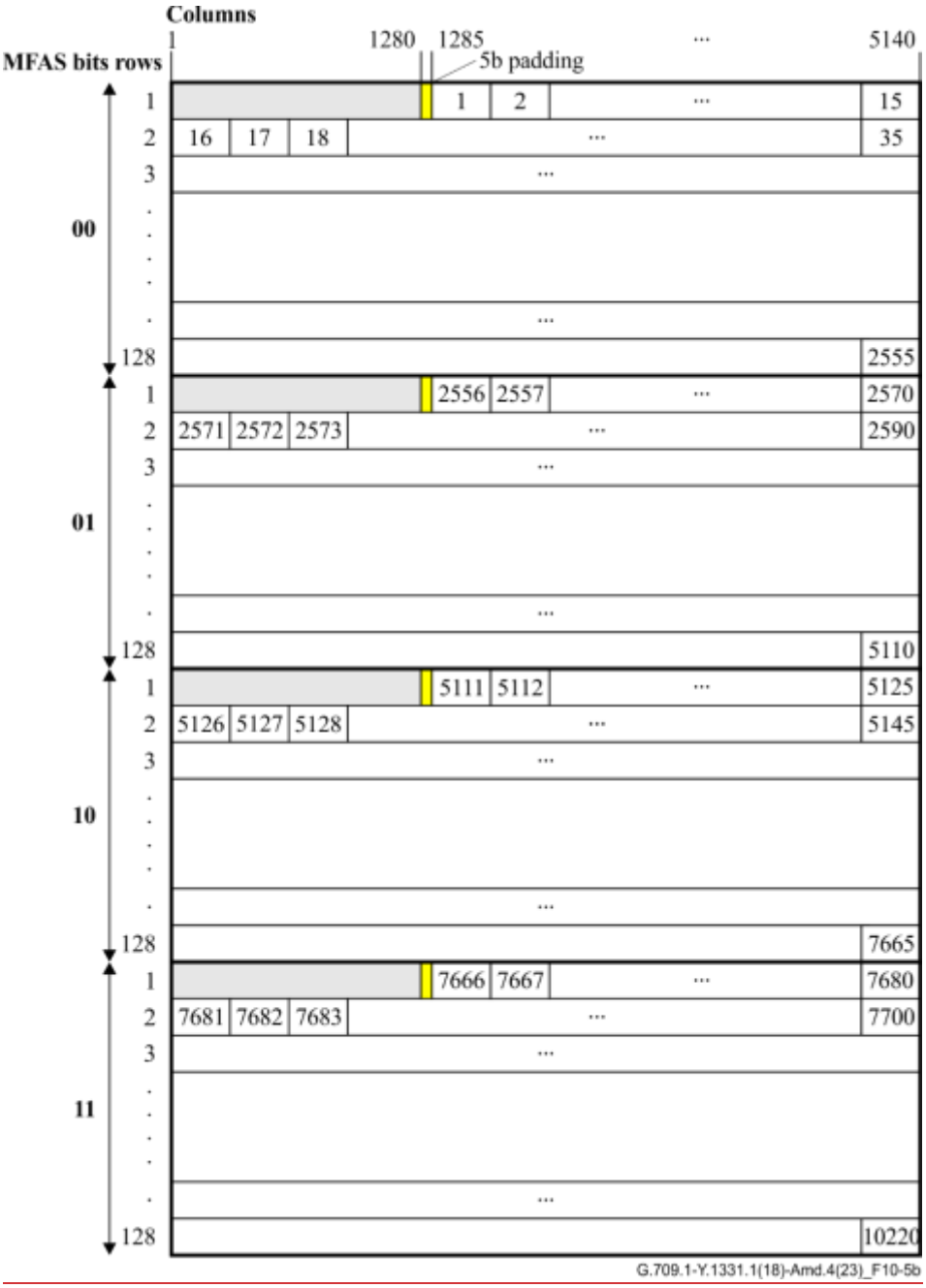

Figure 10-5b – FlexO instance payload 4-frame multi-frame structure with 257-bit payload blocks for the GMP mapping of Ethernet client signal

10.2.2 Ethernet characteristic information

In the mapping (source) direction, the decoded Ethernet client FEC code-words are re-interleaved to form a stream of 257b blocks with the alignment markers removed. For 100GBASE-R (100GE), 200GBASE-R (200GE) or 400GBASE-R (400GE) client types, the order and bit ordering of these blocks shall match the ordering in the signal prior to FEC decoding. For 100GE clients, the AM fields contain BIP counters which are discarded along with the alignment marker. The client am_sf<2:0> bits are extracted for 200GE/400GE client types prior to alignment marker removal for transmission in the overhead fields of the FlexO frame and the 257b blocks are descrambled following the procedures in clause 119.2.4.3 of [IEEE 802.3].

The inverse process is implemented in the demapping (sink) direction. For 200GE/400GE client types, the 257b blocks are scrambled following the procedures in clause 119.2.4.3 of [IEEE 802.3] and the am_sf<2:0> fields extracted from the received FlexO frame overhead fields are processed

as described in CSTAT clause 10.2.3.3 and inserted in the appropriate locations in the AM fields. For 100GE clients the BIP counters are recomputed and inserted. For 100GE clients, no scrambling is performed (the blocks are intrinsically scrambled).

10.2.3 Client mapping specific overhead

The client mapping specific overhead shown in Figure 9-7a consists of a multiplex structure identifier (MSI), justification control (JC1-JC6) and client status (CSTAT) overhead as shown in Figure 10-6. The FlexO overhead locations are present in each FlexO instance.

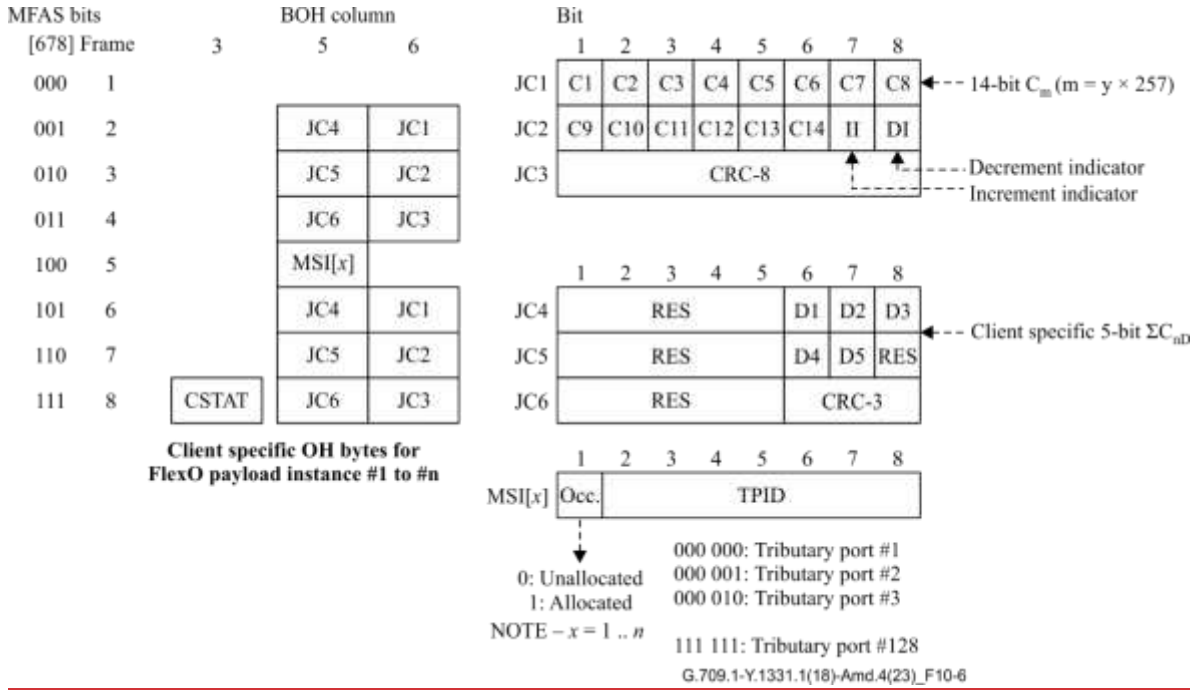

Figure 10-6 – Client mapping specific overhead for mapping Ethernet to FlexO-xe

10.2.3.1 FlexO multiplex structure identifier (MSI)

The FlexO multiplex structure identifier (MSI) overhead is located in frame 5, in overhead byte 5 in all n FlexO frames, as illustrated in Figure 10-7. The MSI indicates the Ethernet content of each FlexO instance payload. One byte is used for each FlexO instance.

– The FlexO occupation (OCC) bit 1 indicates if the FlexO instance payload is allocated or unallocated.

– The tributary port identifier (TPID) in bits 2 to 8 indicates the tributary port number of the Ethernet client which is being transported in this FlexO instance; Ethernet tributary ports are numbered 1 to 128. The value is set to all-0s when the occupation bit has the value 0 (FlexO instance is unallocated).

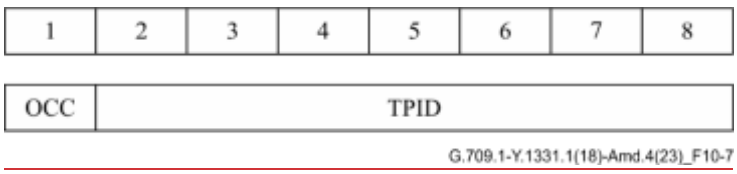

Figure 10-7 – Ethernet GMP MSI

10.2.3.2 FlexO justification overhead (JC)

GMP overhead is carried once per 4-frame multi-frame in bytes JC1-JC6. The 14-bit $C_m(t)$ (i.e., m-bit block count value) is carried in bits C1-14 of JC1 and JC2 (C1=MSB, …, C14=LSB) and the

encoded 5-bit $\Sigma C_{nD}(t)$ (cumulative value of $C_{nD}(t)$) is carried in bit D1-D5 of JC4 and JC5 (D1=MSB, … D5=LSB).

$C_m(t)$ shall be protected with a CRC8 (carried in JC3 OH byte) and $\Sigma C_{nD}(t)$ shall be protected with a CRC3 (carried in the four LSBs of JC6 OH byte).

The CRC-8 located in JC3 is calculated over the JC1 and JC2 bits. The CRC-8 uses the $g(x) = x^8 + x^3 + x^2 + 1$ generator polynomial, and is calculated as follows:

1) The JC1 and JC2 octets are taken in network octet order, most significant bit first, to form a 16-bit pattern representing the coefficients of a polynomial *M(x)* of degree 15.

2) *M(x)* is multiplied by x^8 and divided (modulo 2) by *G(x)*, producing a remainder *R(x)* of degree 7 or less.

3) The coefficients of *R(x)* are considered to be an 8-bit sequence, where x^7 is the most significant bit.

4) This 8-bit sequence is the CRC-8 where the first bit of the CRC-8 to be transmitted is the coefficient of x^7 and the last bit transmitted is the coefficient of x^0.

The de-mapper process performs steps 1-3 in the same manner as the mapper process, except that here, the *M(x)* polynomial of step 1 includes the CRC bits of JC3, resulting in *M(x)* having degree 23. In the absence of bit errors, the remainder shall be 0000 0000.

NOTE – Refer to Appendix VI of [ITU-T G.709] for a parallel logic implementation of CRC-8.

The CRC-3 is calculated over bits 6-8 in JC4 and JC5. The CRC-3 uses the $g(x) = x^3 + x^2 + 1$ generator polynomial, and is calculated as follows:

1) The JC4 bits 6-8 and JC5 bits 6-8 are taken in network transmission order, most significant bit first, to form a 6-bit pattern representing the coefficients of a polynomial *M(x)* of degree 5.

2) *M(x)* is multiplied by x^3 and divided (modulo 2) by *G(x)*, producing a remainder *R(x)* of degree 2 or less.

3) The coefficients of *R(x)* are considered to be a 3-bit sequence, where x^2 is the most significant bit.

4) This 3-bit sequence is the CRC-3 where the first bit of the CRC-3 to be transmitted is the coefficient of x^2 and the last bit transmitted is the coefficient of x^0.

The demapper process performs steps 1-3 in the same manner as the mapper process. In the absence of bit errors, the remainder shall be 000.

10.2.3.3 Client status (CSTAT)

An 8-bit (1 byte) field, as shown in Figure 10-8, is provided for general purpose status indication.

– Client signal fail (CSF)

– Maintenance (MNT)

– Client local and remote degrades (LD, RD)

– Reserved (RES)

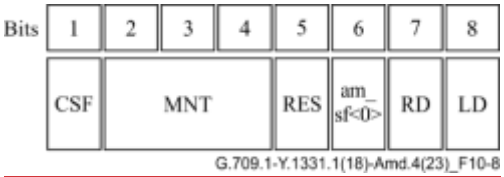

Figure 10-8 – Ethernet GMP CSTAT field

10.2.3.3.1 Client signal fail (CSF)

The client signal fail (CSF) bit is set to "1" to indicate that an incoming client fault was detected; otherwise it is set to "0". The client signal fail (CSF) bit indicates forward signal fail status detected at the local RX client interface in the downstream direction. The replacement signal for client fault conditions is Ethernet local fault (LF) as defined in [IEEE 802.3] generated using a local clock.

10.2.3.3.2 Reserved (RES)

One bit of the CSTAT byte is reserved for future international standardization as shown in Figure 10-8. These bits are set to "0".

10.2.3.3.3 Maintenance (MNT)

Three bits of the CSTAT byte are used for signalling maintenance states.

– 000 – Normal operation

– 101 – LCK

NOTE – 100 value is reserved due to FlexOsec squelch pattern.

LCK definition and behaviour is the same as [ITU-T G.709]. A locked (LCK) is a signal sent downstream as an indication that upstream the connection is "locked". The replacement signal for client locked maintenance is Ethernet local fault (LF) as defined in [IEEE 802.3] generated using a local clock.

10.2.3.3.4 Client degrade indication (LD/RD)

The 3-bit host link degrade indication field is defined to indicate to the downstream device the quality of the client. This is transparently passed from the client's terminated alignment marker fields, which are referred to as am_sf<0> (reserved), am_sf<1> (remote degrade RD) and am_sf<2> (local degrade LD).

These are only applicable to 200GE and 400GE clients. These are applied as in Annex K of [ITU-T G.709].

10.3 FlexO payload PRBS test pattern

A framed FlexO PRBS test pattern is used for validating FlexO interfaces through links and regens. The required PRBS31 is per [IEEE 802.3] with initial state being all 1s.

- The PRBS polynomial pattern is inserted per FlexO instance, replicated in all instances on a FlexO-x(e)-<fec> interface.
- The PRBS pattern will be identified by a unique payload type identifier as shown in Table 9-4.
- The PRBS in the source is inserted in the full payload area shown in Figure 8-1. Stuffing or padding used by mapping procedures is ignored (overwritten) when PRBS is used.
- The PRBS in the sink is monitored from the FlexO payload area. The PRBS checker shall recover and verify the PRBS31 sequence.

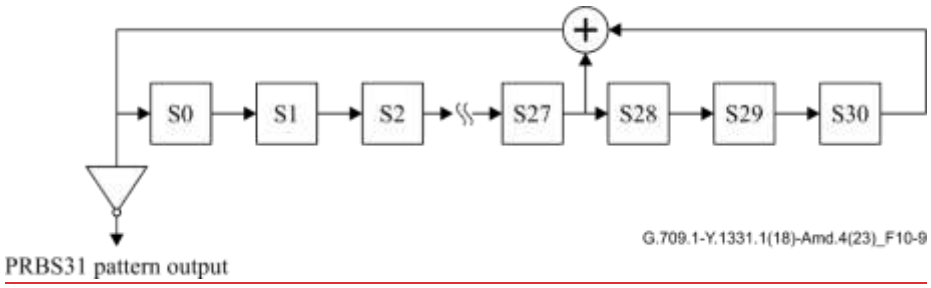

Figure 10-9 – FlexO PRBS

10.3.1 Client mapping specific overhead

The client mapping specific overhead shown in Figure 9-7a is not used for PRBS test pattern and is reserved.

11 100G FlexO-1-RS interface

11.1 Frame structure

The 100G FlexO-1-RS frame structure is shown in Figure 11-1 and consists of 128 rows by 5,440 1-bit columns. It contains a FlexO frame structure in columns 1 to 5140 and a FEC parity area in columns 5,141 to 5,440 in every row. FlexO-1-RS interfaces use alignment markers as described in clause 9.1.

Each row constitutes a 5,440-bit FEC codeword, with the last 300 bits used for the FEC parity bits. This results in a bit-oriented structure. The MSB in each FEC codeword is column 1, the LSB is column 5,440.

NOTE – The 100G FlexO-1-RS frame structure is derived from 100Gbit/s Ethernet clause 91 [IEEE 802.3] FEC alignment and lane architecture, without any 66b alignment or 256b/257b transcoding functions.

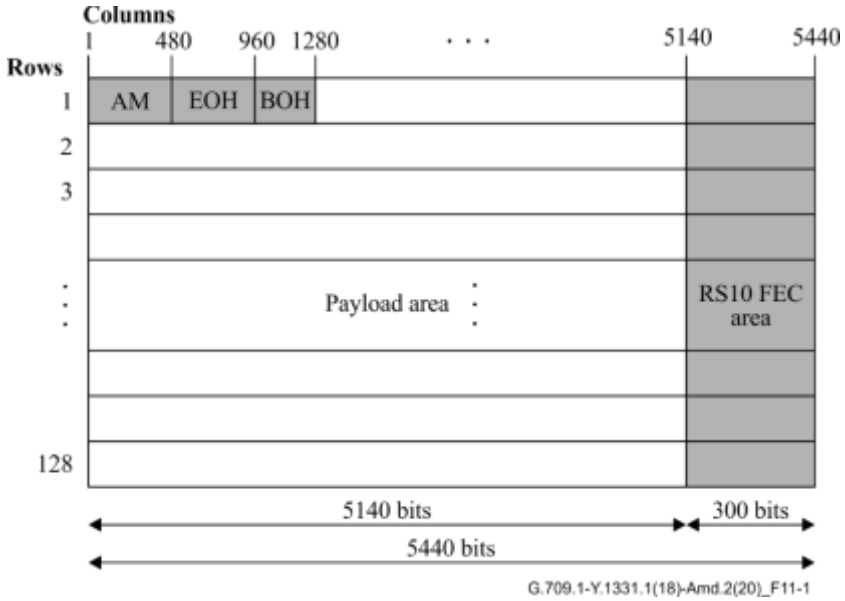

Figure 11-1 – 100G FlexO-1-RS frame structure

11.2 Bit rate and frame periods

The bit rate and tolerance of the 100G FlexO-1-RS signal is defined in Table 11-1.

Table 11-1 – 100G FlexO-1-RS types and bit rates

100G FlexO-1-RS nominal bit rate	Bit-rate tolerance
30592/27233 × 99 532 800 kbit/s	±20 ppm
NOTE 1 – The nominal 100G FlexO-1-RS bit rates are approximately: 111 809 474.446 kbit/s. NOTE 2 – The 100G FlexO-1-RS bit rate can be based on the OTUC bit rate as follows: 256/241 × OTUC bit rate = 256/241 × 239/226 × 99 532 800 kbit/s. NOTE 3 – The resulting 100G FlexO-1-RS bit rate is within a -4.46 ppm offset of the OTU4 nominal bit rate.	

The frame and multi-frame periods of the 100G FlexO-1-RS signal are defined in Table 11-2.

Table 11-2 – 100G FlexO-1-RS frame and multi-frame periods

Frame period (Note)	Multi-frame period (Note)
~6.228 µs	49.822 µs
NOTE – The period is an approximated value, rounded to 3 decimal places.	

11.3 Overhead

100G FlexO-1-RS specific overhead is not defined.

11.4 Scrambling

The 100G FlexO-1-RS frame payload, fixed stuffing, basic overhead and extended overhead must be scrambled prior to transmission, in order to provide DC balance and proper running disparity on the interface. The am_i fields in the AMs are not scrambled and the chosen values have properties of already being DC balanced. -Figure 11-3 below shows highlighted areas as scrambled.

The operation of the scrambler shall be functionally equivalent to that of a frame-synchronous additive scrambler with sequence length 65535 and the generating polynomial shall be $x^{16} + x^{12} + x^3 + x + 1$. See Figure 11-3 [ITU-T G.709] for an illustration of this scrambler.

The scrambler resets to 0xFFFF on the most significant (first transmitted) bit of the start of frame and the scrambler state advances during each bit of the FlexO-1-RS frame (see Figure 11-2). In the source function, the AM values (am_i fields) are inserted after scrambling and before the input to the FEC encoder. In other words, the FEC encoding is performed on unscrambled AM bits (am_i fields). The FEC encoder overwrites the FEC bit fields. The sink then receives unscrambled AM (am_i fields) and FEC fields, as illustrated in Figure 11-3.

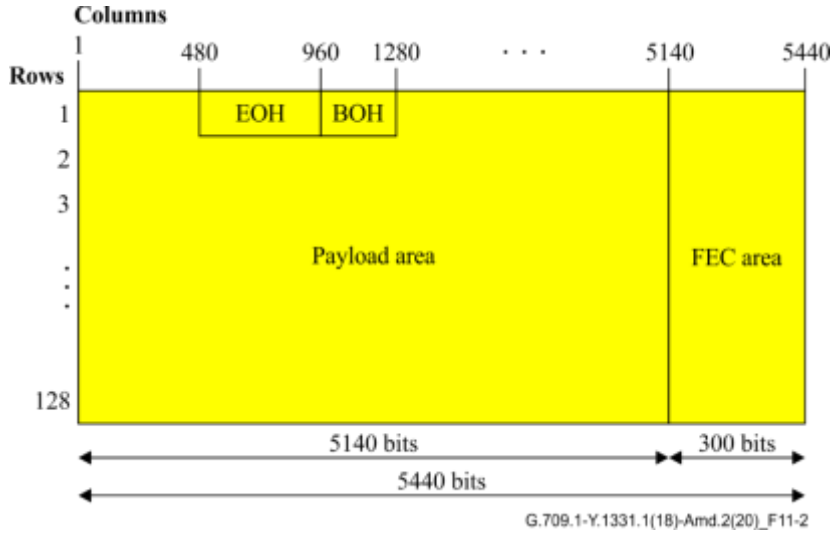

Figure 11-2 – 100G FlexO-1-RS frame after scrambling

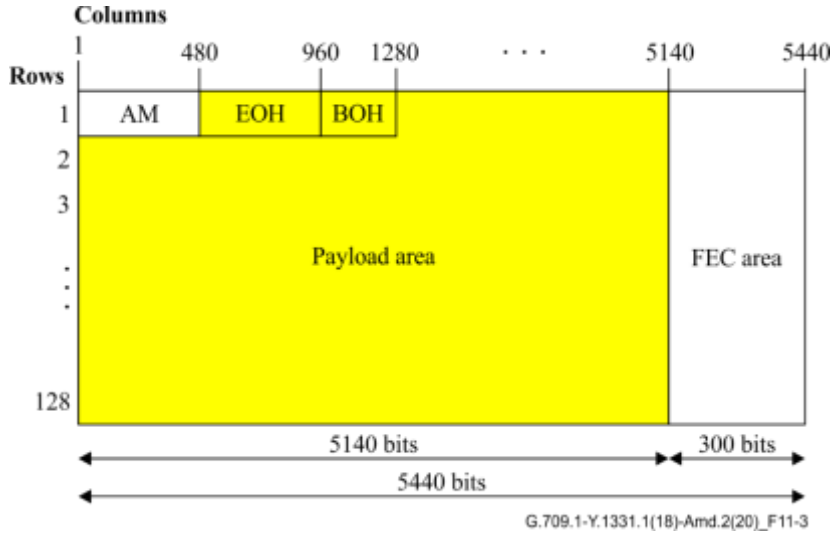

Figure 11-3 – 100G FlexO-1-RS frame after AM and FEC insertion

11.5 Forward error correction (FEC)

A 100G FlexO-1-RS FEC codeword occupies one row in the 100G FlexO-1-RS frame. The 100G FlexO-1-RS frame allocates 300 bits for FEC parity, per row, as shown in Figure 11-1.

The FEC scheme employs a Reed-Solomon code operating over the Galois Field GF(2^{10}), where the symbol size is 10 bits.

A Reed-Solomon code is denoted as RS(n,k) where k represents the number of message symbols to generate 2t parity symbols, which are appended to the message of total length n. The corresponding formula is n=k+2t, specifically:

n=544

k=514

t=15

The FEC encoder processes 20 * 257-bit data blocks, resulting in the 5140 data bits in the FEC codeword (row) and generates 20 * 15 = 300 bits of FEC parity.

NOTE – The 100G FlexO-1-RS FEC is based on RS10 (544, 514), as specified in clause 91 of [IEEE 802.3] for 100GBASE-KP4 interfaces.

11.6 FOIC1.k-RS interface

11.6.1 FOIC1.4-RS interface

A FlexO frame is adapted over multi-channel parallel interfaces, using four ~28 Gbit/s physical lanes. No lane bit-multiplexing is performed.

The alignment markers for the FlexO frame are distributed on four FOIC1.4 lanes, resulting in 240-bit of data per lane. The alignment marker ~~(AM)~~ values are specified in clause 9.1. Each AM has unique UMx and UPx values. When the four AMs are distributed to lanes 0, 1, 2 and 3, the unique values are used for lane reordering in the sink function. The CMx values are replicated on all four lanes to facilitate the searching, alignment and deskewing process.

After FEC encoding, the data and parity bits are distributed to all four logical FOIC1.4 lanes, in groups of 10-bits, in a round robin distribution scheme from the lowest to the highest numbered lanes. The resulting per-lane transmitted values of the AM fields are illustrated in Table 11-3 where the transmission order is from left to right. In other words, for example, AM0 is transmitted in Lane 0, AM1 is transmitted in Lane 1, etc., and the bits of each 10-bit word are transmitted MSB first.

NOTE 1 – The inverse multiplexing function is based on clause 91 [IEEE 802.3].

NOTE 2 – The mechanism is compatible and can reuse optical modules being developed for IEEE 100GBASE-R4, with OTU4 rate support.

NOTE 3 – The electrical specifications for an FOIC1.4-RS 25G lane is found in [b-OIF CEI].

Table 11-3 – AM bit distribution over the four FOIC1.4-RS lanes

AM bits	Lane 0 10-bit symbol of AM0	Lane 1 10-bit symbol of AM1	Lane 2 10-bit symbol of AM2	Lane 3 10-bit symbol of AM3
1 – 40	0101100101	0101100101	0101100101	0101100101
41 – 80	0100100110	0100100110	0100100110	0100100110
81 – 120	0100011011	0100001000	0100011000	0100010110
121 – 160	0110100110	0010100110	1010100110	1010100110
161 – 200	1010110110	1010110110	1010110110	1010110110
201 – 240	0110111001	0110111110	0110110111	0110110010
241 – 280	1011100000	0110010110	1111011111	0001011000
281 – 320	0010001110	1001111011	0011001111	0100000001
321 – 360	1100111101	0111111000	0110101010	0000101111
361 – 400	1001000111	0110011010	0000001000	0111101001
401 – 440	1111011100	0101100001	0011001100	1110111111
441 – 480	0100110000	0010000001	0010010101	1011110100
NOTE – Transmission order of each 10-bit word is left-to-right (MSB first). The transmission order within the FlexO frame is left-to-right across the row and down the table. The transmission order for each lane is per-word and down the table.				

11.6.2 FOIC1.4-RS skew tolerance requirements

The lane skew tolerance requirement is 180 ns.

NOTE – These requirements are in line with CAUI4 [IEEE 802.3].

11.6.3 FOIC1.4-RS 28G lane bit rate

The FOIC1.4-RS lane is synchronous to the FlexO-1-RS frame. There are four lanes.

The bit rate and tolerance of the FOIC1.4-RS lane signal is defined in Table 11-4.

Table 11-4 – FOIC1.4-RS lane rate

FOIC1.4-RS nominal lane bit rate	Bit-rate tolerance
30592/27233 × 24 883 200 kbit/s	±20 ppm
NOTE 1 – The nominal lane rate is approximately: 27 952 368.611 kbit/s. NOTE 2 – FOIC1.4-RS_lane_rate = 100G_FlexO-1-RS_rate/4.	

NOTE – The 100G FlexO-1-RS rate is specified in clause 11.2.

This results in a FOIC1.4-RS lane bit rate with a −4.46 ppm offset from the OTL4.4 nominal bit rate.

11.6.4 m*FOIC1.4-RS interface

The m*FOIC1.4-RS interface supports multiple optical tributary signals on each of the m single optical spans with 3R regeneration at each end.

An m*FOIC1.4-RS interface signal contains one OTUCn signal distributed across the m optical interfaces and the k=4 lanes per optical interface.

Specifications of the optical tributary signal carrying each FOIC1.4-RS lane are contained in [ITU-T G.695] and [ITU-T G.959.1].

11.6.5 FOIC1.1-RS interface

A FlexO frame is adapted over a single ~112 Gbit/s physical lane.

The single lane of a FOIC1.1-RS interface is generated by bit multiplexing of each four logical lanes, e.g., bit multiplexing of lane 0, lane 1, lane 2 and lane 3. The logical lanes and AM values are identical to FOIC1.4-RS as defined in clauses 11.6.1 and 11.6.4.

NOTE – The mechanism is compatible and can reuse optical modules with 100G per lane being developed for IEEE 100GBASE xR1, with 100G OTN rate support.

11.6.6 FOIC1.1-RS skew tolerance requirements

The lane skew tolerance requirement is 180 ns.

NOTE – These requirements are in line with 100GAUI-1 [IEEE 802.3].

11.6.7 FOIC1.1-RS 112G lane bit rate

The single FOIC1.1-RS lane is synchronous to the FlexO-1-RS frame.

The bit rate and tolerance of the FOIC1.1-RS lane signal is defined in Table 11-5.

Table 11-5 – FOIC1.1-RS lane rate

FOIC1.1-RS nominal lane bit rate	Bit-rate tolerance
30592/27233 × 99 532 800 kbit/s	±20 ppm
NOTE 1 – The nominal lane rate is approximately: 111 809 474.444 kbit/s. NOTE 2 – FOIC1.1-RS_lane_rate = 100G_FlexO-1-RS_rate.	

NOTE – The 100G FlexO-1-RS rate is specified in clause 11.2.

12 200G FlexO-2-RS interface

12.1 Frame structure

The 200G FlexO-2-RS frame structure is shown in Figure 12-3 and consists of two 10-bit interleaved 100G FlexO frame structures in columns 1 to 10280 and a FEC area in columns 10281 to 10880 in every row as illustrated in Figure 12-3. FlexO-2-RS interfaces use alignment markers as described in clause 9.1.

NOTE – The 200G FlexO-2-RS frame structure is derived from 200 Gbit/s Ethernet clause 119 [IEEE 802.3] FEC alignment and lane architecture, without any 66b alignment or 256b/257b transcoding functions.

Figure 12-1 – Blank figure (deleted by Amd.1) Partial fill

For the case that a m×200G FlexO-2-RS group carries an OTUCn with n < 2m, some 200G FlexO-2-RS signals may contain only one OTUC instance (see Figure 12-2). When a FlexO-2-RS contains fewer than 2 OTUC instances, the equipped OTUC instance is located in the first 100G FlexO frame within this 200G FlexO-2-RS #m frame. The second 100G FlexO frame is not carrying an OTUC instance and has its GID field set to all-0s to indicate that it is unequipped.

The following rules govern unequipped instances:

– Unequipped OTUC instances must always be the highest numbered FlexO instance(s) in a FlexO-2-RS frame.

– There must always be at least one equipped instance in every FlexO-2-RS frame.

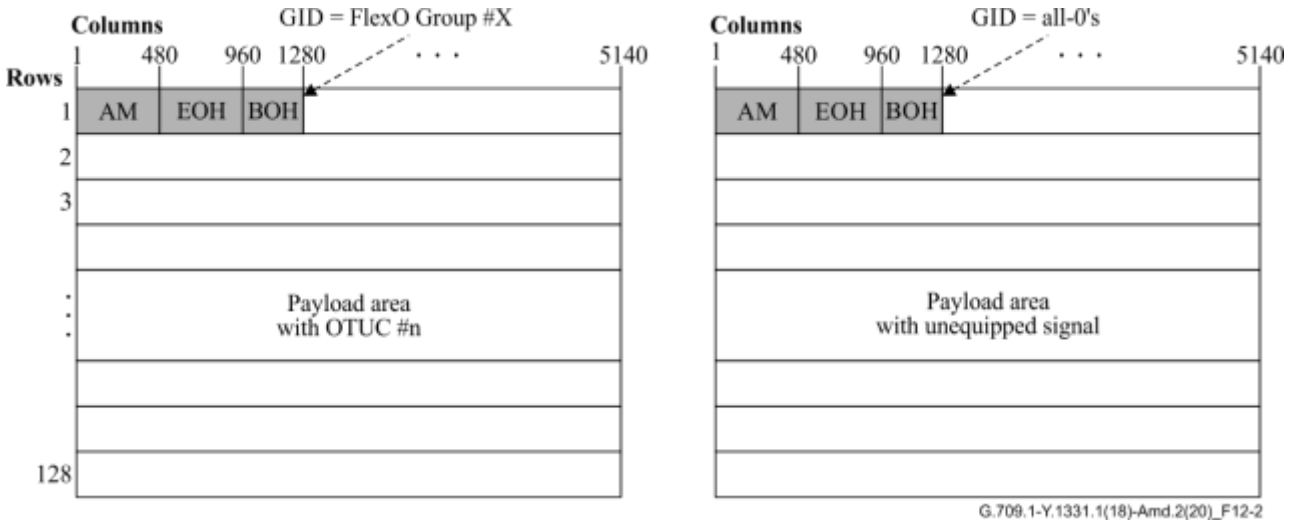

Figure 12-2 – 100G FlexO frames within 200G FlexO-2-RS #m signal for case of partial fill

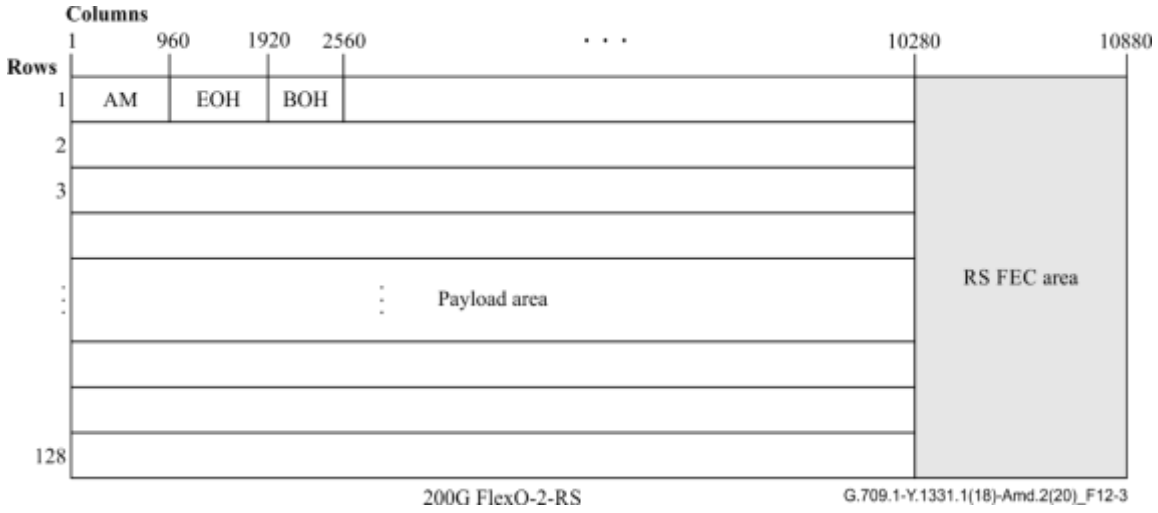

Figure 12-3 – Mapping FlexO instances into the 200G Flex-2-RS frame structure

12.2 Bit rate and frame period

The bit rate and tolerance of the 200G FlexO-2-RS signal is defined in Table 12-1.

Table 12-1 – 200G FlexO-2-RS types and bit rates

200G FlexO-2-RS nominal bit rate	Bit-rate tolerance
2 ×30592/27233 × 99 532 800 kbit/s	±20 ppm
NOTE 1 – The nominal 200G FlexO-2-RS bit rate is approximately: 223 618 948.893 kbit/s. NOTE 2 – The 200G FlexO-2-RS bit rate can be based on the OTUC bit rate as follows: 2 × 256/241 × OTUC bit rate = 2 × 256/241 × 239/226 × 99 532 800 kbit/s.	

The frame and multi-frame periods of the 200G FlexO-2-RS signal are defined in Table 12-2.

Table 12-2 – 200G FlexO-2-RS frame and multi-frame periods

Frame period (Note)	Multi-frame period (Note)
~6.228 µs	49.822 µs
NOTE – The period is an approximated value, rounded to 3 decimal places.	

12.3 Overhead

200G FlexO-2-RS specific overhead is not defined.

12.4 Scrambling

The operation of the 200G FlexO-2-RS scrambler is based on the interleaved 200G FlexO-2-RS frame structure shown in Figure 12-3 which is generated by 10-bit interleaving of the two instances of 128 rows by 5,440 1-bit columns of the 200G FlexO-2-RS frame structure.

The interleaved 200G FlexO-2-RS frame payload, fixed stuffing, basic overhead and extended overhead must be scrambled prior to transmission, in order to provide DC balance and proper running disparity on the interface. The am_i fields in the AMs are not scrambled and the chosen values have properties of already being DC balanced. Figure 12-5 below shows highlighted areas as scrambled.

The operation of the scrambler shall be functionally equivalent to that of a frame-synchronous additive scrambler of sequence length 65535 and the generating polynomial shall be $x^{16} + x^{12} + x^3 + x + 1$. See Figure 11-3 [ITU-T G.709] for an illustration of this scrambler.

The scrambler resets to 0xFFFF on the most significant bit of the start of frame and the scrambler state advances during each bit of the interleaved 200G FlexO-2-RS frame, see Figure 12-4. In the source function, the AM values (am_i fields) are inserted after scrambling and before the input to the FEC encoder. In other words, the FEC encoding is performed on unscrambled AM bits (am_i fields). The FEC encoder overwrites the FEC bit fields. The sink then receives unscrambled AM (am_i fields) and FEC fields, as illustrated in Figure 12-5.

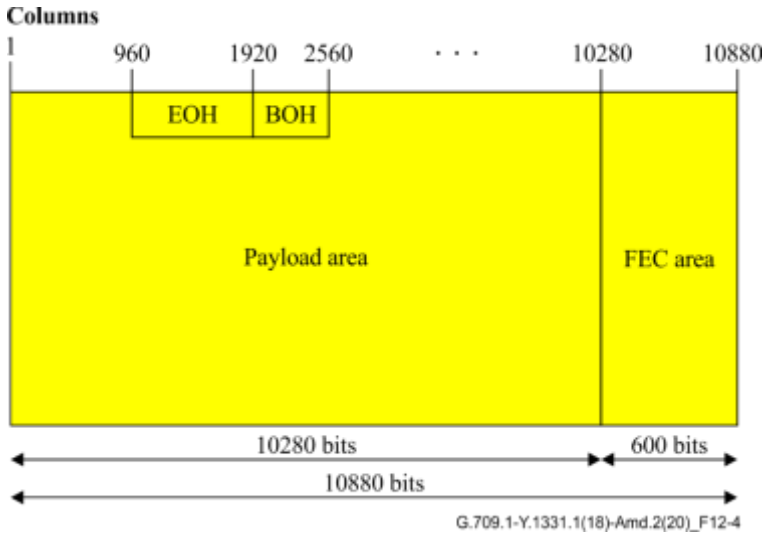

Figure 12-4 – 200G FlexO-2-RS frame after scrambling

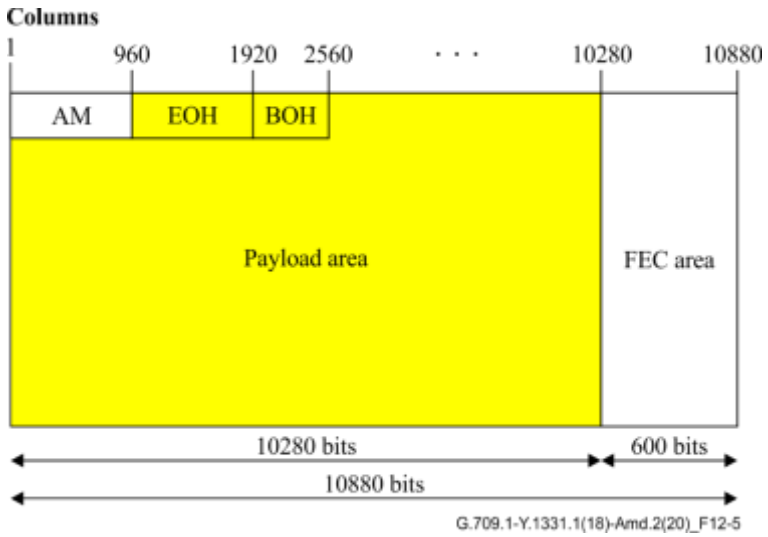

Figure 12-5 – 200G FlexO-2-RS frame after AM and FEC insertion

12.5 Forward error correction (FEC)

The FlexO-2-RS FEC area contains the Reed-Solomon RS(544,514) FEC codes. The RS(544,514) FEC code shall be computed as specified in Annex A.

12.6 FOIC2.k-RS interface

12.6.1 FOIC2.4-RS interface

A FOIC2.4-RS interface is used as a system interface with 200G optical modules. The FlexO-2-RS frame structure is adapted over multi-channel parallel interfaces, using four ~56 Gbit/s physical lanes.

The alignment markers for the FlexO frame are distributed on eight logical FOIC2.4 lanes, resulting in 120-bit of data per logical lane. The alignment marker ~~(AM)~~ values are specified in clause 9.1.3. Each AM has unique UMx and UPx values. When the eight AMs are distributed to lanes 0, 1, 2 to 7, the differing values are used for lane reordering in the sink function. The CMx values are replicated on all eight lanes to facilitate the searching, alignment and deskewing process.

After FEC encoding the FlexO-2-RS frame (see Annex A), each set of two sub-rows (i.e., two FEC codewords) are interleaved (not round-robin) on a 10-bit basis and then distributed to 8 logical lanes in a round robin distribution scheme from the lowest to the highest numbered lanes. The specific scheme of interleaving and distribution is specified in clause 119.2.4.7 of [IEEE 802.3] for 200GBASE-R interface. The resulting per-lane transmitted values of the AM fields are illustrated in Table 12-3 where the transmission order is from left to right. For example, AM0 is transmitted in Lane 0, AM1 is transmitted in Lane 1, etc., and the bits of each 10-bit word are transmitted MSB first.

The 4 physical lanes of a FOIC2.4-RS interface are generated by bit multiplexing two specific logical lanes onto a physical lane.

NOTE 1 – The inverse multiplexing function is based on clause 91 [IEEE 802.3].

NOTE 2 – The mechanism is compatible and can reuse optical modules being developed for IEEE 200GBASE-xR4, with 200G OTN rate support.

Table 12-3 – AM bit distribution over the eight logical lanes

AM bits	Lane 0 10-bit symbol of AM0	Lane 1 10-bit symbol of AM1	Lane 2 10-bit symbol of AM2	Lane 3 10-bit symbol of AM3	Lane 4 10-bit symbol of AM4	Lane 5 10-bit symbol of AM5	Lane 6 10-bit symbol of AM6	Lane 7 10-bit symbol of AM7
1-80	0101100101	0101100101	0101100101	0101100101	0101100101	0101100101	0101100101	0101100101
81-160	0100100110	0100100110	0100100110	0100100110	0100100110	0100100110	0100100110	0100100110
161-240	0100101000	0100001000	0100011000	0100010110	0100100001	0100010011	0100101111	0100010001
241-320	0010100110	0010100110	1010100110	1010100110	1110100110	1110100110	0010100110	0010100110
321-400	1010110110	1010110110	1010110110	1010110110	1010110110	1010110110	1010110110	1010110110
401-480	0110110110	0110111110	0110110111	0110110010	0110111001	0110110111	0110110111	0110110100
481-560	1011110011	0110010110	1111011111	0001011000	1000010101	0010010010	0111010000	1100011010
561-640	0100000011	1001111011	0011001111	0100000001	0010001010	0011110010	1000111001	1101101110
641-720	0011000110	0111111000	0110101010	0000101111	0100111101	1000101110	1000010110	1101101010
721-800	0101000011	0110011010	0000001000	0111101001	1001111010	0011011011	0010001011	1100111001
801-880	0010111111	0101100001	0011001100	1110111111	1011011101	0111000011	1101110001	0100100100
881-960	0011001110	0010000001	0010010101	1011110100	0110110000	0101110100	1001111010	0100100101
NOTE – Transmission order of each 10-bit word is left-to-right (MSB first). The transmission order within the FlexO frame is left-to-right across the row and down the table. The transmission order for each lane is per-word and down the table.								

12.6.2 FOIC2.4-RS skew tolerance requirements

The lane skew tolerance requirement is 180 ns.

NOTE – These requirements are in line with 200GAUI-4 [IEEE 802.3].

12.6.3 FOIC2.4-RS 56G lane bit rate

The FOIC2.4-RS lane is synchronous to the FlexO-2-RS frame. There are four lanes.

The bit rate and tolerance of the FOIC2.4-RS lane signal is defined in Table 12-4.

Table 12-4 – FOIC2.4-RS lane rate

FOIC2.4-RS nominal lane bit rate	Bit-rate tolerance
30592/27233 × 49 766 400 kbit/s	±20 ppm
NOTE 1 – The nominal FOIC2.4-RS lane rate is approximately: 55 904 737.223 kbit/s NOTE 2 – FOIC2.4-RS_lane_rate = 200G_FlexO-2-RS_rate/4	

NOTE – The 200G FlexO-2-RS bit rate is specified in clause 12.2.

12.6.4 m*FOIC2.4-RS interface

The m*FOIC2.4-RS interface supports multiple optical tributary signals on each of the m single optical spans with 3R regeneration at each end.

An m*FOIC2.4-RS interface signal contains one OTUCn signal distributed across the m optical interfaces and the k=4 lanes per optical interface.

Specifications of the optical tributary signal carrying each FOIC2.4-RS lane are contained in [ITU-T G.695] and [ITU-T G.959.1].

12.6.5 FOIC2.4-RS interface processes

Figure 12-6 shows the processes of 200G FlexO-2-RS. It can be seen that it is divided into three parts (the part of reusing 100G FlexO, the part of purely new design and the part of reusing IEEE802.3 200GE PCS/FEC).

The processes of scrambler/descrambler and AM insertion/removal are the only new designs. Before scrambler in the source and after descrambler in the sink, they keep completely the same processes as 100G FlexO's.

In the part of reusing IEEE802.3 200GE PCS lower-part and FEC, it completely reuses all processes related to IEEE802.3 200GE PCS lower-part and FEC. 200G FlexO uses 2*100G KP4-FEC.

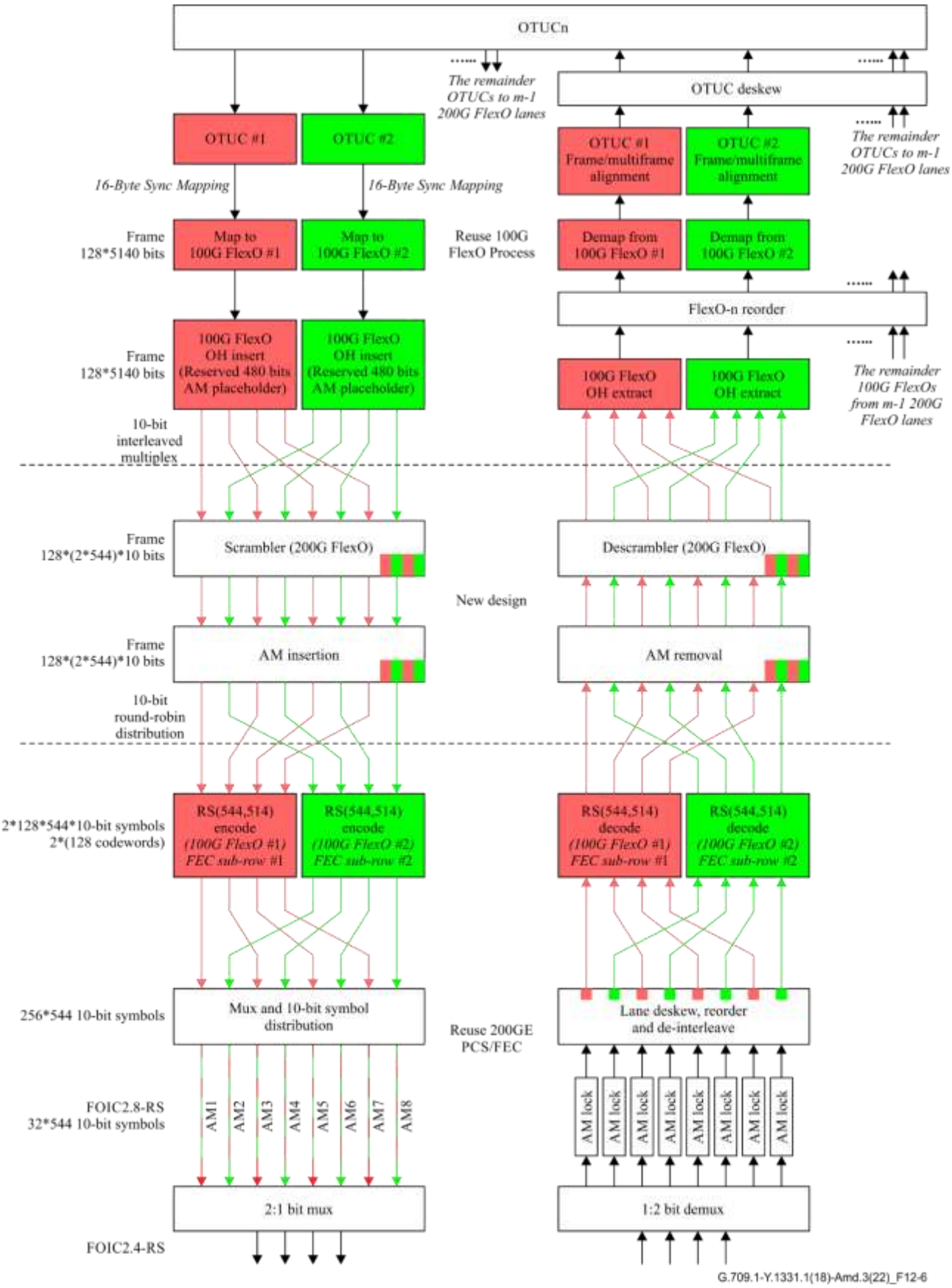

Figure 12-6 – 200G FlexO-2-RS processes

13 400G FlexO-4-RS interface

13.1 Frame structure

The 400G FlexO-4-RS frame structure is shown in Figure 13-3 and consists of four 10-bit interleaved FlexO frame structure instances in columns 1 to 10280 and a FEC area in columns 10281to 10880 in every row as illustrated in Figure 13-3. FlexO-4-RS interfaces use alignment markers as described in clause 9.1.

NOTE – The 400G FlexO-4-RS frame structure is derived from 400 Gbit/s Ethernet clause 119 [IEEE 802.3] FEC alignment and lane architecture, without any 66b alignment or 256b/257b transcoding functions.

Figure 13-1 – Blank figure (deleted by Amd.1) Partial fill

For the case that a m×400G FlexO-4-RS group carries an OTUCn with n < 4m, some 400G FlexO-4-RS signals may contain only three, two or one OTUC instance(s), see Figure 13-2. When a FlexO-4-RS frame contains fewer than 4 OTUC instances, these three, two or one OTUC instance(s) is(are) located in the first one, two or three 100G FlexO frame(s) within this 400G FlexO-4-RS #m frame. The last one, two or three 100G FlexO frames are not carrying an OTUC instance and have their GID field set to all-0s to indicate that the 100G FlexO frame is unequipped.

The same rules in clause 12.1 governing unequipped instances apply.

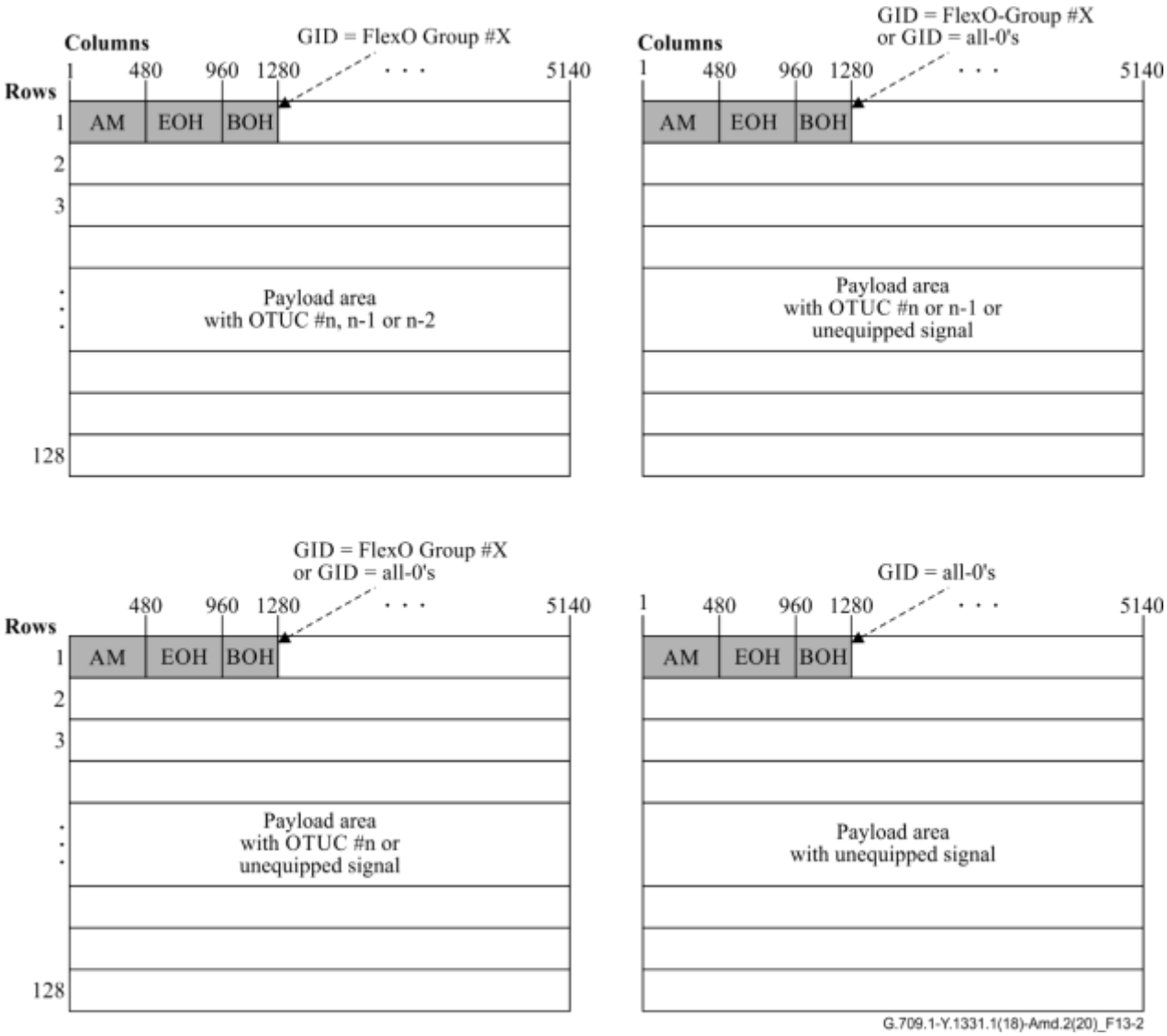

Figure 13-2 – 100G FlexO frames within 400G FlexO-4-RS #m signal for case of partial fill

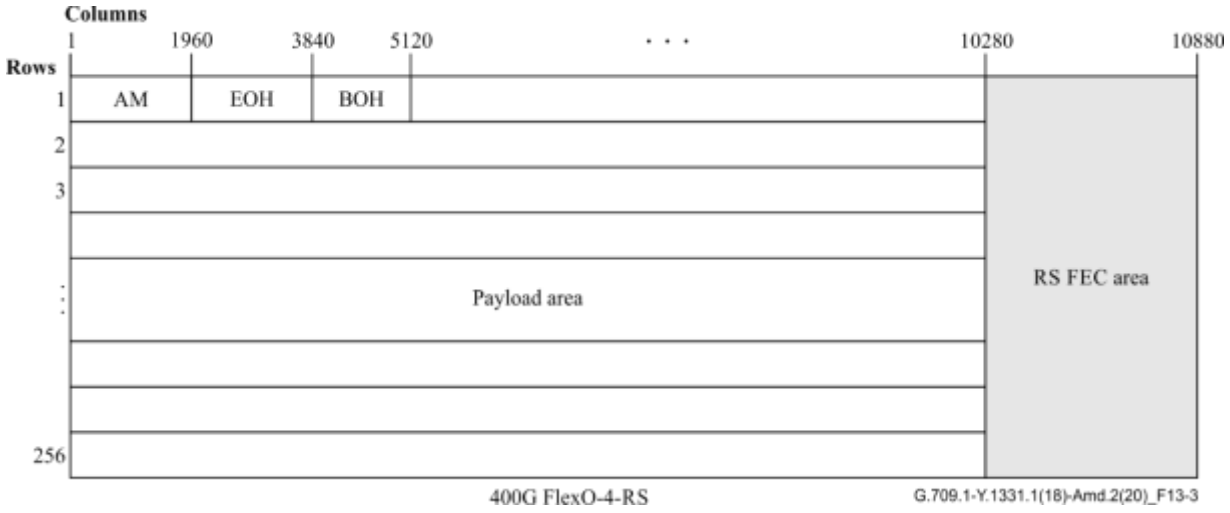

Figure 13-3 – Mapping FlexO instances into the 400G FlexO-4-RS frame structure

13.2 Bit rate and frame periods

The bit rate and tolerance of the 400G FlexO-4-RS signal is defined in Table 13-1.

Table 13-1 – 400G FlexO-4-RS types and bit rates

400G FlexO-4-RS nominal bit rate	Bit-rate tolerance
4 ×30592/27233 × 99 532 800 kbit/s	±20 ppm
NOTE 1 – The nominal 400G FlexO-4-RS bit rate is approximately: 447 237 897.786 kbit/s. NOTE 2 – The 400G FlexO-4-RS bit rate can be based on the OTUC bit rate as follows: 4 × 256/241 × OTUC bit rate = 4 × 256/241 × 239/226 × 99 532 800 kbit/s.	

The frame and multi-frame periods of the 400G FlexO-4-RS signal are defined in Table 13-2.

Table 13-2 – 400G FlexO-4-RS frame and multi-frame periods

Frame period (Note)	Multi-frame period (Note)
~6.228 µs	49.822 µs
NOTE – The period is an approximated value, rounded to 3 decimal places.	

13.3 Overhead

400G FlexO-4-RS specific overhead is not defined.

13.4 Scrambling

The operation of the 400G FlexO-4-RS scrambler is based on the interleaved 400G FlexO-4-RS frame structure shown in Figure 13-3 which is generated by 10-bit multiplexing of the two instances of 256 rows by 5,440 1-bit columns of the 400G FlexO-4-RS frame structure.

The interleaved 400G FlexO-4-RS frame payload, fixed stuffing, basic overhead and extended overhead must be scrambled prior to transmission, in order to provide DC balance and proper running disparity on the interface. The am_i fields in the AMs are not scrambled and the chosen values have properties of already being DC balanced. The padding fields are scrambled. Figure 13-5 below shows highlighted areas as scrambled.

The operation of the scrambler shall be functionally equivalent to that of a frame-synchronous scrambler of sequence 65535 and the generating polynomial shall be $x^{16} + x^{12} + x^3 + x + 1$. See Figure 11-3 [ITU-T G.709] for an illustration of this scrambler.

The scrambler resets to 0xFFFF on the most significant bit of the start of frame and the scrambler state advances during each bit of the interleaved 400G FlexO-4-RS frame, see Figure 13-4. In the source function, the AM values (am_i fields) are inserted after scrambling and before the input to the FEC encoder. In other words, the FEC encoding is performed on unscrambled AM bits (am_i fields). The FEC encoder overwrites the FEC bit fields. The sink then receives unscrambled AM (am_i fields) and FEC fields, as illustrated in Figure 13-5.

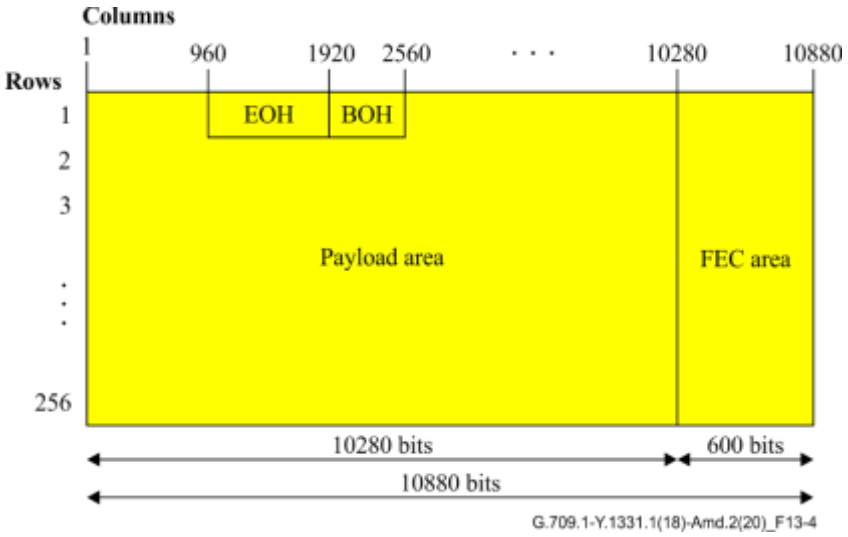

Figure 13-4 – 400G FlexO-4-RS frame after scrambling

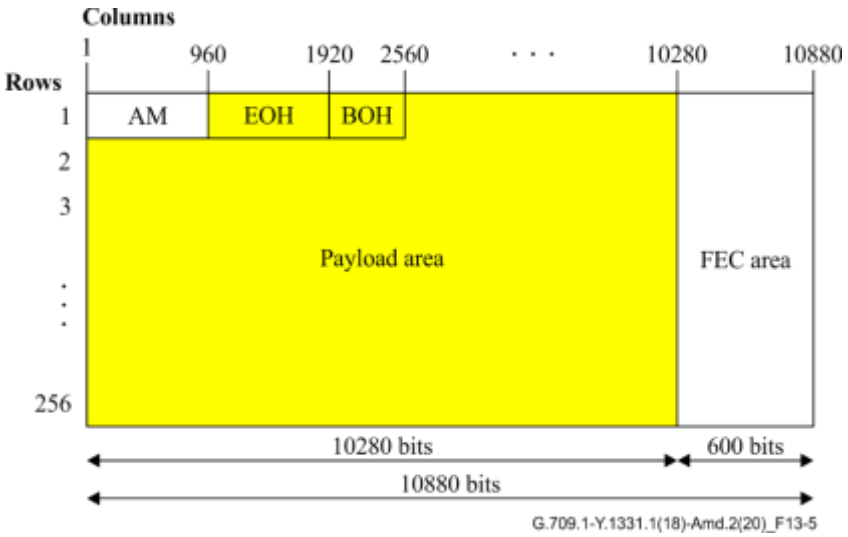

Figure 13-5 – 400G FlexO-4-RS frame after AM and FEC insertion

13.5 Forward error correction (FEC)

The FlexO-4-RS FEC area contains the Reed-Solomon RS(544,514) FEC codes. The RS(544,514) FEC code shall be computed as specified in Annex A.

13.6 FOIC4.k-RS interface

13.6.1 FOIC4.8-RS interface

A FOIC4.8-RS interface is used as a system interface with 400G optical modules. The FlexO-4-RS frame structure is adapted over multi-channel parallel interfaces, using eight ~56 Gbit/s physical lanes.

The alignment markers for the 400G FlexO frame are distributed on sixteen lanes, resulting in 120-bit of data per lane. The alignment marker ~~(AM)~~ values are specified in clause 9.1.5. Each AM has unique UMx and UPx values. When the sixteen AMs distributed to lanes 0, 1, 2 to 15, the differing values are used for lane reordering in the sink function. The CMx values are replicated on all sixteen lanes to facilitate the searching, alignment and deskewing process.

After FEC encoding the FlexO-4-RS frame (see Annex A), each set of two sub-rows (i.e., two FEC codewords) are interleaved (not round-robin) on a 10-bit basis and then distributed to 8 logical lanes in a round robin distribution scheme from the lowest to the highest numbered lanes.

The specific scheme of interleaving and distribution is specified in clause 119.2.4.7 of [IEEE 802.3] for 400GBASE-R interface. The resulting per-lane transmitted values of the AM fields are illustrated in Table 13-3 where the transmission order is from left to right. For example, AM0 is transmitted in Lane 0, AM1 is transmitted in Lane 1, etc., and the bits of each 10-bit word are transmitted MSB first.

The 8 lanes of a FOIC4.8-RS interface are generated by bit multiplexing of each two logical lanes, e.g., bit multiplexing of lane 0 and lane 1, lane 2 and lane 3, lane 4 and lane 5, lane 6 and lane 7, lane 8 and lane 9, lane 10 and lane 11, lane 12 and lane 13, lane 14 and lane 15.

NOTE 1 – The inverse multiplexing function is based on clause 91 [IEEE 802.3].

NOTE 2 – The mechanism is compatible and can reuse optical modules being developed for IEEE 400GBASE-xR4, with 400G OTN rate support.

Table 13-3 – AM bit distribution over the sixteen logical lanes

AM bits	Lane 0 10-bit symbol of AM0	Lane 1 10-bit symbol of AM1	Lane 2 10-bit symbol of AM2	Lane 3 10-bit symbol of AM3	Lane 4 10-bit symbol of AM4	Lane 5 10-bit symbol of AM5	Lane 6 10-bit symbol of AM6	Lane 7 10-bit symbol of AM7
1-80	0101100101	0101100101	0101100101	0101100101	0101100101	0101100101	0101100101	0101100101
161-240	0100100110	0100100110	0100100110	0100100110	0100100110	0100100110	0100100110	0100100110
321-400	0100011011	0100001000	0100011000	0100010110	0100100001	0100010011	0100101111	0100010001
481-560	0110100110	0010100110	1010100110	1010100110	1110100110	1110100110	0010100110	0010100110
641-720	1010110110	1010110110	1010110110	1010110110	1010110110	1010110110	1010110110	1010110110
801-880	0110111001	0110111110	0110110111	0110110010	0110111001	0110110111	0110110111	0110110100
961-1040	1011100000	0110010110	1111011111	0001011000	1000010101	0010010010	0111010000	1100011010
1121-1200	0010001110	1001111011	0011001111	0100000001	0010001010	0011110010	1000111001	1101101110
1281-1360	1100111101	0111111000	0110101010	0000101111	0100111101	1000101110	1000010110	1101101010
1441-1520	1001000111	0110011010	0000001000	0111101001	1001111010	0011011011	0010001011	1100111001
1601-1680	1111011100	0101100001	0011001100	1110111111	1011011101	0111000011	1101110001	0100100100
1761-1840	0100110000	0010000001	0010010101	1011110100	0110110000	0101110100	1001111010	0100100101

Table 13-3 – AM bit distribution over the sixteen logical lanes

AM bits	Lane 8 10-bit symbol of AM8	Lane 9 10-bit symbol of AM9	Lane 10 10-bit symbol of AM10	Lane 11 10-bit symbol of AM11	Lane 12 10-bit symbol of AM12	Lane 13 10-bit symbol of AM13	Lane 14 10-bit symbol of AM14	Lane 15 10-bit symbol of AM15
81-160	0101100101	0101100101	0101100101	0101100101	0101100101	0101100101	0101100101	0101100101
241-320	0100100110	0100100110	0100100110	0100100110	0100100110	0100100110	0100100110	0100100110
401-480	0100000001	0100110101	0100010111	0100001101	0100000110	0100001010	0100000010	0100001011
561-640	1010100110	1010100110	1110100110	1010100110	0010100110	0010100110	1110100110	0110100110
721-800	1010110110	1010110110	1010110110	1010110110	1010110110	1010110110	1010110110	1010110110
881-960	0110111111	0110110100	0110110010	0110111000	0110111101	0110110011	0110111000	0110110110
1041-1120	1001100001	0101100011	0000101010	1110010001	1010010001	0011100011	1101010100	1010011001
1201-1280	1111001110	1000100011	0111010111	0001100110	0101101111	0011101001	1111011111	0101011101
1361-1440	1010111000	0011110010	0001101111	0001110001	1010100100	1100001111	0110010101	1001111010
1521-1600	0001100111	1110100111	0111110101	1100011011	1001011011	0011000111	1100101010	0101011001
1681-1760	1000001100	0001110111	0110001010	1011100110	1010100100	0011000101	1100001000	1010101000
1841-1920	0101010001	0011000011	0011100100	0111100011	0001010110	1000111100	0010011010	1001100001
NOTE – Transmission order of each 10-bit word is left-to-right (MSB first). The transmission order within the FlexO frame is left-to-right across the row and down the table. The transmission order for each lane is per-word and down the table.								

13.6.2 FOIC4.8-RS skew tolerance requirements

The lane skew tolerance requirement is 180 ns.

NOTE – These requirements are in line with 400GAUI-4 [IEEE 802.3].

13.6.3 FOIC4.8-RS 56G lane bit rate

The FOIC4.8-RS lane is synchronous to the FlexO-4-RS frame. There are eight lanes.

The bit rate and tolerance of the FOIC4.8-RS lane signal is defined in Table 13-4.

Table 13-4 – FOIC4.8-RS lane rate

FOIC4.8-RS nominal lane bit rate	Bit-rate tolerance
30592/27233 × 49 766 400 kbit/s	±20 ppm
NOTE 1 – The nominal FOIC4.8-RS lane rate is approximately: 55 904 737.223 kbit/s NOTE 2 – FOIC4.8-RS_lane_rate = 400G_FlexO-4-RS_rate/8	

The 400G FlexO-4-RS bit rate is specified in clause 13.2.

13.6.4 m*FOIC4.8-RS interface

The m*FOIC4.8-RS interface supports multiple optical tributary signals on each of the m single optical spans with 3R regeneration at each end.

An m*FOIC4.8-RS interface signal contains one OTUCn signal distributed across the m optical interfaces and the k=8 lanes per optical interface.

Specifications of the optical tributary signal carrying each FOIC4.8-RS lane are contained in [ITU-T G.695] and [ITU-T G.959.1].

13.6.5 FOIC4.8-RS interface processes

Figure 13-6 shows the processes of 400G FlexO-4-RS. It can be seen that it is divided into three parts (the part of reusing 100G FlexO, the part of purely new design and the part of reusing IEEE802.3 400GE PCS/FEC).

The processes of scrambler/descrambler and AM insertion/removal are the only new designs. Before scrambler in the source and after descrambler in the sink, they keep completely the same processes as 100G FlexO's.

In the part of reusing IEEE802.3 400GE PCS lower-part and FEC, it completely reuses all processes related of IEEE802.3 400GE PCS lower-part and FEC. 400G FlexO uses 2*200G KP4-FEC.

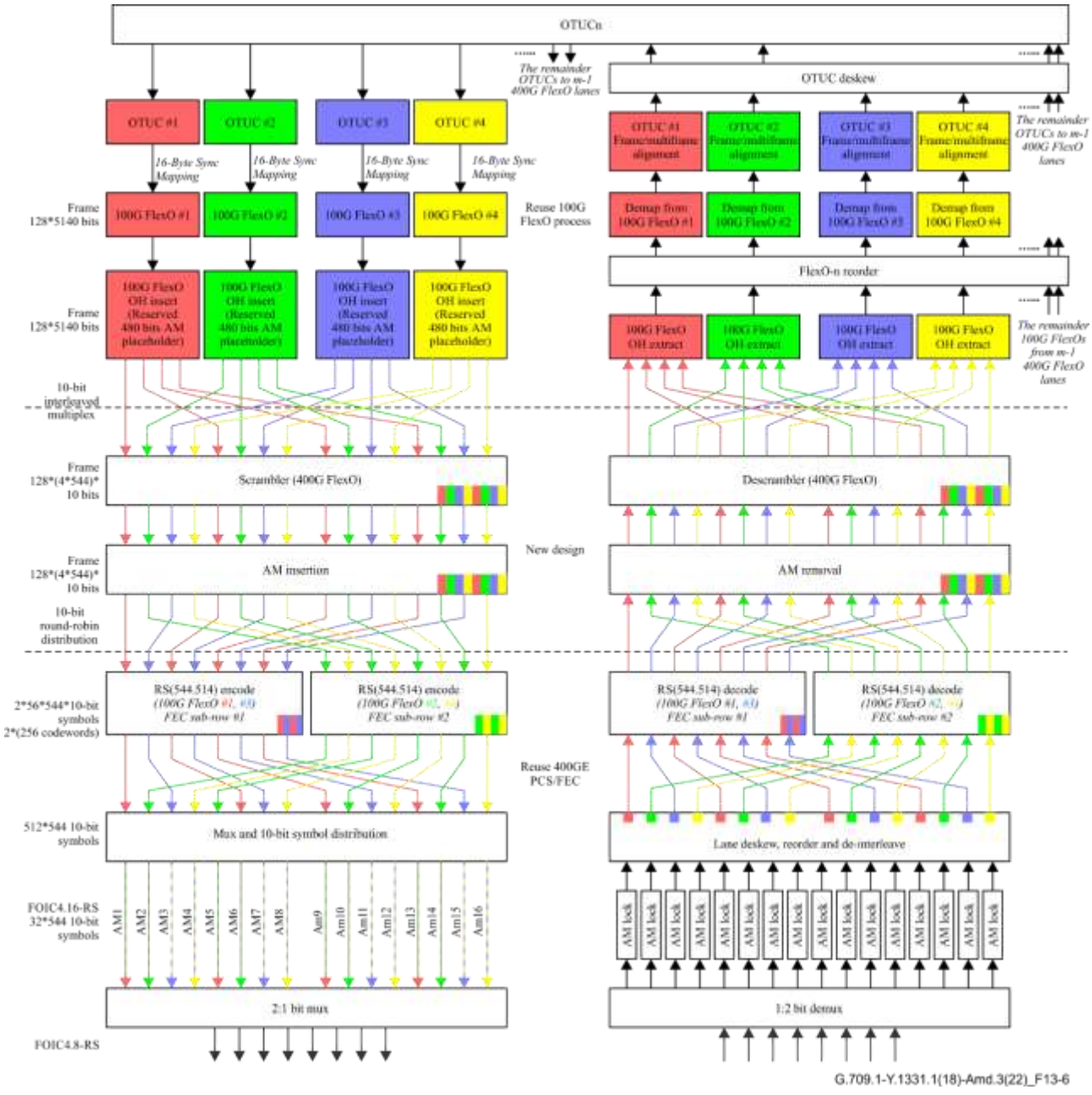

Figure 13-6 – 400G FlexO-4-RS processes

13.6.6 FOIC4.4-RS interface

A FOIC4.4-RS interface is used as a system interface with 400G optical modules. The FlexO-4-RS frame structure is adapted over multi-channel parallel interfaces, using four ~112 Gbit/s physical lanes.

The 4 lanes of a FOIC4.4-RS interface are generated by bit multiplexing of each four logical lanes, e.g., bit multiplexing of lane 0, lane 1, lane 2 and lane 3 (physical lane 0); and lane 4, lane 5, lane 6 and lane 7 (physical lane 1); and lane 8, lane 9, lane 10 and lane 11 (physical lane 2); and lane 12,

lane 13, lane 14 and lane 15 (physical lane 3). The logical lanes and alignment marker values are identical to the sixteen logical lanes of FOIC4.8-RS as defined in clauses 13.6.1 and 13.6.4.

NOTE – The mechanism is compatible and can reuse optical modules with 100G per lane being developed for IEEE 400GBASE xR4, with 400G OTN rate support.

13.6.7 FOIC4.4-RS skew tolerance requirements

The lane skew tolerance requirement is 180 ns.

NOTE – These requirements are in line with 400GAUI-4 [IEEE 802.3].

13.6.8 FOIC4.4-RS 112G lane bit rate

The FOIC4.4-RS lane is synchronous to the FlexO-4-RS frame. There are four lanes.

The bit rate and tolerance of the FOIC4.4-RS lane signal is defined in Table 13-5.

Table 13-5 – FOIC4.4-RS lane rate

FOIC4.4-RS nominal lane bit rate	Bit-rate tolerance
30592/27233 × 99 532 800 kbit/s	±20 ppm
NOTE 1 – The nominal lane rate is approximately: 111 809 474.444 kbit/s. NOTE 2 – FOIC4.4-RS_lane_rate = 100G_FlexO-4-RS_rate.	

NOTE – The 400G FlexO-4-RS rate is specified in clause 13.2.

Annex A

Forward error correction for FlexO-x-RS (x = 2,4) using 10-bit interleaved RS(544,514) codecs

(This annex forms an integral part of this Recommendation.)

NOTE 1 – The FlexO-x-RS FEC (x = 2,4) is based on RS(544, 514,10), as specified in clause 119 of [IEEE 802.3] for 200GBASE-R and 400GBASE-R interfaces.

The forward error correction for the FlexO-x-RS uses 10-bit interleaved codecs using a Reed-Solomon RS(544,514) code. The RS(544,514) code is a non-binary code (the FEC algorithm operates on 10-bit symbols) and belongs to the family of systematic linear cyclic block codes.

For FEC processing, a FlexO-x-RS row is separated into 2 sub-rows using 10-bit-interleaving as shown in Figure A.1. Each FEC encoder/decoder processes one of these sub-rows. The 10-bit FEC parity check blocks are calculated over the 10-bit information blocks 1 to 514 of each sub-row and transmitted in 10-bit blocks 515 to 544 of the same sub-row.

NOTE 2 – After FEC encoding and before distribution to logical lanes, the two sub-rows are 10-bit re-interleaved following the procedure described in clause 119.2.4.7 of [IEEE 802.3] that is not round-robin interleaving.

NOTE 3 – In [IEEE 802.3], sub-row #1 is referred to as A and sub-row #2 is referred to as B.

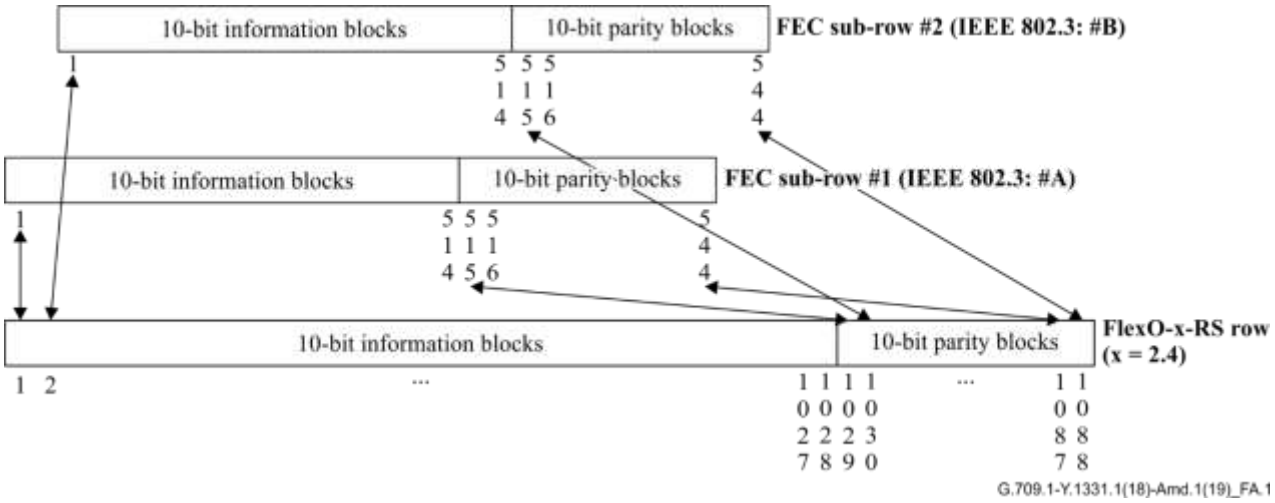

Figure A.1 – FEC sub-rows

The 10-bit blocks in a FlexO-x-RS row belonging to FEC sub-row X (X = 1,2) are defined by: X + 10 × (i – 1) (for i = 1...544).

The generator polynomial of the code is given by:

$$G(z) = \prod_{i=0}^{29}(z - \alpha^i)$$

where α is a root of the binary primitive polynomial $x^{10} + x^3 + 1$.

The FEC code word (see Figure A.2) consists of 10-bit information blocks and parity blocks (FEC redundancy) and is represented by the polynomial:

$$C(z) = I(z) + R(z)$$

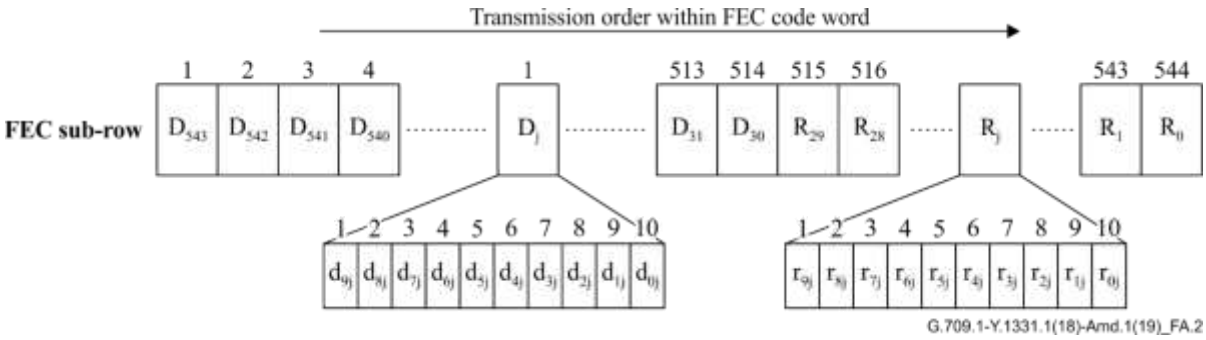

Figure A.2 – RS(544,514) FEC code word

10-bit information blocks are represented by:

$$I(z) = D_{543} \cdot z^{543} + D_{542} \cdot z^{542} + \cdots + D_{30} \cdot z^{30}$$

Where D_j (j = 30 to 1087) is the 10-bit information block represented by an element out of GF(256) and:

$$D_j = d_{9j} \cdot \alpha^9 + d_{8j} \cdot \alpha^8 + \cdots + d_{1j} \cdot \alpha^1 + d_{0j}$$

Bit d_{9j} is the MSB and $d_{0\,j}$ the LSB of the 10-bit information block.

D_{543} corresponds to 10-bit block 1 in the FEC sub-row and D_{30} to 10-bit block 514.

10-bit parity blocks are represented by:

$$R(z) = R_{29} \cdot z^{29} + R_{28} \cdot z^{28} + \cdots + R_1 \cdot z^1 + R_0$$

Where R_j (j = 0 to 29) is the 10-bit parity block represented by an element out of GF(2^{10}) and:

$$R_j = r_{9j} \cdot \alpha^9 + r_{8j} \cdot \alpha^8 + \cdots + r_{1j} \cdot \alpha^1 + r_{0j}$$

Bit r_{9j} is the MSB and $r_{0\,j}$ the LSB of the 10-bit parity block.

R_{29} corresponds to the 10-bit block 515 in the FEC sub-row and R_0 to 10-bit block 544.

R(z) is calculated by:

$$R(z) = I(z) \bmod G(z)$$

where "mod" is the modulo calculation over the code generator polynomial *G(z)* with elements out of the GF(2^{10}). Each element in GF(2^{10}) is defined by the binary primitive polynomial $x^{10} + x^3 + 1$.

The Hamming distance of the RS(544,514) code is d_{min} = 31. The code can correct up to 15 symbol errors in the FEC code word when it is used for error correction. The FEC can detect up to 30 symbol errors in the FEC code word when it is used for error detection capability only.

Annex B

FlexOsec encryption and authentication

(This annex forms an integral part of this Recommendation.)

This annex specifies encryption and authentication of fixed-length FlexO frame structures. It contains specific authentication and encryption process details for the different cipher suite types (profiles).

A cipher suite type is an interoperable specification of cryptographic algorithms together with the values of parameters (e.g., key size) to be used by those algorithms. Specification of the cryptographic functions required by FlexOsec in terms of cipher suite types increase interoperability by providing a clear default and a limited number of alternatives.

B.1 GCM-AES-256 frame payload encryption

The GCM-AES-256 cipher suite corresponds to CST value of 000001 as shown in Table 9-6. This profile is based on cryptographic algorithms and processes as defined in [NIST SP 800-38D].

In this cipher suite type, the FlexO frame payload is encrypted for confidentiality as shown in Figure B.1. The FlexO frame payload along with BOH and a subset of EOH are authenticated for integrity as shown in Figure B.2.

In the FlexOsec scheme, confidentiality and integrity are applied individually per 100G FlexO instance. The frame format discussed is this annex is prior to FEC adaptation and FlexO-x interface interleaving.

B.1.1 GCM-AES-256 confidentiality (encryption)

The bits in the FlexO frame payload area are encrypted prior to transmission for cases where confidentiality on the interface is required, as illustrated in Figure B.1. These bits correspond to the FlexO frame payload area and are excluding AM, EOH and BOH areas. For the purpose of FlexOsec application, the FlexO frame structure can be represented as 5140 × 128-bit fixed-length blocks. An alternate representation using 128-bit blocks is shown in Figure B.2.

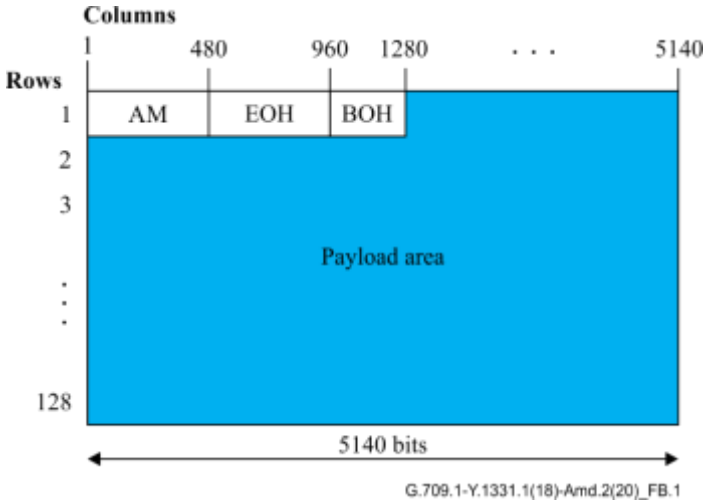

Figure B.1 – FlexO frame encryption

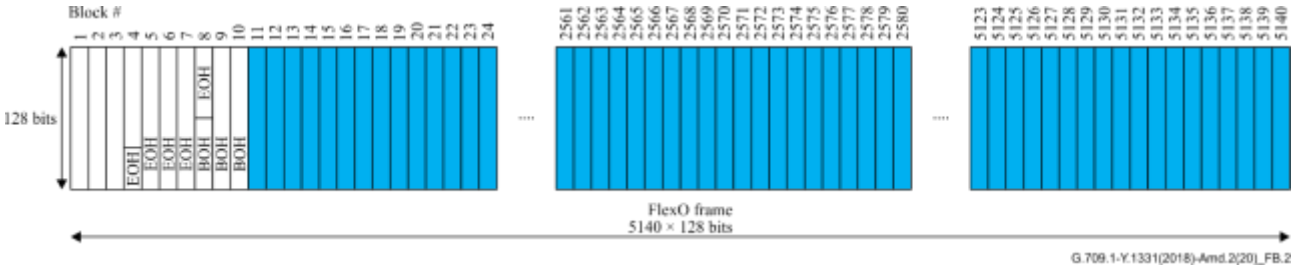

Figure B.2 – FlexO frame encryption (128-bit representation)

B.1.2 GCM-AES-256 integrity (authentication)

The bits in the FlexO frame payload area, BOH and subset of the EOH are authenticated prior to transmission for cases where the integrity of the information on the interface is required, as illustrated in Figure B.3. An alternate representation using 128-bit blocks is shown in Figure B.4. The authentication starts at bit 769 (in the EOH), which corresponds to the 7th 128-bit word, and runs until the end of the frame.

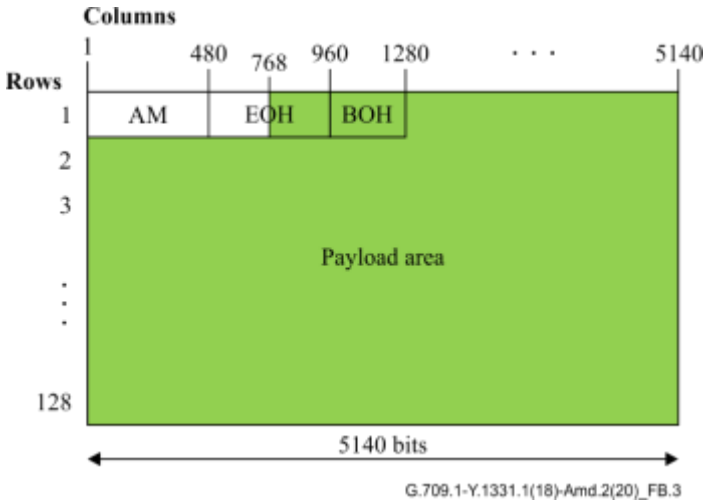

Figure B.3 – FlexO frame authentication

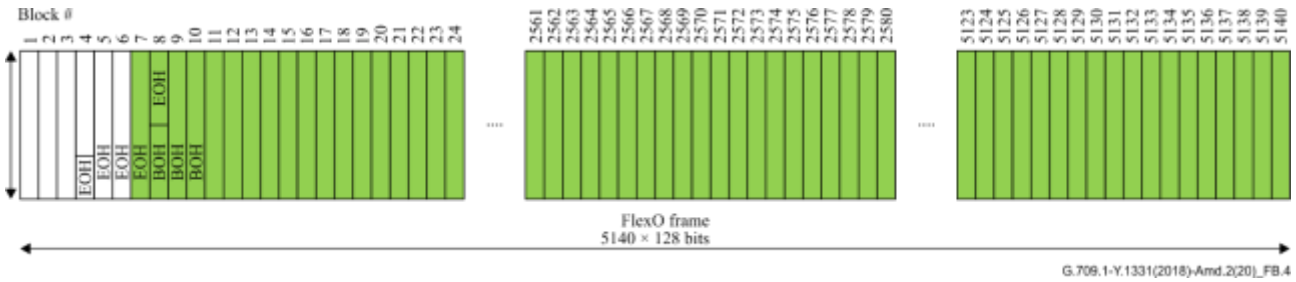

Figure B.4 – FlexO frame authentication (128-bit representation)

An authentication tag (AT) is created using algorithms specified in clause B.1.2, with 128-bit words from the FlexO instance #i frame #j. The AT is then inserted in the next EOH of FlexO instance #i frame #j+1. The authentication tag is unique to each 100G FlexO instance.

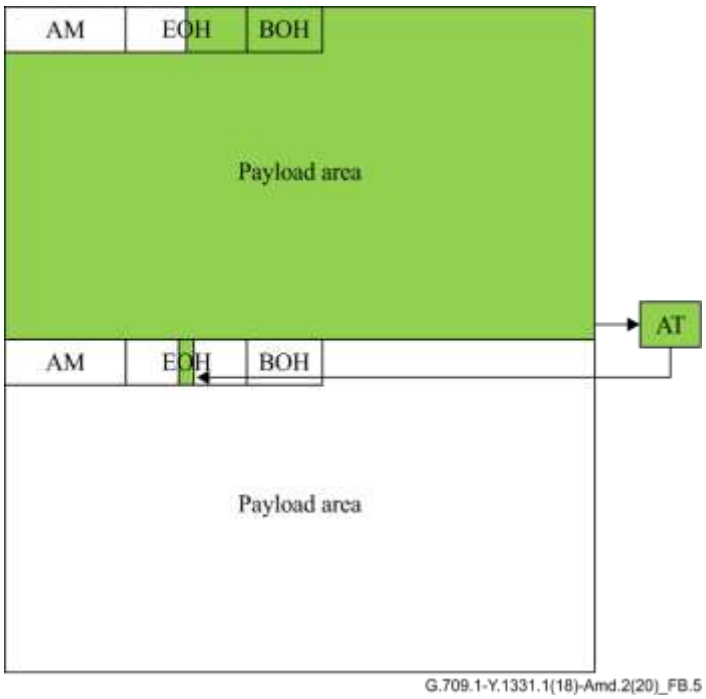

Figure B.5 – FlexO AT insertion

In the process flow, some values in the FlexOsec overhead are inserted after AT calculation (algorithm) in the source functions and before in the sink functions. Some OH values will be assumed as all-0s for the AT algorithms and these are reflected in the Table B.1 below.

Table B.1 – FlexOsec OH AT calculation

FlexOsec OH field	Tag calculation	Note
Authentication tag (AT)	Not part of tag calculation	
Frame number (FN)	Use FN value	
Key index (KI)	Use KI value	
Cipher suite type (CST)	Use CST value	
KCC	All-0s	KCC inserted after tag calculation
Reserved (RES)	All-0s	

Since the AT value of a current frame (n) is presented in the following frame (n+1), buffering of a FlexO frame could optionally be required for some applications that want to discard frames that have failed integrity check (authentication failures). The individual frames can be optionally replaced with a repeating SquelchText = 0x04 byte pattern replacing the area covered by authentication as shown in Figure B.3.

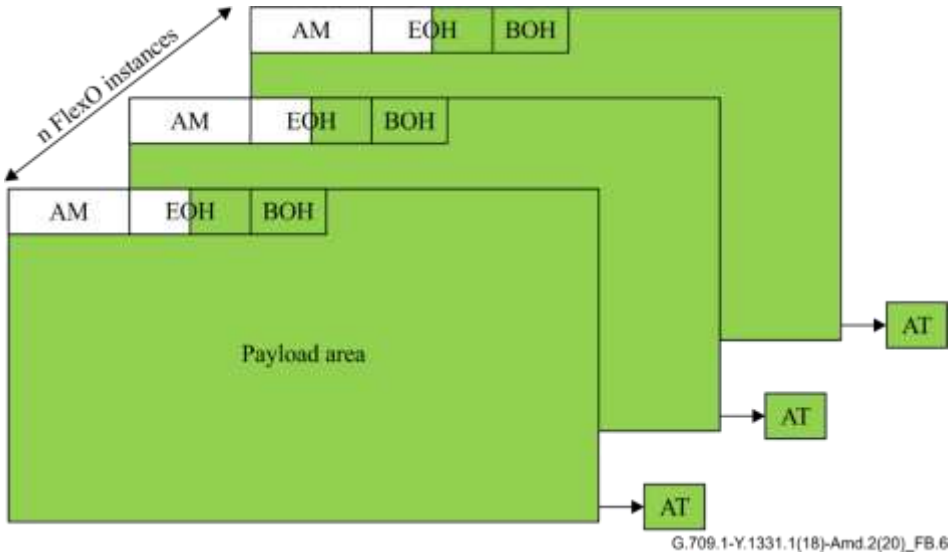

Figure B.6 – Per instance FlexO processing

B.1.3 IV construction

The 96-bit initial vector for this cipher suite type is based on deterministic construction as defined in clause 8.2.1 of [NIST SP 800-38D]. In order to promote interoperability for the default IV length of 96 bits, the leading (i.e., leftmost) 32 bits of the IV hold a user configurable fixed identifier and the trailing (i.e., rightmost) 64 bits hold the invocation field, which is the frame number (FN).

NOTE – The construction described in this clause meets the total number of invocation requirements as specified in clause 8.3 of [NIST SP 800-38D].

B.1.4 GCM-AES-256 algorithms

The authenticated encryption and authenticated decryption algorithms for this cipher suite type are based on the GCM specifications in clause 7 of [NIST SP 800-38D]. These are referred to as algorithms 4 and 5, for the authenticated encryption and authenticated decryption functions, respectively. The specifications include the inputs, the outputs, the steps of the algorithm, diagrams, and summaries.

Table B.2 – GCM-AES-256 parameters

Parameter	Name	Length
C	CipherText	656640 bits (5130 × 128 bits)
P	PlainText	656640 bits (5130 × 128 bits)
A	Additional authenticated data	512 bits (4 × 128 bits)
T	Authentication tag (referred to as AT in recommendation)	128 bits
K	Key	256 bits
IV	Initial vector	96 bits

Figure B.6 below shows how the FlexO frame bits are processed with respective cryptographic algorithms. There are three inputs into the NIST authenticated encryption algorithm referred to as algorithm 4: J0, AAD and P (plaintext). The first bits transmitted are the leftmost bits in the figure.

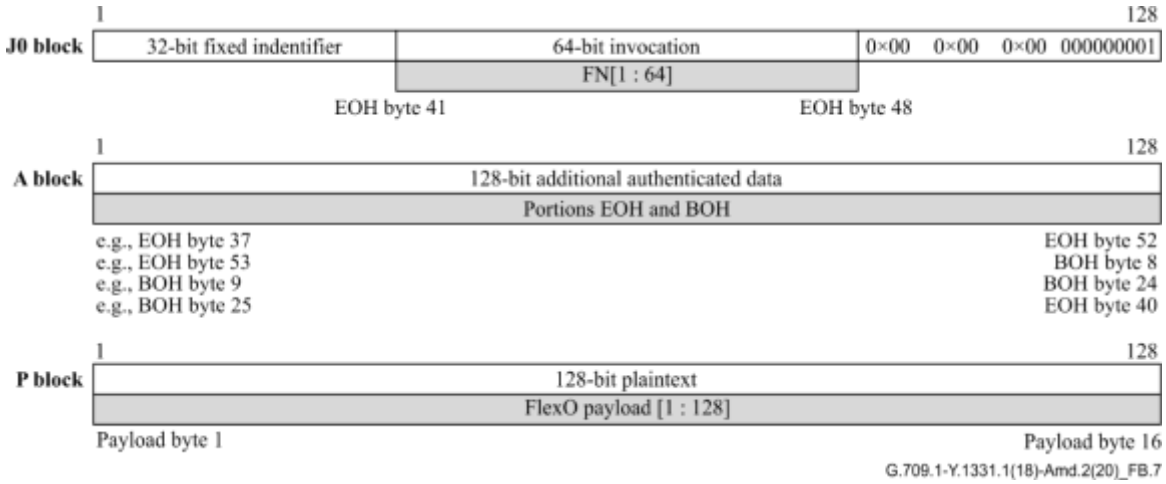

Figure B.7 – FlexOsec bit ordering

Annex C

GMP parameters for mapping Ethernet to FlexO-xe

(This annex forms an integral part of this Recommendation.)

Refer to [ITU-T G.709] Annex D for the general principles of the generic mapping procedure (GMP). The GMP justification control bytes (JC1-6) are carried in the client mapping specific overhead area of the FlexO instances as described in clause 10.2.3. For clients which are split across multiple FlexO instances the mappers are locked and the JC bytes are replicated and present in all FlexO instances carrying the client. For all client types, the JC bytes are present in the second, third and fourth frame of the 4-frame multi-frame, to signal the GMP parameters C_m and ΣC_{nD} from the mapper to the de-mapper. The parameters received in multi-frame *n* indicate the data and stuff locations in multi-frame *n*+1.

For each y00GE client, y=[1,2 or 4]:

- m = GMP data/stuff granularity = y × 257-bits.
- n = y × 257/32 = y × 8.015625-bit unit and represents the timing granularity of the GMP mapping present in C_m and ΣC_{nD} parameters.
- $P_{m,server}$ = maximum number of m-bit data entities in 4-frame multi-frame server payload of the y multi-frame aligned FlexO instances = 10220.
- C_m = number of client m-bit data entities in 4-frame multi-frame server payload of the y multi-frame aligned FlexO instances. It is encoded with 14 bits and carried in JC1 and JC2 control OH bytes.
- C_n = number of equivalent client n-bit data entities in 4-frame multi-frame server payload of the y multi-frame aligned FlexO instances. This value provides additional 'n'-bit timing information.
- ΣC_{nD} – accumulated value of the remainder of C_n and C_m. It is encoded with 5-bits and carried in JC4 and JC5 control OH bytes.

C_n and C_m being integer values, then: $C_n(t) = 32 \times C_m(t) + (\Sigma C_{nD}(t) - \Sigma C_{nD}(t-1))$.

NOTE – In this context m is not used as the parameter for the number of PHYs in a FlexO-x-<fec>-m group.

The support for n-bit timing information (ΣC_{nD}) in the JC4/JC5/JC6 OH is required.

The y 100G streams of a client signal are mapped to the y × FlexO instances payload structure as y × 100G aligned 257b block streams. The payload area for this mapping consists of the payload of the aligned 4-frame multi-frames of y × 100G FlexO instances in ascending IID order. Groups of m consecutive bits of the client are mapped into m bits of the y aligned 4-frame multi-frame payload areas under control of the GMP data/stuff control mechanism. Each group of m in the y aligned 4-frame multi-frame payload areas may carry either m client bits or m stuff bits. The stuff bits shall be transmitted as zeros and shall be ignored on reception.

The client information bit rate is 100 384 497 kbits/s. The server input nominal bit rate is 100 385 723 kbit/s.

The de-mapping process decodes $C_m(t)$ and $C_{nD}(t)$ from JC1/JC2/JC3 and JC4/JC5/JC6 and interprets $C_m(t)$ and $C_{nD}(t)$ according to Annex D of [ITU-T G.709]. CRC8 shall be used to protect against an error in JC1/JC2/JC3 and CRC3 protects against an error in JC4/JC5/JC6 signals.

Table C.1 presents Ethernet GMP parameters.

Table C.1 – Ethernet GMP parameters

Ref	GMP parameter	Formula	Value	Units
f_{client}	Nominal client information bit rate	100GE clients: 100 Gbit/s × 257/256 × 16383/16384	100,384,497,642.517	bit/s
		200GE/400GE clients: y × 100 Gbit/s × 257/256 × 20479/20480	y × 100,385,723,114.014	
Δf_{client}	client bit rate tolerance		100	ppm
f_{server}	server nominal bit rate f		y × 100,622,438,327.432	bit/s
Δf_{server}	server bit rate tolerance		20	ppm
T_{server}	period of server multi-frame	B_{server}/f_{server}	26.154	µs
B_{server}	number of bits per server multi-frame		y × 2,631,680	bits
O_{server}	number of overhead bits per server multi-frame		y × 5,140	bits
P_{server}	maximum number of bits in server payload area	B_{server}-O_{server}	y × 2,626,540	bits
$f_{p,server}$	nominal server payload bit rate	$f_{server}\times P_{server}/B_{server}$	y × 100,425,910,127.574	bit/s
m	GMP data/stuff granularity		y × 257	bits
M	m and n ratio	m/n	32	
$P_{m,server}$	maximum number of (m bit) data entities in the server	P_{server}/m	10220	y × 257b blocks

Table C.1 – Ethernet GMP parameters

Ref	GMP parameter	Formula	Value		Units
	payload area				
C_m	number of client m-bit data entities per server multi-frame				
$c_{m,nom}$	c_m value at nominal client and server bit rates	$(f_{client}/f_{p,server})\times P_{m,server}$	100GE clients	10215.785	y × 257b blocks
			200GE/400GE clients	10215.910	
$c_{m,min}$	c_m value at minimum client and maximum server bit rates	$(1-\Delta f_{client})/(1+\Delta f_{server})\times c_{m,nom}$	100GE clients	10,214.559	y × 257b blocks
			200GE/400GE clients	10,214.684	
$c_{m,max}$	c_m value at maximum client and minimum server bit rates	$(1+\Delta f_{client})/(1-\Delta f_{server})\times c_{m,nom}$	100GE clients	10,217.011	
			200GE/400GE clients	10,217.136	
$C_{m,min}$	rounded down value of $c_{m,min}$	$\lfloor c_{m,min} \rfloor$	10214		
$C_{m,max}$	rounded up value of $c_{m,max}$	$\lceil c_{m,max} \rceil$	10218		
n	GMP justification accuracy, n bit data entity		y × 8.03125		bits
$P_{n,server}$	maximum number of (n bits) data entities in the server payload area	P_{server}/n	1,308,160.000		y × 8.03125b blocks
C_n	number of client n-bit data entities per server multi-frame				

Table **C.**1 – Ethernet GMP parameters

Ref	GMP parameter	Formula	Value		Units
$c_{n,nom}$	c_n value at nominal client and server bit rates	$(f_{client}/f_{p,server})\times P_{n,server}$	100GE clients	1,307,620.556	
			200GE/400GE clients	1,307,636.519	
$c_{n,min}$	c_n value at minimum client and maximum server bit rates	$(1-\Delta f_{client})/(1+\Delta f_{server})\times c_{n,nom}$	100GE clients	1,307,463.645	y × 8.03125 blocks
			200GE/400GE clients	1,307,479.603	
$c_{n,max}$	c_n value at maximum client and minimum server bit rates	$(1+\Delta f_{client})/(1-\Delta f_{server})\times c_{n,nom}$	100GE clients	1,307,777.474	
			200GE/400GE clients	1,307,793.436	
c_{nD}	remainder of C_n and C_m	$c_n-(8\times(m/n)\times c_m)$	Variable		n-bit
C_{nD}	integer value of c_{nD}	$C_n-(8\times(m/n)\times C_m)$	Variable		
ΣC_{nD}	accumulated value of C_{nD}		0-31		

Where,

- Client information rate is the y00GE rate y=[1,2 or 4] with f_{client} nominal bit rate and Δf_{client} bit rate worst case tolerance.
- Server is the aligned 4-frame multi-frame (both payload and overhead) of y FlexO instances with f_{server} nominal bit rate, Δf_{server} bit rate tolerance and B_{server} number of bits per server 4-frame multi-frame.
- Server payload is the aligned 4-frame multi-frame payloads (before AM/EOH/BOH insert) of y FlexO instances with $f_{p,server}$ nominal bit rate, Δf_{server} bit rate tolerance and P_{server} number of bits per server 4-frame multi-frame payload area.
- The maximum number of m (= y × 257) bit GMP data entities per y × 4-frame multi-frame payload is $P_{m,server}$ (=10220).
- For FlexO-xe, use n=[m/32] = [y × 257-bit]/32 = [y × 8.03125] UI that is used as a phase unit "n-bit equivalent" for c_n parameter. c_n indicates the number "n-bit equivalent" of the 100G client stream per FlexO 4-frame multi-frame server payload. It can be used as a finer phase indicator to encode the client clock at the GMP mapper.
- So, $c_{n,nom} = 32*c_{m,nom}$; $c_{n,min}=32*c_{m,min}$; $c_{n,max}=32*c_{m,max}$.
- $C_m = P_{m,server}\times$[client_bit_rate/Server_Payload_bit_rate].
- C_m is an integer value indicating the number of m-bit client blocks carried in the y × FlexO 4-frame server multi-frame payload = int($P_{m,server}$ ×

[client_bit_rate/Server_Payload_bit_rate]). This value must be duplicated and have the same value in every FlexO instance carrying 100G streams from the same client.

- $C_m \leq P_{m,server}$ and is a value varying between $C_{m,min}$ and $C_{m.max}$ for the given client and payload type, due to client and payload bit rate tolerance range (±100 ppm and ±20 ppm).
- ⌊ ⌋ and ⌈ ⌉ denote the floor and ceiling operators respectively.

GMP is a positional mapping with non-fixed stuff locations. The stuff locations within the payload are determined using a delta-sigma algorithm based on the $C_m(t)$ value.

For information only, Table C.2 shows the location of the "stuff" GMP blocks for a few specific C_m values.

Table C.2 – Ethernet GMP stuff locations

C_m	~~H~~Locations
10220	N/A
10219	1
10218	1, 5111
10217	1, 3407, 6814
10216	1, 2556, 5111, 7666
10215	1, 2045, 4089, 6133, 8177
10214	1, 1704, 3407, 5111, 6814, 8517

Appendix I

Example applications

(This appendix does not form an integral part of this Recommendation.)

FlexO-x-RS-m interface group can be used for a variety of applications. Example applications for a FlexO-x-RS interface are shown in Figure I.1 and Figure I.2. An interoperable interface might represent an OTN handoff between router (R) and transport (T) nodes, or could be a handoff between different administrative domains.

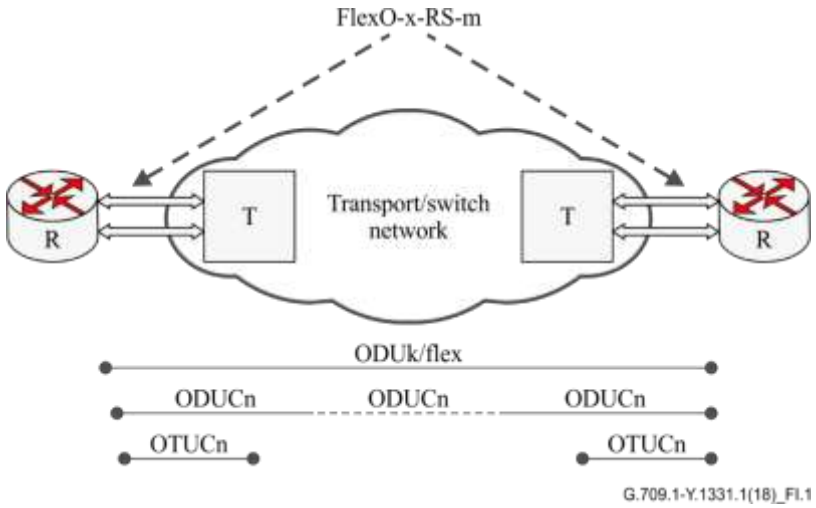

Figure I.1 – Example FlexO-x-RS handoff router-transport

The R-T topology is used in Figure I.1, to draw an analogy between FlexO-x-RS and FlexE use cases presented in [OIF FlexE]. The ODUk/flex (which can be a rate higher than 100Gbit/s) is the transport service (path) and maintenance entity in the OTN transport/switch network. The ODUCn/OTUCn is the section and FlexO-x-RS provides the interfacing capabilities (e.g., FEC, bonding and scrambling).

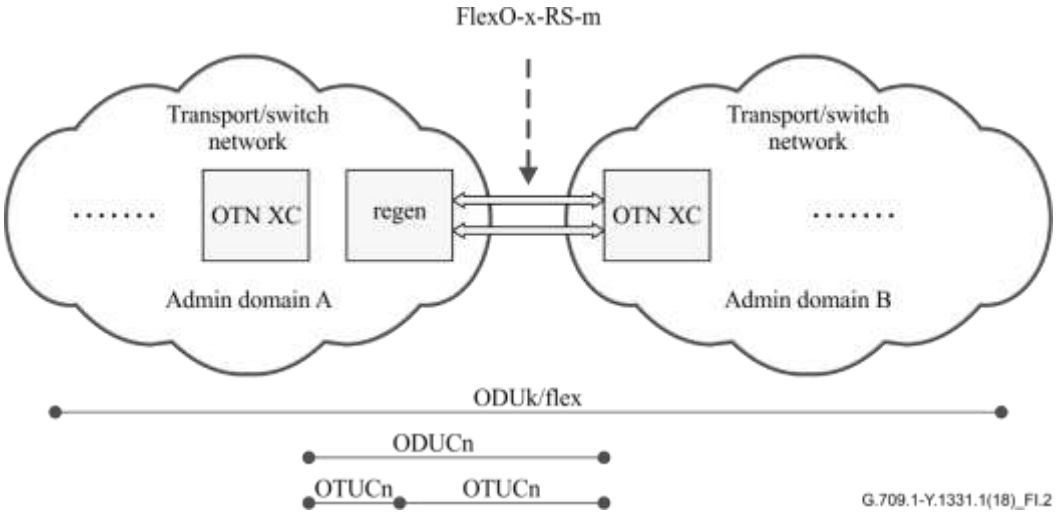

Figure I.2 – Example FlexO-x-RS inter-domain handoff

The example of Figure I.2 shows a FlexO-x-RS inter-domain interface used as a handoff between two OTN switch/transport administrative domains (A and B). The administrative domains can represent different carriers, different equipment vendors within a carrier or different segments (metro vs core) within a carrier. The OTUCn is the regenerator section, the ODUCn is the multiplexed section and the m*OTUC is the FlexO-x-RS-m interface group bonded using m FlexO-x-RS interfaces.

Bibliography

[b-ITU-T G.806] Recommendation ITU-T G.806 (2012), *Characteristics of transport equipment – Description methodology and generic functionality*.

[b-ITU-T G-Sup.58] ITU-T G-series Recommendations – Supplement 58 (~~2018~~2022), *Optical transport network (OTN) module framer interfaces (MFI).*

[b-ITU-T X.800] Recommendation ITU-T X.800 (1991), *Security architecture for Open Systems Interconnection for CCITT applications*.

[b-IEEE 1588] IEEE 1588-2008 – *IEEE Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems*.

[b-ISO/IEC 18033-3] ISO/IEC 18033-3:2010, *Information technology – Security techniques – Encryption algorithms – Part 3: Block ciphers*.

[b-OIF CEI] Optical Internetworking Forum Implementation Agreement OIF-CEI-~~04~~05.~~0~~ 1 (~~2017~~2022), *Common Electrical I/O (CEI) – Electrical and Jitter Interoperability agreements for 6G+ bps, 11G+ bps,25G+ bps, ~~and~~ 56G+ bps and 112G+ bps I/O.*

ITU-T Y-SERIES RECOMMENDATIONS

Global information infrastructure, Internet protocol aspects, next-generation networks, Internet of Things and smart cities

GLOBAL INFORMATION INFRASTRUCTURE	Y.100-Y.999
INTERNET PROTOCOL ASPECTS	Y.1000-Y.1999
General	Y.1000-Y.1099
Services and applications	Y.1100-Y.1199
Architecture, access, network capabilities and resource management	Y.1200-Y.1299
Transport	**Y.1300-Y.1399**
Interworking	Y.1400-Y.1499
Quality of service and network performance	Y.1500-Y.1599
Signalling	Y.1600-Y.1699
Operation, administration and maintenance	Y.1700-Y.1799
Charging	Y.1800-Y.1899
IPTV over NGN	Y.1900-Y.1999
NEXT GENERATION NETWORKS	Y.2000-Y.2999
FUTURE NETWORKS	Y.3000-Y.3499
CLOUD COMPUTING	Y.3500-Y.3599
BIG DATA	Y.3600-Y.3799
QUANTUM KEY DISTRIBUTION NETWORKS	Y.3800-Y.3999
INTERNET OF THINGS AND SMART CITIES AND COMMUNITIES	Y.4000-Y.4999

For further details, please refer to the list of ITU-T Recommendations.

SERIES OF ITU-T RECOMMENDATIONS

Series A	Organization of the work of ITU-T
Series D	Tariff and accounting principles and international telecommunication/ICT economic and policy issues
Series E	Overall network operation, telephone service, service operation and human factors
Series F	Non-telephone telecommunication services
Series G	**Transmission systems and media, digital systems and networks**
Series H	Audiovisual and multimedia systems
Series I	Integrated services digital network
Series J	Cable networks and transmission of television, sound programme and other multimedia signals
Series K	Protection against interference
Series L	Environment and ICTs, climate change, e-waste, energy efficiency; construction, installation and protection of cables and other elements of outside plant
Series M	Telecommunication management, including TMN and network maintenance
Series N	Maintenance: international sound programme and television transmission circuits
Series O	Specifications of measuring equipment
Series P	Telephone transmission quality, telephone installations, local line networks
Series Q	Switching and signalling, and associated measurements and tests
Series R	Telegraph transmission
Series S	Telegraph services terminal equipment
Series T	Terminals for telematic services
Series U	Telegraph switching
Series V	Data communication over the telephone network
Series X	Data networks, open system communications and security
Series Y	**Global information infrastructure, Internet protocol aspects, next-generation networks, Internet of Things and smart cities**
Series Z	Languages and general software aspects for telecommunication systems

Published in Switzerland
Geneva, 2024