International Telecommunication Union

ITU-T G.709.1/Y.1331.1
(06/2018)

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Recommendation ITU-T G.709.1/Y.1331.1

Flexible OTN short-reach interfaces

Summary

Recommendation ITU-T G.709.1/Y.1331.1 specifies a set of flexible interoperable short-reach optical transport network (OTN) interfaces over which an OTUCn (n ≥ 1) is transferred, using bonded interfaces. The Recommendation defines the frame structure for FlexO using the RS(544,514) FEC.

History

Edition	Recommendation	Approval	Study Group	Unique ID[*]
1.0	ITU-T G.709.1/Y.1331.1	2017-01-12	15	11.1002/1000/13082
2.0	ITU-T G.709.1/Y.1331.1	2018-06-22	15	11.1002/1000/13521

Keywords

FEC, FlexO, OTN, short-reach.

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[*] To access the Recommendation, type the URL http://handle.itu.int/ in the address field of your web browser, followed by the Recommendation's unique ID. For example, http://handle.itu.int/11.1002/1000/11 830-en.

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Flexible OTN short-reach interfaces

1   Scope

This Recommendation specifies a set of flexible-bandwidth interoperable short-reach optical transport network (OTN) interfaces, the so called FlexO-x-RS-m interface group, over which an aggregate OTUCn (n ≥ 1) can be transferred using bonded FlexO short-reach interfaces as lower bandwidth elements.

The types of FlexO short-reach interfaces that can serve as FlexO-x-RS-m group members are covered by application codes which are at the time of publication 4I1-9D1F, 4L1-9C1F, C4S1-9D1F, 4L1-9D1F, C4S1-4D1F, 8R1-4D1F, 4I1-4D1F and 8I1-4D1F. These application codes are presented in [ITU-T G.695] and [ITU-T G.959.1].

The definition of a FlexO-x-RS interface group complements the existing B100G functions specified in [ITU-T G.709], such as OTUCn frame, ODUk/flex, with new functions such as physical interface bonding, forward error correction (FEC) coding, group management and OTUCn (de)mapping.

This FlexO-x-RS Recommendation complements [ITU-T G.709] and [ITU-T G.798] and provides specifications for new functions that are specific to the processing of FlexO-x-RS-m interface group. In addition, some introduction material for the addressed application is included.

2   References

The following ITU-T Recommendations and other references contain provisions which, through reference in this text, constitute provisions of this Recommendation. At the time of publication, the editions indicated were valid. All Recommendations and other references are subject to revision; users of this Recommendation are therefore encouraged to investigate the possibility of applying the most recent edition of the Recommendations and other references listed below. A list of the currently valid ITU-T Recommendations is regularly published. The reference to a document within this Recommendation does not give it, as a stand-alone document, the status of a Recommendation.

[ITU-T G.695]   Recommendation ITU-T G.695 (2018), *Optical interfaces for coarse wavelength division multiplexing applications*.

[ITU-T G.709]   Recommendation ITU-T G.709/Y.1331 (2016), *Interfaces for the optical transport network*.

[ITU-T G.798]   Recommendation ITU-T G.798 (2017), *Characteristics of optical transport network hierarchy equipment functional blocks*.

[ITU-T G.870]   Recommendation ITU-T G.870/Y.1352 (2016), *Terms and definitions for optical transport networks*.

[ITU-T G.872]   Recommendation ITU-T G.872 (2017), *Architecture of optical transport networks*.

[ITU-T G.959.1]   Recommendation ITU-T G.959.1 (2018*), Optical transport network physical layer interfaces*.

[ITU-T G.7041]   Recommendation ITU-T G.7041/Y.1303 (2016*), Generic framing procedure*.

[ITU-T G.8260]   Recommendation ITU-T G.8260 (2015), *Definitions and terminology for synchronization in packet networks*.

[IEEE 802.3]	IEEE Std. 802.3:2015, IEEE *Standard for Information Technology – Telecommunications and Information Exchange Between Systems – Local and Metropolitan Area Networks – Specific Requirements Part 3: Carrier Sense Multiple Access With Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications*.
[IEEE 802.3bs]	IEEE Std 802.3bs-2017, IEEE *Standard for Ethernet Amendment 10: Media Access Control Parameters, Physical Layers and Management Parameters for 200 Gb/s and 400 Gb/s Operation*.
[OIF FlexE]	Optical Interworking Forum, OIF (2017), *FlexEthernet Implementation Agreement 1.1*.

3 Definitions

3.1 Terms defined elsewhere

This Recommendation uses the following terms defined elsewhere:

3.1.1 Terms defined in [ITU-T G.870]:

– completely standardized OTUCn (OTUCn)

– optical data unit (ODUCn)

– optical payload unit (OPUCn)

– optical transport network (OTN)

3.2 Terms defined in this Recommendation

This Recommendation defines the following terms:

3.2.1 **FlexO**: Information structure with a specific bit rate and frame format, consisting of overhead and payload, intended to be used in a group with n (n ≥ 1) instances for the transport of an OTUCn signal.

3.2.2 **FlexO-x**: Information structure consisting of x (x ≥ 1) 10-bit interleaved FlexO instances, intended to be used in a group with m (m = $\lceil$ n/x $\rceil$) instances for the transport of an OTUCn signal. The order x signifies the FlexO-x interface rate in units of 100G. Specific variants are 100G FlexO-1, 200G FlexO-2 and 400G FlexO-4.

3.2.3 **FlexO-x-RS**: Information structure consisting of a FlexO-x plus Reed-Solomon FEC parity.

3.2.4 **FlexO-x-RS interface**: Refers to an individual member interface that is part of a FlexO-x-RS-m interface group.

NOTE – The terms "member" and "PHY" are often used to refer to a FlexO-x interface.

3.2.5 **FlexO-x-RS-m interface group**: Refers to the group of m * FlexO-x-RS interfaces.

NOTE – The text may use "FlexO group" as short-hand for FlexO interface group.

3.2.6 **FOICx.k-RS**: Refers to a FlexO-x-RS interface using k parallel FOICx.k-RS lanes.

NOTE – "FOICx.k" is the FlexO equivalent of "OTLk.m" for OTUk as defined in [ITU-T G.709].

3.2.7 **FOICx.k-RS lane**: Refers to an electrical/optical lane of a FlexO-x-RS interface.

4 Abbreviations and acronyms

This Recommendation uses the following abbreviations and acronyms:

AM   Alignment Marker

B100G	Beyond 100G
BMP	Bit-synchronous Mapping Procedure
CAUI	(Chip to) 100 Gb/s Attachment Unit Interface
CFP2	C (100G) Form-factor Pluggable Optical Module
CM	Common Marker
CRC	Cyclic Redundancy Check
FA	Frame Alignment
FAS	Frame Alignment Signal
FCC	FlexO Communications Channel
FEC	Forward Error Correction
FlexE	Flexible Ethernet
FlexO	Flexible Optical Transport Network
FOIC-RS	FlexO-x-RS Interface
GFP	Generic Framing Procedure
GID	Group Identification
IA	Implementation Agreement
LSB	Least Significant Bit
MAP	PHY Map field
MFAS	Multi-Frame Alignment Signal
MS	Multiplexed Section
MSB	Most Significant Bit
ODU	Optical Data Unit
OH	Overhead
OPU	Optical Payload Unit
OSMC	OTN Synchronization Messaging Channel
OTL	Optical Transport Lane
OTN	Optical Transport Network
OTU	Optical Transport Unit
PCS	Physical Coding Sublayer
PHY	Physical Layer
PID	PHY Identification
PTP	Precise Timing Protocol
QSFP28	Quad (100G) Small Form-factor Pluggable
RES	Reserved for Future International Standardization
RPF	Remote Physical Layer Fault
RS	Reed-Solomon
SM	Section Monitoring

SSM   Synchronization Status Message

STAT   Status

UM   Unique Marker

UP   Unique Padding

5   Conventions

This Recommendation uses the following conventions:

k: The index "k" is used to represent a supported bit rate and the different versions of OPUk, ODUk and OTUk. Example for k are "1" for an approximate bit rate of 2.5 Gbit/s, "2" for an approximate bit rate of 10 Gbit/s, and "3" for an approximate bit rate of 40 Gbit/s.

Cn: The index Cn is used for $n \times 100G$ (C=100G).

m: The index "m" is used to represent the bit rate or set of bit rates supported on the interface. This is one or more digits "k", where each "k" represents a particular bit rate. For example, valid values for m are (1, 2, 3, 12, 123, 23).

n: The index "n" is used to represent the order of the OTM, OTS, OMS, OPS, OCG, OMU. n represents the maximum number of wavelengths that can be supported at the lowest bit rate supported on the wavelength. It is possible that a reduced number of higher bit rate wavelengths are supported. n = 0 represents the case of a single channel without a specific colour assigned to the channel.

r: The index "r", if present, is used to indicate a reduced functionality OTM, OCG, OCC and OCh (non-associated overhead is not supported). Note that for n = 0 the index r is not required as it implies always reduced functionality.

Transmission order: The order of transmission of information in all the diagrams in this Recommendation is first from left to right and then from top to bottom. Within each byte the most significant bit is transmitted first. The most significant bit (bit 1) is illustrated on the left side of all diagrams.

Value of reserved bit(s):   The value of an overhead bit, which is reserved for future international standardization, shall be set to "0".

Value of non-sourced bit(s):   Unless stated otherwise, any non-sourced bits shall be set to "0".

6   Introduction and applications

A FlexO-x-RS-m (Flexible OTN short reach) interface group is defined for interoperable multi-vendor applications. It complements B100G (beyond 100G) [ITU-T G.709], by providing an interoperable interface for OTUCn transport signals. A FlexO-x-RS-m interface group provides modularity by bonding standard-rate interfaces (e.g., m × 100G), over which the OTUCn (n ≥ 1) signal is adapted. The value of m is not standardized. The specification of OTUCn in [ITU-T G.709] excludes interface specific functions such as FEC, scrambling and bit alignment. A FlexO-x-RS interface or a FlexO-x-RS-m group wraps OTUCn, abstracting the transport signal from the interface. FlexO-x-RS-m enables ODUflex services >100Gbit/s to be supported across multiple interfaces, ahead of next generation interface standards such as 400GE [IEEE 802.3bs].

FlexO-x-RS provides OTN interfaces with comparable functionality to what was introduced in [OIF FlexE] for Ethernet interfaces.

Example applications are provided in Appendix I.

6.1 FlexO-x-RS-m interface group considerations

Considerations and capabilities for a FlexO-x-RS-m interface group:

– provides an interoperable system interface for OTUCn transport signals;

– enables higher capacity ODUflex and OTUCn, by means of bonding m standard-rate interfaces;

– provides interface rate modularity and flexibility;

– provides a frame, alignment, deskew, group management, management communication channel and such functions that are not associated with the OTUCn transport signal; and

– reuses 100G modules (e.g., CFP2, QSFP28) by matching the interface rate to OTU4 as specified in [ITU-T G.709].

The rate-specific FlexO-x-RS interfaces specified in this Recommendation are located at a system external reference point.

NOTE – The logical signal format FOICx.k-RS can be reused on a system internal interface (module framer interface). Related requirements and any optimizations to the FlexO-x-RS-m groups when used as intra-system interface (e.g., lower latency by removing FEC) are beyond the scope of this Recommendation and covered in [b-ITU-T G-Sup.58].

7 Structure and processes

This clause introduces the functions associated with a FlexO-x-RS interface group and the basic signal structure, processes and atomic functions.

7.1 Basic signal structure

The FlexO-x-RS-m interface group in this Recommendation is only specified for short-reach applications. The FlexO-x-RS-m interface group functional model is specified in [ITU-T G.872]. The physical optical interface specifications are beyond the scope of this Recommendation.

The information structure for FlexO-x-RS-m interface group is represented by information containment relationships and flows. The principal information containment relationship is described in Figure 7-1.

One OTUCn signal is mapped into n FlexO signals, each FlexO signal containing one OTUC instance. The n FlexO instances are mapped into m (m ≤ n) FlexO-x-RS interfaces, each FlexO-x-RS interface containing one FlexO instance or multiple, interleaved FlexO instances plus FEC. Each FlexO-x-RS interface is split into k FlexO-x-RS lane signals. Each lane signal is modulated onto one OTSi and the k OTSi's are transported as an OTSiG via one media element.
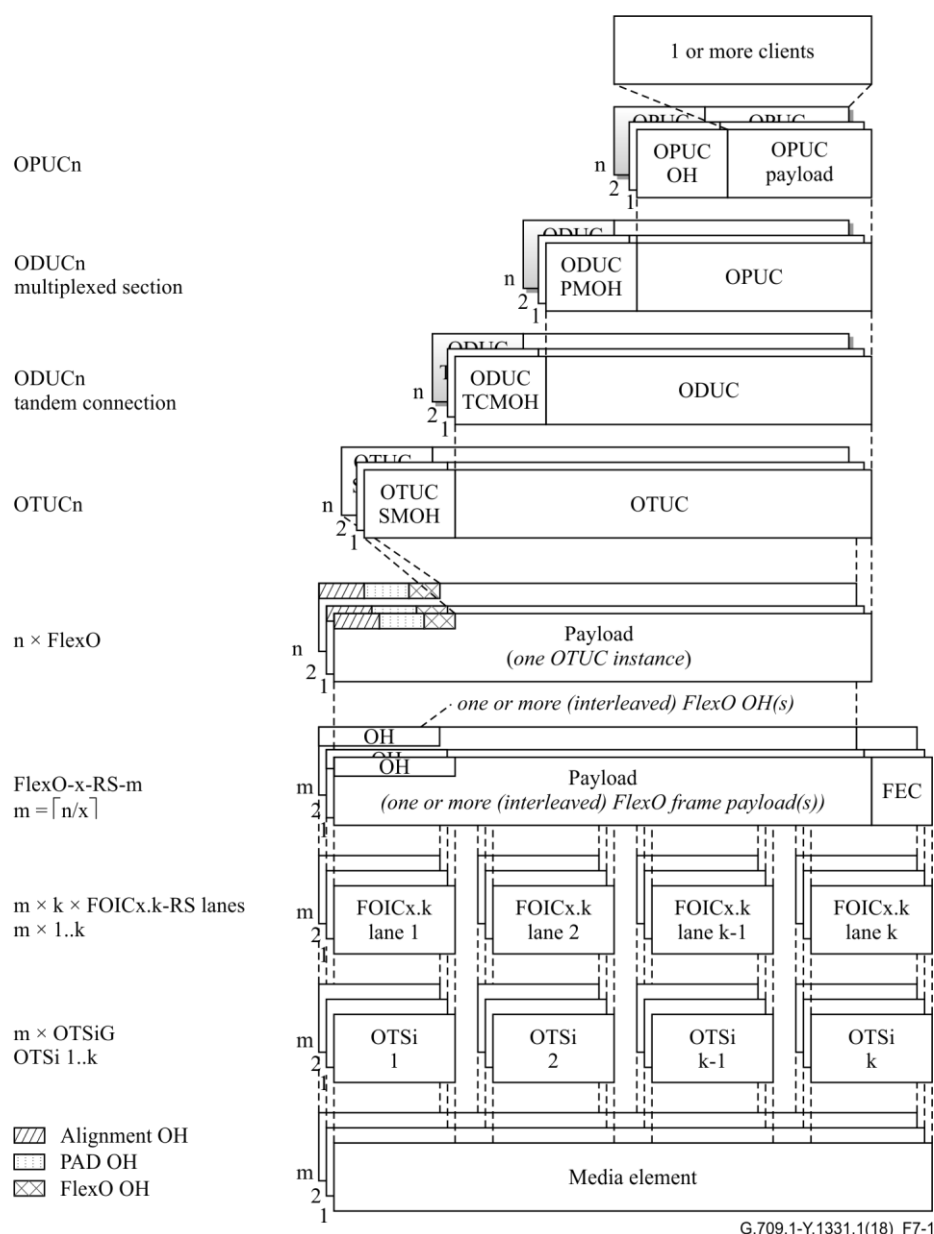
OPUCn

OPUC OH | OPUC payload

ODUCn
multiplexed section

ODUC PMOH | OPUC

ODUCn
tandem connection

ODUC TCMOH | ODUC

OTUCn

OTUC SMOH | OTUC

n × FlexO

Payload
(one OTUC instance)

one or more (interleaved) FlexO OH(s)

FlexO-x-RS-m
$m = \lceil n/x \rceil$

OH

OH

Payload
(one or more (interleaved) FlexO frame payload(s)) | FEC

m × k × FOICx.k-RS lanes
m × 1..k

FOICx.k lane 1 | FOICx.k lane 2 | FOICx.k lane k-1 | FOICx.k lane k

m × OTSiG
OTSi 1..k

OTSi 1 | OTSi 2 | OTSi k-1 | OTSi k

▨ Alignment OH
▨ PAD OH
▨ FlexO OH

Media element

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Figure 7-1 – FlexO-x-RS-m interface group principal information containment relationship

7.2 Processing and information flow

Functions, processed and information flows are more formally specified in [ITU-T G.798].

8 FlexO frame

A FlexO frame is associated with a FlexO-x-RS interface and is independent of an OTUCn frame boundary and transport unit, the latter being specified in [ITU-T G.709].

NOTE – The OTUCn is the transport unit over OTN interfaces and consists of n OTUC frames. It is specified in [ITU-T G.709].

A FlexO frame consists of frame alignment marker area (AM), pad area (PAD), overhead area (OH) and payload area.

The FlexO frames carried over m interfaces of a FlexO-x-RS-m interface group are frame/multi-frame aligned at the source.

8.1 Frame structure

The FlexO frame structure is shown in Figure 8-1 and consists of 128 rows by 5,140 1-bit columns. It contains a frame alignment marker group area (AM) in row 1, columns 1 to 480, a pad area (PAD) in row 1, columns 481 to 960 per 100G instance, an overhead area (OH) in row 1 columns 961 to 1280 and a ($128 \times 5140 - 1280 = 656640$ bit) payload area in the remainder of the frame.

NOTE – The FlexO frame structure is derived from 100Gbit/s Ethernet clause 91 [IEEE 802.3] FEC alignment and lane architecture, without any 66b alignment or 256b/257b transcoding functions.
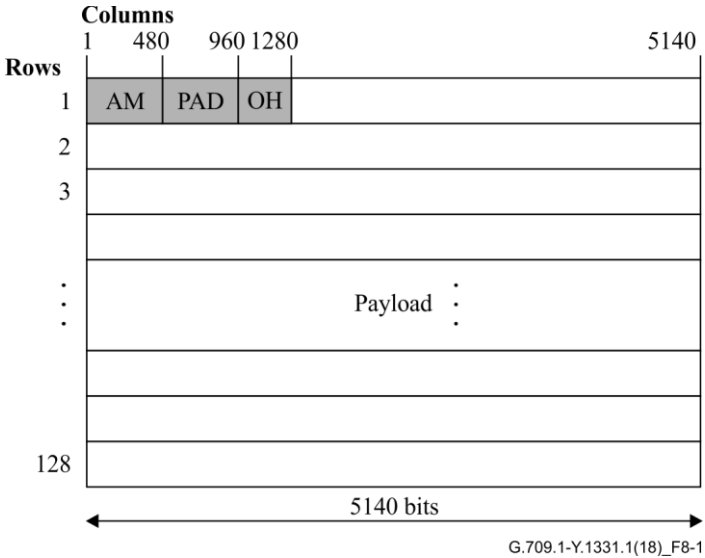

Figure 8-1 – FlexO frame structure

8.2 Multi-frame structure

In order to pad the payload area and provide space for additional OH fields, an 8-frame FlexO multi-frame structure is defined. The FlexO multi-frame structure is shown in Figure 8-2. It uses the three least significant bits of the multi-frame alignment signal (MFAS) overhead to identify the eight frames within the multi-frame.

The multi-frame contains seven fixed stuff locations in the payload area of FlexO frames, each containing 1,280 bits. These fixed-stuff locations are located in row 65, columns 1 to 1,280 of the first seven frames within the multi-frame. The last frame within the multi-frame does not contain fixed stuff.

The fixed stuff bits are filled with all-0s and not checked at the receiver sink function.

The FlexO multi-frame payload, excluding the fixed stuff (FS) locations, consists of 5,244,160 bits (655,520 bytes) out of the total 5,263,360 bits (657,920 bytes) per FlexO multi-frame.
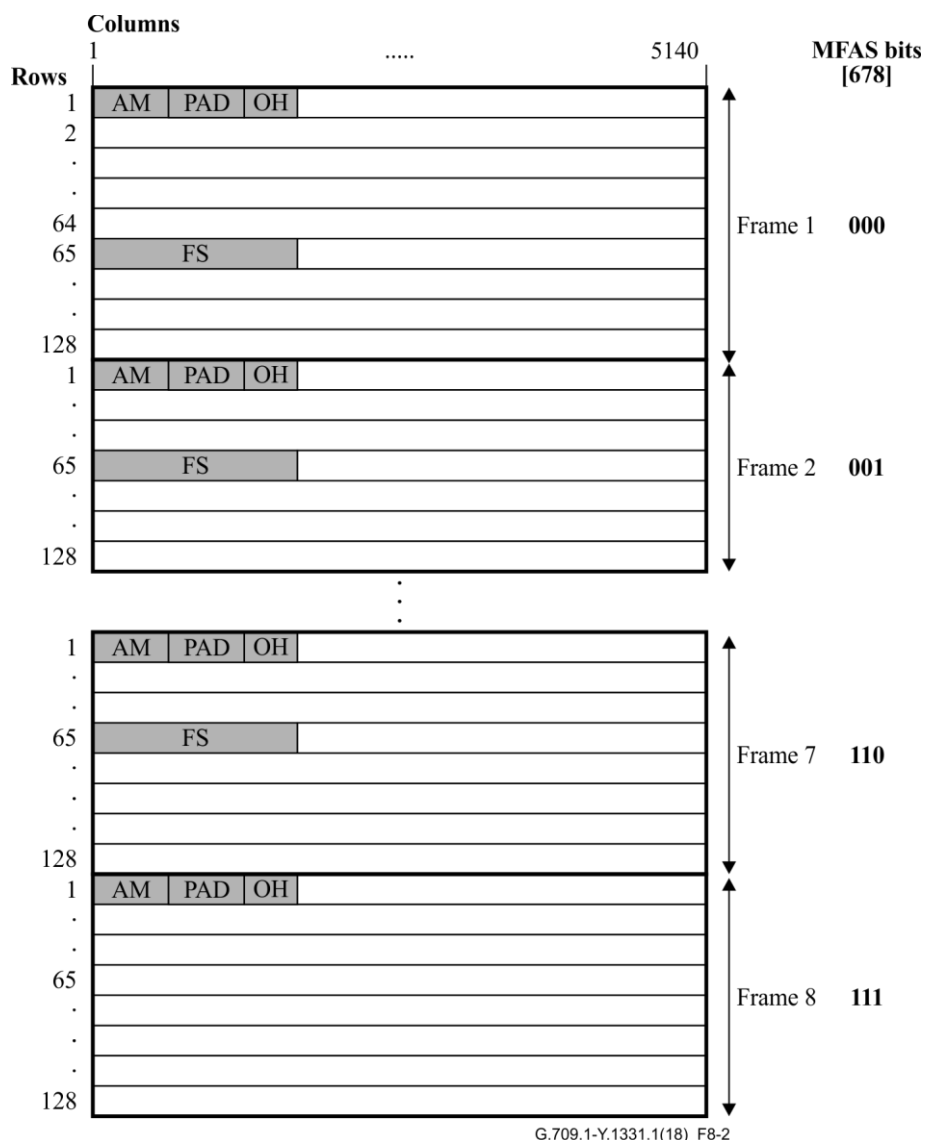
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Figure 8-2 – FlexO multi-frame structure

8.3 Bit rates and frame periods

The bit rate and tolerance of the FlexO signal is defined in Table 8-1.

Table 8-1 – FlexO bit rate

FlexO nominal bit rate	FlexO bit-rate tolerance
491384/462961 × 99 532 800 kbit/s	±20 ppm
NOTE 1 – The nominal FlexO bit rate is approximately: 105 643 510.782 kbit/s. NOTE 2 – The FlexO bit rate can be based on the OTUC bit rate as follows: 4112/4097 × OTUC bit rate = 4112/4097 × 239/226 × 99 532 800 kbit/s.	

The frame and multi-frame periods of the FlexO signal are defined in Table 8-2.

Table 8-2 – FlexO frame and multi-frame periods

Frame period (Note)	Multi-frame period (Note)
~6.228 µs	49.822 µs
NOTE – The period is an approximated value, rounded to 3 decimal places.	

9 Alignment markers and overhead

The FlexO frame overhead consists of alignment markers (AM), padding (PAD), group management, synchronization and communication channel fields. FlexO overhead areas in an elementary FlexO frame consist of 1,280 bits per 100G FlexO instance. It includes information to support group management and alignment functions. The FlexO overhead is terminated where the FlexO frame is assembled and disassembled.

The aggregate frame of a higher rate FlexO-x-RS interface is constructed by interleaving multiple FlexO frame instances.

An overview of FlexO overhead areas is presented in Figure 9-1. The term OH refers to the 320-bit field following the PAD.
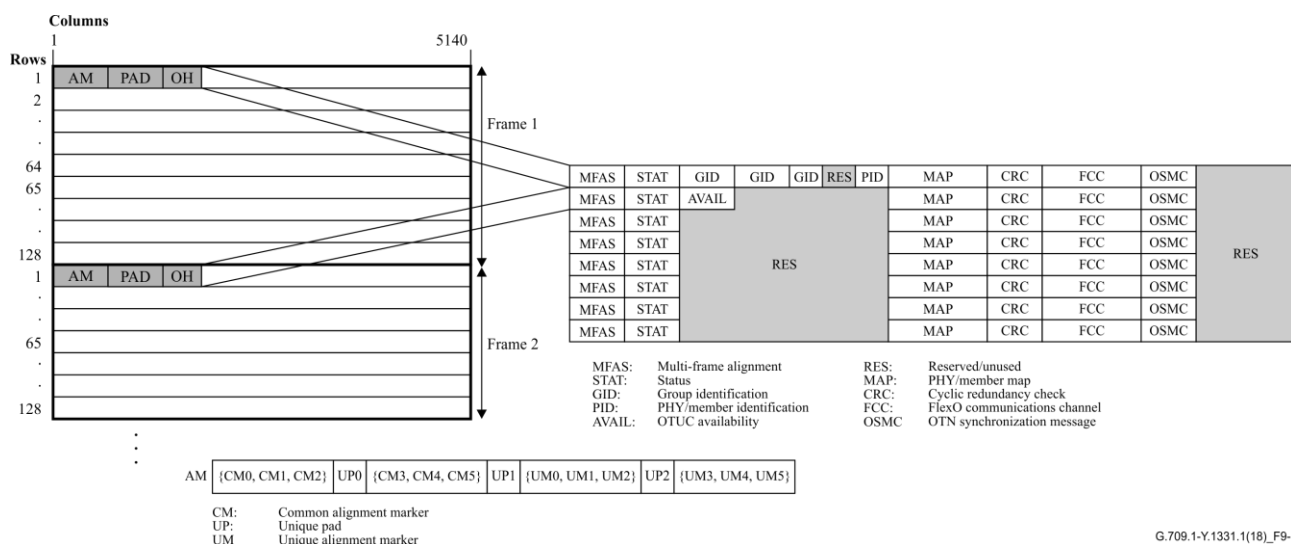

Figure 9-1 – Overhead overview

9.1 Lane alignment markers

Lane alignment markers are used for lane alignment, lane delineation, lane ordering and lane deskewing.

The alignment marker (AM) area length for a FlexO frame is defined as 480 bits, which holds four 120-bit lane alignment markers.

A lane alignment marker, as shown in Figure 9-2, consists of a common portion across all lanes, a unique portion per lane and some pad bits.

– CMx = 8-bit common marker field (common across lanes) – used for aligning lanes

– UMx = 8-bit unique marker field – used for identifying lanes

– UPx = 8-bit unique pad field – used for providing a DC balance when multiplexing lanes.

NOTE – Alignment marker area length specified by clause 91 [IEEE 802.3] for 100 Gbit/s Ethernet interfaces, is 1285-bit per AM FEC frame period (every 4096 FEC codewords). It consists of 20 AM blocks

of 64-bit, plus 5-bit extra padding required for 257b block alignment. Since the FlexO adaptation method described in this document does not rely on 257b blocks, the five padding bits are unnecessary.
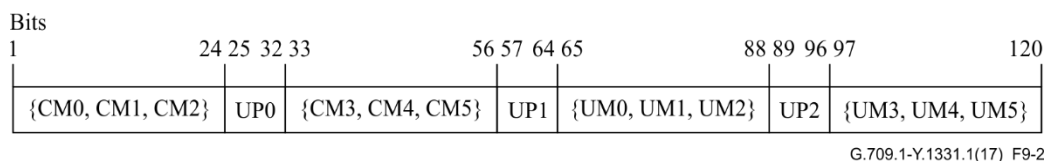

Figure 9-2 – FOICx.k lane alignment marker format

9.1.1 FlexO-1 alignment markers

The 100G FlexO-1 frame signal supports subsequent distribution into four logical lanes, numbered 0, 1, 2 and 3. Each lane carries a 120-bit lane alignment marker (am_i, i = 0,1,2,3) as specified in Table 9-1. Rows of Table 9-1 give the values of am_i transmitted over logical lane i.

The 480-bit FlexO-1 alignment marker area contains 10-bit interleaved parts of am_0, am_1, am_2 and am_3 as illustrated in Figure 9-3. The 480 bits contain the 10-bit interleaved parts of am_0 to am_3 in the order am_0, am_1, am_2, am_3, am_0, am_1, etc.
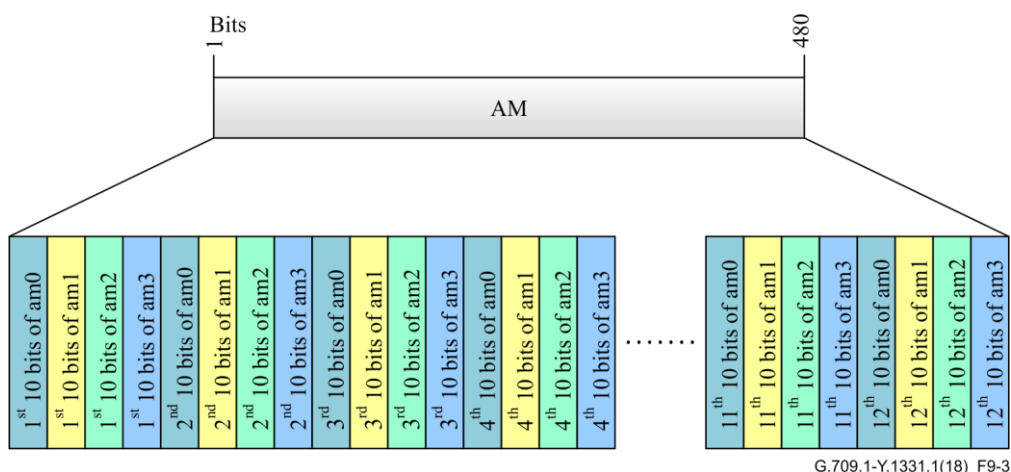

Figure 9-3 – 100G FlexO alignment marker area with four interleaved lane alignment markers

Table 9-1 – FlexO-1 alignment marker encodings

logical lane	Encoding														
	{CM0, CM1, CM2, UP0, CM3, CM4, CM5, UP1, UM0, UM1, UM2, UP2, UM3, UM4, UM5}														
0	59	52	64	6D	A6	AD	9B	9B	80	8E	CF	64	7F	71	30
1	59	52	64	20	A6	AD	9B	E6	5A	7B	7E	19	A5	84	81
2	59	52	64	62	A6	AD	9B	7F	7C	CF	6A	80	83	30	95
3	59	52	64	5A	A6	AD	9B	21	61	01	0B	DE	9E	FE	F4

NOTE – The value in each byte of this Table is in MSB-first transmission order. Note that this per-byte bit ordering is the reverse of AM values found in [IEEE 802.3bs], which uses an LSB-first bit transmission format.

9.1.2 100G FlexO PAD

The FlexO frame signal supports subsequent distribution of PADs into four logical lanes, numbered 0, 1, 2 and 3. Each lane carries a 120-bit pad (pad_i, i = 0,1,2,3). The values of the pads are all-0s.

The 480-bit 100G FlexO PAD area contains 10-bit interleaved parts of pad_0, pad_1, pad_2 and pad_3 as illustrated in Figure 9-4. The 480 bits contain the 10-bit interleaved parts of pad_0 to pad3 in the order pad_0, pad_1, pad_2, pad_3, pad_0, pad_1, etc.
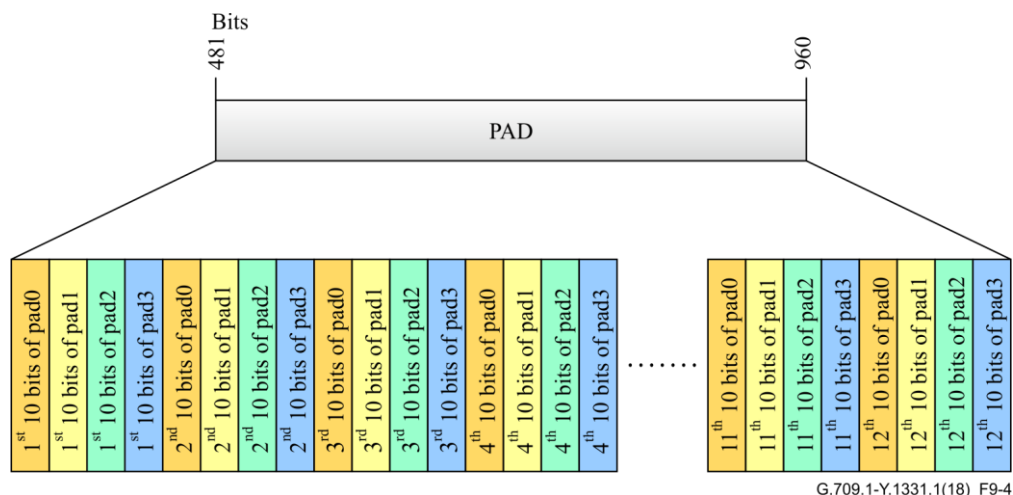

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Figure 9-4 – 100G FlexO PAD area with four interleaved lane padding

9.1.3 FlexO-2 alignment markers

The 200G FlexO-2 frame signal supports subsequent distribution into eight logical lanes, numbered 0, 1, 2 to 7. Each lane carries a 120-bit lane alignment marker (am_i, i = 0,1,2 to 7) as specified in Table 9-2. Rows of Table 9-2 give the values of am_i transmitted over logical lane i.

The 960-bit FlexO-2 alignment marker group area contains 10-bit interleaved parts of am_0, am_1, am_2, am_3, am_4, am_5, am_6 and am_7 as illustrated in Figure 9-5. The 480 bits of the first 100G FlexO-1 instance contain the 10-bit interleaved parts of am_0 to am_7 in the order am_0, am_2, am_4, am_6, am_1, am_3, am_5, am_7, etc. The 480 bits of the second 100G FlexO-1 instance contain the 10-bit interleaved parts of am_0 to am_7 in the order am_1, am_3, am_5, am_7, am_0, am_2, am_4, am_6, etc.
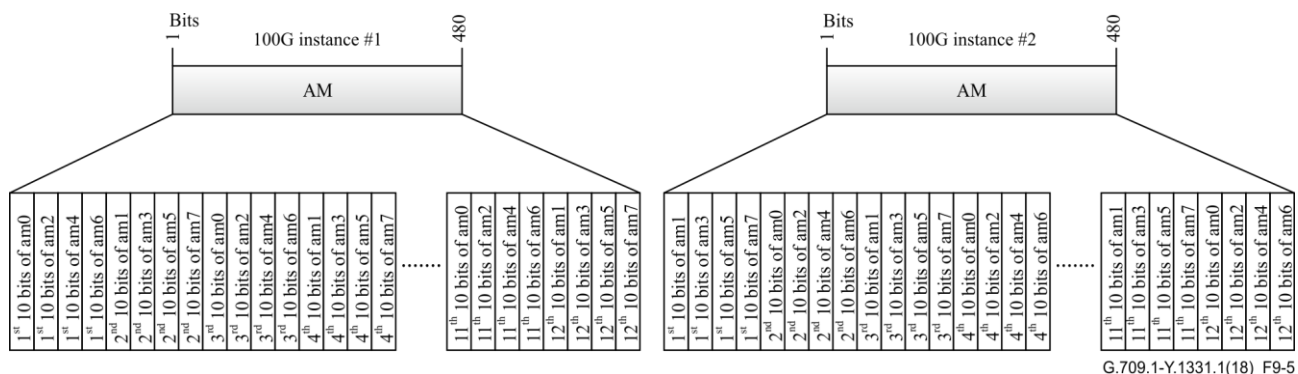

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Figure 9-5 – 200G FlexO alignment marker area with eight interleaved lane alignment markers

Table 9-2 – FlexO-2 alignment marker encodings

logical lane	Encoding {CM0, CM1, CM2, UP0, CM3, CM4, CM5, UP1, UM0, UM1, UM2, UP2, UM3, UM4, UM5}														
0	59	52	64	A0	A6	AD	9B	6B	CD	03	31	94	32	FC	CE
1	59	52	64	20	A6	AD	9B	E6	5A	7B	7E	19	A5	84	81
2	59	52	64	62	A6	AD	9B	7F	7C	CF	6A	80	83	30	95
3	59	52	64	5A	A6	AD	9B	21	61	01	0B	DE	9E	FE	F4
4	59	52	64	87	A6	AD	9B	98	54	8A	4F	67	AB	75	B0
5	59	52	64	45	A6	AD	9B	72	48	F2	8B	8D	B7	0D	74
6	59	52	64	BC	A6	AD	9B	77	42	39	85	88	BD	C6	7A
7	59	52	64	44	A6	AD	9B	4C	6B	6E	DA	B3	94	91	25

NOTE – The value in each byte of this Table is in MSB-first transmission order. Note that this per-byte bit ordering is the reverse of AM values found in [IEEE 802.3bs], which uses an LSB-first bit transmission format.

9.1.4 FlexO-2 PAD

Each instance of 200G FlexO-2-RS frame structure carries a 480-bit PAD field with all-0's value in row 1 and columns 481 to 960 as illustrated in Figure 12-1.

9.1.5 FlexO-4 alignment markers

The 400G FlexO-4 frame signal supports subsequent distribution into sixteen logical lanes, numbered 0, 1, 2 to 15. Each lane carries a 120-bit lane alignment marker (am_i, i = 0,1,2 to 15) as specified in Table 9-3. Rows of Table 9-3 give the values of am_i transmitted over logical lane i.

The 1920-bit FlexO-4 alignment marker group area contains 10-bit interleaved parts of am_0, am_1, am_2, am_3, am_4, am_5, am_6, am_7, am_8, am_9, am_{10}, am_{11}, am_{12}, am_{13}, am_{14} and am_{15} as illustrated in Figure 9-6. The 960 bits of the first 200G FlexO-2 instance contain the 10-bit interleaved parts of am_0 to am_{15} in the order am_0, am_2, am_4, am_6, am_8, am_{10}, am_{12}, am_{14}, am_1, am_3, am_5, am_7, am_9, am_{11}, am_{13}, am_{15}, etc. The 960 bits of the second 200G FlexO-2 instance contain the 10-bit interleaved parts of am_0 to am_{15} in the order am_1, am_3, am_5, am_7, am_9, am_{11}, am_{13}, am_{15}, am_0, am_2, am_4, am_6, am_8, am_{10}, am_{12}, am_{14}, etc.
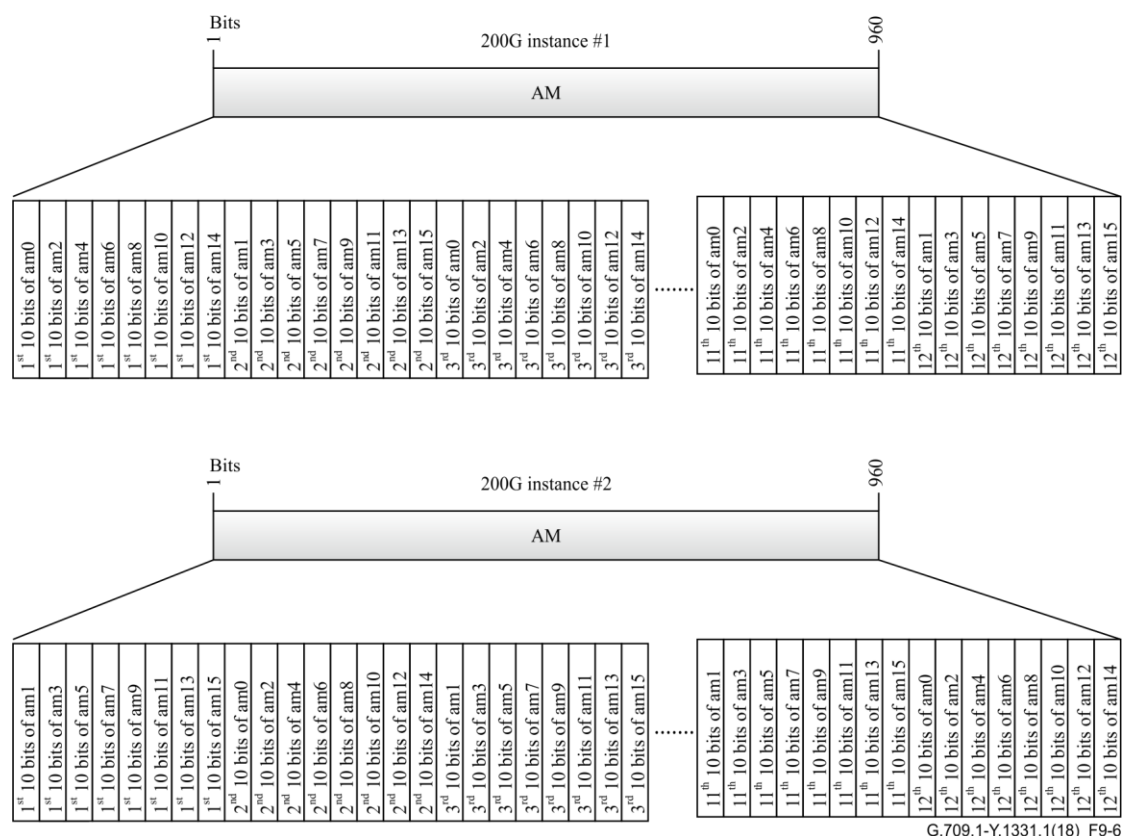
Figure 9-6 – 400G FlexO alignment marker area with sixteen interleaved lane alignment markers

Table 9-3 – FlexO-4 alignment marker encodings

logical lane	Encoding {CM0, CM1, CM2, UP0, CM3, CM4, CM5, UP1, UM0, UM1, UM2, UP2, UM3, UM4, UM5}														
0	59	52	64	6D	A6	AD	9B	9B	80	8E	CF	64	7F	71	30
1	59	52	64	20	A6	AD	9B	E6	5A	7B	7E	19	A5	84	81
2	59	52	64	62	A6	AD	9B	7F	7C	CF	6A	80	83	30	95
3	59	52	64	5A	A6	AD	9B	21	61	01	0B	DE	9E	FE	F4
4	59	52	64	87	A6	AD	9B	98	54	8A	4F	67	AB	75	B0
5	59	52	64	4F	A6	AD	9B	72	48	F2	8B	8D	B7	0D	74
6	59	52	64	BC	A6	AD	9B	77	42	39	85	88	BD	C6	7A
7	59	52	64	44	A6	AD	9B	4C	6B	6E	DA	B3	94	91	25
8	59	52	64	06	A6	AD	9B	F9	87	CE	AE	06	78	31	51
9	59	52	64	D6	A6	AD	9B	45	8E	23	3C	BA	71	DC	C3
10	59	52	64	5F	A6	AD	9B	20	A9	D7	1B	DF	56	28	E4
11	59	52	64	36	A6	AD	9B	8E	44	66	1C	71	BB	99	E3
12	59	52	64	18	A6	AD	9B	DA	45	6F	A9	25	BA	90	56
13	59	52	64	28	A6	AD	9B	33	8C	E9	C3	CC	73	16	3C
14	59	52	64	0B	A6	AD	9B	8D	53	DF	65	72	AC	20	9A
15	59	52	64	2D	A6	AD	9B	6A	65	5D	9E	95	9A	A2	61

NOTE – The value in each byte of this Table is in MSB-first transmission order. Note that this per-byte bit ordering is the reverse of AM values found in [IEEE 802.3bs], which uses an LSB-first bit transmission format.

9.1.6 FlexO-4 PAD

Each 400G FlexO-4-RS frame structure carries a 960-bit PAD field with all-0's value in row 1 and columns 961 to 1920 as illustrated in Figure 13-1.

9.2 Overhead description

The FlexO OH area is contained in the 320 bits following the FlexO frame AM area. The OH structure amounts to 2,560 bits (320 bytes) and is distributed across an 8-frame multi-frame, as shown in Figure 9-7. Each frame contains 40 OH bytes.
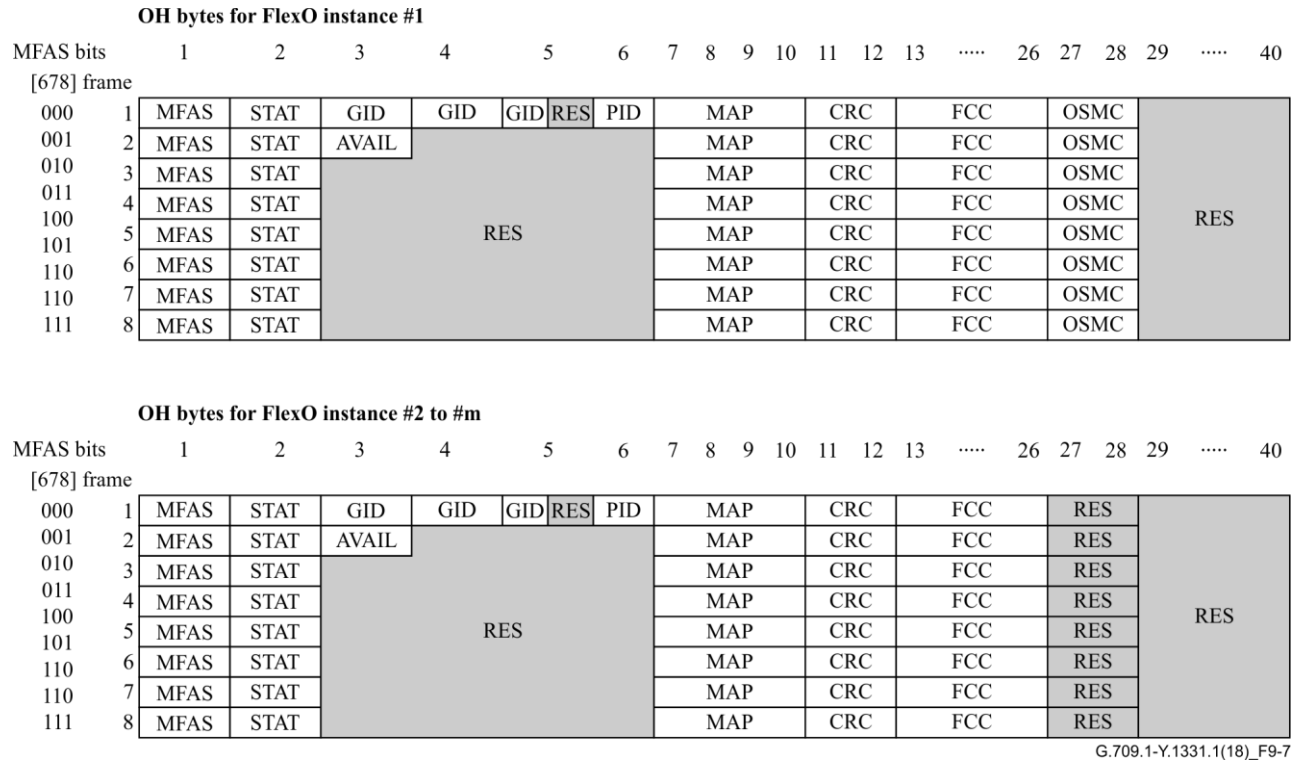

Figure 9-7 – FlexO OH structure

The FlexO OH area contains the following subfields (see Figure 9-7):

– multi-frame alignment signal (MFAS)

– status (STAT)

– group identification (GID)

– PHY identification (PID)

– PHY map (MAP)

– OTUC availability (AVAIL)

– cyclic redundancy check (CRC)

– FlexO management communication channel (FCC)

– bits reserved for future international standardization (RES)

– OTN synchronisation message channel (OSMC)

NOTE – AVAIL field is unused and only required for 100G interfaces.

9.2.1 Multi-frame alignment signal (MFAS)

An 8-bit (1 byte) multi-frame alignment signal field is provided and incremented in every FlexO frame. This MFAS field counts 0x00 to 0xFF and provides a 256-frame FlexO multi-frame. This central multi-frame is used to lock 2-frame, 4-frame, 8-frame, 16-frame, 32-frame, etc. multi-frame structures of overhead and payload structure to the principal frame. The MFAS sequence is shown in Figure 9-8.

Figure 9-8 – Multi-frame alignment signal overhead

The MFAS field is located in all FlexO frames, in overhead byte 1 immediately following the AM.

9.2.2 Group identification (GID)

A 20-bit (2.5 bytes) FlexO group identification (GID) field is provided to indicate the interface group instance that the FlexO-x-RS interface is a member of. The GID provides the ability to check at the receive side that the interface belongs to the intended FlexO group.

The GID field is located in frame 1, in overhead bytes 3, 4 and 5.

The same FlexO group identification value is used in both directions of transport.

Non-zero values for GID are valid and the value of "0" is reserved for this field.

A FlexO-x-RS interface that is not part of any group has its GID value set to "0".

9.2.3 PHY identification (PID)

A FlexO-x-RS-m interface group is composed of m FlexO-x-RS interfaces, also referred to as members or PHYs. An 8-bit (1 byte) field is provided to uniquely identify each member of a group and the order of each member in the group. This information is required in the reordering process.

The PID values of the interfaces in a FlexO group are not necessarily arranged consecutively. The PID values indicate the order of the interfaces within the FlexO group, from low to high. The first FlexO-x-RS interface in the group is the one with the lowest PID value.

The PID field is located in frame 1, in overhead byte 6. The values "0" and "255" are reserved for this field.

The same FlexO PHY identification value is used in both directions of transport.

A FlexO-x-RS interface that is not part of any group has its PID value default to "0".

9.2.4 PHY map (MAP)

A 256-bit (8 bytes) field is provided to indicate the members belonging to the group. Each bit in the field, is set to "1" indicating a member/PHY is part of the group. The bit position of the MAP

corresponds to the PID set for the member FlexO-x-RS interface, with the most significant bit (MSB) corresponding to lowest numbered PID. The remaining unused fields in the MAP are set to "0". The full MAP is sent and received on all members of the group.

The MAP field is located in all frames, in overhead bytes 7, 8, 9 and 10. As shown in Figure 9-9, the MSB of overhead byte 7 in frame 1 is associated with PID #0 and the least significant bit (LSB) of overhead byte 10 in frame 8 is associated with PID #255.

Figure 9-9 – FlexO PHY MAP field

9.2.5 Status (STAT)

An 8-bit (1 byte) field, as shown in Figure 9-10, is provided for general purpose status indication.
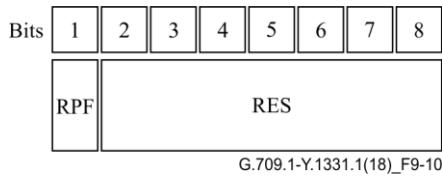
− Remote PHY Fault

− Reserved

Figure 9-10 – FlexO OH STAT field

The STAT field is located in all frames, in overhead byte 2 as shown in Figure 9-7.

9.2.5.1 Remote PHY fault (RPF)

For section monitoring, a single bit remote PHY fault (RPF) indication conveys the signal fail status detected at the remote FlexO sink function in the upstream direction.

RPF is set to "1" to indicate a remote PHY defect indication; otherwise, it is set to "0".

The RPF field is located in bit 1 of the STAT field as shown in Figure 9-10.

9.2.5.2 Reserved (RES)

Seven bits of the STAT byte are reserved for future international standardization as shown in Figure 9-10. These bits are set to "0".

9.2.6 OTUC availability (AVAIL)

The AVAIL field is unused and should be set to a value of 1 for FlexO-1-RS 100G interfaces. For other x != 1 interface rates, it is reserved.

The AVAIL field is located in frame 2, in overhead byte 3.

9.2.7 Cyclic redundancy check (CRC)

The CRC-16 (2 bytes) is located in overhead bytes 11 and 12 of each FlexO frame. The CRC protects the integrity of the OH fields in bytes 2 to 10 and excludes the MFAS, OSMC and FCC fields. The CRC-16 uses the $G(x) = x^{16} + x^6 + x^5 + x^3 + 1$ generator polynomial and is calculated as follows:

1)   The overhead bytes 2 to 10 of the OH frame are taken in network byte order, most significant bit first, to form a 72-bit pattern representing the coefficients of a polynomial $M(x)$ of degree 71.

2) $M(x)$ is multiplied by x^{16} and divided (modulo 2) by $G(x)$, producing a remainder $R(x)$ of degree 15 or less.

3)   The coefficients of $R(x)$ are considered to be a 16-bit sequence, where x^{15} is the most significant bit.

4)   This 16-bit sequence is the CRC-16 where the first bit of the CRC-16 to be transmitted is the coefficient of x^{15} and the last bit transmitted is the coefficient of x^0.

The demapper process performs steps 1-3 in the same manner as the mapper process, except that here, the $M(x)$ polynomial of step 1 includes the CRC-16 bits in received order and has degree 87. In the absence of bit errors, the remainder shall be 0.

9.2.8 FlexO management communications channel (FCC)

An 896-bit (112 bytes) field per multi-frame is provided for a FlexO-x-RS interface management communications channel. As shown in Figure 9-11, these fields are allocated across all 8 frames of the multi-frame. This provides a clear channel. Format and content of the management channel is outside the scope of this recommendation.

NOTE – The FCC is intended for interface management functions and is not a generic communications channel.

The FCC field is located in all frames, in overhead bytes 13 to 26. If unused, the management channel shall be filled with all-0s prior to scrambling. The FCC bytes provide a communication channel per FlexO-x-RS interface with an approximate bandwidth of 17.98 Mbit/s.
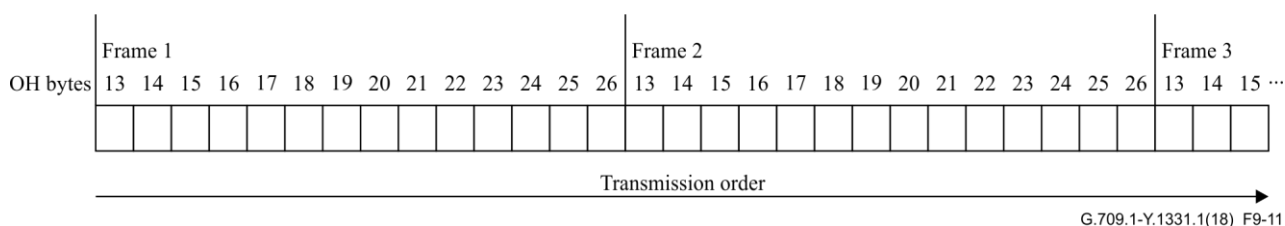

Figure 9-11 – FCC transmission order

9.2.9 FlexO reserved overhead (RES)

123.5 bytes of the FlexO overhead area in the FlexO multi-frame structure are reserved for future international standardization. These bytes/bits are located in frame 1/byte 5, frame 2/bytes 4, 5, 6, frames 3 to 8/bytes 3 to 6 and frames 1 to 8/bytes 29 to 40. These bytes/bits are set to all-0s prior to scrambling.

9.2.10 OTN synchronization message channel (OSMC)

A 128-bit (16 bytes) field per multi-frame is provided for an OTN synchronization message channel (OSMC). As shown in Figure 9-7, these are allocated across all eight frames of the multi-frame. This field provides a clear channel, to transport synchronization status message (SSM) and precise timing protocol (PTP) messages.

The OSMC is only defined on the first FlexO instance (lowest PID value) of a FlexO-x-RS-m interface group.

The OSMC field is located in all frames, in overhead bytes 27 and 28. If unused, the OTN synchronization message channel bytes shall be filled with all-0s prior to scrambling. The OSMC bytes are combined to provide a messaging channel, as illustrated in Figure 9-12, with an approximate bandwidth of 2.56 Mbit/s per 100G interface.
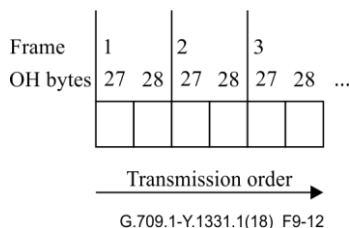

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Figure 9-12 – OSMC transmission order

The SSM and PTP messages within a FlexO instance are encapsulated into GFP-F frames as specified in [ITU-T G.7041]. PTP event messages are timestamped and after encapsulation into GFP-F frames, they are inserted into the OSMC as specified in this clause. GFP-F encapsulated SSM messages (and PTP non-event messages) are inserted into the OSMC at the earliest opportunity. GFP idle frames may be inserted between successive generic framing procedure (GFP) frames.

The mapping of GFP frames is performed by aligning the byte structure of every GFP frame with the byte of the OSMC overhead field. Since the GFP frames are of variable length and may be longer than 16 bytes, a GFP frame may cross the FlexO multi-frame boundary.

9.2.10.1 Generation of event message timestamp

The message timestamp point [ITU-T G.8260] for a PTP event message transported over the OSMC shall be the 32-frame multi-frame event (corresponding to MFAS[4:8] = 00000) preceding the beginning of the GFP frame, in which the PTP event message is carried. Since the GFP frames may be longer than 64 bytes, a frame may cross the FlexO 32-frame multi-frame boundary. Figure 9-13 shows a timestamp diagram example and the relationship to the GFP frames (PTP message).

All PTP event messages are timestamped on egress and ingress interfaces. The timestamp shall be the time at which the event message timestamp point passes the reference plane [ITU-T G.8260] marking the boundary between the PTP node (i.e., OTN node) and the network.

Event message timestamps are generated at the FlexO Access Point. The message timestamp point is specified below as the 32-frame FlexO multi-frame event corresponding to MFAS[4:8] = 00000. For this application, the FlexO multi-frame event is defined as when the first bit of the first alignment marker, corresponding to MFAS[4:8] = 00000 frame, on a lane crosses between the PTP node (i.e., OTN node) and the network (i.e., the analogous point to Ethernet MDI). In the case of a multi-lane PHY, the PTP path data delay is measured from the beginning of the alignment marker at the reference plane, which is equivalent to Ethernet MDI of the lane with the maximum media propagation delay. In practice:

– On egress interfaces, since the alignment markers for all lanes are transmitted at the same time conceptually, any alignment marker can be used for timestamping.

– On ingress interfaces, alignment markers are present in all the lanes, but different lanes may be skewed from each other. The last received alignment marker across all the lanes shall be used for timestamping.

NOTE 1 – The first byte of a GFP (PTP event message) frame is inserted into the FlexO OSMC between 4 and 31 frames after the 32-frame multi-frame boundary.

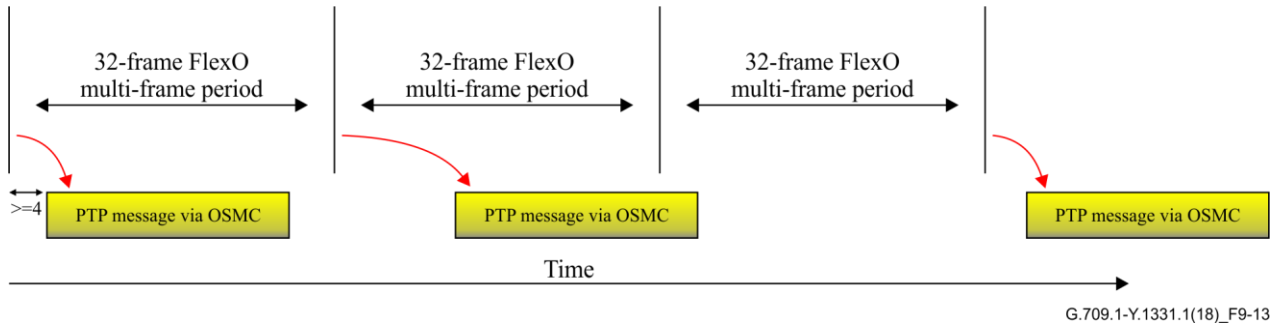NOTE 2 – The guard band of four frames is defined to simplify implementation.

Figure 9-13 – Timing diagram example for OSMC

NOTE 3 – This time synchronization over FlexO-x-RS interface implementation does not generate event message timestamps using a point other than the message timestamp point [ITU-T G.8260].

In this time synchronization over FlexO-x-RS interface implementation, the timestamps are generated at a point removed from the reference plane. Furthermore, the time offset from the reference plane is likely to be different for inbound and outbound event messages. To meet the requirement of this clause, the generated timestamps should be corrected for these offsets. Figure 19 in [b-IEEE 1588] illustrates these offsets. Based on this model, the appropriate corrections are as follows:

$$<egressTimestamp> = <egressMeasuredTimestamp> + egressLatency$$

$$<ingressTimestamp> = <ingressMeasuredTimestamp> - ingressLatency$$

where the actual timestamps <egressTimestamp> and <ingressTimestamp> measured at the reference plane are computed from the detected, i.e., measured, timestamps by their respective latencies. Failure to make these corrections results in a time offset between the slave and master clocks.

The PTP timestamp is associated with the first FlexO instance (lowest PID value) of a FlexO-x-RS-m interface group.

10 Mapping of OTUCn signal into n FlexO instances

In the most general case, the n OTUC instances of an OTUCn are mapped to a FlexO-x-RS-m group of m FlexO-x-RS interfaces, each with a FlexO-x-RS interface bandwidth of ceiling (n/m) *100G.

10.1 Distributing OTUCn and combining OTUC instances

An OTUCn frame structure is specified in clause 11.3 [ITU-T G.709] and contains n synchronous instances of OTUC frame structures. As shown in Figure 10-1, the FlexO source adaptation consists of splitting the OTUCn frame into n * OTUC instances. Similarly, the sink adaptation combines n * OTUC instances into an OTUCn. A single or multiple OTUC instances are then associated to a FlexO-x-RS interface, depending on the FlexO-x-RS interface rate. Alignment and deskewing are performed on the OTUC instances.
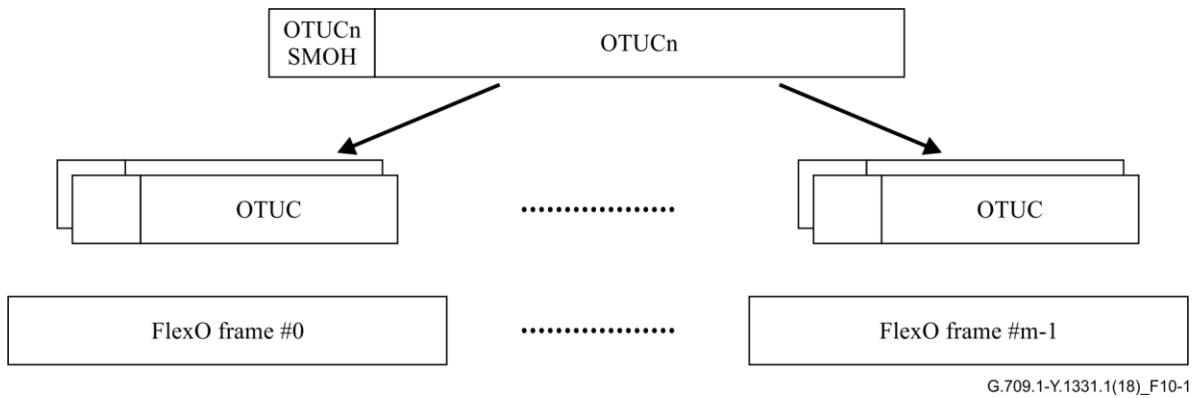
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Figure 10-1 – OTUCn distributed onto n * FlexO frame instances

10.2 FlexO frame payload

The FlexO frame payload area is divided in 128-bit blocks. The 128-bit blocks are aligned to the start of a FlexO payload area (following AM and OH). The FlexO frame payload consists of 5,120 blocks (frame #1-7 of the multi-frame, with fixed stuff payload) and 5,130 blocks (frame eight of the multi-frame, without fixed stuffing).

NOTE – This 128-bit (16-byte) word/block alignment of the 100G OTUC is analogous to the 66b block alignment of a 100G Ethernet PCS stream that is kept through the clause 91 [IEEE 802.3] adaptation process.

10.3 Mapping of OTUC into FlexO frame

Groups of 128 successive bits (16 bytes) of the OTUC signal are mapped into a 128-bit block of the FlexO frame payload area using a bit-synchronous mapping procedure (BMP) control mechanism as specified in clause 17 of [ITU-T G.709]. The 128-bit group of OTUC is aligned to the OTUC frame structure.

The OTUC frame structure is floating in respect to the FlexO frame.

The serial bit stream of an OTUC signal is inserted into the FlexO frame payload so that the bits will be transmitted on the FlexO-x-RS interface in the same order that they were received at the input of the mapper function.

In clause 8.3, the shown bit rate ratio between FlexO frame and payload is 256/241.

10.3.1 Mapping of OTUC into FlexO frame

There exists a one-to-one relationship between an OTUC and a 100G FlexO instance. The FlexO payload area is segmented in 128-bit blocks. The OTUC is mapped in contiguous 128-bit segments.

There are $(5,140*128*8 – 1,280*15) / (239*16*8*4) = 42.85$ OTUC frames per FlexO multi-frame. This results in ~5 OTUC frames per FlexO frame, or a new OTUC frame every ~24 FlexO frame rows, as shown in Figure 10-2.
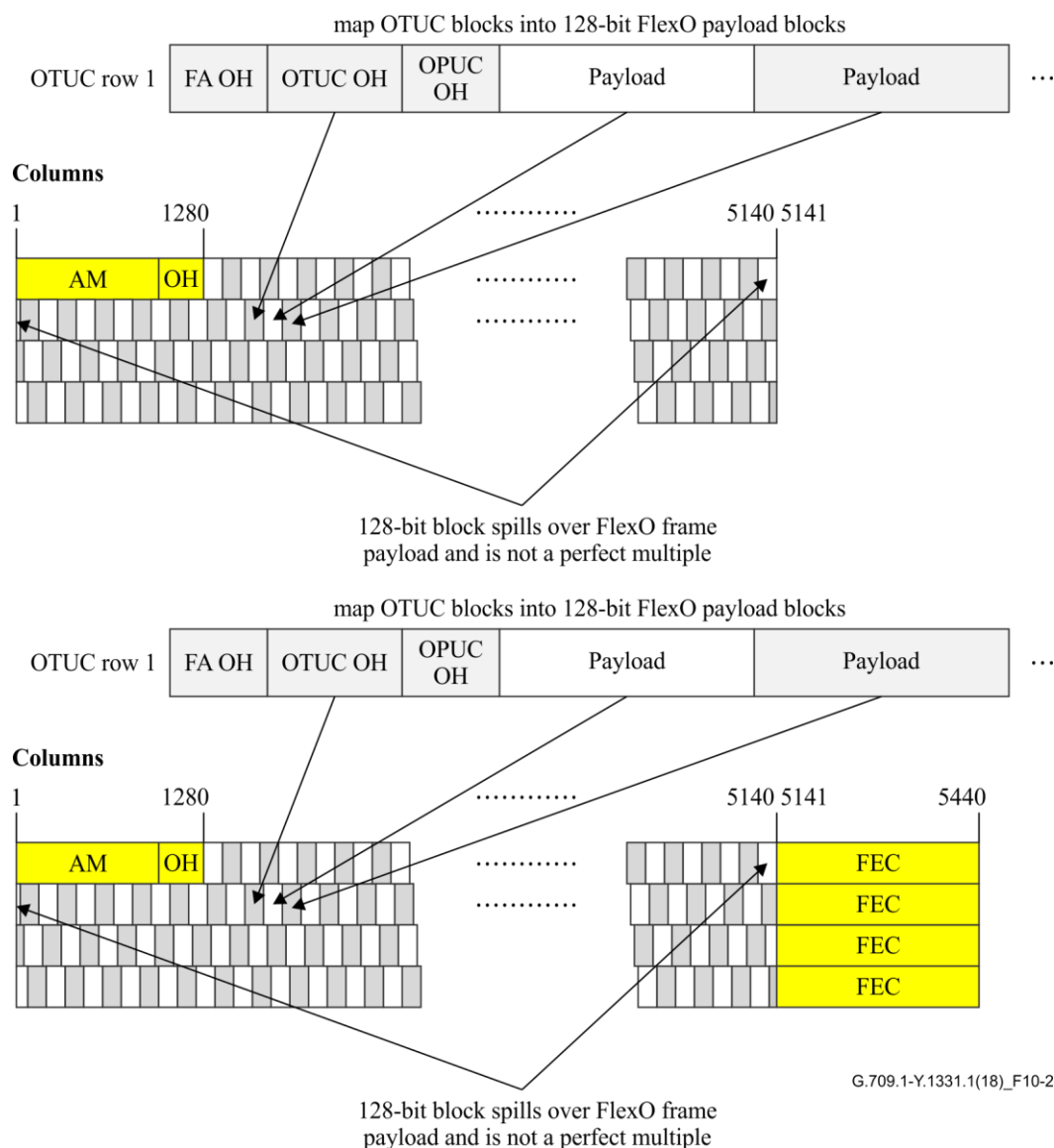
Figure 10-2 – OTUC mapped into 100G FlexO frame payload

The FlexO frame payload does not divide elegantly into 128-bit blocks in a single row. The block will spill over and cross row boundaries as shown in Figure 10-2A. The 128-bit alignment is always consistent across FlexO frames and the first 128-bit block starts immediately following the overhead area.

The AVAIL field indicates whether an OTUC is mapped into the FlexO frame payload (set to "1") or if the FlexO payload is empty (set to "0"). Other AVAIL values are not valid for 100G FlexO-x-RS interfaces.

10.4 FlexO-x-RS-m group alignment and deskewing

FlexO members are identified within a FlexO-x-RS-m group and reordered using GID, MAP and PID FlexO OH field. The PID sequence is used to recreate an OTUCn in proper OTUC instance order. For example OTUC#1 is mapped into a FlexO frame with the minimum PID number and so on.

Deskewing in the sink process is performed between OTUC frames within the group, using OTUC FAS as specified in [ITU-T G.709].

The OTUC frame skew requirements are intended to account for variations due to digital mapping and cable lengths. The skew tolerance requirement is 300 ns.

NOTE – These requirements are in line with [OIF FlexE] Low Skew applications.

11 100G FlexO-1-RS interface

11.1 Frame structure

The 100G FlexO-1-RS frame structure is shown in Figure 11-1 and consists of 128 rows by 5,440 1-bit columns. It contains a FlexO frame structure in columns 1 to 5140 and a FEC parity area in columns 5,141 to 5,440 in every row

Each row constitutes a 5,440-bit FEC codeword, with the last 300 bits used for the FEC parity bits. This results in a bit-oriented structure. The MSB in each FEC codeword is column 1, the LSB is column 5,440.

NOTE – The 100G FlexO-1-RS frame structure is derived from 100Gbit/s Ethernet clause 91 [IEEE 802.3] FEC alignment and lane architecture, without any 66b alignment or 256b/257b transcoding functions.

Figure 11-1 – 100G FlexO-1-RS frame structure

11.2 Bit rate and frame periods

The bit rate and tolerance of the 100G FlexO-1-RS signal is defined in Table 11-1.

Table 11-1 – 100G FlexO-1-RS types and bit rates

100G FlexO-1-RS nominal bit rate	Bit-rate tolerance
30592/27233 × 99 532 800 kbit/s	±20 ppm
NOTE 1 – The nominal 100G FlexO-1-RS bit rates are approximately: 111 809 474.446 kbit/s.	
NOTE 2 – The 100G FlexO-1-RS bit rate can be based on the OTUC bit rate as follows: 256/241 × OTUC bit rate = 256/241 × 239/226 × 99 532 800 kbit/s.	
NOTE 3 – The resulting 100G FlexO-1-RS bit rate is within a -4.46 ppm offset of the OTU4 nominal bit rate.	

The frame and multi-frame periods of the 100G FlexO-1-RS signal are defined in Table 11-2.

Table 11-2 – 100G FlexO-1-RS frame and multi-frame periods

Frame period (Note)	Multi-frame period (Note)
~6.228 µs	49.822 µs
NOTE – The period is an approximated value, rounded to 3 decimal places.	

11.3 Overhead

100G FlexO-1-RS specific overhead is not defined.

11.4 Scrambling

The 100G FlexO-1-RS frame payload, AM padding, fixed stuffing and overhead must be scrambled prior to transmission, in order to provide DC balance and proper running disparity on the interface. The am_i fields in the AMs are not scrambled and the chosen values have properties of already being DC balanced. The padding padi fields of the AMs as shown in Figure 9-3 are scrambled. Figure 11-3 below shows highlighted areas as scrambled.

The operation of the scrambler shall be functionally equivalent to that of a frame-synchronous additive scrambler with sequence length 65535 and the generating polynomial shall be $x^{16} + x^{12} + x^3 + x + 1$. See Figure 11-3 [ITU-T G.709] for an illustration of this scrambler.

The scrambler resets to 0xFFFF on the most significant (first transmitted) bit of the start of frame and the scrambler state advances during each bit of the FlexO-1-RS frame (see Figure 11-2). In the source function, the AM values (am_i fields) are inserted after scrambling and before the input to the FEC encoder. In other words, the FEC encoding is performed on unscrambled AM bits (am_i fields). The FEC encoder overwrites the FEC bit fields. The sink then receives unscrambled AM (am_i fields) and FEC fields, as illustrated in Figure 11-3.
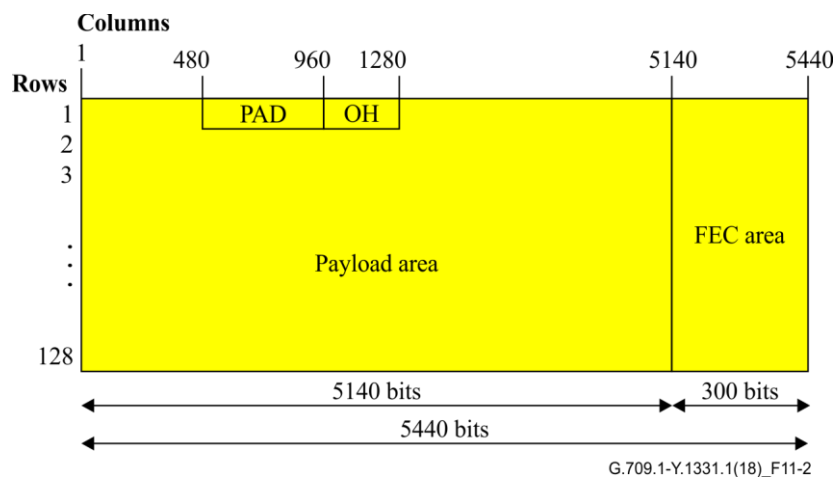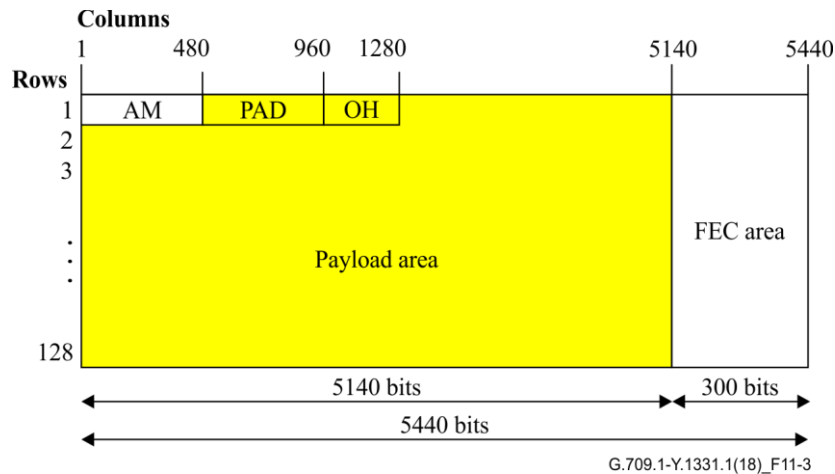

Figure 11-2 – 100G FlexO-1-RS scrambler

Figure 11-3 – 100G FlexO-1-RS scrambler after AM and FEC insertion

11.5 Forward error correction (FEC)

A 100G FlexO-1-RS FEC codeword occupies one row in the 100G FlexO-1-RS frame. The 100G FlexO-1-RS frame allocates 300 bits for FEC parity, per row, as shown in Figure 11-1.

The FEC scheme employs a Reed-Solomon code operating over the Galois Field GF(2^{10}), where the symbol size is 10 bits.

A Reed-Solomon code is denoted as RS(n,k) where k represents the number of message symbols to generate 2t parity symbols, which are appended to the message of total length n. The corresponding formula is n=k+2t, specifically

$$n=544$$
$$k=514$$
$$t=15$$

The FEC encoder processes 20 * 257-bit data blocks, resulting in the 5140 data bits in the FEC codeword (row) and generates 20 * 15 = 300 bits of FEC parity.

NOTE – The 100G FlexO-1-RS FEC is based on RS10 (544, 514), as specified in clause 91 of [IEEE 802.3] for 100GBASE-KP4 interfaces.

11.6 FOIC1.k-RS interface

11.6.1 FOIC1.4-RS interface

A FlexO frame is adapted over multi-channel parallel interfaces, using four ~28 Gbit/s physical lanes. No lane bit-multiplexing is performed.

The alignment markers for the FlexO frame are distributed on four FOIC1.4 lanes, resulting in 240-bit of data per lane. The alignment marker (AM) values are specified in clause 9.1. Each AM has unique UMx and UPx values. When the four AMs are distributed to lanes 0, 1, 2 and 3, the unique values are used for lane reordering in the sink function. The CMx values are replicated on all four lanes to facilitate the searching, alignment and deskewing process.

After FEC encoding, the data and parity bits are distributed to all four logical FOIC1.4 lanes, in groups of 10-bits, in a round robin distribution scheme from the lowest to the highest numbered lanes. The resulting per-lane transmitted values of the AM fields are illustrated in Table 11-3 where the transmission order is from left to right. In other words, for example, AM0 is transmitted in Lane 0, AM1 is transmitted in Lane 1, etc., and the bits of each 10-bit word are transmitted MSB first.

NOTE 1 – The inverse multiplexing function is based on clause 91 [IEEE 802.3].

NOTE 2 – The mechanism is compatible and can reuse optical modules being developed for IEEE 100GBASE-R4, with OTU4 rate support.

NOTE 3 – The electrical specifications for an FOIC1.4-RS 25G lane is found in [b-OIF CEI].

Table 11-3 – AM bit distribution over the four FOIC1.4-RS lanes

AM bits	Lane 0 10-bit symbol of AM0	Lane 1 10-bit symbol of AM1	Lane 2 10-bit symbol of AM2	Lane 3 10-bit symbol of AM3
1 – 40	0101100101	0101100101	0101100101	0101100101
41 – 80	0100100110	0100100110	0100100110	0100100110
81 – 120	0100011011	0100001000	0100011000	0100010110
121 – 160	0110100110	0010100110	1010100110	1010100110
161 – 200	1010110110	1010110110	1010110110	1010110110
201 – 240	0110111001	0110111110	0110110111	0110110010
241 – 280	1011100000	0110010110	1111011111	0001011000
281 – 320	0010001110	1001111011	0011001111	0100000001
321 – 360	1100111101	0111111000	0110101010	0000101111
361 – 400	1001000111	0110011010	0000001000	0111101001
401 – 440	1111011100	0101100001	0011001100	1110111111
441 – 480	0100110000	0010000001	0010010101	1011110100

NOTE – Transmission order of each 10-bit word is left-to-right (MSB first). The transmission order within the FlexO frame is left-to-right across the row and down the table. The transmission order for each lane is per-word and down the table.

11.6.2 FOIC1.4-RS skew tolerance requirements

The lane skew tolerance requirement is 180 ns.

NOTE – These requirements are in line with CAUI4 [IEEE 802.3].

11.6.3 FOIC1.4-RS 28G lane bit rate

The FOIC1.4-RS lane is synchronous to the FlexO-1-RS frame. There are four lanes.

The bit rate and tolerance of the FOIC1.4-RS lane signal is defined in Table 11-4.

Table 11-4 – FOIC1.4-RS lane rate

FOIC1.4-RS nominal lane bit rate	Bit-rate tolerance
30592/27233 × 24 883 200 kbit/s	±20 ppm

NOTE 1 – The nominal lane rate is approximately: 27 952 368.611 kbit/s
NOTE 2 – FOIC1.4-RS_lane_rate = 100G_FlexO-1-RS_rate/4

NOTE – The 100G FlexO-1-RS rate is specified in clause 11.2.

This results in a FOIC1.4-RS lane bit rate with a -4.46 ppm offset from the OTL4.4 nominal bit rate.

11.6.4 m*FOIC1.4-RS interface

The m*FOIC1.4-RS interface supports multiple optical tributary signals on each of the m single optical spans with 3R regeneration at each end.

An m*FOIC1.4-RS interface signal contains one OTUCn signal distributed across the m optical interfaces and the k=4 lanes per optical interface.

Specifications of the optical tributary signal carrying each FOIC1.4-RS lane are contained in [ITU-T G.695] and [ITU-T G.959.1].

12   200G FlexO-2-RS interface

12.1   Frame structure

The 200G FlexO-2-RS frame structure is shown in Figure 12-1 and consists of two instances (A, B) of 128 rows by 5,440 1-bit columns. Each instance contains a 100G FlexO frame structure in columns 1 to 5140 and a FEC area in columns 5,141 to 5,440 in every row as illustrated in Figure 12-3. Instances #A and #B are 10-bit interleaved into the 200G FlexO-2-RS frame.

Each row constitutes a 5,440-bit FEC codeword, with the last 300 bits used for the FEC parity bits. This results in a bit-oriented structure. The MSB in each FEC codeword is bit 1, the LSB is bit 5,440.

NOTE – The 200G FlexO-2-RS frame structure is derived from 200 Gbit/s Ethernet clause 119 [IEEE 802.3bs] FEC alignment and lane architecture, without any 66b alignment or 256b/257b transcoding functions.
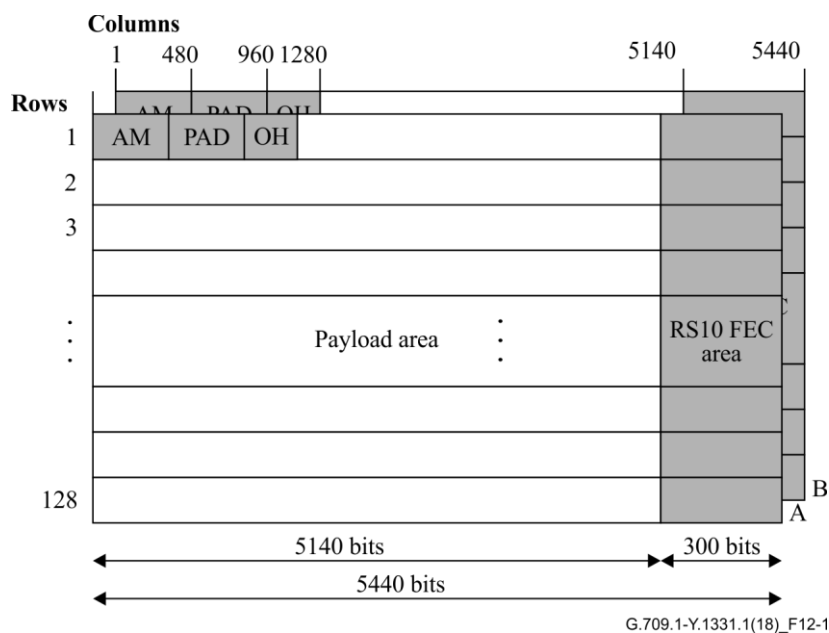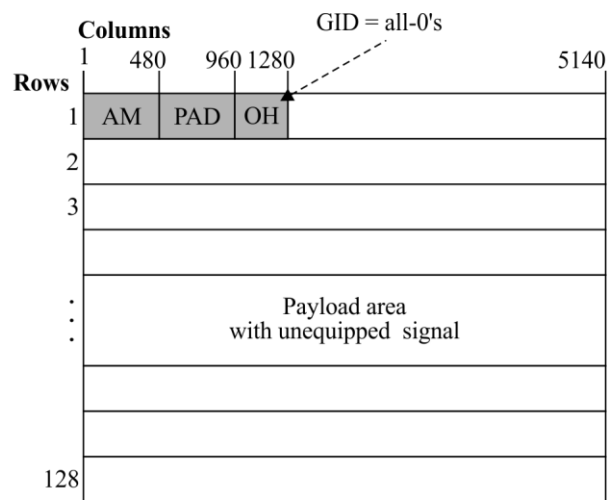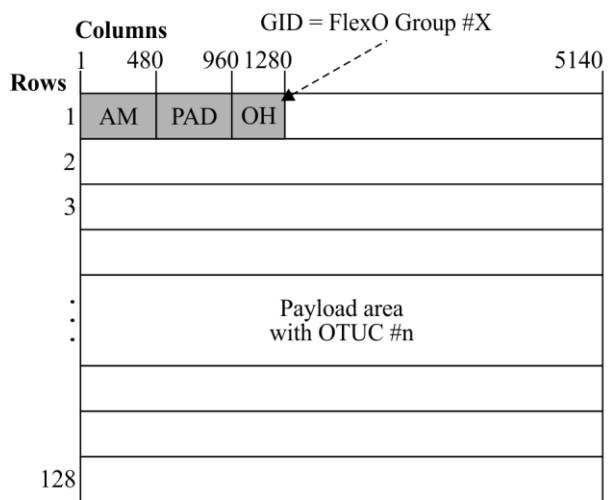

Figure 12-1 – 200G FlexO-2-RS frame structure

Partial fill

For the case that a m×200G FlexO-2-RS group carries an OTUCn with n < 2m, some 200G FlexO-2-RS signals may contain only one OTUC instance, see Figure 12-2. When a FlexO-2-RS contains fewer than 2 OTUC instances, the equipped OTUC instance is located in the first 100G FlexO frame within this 200G FlexO-2-RS #m frame. The second 100G FlexO frame is not carrying an OTUC instance and has its GID field set to all-0s to indicate that it is unequipped.

The following rules govern unequipped instances:

−   Unequipped OTUC instances must always be the highest numbered instance(s) in a FlexO-2-RS frame.

−   There must always be at least one equipped instance in every FlexO-2-RS frame.

Figure 12-2 − 100G FlexO frames within 200G FlexO-2-RS #m signal for case of partial fill
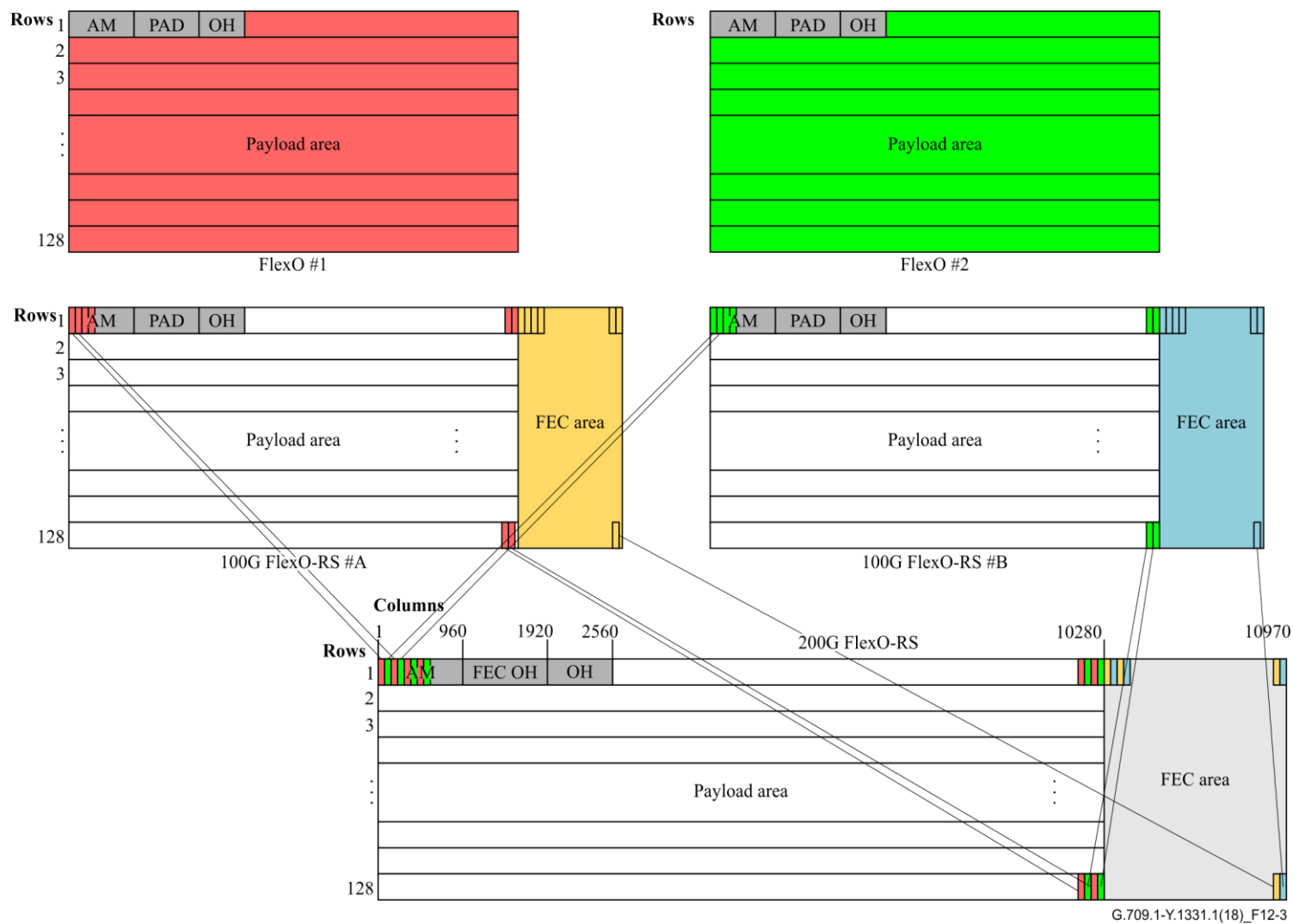
Figure 12-3 – Mapping FlexO instances into the 200G Flex-2-RS frame structure

12.2 Bit rate and frame period

The bit rate and tolerance of the 200G FlexO-2-RS signal is defined in Table 12-1.

Table 12-1 – 200G FlexO-2-RS types and bit rates

200G FlexO-2-RS nominal bit rate	Bit-rate tolerance
$2 \times 30592/27233 \times 99\ 532\ 800$ kbit/s	± 20 ppm
NOTE 1 – The nominal 200G FlexO-2-RS bit rate is approximately: 223 618 948.893 kbit/s. NOTE 2 – The 200G FlexO-2-RS bit rate can be based on the OTUC bit rate as follows: $2 \times 256/241 \times$ OTUC bit rate $= 2 \times 256/241 \times 239/226 \times 99\ 532\ 800$ kbit/s.	

The frame and multi-frame periods of the 200G FlexO-2-RS signal are defined in Table 12-2.

Table 12-2 – 200G FlexO-2-RS frame and multi-frame periods

Frame period (Note)	Multi-frame period (Note)
~6.228 µs	49.822 µs
NOTE – The period is an approximated value, rounded to 3 decimal places.	

12.3 Overhead

200G FlexO-2-RS specific overhead is not defined.

12.4 Scrambling

The operation of the 200G FlexO-2-RS scrambler is based on the interleaved 200G FlexO-2-RS frame structure shown in Figure 12-3 which is generated by 10-bit interleaving of the two instances of 128 rows by 5,440 1-bit columns of the 200G FlexO-2-RS frame structure.

The interleaved 200G FlexO-2-RS frame payload, AM padding, fixed stuffing and overhead must be scrambled prior to transmission, in order to provide DC balance and proper running disparity on the interface. The am_i fields in the AMs are not scrambled and the chosen values have properties of already being DC balanced. The padding fields are scrambled. Figure 12-5 below shows highlighted areas as scrambled.

The operation of the scrambler shall be functionally equivalent to that of a frame-synchronous additive scrambler of sequence length 65535 and the generating polynomial shall be $x^{16} + x^{12} + x^3 + x + 1$. See Figure 11-3 [ITU-T G.709] for an illustration of this scrambler.

The scrambler resets to 0xFFFF on the most significant bit of the start of frame and the scrambler state advances during each bit of the interleaved 200G FlexO-2-RS frame, see Figure 12-4. In the source function, the AM values (am_i fields) are inserted after scrambling and before the input to the FEC encoder. In other words, the FEC encoding is performed on unscrambled AM bits (am_i fields). The FEC encoder overwrites the FEC bit fields. The sink then receives unscrambled AM (am_i fields) and FEC fields, as illustrated in Figure 12-5.
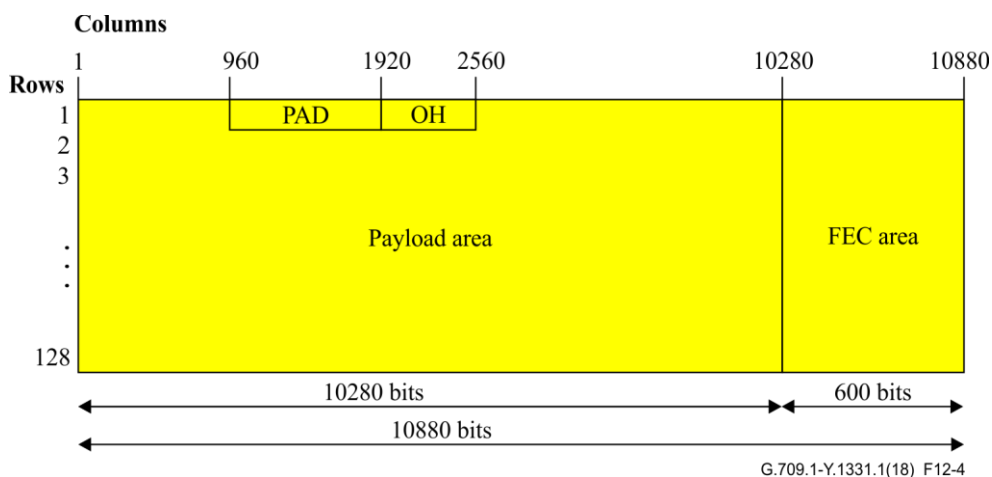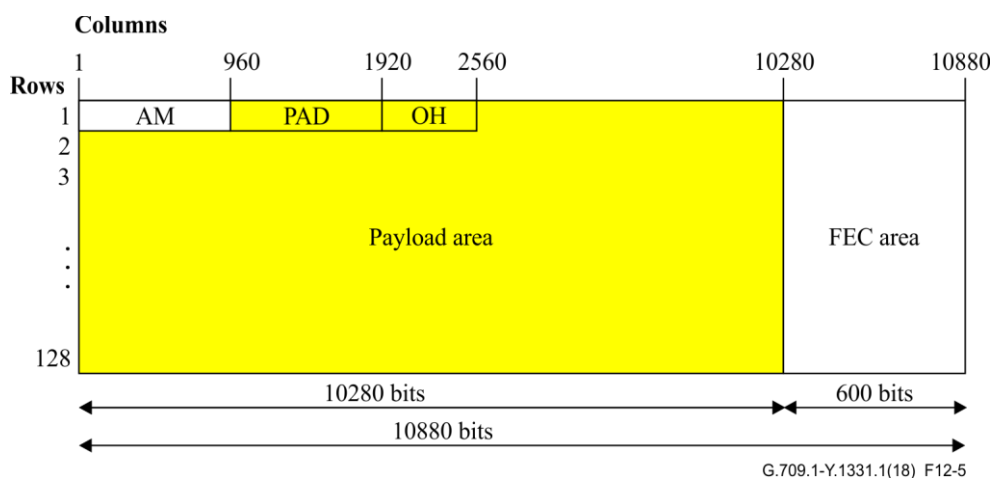
Figure 12-4 – 200G FlexO-2-RS scrambler

Figure 12-5 – 200G FlexO-2-RS scrambler after AM and FEC insertion

12.5 Forward error correction (FEC)

The 200G FlexO-2-RS deploys two 100G FlexO-2-RS instances, each with its own 100G FlexO-2-RS FEC codewords that occupy a row in the 100G FlexO-2-RS frame, as illustrated in Figure 12-1.

Refer to clause 11.4 for the specification of the 100G FlexO-2-RS FEC.

NOTE – The 200G FlexO-2-RS FEC is based on RS10 (544, 514), as specified in clause 119 of [IEEE 802.3bs] for 200GBASE-R interfaces.

12.6 FOIC2.k-RS interface

12.6.1 FOIC2.4-RS interface

A FOIC2.4-RS interface is used as a system interface with 200G optical modules. The FlexO-2-RS frame structure is adapted over multi-channel parallel interfaces, using four ~56 Gbit/s physical lanes.

The alignment markers for the FlexO frame are distributed on eight logical FOIC2.4 lanes, resulting in 120-bit of data per logical lane. The alignment marker (AM) values are specified in clause 9.1.3. Each AM has unique UMx and UPx values. When the eight AMs are distributed to lanes 0, 1, 2 to 7, the differing values are used for lane reordering in the sink function. The CMx values are replicated on all eight lanes to facilitate the searching, alignment and deskewing process.

After FEC encoding two FlexO frames, two FEC codewords separately from two 100G FlexO-1-RS FEC are interleaved on a 10-bit basis and then distributed to 8 logical lanes in a round robin distribution scheme from the lowest to the highest numbered lanes. The specific scheme of interleaving and distribution is specified in clause 119 of [IEEE 802.3bs] for 200GBASE-R interface. The resulting per-lane transmitted values of the AM fields are illustrated in Table 12-3 where the transmission order is from left to right. For example, AM0 is transmitted in Lane 0, AM1 is transmitted in Lane 1, etc., and the bits of each 10-bit word are transmitted MSB first.

The 4 physical lanes of a FOIC2.4-RS interface are generated by bit multiplexing two specific logical lanes onto a physical lane.

NOTE 1 – The inverse multiplexing function is based on clause 91 [IEEE 802.3].

NOTE 2 – The mechanism is compatible and can reuse optical modules being developed for IEEE 200GBASE-R4, with 200G OTN rate support.

Table 12-3 – AM bit distribution over the eight logical lanes

AM bits	Lane 0 10-bit symbol of AM0	Lane 1 10-bit symbol of AM1	Lane 2 10-bit symbol of AM2	Lane 3 10-bit symbol of AM3	Lane 4 10-bit symbol of AM4	Lane 5 10-bit symbol of AM5	Lane 6 10-bit symbol of AM6	Lane 7 10-bit symbol of AM7
1-80	0101100101	0101100101	0101100101	0101100101	0101100101	0101100101	0101100101	0101100101
81-160	0100100110	0100100110	0100100110	0100100110	0100100110	0100100110	0100100110	0100100110
161-240	0100101000	0100001000	0100011000	0100010110	0100100001	0100010011	0100101111	0100010001
241-320	0010100110	0010100110	1010100110	1010100110	1110100110	1110100110	0010100110	0010100110
321-400	1010110110	1010110110	1010110110	1010110110	1010110110	1010110110	1010110110	1010110110
401-480	0110110110	0110111110	0110110111	0110110010	0110111001	0110110111	0110110111	0110110100
481-560	1011110011	0110010110	1111011111	0001011000	1000010101	0010010010	0111010000	1100011010
561-640	0100000011	1001111011	0011001111	0100000001	0010001010	0011110010	1000111001	1101101110
641-720	0011000110	0111111000	0110101010	0000101111	0100111101	1000101110	1000010110	1101101010
721-800	0101000011	0110011010	0000001000	0111101001	1001111010	0011011011	0010001011	1100111001
801-880	0010111111	0101100001	0011001100	1110111111	1011011101	0111000011	1101110001	0100100100
881-960	0011001110	0010000001	0010010101	1011110100	0110110000	0101110100	1001111010	0100100101

NOTE – Transmission order of each 10-bit word is left-to-right (MSB first). The transmission order within the FlexO frame is left-to-right across the row and down the table. The transmission order for each lane is per-word and down the table.

12.6.2   FOIC2.4-RS skew tolerance requirements

The lane skew tolerance requirement is 180 ns.

NOTE – These requirements are in line with 200GAUI-4 [IEEE 802.3bs].

12.6.3   FOIC2.4-RS 56G lane bit rate

The FOIC2.4-RS lane is synchronous to the FlexO-2-RS frame. There are four lanes.

The bit rate and tolerance of the FOIC2.4-RS lane signal is defined in Table 12-4.

Table 12-4 – FOIC2.4-RS lane rate

FOIC2.4-RS nominal lane bit rate	Bit-rate tolerance
$30592/27233 \times 49\,766\,400$ kbit/s	± 20 ppm

NOTE 1 – The nominal FOIC2.4-RS lane rate is approximately: 55 904 737.223 kbit/s
NOTE 2 – FOIC2.4-RS_lane_rate = 200G_FlexO-2-RS_rate/4

NOTE – The 200G FlexO-2-RS bit rate is specified in clause 12.2.

12.6.4   m*FOIC2.4-RS interface

The m*FOIC2.4-RS interface supports multiple optical tributary signals on each of the m single optical spans with 3R regeneration at each end.

An m*FOIC2.4-RS interface signal contains one OTUCn signal distributed across the m optical interfaces and the k=4 lanes per optical interface.

Specifications of the optical tributary signal carrying each FOIC2.4-RS lane are contained in [ITU-T G.695] and [ITU-T G.959.1].

12.6.5   FOIC2.4-RS interface processes

Figure 12-6 shows the processes of 200G FlexO-2-RS. It can be seen that it is divided into three parts (the part of reusing 100G FlexO, the part of purely new design and the part of reusing IEEE802.3 200GE PCS/FEC).

The processes of scrambler/descrambler and AM insertion/removal are the only new designs. Before scrambler in the source and after descrambler in the sink, they keep completely the same processes as 100G FlexO's.

In the part of reusing IEEE802.3 200GE PCS lower-part and FEC, it completely reuses all processes related to IEEE802.3 200GE PCS lower-part and FEC. 200G FlexO uses 2*100G KP4-FEC.
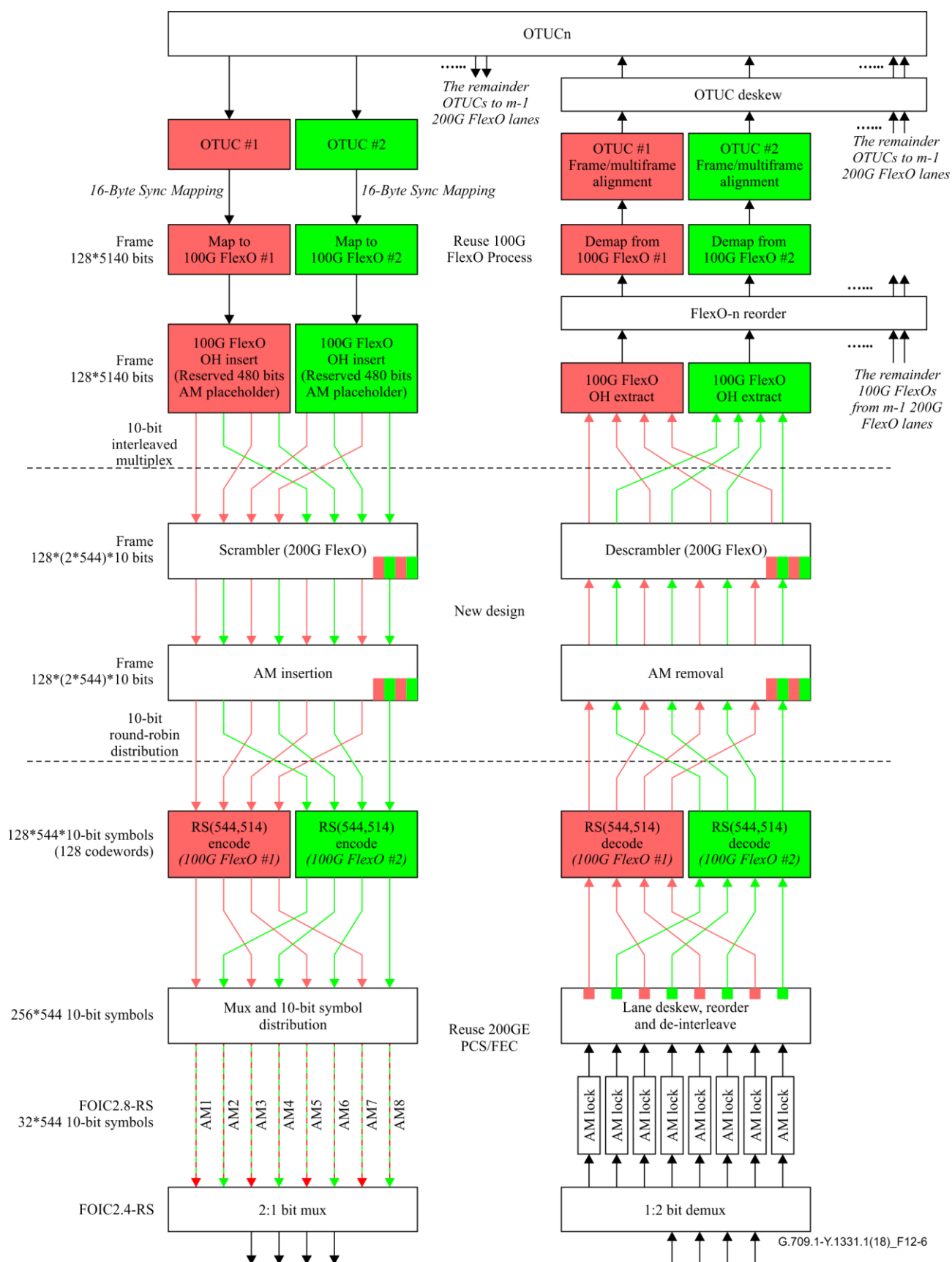
Figure 12-6 – 200G FlexO-2-RS processes

13   400G FlexO-4-RS interface

13.1   Frame structure

The 400G FlexO-4-RS frame structure is shown in Figure 13-1 and consists of four instances (A, B, C, D) of 128 rows by 5440 1-bit columns. Each frame contains four interleaved FlexO frame structure instances in columns 1 to 5140 and a FEC area in columns 5,141 to 5,440 in every row as illustrated in Figure 13-3. 100G FlexO instances #A and #C are interleaved into a 200G intermediate structure #E and 100G FlexO instances #B and #D are interleaved into a 200G intermediate structure #F. 200G intermediate structures #E and #F are 10-bit interleaved into the 400G FlexO-4-RS frame.

Each row of a 200G structure constitutes a 5,440-bit FEC codeword, with the last 300 bits used for the FEC parity bits. This results in a bit-oriented structure. The MSB in each FEC codeword is bit 1, the LSB is bit 5,440.

NOTE – The 400G FlexO-4-RS frame structure is derived from 400 Gbit/s Ethernet clause 119 [IEEE 802.3bs] FEC alignment and lane architecture, without any 66b alignment or 256b/257b transcoding functions.
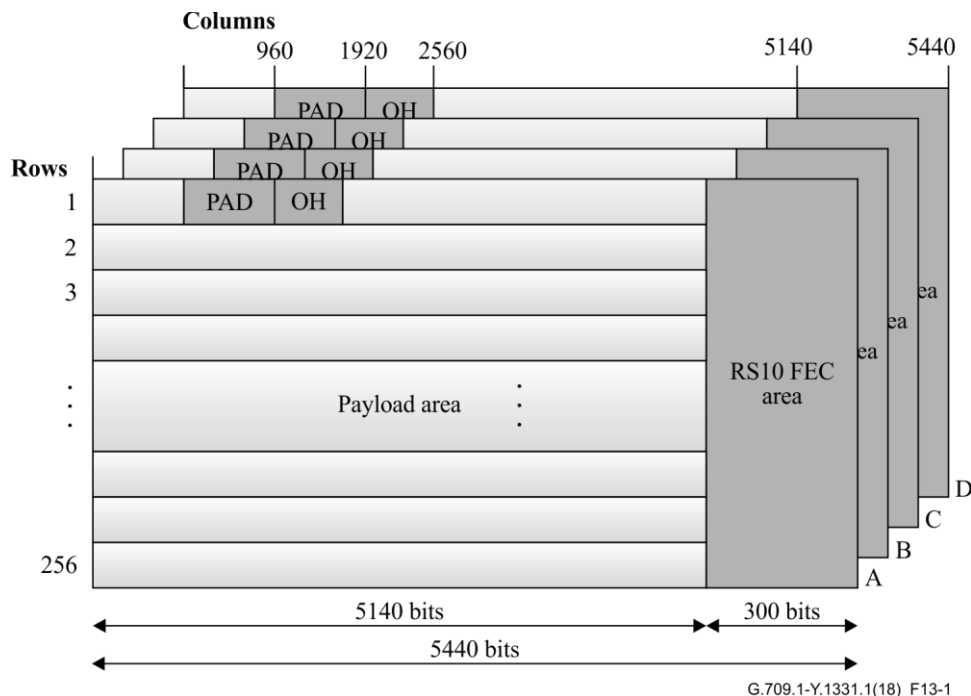

Figure 13-1 − 400G Flex-4-RS frame structure

Partial fill

For the case that a m×400G FlexO-4-RS group carries an OTUCn with n < 4m, some 400G FlexO-4-RS signals may contain only three, two or one OTUC instance(s), see Figure 13-2. When a FlexO-4-RS frame contains fewer than 4 OTUC instances, these three, two or one OTUC instance(s) is(are) located in the first one, two or three 100G FlexO frame(s) within this 400G FlexO-4-RS #m frame. The last one, two or three 100G FlexO frames are not carrying an OTUC instance and have their GID field set to all-0s to indicate that the 100G FlexO frame is unequipped.

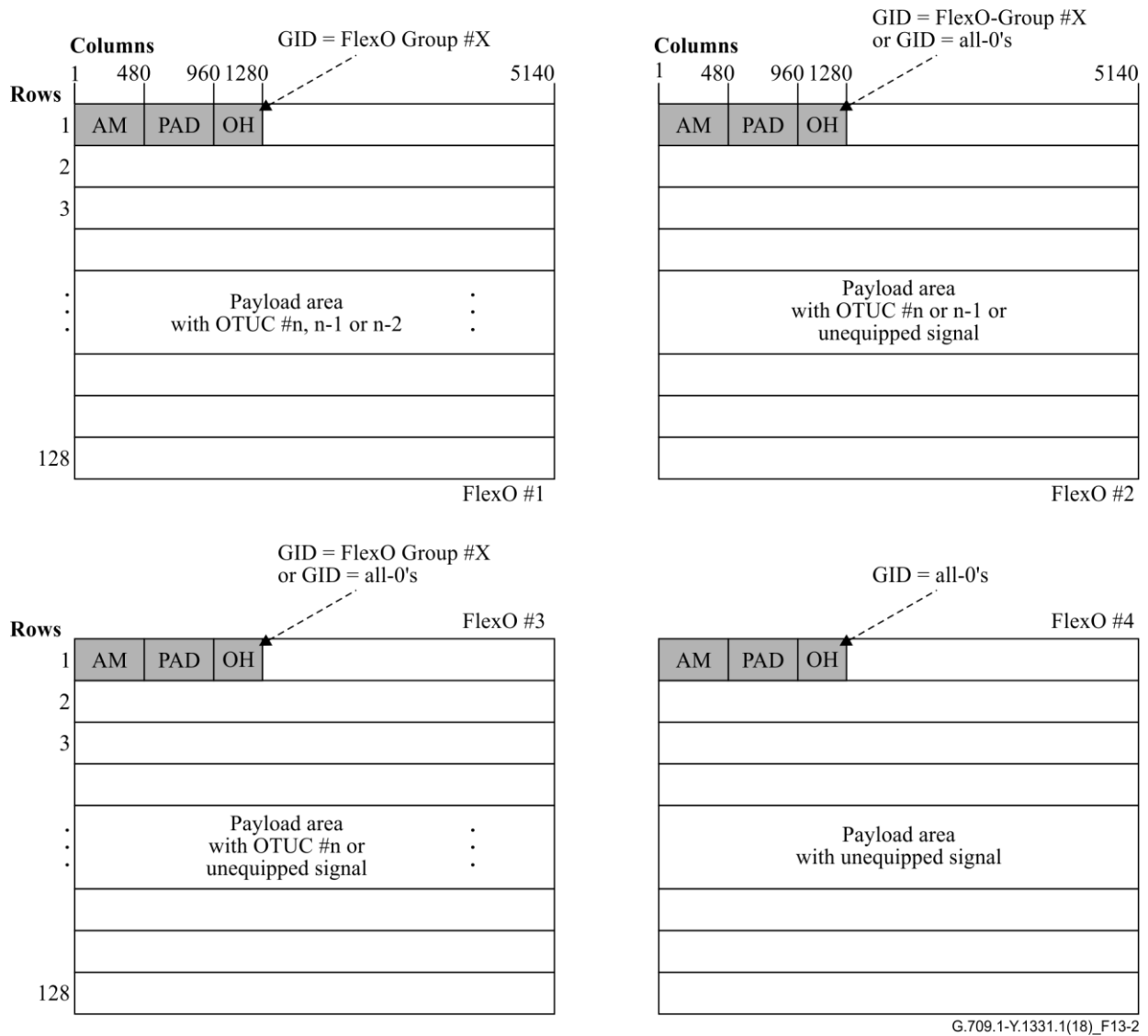The same rules in clause 12.1 governing unequipped instances apply.

Figure 13-2 – 100G FlexO frames within 400G FlexO-4-RS #m signal for case of partial fill
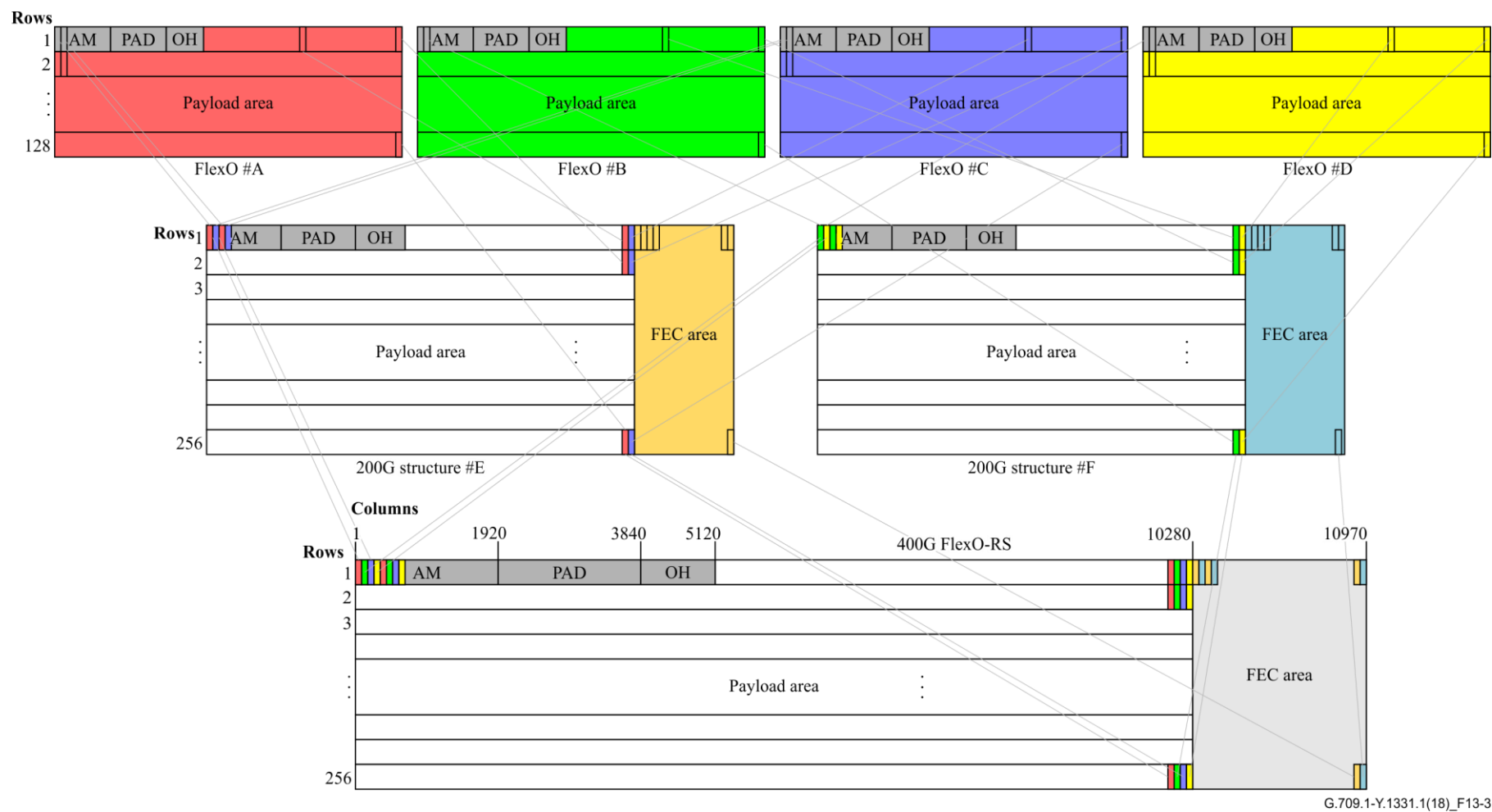
Figure 13-3 − Mapping FlexO instances into the 400G Flex-4-RS frame structure

13.2 Bit rate and frame periods

The bit rate and tolerance of the 400G FlexO-4-RS signal is defined in Table 13-1.

Table 13-1 – 400G FlexO-4-RS types and bit rates

400G FlexO-4-RS nominal bit rate	Bit-rate tolerance
$4 \times 30592/27233 \times 99\,532\,800$ kbit/s	± 20 ppm
NOTE 1 – The nominal 400G FlexO-4-RS bit rate is approximately: 447 237 897.786 kbit/s. NOTE 2 – The 400G FlexO-4-RS bit rate can be based on the OTUC bit rate as follows: $4 \times 256/241 \times$ OTUC bit rate = $4 \times 256/241 \times 239/226 \times 99\,532\,800$ kbit/s.	

The frame and multi-frame periods of the 400G FlexO-4-RS signal are defined in Table 13-2.

Table 13-2 – 400G FlexO-4-RS frame and multi-frame periods

Frame period (Note)	Multi-frame period (Note)
~6.228 µs	49.822 µs
NOTE – The period is an approximated value, rounded to 3 decimal places.	

13.3 Overhead

400G FlexO-4-RS specific overhead is not defined.

13.4 Scrambling

The operation of the 400G FlexO-4-RS scrambler is based on the interleaved 400G FlexO-4-RS frame structure shown in Figure 13-3 which is generated by 10-bit multiplexing of the two instances of 256 rows by 5,440 1-bit columns of the 400G FlexO-4-RS frame structure.

The interleaved 400G FlexO-4-RS frame payload, AM padding, fixed stuffing and overhead must be scrambled prior to transmission, in order to provide DC balance and proper running disparity on the interface. The am_i fields in the AMs are not scrambled and the chosen values have properties of already being DC balanced. The padding fields are scrambled. Figure 13-5 below shows highlighted areas as scrambled.

The operation of the scrambler shall be functionally equivalent to that of a frame-synchronous scrambler of sequence 65535 and the generating polynomial shall be $x^{16} + x^{12} + x^3 + x + 1$. See Figure 11-3 [ITU-T G.709] for an illustration of this scrambler.

The scrambler resets to 0xFFFF on the most significant bit of the start of frame and the scrambler state advances during each bit of the interleaved 400G FlexO-4-RS frame, see Figure 13-4. In the source function, the AM values (am_i fields) are inserted after scrambling and before the input to the FEC encoder. In other words, the FEC encoding is performed on unscrambled AM bits (am_i fields). The FEC encoder overwrites the FEC bit fields. The sink then receives unscrambled AM (am_i fields) and FEC fields, as illustrated in Figure 13-5.
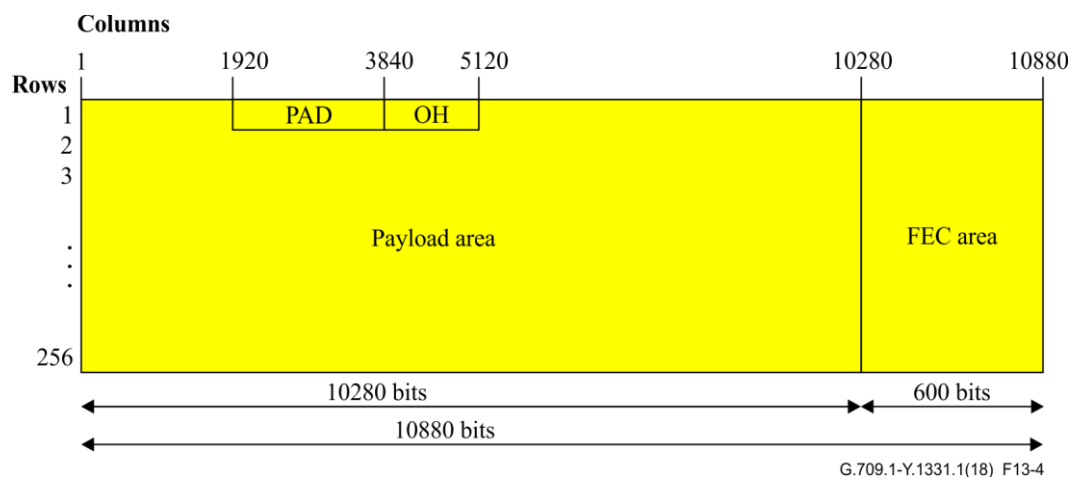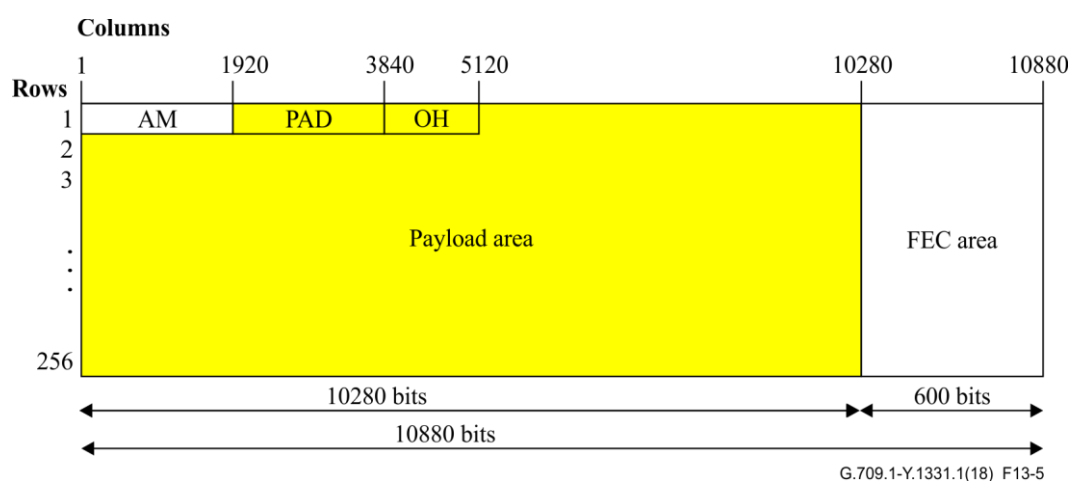
Figure 13-4 – 400G FlexO-4-RS scrambler

Figure 13-5 – 400G FlexO-4-RS scrambler after AM and FEC insertion

13.5 Forward error correction (FEC)

The 400G FlexO-4-RS consists of two 200G intermediate structures, each with its own FEC codewords that occupy a row in the 200G intermediate structure, as illustrated in Figure 13-1.

Refer to clause 11.4 for the specification of the 100G FlexO-1-RS FEC.

NOTE – The 400G FlexO-4-RS FEC is based on RS10 (544, 514), as specified in clause 119 of [IEEE 802.3bs] for 400GBASE-R interfaces.

13.6 FOIC4.k-RS interface

13.6.1 FOIC4.8-RS interface

A FOIC4.8-RS interface is used as a system interface with 400G optical modules. The FlexO-4-RS frame structure is adapted over multi-channel parallel interfaces, using eight ~56 Gbit/s physical lanes.

The alignment markers for the 400G FlexO frame are distributed on sixteen lanes, resulting in 120-bit of data per lane. The alignment marker (AM) values are specified in clause 9.1.5. Each AM has unique UMx and UPx values. When the sixteen AMs distributed to lanes 0, 1, 2 to 15, the differing values are used for lane reordering in the sink function. The CMx values are replicated on all sixteen lanes to facilitate the searching, alignment and deskewing process.

After FEC encoding, two FEC codewords separately from two 200G FlexO-4-RS FEC are interleaved on a 10-bit basis and then is distributed to 16 logical lanes in a round robin distribution

scheme from the lowest to the highest numbered lanes. The specific scheme of interleaving and distribution is specified in clause 119 of [IEEE 802.3bs] for 400GBASE-R interface. The resulting per-lane transmitted values of the AM fields are illustrated in Table 13-3 where the transmission order is from left to right. For example, AM0 is transmitted in Lane 0, AM1 is transmitted in Lane 1, etc., and the bits of each 10-bit word are transmitted MSB first.

The 8 lanes of a FOIC4.8-RS interface are generated by bit multiplexing of each two logical lanes, e.g., bit multiplexing of lane 0 and lane 1, lane 2 and lane 3, lane 4 and lane 5, lane 6 and lane 7, lane 8 and lane 9, lane 10 and lane 11, lane 12 and lane 13, lane 14 and lane 15.

NOTE 1 – The inverse multiplexing function is based on clause 91 [IEEE 802.3].

NOTE 2 – The mechanism is compatible and can reuse optical modules being developed for IEEE 400GBASE-R4, with 400G OTN rate support.

Table 13-3 – AM bit distribution over the sixteen logical lanes

AM bits	Lane 0 10-bit symbol of AM0	Lane 1 10-bit symbol of AM1	Lane 2 10-bit symbol of AM2	Lane 3 10-bit symbol of AM3	Lane 4 10-bit symbol of AM4	Lane 5 10-bit symbol of AM5	Lane 6 10-bit symbol of AM6	Lane 7 10-bit symbol of AM7
1-80	0101100101	0101100101	0101100101	0101100101	0101100101	0101100101	0101100101	0101100101
161-240	0100100110	0100100110	0100100110	0100100110	0100100110	0100100110	0100100110	0100100110
321-400	0100011011	0100001000	0100011000	0100010110	0100100001	0100010011	0100101111	0100010001
481-560	0110100110	0010100110	1010100110	1010100110	1110100110	1110100110	0010100110	0010100110
641-720	1010110110	1010110110	1010110110	1010110110	1010110110	1010110110	1010110110	1010110110
801-880	0110111001	0110111110	0110110111	0110110010	0110111001	0110110111	0110110111	0110110100
961-1040	1011100000	0110010110	1111011111	0001011000	1000010101	0010010010	0111010000	1100011010
1121-1200	0010001110	1001111011	0011001111	0100000001	0010001010	0011110010	1000111001	1101101110
1281-1360	1100111101	0111111000	0110101010	0000101111	0100111101	1000101110	1000010110	1101101010
1441-1520	1001000111	0110011010	0000001000	0111101001	1001111010	0011011011	0010001011	1100111001
1601-1680	1111011100	0101100001	0011001100	1110111111	1011011101	0111000011	1101110001	0100100100
1761-1840	0100110000	0010000001	0010010101	1011110100	0110110000	0101110100	1001111010	0100100101

AM bits	Lane 8 10-bit symbol of AM8	Lane 9 10-bit symbol of AM9	Lane 10 10-bit symbol of AM10	Lane 11 10-bit symbol of AM11	Lane 12 10-bit symbol of AM12	Lane 13 10-bit symbol of AM13	Lane 14 10-bit symbol of AM14	Lane 15 10-bit symbol of AM15
81-160	0101100101	0101100101	0101100101	0101100101	0101100101	0101100101	0101100101	0101100101
241-320	0100100110	0100100110	0100100110	0100100110	0100100110	0100100110	0100100110	0100100110
401-480	0100000001	0100110101	0100010111	0100001101	0100000110	0100001010	0100000010	0100001011
561-640	1010100110	1010100110	1110100110	1010100110	0010100110	0010100110	1110100110	0110100110
721-800	1010110110	1010110110	1010110110	1010110110	1010110110	1010110110	1010110110	1010110110
881-960	0110111111	0110110100	0110110010	0110111000	0110111101	0110110011	0110111000	0110110110
1041-1120	1001100001	0101100011	0000101010	1110010001	1010010001	0011100011	1101010100	1010011001
1201-1280	1111001110	1000100011	0111010111	0001100110	0101101111	0011101001	1111011111	0101011101
1361-1440	1010111000	0011110010	0001101111	0001110001	1010100100	1100001111	0110010101	1001111010
1521-1600	0001100111	1110100111	0111110101	1100011011	1001011011	0011000111	1100101010	0101011001
1681-1760	1000001100	0001110111	0110001010	1011100110	1010100100	0011000101	1100001000	1010101000
1841-1920	0101010001	0011000011	0011100100	0111100011	0001010110	1000111100	0010011010	1001100001

NOTE – Transmission order of each 10-bit word is left-to-right (MSB first). The transmission order within the FlexO frame is left-to-right across the row and down the table. The transmission order for each lane is per-word and down the table.

13.6.2 FOIC4.8-RS skew tolerance requirements

The lane skew tolerance requirement is 180 ns.

NOTE – These requirements are in line with 400GAUI-4 [IEEE 802.3bs].

13.6.3 FOIC4.8-RS 56G lane bit rate

The FOIC4.8-RS lane is synchronous to the FlexO-4-RS frame. There are eight lanes.

The bit rate and tolerance of the FOIC4.8-RS lane signal is defined in Table 13-4.

Table 13-4 – FOIC4.8-RS lane rate

FOIC4.8-RS nominal lane bit rate	Bit-rate tolerance
$30592/27233 \times 49\ 766\ 400$ kbit/s	±20 ppm
NOTE 1 – The nominal FOIC4.8-RS lane rate is approximately: 55 904 737.223 kbit/s NOTE 2 – FOIC4.8-RS_lane_rate = 400G_FlexO-4-RS_rate/8	

The 400G FlexO-4-RS bit rate is specified in clause 13.2.

13.6.4 m*FOIC4.8-RS interface

The m*FOIC4.8-RS interface supports multiple optical tributary signals on each of the m single optical spans with 3R regeneration at each end.

An m*FOIC4.8-RS interface signal contains one OTUCn signal distributed across the m optical interfaces and the k=8 lanes per optical interface.

Specifications of the optical tributary signal carrying each FOIC4.8-RS lane are contained in [ITU-T G.695] and [ITU-T G.959.1].

13.6.5 FOIC4.8-RS interface processes

Figure 13-6 shows the processes of 400G FlexO-4-RS. It can be seen that it is divided into three parts (the part of reusing 100G FlexO, the part of purely new design and the part of reusing IEEE802.3 400GE PCS/FEC).

The processes of scrambler/descrambler and AM insertion/removal are the only new designs. Before scrambler in the source and after descrambler in the sink, they keep completely the same processes as 100G FlexO's.

In the part of reusing IEEE802.3 400GE PCS lower-part and FEC, it completely reuses all processes related of IEEE802.3 400GE PCS lower-part and FEC. 400G FlexO uses 2*200G KP4-FEC.
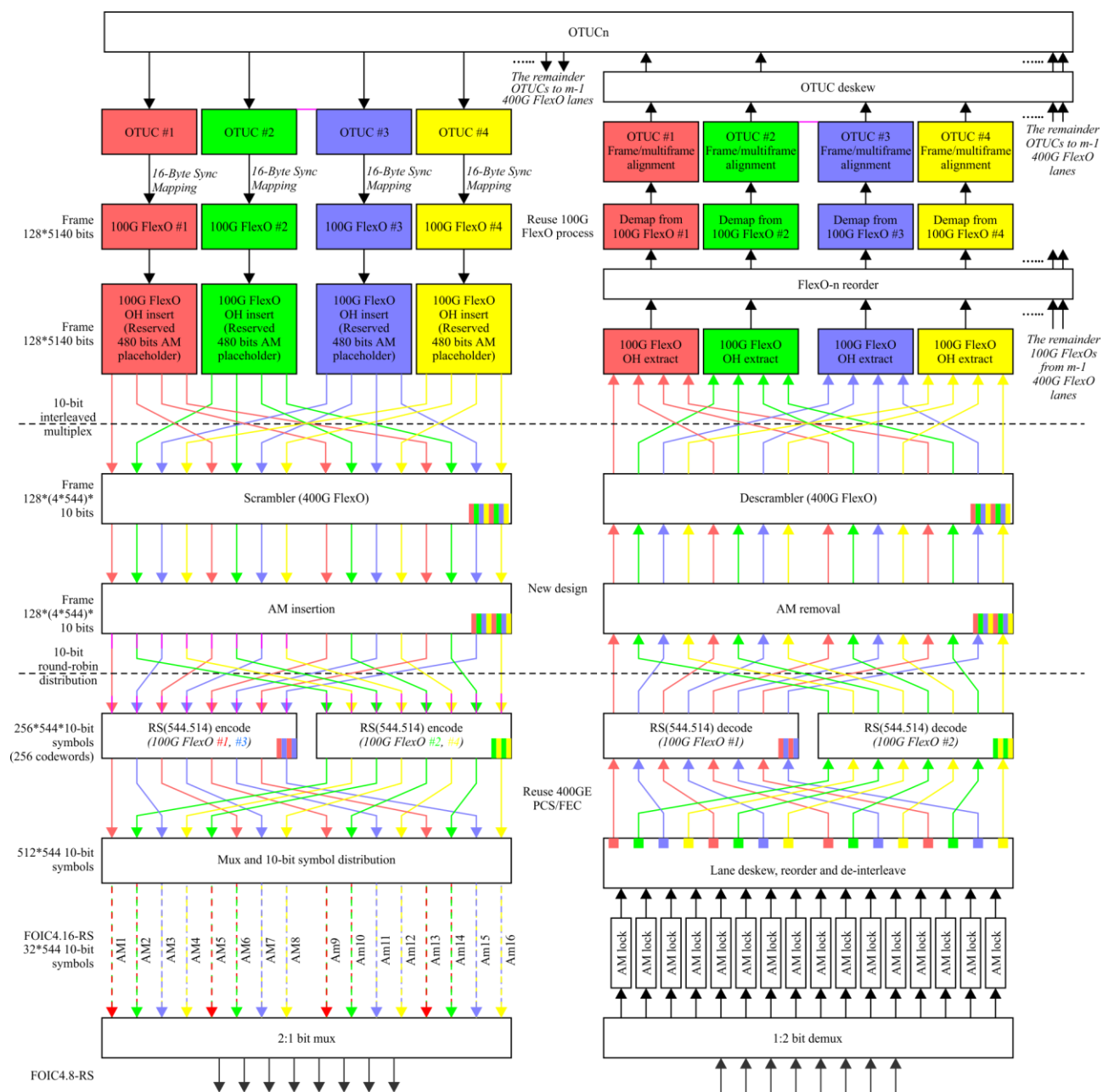
Figure 13-6 – 400G FlexO-4-RS processes

Appendix I

Example applications

(This appendix does not form an integral part of this Recommendation.)

FlexO-x-RS-m interface group can be used for a variety of applications. Example applications for a FlexO-x-RS interface are shown in Figure I.1 and Figure I.2. An interoperable interface might represent an OTN handoff between router (R) and transport (T) nodes, or could be a handoff between different administrative domains.
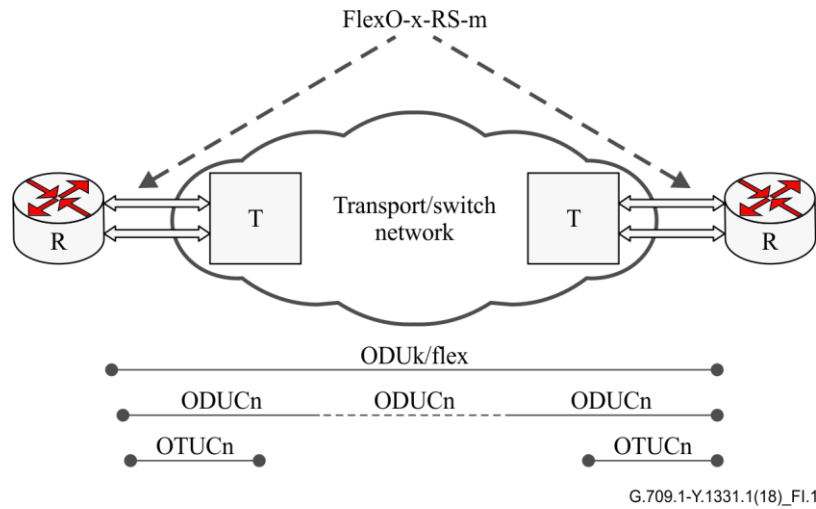

Figure I.1 – Example FlexO-x-RS handoff router-transport

The R-T topology is used in Figure I.1, to draw an analogy between FlexO-x-RS and FlexE use cases presented in [OIF FlexE]. The ODUk/flex (which can be a rate higher than 100Gbit/s) is the transport service (path) and maintenance entity in the OTN transport/switch network. The ODUCn/OTUCn is the section and FlexO-x-RS provides the interfacing capabilities (e.g., FEC, bonding and scrambling).
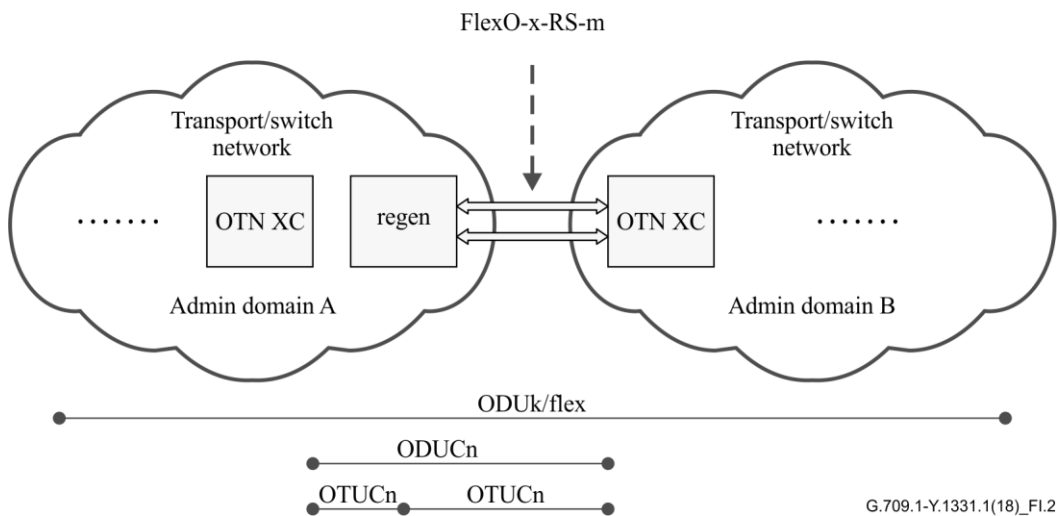

Figure I.2 – Example FlexO-x-RS inter-domain handoff

The example of Figure I.2 shows a FlexO-x-RS inter-domain interface used as a handoff between two OTN switch/transport administrative domains (A and B). The administrative domains can represent different carriers, different equipment vendors within a carrier or different segments (metro vs core) within a carrier. The OTUCn is the regenerator section, the ODUCn is the multiplexed section and the m*OTUC is the FlexO-x-RS-m interface group bonded using m FlexO-x-RS interfaces.

Bibliography

[b-ITU-T G-Sup.58]   ITU-T G-series Recommendations – Supplement 58 (2018), *Optical transport network (OTN) module framer interfaces (MFI).*

[b-IEEE 1588]   IEEE 1588-2008 - *IEEE Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems.*

[b-OIF CEI]   Optical Internetworking Forum Implementation Agreement OIF-CEI-04.0 (2017), *Common Electrical I/O (CEI) – Electrical and Jitter Interoperability agreements for 6G+ bps, 11G+ bps,25G+ bps and 56G+ bps I/O.*

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