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TELECOMMUNICATION
STANDARDIZATION SECTOR
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G.709/Y.1331

Amendment 1

(07/2010)

SERIES G: TRANSMISSION SYSTEMS AND MEDIA, DIGITAL SYSTEMS AND NETWORKS

Digital terminal equipments – General

SERIES Y: GLOBAL INFORMATION INFRASTRUCTURE, INTERNET PROTOCOL ASPECTS AND NEXT-GENERATION NETWORKS

Internet protocol aspects – Transport

Interfaces for the Optical Transport Network (OTN)

Amendment 1

Recommendation ITU-T G.709/Y.1331 (2009) – Amendment 1

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Recommendation ITU-T G.709/Y.1331

Interfaces for the Optical Transport Network (OTN)

Amendment 1

Summary

Amendment 1 to Recommendation ITU-T G.709/Y.1331 (2009) contains extensions related to the addition of 40GBASE-R and 100GBASE-R client mappings.

History

Edition	Recommendation	Approval	Study Group
1.0	ITU-T G.709/Y.1331	2001-02-09	15
1.1	ITU-T G.709/Y.1331 (2001) Amend. 1	2001-11-29	15
2.0	ITU-T G.709/Y.1331	2003-03-16	15
2.1	ITU-T G.709/Y.1331 (2003) Amend. 1	2003-12-14	15
2.2	ITU-T G.709/Y.1331 (2003) Cor. 1	2006-12-14	15
2.3	ITU-T G.709/Y.1331 (2003) Amend. 2	2007-11-22	15
2.4	ITU-T G.709/Y.1331 (2003) Cor.2	2009-01-13	15
2.5	ITU-T G.709/Y.1331 (2003) Amend. 3	2009-04-22	15
3.0	ITU-T G.709/Y.1331	2009-12-22	15
3.1	ITU-T G.709/Y.1331 (2009) Cor. 1	2010-07-29	15
3.2	ITU-T G.709/Y.1331 (2009) Amend. 1	2010-07-29	15

FOREWORD

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The World Telecommunication Standardization Assembly (WTSA), which meets every four years, establishes the topics for study by the ITU-T study groups which, in turn, produce Recommendations on these topics.

The approval of ITU-T Recommendations is covered by the procedure laid down in WTSA Resolution 1.

In some areas of information technology which fall within ITU-T's purview, the necessary standards are prepared on a collaborative basis with ISO and IEC.

NOTE

In this Recommendation, the expression "Administration" is used for conciseness to indicate both a telecommunication administration and a recognized operating agency.

Compliance with this Recommendation is voluntary. However, the Recommendation may contain certain mandatory provisions (to ensure, e.g., interoperability or applicability) and compliance with the Recommendation is achieved when all of these mandatory provisions are met. The words "shall" or some other obligatory language such as "must" and the negative equivalents are used to express requirements. The use of such words does not suggest that compliance with the Recommendation is required of any party.

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As of the date of approval of this Recommendation, ITU had received notice of intellectual property, protected by patents, which may be required to implement this Recommendation. However, implementers are cautioned that this may not represent the latest information and are therefore strongly urged to consult the TSB patent database at http://www.itu.int/ITU-T/ipr/.

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Recommendation ITU-T G.709/Y.1331

Interfaces for the Optical Transport Network (OTN)

Amendment 1

1) Introduction

This amendment contains extensions to the third edition (12/2009) of Recommendation ITU-T G.709/Y.1331, related to the addition of:

– 40GBASE-R and 100GBASE-R client mappings (clauses 2, 15.9.2.1.1, 17.7.4, 17.7.4.1, 17.7.5, 17.7.5.1, Annex E, Annex F, Appendix VII, and Appendix VIII).

2) Additions

2.1) Clause 2, References

Insert the following reference:

[IEEE 802.3ba] IEEE Std 802.3ba-2010, *Information Technology – Local and metropolitan area networks – Specific requirements – Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications – Amendment 4: Media Access Control Parameters, Physical Layers and Management Parameters for 40 Gb/s and 100 Gb/s Operation*.

2.2) Clause 15.9.2.1.1

Modify Table 15-8 as follows:

Table 15-8 – Payload type code points

MSB 1 2 3 4	LSB 5 6 7 8	Hex code (Note 1)	Interpretation
0 0 0 0	0 0 0 1	01	Experimental mapping (Note 3)
0 0 0 0	0 0 1 0	02	Asynchronous CBR mapping, see clause 17.2
0 0 0 0	0 0 1 1	03	Bit synchronous CBR mapping, see clause 17.2
0 0 0 0	0 1 0 0	04	ATM mapping, see clause 17.3
0 0 0 0	0 1 0 1	05	GFP mapping, see clause 17.4
0 0 0 0	0 1 1 0	06	Virtual Concatenated signal, see clause 18 (Note 5)
0 0 0 0	0 1 1 1	07	PCS codeword transparent Ethernet mapping: • 1000BASE-X into OPU0 ~~mapping~~, see clauses 17.7.1 and 17.7.1.1 • 40GBASE-R into OPU3, see clauses 17.7.4 and 17.7.4.1 • 100GBASE-R into OPU4, see clauses 17.7.5 and 17.7.5.1
0 0 0 0	1 0 0 0	08	FC-1200 into OPU2e mapping, see clause 17.8.2
0 0 0 0	1 0 0 1	09	GFP mapping into Extended OPU2 payload, see clause 17.4.1 (Note 6)

Table 15-8 – Payload type code points

MSB 1 2 3 4	LSB 5 6 7 8	Hex code (Note 1)	Interpretation
0 0 0 0	1 0 1 0	0A	STM-1 mapping into ODPU0, see clause 17.7.1
0 0 0 0	1 0 1 1	0B	STM-4 mapping into ODPU0, see clause 17.7.1
0 0 0 0	1 1 0 0	0C	FC-100 mapping into OPDU0, see clause 17.7.1
0 0 0 0	1 1 0 1	0D	FC-200 mapping into ODPU1, see clause 17.7.2
0 0 0 0	1 1 1 0	0E	FC-400 mapping into ODPUflex, see clause 17.9
0 0 0 0	1 1 1 1	0F	FC-800 mapping into ODPUflex, see clause 17.9
0 0 0 1	0 0 0 0	10	Bit stream with octet timing mapping, see clause 17.6.1
0 0 0 1	0 0 0 1	11	Bit stream without octet timing mapping, see clause 17.6.2
0 0 1 0	0 0 0 0	20	ODU multiplex structure supporting ODTUjk only, see clause 19 (AMP only)
0 0 1 0	0 0 0 1	21	ODU multiplex structure supporting ODTUk.ts or ODTUk.ts and ODTUjk, see clause 19 (GMP capable) (Note 7)
0 1 0 1	0 1 0 1	55	Not available (Note 2)
0 1 1 0	0 1 1 0	66	Not available (Note 2)
1 0 0 0	x x x x	80-8F	Reserved codes for proprietary use (Note 4)
1 1 1 1	1 1 0 1	FD	NULL test signal mapping, see clause 17.5.1
1 1 1 1	1 1 1 0	FE	PRBS test signal mapping, see clause 17.5.2
1 1 1 1	1 1 1 1	FF	Not available (Note 2)

2.3) Clause 17.7.4

Modify Tables 17-10A and 17-10B in clause 17.7.4 as follows:

Table 17-10A – C_m (m = 256) for CBR clients close to 40.149G into OPU3

Client signal	Nominal bit rate (kbit/s)	Bit rate tolerance (ppm)	Floor $C_{256, min}$ (Note)	Minimum c_{256}	Nominal c_{256}	Maximum c_{256}	Ceiling $C_{256, max}$ (Note)
Transcoded 40GBASE-R (see clause 17.7.4.1) ~~For further study~~	1027/1024 × 64/66 × 41 250 000	±100	475	475.548	475.605	475.662	476
NOTE – Floor $C_{m, min}$ (m = 256) and Ceiling $C_{m, max}$ (m = 256) values represent the boundaries of client/OPU ppm offset combinations (i.e., min. client/max. OPU and max. client/min. OPU). In steady state, given instances of client/OPU offset combinations should not result in generated C_m values throughout this range but rather should be within as small a range as possible. Under transient ppm offset conditions (e.g., AIS to normal signal), it is possible that C_m values outside the range $C_{m, min}$ to $C_{m, max}$ may be generated and a GMP demapper should be tolerant of such occurrences. Refer to Annex D for a general description of the GMP principles.							

Table 17-10B – C_n (n = 8 or 1) for CBR clients close to 40.149G into OPU3

Client signal	Nominal bit rate (kbit/s)	Bit rate tolerance (ppm)	Floor $C_{8, min}$ (Note)	Minimum c_8	Nominal c_8	Maximum c_8	Ceiling $C_{8, max}$ (Note)
~~For further study~~ Transcoded 40GBASE-R (see clause 17.7.4.1)	1027/1024 × 64/66 × 41 250 000	±100	15217	15217.529	15219.355	15221.181	15222
			Floor $C_{1, min}$ (Note)	Minimum c_1	Nominal c_1	Maximum c_1	Ceiling $C_{1, max}$ (Note)
For further study							
NOTE – Floor $C_{n, min}$ (n = 8, 1) and Ceiling $C_{n, max}$ (n = 8, 1) values represent the boundaries of client/OPU ppm offset combinations (i.e., min. client/max. OPU and max. client/min. OPU). In steady state, given instances of client/OPU offset combinations should not result in generated C_n values throughout this range but rather should be within as small a range as possible. Under transient ppm offset conditions (e.g., AIS to normal signal), it is possible that C_n values outside the range $C_{n, min}$ to $C_{n, max}$ may be generated and a GMP demapper should be tolerant of such occurrences. Refer to Annex D for a general description of the GMP principles.							

Table 17-11 – Replacement signal for CBR clients

Client signal	Replacement signal	Bit rate tolerance (ppm)
~~For further study~~ 40GBASE-R	Continuous 40GBASE-R local fault sequence ordered sets with four PCS lane alignment markers inserted after each 16383 × 4 sixty-six-bit blocks	±100

A 40GBASE-R local fault sequence ordered set is a 66B control block (sync header = 10) with a block type of 0x4B, an "O" code of 0x00, a value of 0x01 to indicate "local fault" in lane 3, and all of the other octets (before scrambling) equal to 0x00.

2.4) Clause 17.7.4.1

Modify clause 17.7.4.1 as follows:

17.7.4.1 40GBASE-R multi-lane processing and transcoding

~~For further study.~~

~~NOTE – Refer to Annex B, Appendix VII and Appendix VIII for further information.~~The 40GBASE-R client signal (64B/66B encoded, nominal aggregate bit-rate of 41 250 000 kbit/s, ±100 ppm) is recovered using the process described in Annex E for parallel 64B/66B interfaces. The lane(s) of the physical interface are bit-disinterleaved, if necessary, into four streams of 10 312 500 kbit/s. 66B block lock and lane alignment marker lock are acquired on each PCS lane, allowing the 66B blocks to be deskewed and reordered.

The resulting sequence is descrambled and transcoded according to the process described in Annex B into 513B code blocks. Each pair of two 513B code blocks is combined according to the process described in Annex F into a 1027B block, resulting in a bit stream of 1027/1024 × 40 000 000 kbit/s ±100 ppm (40 117 187.500 kbit/s ±100 ppm). This process is referred to as "timing transparent transcoding (TTT)", mapping a bit stream which is 1027/1056 times the bit-rate of the aggregate Ethernet signal.

In the mapper, the received Ethernet PCS lane BIP may be compared with the expected Ethernet PCS lane BIP as a non-intrusive monitor or section monitor.

The demapper will either insert a compensated Ethernet PCS lane BIP (for path monitoring) or a newly computed PCS lane BIP (for section monitoring) as described in Annex E.

For 40GBASE-R client mapping, 1-bit timing information (C_1) is not needed.

The demapper will recover from the output of the GMP processor 1027B block lock, and then transdecode each 1027B block to sixteen 66B blocks as described in Annex E. Transdecoded lane alignment markers are constructed with either a compensated BIP-8 or newly calculated BIP-8 depending on whether the interface is provisioned for path or section monitoring. The 66B blocks are then re-distributed round-robin to PCS lanes. If the number of PCS lanes is greater than the number of physical lanes of the egress interface, the appropriate numbers of PCS lanes are bit-multiplexed onto the physical lanes of the egress interface.

2.5) Clause 17.7.5

a) Modify Tables 17-12A and 17-12B in clause 17.7.5 as follows:

Table 17-12A – C_m (m = 640) for CBR clients close to 104.134G into OPU4

Client signal	Nominal bit rate (kbit/s)	Bit rate tolerance (ppm)	Floor $C_{640, min}$ (Note)	Minimum c_{640}	Nominal c_{640}	Maximum c_{640}	Ceiling $C_{640, max}$ (Note)
~~For further study~~ 100GBASE-R (see clause 17.7.5.1)	103 125 000	±100	188	188.131	188.154	188.177	189
NOTE – Floor $C_{m, min}$ (m = 640) and Ceiling $C_{m, max}$ (m = 640) values represent the boundaries of client/OPU ppm offset combinations (i.e., min. client/max. OPU and max. client/min. OPU). In steady state, given instances of client/OPU offset combinations should not result in generated C_m values throughout this range but rather should be within as small a range as possible. Under transient ppm offset conditions (e.g., AIS to normal signal), it is possible that C_m values outside the range $C_{m, min}$ to $C_{m, max}$ may be generated and a GMP demapper should be tolerant of such occurrences. Refer to Annex D for a general description of the GMP principles.							

Table 17-12B – C_n (n = 8 or 1) for CBR clients close to 104.134G into OPU4

Client signal	Nominal bit rate (kbit/s)	Bit rate tolerance (ppm)	Floor $C_{8,\,min}$ (Note)	Minimum c_8	Nominal c_8	Maximum c_8	Ceiling $C_{8,\,max}$ (Note)
~~For further study~~100GBASE-R (see clause 17.7.5.1)	103 125 000	±100	15050	15050.518	15052.324	15054.131	15055
			Floor $C_{1,\,min}$ (Note)	Minimum c_1	Nominal c_1	Maximum c_1	Ceiling $C_{1,\,max}$ (Note)
For further study							
NOTE – Floor $C_{n,\,min}$ (n = 8, 1) and Ceiling $C_{n,\,max}$ (n = 8, 1) values represent the boundaries of client/OPU ppm offset combinations (i.e., min. client/max. OPU and max. client/min. OPU). In steady state, given instances of client/OPU offset combinations should not result in generated C_n values throughout this range but rather should be within as small a range as possible. Under transient ppm offset conditions (e.g., AIS to normal signal), it is possible that C_n values outside the range $C_{n,\,min}$ to $C_{n,\,max}$ may be generated and a GMP demapper should be tolerant of such occurrences. Refer to Annex D for a general description of the GMP principles.							

Table 17-13 – Replacement signal for CBR clients

Client signal	Replacement signal	Bit rate tolerance (ppm)
~~For further study~~ 100GBASE-R (see clause 17.7.5.1)	Continuous 100GBASE-R local fault sequence ordered sets with 20 PCS lane alignment markers inserted after each 16383 × 20 sixty-six-bit blocks	±100

A 100GBASE-R local fault sequence ordered set is a 66B control block (sync header = 10) with a block type of 0x4B, an "O" code of 0x00, a value of 0x01 to indicate "local fault" in lane 3, and all of the other octets (before scrambling) equal to 0x00.

b) Add new clause 17.7.5.1 as follows:

17.7.5.1 100GBASE-R multi-lane processing

The 100GBASE-R client signal (64B/66B encoded, nominal aggregate bit-rate of 103 125 000 kbit/s ± 100 ppm) is recovered using the process described in Annex E for parallel 64B/66B interfaces. The lane(s) of the physical interface are bit-disinterleaved, if necessary, into twenty streams of 5 161 250 kbit/s. 66B block lock and lane alignment marker lock are acquired on each PCS lane, allowing the 66B blocks to be deskewed and reordered.

In the mapper, the received Ethernet PCS lane BIP may be compared with the expected Ethernet PCS lane BIP as a non-intrusive monitor or section monitor.

The demapper will either pass through the PCS lane BIP from the ingress (for path monitoring), or insert a newly computed PCS lane BIP (for section monitoring) as described in Annex E.

For 100GBASE-R client mapping, 1-bit timing information (C_1) is not needed.

The demapper will recover from the output of the GMP processor 64B/66B block lock per the state diagram in Figure 49-12 of [IEEE 802.3] or Figure 82-10 of [IEEE 802.3ba]. If the interface is provisioned to use BIP-8 for section monitoring, BIP-8 is recalculated in each lane alignment marker. The 66B blocks are re-distributed round-robin to PCS lanes. If the number of PCS lanes is greater than the number of physical lanes of the egress interface, the appropriate numbers of PCS lanes are bit-multiplexed onto the physical lanes of the egress interface.

2.6) Appendix V

Delete existant Appendix V.

2.7) Appendix VI

Modify Appendix VI as follows:

Change this appendix to Appendix V, *renumbering all figures and references to this appendix*.

2.8) Appendix VII

Modify Appendix VII as follows:

a) *Change this appendix to* Annex E, *renumbering all clauses, figures, tables and references to this appendix, as necessary*.

b) *Modify the first paragraph in clause VII.1 as follows*:

IEEE 40GBASE-R and 100GBASE-R interfaces ~~currently being~~ specified ~~by the~~in [IEEE ~~P802~~ 802.3ba]-2010 ~~task force will be~~are parallel interfaces intended for short-reach (up to 40 km) interconnection of Ethernet equipment.

c) *Modify the second and the third dash items in clause VII.3 as follows*:

– recover 64B/66B block lock per the state diagram in Figure 49-12 of [IEEE 802.3] (or Figure 82-10 of [~~b-~~IEEE 802.3ba] ~~D2.2~~);

– recover lane alignment marker framing on each PCS lane per the state diagram in Figure 82-11 of [~~b-~~IEEE 802.3ba] ~~D2.2~~.

d) *Modify the last paragraph in clause VII.3 as follows*:

After 64B/66B block lock recovery per the state diagram in Figure 49-12 of [IEEE 802.3] (or Figure 82-10 of [~~b-~~IEEE 802.3ba] ~~D2.2~~), these 66B blocks are re-distributed to PCS lanes at the egress interface. The 66B blocks (including PCS lane alignment markers) resulting from the decoding process are distributed round-robin to PCS lanes. If the number of PCS lanes is greater than the number of physical lanes of the egress interface, the appropriate numbers of PCS lanes are bit-multiplexed onto the physical lanes of the egress interface.

e) *Modify the first paragraph in clause VII.3.1 as follows*:

PCS lane alignment markers have the values shown in Table VII.1 for 40GBASE-R signals which use PCS lane numbers 0-3. ~~Note that these values will need to be aligned with the published IEEE 802.3ba amendment once it is approved.~~

f) *Modify the first paragraph in clause VII.3.2 as follows*:

PCS lane alignment markers have the values shown in Table VII.2 for 100GBASE-R signals which use PCS lane numbers 0-19. ~~Note that these values will need to be aligned with the published IEEE 802.3ba amendment once it is approved.~~

In case of end-to-end path monitoring the lane alignment markers transported over the OPU4 are distributed unchanged to the PCS lanes. In the case of section monitoring the lane alignment markers are located as defined in state diagram in Figure 82-11 of [~~b-~~IEEE 802.3ba] ~~D2.2~~ and the

BIP-8 is newly calculated for each PCS lane as defined in clause 82.2.8 of [~~b-~~IEEE 802.3ba]~~ D2.2~~. This value overwrites BIP_3 and the complement overwrites BIP_7.

g) Modify the sixth paragraph in clause VII.4 as follows:

It will then be up to the Ethernet receiver to handle bit errors within the OTN section that might have altered the PCS alignment marker encodings (for details refer to clause 82.2.1~~9~~8.3 and Figure 82-11 in [~~b-~~IEEE 802.3ba]).

h) Modify the eighth, ninth and tenth paragraphs in clause VII.4.1 as follows:

The OTN BIP-8 is calculated similar to the PCS BIP-8 as described in clause 82.2.8 of [~~b-~~IEEE 802.3ba] ~~D2.2~~ with the exception that the calculation will be done over unscrambled PCS lane data, the original received lane alignment marker and before transcoding. Figure VII.2 shows the byte location of the OTN BIP-8 in the transcoded lane marker.

The transcoded lane marker is transmitted together with the transcoded data blocks over the OTN section as defined in Annex B. At the OTN egress after transdecoding and before scrambling, the ingress alignment marker is recreated using M_0, M_1, M_2 and ingress BIP_3 of the transcoded alignment marker followed by the bit-wise inversion of these bytes. This recreated alignment marker together with the transdecoded and unscrambled data blocks is used to calculate the expected OTN BIP-8 for each PCS lane (refer to clause 82.2.8 of [~~b-~~IEEE 802.3ba]~~ D2.2~~). The expected value will be XORed with the received OTN BIP-8. This error mask will have a "1" for each bit of the OTN BIP-8 which is wrong, and a "0" for each bit which is correct.

The egress BIP_3 for each PCS lane is calculated over the transdecoded and scrambled data blocks including the transdecoded alignment marker (refer to clause VII.4) following the process depicted in clause 82.2.8 of [~~b-~~IEEE 802.3ba]~~ D2.2~~. This is the value that is transmitted in case of section monitoring.

i) Modify the last paragraph in clause VII.4.2 as follows:

An invalid 66B block will be converted to an error control block before transcoding or direct adaptation. An invalid 66B block is one which does not have a sync header of "01" or "10", or one which has a sync header of "10", is not a valid PCS lane alignment marker and has a control block type field which does not appear in Figure B.2~~ (and for 40GBASE-R and 100GBASE-R, is not a valid PCS lane alignment marker)~~ or has one of the values 0x2d, 0x33, 0x66, or 0x55 which are not used for 40GBASE-R or 100GBASE-R. An error control block has sync bits of "10", a block type code of 0x1e, and 8 seven-bit/E/error control characters. This will prevent the Ethernet receiver from interpreting a sequence of bits containing this error as a valid packet.

2.9) Appendix VIII

Modify Appendix VIII as follows:

Change this appendix to Annex F, *renumbering all clauses, figures, tables and references to this appendix, as necessary*.

2.10) Appendix IX

Modify Appendix IX as follows:

Change this appendix to Appendix VI, *renumbering all tables and references to this appendix, as necessary*.

2.11) Appendix X

Modify Appendix X as follows:

a) *Change this appendix to* Appendix VII, *renumbering all tables and references to this appendix, as necessary*.

b) *Modify the first and second paragraphs in Appendix X as follows*:

The purpose of the OTM-0.4v4 interface, as defined in 8.1.3, is to enable the re-use of modules developed for Ethernet 100GBASE-LR4 or 100GBASE-ER4 interfaces. These modules have corresponding optical specifications for OTU4 interfaces with the optical parameters as specified for the application codes 4I1-9D1F and 4L1-9C1F, respectively, in [ITU-T G.959.1]. These modules have a four-lane WDM interface to and from a transmit/receive pair of G.652 optical fibres, and connect to the host board via a 10-lane electrical interface. The conversion between 10 and 4 lanes is performed using an IEEE 802.3ba PMA sublayer as specified in [~~b-~~IEEE 802.3ba] ~~D2.2~~ clause 83. The specification of the 10-lane electrical chip-to-module interface (CAUI) is found in [~~b-~~IEEE 802.3ba] ~~D2.2~~ Annex 83B. The application of the OTL4.10 interface is illustrated in Figure X.1:

Each OTL4.10 lane carries two bit-multiplexed logical lanes of an OTU4 as described in Annex C. The logical lane format has been chosen so that the [~~b-~~IEEE 802.3ba] 10:4 PMA (gearbox) will convert the OTU4 signal between a format of 10 lanes of OTL4.10 and four lanes of OTL4.4. Each OTL4.4 lane carries five bit-multiplexed logical lanes of an OTU4 as described in Annex C.

2.12) Appendix XI

Modify Appendix XI as follows:

Change this appendix to Appendix VIII, *renumbering all tables and references to this appendix, as necessary*.

2.13) Appendix XII

Modify Appendix XII as follows:

Change this appendix to Appendix IX, *renumbering all tables and references to this appendix, as necessary*.

2.14) Bibliography

Modify the Bibliography as follows:

~~[b-IEEE 802.3ba] IEEE 802.3 ba, 40 Gb/s and 100 Gb/s Ethernet TaskForce.~~

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For further details, please refer to the list of ITU-T Recommendations.

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