INTERNATIONAL TELECOMMUNICATION UNION

CCITT G.709

THE INTERNATIONAL
TELEGRAPH AND TELEPHONE
CONSULTATIVE COMMITTEE

GENERAL ASPECTS OF DIGITAL TRANSMISSION SYSTEMS;

TERMINAL EQUIPMENTS

SYNCHRONOUS MULTIPLEXING STRUCTURE

Recommendation G.709

Geneva, 1991

FOREWORD

The CCITT (the International Telegraph and Telephone Consultative Committee) is a permanent organ of the International Telecommunication Union (ITU). CCITT is responsible for studying technical, operating and tariff questions and issuing Recommendations on them with a view to standardizing telecommunications on a worldwide basis.

The Plenary Assembly of CCITT which meets every four years, establishes the topics for study and approves Recommendations prepared by its Study Groups. The approval of Recommendations by the members of CCITT between Plenary Assemblies is covered by the procedure laid down in CCITT Resolution No. 2 (Melbourne, 1988).

Recommendation G.709 was prepared by Study Group XVIII and was approved under the Resolution No. 2 procedure on the 5th of April 1991.

CCITT NOTES

1) In this Recommendation, the expression "Administration" is used for conciseness to indicate both a telecommunication Administration and a recognized private operating agency.

2) A list of abbreviations used in this Recommendation can be found in Annex A.

Recommendation G.709

SYNCHRONOUS MULTIPLEXING STRUCTURE

(Melbourne, 1988, revised 1990)

The CCITT,

considering

(a) that Recommendation G.707 describes the advantages offered by a synchronous digital hierarchy (SDH) and multiplexing method and specifies a set of SDH bit rates;

(b) that Recommendation G.708 specifies:

- the general principles and frame structure of the network-node interface (NNI) for the SDH;
- the overall frame size of 9 rows by N × 270 columns;
- the section overhead (SOH) together with its byte allocation;
- arrangements for international interconnection of synchronous transport modules (STMs);

(c) that Recommendations G.707, G.708 and G.709 form a coherent set of specifications for the SDH and NNI,

recommends

that the formats for multiplexing and mapping elements into the STM-N at the NNI shall be as described in this Recommendation.

1 Basic multiplexing structure

Descriptions of the various multiplexing elements are given in Recommendation G.708.

The relationships between the various multiplexing elements are shown in Figure 1-1/G.709. The detailed multiplexing structure is described in the following sections.

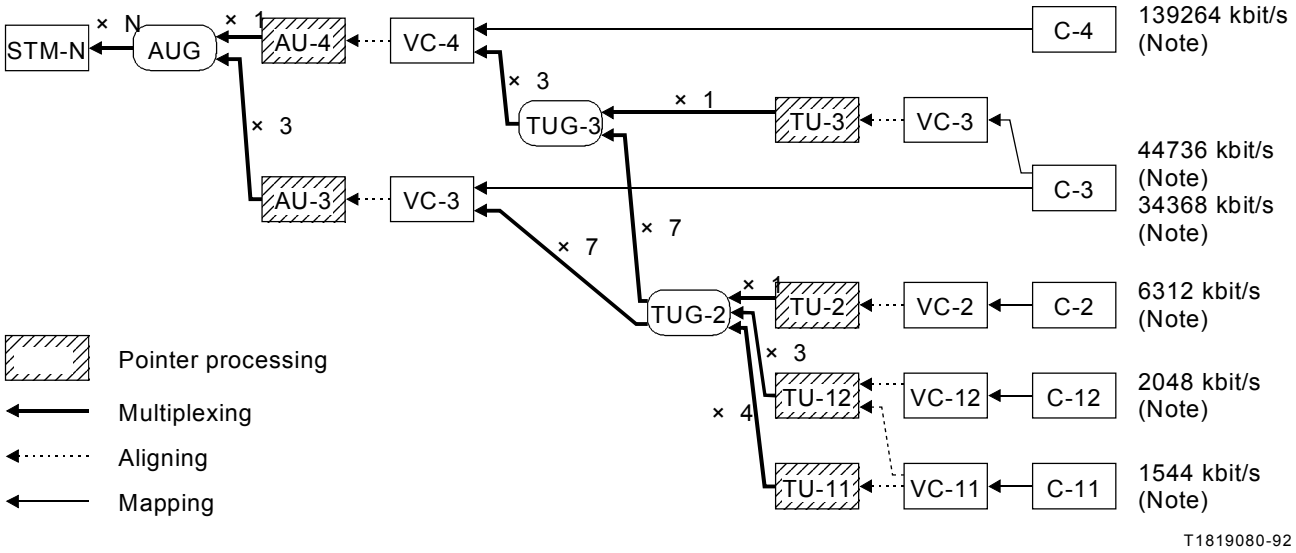
Note – The order of transmission of information in all the diagrams in Recommendation G.709 is first from left to right and then from top to bottom. Within each byte the most significant bit is transmitted first. The most significant bit (bit 1) is illustrated on the left in all the diagrams.

2 Multiplexing method

2.1 *Multiplexing of administrative units (AUs) into STM-N*

2.1.1 *Multiplexing of administrative unit groups (AUGs) into STM-N*

The arrangement of N AUGs multiplexed into the STM-N is shown in Figure 2-1/G.709. The AUG is a structure of 9 rows by 261 columns plus 9 bytes in row four (for the AU pointers). The STM-N consists of an SOH as described in Recommendation G.708 and a structure of 9 rows by N × 261 columns with N × 9 bytes in row four (for the AU pointers). The N AUGs are one-byte interleaved into this structure and have a fixed phase relationship with respect to the STM-N.



Note – G.702 tributaries associated with containers C-*x* are shown. Other signals, e.g. ATM, can also be accommodated.

FIGURE 1-1/G.709

Multiplexing structure

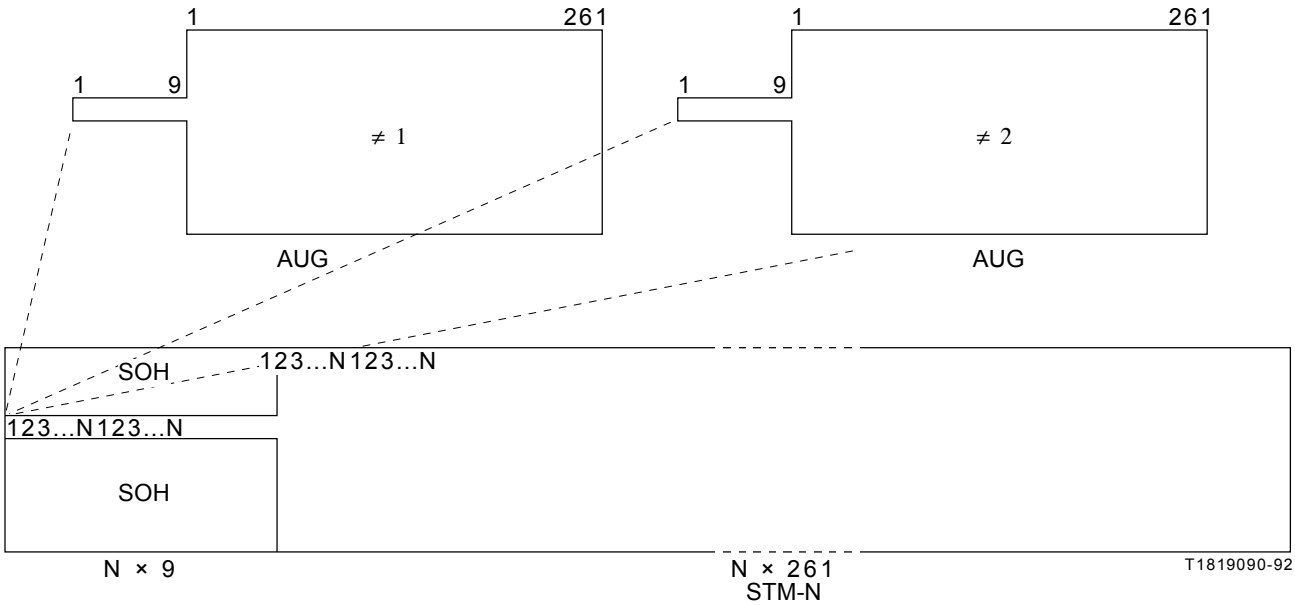
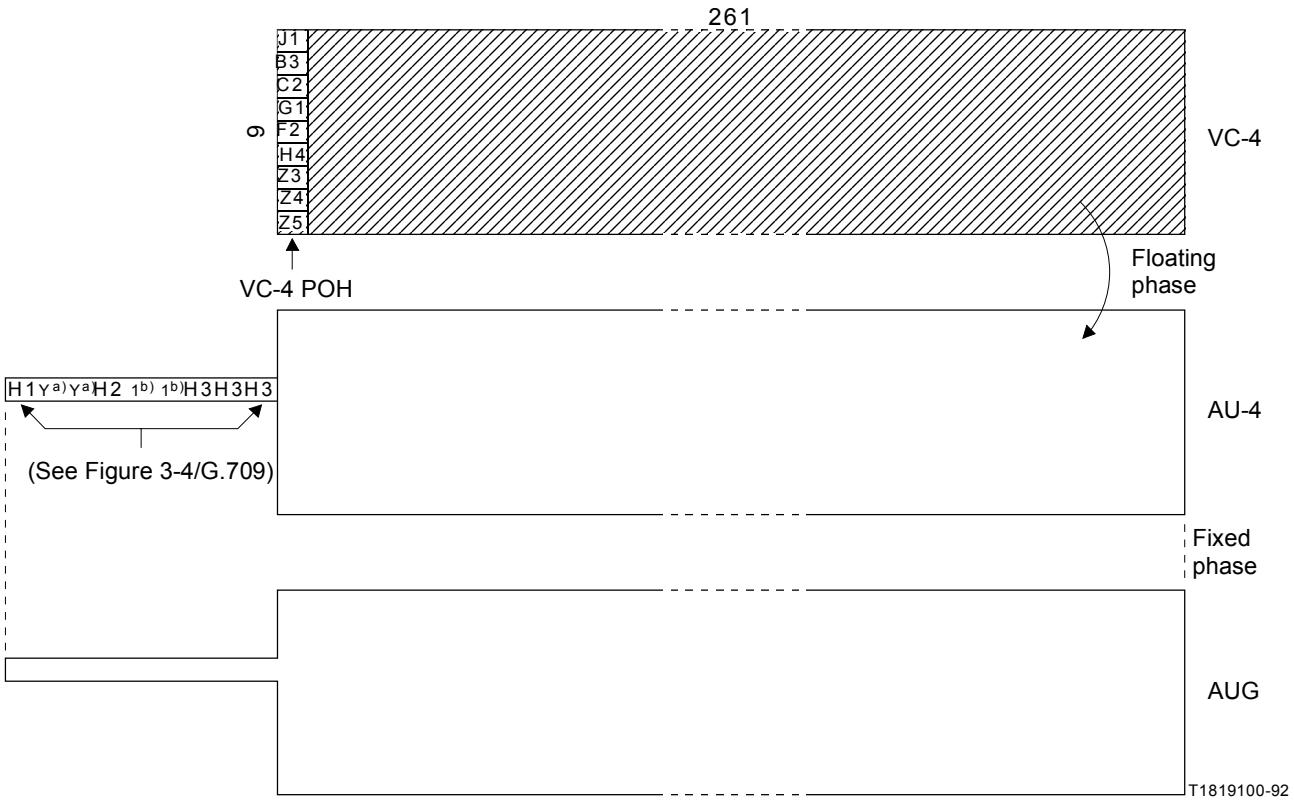


FIGURE 2-1/G.709

Multiplexing of N AUGs into STM-N

2.1.2 *Multiplexing of AU-4s via AUG*

The multiplexing arrangement of a single AU-4 via the AUG is depicted in Figure 2-2/G.709. The 9 bytes at the beginning of row four are allocated to the AU-4 pointer. The remaining 9 rows by 261 columns is allocated to the virtual container-4 (VC-4). The phase of the VC-4 is not fixed with respect to the AU-4. The location of the first byte of the VC-4 with respect to the AU-4 pointer is given by the pointer value. The AU-4 is placed directly in the AUG.



a) Y byte: 1001SS11 (S bits are unspecified).
b) All 1st byte.

FIGURE 2-2/G.709

Multiplexing of AU-4s via AUG

2.1.3 *Multiplexing of AU-3s via AUG*

The multiplexing arrangement of three AU-3s via the AUG is depicted in Figure 2-3/G.709. The 3 bytes at the beginning of row four are allocated to the AU-3 pointer. The remaining 9 rows by 87 columns is allocated to the VC-3 and two columns of fixed stuff. The phase of the VC-3 and the two columns of fixed stuff is not fixed with respect to the AU-3. The location of the first byte of the VC-3 with respect to the AU-3 pointer is given by the pointer value. The three AU-3s are one-byte interleaved in the AUG.

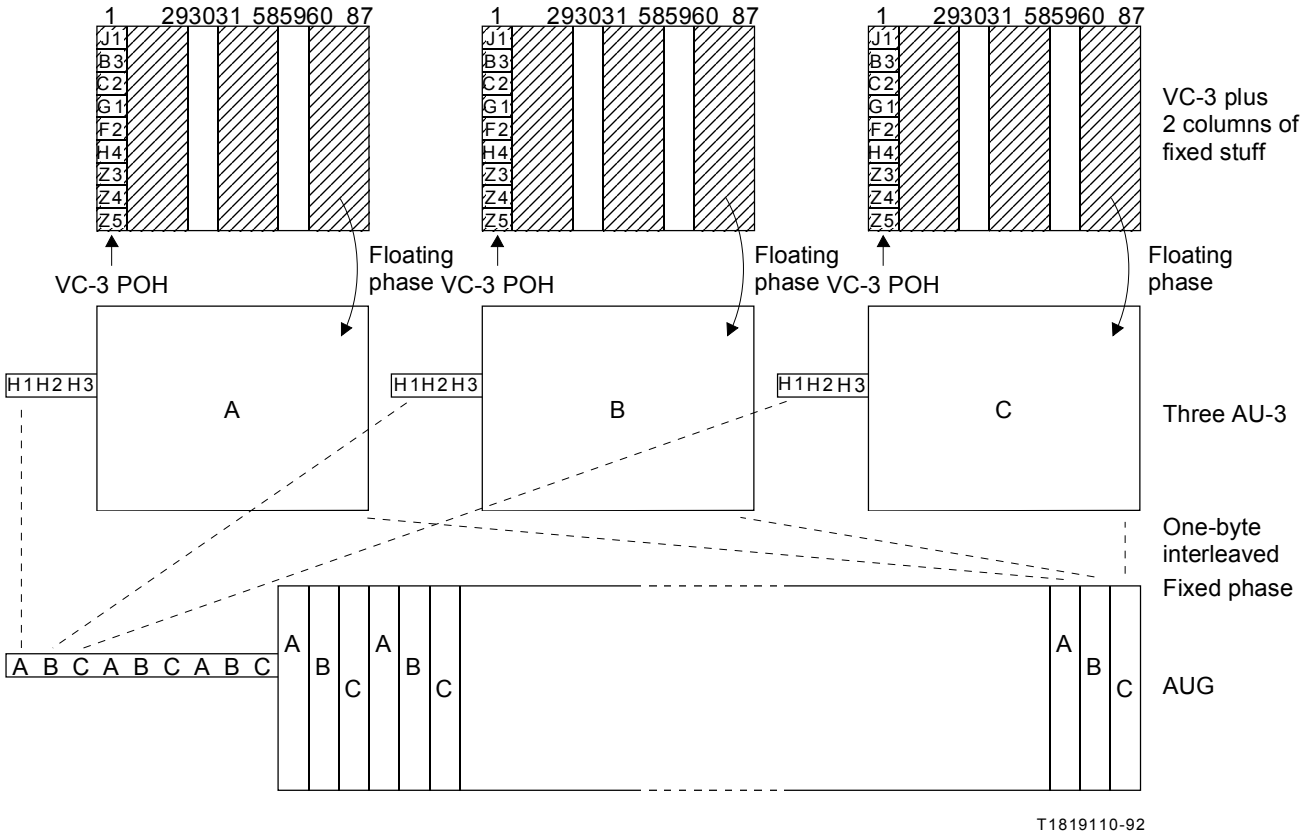


FIGURE 2-3/G.709

Multiplexing of AU-3s via AUG

2.2 *Multiplexing of tributary units (TUs) into VC-4 and VC-3*

2.2.1 *Multiplexing of tributary unit group-3s (TUG-3s) into a VC-4*

The arrangement of three TUG-3s multiplexed in the VC-4 is shown in Figure 2-4/G.709. The TUG-3 is a 9-row by 86-column structure. The VC-4 consists of one column of VC-4 POH, two columns of fixed stuff and a 258-column payload structure. The three TUG-3s are single byte interleaved into the 9-row by 258-column VC-4 payload structure and have a fixed phase with respect to the VC-4.

As described in § 2.1, the phase of the VC-4 with respect to the AU-4 is given by the AU-4 pointer.

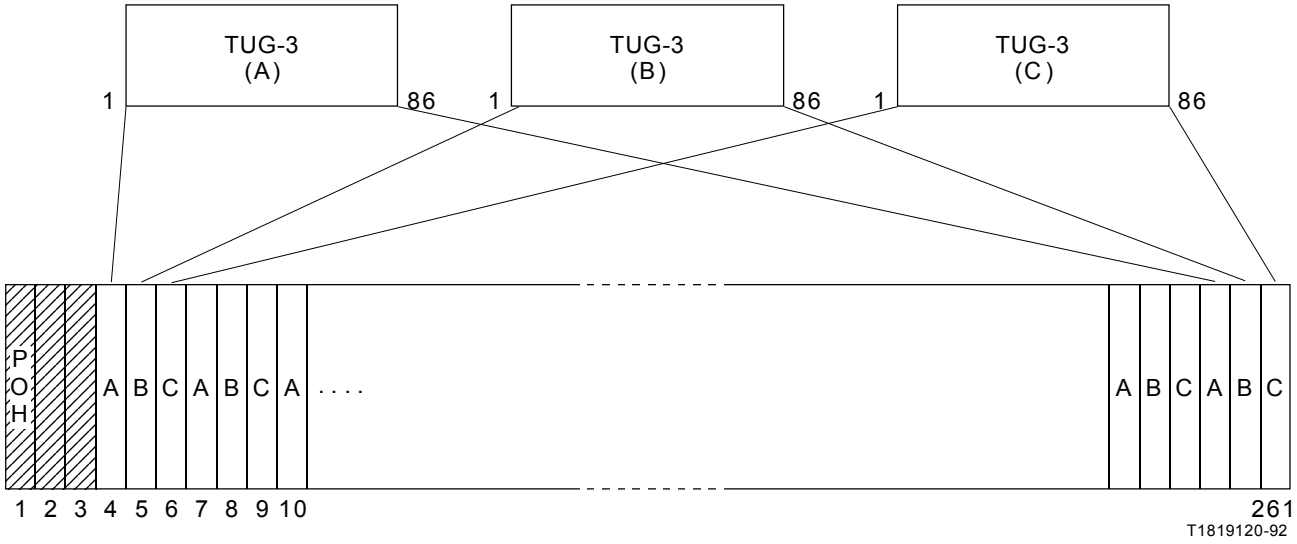


FIGURE 2-4/G.709

Multiplexing of three TUG-3s into a VC-4

2.2.2 *Multiplexing of TU-3s via TUG-3*

The multiplexing of a single TU-3 via the TUG-3 is depicted in Figure 2-5/G.709. The TU-3 consists of the VC-3 with a 9-byte VC-3 POH and the TU-3 pointer. The first column of the 9-row by 86-column TUG-3 is allocated to the TU-3 pointer (bytes H1, H2, H3) and fixed stuff. The phase of the VC-3 with respect to the TUG-3 is indicated by the TU-3 pointer.

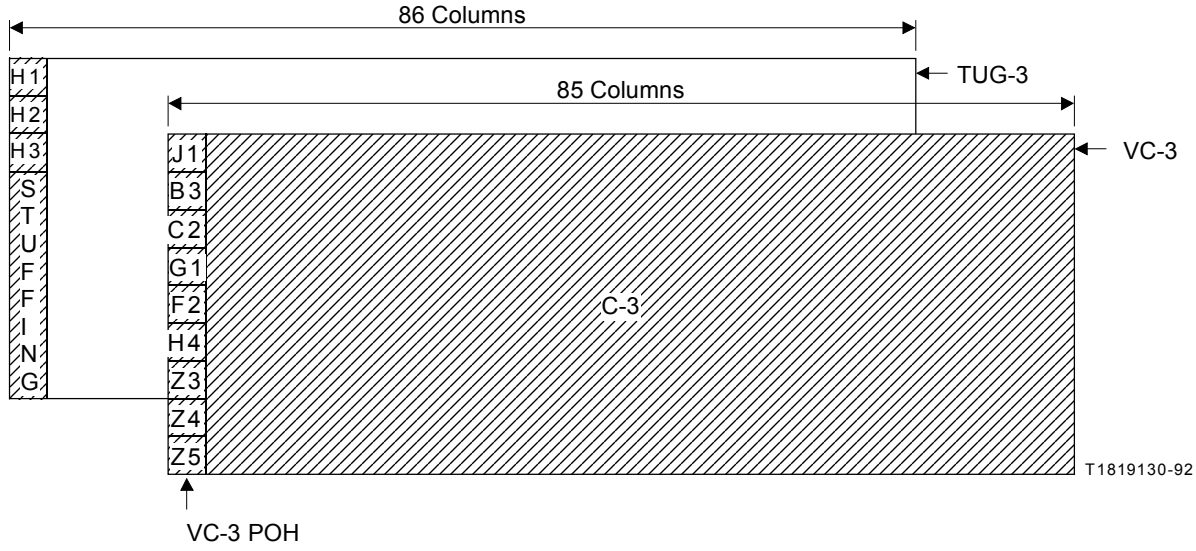


FIGURE 2-5/G.709

Multiplexing of a TU-3 via a TUG-3

2.2.3 *Multiplexing of TUG-2s via TUG-3*

The multiplexing structure for the TUG-2 via the TUG-3 is depicted in Figure 2-6/G.709. The TUG-3 is a 9-row by 86-column structure with the first two columns accommodating the following:

– A null pointer indication (NPI) contained in the first three bytes of the first column. This NPI can be used to distinguish between TUG-3s containing TU-3s and TUG-3s containing TUG-2s. See § 3.2 for details.

– Stuffing in the other bytes of these two columns.

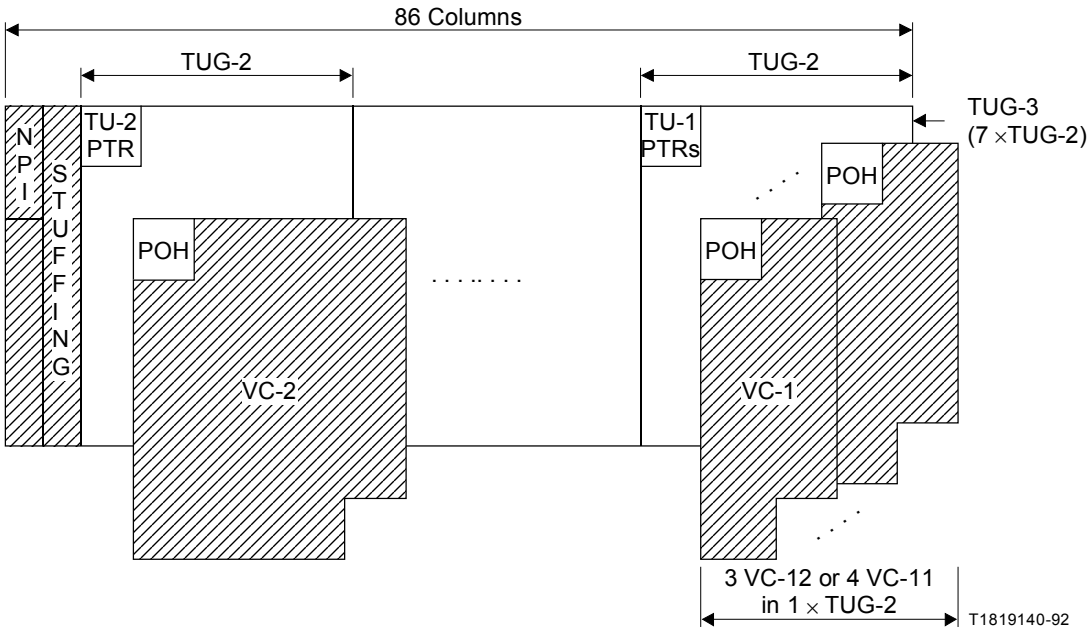


FIGURE 2-6/G.709

Multiplexing of seven TUG-2s via a TUG-3

A group of seven TUG-2s can be multiplexed via the TUG-3.

The arrangement of seven TUG-2s multiplexed via the TUG-3 is depicted in Figure 2-7/G.709. The TUG-2s are one-byte interleaved in the TUG-3.

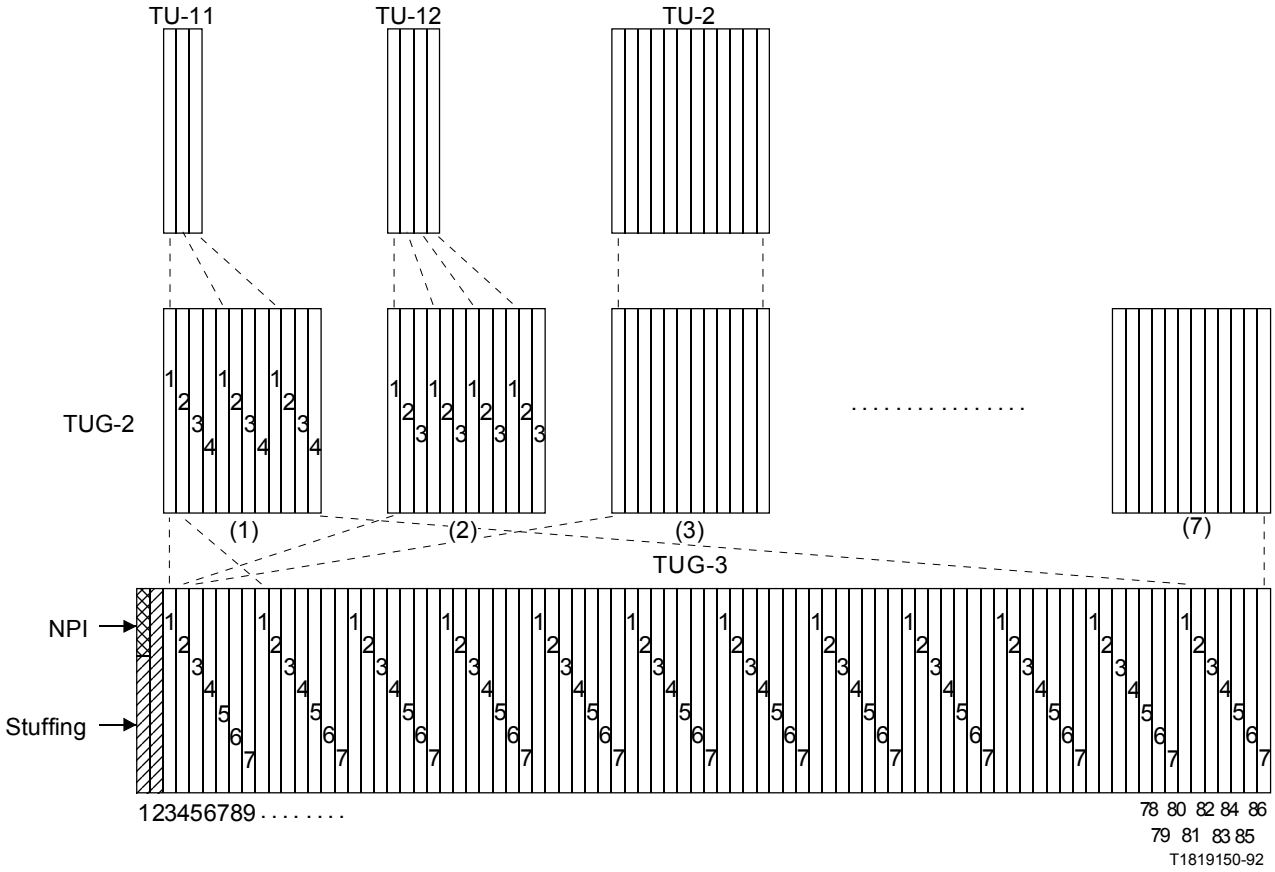


FIGURE 2-7/G.709

Multiplexing of seven TUG-2s via a TUG-3

2.2.4 *Multiplexing of TUG-2s into a VC-3*

The multiplexing structure for TUG-2s into a VC-3 is depicted in Figure 2-8/G.709. The VC-3 consists of VC-3 POH and a 9-row by 84-column payload structure. A group of seven TUG-2s can be multiplexed into the VC-3.

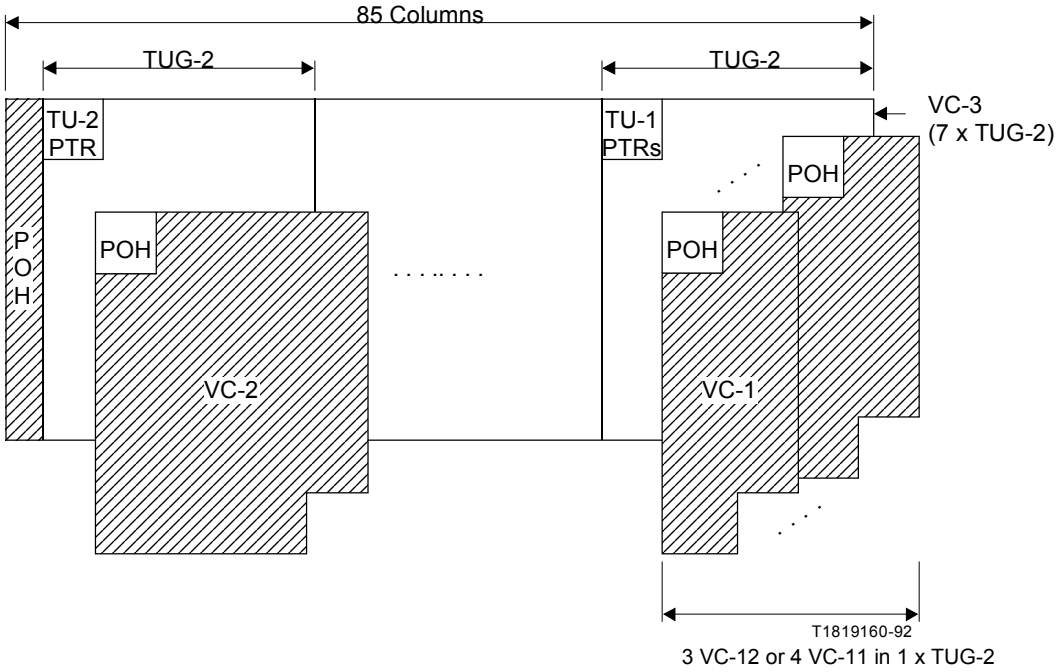


FIGURE 2-8/G.709

Multiplexing of seven TUG-2s into a VC-3

The arrangement of seven TUG-2s multiplexed into the VC-3 is depicted in Figure 2-9/G.709. The TUG-2s are one-byte interleaved in the VC-3. An individual TUG-2 has a fixed location in the VC-3 frame.

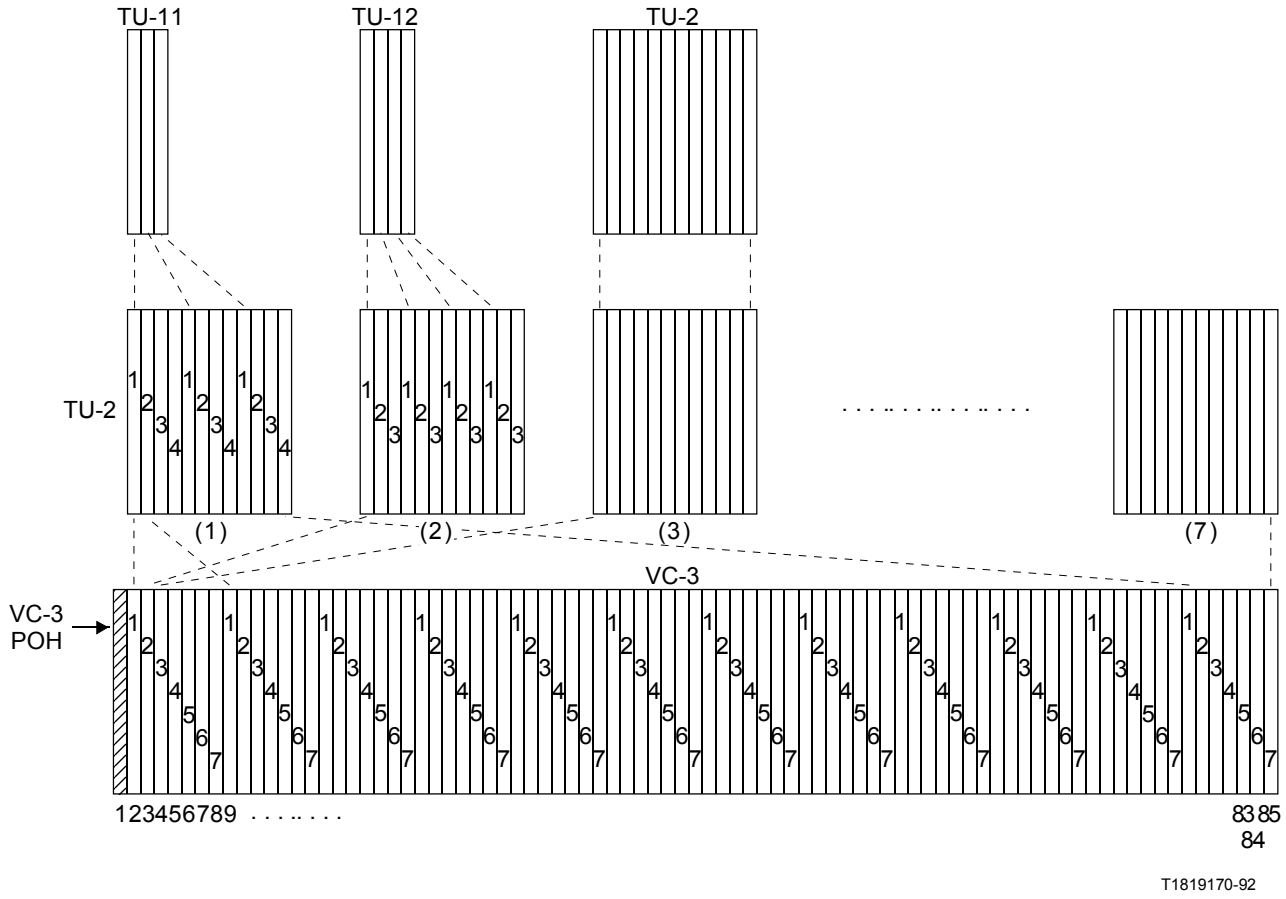


FIGURE 2-9/G.709

Multiplexing of seven TUG-2s into a VC-3

2.2.5 *Multiplexing of TU-2s via TUG-2s*

The multiplexing arrangement of a single TU-2 via the TUG-2 is depicted in Figure 2-9/G.709.

2.2.6 *Multiplexing of TU-1s via TUG-2s*

The multiplexing arrangements of four TU-11s or three TU-12s via the TUG-2 are depicted in Figure 2-9/G.709. The TU-1s are one-byte interleaved in the TUG-2.

2.3 *Maintenance signals*

2.3.1 *Section maintenance signals*

An alarm indication signal (AIS) is a signal sent downstream as an indication that an upstream failure has been detected and alarmed.

The section AIS is detected as an all "1"s in bits 6, 7, 8 of byte K2 after descrambling.

The far end receive failure (FERF) is used to return an indication to the transmit end that the received end has detected an incoming section failure or is receiving section AIS.

FERF is detected by a "110" code in bit positions 6, 7 and 8 of the K2 byte after descrambling.

2.3.2 *Path maintenance signals*

The VC-*n* (*n* = 3, 4) unequipped indication is an all "0"s VC-*n* path signal label (byte C2) after descrambling. This code indicates to the VC-*n* terminating equipment that the VC-*n* is intentionally unoccupied so that alarms can be inhibited. This code is generated as an all "0"s VC-*n* path signal label and a valid VC-*n* path BIP-8 (B3); the VC-*n* payload is unspecified.

The TU-*n* (*n* = 1, 2, 3) path AIS is specified as all "1"s in the entire TU-*n*, including the TU-*n* pointer. Similarly, the AU-*n* (*n* = 3, 4) path AIS is specified as all "1"s in the entire AU-n, including the AU-n pointer. All path AISs are carried within STM-N signals having valid SOH.

The path status byte (G1) is used to convey to the originator of a VC-*n* (*n* = 3 or 4) the terminating path status and performance. Bits 1 through 4 convey the count of errored parity blocks called far end block error (FEBE), detected using the path BIP-8 code. This code has nine legal values, 0-8. The remaining seven possible values should be interpreted as zero errors. Bit 5 is a path FERF.

2.4 *Timing recovery*

The STM-N (N ≥ 1) signal must have sufficient bit timing content at the NNI. A suitable bit pattern, which prevents a long sequence of "1"s and "0"s is provided by using a scrambler.

The operation of the scrambler shall be functionally identical to that of a frame synchronous scrambler of sequence length 127 operating at the line rate.

The generating polynomial shall be $1 + x^6 + x^7$. Figure 2-10/G.709 gives a functional diagram of the frame synchronous scrambler.

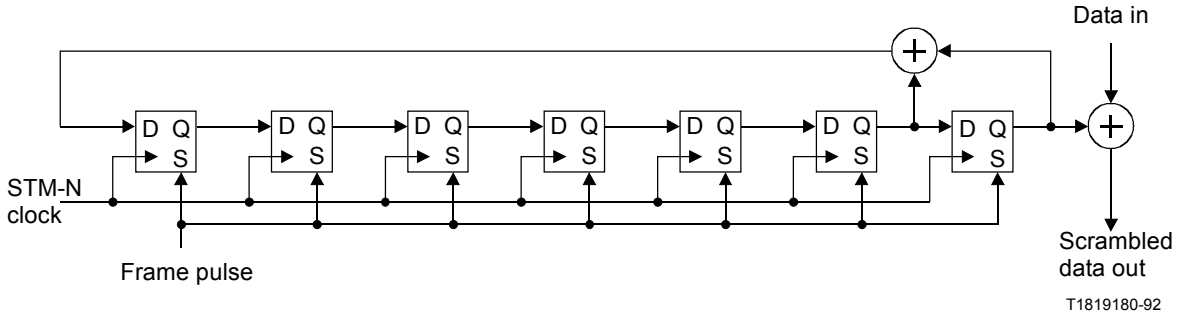


FIGURE 2-10/G.709

Frame synchronous scrambler (functional diagram)

The scrambler shall be reset to "1111111" on the most significant bit of the byte following the last byte of the first row of the STM-N SOH. This bit, and all subsequent bits to be scrambled shall be added to modulo 2 to the output from the x^7 position of the scrambler. The scrambler shall run continuously throughout the complete STM-N frame.

The first row of the STM-N SOH (9 × N bytes, including the A1 and A2 framing bytes) shall not be scrambled.

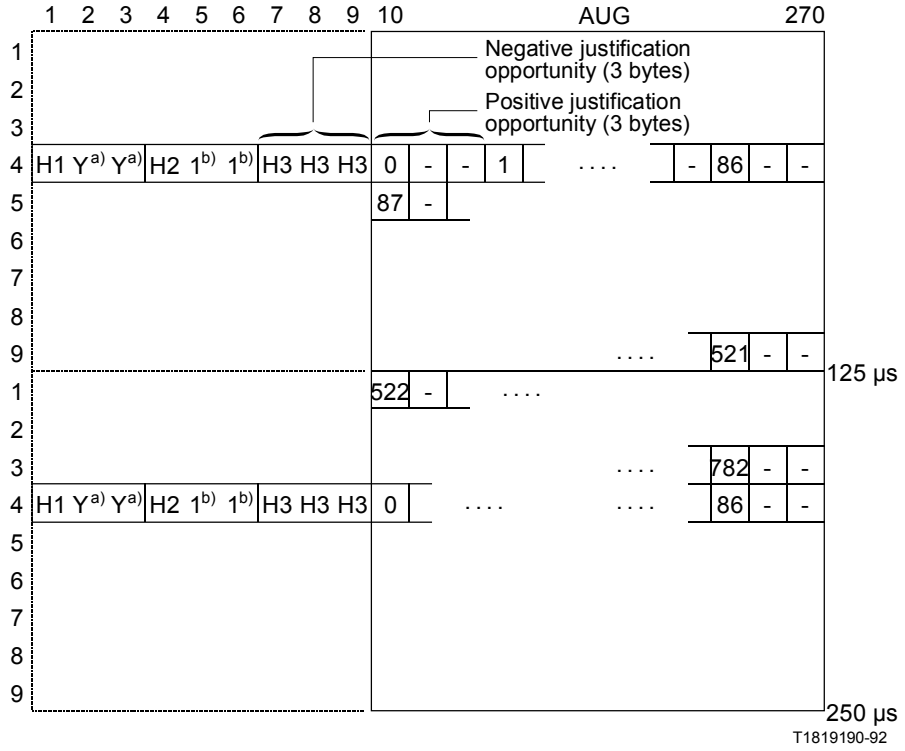
Note – Care should be taken in selecting the binary content of the bytes reserved for national use and which are excluded from the scrambling process of the STM-N signal to ensure that long sequences of "1"s or "0"s do not occur.

3 Pointers

3.1 *AU pointer*

The AU pointer provides a method of allowing flexible and dynamic alignment of the VC within the AU frame.

Dynamic alignment means that the VC is allowed to "float" within the AU frame. Thus, the pointer is able to accommodate differences, not only in the phases of the VC and the SOH, but also in the frame rates.



a) Y byte: 1001SS11 (S bits are unspecified).
b) All 1s byte.

FIGURE 3-1/G.709

AU-4 pointer offset numbering

3.1.1 *AU pointer location*

The AU-4 pointer is contained in bytes H1, H2 and H3 as shown in Figure 3-1/G.709. The three individual AU-3 pointers are contain in three separate H1, H2 and H3 bytes as shown in Figure 3-2/G.709.

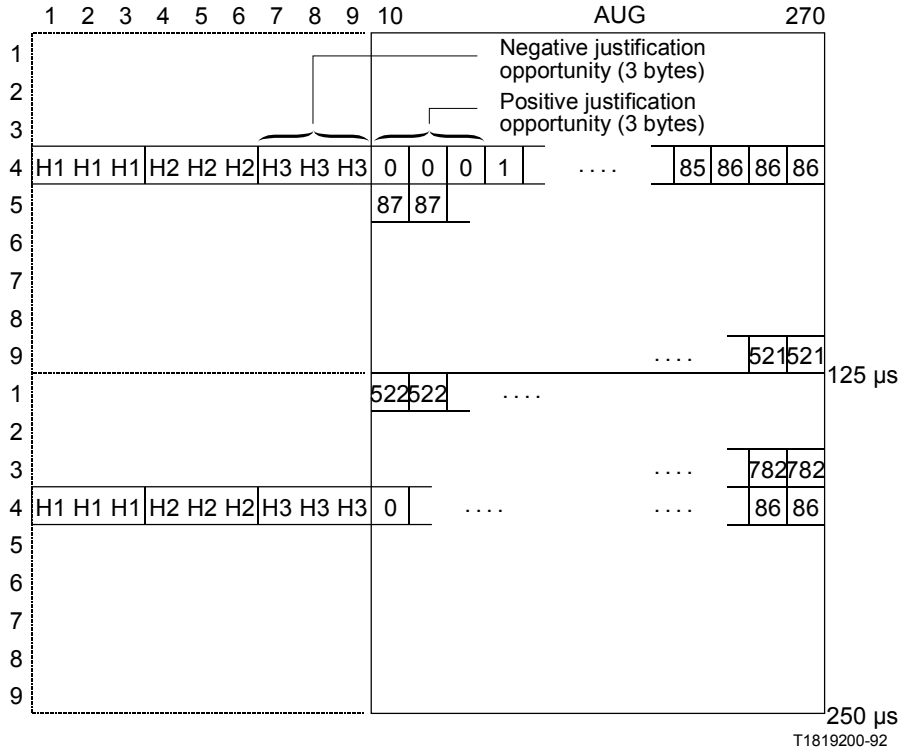


FIGURE 3-2/G.709

AU-3 pointer offset numbering

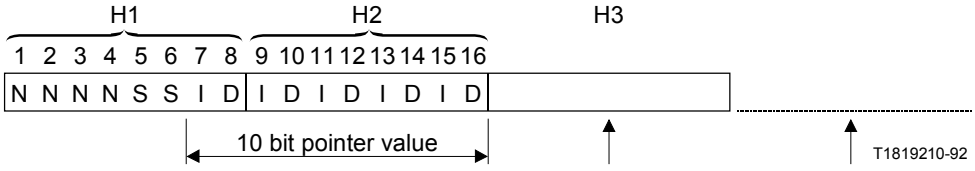
3.1.2 *AU pointer value*

The pointer contained in H1 and H2 designates the location of the byte where the VC begins. The two bytes allocated to the pointer function can be viewed as one word as shown in Figure 3-3/G.709. The last ten bits (bits 7-16) of the pointer word carry the pointer value.

As illustrated in Figure 3-3/G.709, the AU-4 pointer value is a binary number with a range of 0 to 782 which indicates the offset, in three byte increments, between the pointer and the first byte of the VC-4 (see Figure 3-1/G.709). Figure 3-3/G.709 also indicates one additional valid pointer: the concatenation indication (CI). The CI is indicated by "1001" in bits 1-4, bits 5-6 unspecified, and ten "1"s in bits 7-16. The AU-4 pointer is set to CI for AU-4 concatenation (see § 3.1.7).

As illustrated in Figure 3-3/G.709, the AU-3 pointer value is also a binary number with a range of 0 to 782. Since there are three AU-3s in the AUG, each AU-3 has its own associated H1, H2, H3 bytes. As shown in Figure 3-2/G.709, the H bytes are shown in sequence. The first H1, H2, H3 set refers to the first AU-3, the second set to the second AU-3 and so on. For the AU-3s, each pointer operates independently.

In all cases, the AU pointer bytes are not counted in the offset. For example, in an AU-4, the pointer value of 0 indicates that the VC starts in the byte location that immediately follows the last H3 byte, whereas an offset of 87 indicates that the VC starts three bytes after the K2 byte.



I Increment bit
D Decrement bit
N New data flag bit

New data flag
Enabled "1001"
Disabled "0110"

Negative justification
Invert 5 D-bits
Accept majority vote

SS values	AU/TU type
10	AU-4, AU-3, TU-3

Positive justification
Invert 5 I-bits
Accept majority vote

Pointer value (normal range) (bits 7 to 16)
AU-4, AU-3: 0 to 782 decimal
TU-3: 0 to 763 decimal

Concatenation indication (CI)
1001SS1111111111 (S bits are unspecified)

Null pointer indication (NPI)
1001SS1111100000 (S bits are unspecified)

Note 1 – NPI value applies only to TU-3 pointers.

Note 2 – The pointer is set to all "1"s when an AIS occurs.

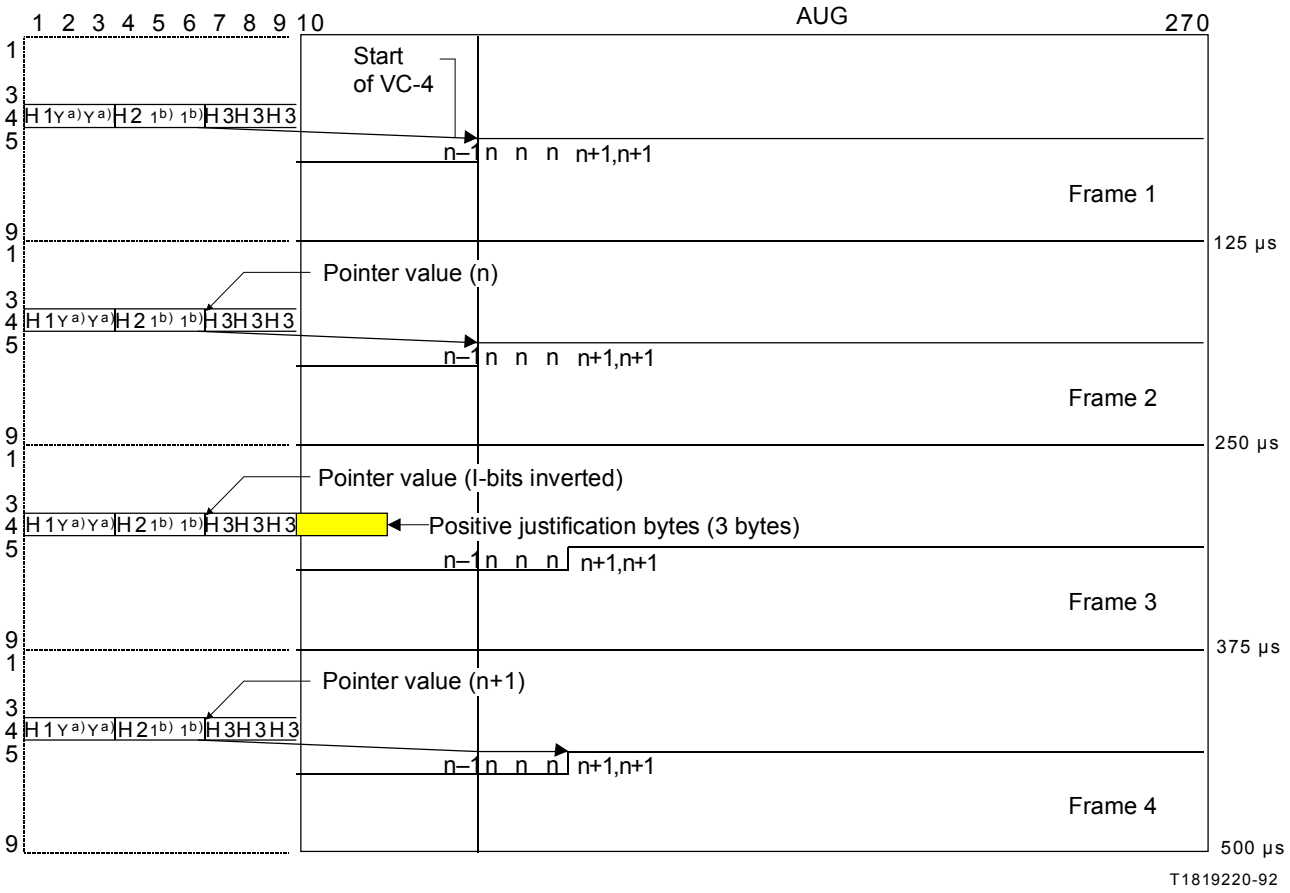
FIGURE 3-3/G.709

AU/TU-3 pointer (H1, H2, H3) coding

3.1.3 *Frequency justification*

If there is a frequency offset between the frame rate of the AUG and that of the VC, then the pointer value will be incremented or decremented as needed, accompanied by a corresponding positive or negative justification byte or bytes. Consecutive pointer operations must be separated by at least three frames (i.e. every fourth frame) in which the pointer value remains constant.

If the frame rate of the VC is too slow with respect to that of the AUG, then the alignment of the VC must periodically slip back in time and the pointer value must be incremented by one. This operation is indicated by inverting bits 7, 9, 11, 13 and 15 (I-bits) of the pointer word to allow 5-bit majority voting at the receiver. Three positive justification bytes appear immediately after the last H3 byte in the AU-4 frame containing inverted I-bits. Subsequent pointers will contain the new offset. This is illustrated in Figure 3-4/G.709.



a) Y byte: 1001SS11 (S bits are unspecified).
b) All 1s byte.

FIGURE 3-4/G.709

AU-4 pointer adjustment operation – Positive justification

For AU-3 frames, a positive justification byte appears immediately after the individual H3 byte of the AU-3 frame containing inverted I-bits. Subsequent pointers will contain the new offset. This is illustrated in Figure 3-5/G.709.

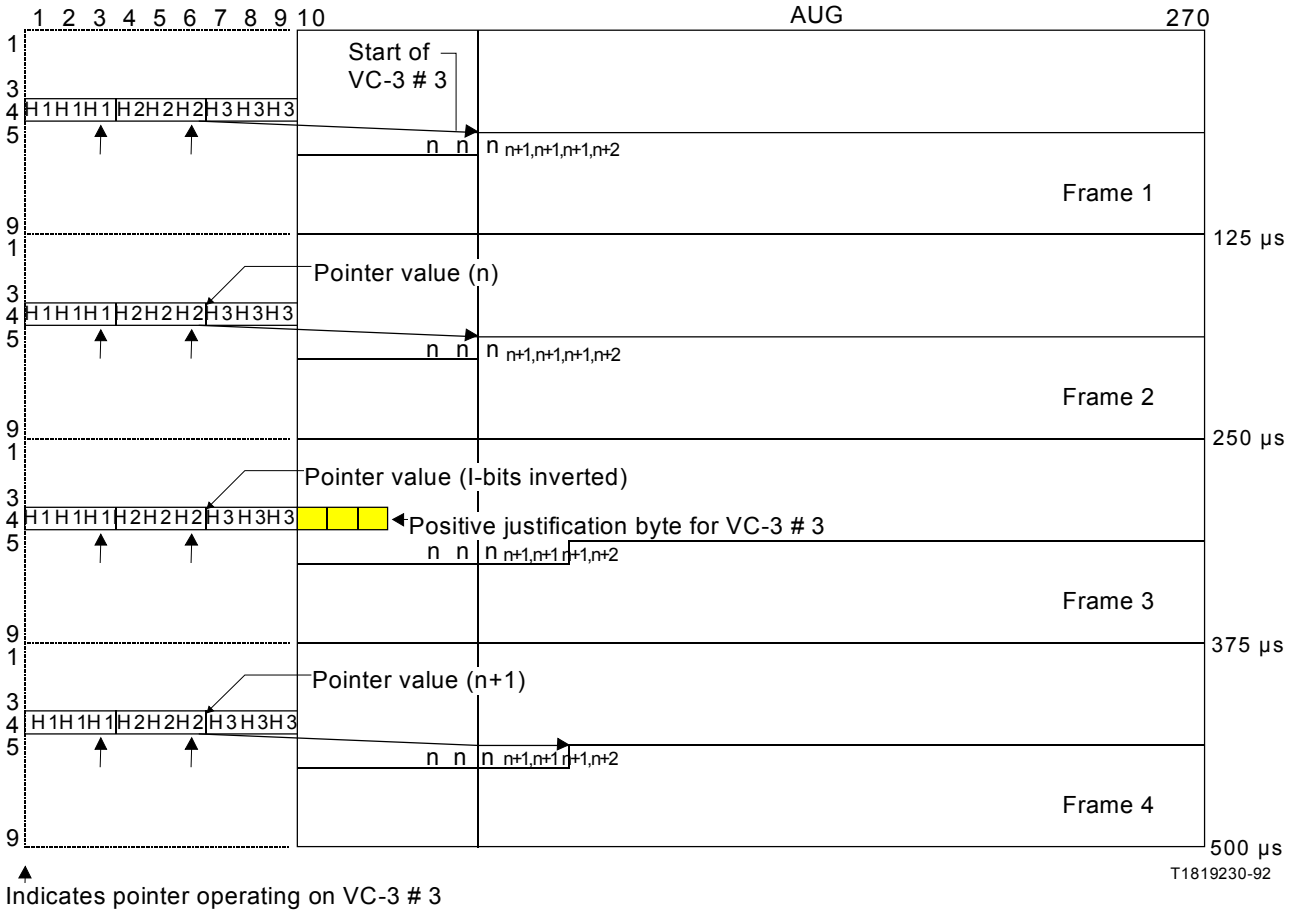
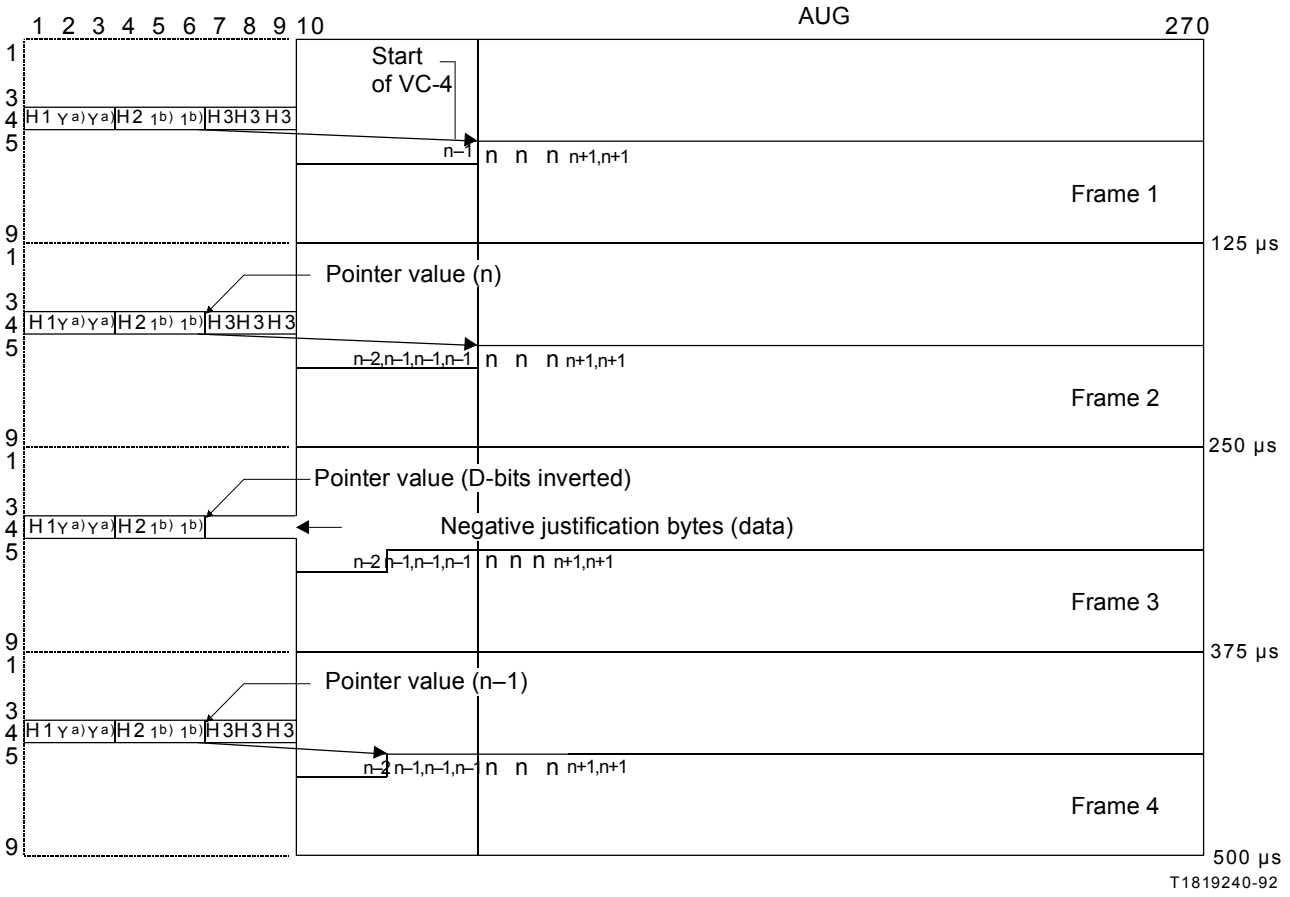


FIGURE 3-5/G.709

AU-3 pointer adjustment operation – Positive justification

If the frame rate of the VC is too fast with respect to that of the AUG, then the alignment of the VC must periodically be advanced in time and the pointer value must be decremented by one. This operation is indicated by inverting bits 8, 10, 12, 14 and 16 (D-bits) of the pointer word to allow 5-bit majority voting at the receiver. Three negative justification bytes appear in the H3 bytes in the AU-4 frame containing inverted D-bits. Subsequent pointers will contain the new offset. This is illustrated in Figure 3-6/G.709.



a) Y byte: 1001SS11 (S bits are unspecified).
b) All 1s byte.

FIGURE 3-6/G.709

AU-4 pointer adjustment operation – Negative justification

For AU-3 frames, a negative justification byte appears in the individual H3 byte of the AU-3 frame containing inverted D-bits. Subsequent pointers will contain the new offset. This is illustrated in Figure 3-7/G.709.

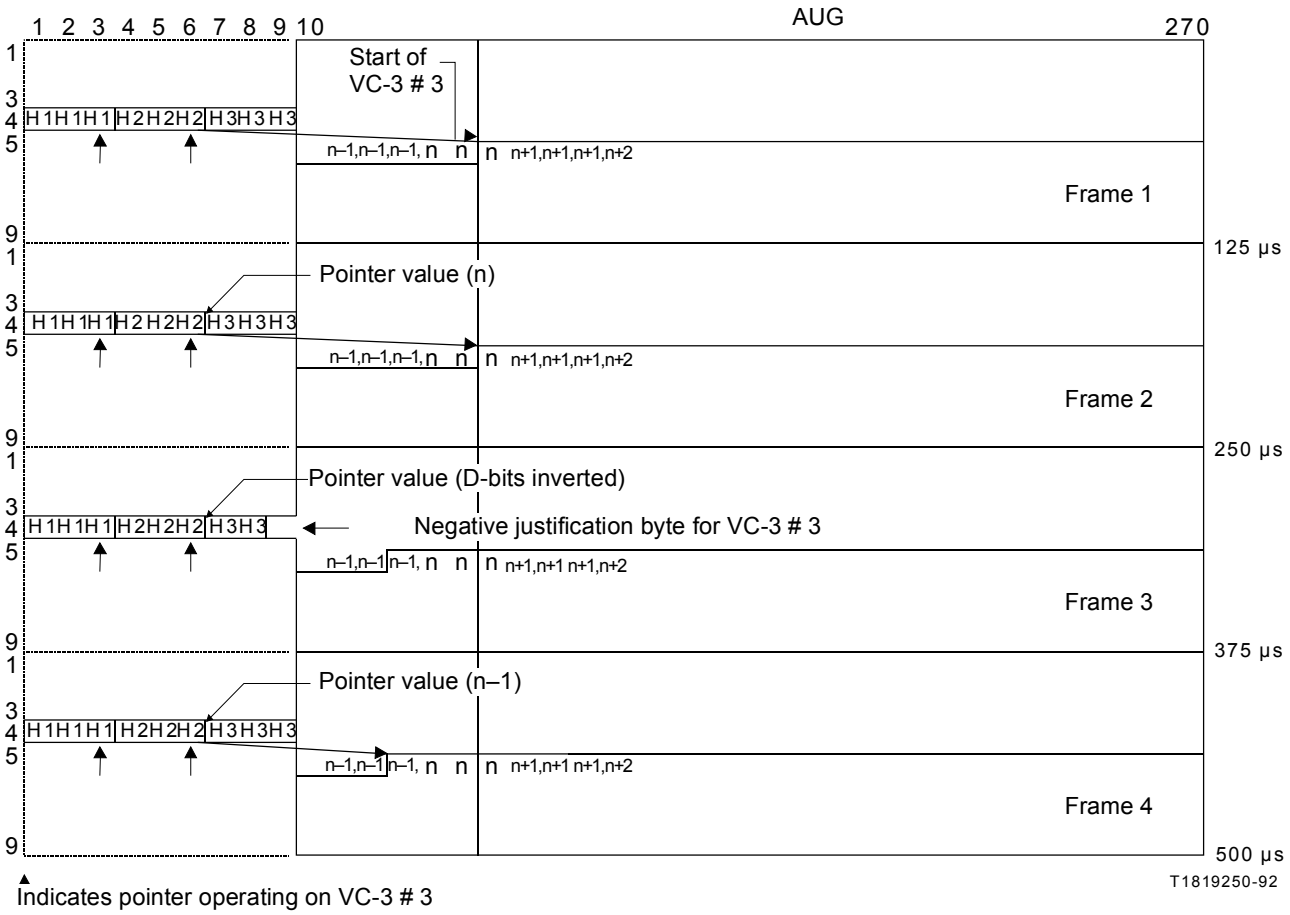


FIGURE 3-7/G.709

AU-3 pointer adjustment operation – Negative justification

3.1.4 *New data flag (NDF)*

Bits 1-4 (N-bits) of the pointer word carry an NDF which allows an arbitrary change of the pointer value if that change is due to a change in the payload.

Four bits are allocated to the flag to allow error correction. The decoding may be performed by accepting NDF enabled if at least three bits match. Normal operation is indicated by a "0110" code in the N-bits. NDF is indicated by inversion of the N-bits to "1001". The new alignment is indicated by the pointer value accompanying the NDF and takes effect at the offset indicated.

3.1.5 *Pointer generation*

The following summarizes the rules for generating the AU pointers:

1) During normal operation, the pointer locates the start of the VC within the AU frame. The NDF is set to "0110".

2) The pointer value can only be changed by operation 3, 4 or 5.

3) If a positive justification is required, the current pointer value is sent with the I-bits inverted and the subsequent positive justification opportunity is filled with dummy information. Subsequent pointers contain the previous pointer value incremented by one. No subsequent increment or decrement operation is allowed for at least three frames following this operation.

4) If a negative justification is required, the current pointer value is sent with the D-bits inverted and the subsequent negative justification opportunity is overwritten with actual data. Subsequent pointers contain the previous pointer value decremented by one. No subsequent increment or decrement operation is allowed for at least three frames following this operation.

5) If the alignment of the VC changes for any reason other than rules 3 or 4, the new pointer value shall be sent accompanied by NDF set to "1001". The NDF only appears in the first frame that contains the new values. The new location of the VC begins at the first occurrence of the offset indicated by the new pointer. No subsequent increment or decrement operation is allowed for at least three frames following this operation.

3.1.6 *Pointer interpretation*

The following summarizes the rules for interpreting the AU pointers:

1) During normal operation, the pointer locates the start of the VC within the AU frame.

2) Any variation from the current pointer value is ignored unless a consistent new value is received three times consecutively or it is preceded by one of the rules 3, 4 or 5. Any consistent new value received three times consecutively overrides (i.e. takes priority over) rules 3 or 4.

3) If the majority of the I-bits of the pointer word are inverted, a positive justification operation is indicated. Subsequent pointer values shall be incremented by one.

4) If the majority of the D-bits of the pointer word are inverted, a negative justification operation is indicated. Subsequent pointer values shall be decremented by one.

5) If the NDF is set to "1001", then the coincident pointer value shall replace the current one at the offset indicated by the new pointer value regardless of the state of the receiver.

3.1.7 *AU-4 concatenation*

AU-4s can be concatenated together to form an AU-4-Xc which can transport payloads requiring greater than one C-4 capacity. A concatenation indication, used to show that this multi C-4 payload carried in a single VC-4-Xc should be kept together, is contained in the AU-4 pointer. The first column of the VC-4-Xc is used for the POH. The remainder of the capacity is available for the payload.

The first AU-4 of an AU-4-Xc shall have a normal range of pointer values. All subsequent AU-4s within the AU-4-Xc shall have their pointer set to CI "1001" in bits 1-4, bits 5-6 unspecified, and ten "1"s in bits 7-16. The CI determines that the pointer processors shall perform the same operations as performed on the first AU-4 of the AU-4-Xc.

3.1.7.1 *Pointer generation*

The following additional pointer generation rule shall apply for AU-4 pointers. If an AU-4-Xc signal is being transmitted, a pointer is generated for the first AU-4 only. The CI is generated in place of the other AU-4 pointers in the AU-4-Xc. All operations indicated by the AU-4 pointer in the first AU-4 apply to each AU-4 in the AU-4-Xc.

3.1.7.2 *Pointer interpretation*

The following additional pointer interpretation rule shall apply for AU-4 pointers. If the pointer contains the CI then the operations performed on the AU-4 are identical to those performed on the first AU-4 within the AU-4-Xc. Any variation from the CI is ignored unless a consistent new pointer value is received three times consecutively.

3.2 *TU-3 pointer*

The TU-3 pointer provides a method of allowing flexible and dynamic alignment of VC-3 within the TU-3 frame, independent of the actual content of the VC.

3.2.1 *TU-3 pointer location*

Three individual TU-3 pointers are contained in the three separate H1, H2 and H3 bytes as shown in Figure 3-8/G.709.

When TUG-2s are multiplexed into a VC-4, the TU-3 pointer location is set to a null pointer indication (NPI). NPI is indicated by "1001" in bits 1-4, bits 5-6 unspecified, five "1"s in bits 7-11 followed by five "0"s in bits 12-16.

3.2.2 *TU-3 pointer value*

The TU-3 pointer value contained in H1 and H2 designates the location of the byte where the VC-3 begins. The two bytes allocated to the pointer function can be viewed as one word as shown in Figure 3-3/G.709. The last ten bits (bits 7 to 16) of the pointer word carry the pointer value.

The TU-3 pointer value is a binary number with a range of 0-764 which indicates the offset between the pointer and the first byte of the VC-3 as shown in Figure 3-8/G.709.

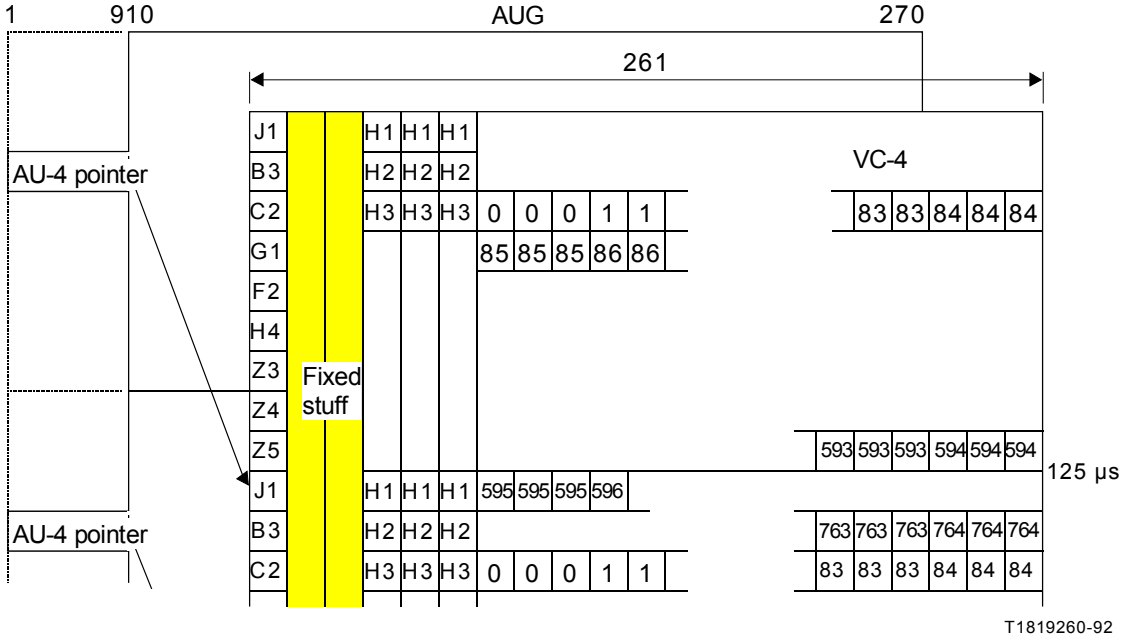


FIGURE 3-8/G.709

TU-3 pointer offset numbering

3.2.3 *Frequency justification*

If there is a frequency offset between the TU-3 frame rate and that of the VC-3, then the pointer value will be incremented or decremented as needed accompanied by a corresponding positive or negative justification byte. Consecutive pointer operations must be separated by at least three frames in which the pointer value remains constant.

If the frame rate of the VC-3 is too slow with respect to that of the TU-3 frame rate, then the alignment of the VC must periodically slip back in time and the pointer must be incremented by one. This operation is indicated by inverting bits 7, 9, 11, 13 and 15 (I-bits) of the pointer word to allow 5-bit majority voting at the receiver. A positive justification byte appears immediately after the individual H3 byte in the TU-3 frame containing inverted I-bits. Subsequent TU-3 pointers will contain the new offset.

If the frame rate of the VC-3 is too fast with respect to that of the TU-3 frame rate, then the alignment of the VC must be periodically advanced in time and the pointer must be decremented by one. This operation is indicated by inverting bits 8, 10, 12, 14 and 16 (D-bits) of the pointer word to allow 5-bit majority voting at the receiver. A negative justification byte appears in the individual H3 byte in the TU-3 frame containing inverted D-bits. Subsequent TU-3 pointers will contain the new offset.

3.2.4 *New data flag*

Bits 1-4 (N-bits) of the pointer word carry an NDF which allows an arbitrary change of the value of the pointer if that change is due to a change in the VC-3.

Four bits are allocated to the flag to allow for error correction. The decoding may be performed by accepting NDF enabled if at least three bits match. Normal operation is indicated by a "0110" code in the N-bits, NDF is indicated by inversion of the N-bits to "1001". The new alignment is indicated by the pointer value accompanying the NDF and takes effect at the indicated offset.

3.2.5 *Pointer generation*

The following summarizes the rules for generating the TU-3 pointers:

1) During normal operation, the pointer locates the start of the VC-3 within the TU-3 frame. The NDF is set to "0110".

2) The pointer value can only be changed by operation 3, 4, or 5.

3) If a positive justification is required, the current pointer value is sent with the I-bits inverted and the subsequent positive justification opportunity is filled with dummy information. Subsequent pointers contain the previous pointer value incremented by one. No subsequent increment or decrement operation is allowed for at least three frames following this operation.

4) If a negative justification is required, the current pointer value is sent with the D-bits inverted and the subsequent negative justification opportunity is overwritten with actual data. Subsequent pointers contain the previous pointer value decremented by one. No subsequent increment or decrement operation is allowed for at least three frames following this operation.

5) If the alignment of the VC changes for any reason other than rules 3 or 4, the new pointer value shall be sent accompanied by the NDF set to "1001". The NDF only appears in the first frame that contains the new value. The new VC location begins at the first occurrence of the offset indicated by the new pointer. No subsequent increment or decrement operation is allowed for at least three frames following this operation.

3.2.6 *Pointer interpretation*

The following summarizes the rules for interpreting the TU-3 pointers:

1) During normal operation the pointer locates the start of the VC-3 within the TU-3 frame.

2) Any variation from the current pointer value is ignored unless a consistent new value is received three times consecutively or it is preceded by one of rules 3, 4 or 5. Any consistent new value received three times consecutively overrides (i.e. takes priority over) rules 3 or 4.

3) If the majority of the I-bits of the pointer word are inverted, a positive justification is indicated. Subsequent pointer values shall be incremented by one.

4) If the majority of the D-bits of the pointer word are inverted, a negative justification is indicated. Subsequent pointer values shall be decremented by one.

5) If the NDF is set to "1001", then the coincident pointer value shall replace the current one at the offset indicated by the new pointer value regardless of the state of the receiver.

6) If the TU-3 pointer contains the NPI, then any variation is ignored unless a consistent new pointer value is received three times consecutively.

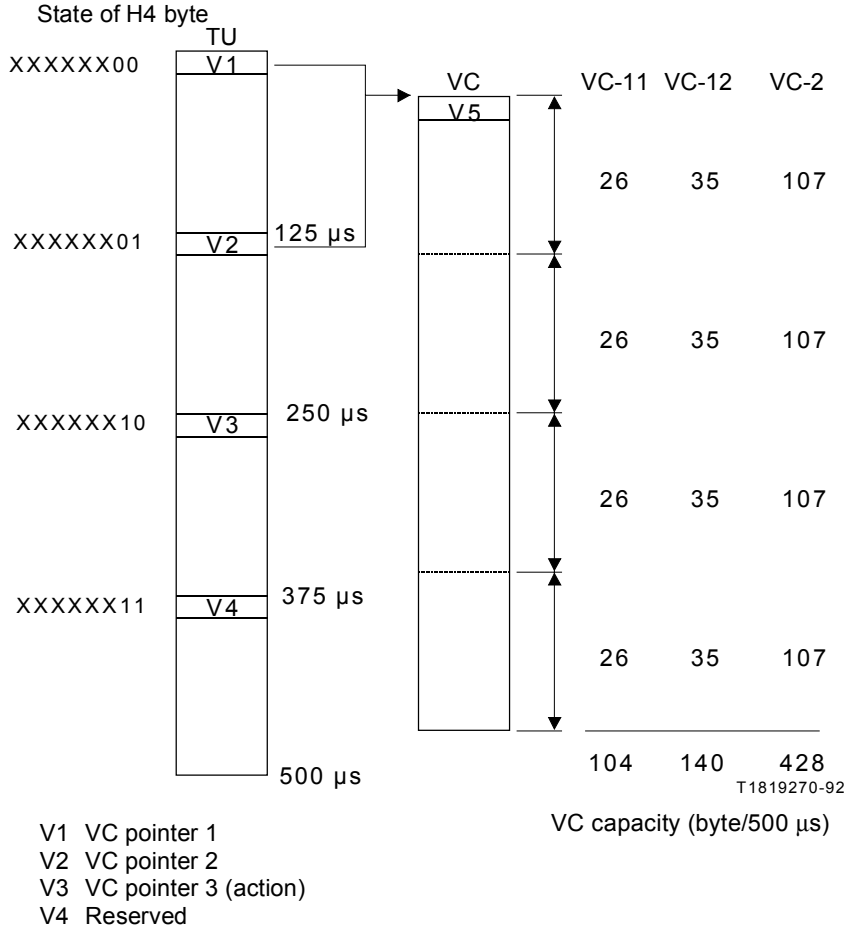
3.3 *TU-1/TU-2 pointer*

The TU-1 pointer is only used with floating mapping. Floating and locked modes of operation are described in § 5.7.

The TU-1 and TU-2 pointers provide a method of allowing flexible and dynamic alignment of the VC-1/VC-2 within the TU-1 and TU-2 multiframes, independent of the actual contents of the VC.

3.3.1 *TU-1/TU-2 pointer location*

The TU-1/TU-2 pointers are contained in the V1 and V2 bytes as illustrated in Figure 3-9/G.709.



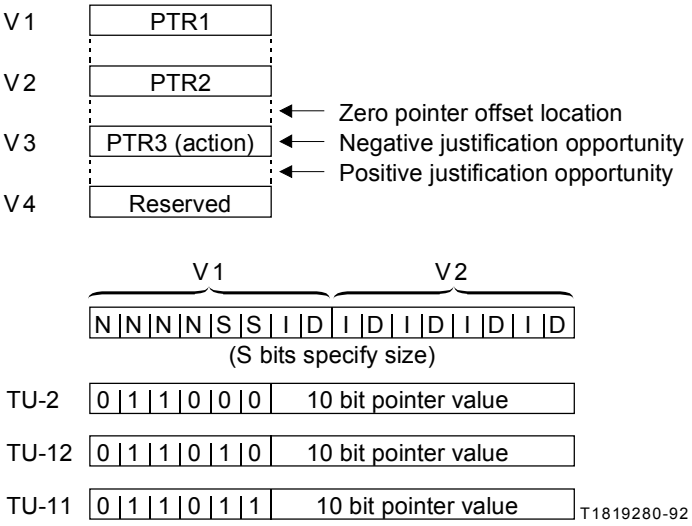
Note – V1, V2, V3 and V4 bytes are part of the TU and are terminated at the pointer processor.

FIGURE 3-9/G.709

VC mapping in multiframed TU

3.3.2 *TU-1/TU-2 pointer value*

The TU pointer word is shown in Figure 3-10/G.709. The two S bits (bits 5 and 6) indicate the TU type.



New data flag
Invert 4-N bits
Accept only exact match

Negative justification

Invert 5-D bits
Accept majority vote

Negative justification

Invert 5-I bits
Accept majority vote

Pointer value (normal range)

TU-2: 0 to 427 decimal
TU-12: 0 to 139 decimal
TU-11: 0 to 103 decimal

Concatenation indication (CI)

1001SS1111111111 (S bits are unspecified)

FIGURE 3-10/G.709

TU-1/TU-2 pointer coding

The pointer value (bits 7-16) is a binary number which indicates the offset from V2 to the first byte of the VC-1/VC-2. The range of the offset is different for each of the TU sizes as illustrated in Figure 3-11/G.709. The pointer bytes are not counted in the offset calculation.

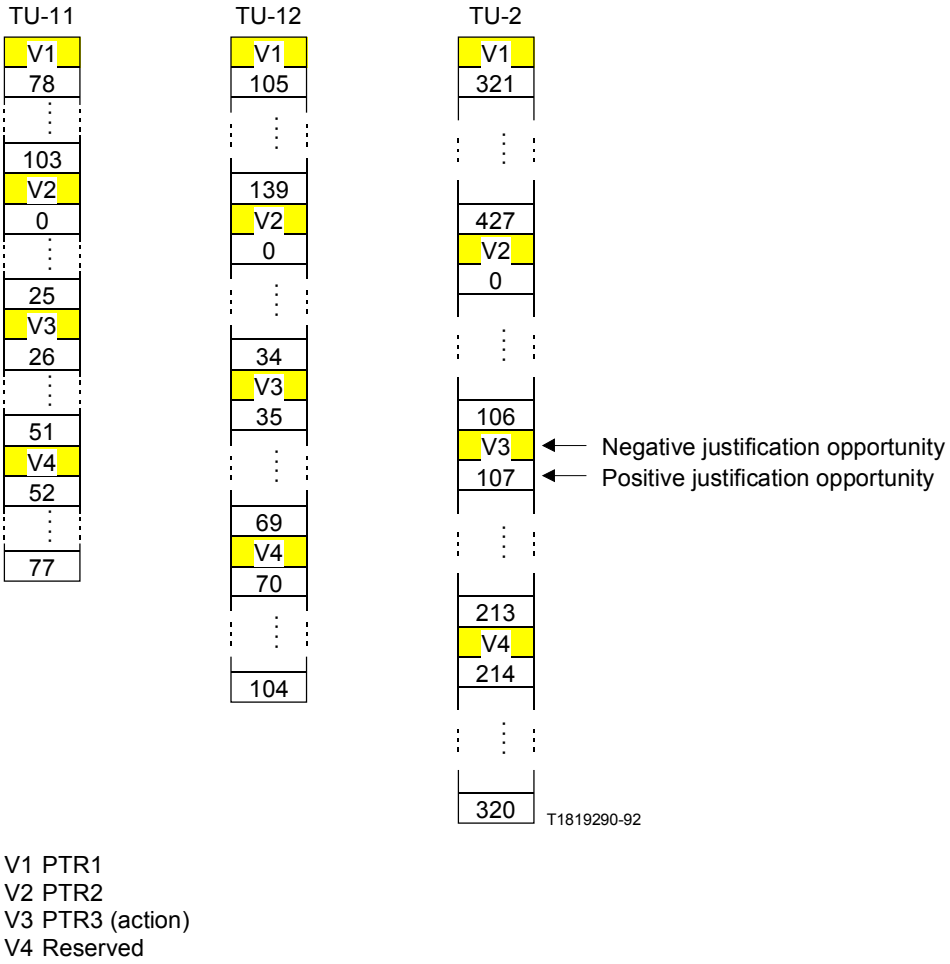


FIGURE 3-11/G.709

TU pointer offsets

3.3.3 *TU-1/TU-2 multiframe indication byte*

TU-1/TU-2 multiframe indication byte (H4) relates to the lowest level of the multiplexing structure and indicates a variety of different multiframes for use by certain payloads. Specifically it provides:

– 500 microseconds (4-frame) multiframe identifying frames containing TU-1/TU-2 pointers in the floating TU-1/TU-2 mode, and reserved byte locations in the locked TU-1 mode;

– 2 ms (16-frame) multiframe for byte synchronous channel associated signalling for 2048 kbit/s payloads in the locked TU-1 mode;

– 3 ms (24-frame) multiframe for byte synchronous channel associated signalling for 1544 kbit/s payloads in the locked TU-1 mode.

The value of the H4 byte, read from the VC-3/VC-4 POH, identifies the frame phase of the next VC-3/VC-4 payload as shown in Figure 3-12/G.709. The coding of the H4 byte is illustrated in Figures 3-13, 3-14, 3-15/G.709.

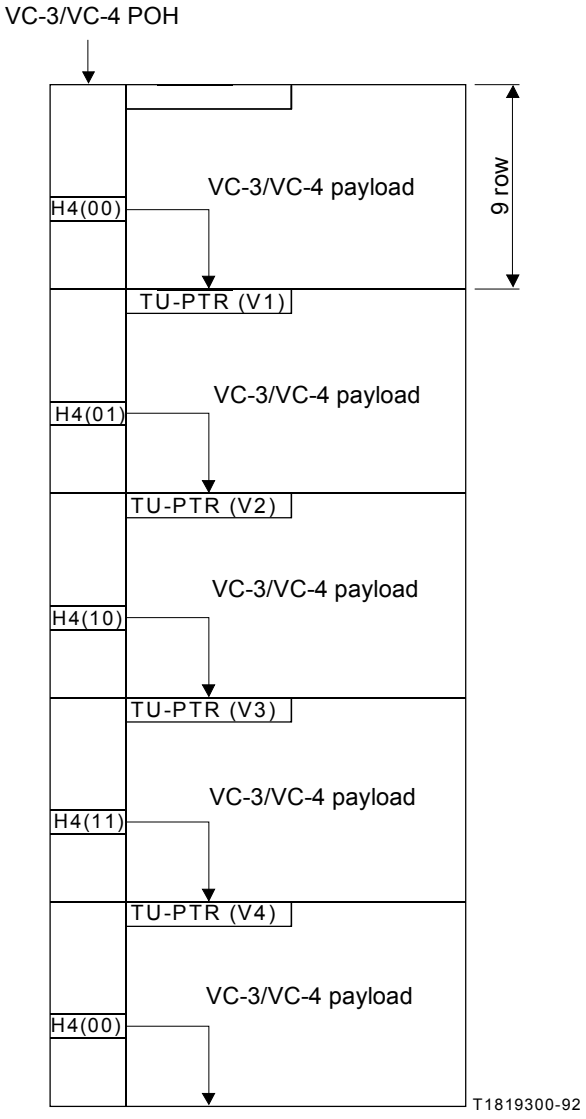


FIGURE 3-12/G.709

An example of TU-1/2 multiframe indication using H4 byte (the case of 500 ms multiframe)

For network elements that operate only in the floating TU-1/TU-2 mode, a simplified multiframe alignment byte may be used. The simplified version provides only the 500 microseconds multiframe. The 2 or 3 ms multiframe of any signalling within floating TU-1s is indicated by per-TU multiframe indicators carried within the TU-1. Figure 3-9/G.709 shows the VC-1/VC-2 mapping in the multiframed TU-1/TU-2.

A converter from locked to floating TUs is permitted to pass H4 through transparently. A converter from floating to locked TUs must recover and align the multiframes from all of the floating TUs and so can transmit any convenient full multiframe on the locked TU side.

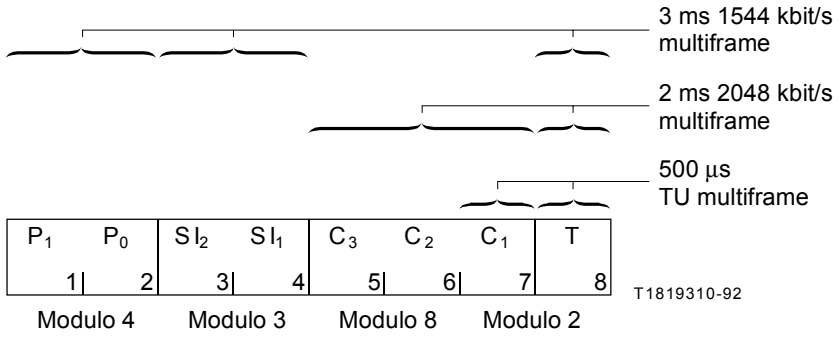


FIGURE 3-13/G.709

TU multiframe indicator byte (H4)

Bit				Frame	Time
1 2	3 4	5 6 7	8		
0 0	0 0	0 0 0	0	0	0
0 0	0 0	0 0 0	1	1	
0 0	0 1	0 0 1	0	2	
0 0	0 1	0 0 1	1	3	500 ms TU multiframe
0 0	1 0	0 1 0	0	4	
0 0	1 0	0 1 0	1	5	
0 1	0 0	0 1 1	0	6	
0 1	0 0	0 1 1	1	7	
0 1	0 1	1 0 0	0	8	
0 1	0 1	1 0 0	1	9	
0 1	1 0	1 0 1	0	10	
0 1	1 0	1 0 1	1	11	
1 0	0 0	1 1 0	0	12	
1 0	0 0	1 1 0	1	13	
1 0	0 1	1 1 1	0	14	
1 0	0 1	1 1 1	1	15	2 ms 2048 kbit/s signalling cycle
1 0	1 0	0 0 0	0	16	
1 0	1 0	0 0 0	1	17	
1 1	0 0	0 0 1	0	18	
1 1	0 0	0 0 1	1	19	
1 1	0 1	0 1 0	0	20	
1 1	0 1	0 1 0	1	21	
1 1	1 0	0 1 1	0	22	
1 1	1 0	0 1 1	1	23	3 ms 1544 kbit/s signalling cycle
0 0	0 0	1 0 0	0	24	
0 0	0 0	1 0 0	1	25	
0 0	0 1	1 0 1	0	26	
0 0	0 1	1 0 1	1	27	
0 0	1 0	1 1 0	0	28	
0 0	1 0	1 1 0	1	29	
0 1	0 0	1 1 1	0	30	
0 1	0 0	1 1 1	1	31	
0 1	0 1	0 0 0	0	32	
0 1	0 1	0 0 0	1	33	
0 1	1 0	0 0 1	0	34	
0 1	1 0	0 0 1	1	35	
1 0	0 0	0 1 0	0	36	
1 0	0 0	0 1 0	1	37	
1 0	0 1	0 1 1	0	38	
1 0	0 1	0 1 1	1	39	
1 0	1 0	1 0 0	0	40	
1 0	1 0	1 0 0	1	41	
1 1	0 0	1 0 1	0	42	
1 1	0 0	1 0 1	1	43	
1 1	0 1	1 1 0	0	44	6 ms = Cycle repeat time
1 1	0 1	1 1 0	1	45	
1 1	1 0	1 1 1	0	46	
1 1	1 0	1 1 1	1	47	

Note – Full H4 coding sequence is mandatory in locked TU mode and optional in floating TU mode.

FIGURE 3-14/G.709

TU multiframe indicator byte (H4) full coding sequence

Bit				Frame	Time
1 2	3 4	5 6 7	8		
1 1	1 1	1 1 0	0	0	0
1 1	1 1	1 1 0	1	1	
1 1	1 1	1 1 1	0	2	
1 1	1 1	1 1 1	1	3	500 ms TU multiframe

Note 1 – Reduced H4 coding sequence is optional in floating TU mode.

Note 2 – Use of reduced mode can be detected by bits 3 and 4 = "1".

FIGURE 3-15/G.709

TU multiframe indicator byte (H4) reduced coding sequence

3.3.4 *TU-1/TU-2 frequency justification*

The TU-1/TU-2 pointer is used to frequency justify the VC-1/VC-2 exactly in the same way that the TU-3 pointer is used to frequency justify the VC-3. A positive justification opportunity immediately follows the V3 byte. Additionally, V3 serves as the negative justification opportunity such that when the opportunity is taken, V3 is overwritten by data. This is also shown in Figure 3-11/G.709. The indication of whether or not a justification opportunity has been taken is provided by the I- and D-bits of the pointer in the current TU multiframe. The value contained in V3 when not being used for a negative justification is not defined. The receiver is required to ignore the value contained in V3 whenever it is not used for negative justification.

3.3.5 *TU-1/TU-2 sizes*

Bits 5 and 6 of TU-1/TU-2 pointer indicate the size of the TU. Three sizes are currently provided:

Size (binary)	Designation	TU pointer range (in 500 µs)
00	TU-2	0-427
10	TU-12	0-139
11	TU-11	0-103

Note that this technique is only used at the TU-1/TU-2 levels.

3.3.6 *New data flag (NDF)*

Bits 1-4 (N-bits) of the pointer word carry an NDF. It is the mechanism which allows an arbitrary change of the value of a pointer, and possibly also the size of the TU, if that change is due to a change in the payload. If the change includes a change in size then, implicitly, there must be a simultaneous new data transition in all of the TUs in the TUG-2.

As with the TU-3 pointer NDF, the normal value is "0110" (transmitted), and the value "1001" (received exactly) indicates a new alignment for the VC, and possibly new size. If a new size is indicated, then all TU pointers in the TUG-2 must simultaneously indicate NDF with the same new size. The new alignment, and possibly size, is indicated by the pointer value and size value accompanying the NDF and takes effect at the offset indicated.

3.3.7 *TU concatenation*

TU-2s may be concatenated to form a TU-2-mc (concatenated m × TU-2s) when a payload is required of more than a C-2. This forms a multi C-2 payload which is carried in a single VC-2-mc (concatenated m × VC-2). The rules by which TU-2s can be concatenated are separated into three categories:

– concatenation of contiguous TU-2s in the higher order VC-3;

– sequential concatenation of TU-2s in the higher order VC-4;

– virtual concatenation of TU-2s in the higher order VC-4.

The details and extensibility of the concept of virtual concatenation of TUs is for further study.

3.3.7.1 *Concatenation of contiguous TU-2s in the higher order VC-3*

TU-2s which are contiguous in time in the higher order VC-3 in which they are carried are concatenated together by the use of the concatenation indication (CI-"1001" in bits 1-4, bits 5-6 unspecified, and all ones in bits 7-16 of the TU-2 pointer). The CI determines that the TU-2 pointer processor performs all the operations as indicated by the first TU-2 pointer in the TU-2-mc.

With this type of concatenation the VC-2-mc contains a single VC POH which appears in VC-2 #1 of the VC-2-mc.

3.3.7.2 *Sequential concatenation of TU-2s in the higher order VC-4*

This type of concatenation which allows the simultaneous transport of TU-2-mcs and TU-3s in the same VC-4 is under study.

3.3.7.3 *Virtual concatenation of TU-2s in the higher order VC-4*

This method of concatenation allows for the transport of a single VC-2-mc in m × TU-2 without the use of CI in the pointer bytes. The method only requires the path termination equipment to provide concatenation functionality.

Virtual concatenation requires the concatenated TU-signals at the origin of the path to be launched with the same pointer value. The so formed TUs shall at each interface be kept in a single higher order VC-4.

When the higher order VC-4 is terminated, the restrictions that apply in passing the concatenated TUs from one interface to another is that all of the concatenated TUs are connected to a single higher order VC-4 and that the time sequencing of the concatenated TUs is not altered.

Differences in delay of the individual concatenated VC-signals may occur due to pointer processing at intermediate equipment. The maximum difference in pointer value within a concatenated group at any interface is for further study. At the path termination the VC-2-mc can be reconstructed by using the pointer values for alignment.

Each concatenated VC-2 signal will carry its own POH. At the VC-2-mc path termination, the individual BIP2s are aggregated to give a single BIP error monitor.

The details and the extensibility of the virtual concatenation method within the VC-4 are under study.

Note – With virtual concatenation, the available capacity of the VC-2-mc is lower than with contiguous concatenation due to the fact that with the virtual concatenation each VC-2 carries its own POH contrary to contiguous concatenation where only the VC-2 #1 of the VC-2-mc carries its own POH. In order to be able to interconnect VC-2-mcs using different types of concatenation, the mapping of signals in VC-2-mcs should be based on the lower available capacity, namely the capacity of VC-2-mc based on virtual concatenation. Stuffing bytes should be inserted in the VC-2-mc payload based upon contiguous concatenation to accommodate the difference in capacity.

3.3.8 *TU pointer generation and interpretation*

The rules for generating and interpreting the TU-1/TU-2 pointer for the VC-1/VC-2 are an extension to the rules provided in §§ 3.2.5 and 3.2.6 for the TU-3 pointer with the following modifications:

1) The term TU-3 is replaced with TU-1/TU-2 and the term VC-3 is replaced with VC-1/VC-2.

2) Additional pointer generation rule 6: if the size of the TU within a TUG-2 is to change, then an NDF, as described in rule 5, is to be sent to all TUs of the new size in the group simultaneously.

3) Additional pointer interpretation rule 7: if an NDF of "1001" and an arbitrary new size of TU are received simultaneously in all of the TUs within a TUG-2, then the coincident pointers and sizes shall replace the current ones immediately.

4) If the TU-2 pointer contains the CI, then any variation is ignored unless a consistent new pointer value is received three times consecutively.

4 Path overhead descriptions

4.1 *VC-3/VC-4 POH*

The VC-3 POH is located in the first column of the 9-row by 85-column VC-3 structure.

The VC-4 POH is located in the first column of the 9-row by 261-column VC-4 structure.

The VC-3/VC-4 POH will be assigned to and remain with the payload until the payload is demapped and will be used for functions that are necessary in transporting all VC-3/VC-4s. Note that this does not preclude the allocation of other overheads in specific accommodations (such as justification control for accommodating asynchronous 44 736 kbit/s signals). That type of overhead is payload specific whereas the POH defined in this section is payload independent.

The VC-4/VC-3 POH consists of nine bytes denoted J1, B3, C2, G1, F2, H4, Z3-Z5 (see Figures 2-2/G.709 and 2-3/G.709).

4.1.1 *VC-3/VC-4 path trace (J1)*

This is the first byte in the VC: its location is indicated by the associated AU or TU pointer. This byte is used to repetitively transmit a 64-byte fixed length string so that a path receiving terminal can verify its continued connection to the intended transmitter. The content of the message is not constrained by this standard since it is assumed to be user programmable at both transmit and receive ends.

4.1.2 *Path BIP-8 (B3)*

One byte is allocated in each VC-3 or VC-4 for a path error monitoring function. This function shall be a BIP-8 code using even parity. The path BIP-8 is calculated over all bits of the previous VC-3 or VC-4 before scrambling. The computed BIP-8 is placed in the B3 byte of the current VC-3 or VC-4 before scrambling.

4.1.3 *Signal label (C2)*

One byte is allocated to indicate the composition of the VC-3/VC-4. Of the 256 possible binary values, two are defined here and the remaining 254 values are reserved to be defined as required in specific VC-3/VC-4 mappings:

– Value 0 indicates "VC-3/VC-4 path unequipped". This value shall be originated if the section is complete but there is no VC-3/VC-4 path originating equipment.

– Value 1 indicates "VC-3/VC-4 path equipped – non specific payloads". This value can be used for all payloads that need no further differentiation, or that achieve differentiation by other means such as messages from an operations system.

Note that any value received, other than value 0 constitutes an "equipped" condition.

4.1.4 *Path status (G1)*

One byte is allocated to convey back to a VC-3/VC-4 path originator the path terminating status and performance. This feature permits the status and performance of the complete duplex path to be monitored at either end, or at any point along that path. As illustrated in Figure 4-1/G.709, bits 1 through 4 convey the count of interleaved-bit blocks that have been detected in error by the path BIP-8 code (B3). This count has nine legal values, namely 0-8 errors. The remaining seven possible values represented by these four bits can only result from some unrelated condition and shall be interpreted as zero errors. VC-3/VC-4 path remote alarm indication is sent back by VC-3/VC-4 assembler whenever the VC-3/VC-4 assembler is not receiving a valid signal. The VC-3/VC-4 path FERF is bit 5, which is set to a "1" to indicate VC-3/VC-4 path FERF, and is otherwise set to zero. The specific received conditions under which VC-3/VC-4 path FERF is initiated are path AIS, signal failure conditions or path trace mismatch. Bits 6, 7 and 8 are not used.

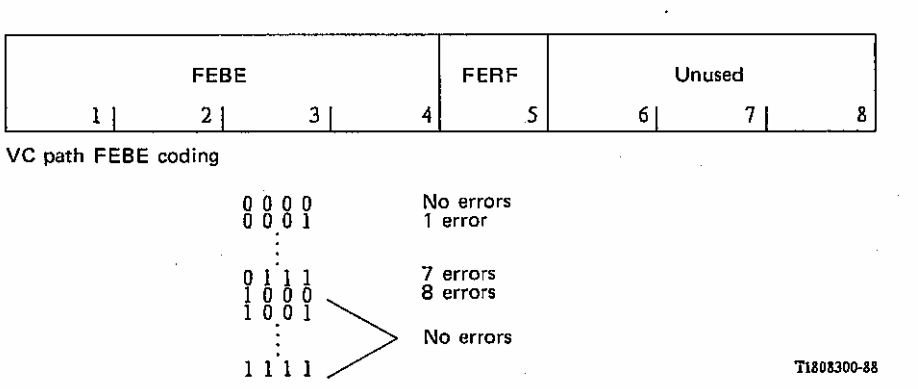


FIGURE 4-1/G.709

VC-3/VC-4 path status (G1)

4.1.5 *Path user channel (F2)*

One byte is allocated for user communication purposes between path elements.

4.1.6 *Position indicator (H4)*

This byte provides a generalized position indicator for payloads and can be payload specific (e.g. H4 can be used as a position multiframe indicator for VC-1/VC-2 or as a position cell start indicator for an ATM payload).

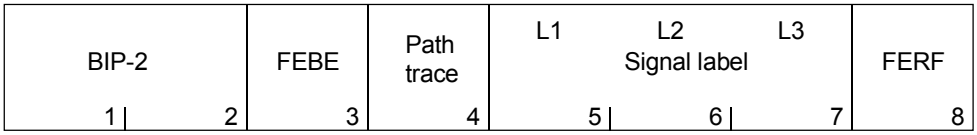
4.1.7 *Spare (Z3 to Z5)*

Three bytes are allocated for future, as yet undefined purposes. These bytes have no defined value. The receiver is required to ignore the value contained in these bytes.

4.2 *VC-1/VC-2 POH*

The first byte in the VC-1/VC-2 pointed to by the TU-1/TU-2 pointer is the VC-1/VC-2 path overhead byte. This byte is designated as V5.

This byte provides the functions of error checking, signal label, and path status of the VC-1/VC-2 paths. The bit assignments of the VC-1/VC-2 POH are specified in the following paragraphs and are illustrated in Figure 4-2/G.709.



VC path signal label coding

L1	L2	L3	Meaning
0	0	0	Unequipped
0	0	1	Equipped – Non-specific
0	1	0	Asynchronous, floating
0	1	1	Bit synchronous, floating
1	0	0	Byte synchronous, floating
1	0	1	}
1	1	0	} Equipped – Unused
1	1	1	}

VC path FEBE coding

T1819740-93

0 No errors
1 One or more errors

Note – VC path overhead is defined only in VC # 1 of VC-21-mc.

FIGURE 4-2/G.709

VC-1/VC-2 path overhead (V5)

V5 is used only in floating mode VC-1/VC-2s and is designated as an R byte in locked mode VC-1/VC-2s. Floating mode and locked mode operation are described in § 5.7.

Bits 1 and 2 are used for error performance monitoring. A bit interleaved parity (BIP) scheme is specified. Bit 1 is set such that parity of all odd number bits (1, 3, 5 and 7) in all bytes in the previous VC-1/VC-2 is even and bit 2 is set similarly for the even number bits (2, 4, 6 and 8).

Note that the calculation of the BIP-2 includes the VC-1/VC-2 POH bytes but excludes bytes V1, V2, V3 (except when used for negative justification) and V4.

Bit 3 is a VC-1/VC-2 path far-end-block-error (FEBE) indication that is set to one and sent back towards a VC-1/VC-2 path originator if one or more errors were detected by the BIP-2, and is otherwise set to zero.

Bit 4 is provisionally reserved for a path validation and trace function. The protocol to be used on this channel requires further study.

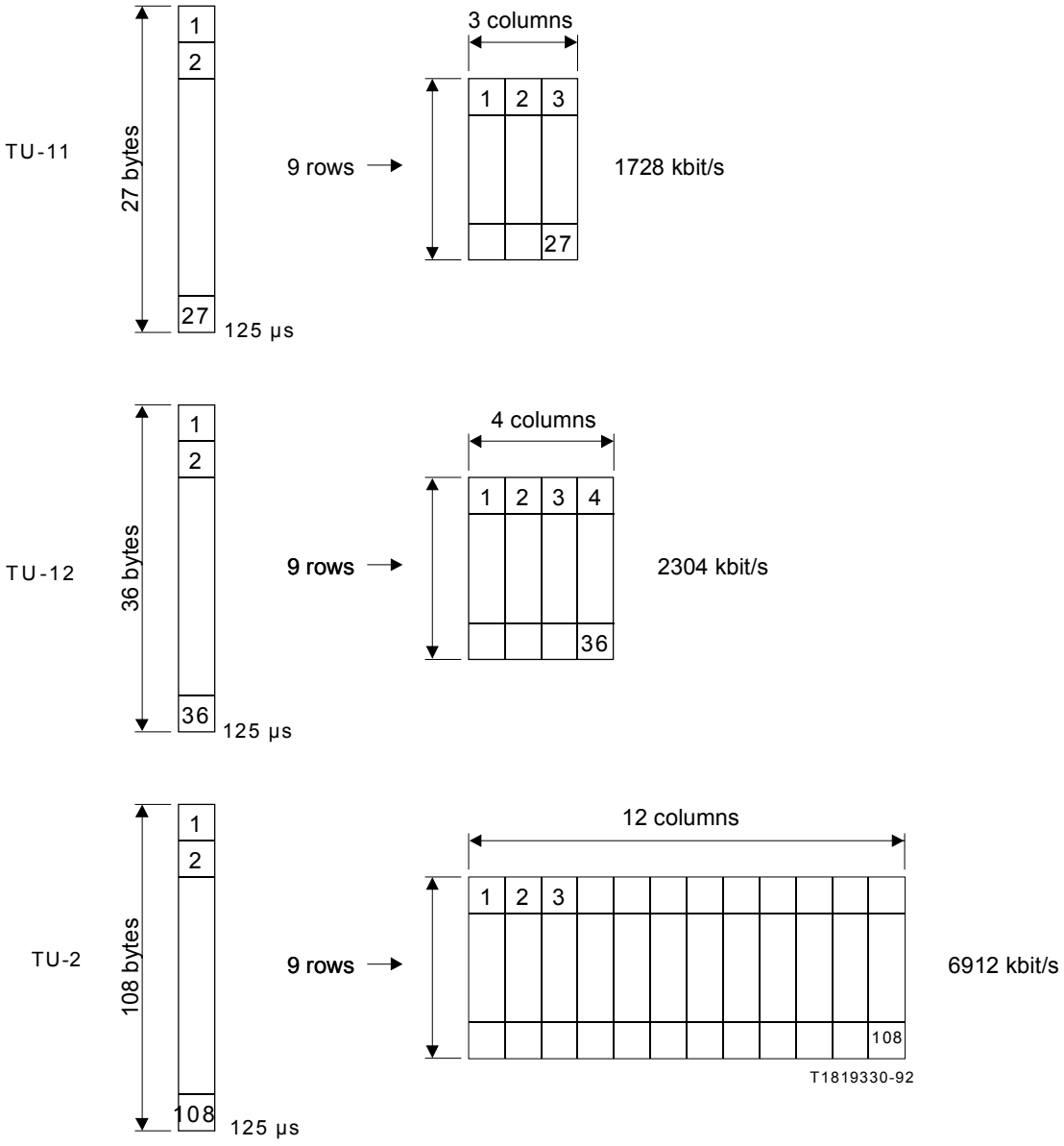
Bits 5 through 7 provide a VC-1/VC-2 signal label. Eight binary values are possible in these three bits. Value 000 indicates “VC-1/VC-2 path unequipped”, and value 001 indicates “VC-1/VC-2 path equipped – non specific payload”. Three values are defined to indicate specific mappings as shown in Figure 4-2/G.709. The use of these three values is optional although they are not to be used for any other purpose. The remaining three values are reserved to be defined in other specific VC-1/VC-2 mappings. Any value received, other than 000, indicates an equipped VC-1/VC-2 path.

Bit 8 is a VC-1/VC-2 path FERF. This bit is set to a one if either a TU-1/TU-2 path AIS or a signal failure condition is being received, otherwise it is set to zero. The VC-1/VC-2 path FERF is sent back by the VC-1/VC-2 assembler.

5 Mapping of tributaries into VCs

Accommodation of asynchronous and synchronous tributaries presently defined in Recommendation G.702 shall be possible. At the TU-1/TU-2 level, asynchronous accommodation utilizes only the floating mode, whereas synchronous accommodation utilizes both the locked and the floating mode.

Figure 5-1/G.709 shows TU-1 and TU-2 sizes and formats.



Note – The TU pointer bytes (V1-V4) are located in byte 1 (using a four frame multiframe).

FIGURE 5-1/G.709

TU-1 and TU-2 sizes and formats

5.1 *Mapping of tributaries into VC-4*

5.1.1 *Asynchronous mapping of 139 264 kbit/s*

One 139 264 kbit/s signal can be mapped into a VC-4 of an STM-1 frame as shown in Figures 5-2/G.709 and 5-3/G.709.

The VC-4 consists of nine bytes (1 column) POH plus a 9-row by 260-column payload structure as shown in Figure 5-2/G.709.

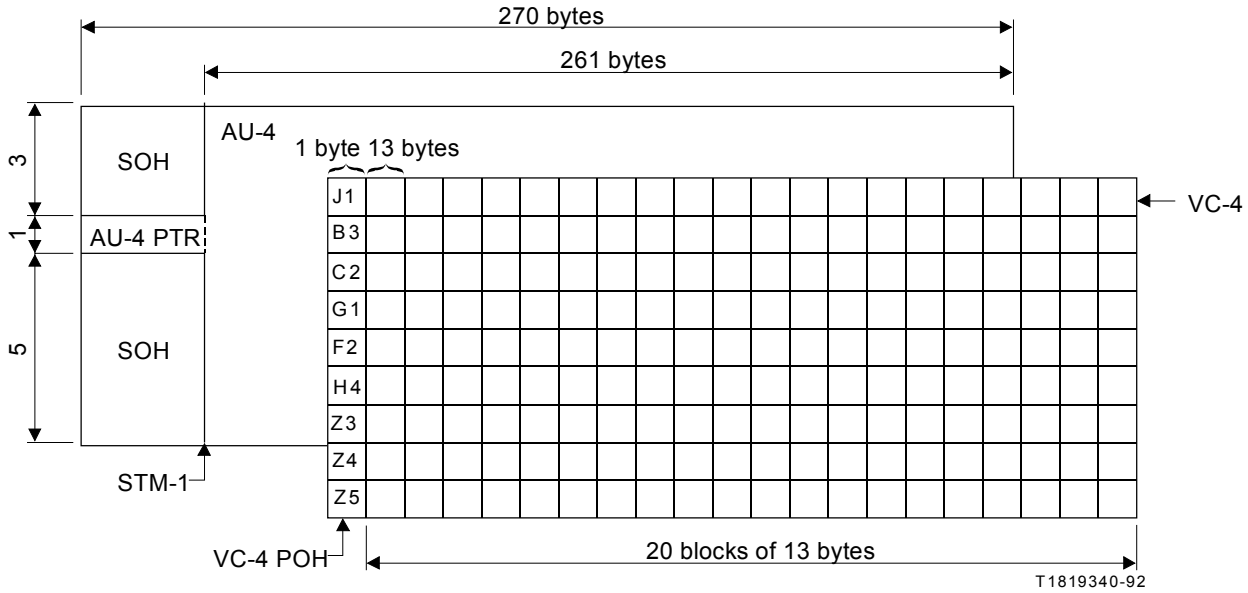


FIGURE 5-2/G.709

Mapping of VC-4 into STM-1 and block structure of VC-4 for asynchronous mapping of 139 264 kbit/s

This payload can be used to carry one 139 264 kbit/s signal:

- Each of the 9 rows is partitioned into 20 blocks, consisting of 13 bytes each (see Figure 5-2/G.709).
- In each row, one justification opportunity bit (S) and five justification control bits (C) are provided (see Figure 5-3/G.709).
- The first byte of each block consists of either:
  - eight information bits (I) (byte W); or
  - eight fixed stuff bits (R) (byte Y); or
  - one justification control bit (C) plus five fixed stuff bits (R) plus two overhead bits (O) (byte X); or
  - six information bits (I) plus one justification opportunity bit (S) plus one fixed stuff bit (R) (byte Z).
- The last 12 bytes of each block consist of information bits (I).

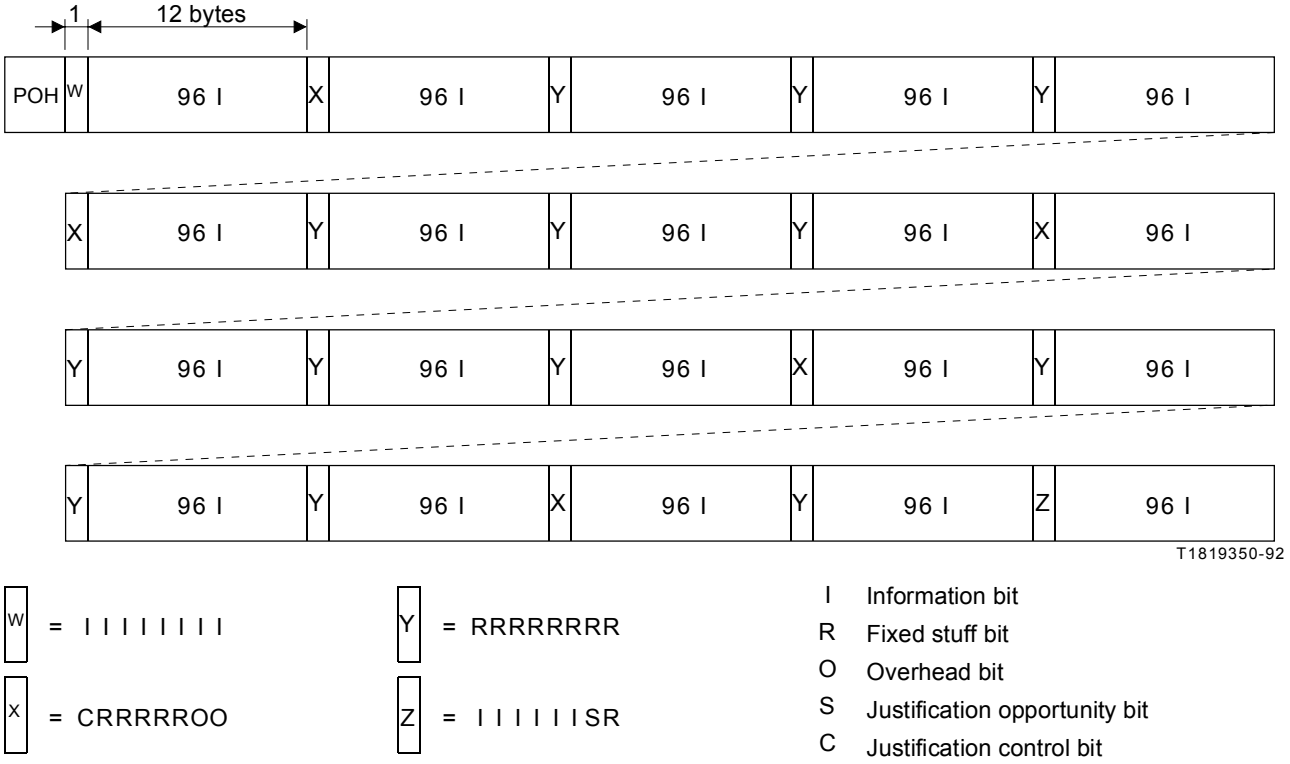
The sequence of all these bytes is shown in Figure 5-3/G.709.

The overhead bits (O) are reserved for further overhead communication purposes.

The set of five justification control bits (C) in every row is used to control the corresponding justification opportunity bit (S). CCCCC = 00000 indicates that the S-bit is an information bit, whereas CCCCC = 11111 indicates that the S-bit is a justification bit.

Majority vote should be used to make the a justification decision in the desynchronizer for protection against single and double bit errors in the C-bits.

The value contained in the S-bit when used as a justification bit is not defined. The receiver is required to ignore the value contained in this bit whenever it is used as a justification bit.



Note – This figure shows one row of the nine-row VC-4 container structure.

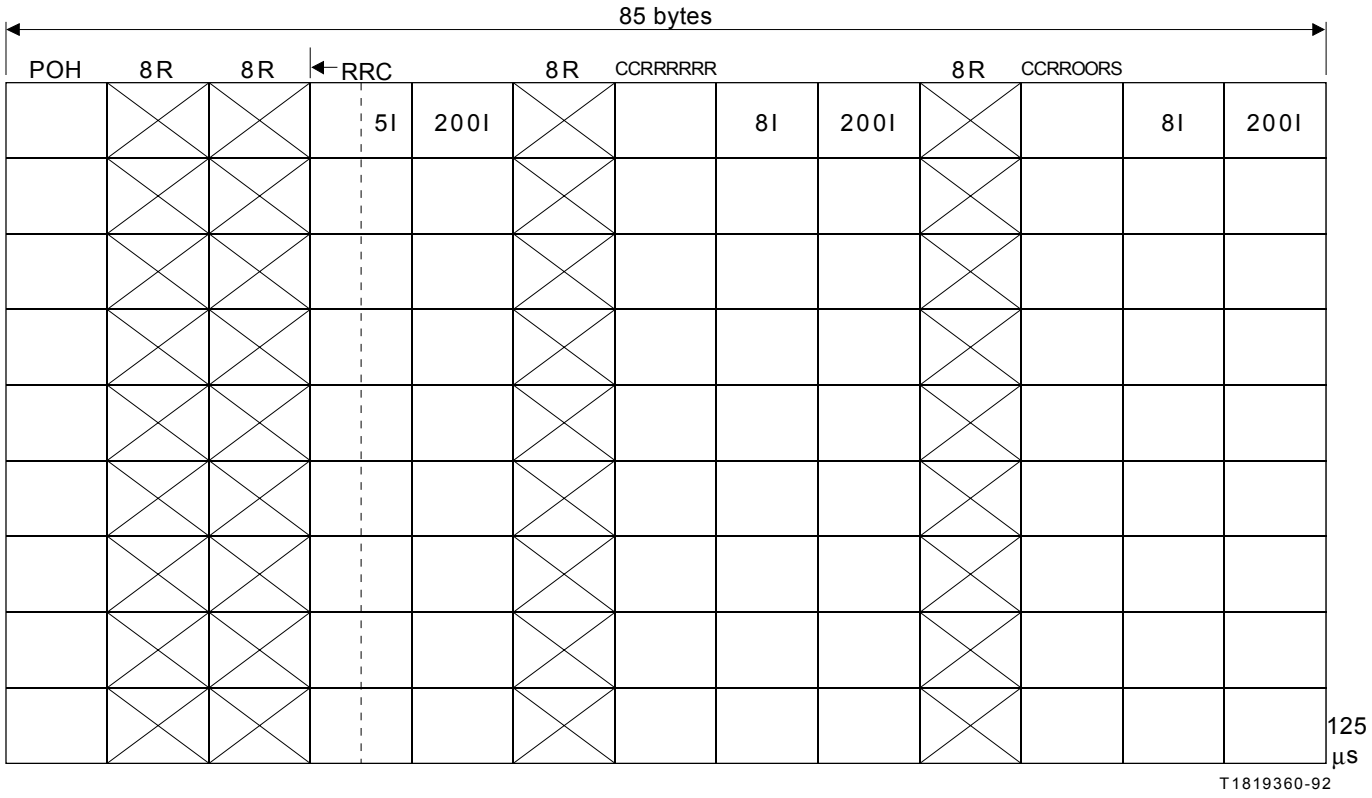
FIGURE 5-3/G.709

Asynchronous mapping of 139 264 kbit/s tributary into VC-4

5.2 *Mapping of tributaries into VC-3*

5.2.1 *Asynchronous mapping of 44 736 kbit/s*

One 44 736 kbit/s signal can be mapped into a VC-3 as shown in Figure 5-4/G.709.



R Information bit
C Fixed stuff bit
S Overhead bit
I Justification opportunity bit
O Justification control bit

FIGURE 5-4/G.709

Asynchronous mapping of 44 736 kbit/s tributary into VC-32

The VC-3 consists of nine subframes every 125 microseconds. Each subframe consists of one byte of VC-3 POH, 621 data bits, a set of five justification control bits, one justification opportunity bit and two overhead communication channel bits.

The remaining bits are fixed stuff (R) bits. The O bits are reserved for future overhead communication purposes.

The set of five justification control bits is used to control the justification opportunity (S) bit. CCCCC = 00000 indicates that the S-bit is a data bit, whereas CCCCC = 11111 indicates that the S-bit is a justification bit. Majority vote should be used to make the justification decision in the desynchronizer for protection against single and double bit errors in the C-bits.

The value contained in the S-bit when used as justification bits is not defined. The receiver is required to ignore the value contained in this bit whenever it is used as a justification bit.

5.2.2 *Asynchronous mapping of 34 368 kbit/s*

One 34 368 kbit/s signal can be mapped into a VC-3 as shown in Figure 5-5/G.709.

In addition to the VC-3 POH, the VC-3 consists of a payload of 9×84 bytes every 125 microseconds. This payload is divided into three subframes, each subframe consisting of:

– 1431 information bits (I);

– two sets of five justification control bits (C_1, C_2);

– two justification opportunity bits (S_1, S_2);

– 573 fixed stuff bits (R).

Two sets of five justification control bits C_1 and C_2 are used to control the two justification opportunity bits S_1 and S_2 respectively.

$C_1C_1C_1C_1C_1 = 00000$ indicates that S_1 is a data bit while $C_1C_1C_1C_1C_1 = 11111$ indicates that S_1 is a justification bit. C2-bits control S_2 in the same way. Majority vote should be used to make the justification decision in the desynchronizer for protection against single and double bit errors in the C-bits.

The value contained in S_1 and S_2 when they are justification bits is not defined. The receiver is required to ignore the value contained in these bits whenever they are used as justification bits.

Note – The same mapping could be used for bit or byte synchronous 34 368 kbit/s. In these cases, S_1 bit should be a fixed stuff and S_2 bit an information bit. By setting the C_1 bits to 1 and the C_2 bits to 0, a common desynchronizer could be used for both asynchronous and synchronous 34 368 kbit/s mappings.

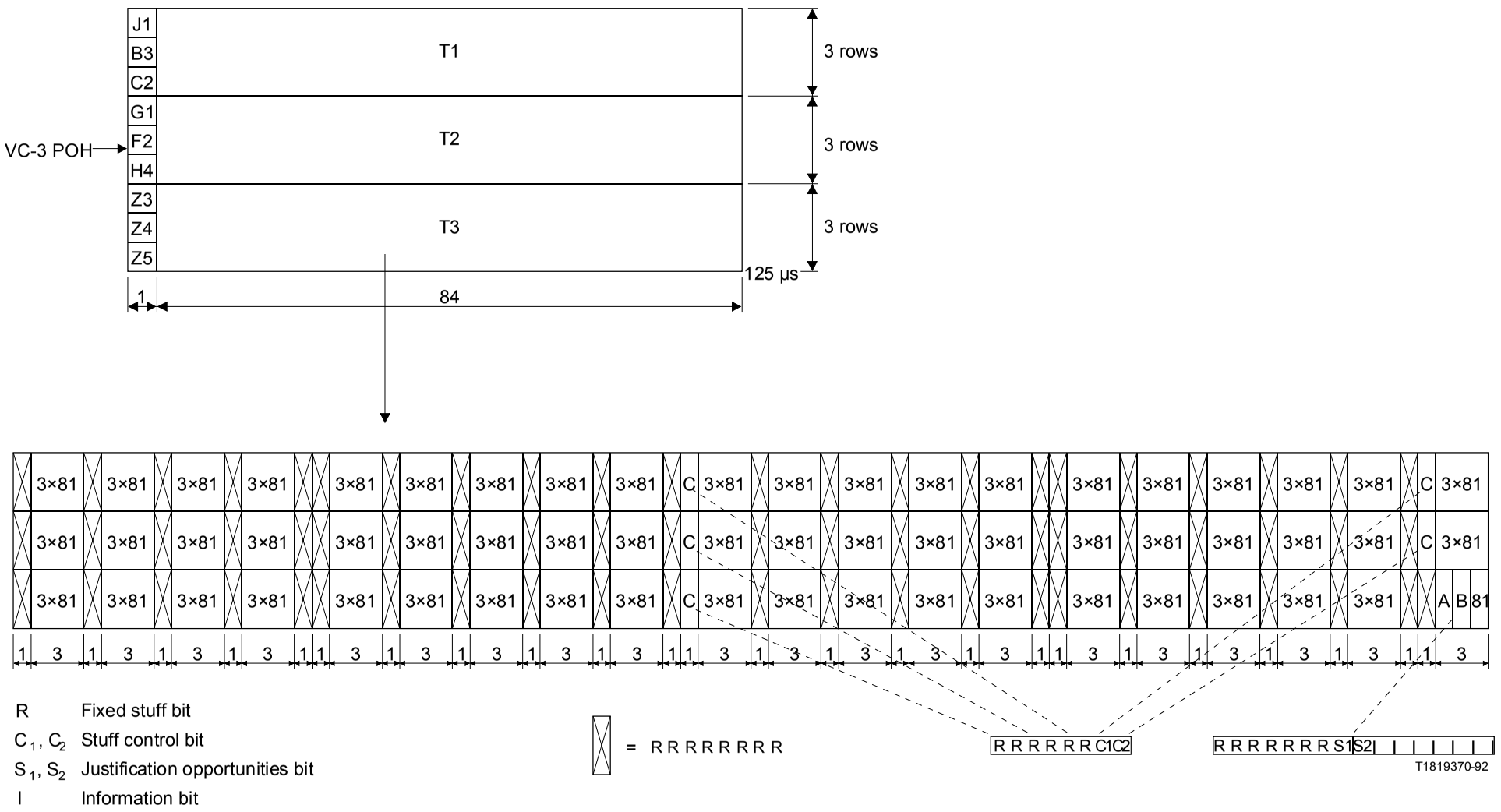


FIGURE 5-5/G.709

Asynchronous mapping of 34 368 kbit/s tributary into a VC-3

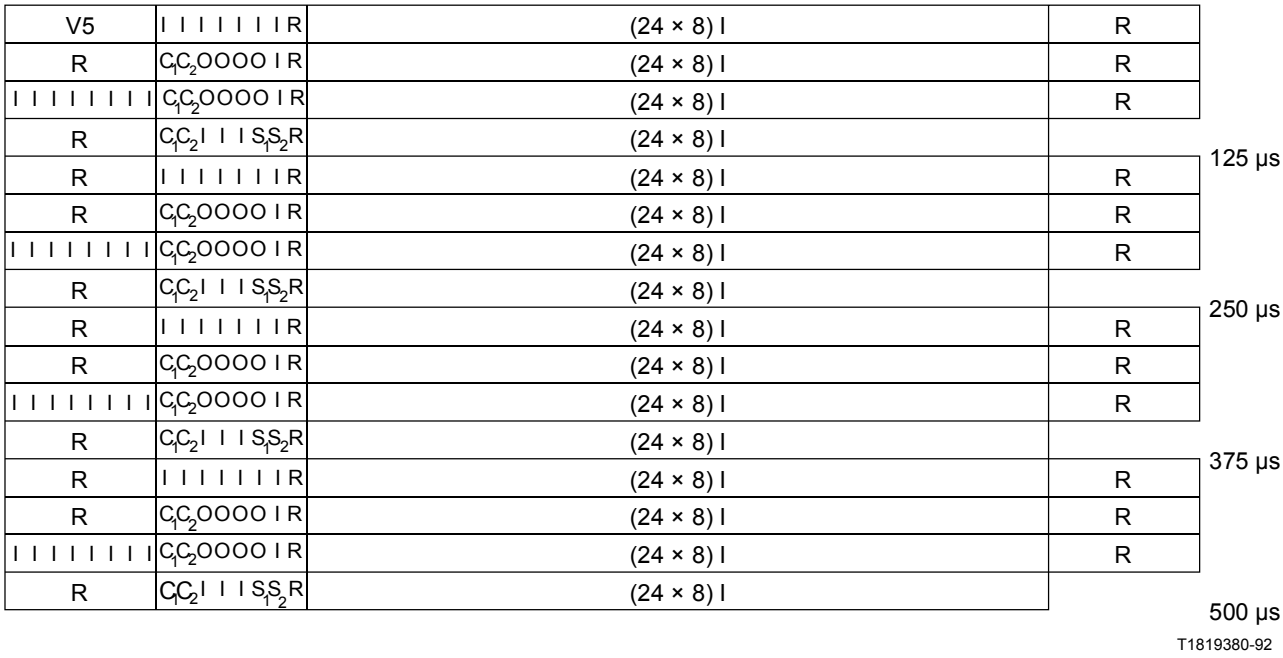
5.3 *Mapping of tributaries into the VC-2*

5.3.1 *Byte synchronous mapping of 8448 kbit/s*

Under study.

5.3.2 *Asynchronous mapping of 6312 kbit/s*

One 6312 kbit/s signal can be mapped into a VC-21. Figure 5-6/G.709 shows this over a period of 500 µs.



I Information bit
R Fixed stuff bit
O Overhead bit
S Justification opportunity bit
C Justification control bit

FIGURE 5-6/G.709

Asynchronous mapping of 6312 kbit/s tributary

In addition to the VC-2 POH, the VC-2 consists of 3152 data bits, 24 justification control bits, 8 justification opportunity bits and 32 overhead communication channel bits. The remaining are fixed stuff (R). The O bits are reserved for future overhead communication purposes.

Two sets (C_1, C_2) of three justification control bits, are used to control the two justification opportunity bits S_1 and S_2 respectively.

$C_1C_1C_1$ = 000 indicates that S_1 is a data bit while $C_1C_1C_1$ = 111 indicates that S_1 is a justification bit. C_2 bits control S_2 in the same way. Majority vote should be used to make the justification decision in the desynchronizer for protection against single bit error in the C-bits.

The value contained in S_1 and S_2 when they are justification bits is not defined. The receiver is required to ignore the value contained in these bits whenever they are used as justification bits.

5.3.3 *Bit synchronous mapping of 6312 kbit/s*

The bit synchronous mapping for 6312 kbit/s tributary is shown in Figure 5-7/G.709.

Note that a common desynchronizer can be used for both asynchronous and bit synchronous mapping.

V5	I I I I I I I R	(24 × 8) I	R	
R	1 0 OOOO I R	(24 × 8) I	R	
I I I I I I I I	1 0 OOOO I R	(24 × 8) I	R	
R	1 0 I I I R I R	(24 × 8) I		125 µs
R	I I I I I I I R	(24 × 8) I	R	
R	1 0 OOOO I R	(24 × 8) I	R	
I I I I I I I I	1 0 OOOO I R	(24 × 8) I	R	
R	1 0 I I I R I R	(24 × 8) I		250 µs
R	I I I I I I I R	(24 × 8) I	R	
R	1 0 OOOO I R	(24 × 8) I	R	
I I I I I I I I	1 0 OOOO I R	(24 × 8) I	R	
R	1 0 I I I R I R	(24 × 8) I		375 µs
R	I I I I I I I R	(24 × 8) I	R	
R	1 0 OOOO I R	(24 × 8) I	R	
I I I I I I I I	1 0 OOOO I R	(24 × 8) I	R	
R	1 0 I I I R I R	(24 × 8) I		500 µs

I Information bit
R Fixed stuff bit
O Overhead bit

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FIGURE 5-7/G.709

Bit synchronous mapping of 6312 kbit/s tributary

5.3.4 *Byte synchronous mapping of 6312 kbit/s*

Under study.

5.4 *Mapping of tributaries into VC-12*

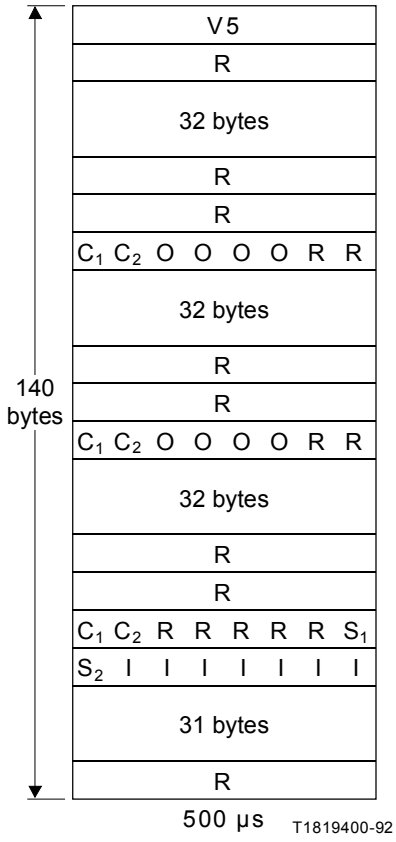
5.4.1 *Asynchronous mapping of 2048 kbit/s*

One 2048 kbit/s signal can be mapped into a VC-12. Figure 5-8/G.709 shows this over a period of 500 microseconds.

In addition to the VC-1 POH, the VC-12 consists of 1023 data bits, six justification control bits, two justification opportunity bits, and eight overhead communication channel bits. The remaining bits are fixed stuff (R) bits. The O bits are reserved for future overhead communication purposes.

Two sets (C_1, C_2) of three justification control bits are used to control the two justification opportunities S_1 and S_2 respectively. $C_1C_1C_1 = 000$ indicates that S_1 is a data bit while $C_1C_1C_1 = 111$ indicates that S_1 is a justification bit. C_2 controls S_2 in the same way. Majority vote should be used to make the justification decision in the desynchronizer for protection against single bit errors in the C-bits.

The value contained in C_1 and C_2 when they are justification bits is not defined. The receiver is required to ignore the value contained in these bits whenever they are used as justification bits.



I Information bit
R Fixed stuff bit(s)
O Overhead bit
S Justification opportunity bit
C Justification control bit

FIGURE 5-8/G.709

Asynchronous mapping of 2048 kbit/s tributary

5.4.2 *Bit synchronous mapping of 2048 kbit/s*

The bits synchronous mapping for 2048 kbit/s tributaries is shown in Figure 5-9/G.709.

Note that a common desynchronizer can be used for both asynchronous and bit synchronous mappings.

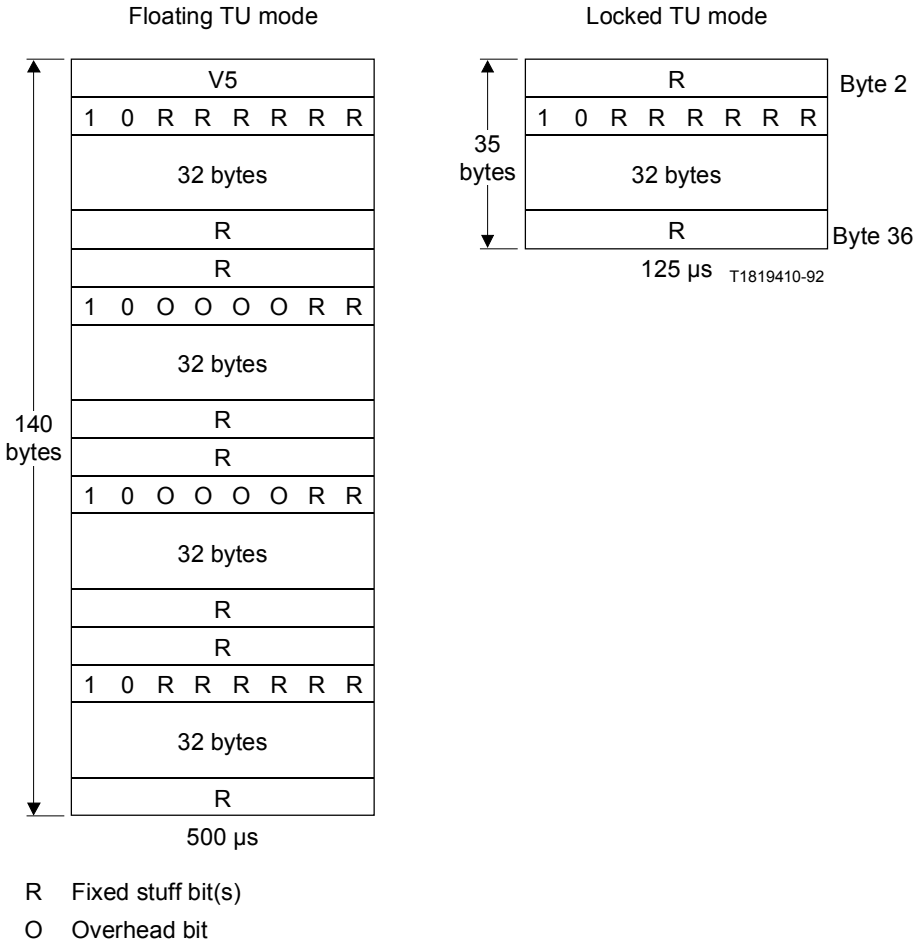


FIGURE 5-9/G.709

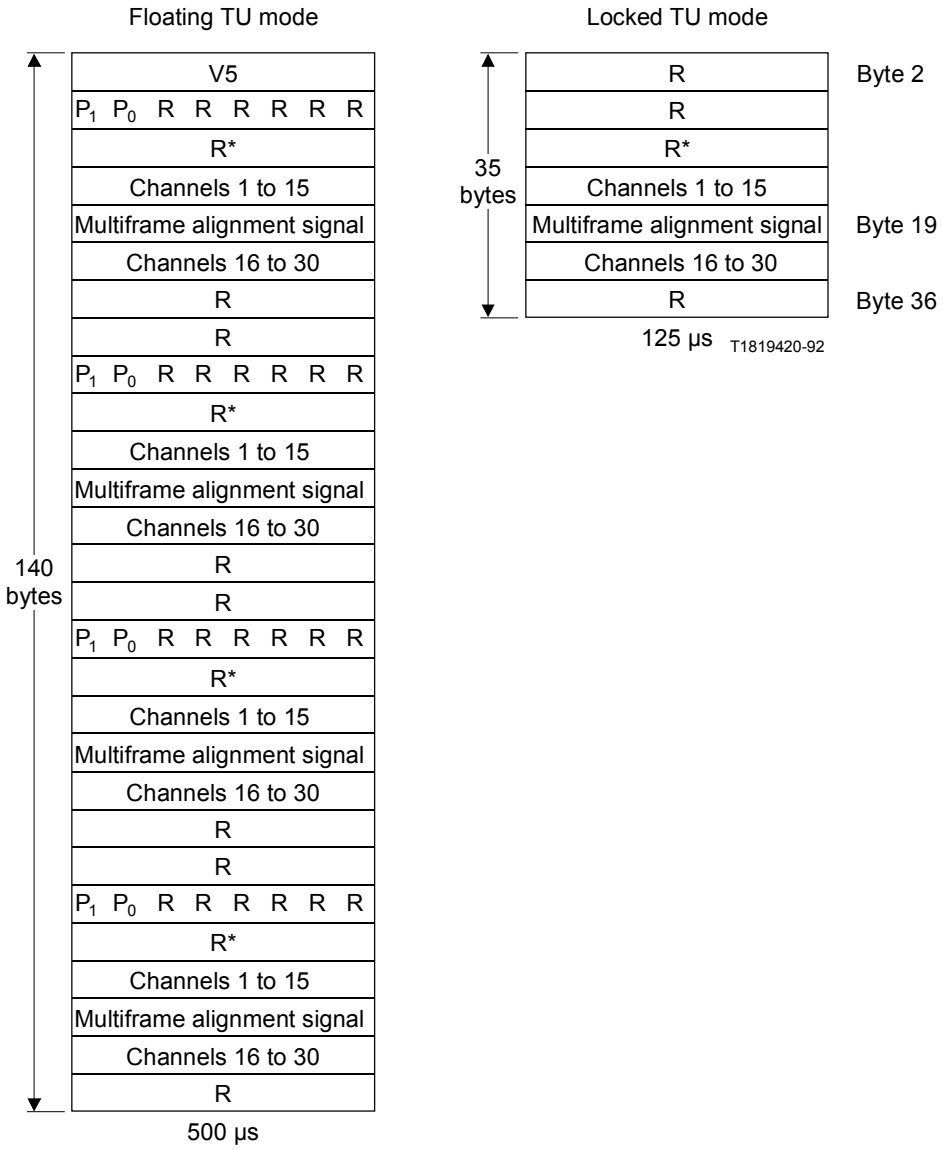
Bit synchronous mapping for 2048 kbit/s tributary

5.4.3 *Byte synchronous mapping of 2048 kbit/s*

Figure 5-10/G.709 shows byte synchronous mapping for 30 channel 2048 kbit/s tributaries employing channel associated signalling (CAS). Signalling is carried in byte 19. The signalling assignments are shown in Figure 5-11/G.709.

The S_1, S_2, S_3 and S_4 bits contain the signalling for the 30×64 kbit/s channels. The phase of the signalling bits is indicated in the P_1 and P_0 bits in floating TU mode and in the position indicator byte (H4) in locked TU mode. This is illustrated in Figure 5-11/G.709.

Byte synchronous mapping of 31 channel tributaries is shown in Figure 5-12/G.709. Byte 19 carries tributary channel 16.



R Fixed stuff bit(s)

R* May be used for timeslot 0 if required

P_1 P_0 00 at the start of the signalling frame on the first byte of the signalling frame

FIGURE 5-10/G.709

Byte synchronous mapping for 2048 kbit/s tributary (30 channels with channel associated signalling)

Locked													
				Floating									
H4 value				CAS format								Channel	
C_3	C_2	C_1	T	S_1	S_2	S_3	S_4	S_1	S_2	S_3	S_4		P_1 P_0
0	0	0	0	0	0	0	0	x	y	x	x	None	0 0
0	0	0	1	a	b	c	d	a	b	c	d	1/16	0 0
0	0	1	0	a	b	c	d	a	b	c	d	2/17	0 0
1	1	1	1	a	b	c	d	a	b	c	d	15/30	1 1

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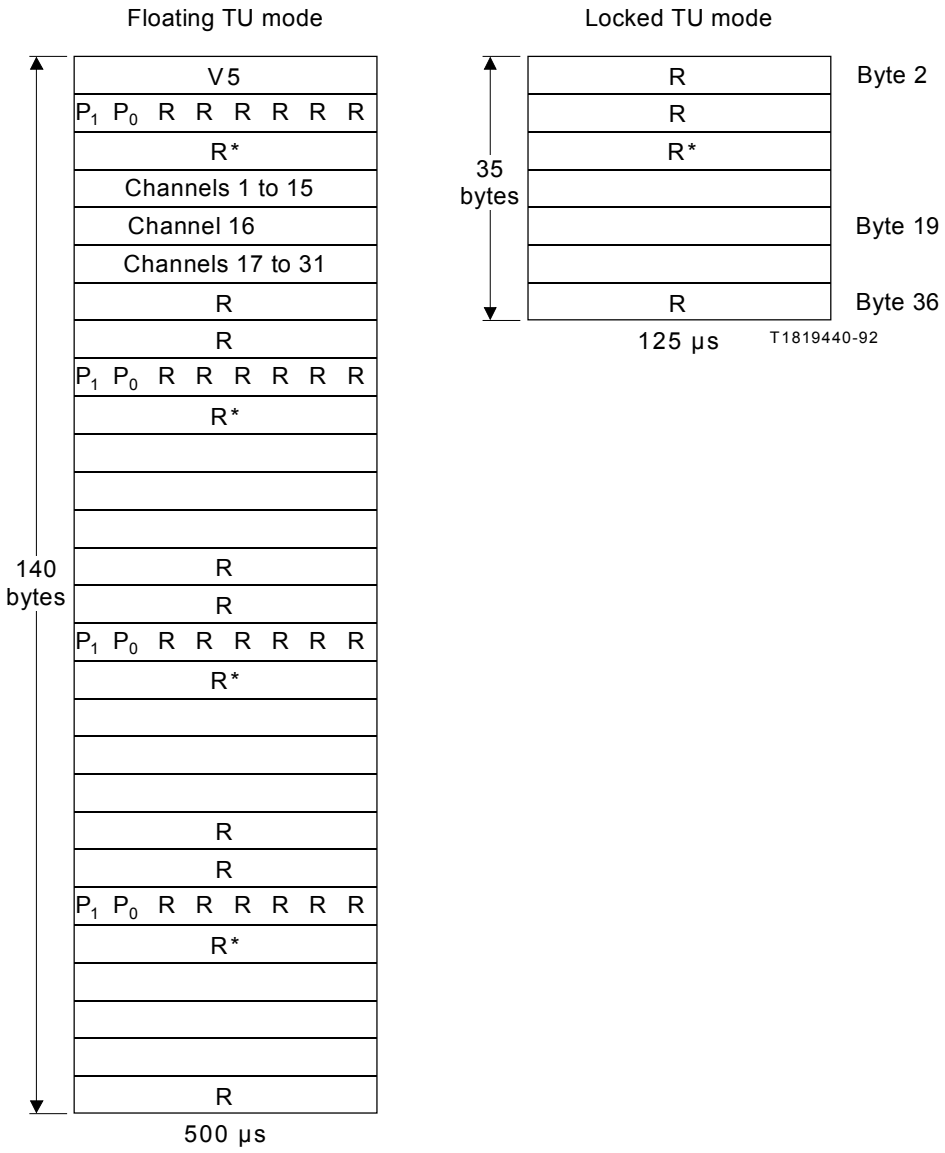
FIGURE 5-11/G.709

Out slot signalling assignments
(30-channel signalling operations)



R Fixed stuff bit(s)

R* May be used for timeslot 0 if required

P_1 P_0 00 at the start of the signalling frame on the first byte of the signalling frame

FIGURE 5-12/G.709

Byte synchronous mapping for 2048 kbit/s tributary (31 channels with common channel signalling)

5.5 *Mapping of tributaries into VC-11*

5.5.1 *Asynchronous mapping of 1544 kbit/s*

One 1544 kbit/s signal can be mapped into a VC-11. Figure 5-13/G.709 shows this over a period of 500 microseconds.

In addition to the VC-1 POH, the VC-11 consists of 771 data bits, six justification control bits, two justification opportunity bits, and eight overhead communication channel bits. The remaining bits are fixed stuff (R) bits. The O bits are reserved for future communication purposes.

Two sets (C_1, C_2) of three justification control bits are used to control the two justification opportunities, S_1 and S_2 respectively.

$C_1C_1C_1 = 000$ indicates that S_1 is a data bit while $C_1C_1C_1 = 111$ indicates that S_1 is a justification bit. C_2 controls S_2 in the same way. Majority vote should be used to make the justification decision in the desynchronizer for protection against single bit errors in the C-bits.

The value contained in S_1 and S_2 when they are justification bits is not defined. The receiver is required to ignore the value contained in these bits whenever they are used as justification bits.

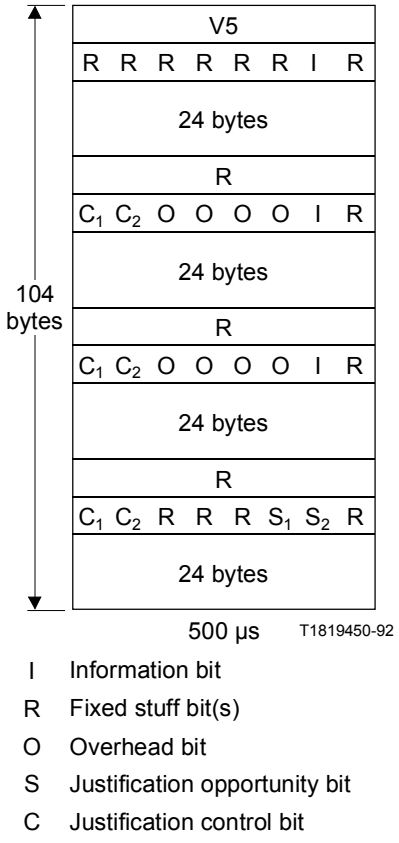


FIGURE 5-13/G.709

Asynchronous mapping of 1544 kbit/s tributary

5.5.2 *Bit synchronous mapping of 1544 kbit/s*

The bits synchronous mapping for 1544 kbit/s tributaries is shown in Figure 5-14/G.709.

Note that a common desynchronizer can be used for both asynchronous and bit synchronous mappings.

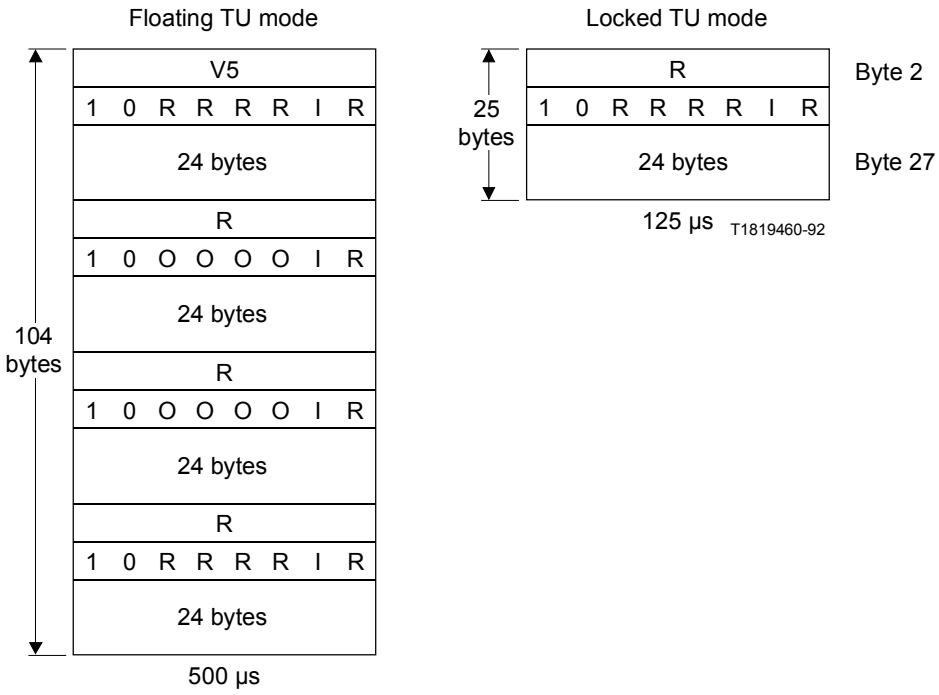


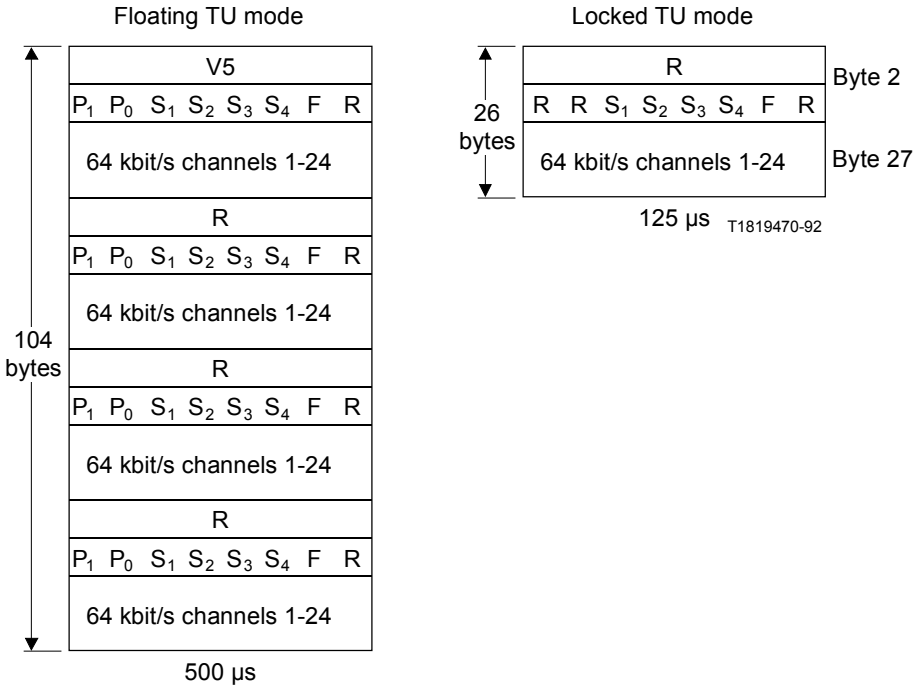
FIGURE 5-14/G.709

Bit synchronous mapping for 1544 kbit/s tributary

5.5.3 *Byte synchronous mapping of 1544 kbit/s*

The byte synchronous mapping for 1544 kbit/s is depicted in Figure 5-15/G.709.

The S_1, S_2, S_3 and S_4 bits contain the signalling for the 24×64 kbit/s channels. The phase of the signalling bits can be indicated in the P_1 and P_0 bits in floating TU mode, and in the position indicator byte (H4) in locked mode. This is illustrated in Figure 5-16/G.709. The usage of the P-bits is optional since the common channel signalling method and other channel associated signalling methods (e.g. Recommendation G.704, §§ 3.1.3 and 3.2.3) do not need the P-bits. The operations of the alternative channel associated signalling method is shown in Figure 5-17/G.709.



F 1544 kbit/s tributary frame bit

P_1 P_0 Signalling phase indicator

S Signalling

R Fixed stuff bit(s)

P_1 P_0 00 on the first signalling byte of the multiframe

FIGURE 5-15/G.709

Byte synchronous mapping for 1544 kbit/s tributary

Locked																			
					Floating														
					Signalling														
H4 value					2 state				4 state				16 state						
P_1	P_0	S_2	S_1	T	S_1	S_2	S_3	S_4	S_1	S_2	S_3	S_4	S_1	S_2	S_3	S_4	P_1	P_0
0	0	0	0	0	A_1	A_2	A_3	A_4	A_1	A_2	A_3	A_4	A_1	A_2	A_3	A_4	0	0
0	0	0	0	1	A_5	A_6	A_7	A_8	A_5	A_6	A_7	A_8	A_5	A_6	A_7	A_8	0	0
0	0	0	1	0	A_9	A_{10}	A_{11}	A_{12}	A_9	A_{10}	A_{11}	A_{12}	A_9	A_{10}	A_{11}	A_{12}	0	0
0	0	0	1	1	A_{13}	A_{14}	A_{15}	A_{16}	A_{13}	A_{14}	A_{15}	A_{16}	A_{13}	A_{14}	A_{15}	A_{16}	0	0
0	0	1	0	0	A_{17}	A_{18}	A_{19}	A_{20}	A_{17}	A_{18}	A_{19}	A_{20}	A_{17}	A_{18}	A_{19}	A_{20}	0	0
0	0	1	0	1	A_{21}	A_{22}	A_{23}	A_{24}	A_{21}	A_{22}	A_{23}	A_{24}	A_{21}	A_{22}	A_{23}	A_{24}	0	0
0	1	0	0	0	A_1	A_2	A_3	A_4	B_1	B_2	B_3	B_4	B_1	B_2	B_3	B_4	0	1
0	1	0	0	1	A_5	A_6	A_7	A_8	B_5	B_6	B_7	B_8	B_5	B_6	B_7	B_8	0	1
0	1	0	1	0	A_9	A_{10}	A_{11}	A_{12}	B_9	B_{10}	B_{11}	B_{12}	B_9	B_{10}	B_{11}	B_{12}	0	1
0	1	0	1	1	A_{13}	A_{14}	A_{15}	A_{16}	B_{13}	B_{14}	B_{15}	B_{16}	B_{13}	B_{14}	B_{15}	B_{16}	0	1
0	1	1	0	0	A_{17}	A_{18}	A_{19}	A_{20}	B_{17}	B_{18}	B_{19}	B_{20}	B_{17}	B_{18}	B_{19}	B_{20}	0	1
0	1	1	0	1	A_{21}	A_{22}	A_{23}	A_{24}	B_{21}	B_{22}	B_{23}	B_{24}	B_{21}	B_{22}	B_{23}	B_{24}	0	1
1	0	0	0	0	A_1	A_2	A_3	A_4	A_1	A_2	A_3	A_4	C_1	C_2	C_3	C_4	1	0
1	0	0	0	1	A_5	A_6	A_7	A_8	A_5	A_6	A_7	A_8	C_5	C_6	C_7	C_8	1	0
1	0	0	1	0	A_9	A_{10}	A_{11}	A_{12}	A_9	A_{10}	A_{11}	A_{12}	C_9	C_{10}	C_{11}	C_{12}	1	0
1	0	0	1	1	A_{13}	A_{14}	A_{15}	A_{16}	A_{13}	A_{14}	A_{15}	A_{16}	C_{13}	C_{14}	C_{15}	C_{16}	1	0
1	0	1	0	0	A_{17}	A_{18}	A_{19}	A_{20}	A_{17}	A_{18}	A_{19}	A_{20}	C_{17}	C_{18}	C_{19}	C_{20}	1	0
1	0	1	0	1	A_{21}	A_{22}	A_{23}	A_{24}	A_{21}	A_{22}	A_{23}	A_{24}	C_{21}	C_{22}	C_{23}	C_{24}	1	0
1	1	0	0	0	A_1	A_2	A_3	A_4	B_1	B_2	B_3	B_4	D_1	D_2	D_3	D_4	1	1
1	1	0	0	1	A_5	A_6	A_7	A_8	B_5	B_6	B_7	B_8	D_5	D_6	D_7	D_8	1	1
1	1	0	1	0	A_9	A_{10}	A_{11}	A_{12}	B_9	B_{10}	B_{11}	B_{12}	D_9	D_{10}	D_{11}	D_{12}	1	1
1	1	0	1	1	A_{13}	A_{14}	A_{15}	A_{16}	B_{13}	B_{14}	B_{15}	B_{16}	D_{13}	D_{14}	D_{15}	D_{16}	1	1
1	1	1	0	0	A_{17}	A_{18}	A_{19}	A_{20}	B_{17}	B_{18}	B_{19}	B_{20}	D_{17}	D_{18}	D_{19}	D_{20}	1	1
1	1	1	0	1	A_{21}	A_{22}	A_{23}	A_{24}	B_{21}	B_{22}	B_{23}	B_{24}	D_{21}	D_{22}	D_{23}	D_{24}	1	1

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FIGURE 5-16/G.709

Out slot signalling assignments
(24-channel signalling operations)

Frame number	n	n+1	n+2	n+3	n+4	n+5	n+6	n+7
Use of S_i bit (i = 1 ,2 ,3 ,4)	F_s	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	X
(Note 1)	(Note 2)	(Note 3)						(Note 5)

Note 1 – Each S_i (i = 1, 2, 3, 4) constitutes an independent signalling multiframe over eight frames. S_i includes the phase indicator in itself so that the PP-bits cannot be used for the phase indicator.

Note 2 – The F_s bit is either alternate 0, 1 or the following 48 bit digital pattern:

A101011011 0000011001 1010100111 0011110110 10000101

For the 48 bit digital pattern, the A-bit is usually fixed to state 1 and is reserved for optional use. The pattern is generated according to the following primitive polynomial (refer to Recommendation X.50):

$$x^7 + x^4 + 1$$

Note 3 – Y_j bit (j = 1 to 6) carries channel associated signalling or maintenance information. When the 48 bit pattern is adopted as F_s frame alignment signal, each Y_j bit (j = 1 to 6) can be multiframed, as follows.

$$Y_{j1}, Y_{j2}, \ldots, Y_{j12}$$

Y_{jl} bit carries the following 16 bit frame alignment pattern generated according to the same primitive polynomial as for the 48 bit pattern.

A011101011011000

The A-bit is usually fixed to 1 and is reserved for optional use. Each Y_{ji} (i = 2 to 12) bit carries channel associated signalling for sub-rate circuits and/or maintenance information.

Note 4 – S_i bits (F_s, Y_1, . . . , Y_6 and X), all at state 1 indicates alarm indication signal AIS) for six 64 kbit/s channels.

Note 5 – The X-bit is usually fixed to state 1. When backward AIS for six 64 kbit/s channels is required to be sent, the X-bit is set to state 0.

FIGURE 5-17/G.709

Out slot signalling assignments (24-channel signalling operations)

5.6 *VC-11 to VC-12 conversion for transport by a TU-12*

When transporting a VC-11 in a TU-12, the VC-11 is adapted by adding fixed stuff with even parity as shown in Figure 5-18/G.709. Thus the resulting TU-12 payload can be monitored and cross-connected in the network as though it were a VC-12 with its BIP value unchanged while preserving end-to-end integrity of the real VC-11 path.

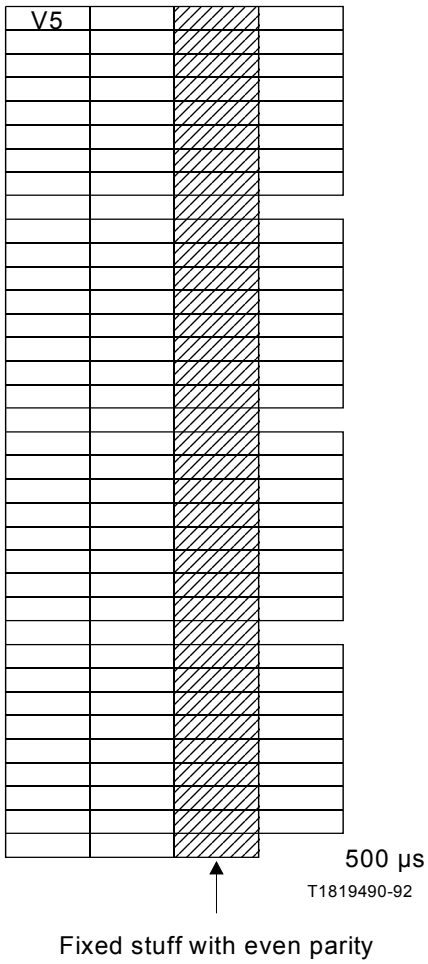


FIGURE 5-18/G.709

Conversion of VC-11 to VC-12 for transport by TU-12

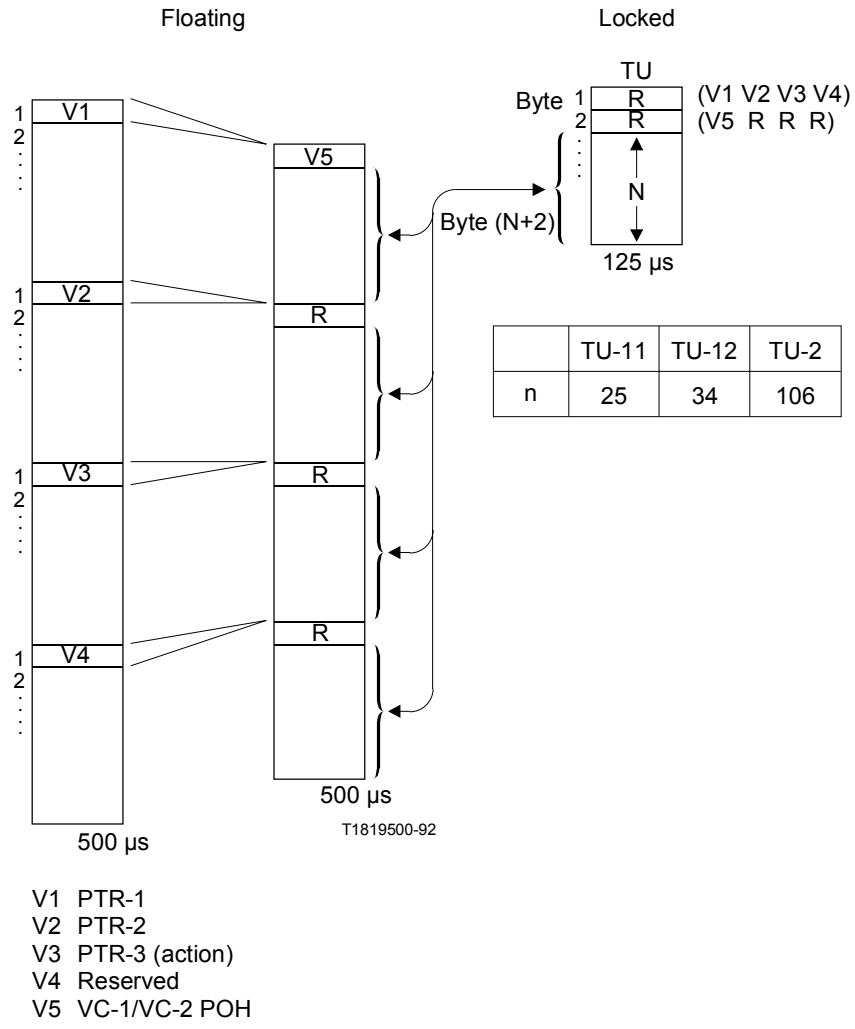
5.7 *Floating and locked mode conversion*

There are two possible multiplexing modes of the TU structures: floating and locked.

In the floating TU mode four consecutive 125 microseconds VC-*n* frames (*n* = 11, 12, 2) are organized into a 500 microseconds multiframe, the phase of which is indicated by the position indicator byte (H4) in the VC-m POH (m = 3, 4). This 500 microseconds TU multiframe is shown in Figure 3-9/G.709.

Locked TU mode of transport is a fixed mapping of synchronous structured payloads into a VC-m. This provides a direct correspondence between subtending tributary information and the location of that information within the VC-*n*. Since the tributary information is fixed and immediately identifiable with respect to the AU-m pointer associated with the VC-m, no TU pointers are required. All bytes of a TU or TUG are available for payload usage.

Figure 5-19/G.709 illustrates the conversion between floating and locked TU modes for each of the three TU sizes. Note that certain bytes (R) in the current set of mappings are not used in the floating mode in order that those mappings can be used in both floating and locked modes. Since the V1-V4 and V5 bytes are reserved, the 500 microseconds VC multiframe is unnecessary. Therefore the role of the position indicator byte (H4) in locked mode is to define 2 and 3 ms signalling frames for byte synchronous mappings.



	TU-11	TU-12	TU-2
n	25	34	106

FIGURE 5-19/G.709

Conversion between floating and locked TU modes

5.8 *Mapping of ATM cells*

The mapping of ATM cells is performed by aligning the byte structure of every cell with the byte structure of the virtual container used including the concatenated structure (VC-*x* or VC-x-mc, $x >= 1$). Since the relevant C-*x* capacity may not be an integer multiple of the ATM cell length (53 octets), a cell is allowed to cross the C-x boundary.

The ATM cell information field (48 bytes) shall be scrambled before mapping into the VC-*x* or VC-x-mc. In the reverse operation, following termination of the VC-*x* or VC-x-mc signal, the ATM cell information field will be descrambled before being passed to the ATM Layer. A self-synchronizing scrambler with generator polynomial $x^{43} + 1$ shall be used. The scrambler operates for the duration of the cell information field. During the 5-octet header the scrambler operation is suspended and the scrambler state retained. Cell information field scrambling is required to provide security against false cell delineation and cell information field replicating the STM-N frame alignment word.

When the VC-*x* or VC-x-mc is terminated, the cell must be recovered. The ATM cell header contains a header error control (HEC) field which is used in a similar way to a frame alignment word to achieve cell delineation. This HEC method uses the correlation between the header bits to be protected by the HEC (32 bits) and the control bit of the HEC (8 bits) introduced in the header after computation with a shortened cyclic code with generating polynomial $g(x) = x^8 + x^2 + x + 1$.

The remainder from this polynomial is then added to the fixed pattern "01010101" in order to improve the cell delineation performance. This method is similar to conventional frame alignment recovery where the alignment word is not fixed but varies from cell to cell.

More information on HEC cell delineation is given in Recommendation I.432.

5.8.1 *Mapping of ATM cells into VC-4*

The ATM cell stream is mapped into C-4 with its octet boundaries aligned with the C-4 byte boundaries. The C-4 is then mapped into VC-4 together with the VC-4 POH (see Figure 5-20/G.709). The ATM cell boundaries are thus aligned with the VC-4 byte boundaries. Since the C-4 capacity (2340 octets) is not an integer multiple of the cell length (53 octets), a cell may cross a C-4 boundary.

The H4 byte indicates the offset in octets from itself to the first cell boundary following the H4 byte in the payload. The permissible range of values of H4 is 0 to 52. The bit allocation for the H4 byte is given in Figure 5-21/G.709.

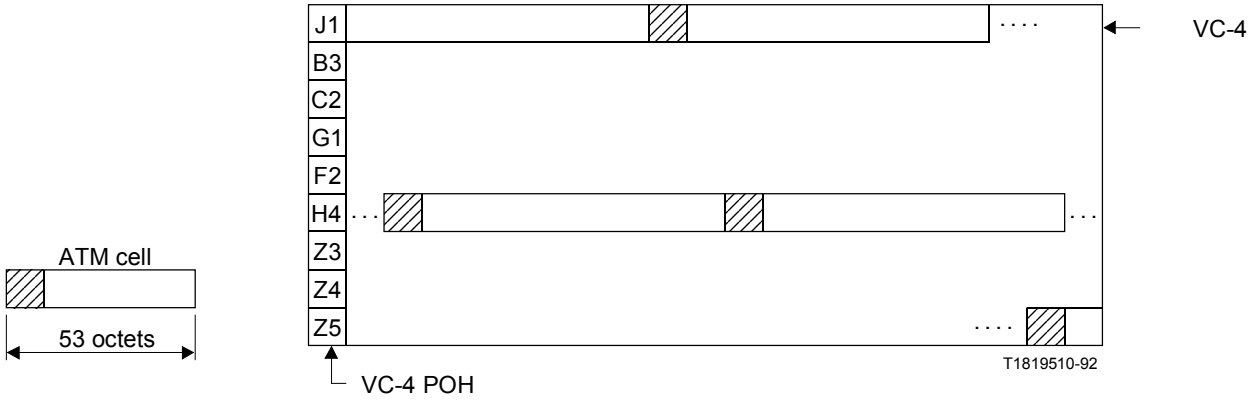


FIGURE 5-20/G.709

Mapping of ATM cells in the VC-4

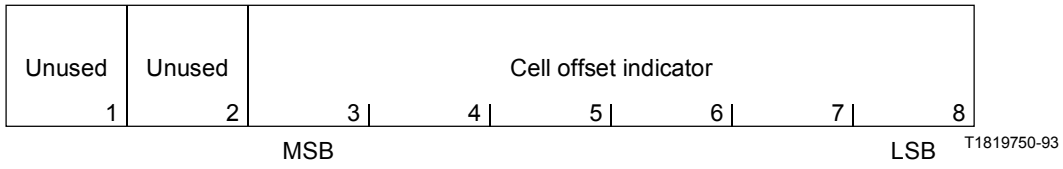


FIGURE 5-21/G.709

Multiframe indicator (H4) coding for mapping of ATM cells in the VC-4

The H4 position indicator will be set at the sending side to indicate the next occurrence of a cell boundary. The H4 position indicator provides a cell boundary indication which may optionally be used to supplement the mandatory HEC cell delineation mechanism.

The H4 byte may be used to assist in finding the initial cell delineation. It does not allow, however, the confirmation of cell delineation or determination of loss of cell delineation.

5.8.2 *Mapping of ATM cells into other VCs*

Detailed mappings are under study.

ANNEX A

(to Recommendation G.709)

Alphabetical list of abbreviations used in this Recommendation

AIS	Alarm indication signal
AU	Administrative unit
AUG	Administrative unit group
CAS	Channel associated signalling
CI	Concatenation indication
FEBE	Far end block error
FERF	Far end receive failure
HEC	Header error control
NDF	New data flag
NNI	Network-node interface
NPI	Null pointer indication
POH	Path overhead
PTR	Pointer
SDH	Synchronous digital hierarchy
SOH	Section overhead
STM	Synchronous transport module
TU	Tributary unit
TUG	Tributary unit group
VC	Virtual container

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