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SERIES G: TRANSMISSION SYSTEMS AND MEDIA, DIGITAL SYSTEMS AND NETWORKS

General aspects of digital transmission systems; terminal equipments

General

FRAME ALIGNMENT AND CYCLIC REDUNDANCY CHECK (CRC) PROCEDURES RELATING TO BASIC FRAME STRUCTURES DEFINED IN RECOMMENDATION G.704

Reedition of CCITT Recommendation G.706 published in the Blue Book, Fascicle III.4 (1988)

NOTES

1 CCITT Recommendation G.706 was published in Fascicle III.4 of the *Blue Book*. This file is an extract from the *Blue Book*. While the presentation and layout of the text might be slightly different from the *Blue Book* version, the contents of the file are identical to the *Blue Book* version and copyright conditions remain unchanged (see below).

2 In this Recommendation, the expression “Administration” is used for conciseness to indicate both a telecommunication administration and a recognized operating agency.

Recommendation G.706

FRAME ALIGNMENT AND CYCLIC REDUNDANCY CHECK (CRC) PROCEDURES RELATING TO BASIC FRAME STRUCTURES DEFINED IN RECOMMENDATION G.704

(Melbourne, 1988)

1 General

This Recommendation relates to equipment which receives signals with basic frame structures as defined in Recommendation G.704. It defines the frame alignment, the cyclic redundancy check (CRC) multiframe alignment and CRC bit error monitoring procedures to be used by such equipment. Annex A contains background information about the use of the CRC procedures and their limitations.

2 Frame alignment and CRC procedures at l544 kbit/s interface

2.1 *Loss and recovery of frame alignment*

There are two alternative multiframe structures at the 1544 kbit/s interface:

a) 24-frame multiframe, and

b) 12-frame multiframe.

2.1.1 *Loss of frame alignment*

The frame alignment signal should be monitored to determine if frame alignment has been lost. Loss of frame alignment should be detected within 12 ms. Loss of frame alignment must be confirmed over several frames to avoid the unnecessary initiation of the frame alignment recovery procedure due to transmission bit errors. The frame alignment recovery procedure should commence immediately once loss of frame alignment has been confirmed.

Note – For the 12-frame multiframe described in Recommendation G.704, loss of multiframe alignment is deemed to occur when loss of frame alignment occurs.

2.1.2 *Recovery of frame alignment*

2.1.2.1 *Frame alignment recovery time*

The frame alignment recovery time is specified in terms of the maximum average reframe time in the absence of errors. The maximum average reframe time is the average time to reframe when the maximum number of bit positions must be examined for locating the frame alignment signal.

a) 24-frame multiframe

The maximum average reframe time should not exceed 15 ms.

Note – Some existing designs of equipment were designed to a limit of 50 ms.

b) 12-frame multiframe

The maximum average reframe time should not exceed 50 ms.

Note – These times do not include the time required for the CRC procedure for false frame alignment verification defined in § 2.2.2.

2.1.2.2 *Strategy for frame alignment recovery*

a) *24-frame multiframe*

Frame alignment should be recovered by detecting the valid frame alignment signal. When the CRC-6 code is utilized for error performance monitoring (see § 2.2.3), the CRC-6 information may be coupled with the framing algorithm to ensure that a valid frame alignment signal contained within the 24 F-bits is the only pattern onto which the reframe circuit can permanently lock. This procedure is illustrated in Figure 1/G.706.

b) *12-frame multiframe*

Overall frame alignment should be recovered by way of simultaneous detection of the frame alignment signal and the multiframe alignment signal, or of frame alignment followed by multiframe alignment.

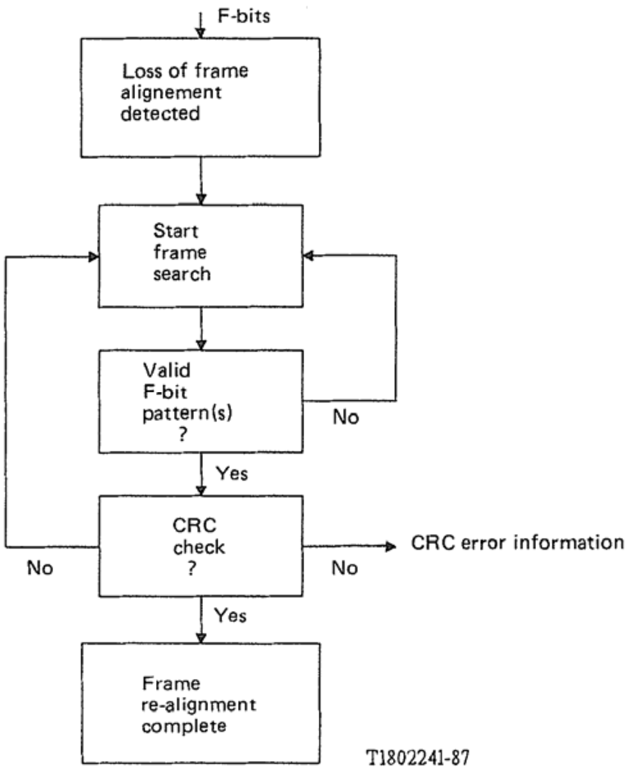

FIGURE 1/G.706

False frame alignment protection using a cyclic redundancy check (CRC) (1544 and 6312 kbit/s)

2.2 *CRC bit monitoring*

Error monitoring by CRC-6 assumes a signal quality sufficient for frame alignment to be established so that CRC-6 bits can be correctly accessed.

2.2.1 *Monitoring procedure*

i) A received CRC Message Block (CMB) is acted upon by the multiplication/division process defined in Recommendation G.704 after having its F-bits replaced by binary 1s.

ii) The remainder resulting from the division process is then stored and compared on a bit-by-bit basis with the CRC bits received in the next CMB.

iii) If the remainder exactly corresponds to the CRC bits contained in the next CMB of the received signal, it is assumed that the checked CMB is error-free.

2.2.2 *Monitoring for false frame alignment* (see § A.1.1)

In the case of the 24-frame multiframe, when the CRC-6 code is utilized for error performance monitoring, it may also be used to provide immunity against spurious frame alignment signals. The procedure described in § 2.1.2.2 a) should be followed.

2.2.3 *Error performance monitoring using CRC-6* (see § A.1.2)

For the purpose of error performance monitoring, it should be possible to obtain indications of each CRC message block which is received in error. The consequent error information should be used in accordance with the requirements to be defined in respective equipment Recommendations.

3 Frame alignment and CRC procedures at 6312 kbit/s interface

3.1 *Loss and recovery of frame alignment*

For the 6312 kbit/s hierarchical level, the term "frame alignment" is synonymous with "multiframe alignment". The last five bits of the 789-bit frame are designated as the F-bits (see Recommendation G.704) and are time-shared as a frame alignment signal and for other purposes.

3.1.1 *Loss of frame alignment*

The frame alignment signal should be monitored to determine if frame alignment has been lost. The loss of frame alignment is declared when seven consecutive incorrect frame alignment signals have been received.

The recovery of frame alignment procedure should start immediately once loss of frame alignment has been confirmed.

3.1.2 *Recovery of frame alignment*

3.1.2.1 *Frame alignment recovery time*

The frame alignment recovery time is specified in terms of the maximum average reframe time in the absence of errors. The maximum average reframe time is the average time to reframe when the maximum number of bit positions must be examined for locating the frame alignment signal.

The maximum average reframe time should be less than 5 ms.

3.1.2.2 *Strategy for frame alignment recovery*

Frame alignment should be recovered by detecting three consecutive correct frame alignment signals. In addition to this, the CRC-5 code (see § 3.2) should be coupled with the framing algorithm to ensure that a valid frame alignment signal contained within the F-bits is the only pattern onto which the reframe circuit can permanently lock. This procedure is illustrated in Figure 1/G.706.

3.2 *CRC bit monitoring*

Error monitoring by CRC-5 assumes a signal quality sufficient for frame alignment to be established so that the CRC-5 bits can be correctly accessed.

3.2.1 *Monitoring procedure*

i) A received sequence of 3156 serial bits (i.e. 3151 bits of CMB and 5 CRC bits) is divided by the generator polynomial defined in Recommendation G.704.

ii) If the remainder resulting from the division process is 00000, it is assumed that the checked CMB is error-free.

3.2.2 *Monitoring for false frame alignment* (see § A.1.1)

The procedure in § 3.1.2.2 should be followed when the CRC-5 code is used to provide immunity against false frame alignment signal.

Using the CRC-5 code, it should be possible to detect false frame alignment within 1 second and with greater than 0.99 probability. On detection of such an event, a re-search for correct frame alignment should be initiated.

With a random error ratio of 10^{-4}, the mean time between two events of falsely initiating a search for frame alignment due to an excessive number of errored CRC message blocks should be more than one year.

Note 1 – With a random error ratio of approximately 10^{-3}, it is almost impossible to distinguish whether CRC errors are caused by the false frame alignment or by transmission bit errors.

Note 2 – To achieve the probability bounds stated above, one method is to count the errored CRC-5 message blocks with the understanding that a count of 32 consecutive errored CRC-5 blocks indicates false frame alignment.

3.2.3 *Error performance monitoring using CRC-5* (see § A.1.2)

For the purpose of error performance monitoring, it should be possible to obtain indications for each CRC message block which is received in error. The consequent error information should be used in accordance with the requirements to be defined in the respective equipment Recommendations.

4 Frame alignment and CRC procedures at 2048 kbit/s interface

4.1 *Loss and recovery of frame alignment*

4.1.1 *Loss of frame alignment*

Frame alignment will be assumed to have been lost when three consecutive incorrect frame alignment signals have been received.

Note 1 – In addition to the preceding, in order to limit the effect of spurious frame alignment signals, the following procedure may be used:

Frame alignment will be assumed to have been lost when bit 2 in time slot 0 in frames not containing the frame alignment signal has been received with an error on three consecutive occasions.

Note 2 – Loss of frame alignment can also be invoked by an inability to achieve CRC multiframe alignment in accordance with § 4.2, or by exceeding a specified count of errored CRC message blocks as indicated in § 4.3.2.

4.1.2 *Strategy for frame alignment recovery*

Frame alignment will be assumed to have been recovered when the following sequence is detected:

– for the first time, the presence of the correct frame alignment signal;

– the absence of the frame alignment signal in the following frame detected by verifying that bit 2 of the basic frame is a 1;

– for the second time, the presence of the correct frame alignment signal in the next frame.

Note – To avoid the possibility of a state in which no frame alignment can be achieved due to the presence of a spurious frame alignment signal, the following procedure may be used:

When a valid frame alignment signal is detected in frame n, a check should be made to ensure that a frame alignment signal does not exist in frame $n + 1$, and also that a frame alignment signal exists in frame $n + 2$. Failure to meet one or both of these requirements should cause a new search to be initiated in frame $n + 2$.

4.2 *CRC multiframe alignment using information in bit 1 of the basic frame*

If a condition of assumed frame alignment has been achieved, CRC multiframe alignment should be deemed to have occurred if at least two valid CRC multiframe alignment signals can be located within 8 ms, the time separating two CRC multiframe alignment signals being 2 ms or a multiple of 2 ms. The search for the CRC multiframe alignment signal should be made only in basic frames not containing the frame alignment signal.

If multiframe alignment cannot be achieved within 8 ms, it should be assumed that frame alignment is due to a spurious frame alignment signal and a re-search for frame alignment should be initiated.

Note 1 – The re-search for frame alignment should be started at a point just after the location of the assumed spurious frame alignment signal. This will usually avoid realignment onto the spurious frame alignment signal.

Note 2 – Consequent actions taken as a result of loss of frame alignment should no longer be applied once frame alignment has been recovered. However, if CRC multiframe alignment cannot be achieved within a time limit in the range of 100 ms to 500 ms, e.g. owing to the CRC procedure not being implemented at the transmitting side, consequent actions should be taken equivalent to those specified for loss of frame alignment.

4.3 *CRC bit monitoring*

If frame and CRC multiframe alignment have been achieved, the monitoring of the CRC bits in each sub-multiframe should commence.

4.3.1 *Monitoring procedure*

i) A received CRC sub-multiframe (SMF) is acted upon by the multiplication/division process defined in Recommendation G.704 after having its CRC bits extracted and replaced by 0s.

ii) The remainder resulting from the division process is then stored and subsequently compared on a bit-by-bit basis with the CRC bits received in the next SMF.

iii) If the remainder exactly corresponds to the CRC bits contained in the next SMF of the received signal, it is assumed that the checked SMF is error-free.

4.3.2 *Monitoring for false frame alignment* (see § A.1.1)

It should be possible to detect a condition of false frame alignment within 1 second and with a probability greater than 0.99. On detection of such an event, a re-search for frame alignment should be initiated.

With a random error ratio of 10^{-3} the probability of falsely initiating a search for frame alignment due to an excessive number of errored CRC blocks should be less than 10^{-4} over a 1 second period.

Figure 2/G.706 shows an illustration of the procedure to be followed in passing from the frame alignment search to error monitoring using CRC.

Note 1 – The re-search for frame alignment should be started at a point just after the location of the assumed spurious frame alignment signal. This will usually avoid realignment onto the spurious frame alignment signal.

Note 2 – To achieve the probability bounds stated above, a preferred threshold count is 915 errored CRC blocks out of 1000, with the understanding that a count of ≥ 915 errored CRC blocks indicates false frame alignment.

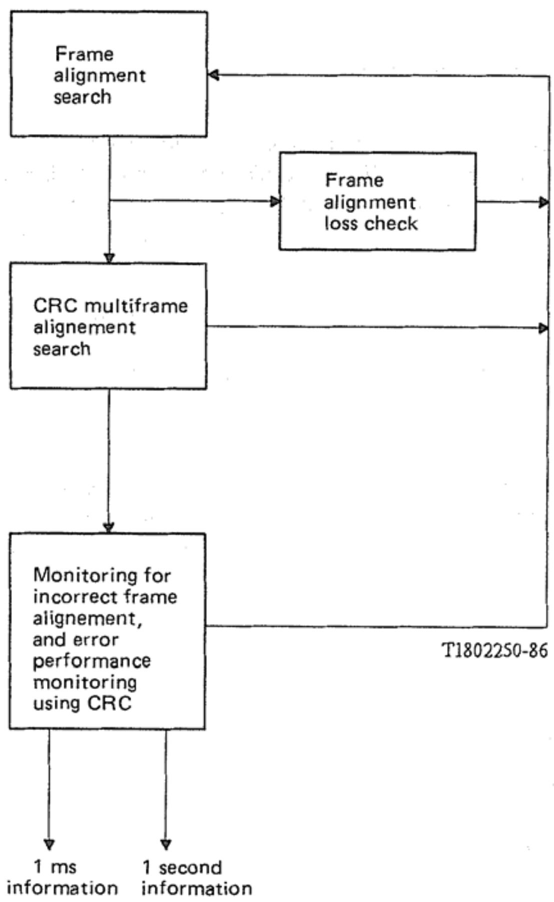

FIGURE 2/G.706

Procedure to be followed in passing from the frame alignment search to error monitoring using a cyclic redundancy check (CRC) (2048 kbit/s)

4.3.3 *Error performance monitoring using CRC-4* (see § A.1.2)

Information on the status of the CRC processing should be made available in two forms:

a) *Direct information*

Every time a CRC block is detected in error, it will be necessary to indicate this condition.

b) *Integrated information*

In consecutive 1 second periods, the number of errored CRC blocks should be made available. This number will be in the range 0 to 1000 (decimal).

5 Frame alignment and CRC procedures at 8448 kbit/s interface

For further study.

ANNEX A

(to Recommendation G.706)

Background information on the use of cyclic redundancy check (CRC) procedures

A.1 *Reasons for application of CRC*

CRC procedures can be used for both protection against false frame alignment and for bit error monitoring.

A.1.1 *Protection against false frame alignment*

The CRC procedures are used to protect against false frame alignment of receivers of multiplex signals. For example, false frame alignment could occur in an ISDN if a user imitates a frame alignment signal in his non-voice terminal. However, since a user is not controlling the composition of a multiplex frame, the addition of CRC bits, and evaluation of these bits in the receiver, leads to detection of the false frame alignment.

A.1.2 *Bit error monitoring*

The CRC procedure is also used for improved bit error ratio monitoring if low values of error ratio (e.g. 10^{-6}) are to be considered. CRC monitoring (like monitoring of the frame alignment signal) takes account of the entire digital link between the source and sink of a multiplex signal, as opposed to code violation monitoring (e.g. monitoring of AMI, HDB3 or B8ZS violations) which concerns only the digital line section nearest to the receiver, or in many cases only an interface line [e.g. between a digital multiplexer and an Exchange Terminal (ET)].

A.2 *Limitations of CRC procedures*

A.2.1 *Probability of undetected bit errors*

It can be estimated [1] that for CRC-*n*, and long message/check blocks, the probability that an error remains undetected approaches 2^{-n} even with a high bit error ratio; with a low bit error ratio, the probability is lower. The resulting inaccuracy (at most, with CRC-4, about 6% of blocks with undetected errors; similarly, with CRC-6, 1.6%) is tolerable for the required purpose.

A.2.2 *Limitation of application to bit error ratio measurement*

The CRC monitoring procedure is not well suited to measure values of bit error ratio that are so high that on average every message/check block contains at least one bit error (i.e. for BER = 10^{-3} or higher).

Reference

[1] LEUNG, C. and WITZKE, K.A. – A comparison of some error detecting CRC code standards. *IEEE Trans*. Vol. COM-33, pp. 996-998, 1985.

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