INTERNATIONAL TELECOMMUNICATION UNION

CCITT

THE INTERNATIONAL
TELEGRAPH AND TELEPHONE
CONSULTATIVE COMMITTEE

G.704

(11/1988)

SERIES G: TRANSMISSION SYSTEMS AND MEDIA, DIGITAL SYSTEMS AND NETWORKS

General aspects of digital transmission systems; terminal equipments

General

SYNCHRONOUS FRAME STRUCTURES USED AT PRIMARY AND SECONDARY HIERARCHICAL LEVELS

Reedition of CCITT Recommendation G.704 published in the Blue Book, Fascicle III.4 (1988)

NOTES

1 CCITT Recommendation G.704 was published in Fascicle III.4 of the *Blue Book*. This file is an extract from the *Blue Book.* While the presentation and layout of the text might be slightly different from the *Blue Book* version, the contents of the file are identical to the *Blue Book* version and copyright conditions remain unchanged (see below).

2 In this Recommendation, the expression "Administration" is used for conciseness to indicate both a telecommunication administration and a recognized operating agency.

Recommendation G.704

SYNCHRONOUS FRAME STRUCTURES USED AT PRIMARY AND SECONDARY HIERARCHICAL LEVELS

(Malaga-Torremolinos, 1984; amended at Melbourne, 1988)

1 General

This Recommendation gives functional characteristics of interfaces associated with:

– network nodes, in particular, synchronous digital multiplex equipment and digital exchanges in IDNs for telephony and ISDNs, and

– PCM multiplexing equipment.

Paragraph 2 deals with basic frame structures, including details of frame length, frame alignment signals, cyclic redundancy check (CRC) procedures and other basic information.

Paragraphs 3 to 6 contain more specific information about how certain channels at 64 kbit/s and at other bit rates are accomodated within the basic frame structures described in § 2.

Electrical characteristics for these interfaces are defined in Recommendation G.703.

Note 1 – This Recommendation does not necessarily apply to those cases where the signals that cross the interfaces are devoted to non-switched connections, such as those for the transport of encoded wideband signals (e.g. broadcast TV signals or multiplexed sound-programme signals which need not be individually routed via the ISDN), see also Annex A to Recommendation G.702.

Note 2 – The frame structures recommended in this Recommendation do not apply to certain maintenance signals, such as the all 1s signals transmitted during fault conditions or other signals transmitted during out-of-service conditions.

Note 3 – Frame structures associated with digital multiplexing equipments using justification are covered in each corresponding equipment Recommendation.

Note 4 – Inclusion of channel structures at other bit rates than 64 kbit/s is a matter for further study. Recommendations G.761 and G.763 dealing with the characteristics of PCM/ADPCM transcoding equipment contain information about channel structures at 32 kbit/s. The more general use of those particular structures is a subject of further study.

2 Basic frame structures

2.1 *Basic frame structure at 1544 kbit/s*

2.1.1 *Frame length:*

193 bits, numbered 1 to 193. The frame repetition rate is 8000 Hz.

2.1.2 *F-bit*

The first bit of a frame is designated an F-bit, and is used for such purposes as frame alignment, performance monitoring and providing a data link.

2.1.3 *Allocation of F-bit*

Two alternative methods as given in Tables 1/G.704 and 2/G.704 for allocation of F-bits are recommended.

TABLE 1/G.704

Multiframe structure for the 24 frame multiframe

Frame number within multiframe	F-bit				Bit number(s) in each channel time slot		Signalling channel designation [a)]
	Bit number within multiframe	Assignements					
		FAS	DL	CRC	For character signal[a)]	For signalling [a)]	
1	1	–	*m*	–	1-8	–	
2	194	–	–	e_1	1-8	–	
3	387	–	*m*	–	1-8	–	
4	580	0	–	–	1-8	–	
5	773	–	*m*	–	1-8	–	
6	966	–	–	e_2	1-7	8	A
7	1159	–	*m*	–	1-8	–	
8	1352	0	–	–	1-8	–	
9	1545	–	*m*	–	1-8	–	
10	1738	–	–	e_3	1-8	–	
11	1931	–	*m*	–	1-8	–	
12	2124	1	–	–	1-7	8	B
13	2317	–	*m*	–	1-8	–	
14	2510	–	–	e_4	1-8	–	
15	2703	–	*m*	–	1-8	–	
16	2896	0	–	–	1-8	–	
17	3089	–	*m*	–	1-8	–	
18	3282	–	–	e_5	1-7	8	C
19	3475	–	*m*	–	1-8	–	
20	3668	1	–	–	1-8	–	
21	3861	–	*m*	–	1-8	–	
22	4054	–	–	e_6	1-8	–	
23	4247	–	*m*	–	1-8	–	
24	4440	1	–	–	1-7	8	D

FAS Frame alignement signal (. . . 001011 . . .).
DL 4 kbit/s data link (message bits *m*).
CRC CRC-6 (block check field (check bits e_1 . . . e_6).
[a)] Only applicable in the case of channel associated signalling see (§ 3.1.3.2).

TABLE 2/G.704

Allocation of F-bit for the 12-frame multiframe

Frame number	Frame alignment signal	Multiframe alignment signal or signalling
1	1	–
2	–	S
3	0	–
4	–	S

Note – For multiframe structure, see § 3.1.3.2.2.

2.1.3.1 *Method 1: Twenty-four-frame multiframe*

Allocation of the F-bit to the multiframe alignment signal, the CRC check bits and the data link is given in Table 1/G.704.

2.1.3.1.1 *Multiframe alignment signal*

The F-bit of every fourth frame forms the pattern 001011 . . . 001011. This multiframe alignment signal is used to identify where each particular frame is located within the multiframe in order to extract the cyclic redundancy check code, CRC-6, and the data link information, as well as to identify those frames that contain signalling (frames 6, 12, 18 and 24), if channel associated signalling is used.

2.1.3.1.2 *Cyclic redundancy check*

The CRC-6 is a method of performance monitoring that is contained within the F-bit position of frames 2, 6, 10, 14 18 and 22 of every multiframe (see Table 1/G.704).

The CRC-6 message block check bits e_1, e_2, e_3, e_4, e_5, and e_6 are contained within multiframe bits 194, 966, 1738, 2510, 3282 and 4054 respectively, as shown in Table 1/G.704. The CRC-6 Message Block (CMB) is a sequence of 4632 serial bits that is coincident with a multiframe. By definition, CMB N begins at bit position 1 of multiframe N and ends at bit position 4632 of multiframe N. The first transmitted CRC bit of a multiframe is the most significant bit of the CMB polynomial.

In calculating the CRC-6 bits, the F-bits are replaced by binary 1s. All information in the other bit positions will be identical to the information in the corresponding multiframe bit positions.

The check-bit sequence e_1 through e_6 transmitted in multiframe N+1, is the remainder after multiplication by x^6 and then division (modulo-2) by the generator polynomial x^6+x+1 of the polynomial corresponding to CMB N. The first check bit (e_1) is the most significant bit of the remainder; the last check bit (e_6) is the least significant bit of the remainder. Each multiframe contains the CRC-6 check bits generated for the preceding CMB.

At the receiver, the received CMB, with each F-bit having first been replaced by a binary 1, is acted upon by the multiplication/division process described above. The resulting remainder is compared on a bit-by-bit basis, with the CRC-6 check bits contained in the subsequently received multiframe. The compared check bits will be identical in the absence of transmission errors.

2.1.3.1.3 *4 kbit/s data link*

Beginning with frame 1 of the multiframe (see Table 1/G.704) the first bit of every other frame is part of the 4 kbit/s data link. This data link provides a communication path between primary hierarchical level terminals and will contain data, an idle data link sequence or a loss of frame alignment alarm sequence.

The format to be used for the transmission of data over them-bits of the data link is still under study.

The idle data link pattern is also under study.

A loss of frame alignment alarm sequence is used when a loss of frame alignment (LFA) condition has been detected. After a loss of frame alignment condition is detectd at local end A, a 16-bit LFA sequence of eight 1s eight 0s (1111111100000000) will be transmitted in the m-bits of the 4 kbit/s data link continuously to remote end B.

2.1.3.2 *Method 2: Twelve-frame multiframe*

Allocation of the F-bit to the frame alignment signal, multiframe alignment signal and signalling is given in Table 2/G.704.

2.2 *Basic frame structure at 6312 kbit/s*

2.2.1 *Frame length*

The number of bits per frame is 789. The frame repetition rate is 8000 Hz.

2.2.2 *F-bits*

The last five bits of a frame are designated as F-bits, and are used for such purposes as frame alignment, performance monitoring and providing a data link.

2.2.3 *Allocation of F-bits*

Allocation of the F-bits is given in Table 3/G.704.

TABLE 3/G.704

Allocation of F-bits

Frame number	Bit number				
	785	786	787	788	789
1	1	1	0	0	*m*
2	1	0	1	0	0
3	*x*	*x*	*x*	*a*	*m*
4	e_1	e_2	e_3	e_4	e_5

m Data link bit.
a Remote end alarm bit (1 state = alarm, 0 state = no alarm).
e_i CRC-5 check bit (i = 1 to 5).
x Spare bits, to be set at state 1 if not used.

2.2.3.1 *Frame alignment signal*

The frame and multiframe alignment signal is 110010100, and is carried on the F-bits in frames 1 and 2, excluding bit 789 of frame 1.

2.2.3.2 *Cyclic redundancy check*

The cyclic redundancy check 5 (CRC-5) message block (CMB) is a sequence of 3151 serial bits which starts at bit number 1 of frame number 1 and ends at bit number 784 of frame number 4. The CRC-5 message block check bits e_1, e_2, e_3, e_4 and e_5 occupy the last five bits of the multiframe as shown in Table 3/G.704.

The check-bit sequence e_1 through e_5 transmitted in multiframe N is the remainder after multiplication by x^5 and then division (modulo-2) by the generator polynomial $x^5+x^4+x^2+1$ of the polynomial corresponding to CMB N. The first check bit (e_1) is the most significant bit of the remainder; the last check bit (e_5) is the least significant bit of the remainder. Each multiframe contains the CRC-5 check bits generated for the corresponding CMB.

At the receiver the incoming sequence of 3156 serial bits (i.e. 3151 bits of CMB and 5 CRC bits), when divided by the generator polynomials, will result in a remainder of 00000 in the absence of transmission errors.

2.2.3.3 *4 kbit/s data link*

The bit *m* shown in Table 3/G.704 is used as a data link bit. These bits provide 4 kbit/s data transmission capability associated with the 6312 kbit/s digital path.

2.2.3.4 *Remote end alarm indication*

After a loss of frame alignment condition is detected at local end A, remote end alarm signal bit *a*, shown in Table 3/G.704, will be transmitted to remote end B.

2.3 *Basic frame structure at 2048 kbit/s*

2.3.1 *Frame length*

256 bits, numbered 1 to 256. The frame repetition rate is 8000 Hz.

2.3.2 *Allocation of bits number 1 to 8 of the frame*

Allocation of bits number 1 to 8 of the frame is shown in Table 4a/G.704.

TABLE 4a/G.704

Allocation of bits 1 to 8 of the frame

Alternate frames \ Bit number	1	2	3	4	5	6	7	8
Frame containing the frame alignment signal	S_i	0	0	1	1	0	1	1
	Note 1	Frame alignment signal						
Frame not containing the frame alignment signal	S_i	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
	Note 1	Note 2	Note 3	Note 4				

Note 1 – S_i = bits reserved for international use. One specific use is described in § 2.3.3. Other possible uses may be defined at a later stage. If no use is realized, these bits should be fixed at 1 on digital paths crossing an international border. However, they may be used nationally if the digital path does not cross a border.

Note 2 – This bit is fixed at 1 to assist in avoiding simulations of the frame alignement signal.

Note 3 – A = Remote alarm indication. In undisturbed operation, set to 0; in alarm condition, set to 1.

Note 4 – S_{a4} to S_{a8} = Additional spare bits whose use may be as follows:

i) Bits S_{a4} to S_{a8} may be recommended by CCITT for use in specific point-to-point applications (e.g. transcoder equipments conforming to Recommendation G.761;

ii) Bit S_{a4} may be recommended by CCITT as a message-based data link for operations, maintenance and performance monitoring. This channel originates at the point where the frame is generated and terminates where the frame is split up. This requires further study;

iii) Bits S_{a5} to S_{a7} are for national usage where there is no demand on them for specific point-to-point applications (see i) above.

Bits S_{a4} to S_{a8} (where these are not used) should be set to 1 on links crossing an international border.

2.3.3 *Description of the CRC-4 procedure in bit 1 of the frame*

2.3.3.1 *Special use of bit 1 of the frame*

Where there is a need to provide additional protection against simulation of the frame alignment signal, and/or where there is a need for an enhanced error monitoring capability, then bit 1 should be used for a Cyclic Redundancy Check-4 (CRC-4) procedure as detailed below.

Note – Equipment incorporating the CRC-4 procedure should be designed to be capable of interworking with equipment which does not incorporate the CRC procedure, with the option being manually selectable (e.g. by straps). For such interworking, bit 1 of the frame should be fixed at 1 in both directions (see Table 4a/G.704, Note 1).

2.3.3.2 *The allocation of bits 1 to 8 of the frame is shown in Table 4b/G.704 for a complete CRC-4 multiframe.*

TABLE 4b/G.704

CRC-4 multiframe structure

	Sub-multiframe (SMF)	Frame number	Bits 1 to 8 of the frame							
			1	2	3	4	5	6	7	8
Multiframe	I	0	C_1	0	0	1	1	0	1	1
		1	0	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
		2	C_2	0	0	1	1	0	1	1
		3	0	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
		4	C_3	0	0	1	1	0	1	1
		5	1	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
		6	C_4	0	0	1	1	0	1	1
		7	0	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
	II	8	C_1	0	0	1	1	0	1	1
		9	1	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
		10	C_2	0	0	1	1	0	1	1
		11	1	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
		12	C_3	0	0	1	1	0	1	1
		13	E	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
		14	C_4	0	0	1	1	0	1	1
		15	E	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}

Note 1 – E = CRC-4 error indication bits (voir le § 2.3.3.4).

Note 2 – S_{a4} to S_{a8} = Spare bits (see Note 4 to Table 4a/G.704).

Note 3 – C_1 à C_4 = Cyclic Redundancy Check-4 (CRC-4) bits (see §§ 2.3.3.4 and 2.3.3.5).

Note 4 – A = Remote alarm indication (see Table 4a/G.704).

2.3.3.3 Each CRC-4 multiframe, which is composed of 16 frames numbered 0 to 15, is divided into two 8-frame sub-multiframes (SMF), designated SMF I and SMF II which signifies their respective order of occurrence within the CRC-4 multiframe structure. The SMF is the Cyclic Redundancy Check-4 (CRC-4) block size (i.e. 2048 bits).

The CRC-4 multiframe structure is not related to the possible use of a multiframe structure in 64 kbit/s channel time slot 16 (see § 5.1.3.2).

2.3.3.4 *Use of bit 1 in 2048 kbit/s CRC-4 multiframe*

In those frames containing the frame alignment signal (defined in § 2.3.2), bit 1 is used to transmit the CRC-4 bits. There are four CRC-4 bits, designated C_1, C_2, C_3 and C_4 in each SMF.

In those frames not containing the frame alignment signal (see § 2.3.2), bit 1 is used to transmit the 6-bit CRC-4 multiframe alignment signal and two CRC-4 error indication bits (E).

The CRC multiframe alignment signal has the form 001011.

The E-bits should be used to indicate received errored sub-multiframes by setting the binary state of one E-bit from 1 to 0 for each errored sub-multiframe. Any delay between the detection of an errored sub-multiframe and the setting of the E-bit that indicates the error state must be less than 1 second.

Note 1 – The E-bits will always be taken into account even if the SMF which contains them is found to be errored, since there is little likelihood that the E-bits themselves will be errored.

Note 2 – In the short term, there may exist equipments which do not use the E-bits; in this case the E-bits are set to binary 1.

2.3.3.5 *Cyclic Redundancy Check*

2.3.3.5.1 *Multiplication/division process*

A particular CRC-4 word, located in sub-multiframe N, is the remainder after multiplication by x^4 and then division (modulo 2) by the generator polynomial $x^4 + x + 1$, of the polynomial representation of sub- multiframe $N-1$).

Note – When representing the contents of the check block as a polynomial, the first bit in the block, i.e. frame 0, bit 1 or frame 8, bit 1, should be taken as being the most significant bit. Similarly, C_1 is defined to be the most significant bit of the remainder and C_4 the least significant bit of the remainder.

2.3.3.5.2 *Encoding procedure*

i) The CRC-4 bits in the SMF are replaced by binary 0s.

ii) The SMF is then acted upon by the multiplication/division process referred to in § 2.3.3.5.1.

iii) The remainder resulting from the multiplication/division process is stored, ready for insertion into the respective CRC-4 locations of the next SMF.

Note – The CRC-4 bits thus generated do not affect the result of the multiplication/division process in the next SMF because, as indicated in i) above, the CRC-4 bit positions in an SMF are initially set to 0 during the multiplication/division process.

2.3.3.5.3 *Decoding procedure*

i) A received SMF is acted upon by the multiplication/division process referred to in § 2.3.3.5.1, after having its CRC-4 bits extracted and replaced by 0s.

ii) The remainder resulting from this division process is then stored and subsequently compared on a bit-by-bit basis with the CRC bits received in the next SMF.

iii) If the remainder calculated in the decoder exactly corresponds to the CRC-4 bits received in the next SMF, it is assumed that the checked SMF is error free.

2.4 *Basic frame structure at 8448 kbit/s*

2.4.1 *Frame length*

The number of bits per frame is 1056. They are numbered from 1 to 1056. The frame repetition rate is 8000 Hz.

2.4.2 *Frame alignment signal*

The frame alignment signal is 11100110 100000 and occupies the bit-positions 1 to 8 and 529 to 534.

2.4.3 *Service digits*

Bit 535 is used to convey alarm indication (bit 535 at 1 state – alarm; bits 535 at 0 state = no alarm).

Bit 536 is left free for national use and should be fixed at 1 on paths crossing the international border. The same applies to bits 9-40 in the case of channel-associated signalling.

3 Characteristics of frame structure carrying channels at various bit rates in 1544 kbit/s

3.1 *Interface at 1544 kbit/s carrying 64 kbit/s channels*

3.1.1 *Frame structure*

3.1.1.1 *Number of bits per 64 kbit/s channel time slot*

Eight, numbered 1 to 8.

3.1.1.2 *Number of 64 kbit/s channel time slots per frame*

Bits 2 to 193 in the basic frame carry 24 octet interleaved 64 kbit/s channel time slots, numbered 1 to 24.

3.1.1.3 *Allocation of F-bit*

Refer to § 2.1.3.

3.1.2 *Use of 64 kbit/s channel time slots*

Each 64 kbit/s channel time slot can accommodate e.g., a PCM encoded voiceband signal conforming to Rec. G.711 or data information with a bit rate up to 64 kbit/s.

3.1.3 *Signalling*

Two alternative methods as given in §§ 3.1.3.1 and 3.1.3.2 are recommended:

3.1.3.1 *Common channel signalling*

One 64 kbit/s channel time slot is used to provide common channel signalling at a rate of 64 kbit/s. In the case of the 12-frame multiframe method of § 2.1.3.2, the pattern of the S-bitmay be arranged to carry common channel signalling at a rate of 4 kbit/s or a sub-multiple of this rate.

3.1.3.2 *Channel associated signalling*

3.1.3.2.1 *Allocation of signalling bits for the 24-frame multiframe*

As can be seen in Table 1/G.704, there are four different signalling bits (A, B, C and D) in the multiframe. This channel associated signalling can provide four independent 333-bit/s signalling channels designated A, B, C and D, two independent 667-bit/s signalling channels designated A and B (see Note,) or one 1333-bit/s signalling channel.

Note – When only four state signalling is required, the A, B signalling bits previously associated with frames 6 and 12 respectively should be mapped into the A, B, C, D signalling bits of frames 6, 12, 18 and 24 respectively as follows: A=A, B=B, C=A, D=B. In this case the ABCD signalling is the same as the AB signalling specified in § 3.1.3.2.2.

3.1.3.2.2 *Allocation of signalling bits for the 12-frame multiframe*

Based on agreement between the Administrations involved, channel-associated signalling is provided for intra-regional circuits according to the following arrangement:

A multiframe comprises 12 frames as shown in Table 5/G.704. The multiframe alignment signal is carried on the S-bit as shown in the table.

Frames 6 and 12 are designated as signalling frames. The eight bit in each channel time slot is used in every signalling frame to carry the signalling associated with that channel.

TABLE 5/G.704

Multiframe structure

Frame number	Frame alignment signal (see Note 1)	Multiframe alignment signal (S bit)	Bit number(s) in each channel time slot		Signalling channel designation (see Note 2)
			For character signal	For signalling	
1	1	–	1-8	–	
2	–	0	1-8	–	
3	0	–	1-8	–	
4	–	0	1-8	–	
5	1	–	1-8	–	
6	–	1	1-7	8	A
7	0	–	1-8	–	
8	–	1	1-8	–	
9	1	–	1-8	–	
10	–	1	1-8	–	
11	0	–	1-8	–	
12	–	0	1-7	8	B

Note 1 – When the S-bit is modified to signal the alarm indications to the remote end, the S-bit in frame 12 is changed from state 0 to 1.

Note 2 – Channel associated signalling provides two independent 667-bit/s signalling channels designated A and B or one 1333-bit/s signalling channel.

3.2 *Interface at 1544 kbit/s carrying 32 kbit/s channel time slots* (see Note)

Note – This interface provides for the carrying of 32 kbit/s information. The interface will be used between network nodes and will apply to primary rate multiplexing equipment, digital cross-connect equipment, transcoder and other equipment relevant to the network nodes. Switching in this case is assumed to take place on a 64 kbit/s basis.

3.2.1 *Frame structure*

3.2.1.1 *Number of bits per 32 kbit/s channel time slot*

Four, numbered 1 to 4.

3.2.1.2 *Number of 32 kbit/s channel time slots per frame*

Bits 2 to 193 in the basic frame can carry forty-eight 4-bit interleaved 32 kbit/s channel time slots, numbered 1 to 48.

3.2.1.3 *Allocation of F-bits*

Refer to § 2.1.3.

3.2.2 Use of 32 kbit/s channel time slot

Each 32 kbit/s channel time slot can accomodate an ADPCM-encoded voiceband signal conforming to Rec. G.721, or data with a bit rate up to 32 kbit/s.

3.2.3 *384 kbit/s 12-channel time slot grouping*

3.2.3.1 *Structure of 12-channel time slot grouping*

The 1544 kbit/s frame for 32 kbit/s channel time slots shown in Table 6/G.704 is structured to provide four independent 384 kbit/s 12-channel time slot groupings. These are numbered 1-4, and transmitted in numbered order starting with time slot grouping number 1.

The signalling grouping channels (SGC) for time slot groupings 1-4, occupy time slots 12, 24, 36 and 48 respectively. Each time slot grouping can be independently configured for situations requiring channel associated signalling or situations with no signalling requirement (e.g. external common signalling). (See § 3.2.3.1.1.)

TABLE 6/G.704

32 kbit/s channel time slots frame structure for 1544 kbit/s interface

Time slot grouping	Time slots												
No. 1	1	2	3	4	5	6	7	8	9	10	11	12	(SGC)
No. 2	13	14	15	16	17	18	19	20	21	22	23	24	(SGC)
No. 3	25	26	27	28	29	30	31	32	33	34	35	36	(SGC)
No. 4	37	38	39	40	41	42	43	44	45	46	47	48	(SGC)

Note 1 – Each time slot signifies a 32 kbit/s channel.

Note 2 – The signalling grouping channel (SGC) occupies the twelfth 32 kbit/s time slot of each time slot grouping.

3.2.3.1.1 *Use of a 384 kbit/s time slot grouping*

Use of a 384 kbit/s time slot grouping is categorized into two possible configurations:

– When no signalling capabilities are required, a 384 kbit/s time slot grouping can carry twelve 32 kbit/s channel time slots;

– When channel associated signalling capabilities are required, a 384 kbit/s time slot grouping will consist of eleven 32 kbit/s channel time slots and a 32 kbit/s channel time slot defined as a signalling grouping channel.

3.2.3.1.2 *Use of a signalling grouping channel*

A signalling grouping channel is used for the transmission of channel associated A-B-C-D signalling information, signalling grouping channel alarm information, the signalling grouping channel multiframe alignment signal, and CRC-6 error detection information between network nodes.

3.2.4 *32 kbit/s signalling grouping channel multiframe structure*

3.2.4.1 *Number of bits per 32 kbit/s signalling grouping channel time slot*

Four, numbered 1 to 4.

3.2.4.2 *Bit allocation of 32 kbit/s signalling grouping channel time slot*

Allocated to the last four bits of each time slot grouping.

3.2.4.3 *Multiframe structure*

The signalling grouping channel multiframe structure consists of 24 consecutive frames numbered 1 to 24. Table 7/G.704 shows the signalling grouping channel multiframe structure.

TABLE 7/G.704

32 kbit/s signalling grouping channel multiframe structure

Time slot grouping frame number	Signalling grouping channel bit number			
	1	2	3	4
1	A_j	A_{j+1}	0	S_1
2	A_{j+2}	A_{j+3}	1	S_2
3	A_{j+4}	A_{j+5}	0	CRC-1
4	A_{j+6}	A_{j+7}	1	S_4
5	A_{j+8}	A_{j+9}	0	S_5
6	A_{j+10}	M_1	1	S_6
7	B_j	B_{j+1}	0	CRC-2
8	B_{j+2}	B_{j+3}	1	S_8
9	B_{j+4}	B_{j+5}	0	S_9
10	B_{j+6}	B_{j+7}	1	S_{10}
11	B_{j+8}	B_{j+9}	0	CRC-3
12	B_{j+10}	M_2	1	S_{12}
13	C_j	C_{j+1}	1	S_{13}
14	C_{j+2}	C_{j+3}	0	S_{14}
15	C_{j+4}	C_{j+5}	1	CRC-4
16	C_{j+6}	C_{j+7}	0	S_{16}
17	C_{j+8}	C_{j+9}	1	S_{17}
18	C_{j+10}	M_2	0	S_{18}
19	D_j	D_{j+1}	1	CRC-5
20	D_{j+2}	D_{j+3}	0	S_{20}
21	D_{j+4}	D_{j+5}	1	S_{21}
22	D_{j+6}	D_{j+7}	0	S_{22}
23	D_{j+8}	D_{j+9}	1	CRC-6
24	D_{j+10}	M_4	0	S_{24}

Note 1 – $_j = 1$ for 12th 32 kbit/s channel time slot

$_j = 13$ for 24th 32 kbit/s channel time slot

$_j = 25$ for 36th 32 kbit/s channel time slot

$_j = 37$ for 48th 32 kbit/s channel time slot

Note 2 – (A_j, B_j, C_j, D_j): A, B, C, D signalling bits

M_j: Signalling grouping channel alarm indication bits

S_k: Spare bits

Note 3 – The signalling grouping channel provides A, B, C, D signalling capability for 11 channels within each time slot grouping.

3.2.4.4 *Signalling grouping channel multiframe alignment signal*

Bit 3 of the signalling grouping channel, as shown in Table 7/G.704, contains the signal grouping channel multiframe alignment signal used to associate the signalling bits in the signal grouping channel with the proper channels of the associated time slot grouping.

Note – The signalling grouping channel multiframe alignment signal is independent of, and different from, the framing bit of the 1544 kbit/s frame.

3.2.4.5 *CRC-6 error detection information for the time slot grouping*

An optional 2 kbit/s CRC-6 error detection code word may be transmitted in the bit position indicated by CRC-1 through CRC-6 in Table 7/G.704.

The CRC-6 message block (CMB) is a sequence of 1152 serial bits that is concident with a time slot grouping multiframe. By definition, CMB *N* begins at bit position 0 of time slot grouping multiframe *N* and ends at bit position 1151 of time slot grouping multiframe *N*.

The check-bit sequence CRC-1 through CRC-6 transmitted in multiframe $N + 1$ is the remainder after multiplication by x^6, and then division (modulo 2) by the generator polynomial $x^6 + x + 1$ of the the polynomial corresponding to CMB *N*. The first check bit, CRC-1, is the most significant bit of the remainder; the last check bit CRC-6, is the least significant bit. The time slot grouping channel is included in this calculation with bit 4 of the time slot grouping channel being set to 1.

When not utilizing the option to transmit the CRC-6 error detection signal, CRC-1 through CRC-6 shall be set to 1.

3.2.4.6 *Signalling*

Two alternative methods as given in §§ 3.2.4.6.1 and 3.2.4.6.2 are recommended.

3.2.4.6.1 *Common channel signalling*

Refer to § 3.1.3.1. Two successive 32 kbit/s channel time slots are used for 64 kbit/s common channel signalling transmission.

3.2.4.6.2 *Channel associated signalling*

As indicated in Table 7/G.704, bits 1 and 2 of the signalling grouping channel convey the channel associated signalling information for the channels of the associated time slot grouping.

The signalling grouping channel can provide four independent 333 bit/s signalling channels designated A, B, C and D, two independent 667 bit/s signalling channels designated A and B, or one 1333 bit/s signalling channel designated A. Where only A-B signalling is used, the A-B signalling is repeated for the C-D positions respectively. Where only A signalling is used, the A signalling is repeated for the B-C-D positions respectively.

3.2.4.7 *Signalling grouping channel alarm indication signals*

As indicated in Table 7/G.704, the signalling grouping channel contains four alarm indication bits, M_1, M_2, M_3 and M_4.

M_1 provides the capability to transmit through the interface a remote time slot grouping alarm indication of a failure in the opposite direction of transmission.

M_2 provides the capability to transmit through the interface an indication of a failure in tributary input signals to the network node.

M_3 provides the capability to transmit through the interface an indication of a failure in tributary output signals from the network node.

M_4 is set to 1 whenever M_1 and/or M_2 and/or M_3 are set to 1.

3.2.5 *Signal grouping channel unused bits*

The bits marked S in Table 7/G.704 are currently unused and set to 1. The definition and allocation of the S-bits are for further study.

3.2.6 *Loss and recovery of signalling channel multiframe alignment*

Loss of the signalling grouping channel multiframe alignment signal is declared when two out of four signalling grouping channel framing bits are in error. The rare occurrence of a single instantaneous slip of ± 11 frames is undetected by the two-out-of-four algorithm. Signalling grouping channel multiframe alignment shall be declared when the correct sequence of 24 valid signalling grouping channel framing bits is detected, beginning with the first frame of the multiframe.

3.3 *Interface at 1544 kbit/s carrying n × 64 kbit/s*

Electrical characteristics should follow Recommendation G.703.

The time slot mapping to the 1544 kbit/s interface is for further study.

4 Characteristics of frame structures carrying channels at various bit rates in 6312 kbit/s interfaces

4.1 *Interface at 6312 kbit/s carrying 64 kbit/s channels*

4.1.1 *Frame structure*

4.1.1.1 *Number of bits per 64 kbit/s channel time slot*

Eight, numbered 1 to 8.

4.1.1.2 *Number of 64 kbit/s channel time slots per frame*

Bits 1 to 784 in the basic frame carry 98 octet interleaved 64 kbit/s channel time slots, numbered 1 to 98. Five bits per frame (F-bits are added at the end of the frame for the frame alignment signal and for other signals.

4.1.1.3 *Allocation of the F-bits*

Refer to Table 3/G.704.

4.1.2 *Use of 64 kbit/s channel time slots*

Each 64 kbit/s channel time slot can accomodate e.g., a PCM-encoded voiceband signal conforming to Recommendation G.711 or data information with a bit rate up to 64 kbit/s. 64 kbit/s channel time slots 97, 98 may be used for signalling.

4.1.3 *Signalling*

Two alternative methods as given in §§ 4.1.3.1 and 4.1.3.2 are recommended.

4.1.3.1 *Common channel signalling*

Use of 64 kbit/s channel time slots 97 and 98 for common channel signalling is under study.

4.1.3.2 *Channel associated signalling*

Based on agreement between the Administrations concerned, channel associated signalling is provided for intra-regional circuits according to the following arrangement:

4.1.3.2.1 *Allocation of signalling bit*

Sixteen signalling bits (bit positions 769 to 784) are designated as ST_1 to ST_{16}. One ST_i-bit (i = 1 to 16) accomodates signalling information corresponding to six channel time slots i, $16 + i$, $32 + i$, $48 + i$, $64 + i$ and $80 + i$ in a manner described in § 4.1.3.2.2 below.

4.1.3.2.2 *Signalling multiframe structure*

Each ST-bit constitutes an independent signalling multiframe over eight frames as shown in Table 8/G.704.

TABLE 8/G.704

Signalling multiframe structure

Frame number	n	n+1	n+2	n+3	n+4	n+5	n+6	n+7
Use of ST-bit	F_s	S_1	S_2	S_3	S_4	S_5	S_6	S_p
	(See Note 1)	(See Note 2)						(See Note 4)

Note 1 – The F_s-bit is either alernate 0, 1 or the following 48 bit digital pattern:

A101011011 0000011001 1010100111 0011110110 10000101

For the 48 bit digital pattern, the A-bit is usually fixed to state 1 and is reserved for optional use. The pattern is generated according to the following primitive polynomial (refer to Recommendation X.50):

$$x^7 + x^4 + 1$$

Note 2 – S_j-bits (j = 1 to 6) carry channel associated signalling or maintenance information. When the 48 bit pattern is adopted as the F_s frame alignment signal, each S_j-bit (j = 1 to 6) can be multiframed, as follows:

$$S_{j1}, S_{j2}, \ldots, S_{j12}$$

The S_{j1}-bit carries the following 16 bit frame alignment pattern generated according to the same primitive polynomial as for the 48 bit pattern.

A011101011011000

The A-bit is usually fixed to 1 and is reserved for optional use. Each S_{ji}-bit (i = 2 to 12) carries channel associated signalling for sub-rate circuits and/or maintenance information.

Note 3 – ST-bits (F_s, S_1, . . ., S_6 and S_p) all at state 1 indicate Alarm Indication Signal (AIS) for six 64 kbit/s channels.

Note 4 – The S_p-bit is usually fixed to state 1. When backward AIS for six 64 kbit/s channels is required to be sent, the S_p is set to state 0.

4.2 *Interfaces at 6312 kbit/s carrying other channels than 64 kbit/s*

For further study.

5 Characteristics of frame structures carrying channels at various bit rates in 2048 kbit/s interfaces

5.1 *Interface at 2048 kbit/s carrying 64 kbit/s channels*

5.1.1 *Frame structure*

5.1.1.1 *Number of bits per 64 kbit/s channel time slot*

Eight, numbered 1 to 8.

5.1.1.2 *Number of 64 kbit/s channel time slots per frame*

Bits 1 to 256 in the basic frame carry 32 octet interleaved time slots numbered 0 to 31.

5.1.1.3 *Allocation of the bits of 64 kbit/s channel time slot 0*

See Table 4a/G.704 (§ 2.3.2).

5.1.2 *Use of other 64 kbit/s channel time slots*

Each of the 64 kbit/s channel time slots 1 to 15 and 17 to 31 can accomodate e.g., a PCM-encoded voiceband signal according to Recommendation G.711 or a 64 kbit/s digital signal.

The 64 kbit/s channel time slot 16 may be used for signalling. If not needed for signalling, in some cases it may be used for a 64 kbit/s channel in the same way as time slots 1 to 15 and 17 to 31.

5.1.3 *Signalling*

The use of 64 kbit/s channel time slot 16 is recommended for either common channel or channel associated signalling as required.

The detailed requirements for the organization of particular signalling systems will be included in the specifications for those signalling systems.

5.1.3.1 *Common channel signalling*

The 64 kbit/s channel time slot 16 may be used for common channel signalling systems up to a rate of 64 kbit/s. The method of obtaining signal alignent will form part of the particular common channel signallling specification.

5.1.3.2 *Channel associated signalling*

This section contains the recommended arrangement for the use of the 64 kbit/s capability of channel time slot 16 for channel associated signalling.

5.1.3.2.1 *Multiframe structure*

A multiframe comprises 16 consecutive frames (whose structure is given in § 5.1.1 above) and these are numbered from 0 to 15.

The multiframe alignment signal is 0000 and occupies digit time slots 1 to 4 of 64 kbit/s channel time slot 16 in frame 0.

5.3.1.2.2 *Allocation of 64-kbit/s channel time slot 16*

When 64 kbit/s channel time slot 16 is used for channel associated signalling, the 64-kbit/s capacity is sub-multiplexed into lower-rate signalling channels using the multiframe alignement signal as a reference.

Details of the bit allocation are given in Table 9/G.704.

5.2 *Interface at 2048 kbit/s carrying n × 64 kbit/s*

Electrical characteristics should follow Recommendation G.703 (see Note 4 of Preamble to G.703). For the accomodation of $n \times 64$ kbit time slots in the 2048 kbit/s frame, two situations are envisaged.

5.2.1 *One n × 64 kbit/s signal on the tributary side of a multiplex equipment*

Time slots of the 2048 kbit/s frame are filled as follows:

TS0: according to § 2.3;

TS16: reserved for the accomodation, if required, of a 64 kbit/s signalling channel.

– If $2 \leq n \leq 15$, TS1 to TSn are filled with $n \times 64$ kbit/s data [see a) of Figure 1/G.704];

– If $15 < n \leq 30$, TS1 to TS15 and TS17 to TS(n+1) are filled with $n \times 64$ kbit/s data [see b) of Figure 1/G.704].

– Remaining time slots are filled with all 1s.

TABLE 9/G.704

Bit allocation of channel associated 64 kbit/s time slot 16 for channel associated signalling

Time slot 16 of frame 0	Time slot 16 of frame 1		Time slot 16 of frame 2		– – –	Time slot 16 of frame 15	
0000 xyxx	abcd Channel 1	abcd Channel 16	abcd Channel 2	abcd Channel 17	– – –	abcd Channel 15	abcd Channel 30

Note 1 – Channel numbers refer to telephone channel numbers. 64 kbit/s channel time slots 1 to 15 and 17 to 31 are assigned to telephone channels numbered from 1 to 30.

Note 2 – This bit allocation provides four 500-bit/s signalling channels designated a, b, c and d for each channel for telephone and other services. With this arrangement, the signalling distortion of each signalling channel introduced by the PCM transmission system, will not exceed ± 2 ms.

Note 3 – When bits b, c or d are not used they should have the values: b = 1, c = 0, d = 1.

It is recommended that the combination 0000 of bits a, b, c and d should not be used for signalling purposes for channels 1-15.

Note 4 – x = spare bit, to be set to 1 if not used.
y = bit used for alarm indication to the remote end. In undisturbed operation, set to 0; in an alarm condition, set to 1.

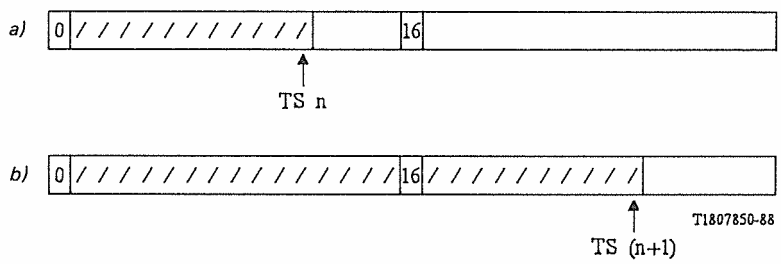

FIGURE 1/G.704

5.2.2 *One or more n × 64 kbit/s signal on the multiplexed signal side of a multiplexing equipment*

For any one $n \times 64$ kbit/s signal, time slots of the 2048 kbit/s frame are filled as follows:

TS0: according to § 2.3;

TS16: reserved for the accomodation, if required, of a 64 kbit/s signalling channel.

TS(x) of the 2048 kbit/s frame is designated as the time slot into which the first time slot of the $n \times 64$ kbit/s is accomodated.

– If $x \leq 15$ and $x + (n–1) \leq 15$, or, if $x \geq 17$ and $x + (n–1) \leq 31$, then the filling of time slots is from TS (x) to TS (x+n–1) [see a)and b) of Figure 2/G.704];

– If $x + (n–1) \geq 16$, then the filling of time slots is from TS (x) to TS15 and TS17 to TS (x+n) (see c) of Figure 2/G.704).

Note – Once $n \times 64$ kbit/s signal has been accomodated into the multiplexed signal, care should be taken in the interpretation of the above rules to ensure that further such signals only use the time slots which remain spare.

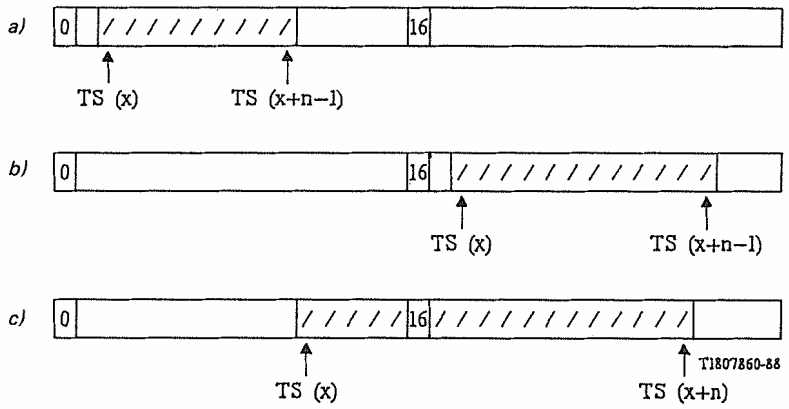

FIGURE 2/G.704

6 Characteristics of frame structures carrying channels at various bit rates in 8448 kbit/s interface

6.1 *Interface at 8448 kbit/s carrying 64 kbit/s channels*

6.1.1 *Frame structure*

6.1.1.1 *Number of bits per 64 kbit/s channel time slot*

Eight, numbered from 1 to 8.

6.1.1.2 *Number of 64 kbit/s channel time time slots per frame*

Bits 1 to 1056 in the basic frame carry 132 octet interleaved 64 kbit/s channel time slots, numbered form 0 to 131.

6.1.2 *Use of 64 kbit/s channel time slots*

6.1.2.1 *64 kbit/s channel time slot assignment in case of channel associated signalling*

64 kbit/s channel time slots 5 to 32, 34 to 65, 71 to 98 and 100 to 131 are assigned to 120 telephone channels from 1 to 120.

64 kbit/s channel time slot 0 and the first 6 bits in 64 kbit/s channel time slot 66 are assigned to framing: the remaining 2 bits in 64 kbit/s channel time slot 66 are devoted to services.

64 kbit/s channel time slots 67 to 70 are assigned to channel associated signalling as covered in § 6.1.4.2 below.

64 kbit/s channel time slots 1 to 4, 33 are left free for national use.

6.1.2.2 *64 kbit/s channel time slot assignment in case of common channel signalling*

64 kbit/s channel time slots 2 to 32, 34 to 65, 67 to 98 and 100 to 131 are available for 127 telephone, signalling or other service channels. By bilateral agreement between the Administrations concerned, 64 kbit/s channel time slot 1 may either be used to provide another telephone or service channel or left free for service purposes within a digital exchange.

The 64 kbit/s channels corresponding to 64 kbit/s channel time slot 1 to 32, 34 to 65 (etc. as above) are numbered 0 to 127.

64 kbit/s channel time slot 0 and the first 6 bits in channel time slot 66 are assigned to framing, the remaining 2 bits in 64 kbit/s channel time slot 66 are assigned to service.

64 kbit/s channel time slots 67 to 70 are, in descending order of priority, available for common channel signalling as covered in § 6.1.4.1 below.

64 kbit/s channel slot 33 is left free for national use.

6.1.3 *Description of the CRC procedure in 64 kbit/s channel time slot 99*

In order to provide an end-to-end quality monitoring of the 8 Mbit/s link, a CRC-6 procedure is used and the six bits C_1 to C_6 computed at the source location are inserted in bit positions 1 to 6 of the time slot 99 (see Figure 3/G.704).

In addition, bit 7 of this time slot, denoted E, is used to send in the transmitting direction an indication about the received signal arriving from the opposite direction. Bit E indicates whether or not the most recent CRC block arriving at the opposite end had errors.

The CRC-6 bits C_1 to C_6 are computed for each frame. The CRC-6 block size is then 132 octets, i.e. 1056 bits, and the computation is made 8000 times per second.

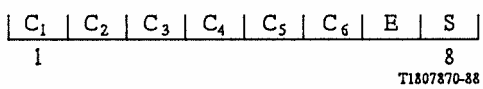

FIGURE 3/G.704

Time slot 99

6.1.3.1 *Multiplication/division process*

A given C_1-C_6 word located in frame N is the remainder after multiplication by x_6 and then division (modulo 2) by the generator polynomial $x_6 + x + 1$ of the polynomial representation of frame (N–1).

Note – When representing the contents of a frame as a polynomial, the first bit in the frame should be taken as being the most significant bit. Similarly C_1 is defined to be the most significant bit of the remainder and C_6 the least significant bit of the remainder.

6.1.3.2 *Encoding procedure*

The CRC bit positions are initially set at 0 i.e.:

$$C_1 = C_2 = C_3 = C_4 = C_5 = C_6 = 0$$

The frame is then acted upon by the multiplication/division process referred to above in § 6.1.3.1.

The remainder resulting from the multiplication/division process is stored ready for insertion into the respective CRC locations of the next frame.

Note – These CRC bits do not affect the computation of the CRC bits in the next frame since the corresponding locations are set to 0 before the computation.

6.1.3.3 *Decoding procedure*

A received frame is acted upon by the multiplication/division process, referred to above in § 6.1.3.1, after having its CRC bits extracted and replaced by 0s.

The remainder resulting from this multiplication/division process is then stored and subsequently compared on a bit by bit basis with the CRC received in the next frame.

If the decoder-calculated remainder exactly corresponds to the CRC bits sent from the encoder, it is assumed that the checked frame is error free.

6.1.3.4 *Action on bit E*

Bit E of frame *N* is set to 1 in the transmitting direction if bits C_1 to C_6 detected in the most recent frame at the opposite end have been found in error (at least one bit in error). If no errors, E is set to 0.

6.1.4 *Signalling*

The use of channel time slots 67 to 70 is recommended for either common channel or channel-associated signalling as required. The detailed requirements for the organization of particular signalling systems will be included in the specifications for those signalling systems.

6.1.4.1 *Common channel signalling*

64 kbit/s channel time slots 67 to 70 may be used for common channel signalling in a descending order of priority up to a rate of 64 kbit/s. The method of obtaining signal alignment will form part of the particular common channel signalling specification.

6.1.4.2 *Channel associated signalling*

The recommended arrangement for the use of the 64 kbit/s capacity in each 64 kbit/s channel time slot 67 to 70 for channel associated signalling is as follows:

6.1.4.2.1 *Multiframe structure*

A multiframe for each 64 kbit/s bit-stream comprises 16 consecutive frames (whose structure is given in § 6.1.1 above) and these are numbered from 0 to 15.

The multiframe alignment signal is 0000 and occupies digit time slots 1 to 4 of channel time slots 67 to 70 in frame 0.

6.1.4.2.2 *Allocation of 64 kbit/s channel time slots 67 to 70*

When 64 kbit/s channel time slots 67 to 70 are used for channel associated signalling, the 64 kbit/s capacity of each of the four 64 kbit/s channel time slots is sub-multiplexed into lower rate signalling channels using the multiframe alignment signal as a reference. Details of the bit allocation are given in Table 10/G.704.

6.2 *Interface at 8448 kbit/s carrying other channels than 64 kbit/s*

For further study.

TABLE 10/G.704

Bit allocation of 64 kbit/s channel time slots 67 to 70

64 kbit/s channel time slot / Frame	67		68		69		70	
0	0000*xyxx*		0000*xyxx*		0000*xyxx*		0000*xyxx*	
1	*abcd* Channel 1	*abcd* Channel 16	*abcd* Channel 31	*abcd* Channel 46	*abcd* Channel 61	*abcd* Channel 76	*abcd* Channel 91	*abcd* Channel 106
. .	. .	. .	. .	. .	. .	. .	. .	. .
15	*abcd* Channel 15	*abcd* Channel 30	*abcd* Channel 45	*abcd* Channel 60	*abcd* Channel 75	*abcd* Channel 90	*abcd* Channel 105	*abcd* Channel 120

Note 1 – Channel numbers refer to telephone channel numbers. Refer to § 6.1.2.1 for the assignment of 64 kbit/s channel time slots to the telephone channels.

Note 2 – This bit allocation provides four 500-bit/s signalling channels designated a, b, c and d for each channel for telephone and other services. With this arrangement, the signalling distortion of each signalling channel introduced by the PCM transmission system, will not exceed ± 2 ms.

Note 3 – When bits b, c or d are not used they should have the values: b = 1, c = 0, d = 1.

It is recommended the the combination 0000 of bits *a*, *b*, *c* and *d* should not be used for signalling purposes for channels 1-15, 31-45, 61-75 and 91-125.

Note 4 – x = spare bit, to be set to 1 if not used.

y = bit used for alarm indication to the remote end. In undisturbed operation, set to 0; in an alarm condition, set to 1.

ANNEX A

(to Recommendation G.704)

Examples of CRC implementations using shift registers

A.1 *CRC-6 procedure for interface at 1544 kbit/s* (Reference: § 2.1.3.1.2)

See Figure A-1/G.704.

Input I to the shift register: CMB *N* with F bits set to 1.

Generator polynomial of the shift register: $x^6 + x + 1$.

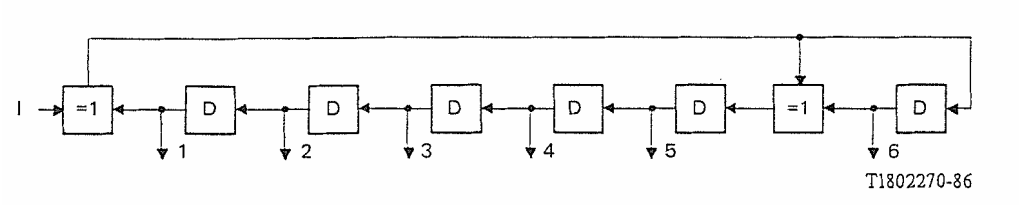

FIGURE A-1/G.704

At I, the CMB is fed serially (i.e. bit by bit) into the circuit, starting with bit number 1 of the multiframe (see Table 1/G.704). When the last bit of the CMB (i.e. bit number 4632 within the multiframe has been fed into the shift register, the CRC bits e_1 to e_6 are available at the outputs 1 to 6. (Output 1 provides the most significant bit, e_1, and output 6 the least significant bit, e_6). Bits e_1 to e_6 are transmitted in the next CMB (c.f. Table 1/G.704).

Note – The outputs (1 to 6) of the shift register stages are reset to 0 after each CMB.

A.2 *CRC-5 procedure for interface at 6312 kbit/s* (Reference: § 2.2.3.2)

Input I to the shift register: CMB *N*.

Generator polynomial of the shift register: $x^5 + x^4 + x^2 + 1$.

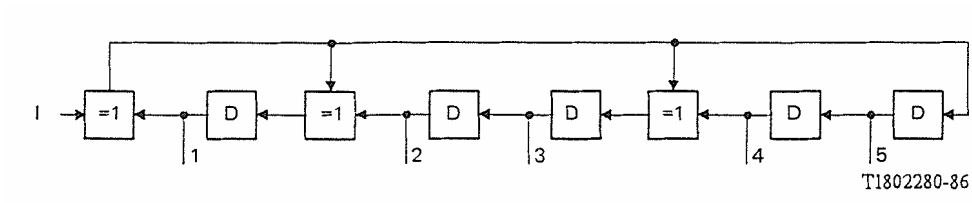

Figure A-2/G.704

At I, the CMB is fed serially (i.e. bit by bit) into the circuit, starting with bit number 1 of frame number 1 (see Table 3/G.704). When the last bit of the CMB (i.e. bit number 784 of frame number 4) has been fed into the the shift register, the CRC bits e_1 to e_5 are available at the outputs 1 to 5. (Output 1 provides the most significant bit, e_1, and output 5 the least significant bit, e_5). Bits e_1 to e_5 are transmitted in the corresponding multiframe (see Table 3/G.704).

Note – The outputs (1 to 5) of the shift register stages are reset to 0 after each CMB.

A.3 *CRC-4 procedure for interface at 2048kbit/s* (Reference: § 2.3.3.5)

See Figure A-3/G.704.

Input I to the shift register: SMF (*N*) with C_1, C_2, C_3, C_4 set to 0.

Generator polynomial of the shift register: $x^4 + x + 1$.

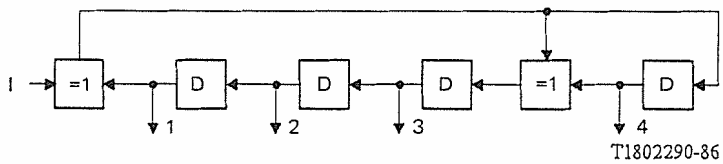

FIGURE A-3/G.704

At I, the SMF is fed serially (i.e. bit by bit) into the circuit, starting with bit $C_1 = 0$ (see Table 4b/G.704). When the last bit of the SMF (i.e. bit number 256 of frame number 7, respectively of frame number 15) has been fed into the shift register, the CRC bits C_1 to C_4 are available at the outputs 1 to 4. (Output 1 provides the most significant bit, C_1, and output 4 the least significant bit, C_4). Bits C_1 to C_4 are transmitted in the next SMF, i.e. SMF(*N*+1).

Note – The outputs (1 to 4) of the shift register stages are reset to 0 after each SMF.

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Printed in Switzerland

Geneva, 2007