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G.703

(10/98)

SERIES G: TRANSMISSION SYSTEMS AND MEDIA, DIGITAL SYSTEMS AND NETWORKS

Digital transmission systems – Terminal equipments – General

Physical/electrical characteristics of hierarchical digital interfaces

ITU-T Recommendation G.703

(Previously CCITT Recommendation)

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ITU-T RECOMMENDATION G.703

PHYSICAL/ELECTRICAL CHARACTERISTICS OF HIERARCHICAL DIGITAL INTERFACES

Summary

This Recommendation specifies the recommended physical and electrical characteristics of the interfaces at hierarchical bit rates as described in Recommendation G.702. The interfaces are defined in terms of general characteristics, specifications at the output ports and input ports and/or cross-connect points, earthing of outer conductor or screen and coding rules.

History

Issue	Notes
10/98	This revision includes a correction to the specification of the 1544 and 44 736 kbit/s interfaces and the addition of Appendix I. Appendix I contains a previous version of the 1544 kbit/s interface specification. The overvoltage protection requirements have been deleted and replaced with a reference to Recommendation K.41 "Resistibility of internal interfaces of telecommunication centres to surge overvoltages". The grounding requirements for the screen (if existing) of a symmetrical pair, or the outer conductor of a coaxial cable have been enhanced. Editorial modifications are included to comply with Recommendation A.3. Clauses 1 to 12 in the 1991 revision are as a consequence renumbered into clauses 4 to 15. Appendix II on 64 and 6312 kHz synchronization interfaces for use in Japan has been added.
1991	Previous revision
1972	Initial version

Source

ITU-T Recommendation G.703 was revised by ITU-T Study Group 15 (1997-2000) and was approved under the WTSC Resolution No. 1 procedure on the 13th of October 1998.

FOREWORD

ITU (International Telecommunication Union) is the United Nations Specialized Agency in the field of telecommunications. The ITU Telecommunication Standardization Sector (ITU-T) is a permanent organ of the ITU. The ITU-T is responsible for studying technical, operating and tariff questions and issuing Recommendations on them with a view to standardizing telecommunications on a worldwide basis.

The World Telecommunication Standardization Conference (WTSC), which meets every four years, establishes the topics for study by the ITU-T Study Groups which, in their turn, produce Recommendations on these topics.

The approval of Recommendations by the Members of the ITU-T is covered by the procedure laid down in WTSC Resolution No. 1.

In some areas of information technology which fall within ITU-T's purview, the necessary standards are prepared on a collaborative basis with ISO and IEC.

NOTE

In this Recommendation the term *recognized operating agency (ROA)* includes any individual, company, corporation or governmental organization that operates a public correspondence service. The terms *Administration, ROA* and *public correspondence* are defined in the *Constitution of the ITU (Geneva, 1992)*.

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As of the date of approval of this Recommendation, the ITU had not received notice of intellectual property, protected by patents, which may be required to implement this Recommendation. However, implementors are cautioned that this may not represent the latest information and are therefore strongly urged to consult the TSB patent database.

CONTENTS

Recommendation G.703

PHYSICAL/ELECTRICAL CHARACTERISTICS OF HIERARCHICAL DIGITAL INTERFACES

(Geneva, 1972; revised 1998)

1 Scope

This Recommendation provides the recommended physical and electrical characteristics of the interfaces at hierarchical bit rates as described in Recommendation G.702, to enable the interconnection of digital network components (digital sections, multiplex equipment, exchanges) to form an international digital link or connection. The characteristics given in this Recommendation should be applied to new equipment (component) designs.

NOTE 1 – The characteristics of interfaces at non-hierarchical bit rates, except $n \times 64$ kbit/s interfaces conveyed by 1544 kbit/s or 2048 kbit/s interfaces, are specified in the respective equipment Recommendations.

NOTE 2 – The jitter specifications contained in the following clauses 9, 10, 11 and 12 are intended to be imposed at international interconnection points.

NOTE 3 – The interfaces described in clauses 5 to 12 correspond to the ports T (output port) and T′ (input port) as recommended for interconnection in CCIR Recommendation AC/9 with reference to Report AH/9 of CCIR Study Group 9. (This Report defines the points T and T′.)

NOTE 4 – For signals with bit rates of $n \times 64$ kbit/s (n = 2 to 31) which are routed through multiplexing equipment specified for the 2048 kbit/s hierarchy, the interface shall have the same physical/electrical characteristics as those for the 2048 kbit/s interface specified in clause 9. For signals with bit rates of $n \times 64$ kbit/s (n = 2 to 23) which are routed through multiplexing equipment specified for the 1544 kbit/s hierarchy, the interface shall have the same physical/electrical characteristics as those for the 1544 kbit/s interface specified in clause 5.

NOTE 5 – The specifications contained in this Recommendation are related to the physical interface only (i.e. to characterize the line codes and input/output equipment interfaces); in particular, the required frequency tolerances do not imply overall equipment performances which may be driven by tighter requirements in Recommendations for specific network/equipment applications (e.g. Recommendations G.813 and G.783).

2 References

The following ITU-T Recommendations and other references contain provisions which, through reference in this text, constitute provisions of this Recommendation. At the time of publication, the editions indicated were valid. All Recommendations and other references are subject to revision; all users of this Recommendation are therefore encouraged to investigate the possibility of applying the most recent edition of the Recommendations and other references listed below. A list of the currently valid ITU-T Recommendations is regularly published.

– CCITT Recommendation G.702 (1988), *Digital hierarchy bit rates.*

– ITU-T Recommendation G.704 (1998), *Synchronous frame structures used at 1544, 6312, 2048, 8448 and 44 736 kbit/s hierarchical levels.*

– CCITT Recommendation G.742 (1988), *Second order digital multiplex equipment operating at 8448 kbit/s and using positive justification.*

– CCITT Recommendation G.747 (1988), *Second order digital multiplex equipment operating at 6312 kbit/s and multiplexing three tributaries at 2048 kbit/s.*

– CCITT Recommendation G.751 (1988), *Digital multiplex equipments operating at the third order bit rate of 34 368 kbit/s and the fourth order bit rate of 139 264 kbit/s and using positive justification.*

– CCITT Recommendation G.752 (1980), *Characteristics of digital multiplex equipment based on a second order bit rate of 6312 kbit/s and using positive justification.*

– CCITT Recommendation G.753 (1988), *Third order digital multiplex equipment operating at 34 368 kbit/s and using positive/zero/ negative justification.*

– CCITT Recommendation G.755 (1988), *Digital multiplex equipment operating at 139 264 kbit/s and multiplexing three tributaries at 44 736 kbit/s.*

– ITU-T Recommendation K.27 (1996), *Bonding configurations and earthing inside a telecommunication building.*

– ITU-T Recommendation K.41 (1998), *Resistibility of internal interfaces of telecommunication centres to surge overvoltages.*

– IEC 60469-2, *Pulse techniques and apparatus. Part 2: Pulse measurement and analysis, general considerations.*

– CCITT Handbook (1976), *Earthing of Telecommunication Installations.*

3 Abbreviations

This Recommendation uses the following abbreviations:

AIS Alarm Indication Signal

AMI Alternate Mark Inversion

B3ZS Bipolar with three-Zero Substitution

B8ZS Bipolar with eight-Zero Substitution

CMI Coded Mark Inversion

HDB2 High Density Bipolar of order 2 code

HDB3 High Density Bipolar of order 3 code

ZBTSI Zero Byte Time Slot Interchange

4 Interface at 64 kbit/s

4.1 Functional requirements

The following basic requirements for the design of the interface are recommended:

In both directions of transmission, three signals can be carried across the interface:

– 64 kbit/s information signal;

– 64 kHz timing signal;

– 8 kHz timing signal.

NOTE 1 – The 64 kbit/s information signal and the 64 kHz timing signal are mandatory. However, although an 8 kHz timing must be generated by the controlling equipment (e.g. PCM multiplex or time slot access equipment), it should not be mandatory for the subordinate equipment on the other side of the interface to either utilize the 8 kHz timing signal from the controlling equipment or to supply an 8 kHz timing signal.

NOTE 2 – The detection of an upstream fault can be transmitted across the 64 kbit/s interface by transmitting an alarm indication signal (AIS) towards the subordinate equipment.

The interface should be bit sequence independent at 64 kbit/s.

NOTE 3 – An unrestricted 64 kbit/s signal can be transmitted across the interface. However, this does not imply that unrestricted 64 kbit/s paths are realizable on a global basis. This is because some Administrations presently have or are continuing to install extensive networks composed of digital line sections whose characteristics do not permit the transmission of long sequences of 0s. (Recommendation G.733 provides for PCM multiplexes with characteristics appropriate for such digital line sections.) Specifically for octet timed sources, in 1544 kbit/s digital networks it is required that at least one binary 1 should be contained in any octet of a 64 kbit/s digital signal. For a bit stream which is not octet timed no more than 7 consecutive 0s should appear in the 64 kbit/s signal.

NOTE 4 – Although the interface is bit sequence independent, the use of the AIS (all 1s bit pattern) may result in some minor restrictions for the 64 kbit/s source. For example, an all 1s alignment signal could result in problems.

4.1.1 Three types of envisaged interfaces

4.1.1.1 Codirectional interface

The term "codirectional" is used to describe an interface across which the information and its associated timing signal are transmitted in the same direction (see Figure 1).

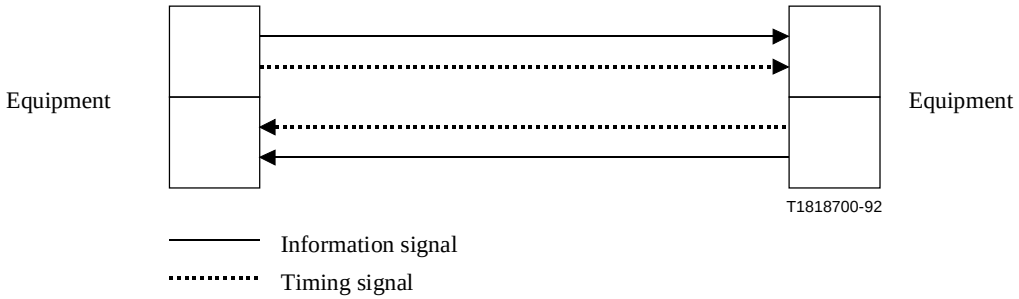


Figure 1/G.703 – Codirectional interface

4.1.1.2 Centralized clock interface

The term "centralized clock" is used to describe an interface wherein for both directions of transmission of the information signal, the associated timing signals are supplied from a centralized clock, which may be derived for example from certain incoming line signals (see Figure 2).

NOTE – The codirectional interface or centralized clock interface should be used for synchronized networks and for plesiochronous networks having clocks of the stability required (see Recommendation G.811) to ensure an adequate interval between the occurrence of slips.

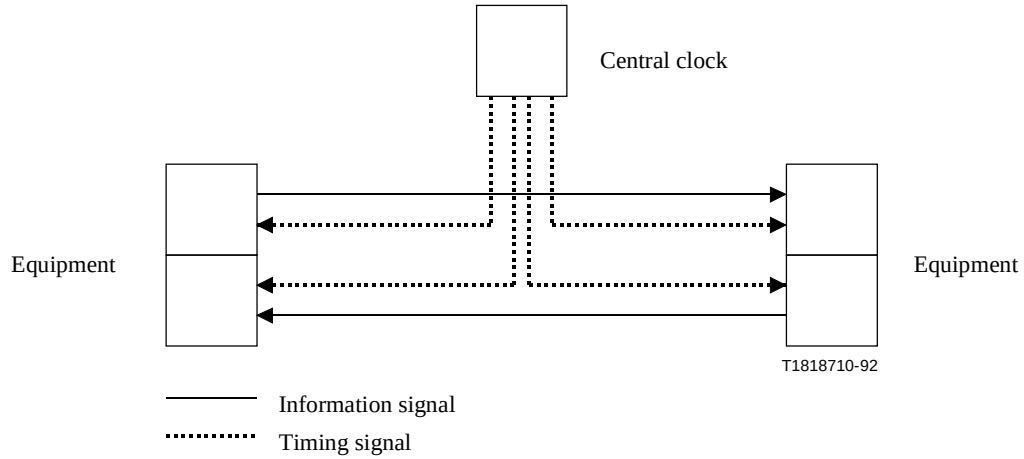


Figure 2/G.703 – Centralized clock interface

4.1.1.3 Contradirectional interface

The term "contradirectional" is used to describe an interface across which the timing signals associated with both directions of transmission are directed towards the subordinate equipment (see Figure 3).

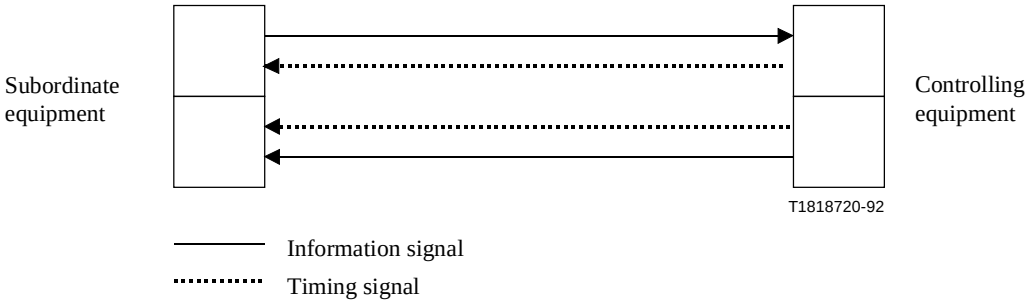


Figure 3/G.703 – Contradirectional interface

4.2 Electrical characteristics

4.2.1 Electrical characteristics of 64 kbit/s codirectional interface

4.2.1.1 General

Nominal bit rate: 64 kbit/s.

Maximum tolerance of signals to be transmitted through the interface: ±100 ppm.

64 kHz and 8 kHz timing signal to be transmitted in a codirectional way with the information signal.

One balanced pair for each direction of transmission; the use of transformers is recommended.

Code conversion rules:

Step 1 – A 64 kbit/s bit period is divided into four unit intervals.

Step 2 – A binary one is coded as a block of the following four bits:

1 1 0 0

Step 3 – A binary zero is coded as a block of the following four bits:

1 0 1 0

Step 4 – The binary signal is converted into a three-level signal by alternating the polarity of consecutive blocks.

Step 5 – The alternation in polarity of the blocks is violated every 8th block. The violation block marks the last bit in an octet.

These conversion rules are illustrated in Figure 4.

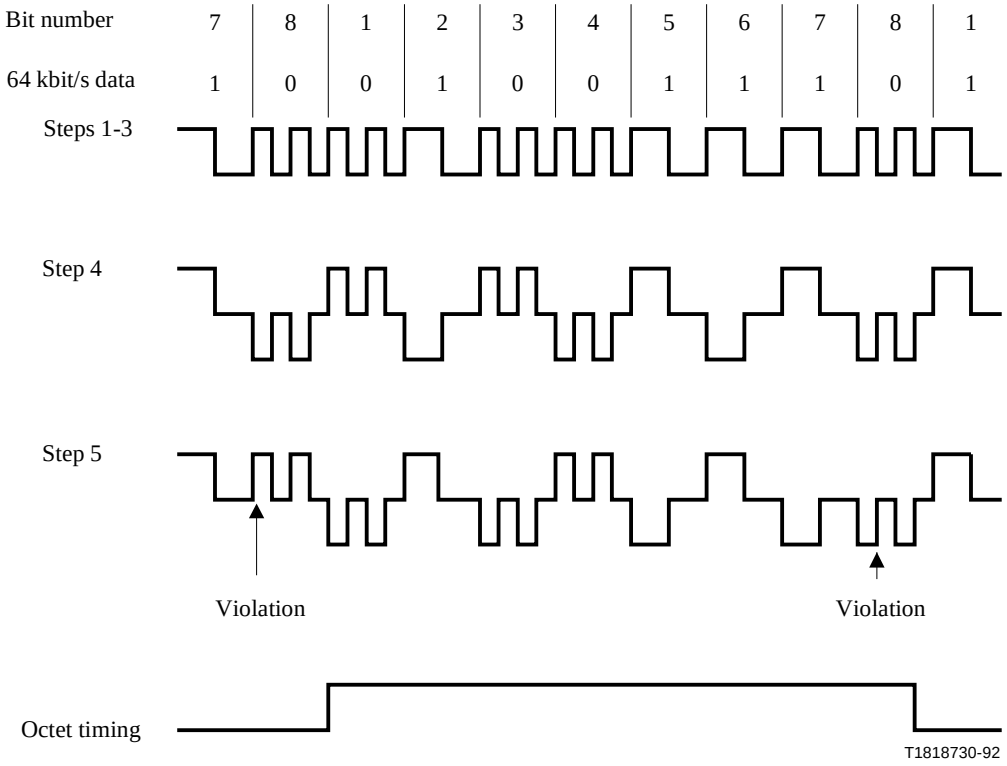


Figure 4/G.703 – Illustration of the conversion rules

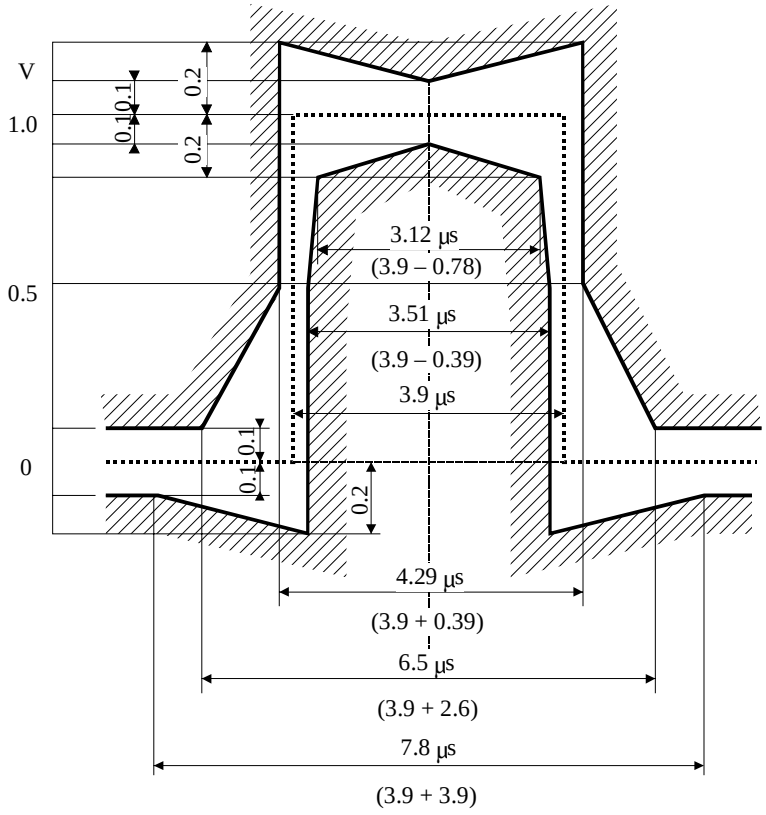
Overvoltage protection requirement: refer to Recommendation K.41.

4.2.1.2 Specifications at the output ports

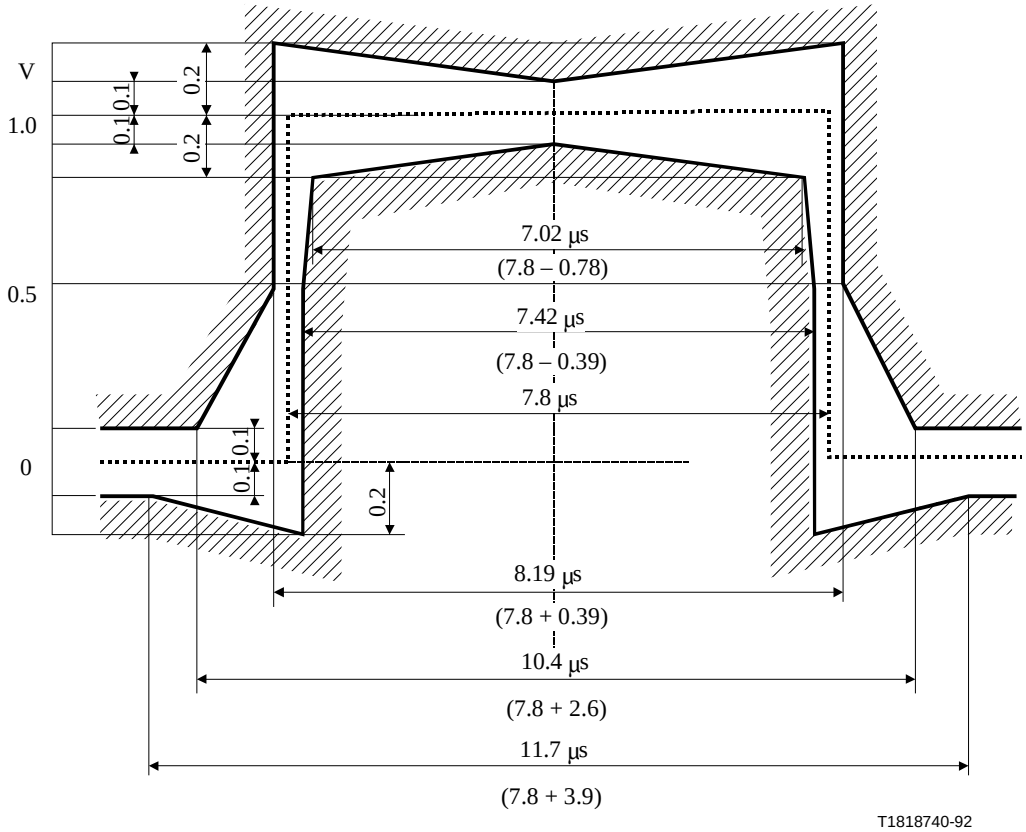
See Table 1.

Table 1/G.703 – Digital 64 kbit/s codirectional interface

Symbol rate	256 kbauds
Pulse shape (nominally rectangular)	All pulses of a valid signal must conform to the masks in Figure 5, irrespective of the polarity
Pair for each direction	One symmetric pair
Test load impedance	120 ohms resistive
Nominal peak voltage of a "mark" (pulse)	1.0 V
Peak voltage of a "space" (no pulse)	0 V ± 0.10 V
Nominal pulse width	3.9 μs
Ratio of the amplitudes of positive and negative pulses at the centre of the pulses interval	0.95 to 1.05
Ratio of the widths of positive and negative pulses at the nominal half amplitude	0.95 to 1.05
Maximum peak-to-peak jitter at the output port (Note)	Refer to clause 2/G.823
NOTE – For the time being these values are valid only for equipments of the 2 Mbit/s hierarchy.	



a) Mask for single pulse



b) Mask for double pulse

NOTE – The limits apply to pulses of either polarity.

Figure 5/G.703 – Pulse masks of the 64 kbit/s codirectional interface

4.2.1.3 Specifications at the input ports

The digital signal presented at the input port shall be as defined above but modified by the characteristics of the interconnecting pairs. The attenuation of these pairs at a frequency of 128 kHz should be in the range 0 to 3 dB. This attenuation should take into account any losses incurred by the presence of a digital distribution frame between the equipments.

The return loss at the input ports should have the following minimum values:

Frequency range (kHz)	Return loss (dB)
4 to 13	12
13 to 256	18
256 to 384	14

To provide nominal immunity against interference, input ports are required to meet the following requirements:

A nominal aggregate signal, encoded as a 64 kbit/s codirectional signal and having a pulse shape as defined in the pulse mask, shall have added to it an interfering signal with the same pulse shape as the wanted signal. The interfering signal should have a bit rate within the limits specified in this Recommendation, but should not be synchronous with the wanted signal. The interfering signal shall be combined with the wanted signal in a combining network, with an overall zero loss in the signal path and with the nominal impedance 120 ohms to give a signal-to-interference ratio of 20 dB. The binary content of the interfering signal should comply with Recommendation O.152 (2^{11} – 1 bit period). No errors shall result when the combined signal, attenuated by up to the maximum specified interconnecting cable loss, is applied to the input port.

4.2.1.4 Grounding of screen

If the symmetrical pair is screened, the screen shall be connected to the bonding network both at the input port and output port.

NOTE 1 – The cable routing is important if leaving the system block. Consult Recommendation K.27 for guidance.

NOTE 2 – The use of isolation to the bonding network is for further study.

4.2.2 Electrical characteristics of the 64 kbit/s centralized clock interface

4.2.2.1 General

Nominal bit rate: 64 kbit/s. The tolerance is determined by the network clock stability (see Recommendation G.811).

For each direction of transmission there should be one symmetrical pair carrying the data signal. In addition, there should be symmetrical pairs carrying the composite timing signal (64 kHz and 8 kHz) from the central clock source to the office terminal equipment. The use of transformers is recommended.

Overvoltage protection requirement: refer to Recommendation K.41.

Code conversion rules:

The data signals are coded in AMI code with a 100% duty ratio. The composite timing signals convey the 64 kHz bit-timing information using AMI code with a 50% to 70% duty ratio and the 8 kHz octet-phase information by introducing violations of the code rule. The structure of the signals and their nominal phase relationships are shown in Figure 6.

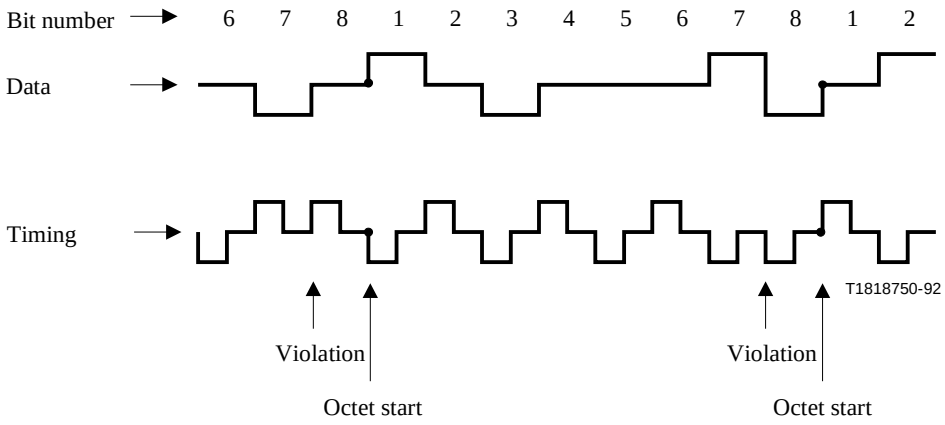


Figure 6/G.703 – Signal structures of the 64-kbit/s central clock interface at office terminal output ports

The data stream at the output ports should be timed by the leading edge of the timing pulse and the detection instant at the input ports should be timed by the trailing edge of each timing pulse.

4.2.2.2 Characteristics at the output ports

See Table 2.

Table 2/G.703 – Digital 64 kbit/s centralized clock interface

Parameters	Data	Timing
Pulse shape	Nominally Rectangular, with rise and fall times less than 1 µs	Nominally Rectangular, with rise and fall times less than 1 µs
Nominal test load impedance	110 ohms resistive	110 ohms resistive
Peak voltage of a "mark" (pulse) (Note 1)	a) 1.0 ± 0.1 V b) 3.4 ± 0.5 V	a) 1.0 ± 0.1 V b) 3.0 ± 0.5 V
Peak value of a "space" (no pulse) (Note 1)	a) 0 ± 0.1 V b) 0 ± 0.5 V	a) 0 ± 0.1 V b) 0 ± 0.5 V
Nominal pulse width (Note 1)	a) 15.6 µs b) 15.6 µs	a) 7.8 µs b) 9.8 to 10.9 µs
Maximum peak-to-peak jitter at the output port (Note 2)	Refer to clause 2/G.823	
NOTE 1 – The choice between the set of parameters a) and b) allows for different office noise environments and different maximum cable lengths between the three involved office equipments. NOTE 2 – For the time being these values are valid only for equipments of the 2 Mbit/s hierarchy.		

4.2.2.3 Characteristics at the input ports

The digital signals presented at the input ports should be as defined above but modified by the characteristics of the interconnecting pairs. The varying parameters in Table 2 will allow typical maximum interconnecting distances of 350 to 450 m.

4.2.2.4 Cable characteristics

The transmission characteristics of the cable to be used are subject to further study.

4.2.3 Electrical characteristics of 64 kbit/s contradirectional interface

4.2.3.1 General

Bit rate: 64 kbit/s.

Maximum tolerance for signals to be transmitted through the interface: ±100 ppm.

For each direction of transmission there should be two symmetrical pairs of wires, one pair carrying the data signal and the other carrying a composite timing signal (64 kHz and 8 kHz). The use of transformers is recommended.

NOTE – If there is a national requirement to provide a separate alarm signal across the interface, this can be done by cutting the 8 kHz timing signal for the transmission direction concerned, i.e. by inhibiting the code violations introduced in the corresponding composite timing signal (see below).

Code conversion rules:

The data signals are coded in AMI code with a 100% duty ratio. The composite timing signals convey the 64 kHz bit-timing information using AMI code with a 50% duty ratio and the 8 kHz octet-phase information by introducing violations of the code rule. The structures of the signals and their phase relationships at data output ports are shown in Figure 7.

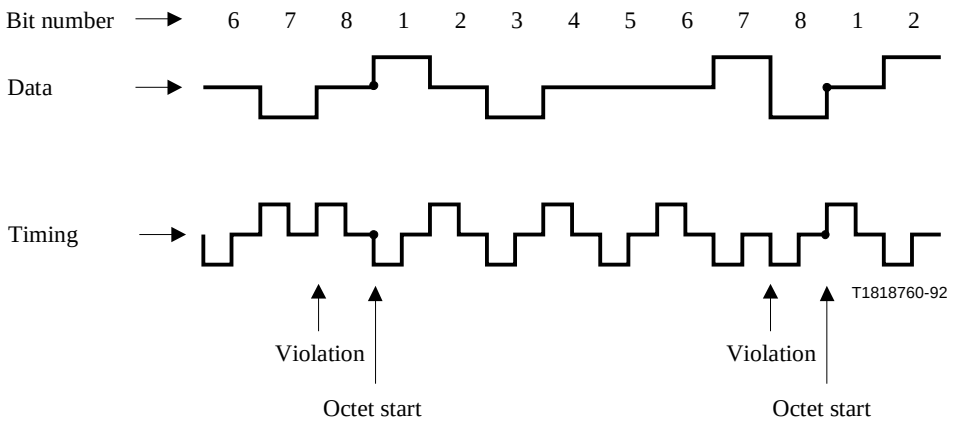


Figure 7/G.703 – Signal structures of the 64-kbit/s contradirectional interface at data output ports

The data pulses received from the service (e.g. data or signalling) side of the interface will be somewhat delayed in relation to the corresponding timing pulses. The detection instant for a received data pulse on the line side (e.g. PCM) of the interface should therefore be at the leading edge of the next timing pulse.

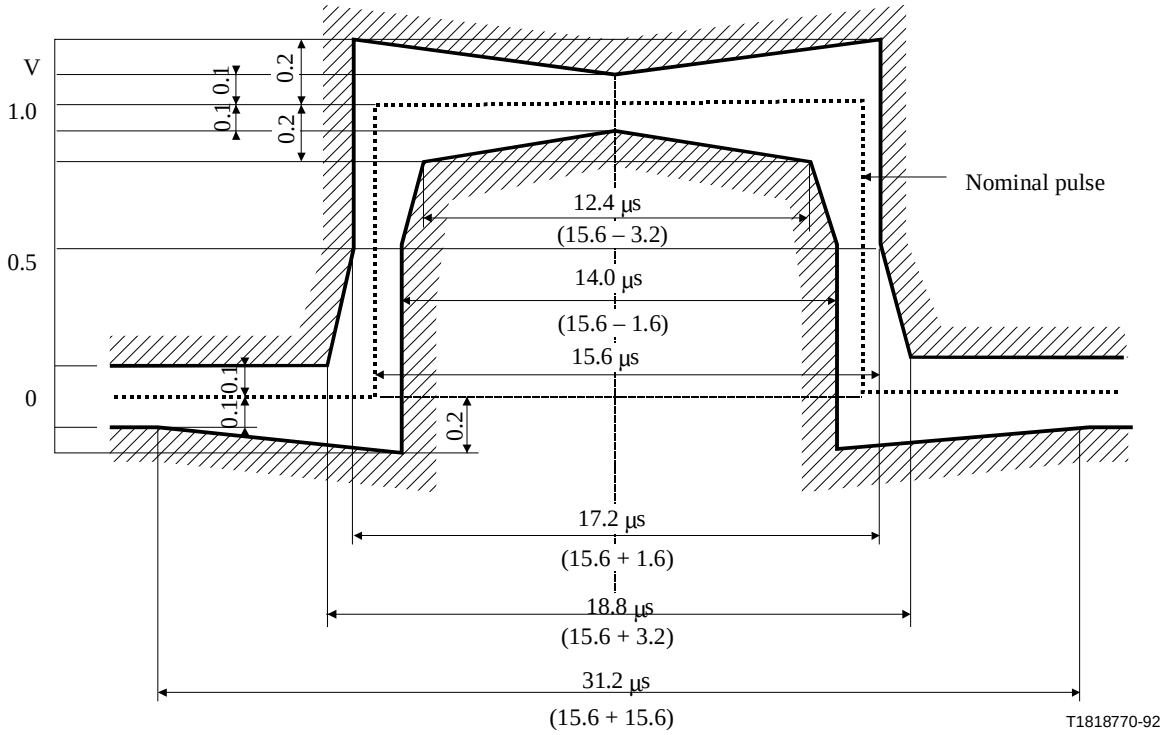
Overvoltage protection requirement: refer to Recommendation K.41.

4.2.3.2 Specifications at the output ports

See Table 3.

Table 3/G.703 – Digital 64 kbit/s contradirectional interface

Parameters	Data	Timing
Pulse shape (nominally rectangular)	All pulses of a valid signal must conform to the mask in Figure 8 irrespective of the polarity	All pulses of a valid signal must conform to the mask in Figure 9 irrespective of the polarity
Pairs in each direction of transmission	One symmetric pair	One symmetric pair
Test load impedance	120 ohms resistive	120 ohms resistive
Nominal peak voltage of a "mark" (pulse)	1.0 V	1.0 V
Peak voltage of a "space" (no pulse)	0 V ± 0.1 V	0 V ± 0.1 V
Nominal pulse width	15.6 μs	7.8 μs
Ratio of the amplitudes of positive and negative pulses at the centre of the pulse interval	0.95 to 1.05	0.95 to 1.05
Ratio of the widths of positive and negative pulses at the nominal half amplitude	0.95 to 1.05	0.95 to 1.05
Maximum peak-to-peak jitter at the output port (Note)	Refer to clause 2/G.823	
NOTE – For the time being these values are valid only for equipments of the 2 Mbit/s hierarchy.		



NOTE 1 – When one pulse is immediately followed by another pulse of the opposite polarity, the time limits at the zero-crossing between the pulses should be ±0.8 µs.

NOTE 2 – The time instants at which a transition from one state to another in the data signal may occur are determined by the timing signal. On the service (e.g. data or signalling) side of the interface, it is essential that these transitions are not initiated in advance of the timing instants given by the received timing signal.

Figure 8/G.703 – Mask of the data pulse of the 64-kbit/s contradirectional interface

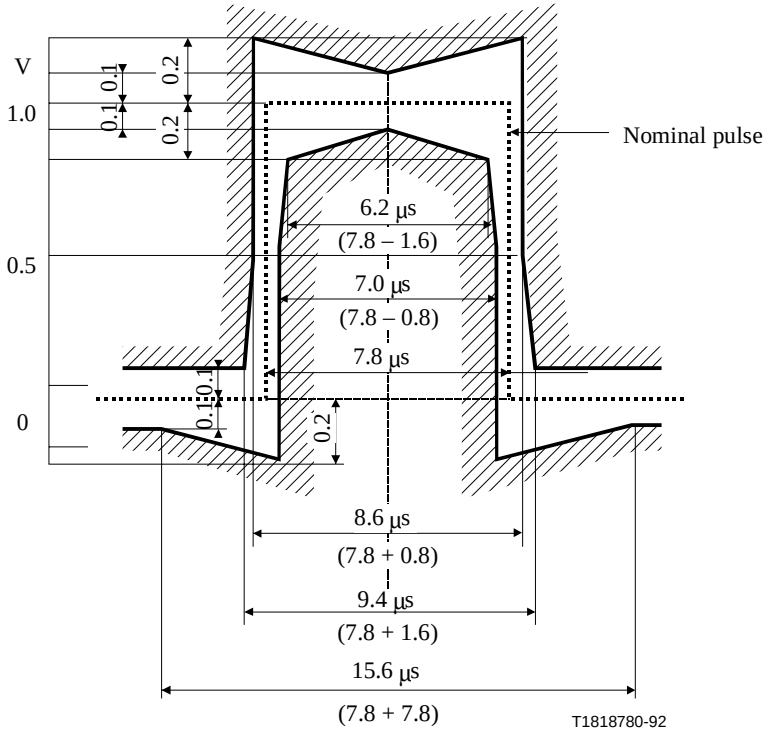


Figure 9/G.703 – Mask of the timing pulse of the 64-kbit/s contradirectional interface

4.2.3.3 Specifications at the input ports

The digital signals presented at the input ports should be as defined above but modified by the characteristics of the interconnecting pairs. The attenuation of these pairs at a frequency of 32 kHz should be in the range 0 to 3 dB. This attenuation should take into account any losses incurred by the presence of a digital distribution frame between the equipments.

The return loss at the input ports should have the following minimum values:

Frequency range (kHz)		**Return loss (dB)**
Data signal	**Composite timing signal**	
1.6 to 3.2	3.2 to 6.4	12
3.2 to 64	6.4 to 128	18
64 to 96	128 to 192	14

To provide nominal immunity against interference, input ports are required to meet the following requirement:

A nominal aggregate signal, encoded as a 64 kbit/s contradirectional signal and having a pulse shape as defined in the pulse mask, shall have added to it an interfering signal with the same pulse shape as the wanted signal. The interfering signal should have a bit rate within the limits specified in this Recommendation, but should not be synchronous with the wanted signal. The interfering signal shall be combined with the wanted signal in a combining network, with an overall zero loss in the signal path and with the nominal impedance 120 ohms to give a signal-to-interference ratio of 20 dB. The binary content of the interfering signal should comply with Recommendation O.152 ($2^{11} – 1$ bit period). No errors shall result when the combined signal, attenuated by up to the maximum specified interconnecting cable loss, is applied to the input port.

NOTE – The return loss specification applies for both the data signal and the composite timing signal input ports.

4.2.3.4 Grounding of screen

If the symmetrical pairs are screened, the screens shall be connected to the bonding network both at the input port and the output port.

NOTE 1 – The cable routing is important if leaving the system block. Consult Recommendation K.27 for guidance.

NOTE 2 – The use of isolation to the bonding network is for further study.

5 Interface at 1544 kbit/s

5.1 General characteristics

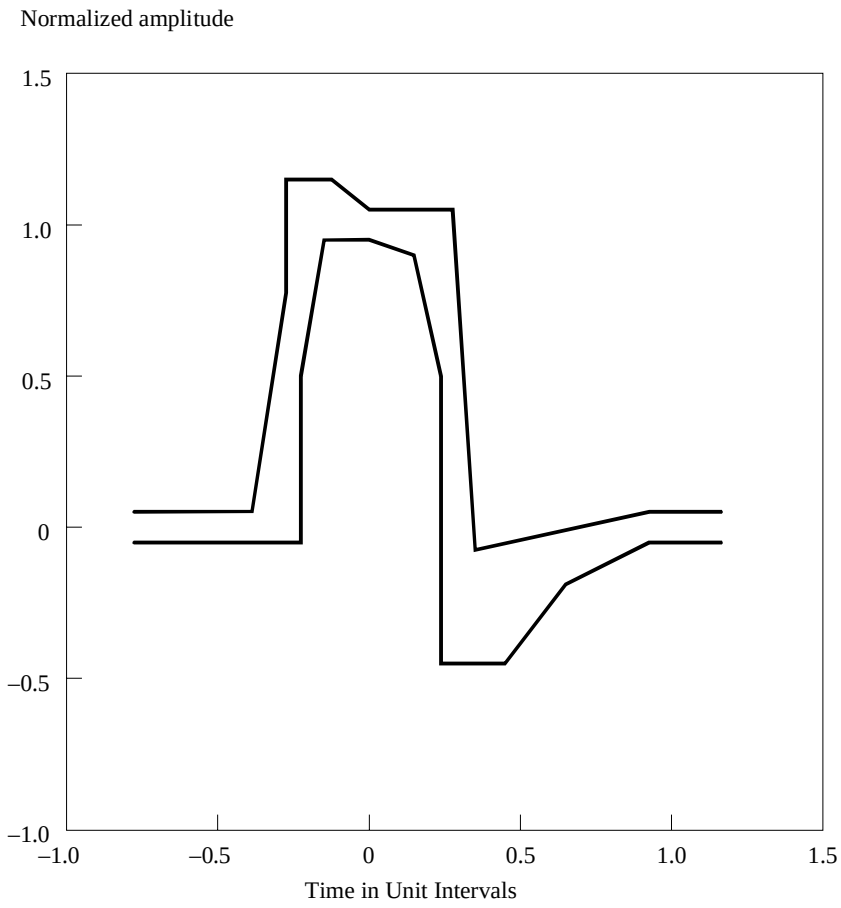
The digital interface signal has a nominal rate of 1544 kbit/s.

The 1544 kbit/s interface specification is defined in Table 4. All signals appearing at the 1544 kbit/s interface shall satisfy each requirement listed.

Table 4/G.703 –Digital interface at 1544 kbit/s

Parameter	Specification
Nominal line rate	1544 kbit/s
Line rate accuracy	In a self timed, free running mode, the line rate accuracy shall be ±50 bits/s (±32 ppm) or better.
Line code	Either (1) AMI with no more than 15 consecutive zeros, and at least N ones in each and every time window of 8(N + 1) digit time slots (where N can range from 1 to 23), or (2) B8ZS (Note 1).
Frame structure	No frame structure is required for 1544 kbit/s transmission or higher level multiplexing to higher level DSN signals.
Medium	One balanced twisted pair shall be used for each direction of transmission.
Test load impedance	A resistive test load of 100 ohms ± 5% shall be used at the interface for the evaluation of pulse shape and the electrical parameters specified below.
Pulse amplitude	The amplitude (Note 2) of an isolated pulse shall be between 2.4 V and 3.6 V.
Pulse shape	The shape of every pulse that approximates an isolated pulse (is preceded by four zeros and followed by one or more zeros) shall conform to the mask in Figure 10. See 5.2 for allowable procedures to be followed in checking conformance.
Power level	For an all-one signal, the power in a 3 kHz ± 1 kHz band centered at 772 kHz shall be between 12.6 dBm and 17.9 dBm. The power in a 3 kHz ± 1 kHz band centered at 1544 kHz shall be at least 29 dB below that at 772 kHz.
Pulse imbalance	In any window of seventeen consecutive bits, the maximum variation in pulse amplitudes shall be less than 200 mV, and the maximum variation in pulse widths (half amplitude) shall be less than 20 ns.
DC power	There shall be no DC power applied at the interface.
Verification access	Access to the signal at the interface shall be provided for verification of these signal specifications.
NOTE 1 – B8ZS is one method of providing bit sequence independence. Bit sequence independence in turn allows unconstrained clear channel capability. Zero Byte Time Slot Interchange (ZBTSI) is another method of providing clear channel transmission. NOTE 2 – While both voltage and power requirements are given to assist in qualification of signals at the interface, the values are not equivalent. Voltage specifications are given for isolated pulses, while power levels are specified for all-ones signal.	

An isolated pulse at the 1544 kbit/s interface shall fit within the mask shown in Figure 10. The corner points for this mask are shown below the figure. In this figure, the y axis shows normalized pulse amplitude. The x axis is time measured in unit intervals. For 1544 kbit/s, the unit interval is 648 nanoseconds.



Minimum curve		Maximum curve	
Time	**Normalized amplitude**	**Time**	**Normalized amplitude**
– 0.77	– 0.05	– 0.77	0.05
– 0.23	– 0.05	– 0.39	0.05
– 0.23	0.5	– 0.27	0.8
– 0.15	0.95	– 0.27	1.15
0.0	0.95	– 0.12	1.15
0.15	0.9	0.0	1.05
0.23	0.5	0.27	1.05
0.23	– 0.45	0.35	– 0.07
0.46	– 0.45	0.93	0.05
0.66	– 0.2	1.16	0.05
0.93	– 0.05		
1.16	– 0.05		

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Figure 10/G.703 – 1544 kbit/s interface isolated pulse mask and corner points

Some 1544 kbit/s interface equipment embedded in the network may have been designed using a different pulse mask than that in this Recommendation. Appendix I describes the earlier specification to provide information to designers of receiving equipment on the possible range of 1544 kbit/s signals in the network.

To accommodate signals generated by equipment predating this Recommendation, the (1544 kbit/s) receivers should be capable of operation with a signal having a transmission rate of deviation of ±200 bits/s (±130 ppm) (see Appendix I for pulse characteristics of older equipment).

5.2 Pulse specification

For Alternate Mark Inversion (AMI) coding, a pulse mask describing an isolated pulse appearing at the interface is used. In most cases, an ideal isolated pulse can only be approximated due to line coding constraints.

Pulse masks are shown in normalized form, with the nominal pulse amplitude shown as 1.0. In judging conformance of an isolated pulse to the mask, it is only permissible to:

a) position the mask horizontally as needed to encompass the pulse; and

b) uniformly scale the amplitude of the isolated pulse to fit the mask.

The baseline of the signal shall coincide with the zero point of the baseline of the mask. (The determination of the signal baseline is described in IEC 60469-2). Judging the conformance of negative-going pulses shall be performed after determining the conformance of positive-going pulses in order to maintain the signal baseline reference.

When viewing inverted negative-going pulses for 1544 kbit/s, only the horizontal positioning of the mask to encompass the pulse is permitted. Note that pulse streams with any significant dc component will not meet the requirements of this clause.

5.3 Eye diagrams

For signals not amenable to the use of pulse masks, another means of specifying the quality of pulses at the interface is an eye diagram, which is formed by superimposing the waveforms of all possible pulse sequences, including the effects of intersymbol interference. Eye diagrams are presented in normalized form with the peak pulse amplitudes normalized to 1.0 on the vertical scale and the time scale shown in terms of the unit interval. In judging the shape of an eye diagram, it is permissible to:

a) position the mask horizontally as needed to encompass the eye diagram; and

b) uniformly scale the amplitude of the mask as needed to encompass the eye diagram.

The baseline of the mask shall coincide with the signal baseline. The determination of signal baseline is described in IEC 60469-2.

6 Interface at 6312 kbit/s

Interconnection of 6312 kbit/s signals for transmission purposes is accomplished at a digital distribution frame.

The signal shall have a bit rate of 6312 kbit/s ± 30 ppm.

One symmetrical pair of characteristic impedance of 110 ohms, or one coaxial pair of characteristic impedance of 75 ohms shall be used for each direction of transmission.

Test load impedance shall be 110 ohms resistive or 75 ohms resistive as appropriate.

A pseudo-ternary code shall be used as indicated in Table 5.

The shape for an isolated pulse measured at the distribution frame shall fall within the mask either of Figure 11 or of Figure 12 and meet the other requirements of Table 5.

The voltage within a time slot containing a zero (space) shall be no greater than either the value produced in that time slot by other pulses (marks) within the mask of Figure 11, or ±0.1 of the peak pulse (mark) amplitude, whichever is greater in magnitude.

Table 5/G.703 – Digital interface at 6312 kbit/s (Note 1)

Location	Digital distribution frame	
Bit rate	6312 kbit/s	
Pair(s) in each direction of transmission	One symmetric pair	One coaxial pair
Code	B6ZS (Note 2)	B8ZS (Note 2)
Test load impedance	110 ohms resistive	75 ohms resistive
Nominal pulse shape (Note 1)	Rectangular, shaped by cable loss (see Figure 11)	Rectangular (see Figure 12)
Signal level	For an all 1s pattern transmitted, the power measured in a 3 kHz bandwidth should be as follows:	
	3156 kHz: 0.2 to 7.3 dBm 6312 kHz: –20 dBm or less	3156 kHz: 6.2 to 13.3 dBm 6312 kHz: –14 dBm or less
NOTE 1 – The pulse mask for 2nd order digital interface is shown in Figures 11 and 12. NOTE 2 – See Annex A.		

	T	Value of curve
Lower curve	$T \le -0.41$ $-0.41 \le T \le 0.24$ $0.24 \le T$	0 $0.5\left[1+\sin\frac{\pi}{2}\left(1+\frac{T}{0.205}\right)\right]$ $0.331e^{-1.9(T-0.3)}$
Upper curve	$T \le -0.72$ $-0.72 \le T \le 0.2$ $0.2 \le T$	0 $0.5\left[1+\sin\frac{\pi}{2}\left(1+\frac{T}{0.36}\right)\right]$ $0.1+0.72e^{-2.13(T-0.2)}$

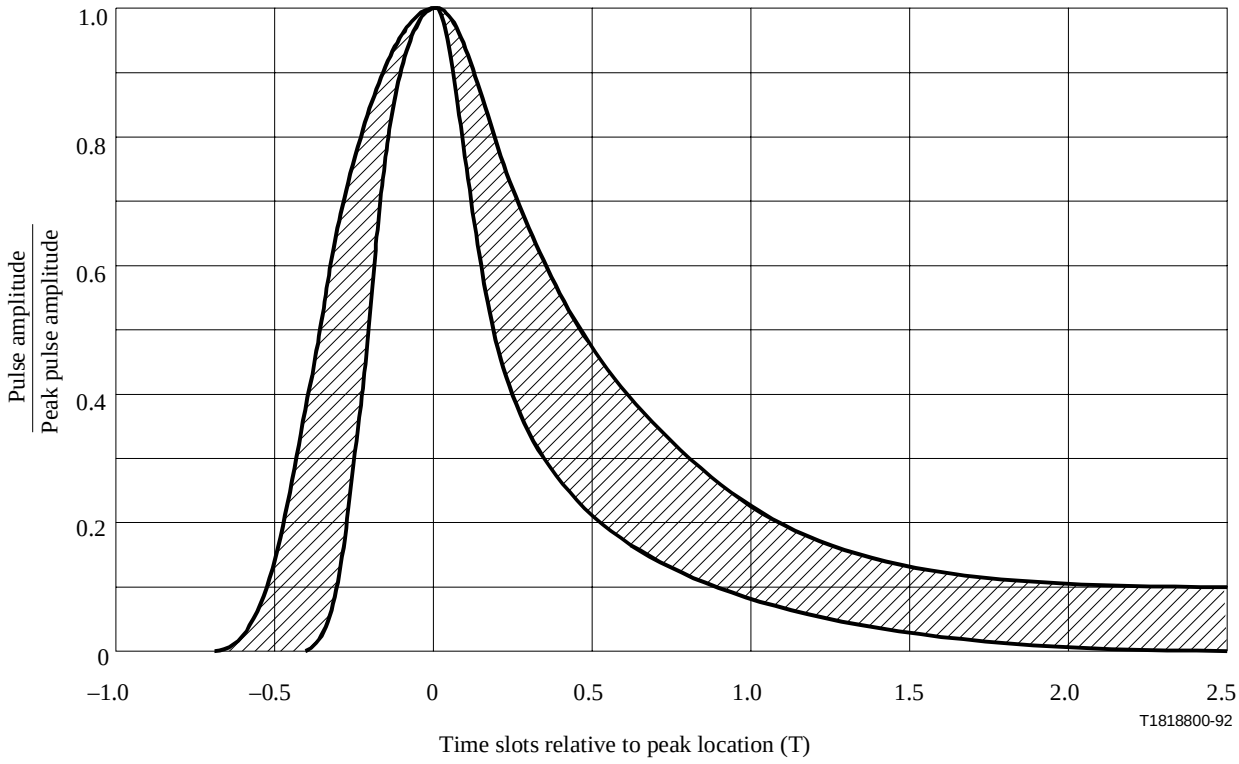


Figure 11/G.703 – Pulse mask for the symmetric pair interface at 6312 kbit/s

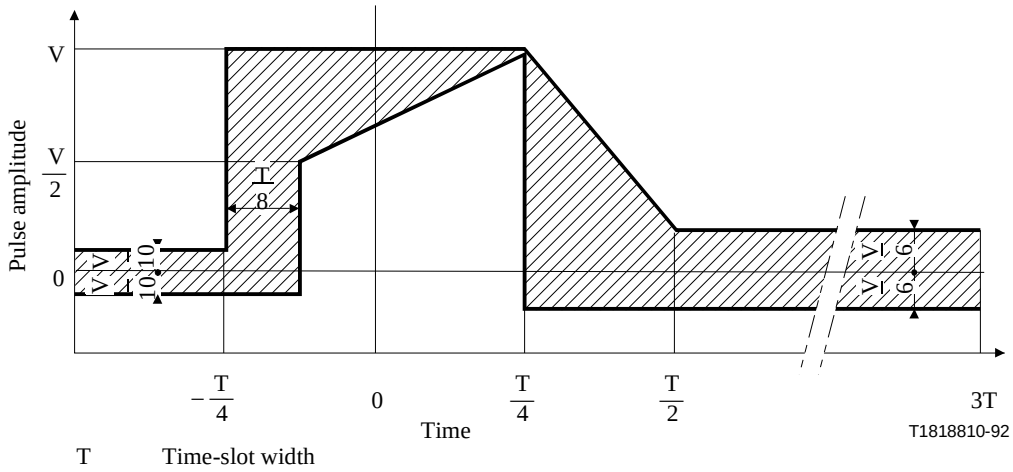


Figure 12/G.703 – Pulse mask for the coaxial pair interface at 6312 kbit/s

7 Interface at 32 064 kbit/s

Interconnection of 32 064 kbit/s signals for transmission purposes is accomplished at a digital distribution frame.

The signal shall have a bit rate of 32 064 kbit/s ± 10 ppm.

One coaxial pair shall be used for each direction of transmission.

The test load impedance shall be 75 ohms ± 5% resistive and the test method shall be direct.

A scrambled AMI code shall be used.

The shape for an isolated pulse measured at the point where the signal arrives at the distribution frame shall fall within the mask in the Figure 13.

The voltage within a time slot containing a zero (space) shall be no greater than either the value produced in that time slot by other pulses (marks) within the mask of Figure 13 or ±0.1 of the peak pulse (mark) amplitude, whichever is greater in magnitude.

	T	Value of curve
Lower curve	$-0.36 \le T < -0.30$	$5.76T + 2.07$
	$-0.30 \le T < 0$	$0.5\left[1+\sin\frac{\pi}{2}\left(1+\frac{T}{0.25}\right)\right]$
	$0 \le T < 0.22$	$0.5\left[1+\sin\frac{\pi}{2}\left(1+\frac{T}{0.16}\right)\right]$
	$0.22 \le T$	$0.11e^{-3.42(T-0.3)}$
Upper curve	$-0.65 \le T < 0$	$1.05\left[1-e^{-4.6(T+0.65)}\right]$
	$0 \le T < 0.25$	$0.5\left[1+\sin\frac{\pi}{2}\left(1+\frac{T}{0.28}\right)\right]$
	$0.25 \le T$	$0.11+0.407e^{-2.1(T-0.29)}$

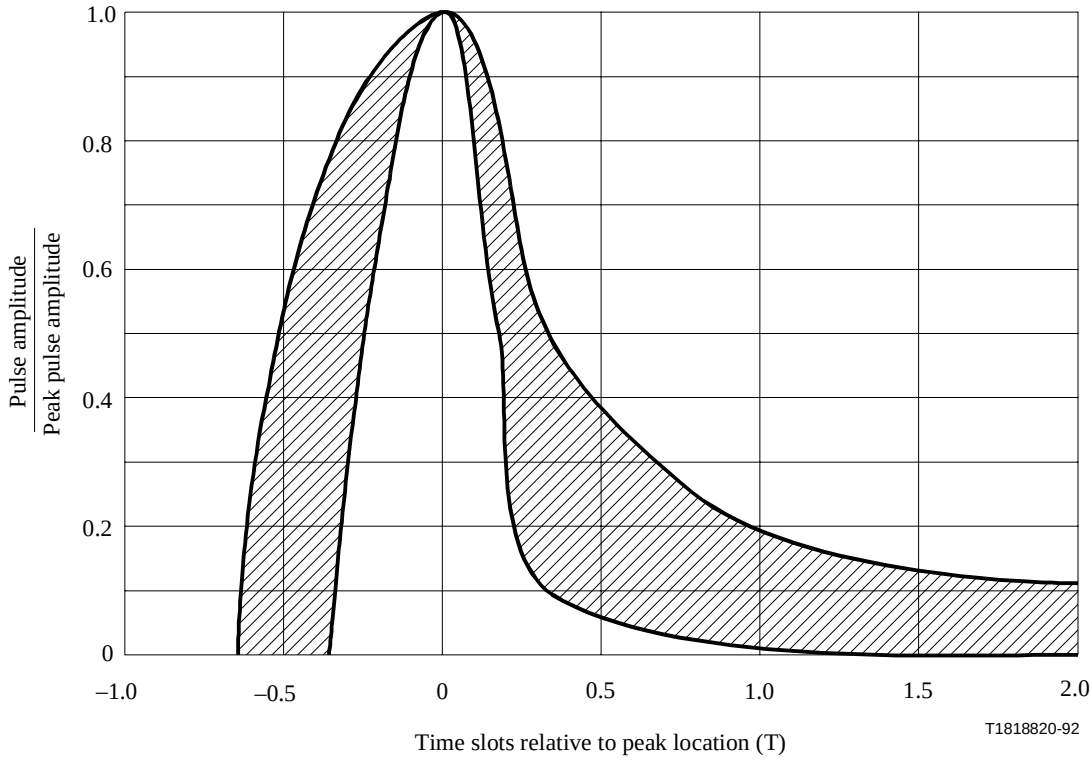


Figure 13/G.703 – Pulse mask for the coaxial pair interface at 32 064 kbit/s

For an all 1s pattern transmitted, the power measured in a 3 kHz bandwidth at the point where the signal arrives at the distribution frame shall be as follows:

– 16 032 kHz: +5 dBm to +12 dBm;

– 32 064 kHz: at least 20 dB below the power at 16 032 kHz.

The connectors and coaxial cable pairs in the distribution frame shall be 75 ohms ± 5%.

8 Interface at 44 736 kbit/s

44 736 kbit/s interface specification is defined in Table 6.

All signals appearing at the 44 736 kbit/s interface shall satisfy each requirement listed.

An isolated pulse (see pulse shape in Table 6) at the 44 736 kbit/s interface shall fit within the mask shown in Figure 14. Equations defining the various line segments making up the mask are listed below the figure. In this figure, the y axis shows normalized pulse amplitude. The x axis is time measured in unit intervals. For 44 736 kbit/s, the unit interval is 22.4 nanoseconds.

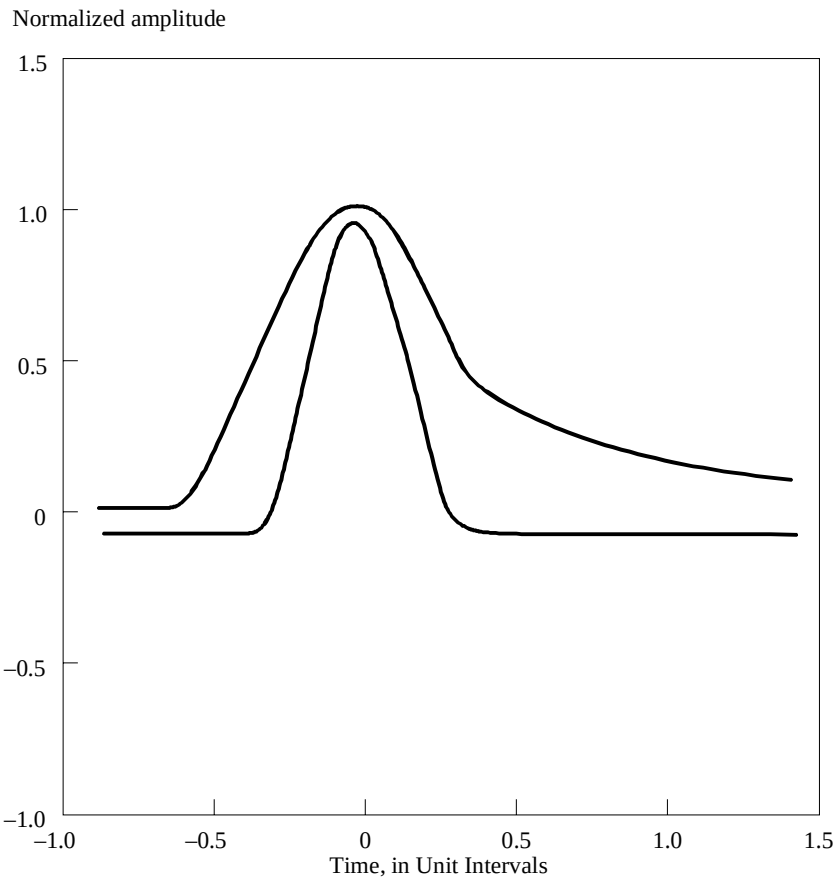
To assure proper operation of transmission facilities and higher order multiplex equipment, all 44 736 kbit/s sources shall use the frame structured defined in Recommendation G.752.

Table 6/G.703 – Digital interface at 44 736 kbit/s

Parameter	Specification
Nominal line rate	44 736 kbit/s
Line rate accuracy	In a self timed, free running mode, the line rate tolerance shall be ±895 bits/s (±20 ppm) or better.
Line code	B3ZS (bipolar with three-zero substitutions)
Frame structure	The signal shall have the frame structure defined in Recommendation G.752 to ensure transmission through all types of 44 736 kbit/s transport equipment. The frame structure is not required for multiplexing to higher level DSN signals.
Medium	One unbalanced coaxial line shall be used for each direction of transmission.
Test load impedance	A resistive test load of 75 ohms ± 5% shall be used at the interface for the evaluation of pulse shape and the electrical parameters specified below.
Pulse amplitude	The amplitude (Note 1) of an isolated pulse shall be between 0.36 V and 0.85 V peak.
Pulse shape	The shape of every pulse that approximates an isolated pulse (is preceded by two zeros and followed by one or more zeros) shall conform to the mask in Figure 14. See 5.2 for allowable procedures to be followed in checking conformance. This mask includes an allowance of ±3% of the peak pulse amplitude at any point on the mask relative to the pulse mask in the earlier version. Equations defining the various line segments making up the mask are listed below the figure.
Power level	A wideband power measurement of an AIS signal (as defined in Recommendation G.704) using a power level sensor with a working frequency range of 200 MHz shall be between −4.7 dBm and +3.6 dBm, including the effects of a range of connecting cable lengths between 68.6 meters (225 feet) and 137.2 meters (450 feet). A low-pass filter having a flat passband and cutoff frequency of 200 MHz shall be used. The rolloff characteristics of this filter are not important; or an alternate power level specification of the power of an all-ones signal (Note 2) is useful for some equipment qualifications. It requires that the power in a 3 kHz ± 1 kHz band centered at 22 368 kHz be between −1.8 dBm and +5.7 dBm. It further requires that the power in a 3 kHz ± 1 kHz band centered at 44 736 kHz be at least 20 dB below that at 22 368 kHz.

Table 6/G.703 – Digital interface at 44 736 kbit/s *(concluded)*

Parameter	Specification
Pulse imbalance	1) The ratio of amplitudes of positive and negative isolated pulses shall be between 0.90 and 1.10. 2) Positive and negative isolated pulses shall both conform to the mask of Figure 14.
DC power	There shall be no DC power applied at the interface.
Verification access	Access to the signal at the interface shall be provided for verification of these signal specifications.
NOTE 1 – While both voltage and power requirements are given to assist in qualification of signals at the interface, the values are not equivalent. Voltage specifications are given for isolated pulses, while power levels are specified for an AIS signal, or alternatively an all-ones signal. NOTE 2 – The all-ones signal is not realizable within the frame structure specified in Recommendation G.752, and is not encountered in North American telecommunication networks.	



Time axis range (Unit Intervals)	Normalized amplitude equation
Upper curve	
$-0.85 \le T \le -0.68$	0.03
$-0.68 \le T \le 0.36$	$0.5\left\{1+\sin\left[\left(\frac{\pi}{2}\right)\left(1+\frac{T}{0.34}\right)\right]\right\}+0.03$
$0.36 \le T \le 1.4$	$0.08+0.407e^{-1.84(T-0.36)}$
Lower curve	
$-0.85 \le T \le -0.36$	–0.03
$-0.36 \le T \le 0.36$	$0.5\left\{1+\sin\left[\left(\frac{\pi}{2}\right)\left(1+\frac{T}{0.18}\right)\right]\right\}-0.03$
$0.36 \le T \le 1.4$	–0.03

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Figure 14/G.703 – 44 736 kbit/s interface isolated pulse mask and equations

9 Interface at 2048 kbit/s

9.1 General characteristics

Bit rate: 2048 kbit/s ± 50 ppm

Code: High density bipolar of order 3 (HDB3) (a description of this code can be found in Annex A).

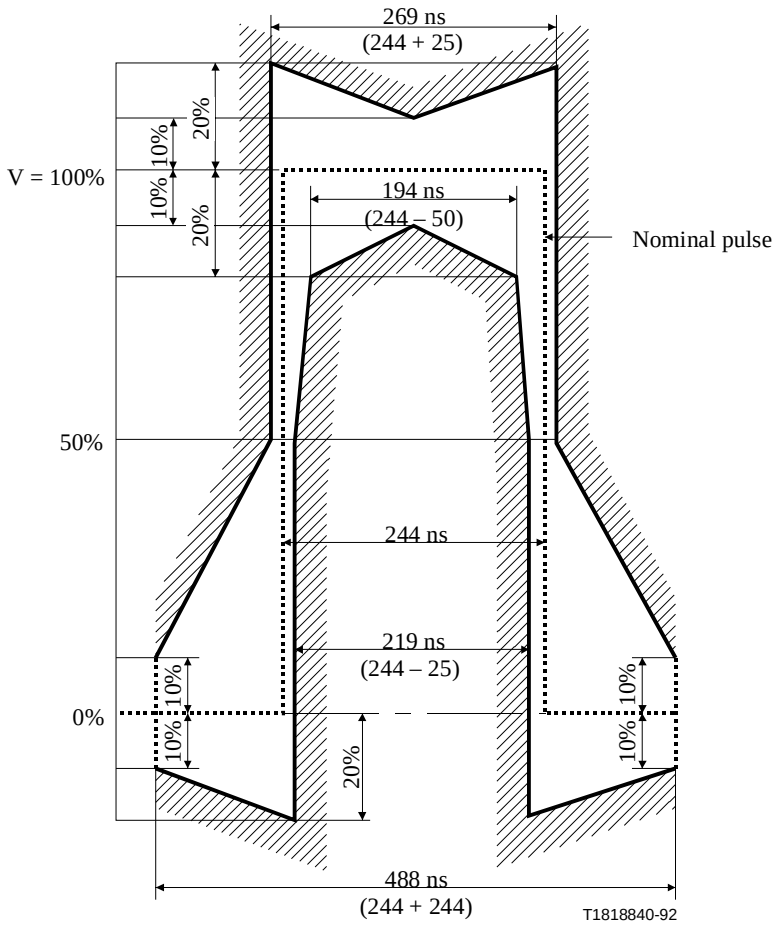
Overvoltage protection requirement: refer to Recommendation K.41.

9.2 Specifications at the output ports

See Table 7.

Table 7/G.703 – Digital interface at 2048 kbit/s

Pulse shape (nominally rectangular)	All marks of a valid signal must conform with the mask (see Figure 15) irrespective of the sign. The value V corresponds to the nominal peak value.	
Pair(s) in each direction	One coaxial pair (see 9.4)	One symmetrical pair (see 9.4)
Test load impedance	75 ohms resistive	120 ohms resistive
Nominal peak voltage of a mark (pulse)	2.37 V	3 V
Peak voltage of a space (no pulse)	0 ± 0.237 V	0 ± 0.3 V
Nominal pulse width	244 ns	
Ratio of the amplitudes of positive and negative pulses at the centre of the pulse interval	0.95 to 1.05	
Ratio of the widths of positive and negative pulses at the nominal half amplitude	0.95 to 1.05	
Maximum peak-to-peak jitter at an output port	Refer to clause 2/G.823	



NOTE – V corresponds to the nominal peak value.

Figure 15/G.703 – Mask of the pulse at the 2048 kbit/s interface

9.3 Specifications at the input ports

The digital signal presented at the input port shall be as defined above but modified by the characteristic of the interconnecting pair. The attenuation of this pair shall be assumed to follow a $\sqrt{f}$ law and the loss at a frequency of 1024 kHz shall be in the range 0 to 6 dB. This attenuation should take into account any losses incurred by the presence of a digital distribution frame between the equipments.

For the jitter to be tolerated at the input port, refer to clause 3/G.823.

The return loss at the input port should have the following provisional minimum values:

Frequency range (kHz)	**Return loss (dB)**
51 to 102	12
102 to 2048	18
2048 to 3072	14

To ensure adequate immunity against signal reflections that can arise at the interface due to impedance irregularities at digital distribution frames and at digital output ports, input ports are required to meet the following requirement:

A nominal aggregate signal, encoded into HDB3 and having a pulse shape as defined in the pulse mask, shall have added to it an interfering signal with the same pulse shape as the wanted signal. The interfering signal should have a bit rate within the limits specified in this Recommendation, but should not be synchronous with the wanted signal. The interfering signal shall be combined with the wanted signal in a combining network, with an overall zero loss in the signal path and with the nominal impedance 75 ohms (in the case of coaxial-pair interface) or 120 ohms (in the case of symmetrical-pair interface), to give a signal-to-interference ratio of 18 dB. The binary content of the interfering signal should comply with Recommendation O.151 (2^{15} – 1 bit period). No errors shall result when the combined signal, attenuated by up to the maximum specified interconnecting cable loss, is applied to the input port.

NOTE – A receiver implementation providing an adaptive rather than a fixed threshold is considered to be more robust against reflections and should therefore be preferred.

9.4 Grounding of outer conductor or screen

The outer conductor of the coaxial pair or the screen of the symmetrical pair shall be connected to the bonding network both at the input port and the output port.

NOTE 1 – The cable routing is important if leaving the system block. Consult Recommendation K.27 for guidance.

NOTE 2 – The direct connection of the outer conductors of co-axial cables to the bonding network at the transmit and receive interfaces may, because of differences in earth potential at each end of the cable, result in unwanted current flowing in the outer conductor, through connectors and through the receiver input circuitry. This may result in errors or even permanent damage. To prevent this problem, DC isolation may be introduced between the outer conductor and bonding network at the receive interface. The method of DC isolation must not compromise the EMC compliance of the equipment and the overall installation.

NOTE 3 – The use of isolation to the bonding network is for further study.

10 Interface at 8448 kbit/s

10.1 General characteristics

Bit rate: 8448 kbit/s ± 30 ppm

Code: High density bipolar of order 3 HDB3 (a description of this code can be found in Annex A).

Overvoltage protection requirement: refer to Recommendation K.41.

10.2 Specification at the output ports

See Table 8.

Table 8/G.703 – Digital interface at 8448 kbit/s

Pulse shape (nominally rectangular)	All marks of a valid signal must conform with the mask (Figure 16) irrespective of the sign.
Pair(s) in each direction	One coaxial pair (see 10.4)
Test load impedance	75 ohms resistive
Nominal peak voltage of a mark (pulse)	2.37 V
Peak voltage of a space (no pulse)	0 V ± 0.237 V
Nominal pulse width	59 ns
Ratio of the amplitudes of positive and negative pulses at the centre of the pulse interval	0.95 to 1.05
Ratio of widths of positive and negative pulses at the nominal half amplitude	0.95 to 1.05
Maximum peak-to-peak jitter at an output port	Refer to clause 2/G.823

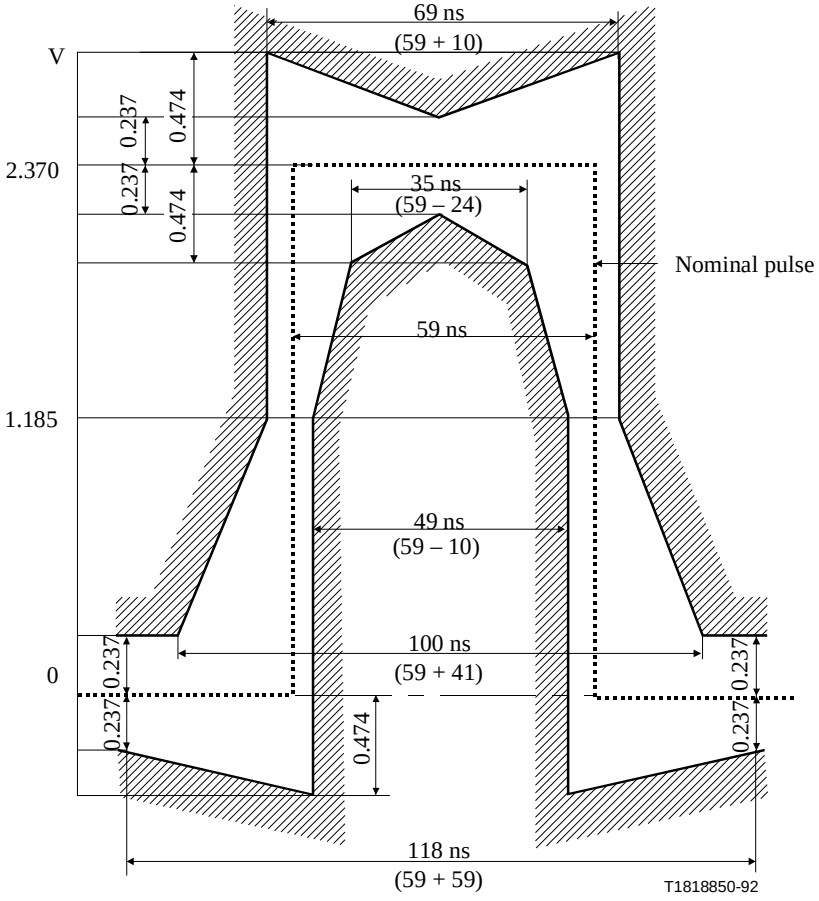


Figure 16/G.703 – Pulse mask at the 8448 kbit/s interface

10.3 Specifications at the input ports

The digital signal presented at the input port shall be as defined above but modified by the characteristics of the interconnecting pairs. The attenuation of this pair shall be assumed to follow a $\sqrt{f}$ law and the loss at a frequency of 4224 kHz shall be in the range 0 to 6 dB. This attenuation should take into account any losses incurred by the presence of a digital distribution frame between the equipments.

For the jitter to be tolerated at the input port, refer to clause 3/G.823.

The return loss at the input port should have the following provisional minimum values:

Frequency range (kHz)	Return loss (dB)
211 to 422	12
422 to 8448	18
8448 to 12 672	14

To ensure adequate immunity against signal reflections that can arise at the interface due to impedance irregularities at digital distribution frames and at digital output ports, input ports are required to meet the following requirement:

A nominal aggregate signal, encoded into HDB3 and having a pulse shape as defined in the pulse mask shall have added to it an interfering signal with the same pulse shape as the wanted signal. The interfering signal should have a bit rate within the limits specified in this Recommendation, but should not be synchronous with the wanted signal. The interfering signal shall be combined with the wanted signal in a combining network, with an overall zero loss in the signal path and with the nominal impedance 75 ohms to give a signal-to-interference ratio of 20 dB. The binary content of the interfering signal should comply with Recommendation O.151 (2^{15} – 1 bit period). No errors shall result when the combined signal, attenuated by up to the maximum specified interconnecting cable loss, is applied to the input port.

10.4 Grounding of outer conductor

The outer conductor of the coaxial pair shall be connected to the bonding network at the input port and the output port.

NOTE 1 – The cable routing is important if leaving the system block. Consult Recommendation K.27 for guidance.

NOTE 2 – The use of isolation to the bonding network is for further study.

11 Interface at 34 368 kbit/s

11.1 General characteristics

Bit rate: 34 368 kbit/s ± 20 ppm

Code: HDB3 (a description of this code can be found in Annex A).

Overvoltage protection requirement: refer to Recommendation K.41.

11.2 Specification at the output ports

See Table 9.

Table 9/G.703 – Digital interface at 34 368 kbit/s

Pulse shape (nominally rectangular)	All marks of a valid signal must conform with the mask (see Figure 17), irrespective of the sign.
Pair(s) in each direction	One coaxial pair (see 11.4)
Test load impedance	75 ohms resistive
Nominal peak voltage of a mark (pulse)	1.0 V
Peak voltage of a space (no pulse)	0 V ± 0.1 V
Nominal pulse width	14.55 ns
Ratio of the amplitudes of positive and negative pulses at the center of a pulse interval	0.95 to 1.05
Ratio of the widths of positive and negative pulses at the nominal half amplitude	0.95 to 1.05
Maximum peak-to-peak jitter at an output port	Refer to clause 2/G.823

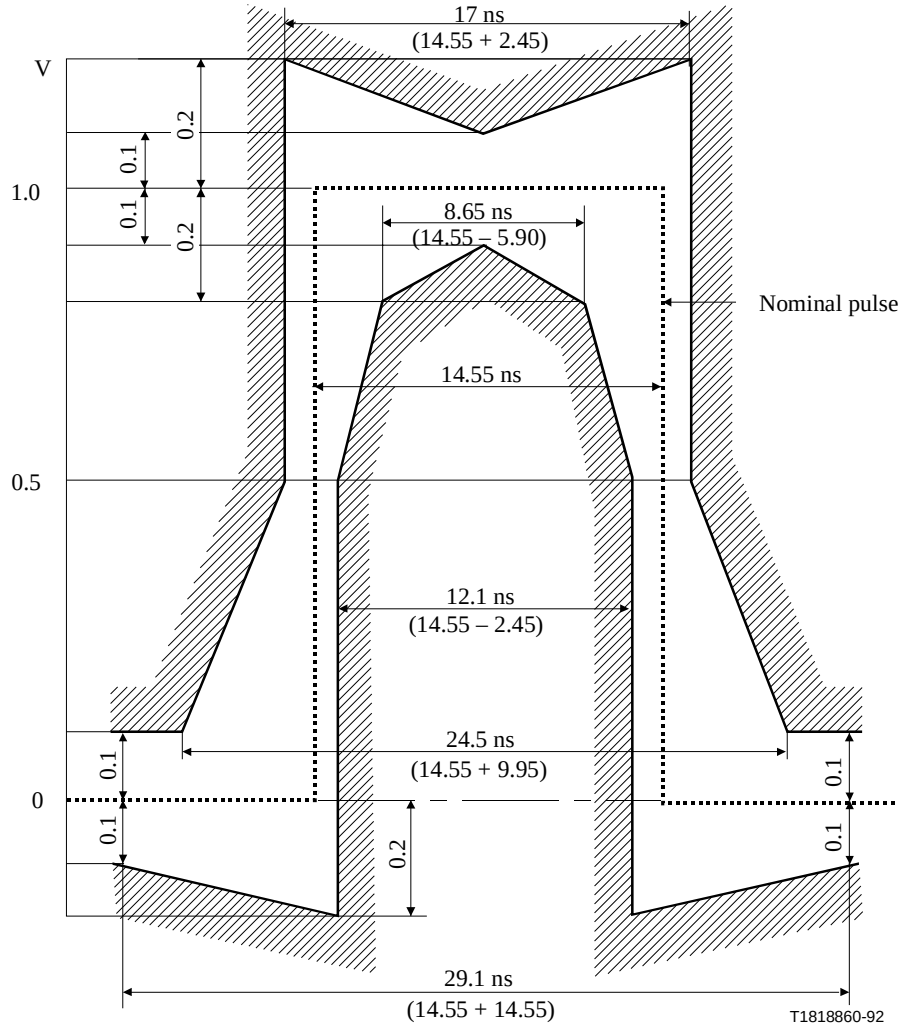


Figure 17/G.703 – Pulse mask at the 34 368 kbit/s interface

11.3 Specifications at the input ports

The digital signal presented at the input port shall be as defined above but modified by the characteristics of the interconnecting pair. The attenuation of this cable shall be assumed to follow

approximately a $\sqrt{f}$ law and the loss at a frequency of 17 184 kHz shall be in the range 0 to 12 dB.

For the jitter to be tolerated at the input port, refer to clause 3/G.823.

The return loss at the input port should have the following provisional minimum values:

Frequency range (kHz)	Return loss (dB)
860 to 1720	12
1720 to 34 368	18
34 368 to 51 550	14

To ensure adequate immunity against signal reflections that can arise at the interface due to impedance irregularities at digital distribution frames and at digital output ports, input ports are required to meet the following requirement:

A nominal aggregate signal, encoded into HDB3 and having a pulse shape as defined in the pulse mask shall have added to it an interfering signal with the same pulse shape as the wanted signal. The interfering signal should have a bit rate within limits specified in this Recommendation, but should not be synchronous with the wanted signal. The interfering signal shall be combined with the wanted signal in a combining network, with an overall zero loss in the signal path and with the nominal impedance 75 ohms to give a signal-to-interference ratio of 20 dB. The binary content of the interfering signal should comply with Recommendation O.151 (2^{23} – 1 bit period). No errors shall result when the combined signal, attenuated by up to the maximum specified interconnecting cable loss, is applied to the input port.

11.4 Grounding of outer conductor

The outer conductor of the coaxial pair shall be connected to the bonding network both at the input port and the output port.

NOTE 1 – The cable routing is important if leaving the system block. Consult Recommendation K.27 for guidance.

NOTE 2 – The use of isolation to the bonding network is for further study.

12 Interface at 139 264 kbit/s

12.1 General characteristics

Bit rate: 139 264 kbit/s ± 15 ppm

Code: Coded Mark Inversion (CMI) (a description of this code can be found in Annex A)

Overvoltage protection requirement: refer to Recommendation K.41.

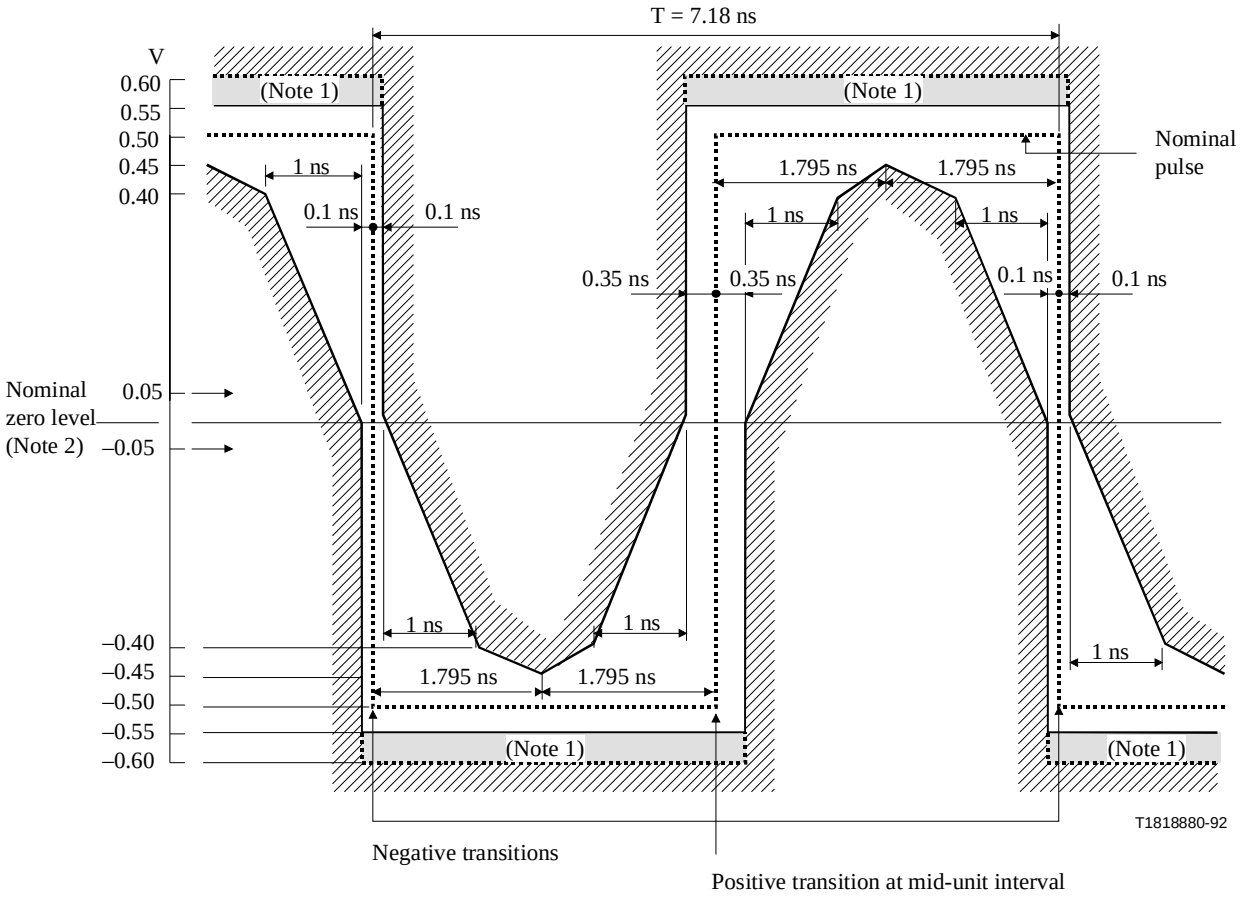
12.2 Specifications at the output ports

The specifications at the output ports are given in Table 10 and Figures 18 and 19.

NOTE – A method based on the measurement of the levels of the fundamental frequency component, the second (and possibly the third) harmonic of a signal corresponding to binary all 0s and binary all 1s, is considered to be a perfectly adequate method of checking that the requirements of Table 10 have been met. The relevant values of the harmonic components are under study.

Table 10/G.703 – Digital interface at 139 264 kbit/s

Pulse shape	Nominally rectangular and conforming to the masks shown in Figures 19 and 20
Pair(s) in each direction	One coaxial pair
Test load impedance	75 ohms resistive
Peak-to-peak voltage	1 ± 0.1 V
Rise time between 10% and 90% amplitudes of the measured steady state amplitude	≤2 ns
Transition timing tolerance (referred to the mean value of the 50% amplitude points of negative transitions)	Negative transitions: ±0.1 ns Positive transitions at unit interval boundaries: ±0.5 ns Positive transitions at mid-interval: ±0.35 ns
Return loss	≥15 dB over frequency range 7 MHz to 210 MHz
Maximum peak-to-peak jitter at an output port	Refer to clause 2/G.823



NOTE 1 – The maximum "steady state" amplitude should not exceed the 0.55 V limit. Overshoots and other transients are permitted to fall into the dotted area, bounded by the amplitude levels 0.55 V and 0.6 V, provided that they do not exceed the steady state level by more than 0.05 V. The possibility of relaxing the amount by which the overshoot may exceed the steady state level is under study.

NOTE 2 – For all measurements using these masks, the signal should be AC coupled, using a capacitor of not less than 0.01 µF, to the input of the oscilloscope used for measurements.

The nominal zero level for both masks should be aligned with the oscilloscope trace with no input signal. With the signal then applied, the vertical position of the trace can be adjusted with the objective of meeting the limits of the masks. Any such adjustment should be the same for both masks and should not exceed ±0.05 V. This may be checked by removing the input signal again and verifying that the trace lies within ±0.05 V of the nominal zero level of the masks.

NOTE 3 – Each pulse in a coded pulse sequence should meet the limits of the relevant mask, irrespective of the state of the preceding or succeeding pulses, with both pulse masks fixed in the same relation to a common timing reference, i.e. with their nominal start and finish edges coincident.

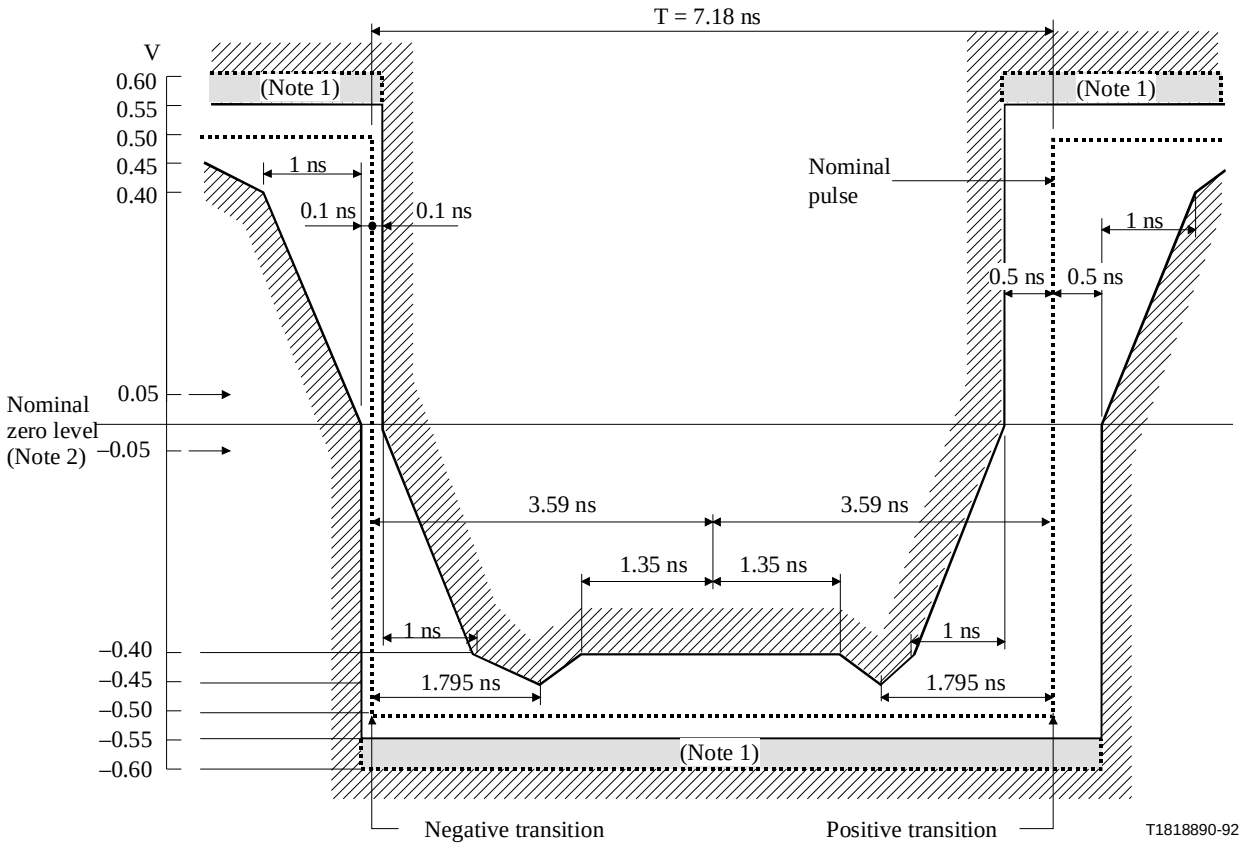
The masks allow for HF jitter caused by intersymbol interference in the output stage, but not for jitter present in the timing signal associated with the source of the interface signal.

When using an oscilloscope technique to determine pulse compliance with the mask, it is important that successive traces of the pulses overlay in order to suppress the effects of low frequency jitter. This can be accomplished by several techniques [e.g. a) triggering the oscilloscope on the measured waveform or b) providing both the oscilloscope and the pulse output circuits with the same clock signal].

These techniques require further study.

NOTE 4 – For the purpose of these masks, the rise time and decay time should be measured between –0.4 V and 0.4 V, and should not exceed 2 ns.

Figure 18/G.703 – Mask of a pulse corresponding to a binary 0



NOTE 1 – The maximum "steady state" amplitude should not exceed the 0.55 V limit. Overshoots and other transients are permitted to fall into the dotted area, bounded by the amplitude levels 0.55 V and 0.6 V, provided that they do not exceed the steady state level by more than 0.05 V. The possibility of relaxing the amount by which the overshoot may exceed the steady state level is under study.

NOTE 2 – For all measurements using these masks, the signal should be AC coupled, using a capacitor of not less than 0.01 µF, to the input of the oscilloscope used for measurements.

The nominal zero level for both masks should be aligned with the oscilloscope trace with no input signal. With the signal then applied, the vertical position of the trace can be adjusted with the objective of meeting the limits of the masks. Any such adjustment should be the same for both masks and should not exceed ±0.05 V. This may be checked by removing the input signal again and verifying that the trace lies within ±0.05 V of the nominal zero level of the masks.

NOTE 3 – Each pulse in a coded sequence should meet the limits of the relevant mask, irrespective of the state of the preceding or succeeding pulses, with both pulse masks fixed in the same relation to a common timing reference, i.e. with their nominal start and finish edges coincident.

The masks allow for HF jitter caused by intersymbol interference in the output stage, but not for jitter present in the timing signal associated with the source of the interface signal.

When using an oscilloscope technique to determine pulse compliance with the mask, it is important that successive traces of the pulses overlay in order to suppress the effects of low frequency jitter. This can be accomplished by several techniques [e.g. a) triggering the oscilloscope on the measured waveform or b) providing both the oscilloscope and the pulse output circuits with the same clock signal].

These techniques require further study.

NOTE 4 – For the purpose of these masks, the rise time and decay time should be measured between –0.4 V and 0.4 V, and should not exceed 2 ns.

NOTE 5 – The inverse pulse will have the same characteristics, noting that the timing tolerance at the level of the negative and positive transitions are ±0.1 ns and ±0.5 ns respectively.

Figure 19/G.703 – Mask of a pulse corresponding to a binary 1

12.3 Specifications at the input ports

The digital signal presented at the input port should conform to Table 10 and Figures 18 and 19 modified by the characteristics of the interconnecting coaxial pair.

The attenuation of the coaxial pair should be assumed to follow an approximate $\sqrt{f}$ law and to have a maximum insertion loss of 12 dB at a frequency of 70 MHz.

For the jitter to be tolerated at the input port, refer to clause 3/G.823.

The return loss characteristics should be the same as that specified for the output port.

12.4 Grounding of outer conductor

The outer conductor of the coaxial pair shall be connected to the bonding network both at the input port and the output port.

NOTE 1 – The cable routing is important if leaving the system block. Consult Recommendation K.27 for guidance.

NOTE 2 – The use of isolation to the bonding network is for further study.

13 2048 kHz synchronization interface

13.1 General

The use of this interface is recommended for all applications where it is required to synchronize a digital equipment by an external 2048 kHz synchronization signal.

Overvoltage protection requirement: refer to Recommendation K.41.

13.2 Specifications at the output port

See Table 11.

Table 11/G.703 – Digital 2048 kHz clock interface

Frequency	2048 kHz ± 50 ppm	
Pulse shape	The signal must conform with the mask (Figure 20). The value V corresponds to the maximum peak value. The value V_1 corresponds to the minimum peak value.	
Type of pair	Coaxial pair (see Note in 13.4)	Symmetrical pair (see Note in 13.4)
Test load impedance	75 ohms resistive	120 ohms resistive
Maximum peak voltage (V_{op})	1.5	1.9
Minimum peak voltage (V_{op})	0.75	1.0
Maximum jitter at an output port	0.05 IU peak-to-peak, measured within the frequency range $_1$ = 20 Hz to $_4$ = 100 kHz (Note)	
NOTE – This value is valid for network timing distribution equipments. Other values may be specified for timing output ports of digital links carrying the network timing.		

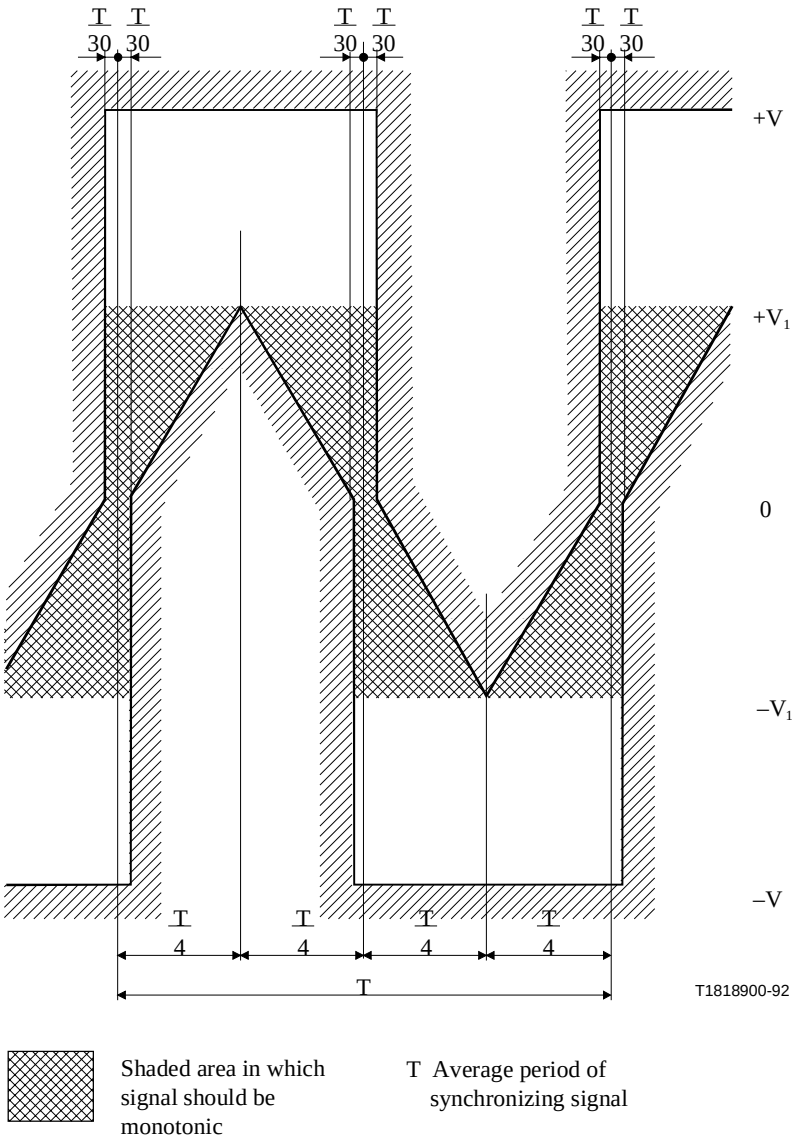


Figure 20/G.703 – Wave shape at an output port

13.3 Specifications at the input ports

The signal presented at the input ports should be as defined above but modified by the characteristics of the interconnecting pair.

The attenuation of this pair shall be assumed to follow a $\sqrt{f}$ law and the loss at a frequency of 2048 kHz should be in the range 0 to 6 dB (minimum value). This attenuation should take into account any losses incurred by the presence of a digital distribution frame between the equipments.

The input port shall be able to tolerate a digital signal with these electrical characteristics but modulated by jitter. The jitter values are under study.

The return loss at 2048 kHz should be ≥15 dB.

13.4 Grounding of outer conductor or screen

The outer conductor of the coaxial pair or the screen of the symmetrical pair shall be connected to the bonding network both at the input port and the output port.

NOTE 1 – The cable routing is important if leaving the system block. Consult Recommendation K.27 for guidance.

NOTE 2 – The use of isolation to the bonding network is for further study.

14 Interface at 97 728 kbit/s

Interconnection of 97 728 kbit/s signals for transmission purposes is accomplished at a digital distribution frame.

The signal shall have a bit rate of 97 728 kbit/s ± 10 ppm.

One coaxial pair shall be used for each direction of transmission.

The test load impedance shall be 75 ohms ± 5% resistive.

A scrambled AMI code[1] shall be used.

The shape for the 97 728 kbit/s output port shall fall within the mask in Figure 21. The shape at the point where the signal arrives at the distribution frame will be modified by the characteristics of the interconnecting cable.

The connectors and cable pairs in the distribution frame shall be 75 ohms ± 5%.

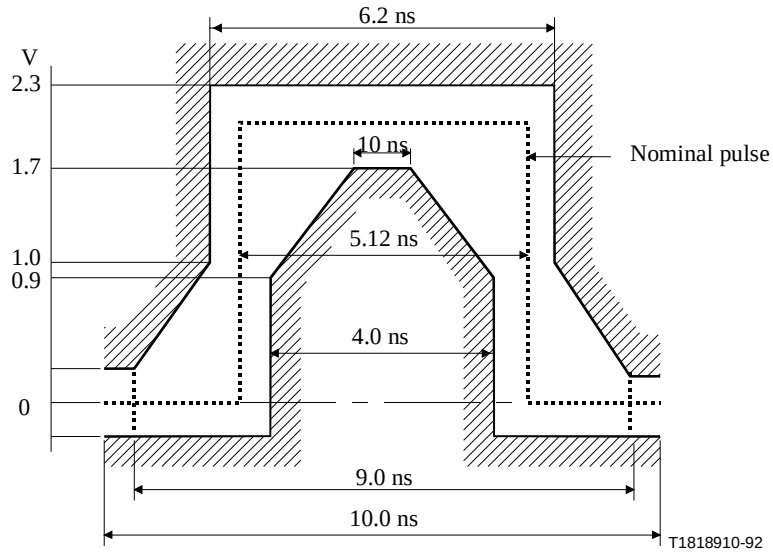


Figure 21/G.703 – Pulse mask at the 97 728 kbit/s output port

15 Interface at 155 520 kbit/s

15.1 General characteristics

Bit rate: 155 520 kbit/s

Bit rate tolerance: ±20 ppm

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[1] An AMI code is scrambled by a five-stage reset-type scrambler with the primitive polynominal of $x^5 + x^3 + 1$.

Code: Coded Mark Inversion (CMI) (a description of this code can be found in Annex A).

Overvoltage protection requirement: refer to Recommendation K.41.

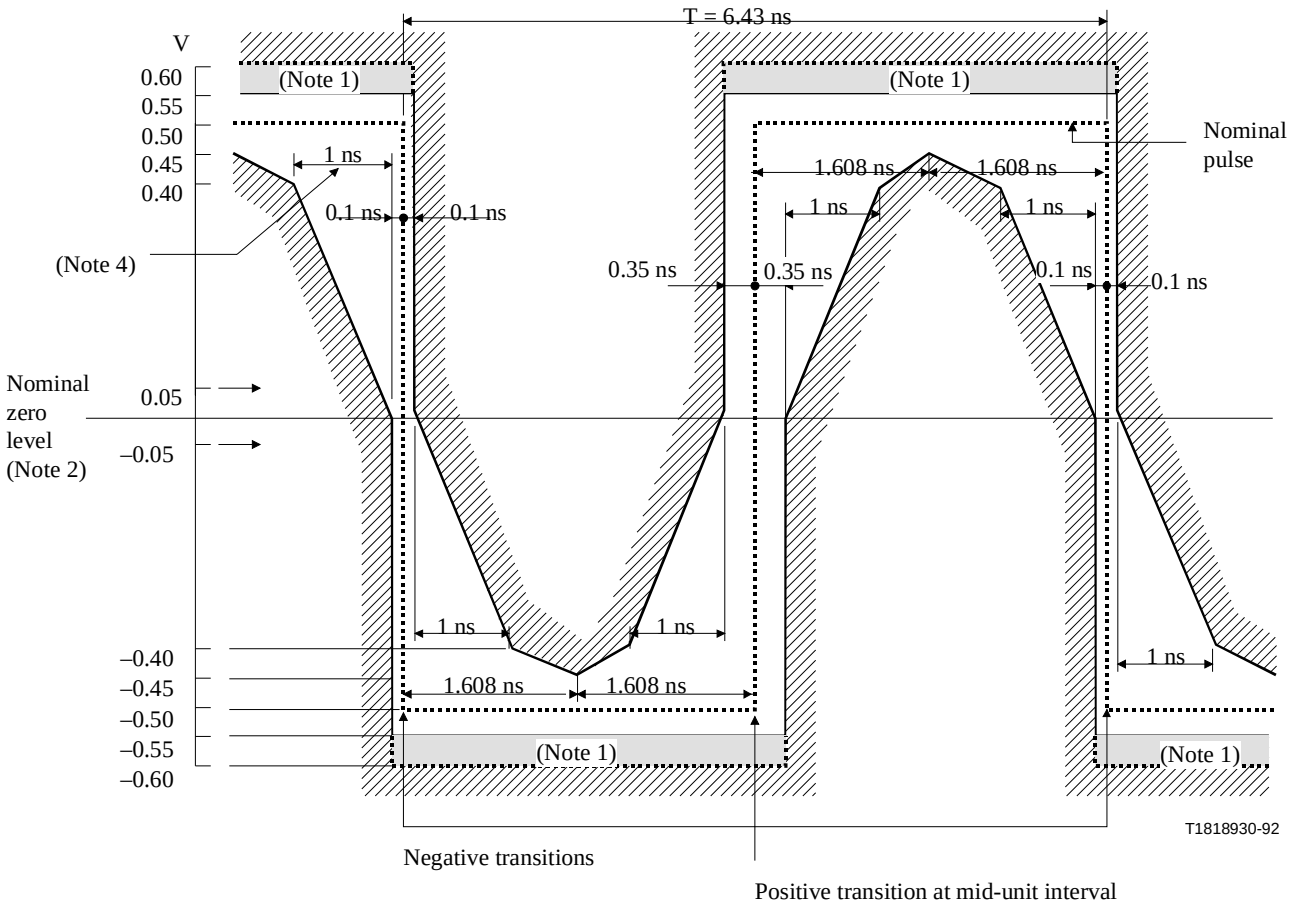
15.2 Specifications at the output ports

The specifications at the output ports are given in Table 12 and in Figures 22 and 23.

NOTE – A method based on the measurement of the levels of the fundamental frequency component, the second (and possibly the third) harmonic of a signal corresponding to the binary all 0s and binary all 1s, is considered to be a perfectly adequate method of checking that the requirements of Table 12 have been met. The relevant values of the harmonic components are under study.

Table 12/G.703 – Specifications at the output ports

Pulse shape	Nominally rectangular and conforming to the masks shown in Figures 22 and 23
Pair(s) in each direction	One coaxial pair
Test load impedance	75 ohms resistive
Peak-to-peak voltage	1 ± 0.1 V
Rise time between 10% and 90% amplitudes of the measured steady state amplitude	≤2 ns
Transition timing tolerance referred to the mean value of the 50% amplitude points of negative transitions	Negative transitions: ±0.1 ns Positive transitions at unit interval boundaries: ±0.5 ns Positive transitions at mid-unit intervals: ± 0.35 ns
Return loss	≥15 dB over frequency range 8 MHz to 240 MHz
Maximum peak-to-peak jitter at an output port	Refer to 4.2/G.825



NOTE 1 – The maximum "steady state" amplitude should not exceed the 0.55 V limit. Overshoots and other transients are permitted to fall into the dotted area, bounded by the amplitude levels 0.55 V and 0.6 V, provided that they do not exceed the steady state level by more than 0.05 V. The possibility of relaxing the amount by which the overshoot may exceed the steady state level is under study.

NOTE 2 – For all measurements using these masks, the signal should be AC coupled, using a capacitor of not less than 0.01 μF, to the input of the oscilloscope used for measurements.

The nominal zero level for both masks should be aligned with the oscilloscope trace with no input signal. With the signal then applied, the vertical position of the trace can be adjusted with the objective of meeting the limits of the masks. Any such adjustment should be the same for both masks and should not exceed ±0.05 V. This may be checked by removing the input signal again and verifying that the trace lies within ±0.05 V of the nominal zero level of the masks.

NOTE 3 – Each pulse in a coded pulse sequence should meet the limits of the relevant mask, irrespective of the state of the preceding or succeeding pulses, with both pulse masks fixed in the same relation to a common timing reference, i.e. with their nominal start and finish edges coincident.

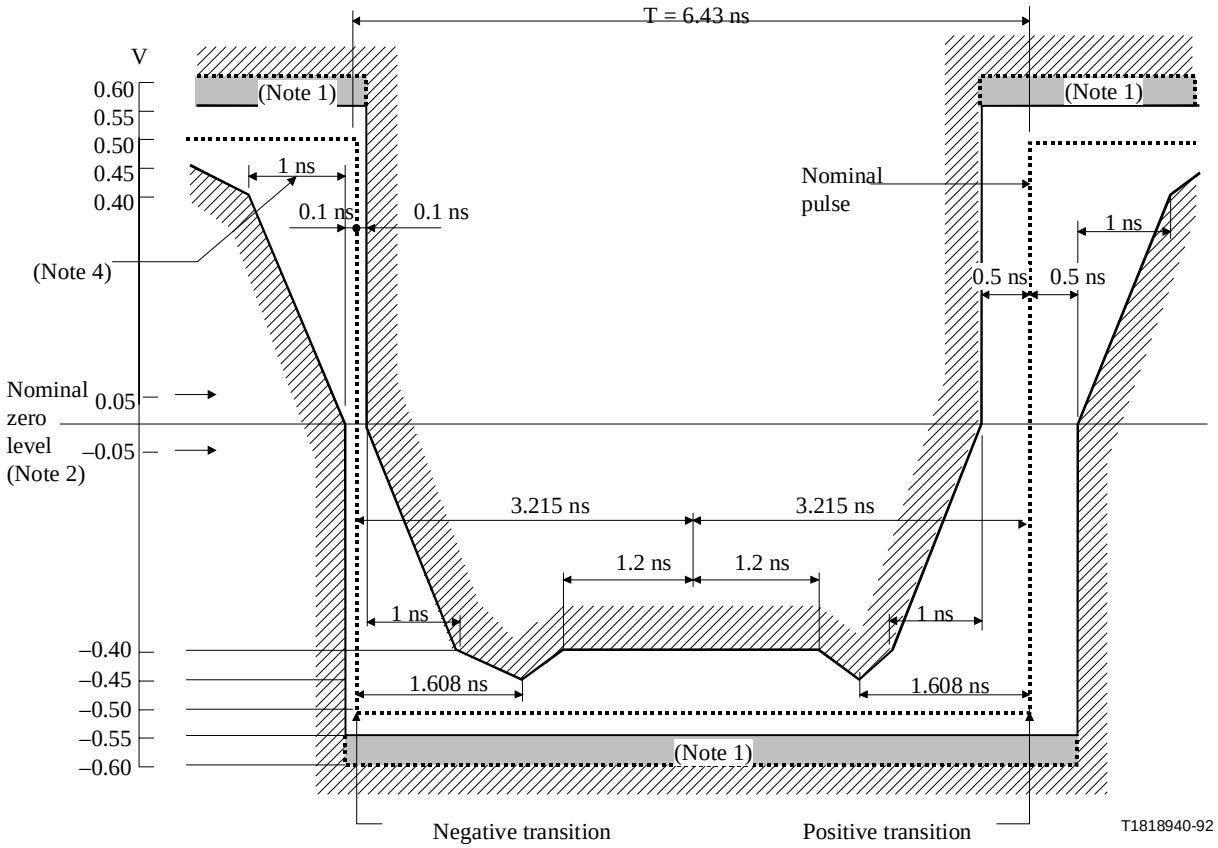
The masks allow for HF jitter caused by intersymbol interference in the output stage, but not for jitter present in the timing signal associated with the source of the interface signal.

When using an oscilloscope technique to determine pulse compliance with the mask, it is important that successive traces of the pulses overlay in order to suppress the effects of low frequency jitter. This can be accomplished by several techniques [e.g. a) triggering the oscilloscope on the measured waveform or b) providing both the oscilloscope and the pulse output circuits with the same clock signal].

These techniques require further study.

NOTE 4 – For the purpose of these masks, the rise time and decay time should be measured between –0.4 V and 0.4 V, and should not exceed 2 ns.

Figure 22/G.703 – Mask of a pulse corresponding to a binary 0 (Note 3)



NOTE 1 – The maximum "steady state" amplitude should not exceed the 0.55 V limit. Overshoots and other transients are permitted to fall into the dotted area, bounded by the amplitude levels 0.55 V and 0.6 V, provided that they do not exceed the steady state level by more than 0.05 V. The possibility of relaxing the amount by which the overshoot may exceed the steady state level is under study.

NOTE 2 – For all measurements using these masks, the signal should be AC coupled, using a capacitor of not less than 0.01 µF, to the input of the oscilloscope used for measurements.

The nominal zero level for both masks should be aligned with the oscilloscope trace with no input signal. With the signal then applied, the vertical position of the trace can be adjusted with the objective of meeting the limits of the masks. Any such adjustment should be the same for both masks and should not exceed ±0.05 V. This may be checked by removing the input signal again and verifying that the trace lies within ±0.05 V of the nominal zero level of the masks.

NOTE 3 – Each pulse in a coded sequence should meet the limits of the relevant mask, irrespective of the state of the preceding or succeeding pulses, with both pulse masks fixed in the same relation to a common timing reference, i.e. with their nominal start and finish edges coincident.

The masks allow for HF jitter caused by intersymbol interference in the output stage, but not for jitter present in the timing signal associated with the source of the interface signal.

When using an oscilloscope technique to determine pulse compliance with the mask, it is important that successive traces of thepulses overlay in order to suppress the effects of low frequency jitter. This can be accomplished by several techniques [e.g. a) triggering the oscilloscope on the measured waveform or b) providing both the oscilloscope and the pulse output circuits with the same clock signal].

These techniques require further study.

NOTE 4 – For the purpose of these masks, the rise time and decay time should be measured between –0.4 V and 0.4 V, and should not exceed 2 ns.

NOTE 5 – The inverse pulse will have the same characteristics, noting that the timing tolerance at the level of the negative and positive transitions are ±0.1 ns and ±0.5 ns respectively.

Figure 23/G.703 – Mask of a pulse corresponding to a binary 1 (Notes 3 and 5)

15.3 Specifications at the input ports

The digital signal presented at the input port should conform to Table 12 and Figures 22 and 23 modified by the characteristics of the interconnecting coaxial pair.

The attenuation of the coaxial pair should be assumed to follow an approximate $\sqrt{f}$ law and to have a maximum insertion loss of 12.7 dB at a frequency of 78 MHz.

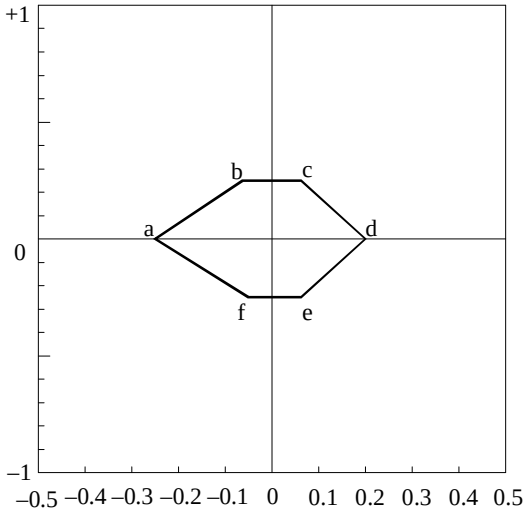
For the jitter to be tolerated at the input port is refer to 4.1/G.825.

The return loss characteristics should be the same as that specified for the output port.

15.4 Specifications at the cross-connect points

– *Signal power level*: A wideband power measurement using a power level sensor with a working frequency range of at least 300 MHz shall be between −2.5 and +4.3 dBm. There shall be no d.c. power transmitted across the interface.

– *Eye diagram*: An eye diagram mask based on the maximum and minimum power levels given above is shown in Figure 24 where the voltage amplitude has been normalized to one, and the time scale is specified in terms of the pulse repetition period T. The corner points of the eye diagram are shown in Figure 24.



Point	Time	Amplitude
a	$-0.25\frac{T}{2}$	–0.00
b	$-0.05\frac{T}{2}$	–0.25
c	$-0.05\frac{T}{2}$	–0.25
d	$-0.20\frac{T}{2}$	–0.00
e	$-0.05\frac{T}{2}$	–0.25
f	$-0.05\frac{T}{2}$	–0.25

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Figure 24/G.703 – STM-1 interface eye diagram

– *Termination*: One coaxial cable shall be used for each direction of transmission.

– *Impedance*: A resistive test load of 75 ohms ± 5% shall be used at the interface for the evaluation of the eye diagram and the electrical parameters of the signal.

15.5 Grounding of outer conductor

The outer conductor of the coaxial pair shall be connected to the bonding network both at the input port and the output port.

NOTE 1 – The cable routing is important if leaving the system block. Consult Recommendation K.27 for guidance.

NOTE 2 – The use of isolation to the bonding network is for further study.

ANNEX A

Definition of codes

This Annex defines the modified alternate mark inversion codes (see Recommendation G.701, item 9005) whose use is specified in this Recommendation.

In these codes, binary 1 bits are generally represented by alternate positive and negative pulses, and binary 0 bits by spaces. Exceptions, as specified for the individual codes, are made when strings of successive 0 bits occur in the binary signal.

In the definitions below, B represents an inserted pulse conforming to the AMI rule (Recommendation G.701, item 9004), and V represents an AMI violation (Recommendation G.701, item 9007).

The encoding of binary signals in accordance with the rules given in this annex includes frame alignment bits, etc.

A.1 Definition of B3ZS (also designated HDB2) and HDB3

Each block of 3 (or 4) successive zeros is replaced by 00V (or 000V respectively) or B0V (B00V). The choice of 00V (000V) or B0V (B00V) is made so that the number of B pulses between consecutive V pulses is odd. In other words, successive V pulses are of alternate polarity so that no d.c. component is introduced.

A.2 Definition of B6ZS and B8ZS

Each block of 6 (or 8) successive zeros is replaced by 0VB0VB (or 000VB0VB respectively).

A.3 Definition of CMI

CMI is a 2-level non-return-to-zero code in which binary 0 is coded so that both amplitude levels, A_1 and A_2, are attained consecutively, each for half a unit time interval (T/2).

Binary 1 is coded by either of the amplitude levels A_1 or A_2, for one full unit time interval (T), in such a way that the level alternates for successive binary 1s.

An example is given in Figure A.1.

NOTE 1 – For binary 0, there is always a positive transition at the midpoint of the binary unit time interval.

NOTE 2 – For binary 1:

a) there is a positive transition at the start of the binary unit time interval if in the preceeding time interval the level was A_1;

b) there is a negative transition at the start of the binary unit time interval if the last binary 1 was encoded by level A_2.

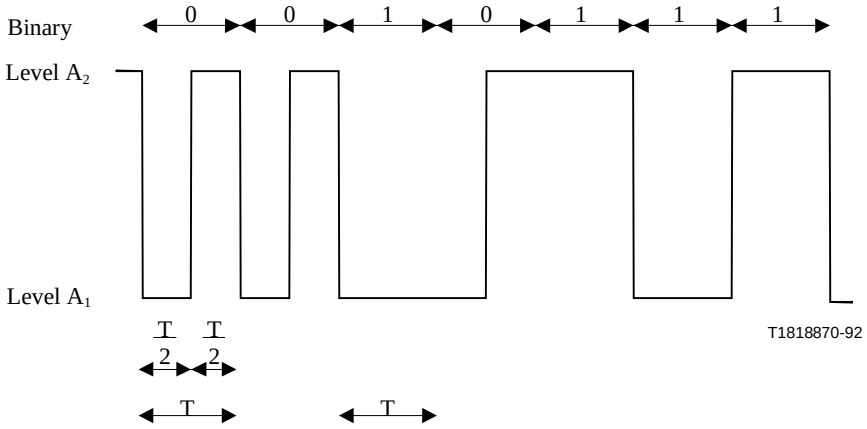


Figure A.1/G.783 – Example of CMI coded binary signal

APPENDIX I

1544 kbit/s specification in the 1991 version of this Recommendation

I.1 General

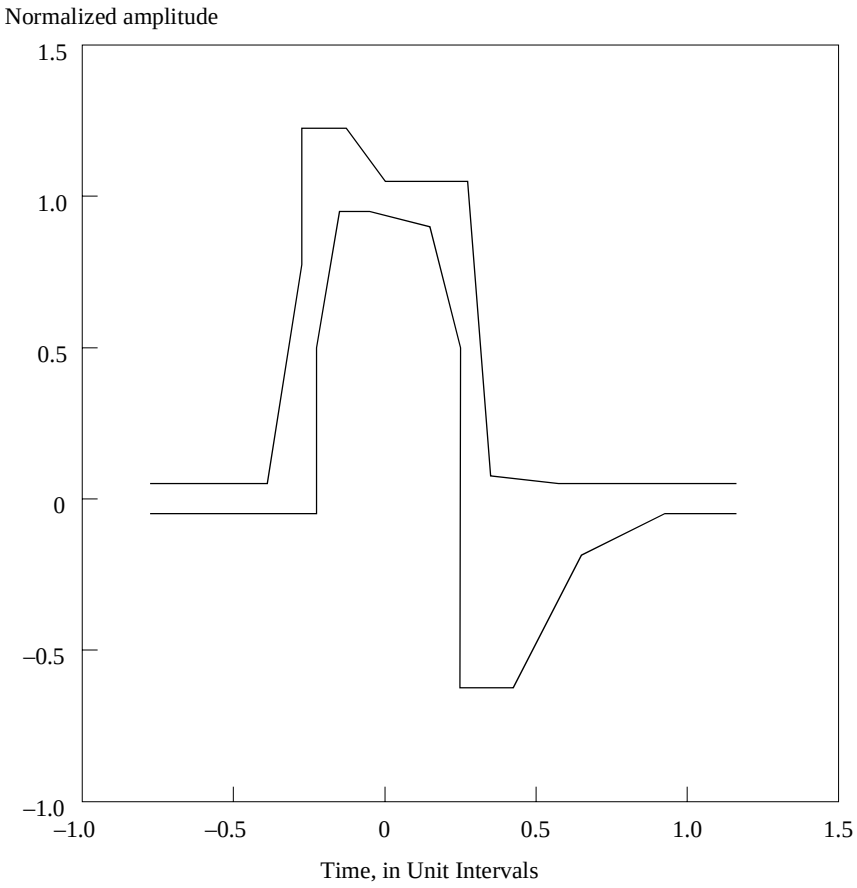
This Appendix describes an earlier 1544 kbit/s interface that included a pulse mask with substantially greater allowance for overshoot on the trailing edge of the pulse than the current standard. While the current pulse mask has been socialized in a number of network compatibility publications since the late 1970s, equipment designed to the earlier specification may be widespread in the network. Hence, designers of equipment need to be aware of the nature of signals that may be delivered to that equipment.

I.2 Interface specification

Most of the interface parameters in Table 4 including power levels and pulse amplitudes apply to the older interface. One major difference is in the line rate tolerance. The older specification calls for a ±130 ppm tolerance, reflecting an earlier, now obsolete, technology for line driver circuitry.

I.3 Pulse mask

Figure I.1 is the 1544 kbit/s pulse mask corresponding to the earlier interface specification. It is based on equipment generating pulses with considerably more overshoot on the trailing edge that is currently allowed in the standard.



Minimum curve		Maximum curve	
Time	**Normalized amplitude**	**Time**	**Normalized amplitude**
– 0.77	– 0.05	– 0.77	0.05
– 0.23	– 0.05	– 0.39	0.05
– 0.23	0.5	– 0.27	0.8
– 0.15	0.95	– 0.27	1.22
– 0.04	0.95	– 0.12	1.22
0.15	0.9	0.0	1.05
0.23	0.5	0.27	1.05
0.23	– 0.62	0.34	0.08
0.42	– 0.62	0.58	0.05
0.66	– 0.2	1.16	0.05
0.93	– 0.05		
1.16	– 0.05		

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Figure I.1/G.703 – Obsolete 1544 kbit/s interface isolated pulse mask and corner points

APPENDIX II

64 and 6312 kHz synchronization interface specification for use in Japan

II.1 64 kHz synchronization interface

The 64 kHz clock signals from the clock supply equipment have the frequencies of a) 64 kHz + 8 kHz or b) 64 kHz + 8 kHz + 400 Hz. Those signals consist of AMI code with a) an 8 kHz bipolar violation, or b) an 8 kHz bipolar violation removed at every 400 Hz.

The signal structures of 64 kHz clock signals are illustrated Figures II.1 and II.2.

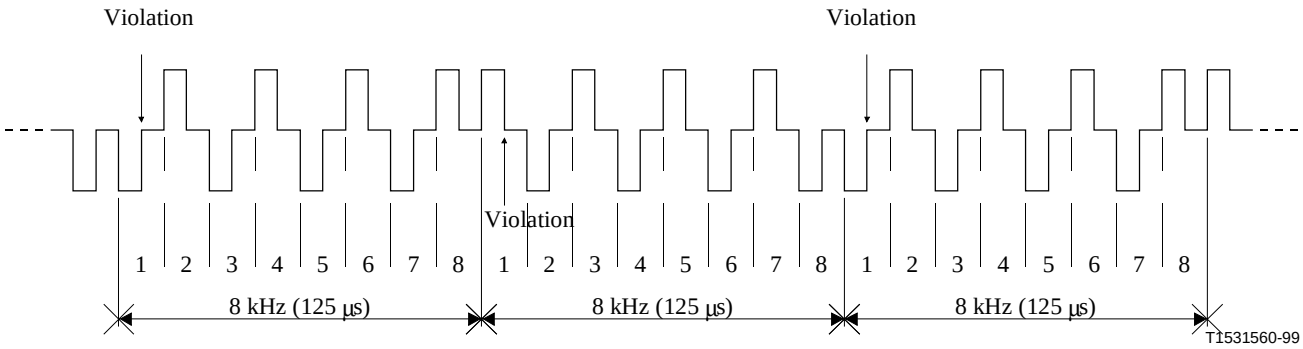

Figure II.1/G.703 – Signal structure of 64 kHz clock interface with a frequency of 64 kHz + 8 kHz

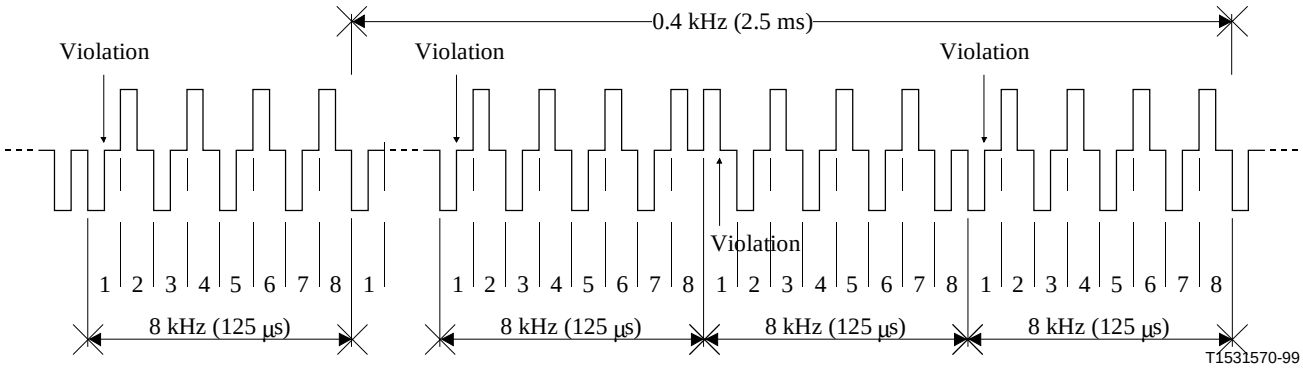

Figure II.2/G.703 – Signal structure of 64 kHz clock interface with a frequency of 64 kHz + 8 kHz + 400 Hz

The specifications of 64 kHz clock signals at input port and output port are shown in Tables II.1 and II.2, respectively.

Table II.1/G.703 – Specification of 64 kHz clock signal at input port

Frequency	a) 64 kHz + 8 kHz or b) 64 kHz + 8 kHz + 400 Hz
Signal format	a) AMI with 8 kHz bipolar violation, b) AMI with 8 kHz bipolar violation removed at every 400 Hz
Alarm condition	Alarm should not be occurred against the amplitude ranged 0.63-1.1 $V_{0\text{-}P}$

Table II.2/G.703 – Specification of 64 kHz clock signal at output port

Frequency	a) 64 kHz + 8 kHz or b) 64 kHz + 8 kHz + 400 Hz
Load impedance	110 ohms resistive
Transmission media	Symmetric pair cable
Pulse width (FWHM)	$\leq 7.8 \pm 0.78$ µs
Amplitude	≤ 1 $V_{0\text{-}P} \pm 0.1$ V

II.2 6312 kHz synchronization interface

Figure II.3 shows the waveform of 6312 kHz clock signal. The specifications of 6312 kHz clock signals at input port and output port are shown in Tables II.3 and II.4, respectively.

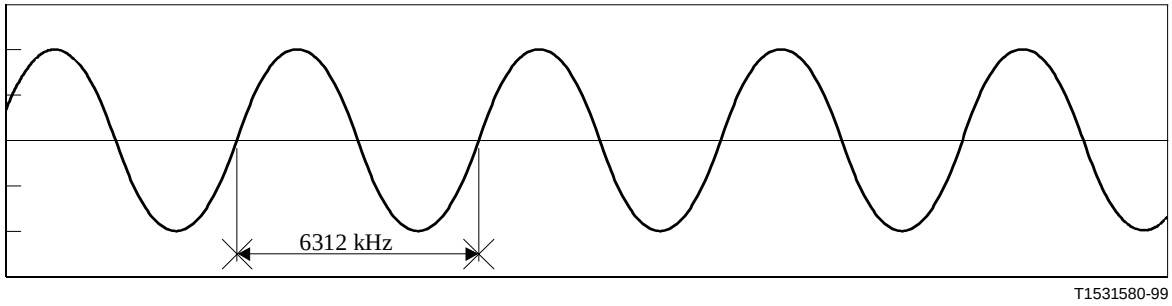

Figure II.3/G.703 – Waveform of 6312 kHz clock signal

Table II.3/G.703 – Specification of 6312 kHz clock signal at input port

Frequency	6312 kHz
Signal format	Sinusoidal wave
Alarm condition	Alarm should not be occurred against the amplitude ranged −16 dBm to +3 dBm

Table II.4/G.703 – Specification of 6312 kHz clock signal at output port

Frequency	6312 kHz
Load impedance	75 ohms resistive
Transmission media	Coaxial pair cable
Amplitude	0 dBm ± 3 dB

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