

ITU-T

TELECOMMUNICATION
STANDARDIZATION SECTOR
OF ITU

G.8264/Y.1364

Corrigendum 1
(11/2009)

SERIES G: TRANSMISSION SYSTEMS AND MEDIA,
DIGITAL SYSTEMS AND NETWORKS

Packet over Transport aspects – Quality and availability
targets

SERIES Y: GLOBAL INFORMATION
INFRASTRUCTURE, INTERNET PROTOCOL ASPECTS
AND NEXT-GENERATION NETWORKS

Internet protocol aspects – Transport

Distribution of timing information through packet
networks

Corrigendum 1

Recommendation ITU-T G.8264/Y.1364 (2008) –
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Distribution of timing information through packet networks

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Summary

Corrigendum 1 to Recommendation ITU-T G.8264/Y.1364 (2008) contains the following editorial and technical corrections:

- Clarification of QL-Failed condition and usage in QL-Disabled mode.
- Clarification of ESMC PDU format.

History

Edition	Recommendation	Approval	Study Group
1.0	ITU-T G.8264/Y.1364	2008-10-29	15
1.1	ITU-T G.8264/Y.1364 (2008) Cor. 1	2009-11-13	15

FOREWORD

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The World Telecommunication Standardization Assembly (WTSA), which meets every four years, establishes the topics for study by the ITU-T study groups which, in turn, produce Recommendations on these topics.

The approval of ITU-T Recommendations is covered by the procedure laid down in WTSA Resolution 1.

In some areas of information technology which fall within ITU-T's purview, the necessary standards are prepared on a collaborative basis with ISO and IEC.

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Distribution of timing information through packet networks

Corrigendum 1

1) Changes in clause 10.2, operation modes

Make the following changes in clause 10.2:

Synchronous operation mode

A synchronous Ethernet interface can be configured in synchronous operation mode.

Its receive side is able to extract the frequency of its input signal and passes it to a system clock (an EEC or better quality clock). It processes the ESMC and extracts the QL. This signal can now be used as a candidate frequency reference.

The transmit part of the interface is locked to the output timing of the system clock and generates the ESMC to transport a QL.

In the particular case of Ethernet interfaces for 1G copper as specified in [IEEE 802.3], these interfaces perform link auto-negotiation to determine the master and slave clocks for the link. In the case where these interfaces are used for synchronous Ethernet, the resulting timing path must be considered if frequency distribution based on synchronous Ethernet is used. The clock master must be consistent with the network synchronization plan.

~~In some application cases, mainly in the access network, it might be possible to recover timing from an Ethernet signal that does not carry an ESMC channel and generate a Synchronous Ethernet signal without ESMC channel. Such usage is under the responsibility of the operator and is for further study.~~

It is an operator choice to utilize a synchronous Ethernet interface as a candidate synchronization interface (i.e., ~~QL Disabled mode~~) in the absence of an ESMC and QL value. Such usage is under the responsibility of the operator and is for further study.

2) Changes to clause 11, SSM for synchronous Ethernet

2.1) *Replace the last two sentences of clause 11.3:*

The protocol behaviour is such that the SSM value is set to DNU if no SSM messages are received after a five second period. Details are contained within the following subclauses.

With:

The protocol behaviour is such that the SSM QL value is considered failed if no ESMC messages are received after a five second period. Details are contained within the following clauses.

2.2) *Make the following changes to clause 11.3.2.2:*

11.3.2.2 QL Reception

The QL state, QL_out is utilized by synchronization selection algorithm described in [ITU-T G.781] (see Annex A of [ITU-T G.781]). For synchronous Ethernet, the slow protocol used for the transmission of the SSM code relies on the use of a "heart-beat" timer. ESMC Information PDUs are sent periodically at a rate of one PDU per second. Lack of reception of an ESMC Information PDU within a five-second period results in SSF=true (QL=QL-FAILED in QL-Enabled

~~mode). the QL being set to DNU. The synchronization reference is now subject to a wait-to-restore period as defined in [ITU-T G.781].~~

The default (initial) value for the QL is SSF=true (QL=QL-FAILED in QL-Enabled mode) ~~DNU~~ and must only change when a valid QL TLV is received.

Upon reception of an event TLV, the QL state is changed to the new QL value, and the information timer is reset.

~~If the NE is operating in QL enabled mode and no QL TLV is received within a five second period, the QL state is set to DNU. The synchronization reference is now subject to a wait to restore period as defined in [ITU-T G.781].~~

3) Clarification of ESMC description

Replace Tables 11-3 and 11-4 with the following tables:

Table 11-3 – ESMC PDU format

Octet number	Size/bits	Field
1-6	6 octets	Destination Address = 01-80-C2-00-00-02 (hex)
7-12	6 octets	Source Address
13-14	2 octets	Slow Protocol Ethertype = 88-09 (hex)
15	1 octet	Slow Protocol Subtype = 0A (hex)
16-18	3 octets	ITU-OUI = 00-19-A7 (hex)
19-20	2 octets	ITU Subtype
21	bits 7:4 (Note 1)	Version
	bit 3	Event flag
	bits 2:0 (Note 2)	Reserved
22-24	3 octets	Reserved
25-1532	36-1490 octets	Data and padding (See point j)
Last 4	4 octets	FCS
NOTE 1 – Bit 7 is the most significant bit of octet 21. Bit 7 to bit 4 (bits 7:4) represent the four-bit version number for the ESMC.		
NOTE 2 – The three least significant bits (bits 2:0) are reserved.		

Table 11-4 – QL TLV format

Octet number	Size/bits	Field
1	8 bits	Type: 0x01
2-3	16 bits	Length: 00-04
4	bits 7:4 (Note)	0x0 (unused)
	bits 3:0	SSM code
NOTE – Bit 7 of octet 4 is the most significant bit. The least significant nibble, bit 3 to bit 0 (bits 3:0) contain the four-bit SSM code.		

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