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Corrigendum 1
(05/2021)

SERIES G: TRANSMISSION SYSTEMS AND MEDIA, DIGITAL SYSTEMS AND NETWORKS

Digital terminal equipments – General

SERIES Y: GLOBAL INFORMATION INFRASTRUCTURE, INTERNET PROTOCOL ASPECTS, NEXT-GENERATION NETWORKS, INTERNET OF THINGS AND SMART CITIES

Internet protocol aspects – Transport

OTU25 and OTU50 short-reach interfaces

Corrigendum 1

Recommendation ITU-T G.709.4/Y.1331.4 (2020) – Corrigendum 1

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For further details, please refer to the list of ITU-T Recommendations.

Recommendation ITU-T G.709.4/Y.1331.4

OTU25 and OTU50 short-reach interfaces

Corrigendum 1

Summary

Corrigendum 1 to Recommendation ITU-T G.709.4/Y.1331.4 (2020) corrects editorial mistakes in the text of clauses 3.2.4, 8.2 and 9.2, the titles of Tables 8-1, 8-2 and 9-2, and text in Table 8-2.

History

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FOREWORD

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The World Telecommunication Standardization Assembly (WTSA), which meets every four years, establishes the topics for study by the ITU-T study groups which, in turn, produce Recommendations on these topics.

The approval of ITU-T Recommendations is covered by the procedure laid down in WTSA Resolution 1.

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In this Recommendation, the expression "Administration" is used for conciseness to indicate both a telecommunication administration and a recognized operating agency.

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Recommendation ITU-T G.709.4/Y.1331.4

OTU25 and OTU50 short-reach interfaces

Corrigendum 1

Editorial note: This is a complete-text publication. Modifications introduced by this corrigendum are shown in revision marks relative to Recommendation ITU-T G.709.4/Y.1334.4 (2020).

1 Scope

This Recommendation specifies 25 Gbit/s and 50 Gbit/s optical transport network (OTN) short-reach interfaces with Reed-Solomon forward error correction codes (OTU25-RS, OTU50-RS) with lower overhead percentage than the Reed-Solomon forward error correction (FEC) code specified for OTUk (k=1,2,3,4) in [ITU-T G.709].

The OTU25-RS and OTU50-RS interfaces complement the OTU25/ODU25 and OTU50/ODU50 functions specified in [ITU-T G.709], with a hard-decision FEC codec, which uses the same overhead percentage (~5.8%) as the FlexO-x-RS FEC codec.

The OTU25-RS and OTU50-RS interfaces may be operated at an approximately 8% and 5% lower rate for use in network scenarios that do not require the support of all clients. Such interfaces are identified as OTU25u-RS and OTU50u-RS interfaces. The OTU25u-RS interface will be equipped with a hard-decision FEC code, which uses a ~3% lower overhead percentage.

This Recommendation makes use of existing [ITU-T G.709], [ITU-T G.798] and [b-ITU-T G-Sup.58] functions by reference and it provides specifications for new functions that are specific to this new interface type. In addition, some introduction material for intended applications is included.

2 References

The following ITU-T Recommendations and other references contain provisions which, through reference in this text, constitute provisions of this Recommendation. At the time of publication, the editions indicated were valid. All Recommendations and other references are subject to revision; users of this Recommendation are therefore encouraged to investigate the possibility of applying the most recent edition of the Recommendations and other references listed below. A list of the currently valid ITU-T Recommendations is regularly published. The reference to a document within this Recommendation does not give it, as a stand-alone document, the status of a Recommendation.

[ITU-T G.709] Recommendation ITU-T G.709/Y.1331 (2020), *Interfaces for the optical transport network*.

[ITU-T G.798] Recommendation ITU-T G.798 (2017), *Characteristics of optical transport network hierarchy equipment functional blocks*.

[IEEE 802.3] IEEE Std 802.3™-2018, IEEE Standard for Ethernet.

[IEEE 802.3cd] IEEE Std 802.3cd™, IEEE Standard for Ethernet, *Amendment 3: Media Access Control Parameters for 50 Gb/s and Physical Layers and Management Parameters for 50 Gb/s, 100 Gb/s, and 200 Gb/s Operation*.

3 Definitions

3.1 Terms defined elsewhere

This Recommendation uses the following terms defined elsewhere:

3.1.1 optical data unit k (ODUk) [ITU-T G.709].

3.1.2 optical transport network (OTN) [ITU-T G.709].

3.1.3 optical payload unit k (OPUk) [ITU-T G.709].

3.2 Terms defined in this Recommendation

This Recommendation defines the following terms:

3.2.1 OTU25-RS: Information structure consisting of an OTU25, plus code word marker, plus Reed-Solomon $(544,514)_{10}$ FEC parity.

3.2.2 OTU25u-RS: Information structure consisting of an OTU25u, plus code word marker, plus Reed-Solomon $(528,514)_{10}$ FEC parity.

3.2.3 OTU50-RS: Information structure consisting of an OTU50, plus alignment marker, plus Reed-Solomon $(544,514)_{10}$ FEC parity.

3.2.4 OTU50u-RS: Information structure consisting of an OTU50u, plus alignment marker, plus Reed-Solomon $(544,514)_{10}$ FEC parity.

4 Abbreviations and acronyms

This Recommendation uses the following abbreviations and acronyms:

AM	Alignment Marker
CMx	Common Marker #x
CPx	Common Pad #x
CWM	Code Word Marker
FEC	Forward Error Correction
LSB	Least Significant Bit
MSB	Most Significant Bit
ODU	Optical Data Unit
ODU*k*	ODU order *k*
OPU	Optical Payload Unit
OPU*k*	OPU order *k*
OTL50.k-RS	group of k Optical Transport Lanes with Reed-Solomon FEC that carry one OTU50
OTN	Optical Transport Network
OTSi	Optical Tributary Signal
OTU	Optical Transport Unit
OTU-RS	Optical Transport Unit with AM/CWM and Reed-Solomon $(528,514)_{10}$ or $(544,514)_{10}$ FEC (e.g., OTU25-RS, OTU50-RS)
RS	Reed Solomon
UMx	Unique Marker #x

5 Conventions

Transmission order: The order of transmission of information in all the diagrams in this Recommendation is first from left to right and then from top to bottom. Within each byte the most significant bit is transmitted first. The most significant bit (bit 1) is illustrated at the left in all the diagrams.

Value of reserved bit(s): The value of an overhead bit, which is reserved or reserved for future international standardization, shall be set to "0".

Value of non-sourced bit(s): Unless stated otherwise, any non-sourced bits shall be set to "0".

6 Introduction

An OTU-RS interface is defined for 25 and 50 Gbit/s short reach interoperable multi-vendor applications, over which a 25 or 50 Gbit/s optical transport unit (OTU) signal is adapted. Such applications include but are not limited to 5G transport over optical transport network (OTN) as described in [b-ITU-T G-Sup.67] and 25G and 50G OTN interfaces on customer premise equipment that support private line services.

The specification of 25 and 50 Gbit/s OTU signals in [ITU-T G.709] excludes interface specific functions such as forward error correction (FEC), scrambling, bit alignment and lane distribution. These functions are specified in this Recommendation.

7 Structure

This clause specifies the basic signal structure for 25 and 50 Gbit/s OTU-RS interfaces.

7.1 Basic signal structure

The OTU-RS interface is specified for short-reach applications.

The information structure for the OTU-RS interface is represented by information containment relationships and information flows. The principal information containment relationship is shown in Figures 7-1 and 7-2.

One OTU25 signal is mapped into an OTU25-RS signal, as illustrated in Figure 7-1. The OTU25-RS interface signal is modulated onto one OTSi and the OTSi is transported via one media element.

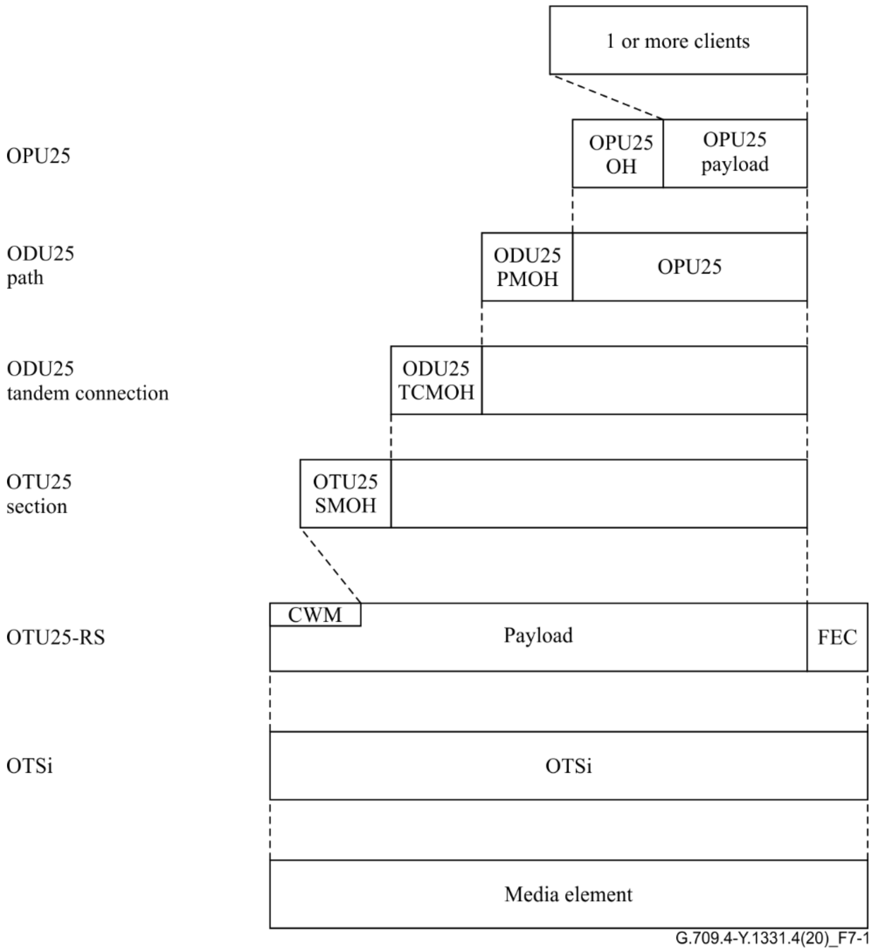

Figure 7-1 – OTU25-RS principal information containment relationship

One OTU50 signal is mapped into an OTU50-RS signal, as illustrated in Figure 7-2. The OTU50-RS interface signal is split into two OTL50.2-RS lane signals which are bit interleaved into a single OTL50.1-RS lane signal. This OTL50.1-RS lane signal is modulated onto one OTSi and the OTSi is transported via one media element.

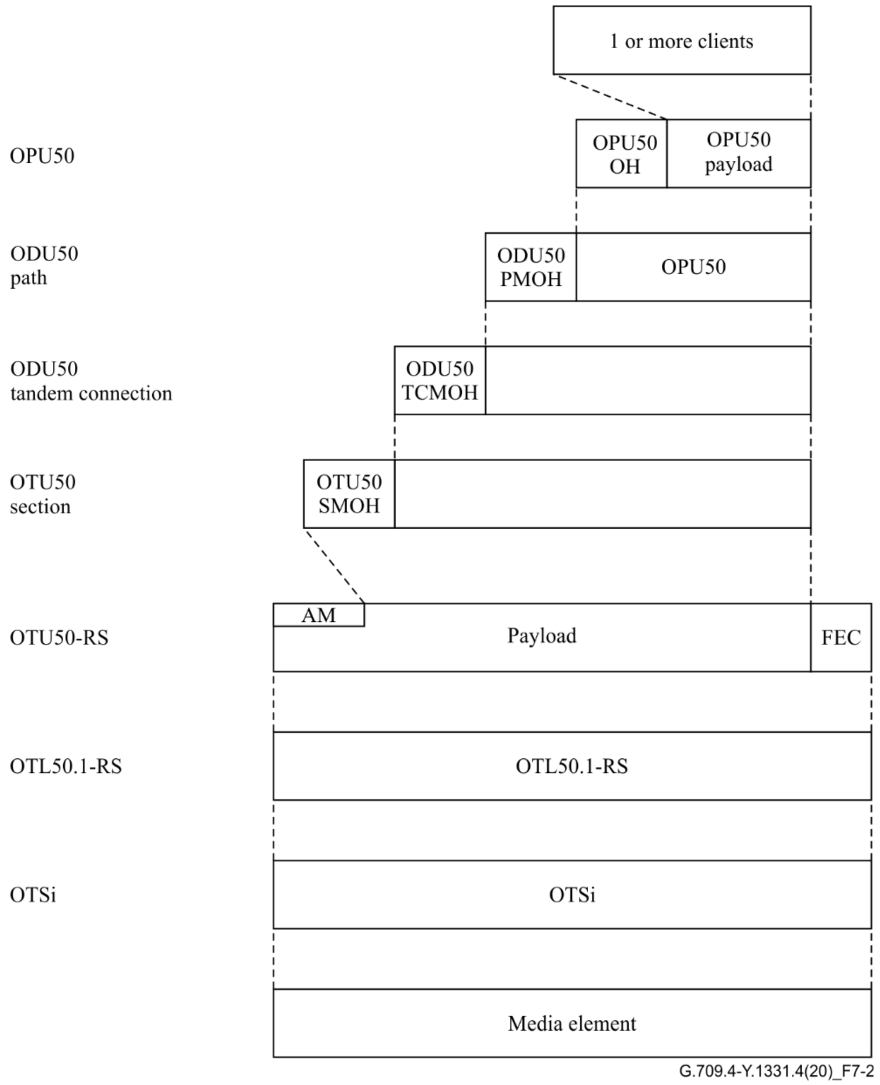

Figure 7-2 – OTU50-RS principal information containment relationship

8 OTU25-RS interface

8.1 Frame structure

The OTU25-RS frame structure is shown in Figure 8-1 and consists of 1024 rows by 5440 1-bit columns.

It contains a frame alignment area with a code word marker (CWM) in row 1, columns 1 to 256, a RS(544,514,10) forward error correction (FEC) parity area in columns 5141 to 5440 and a (1024 × 5140 – 256 =) 5,263,104 bit payload area in the remainder of the frame.

NOTE – The OTU25-RS frame structure is derived from 25 Gbit/s Ethernet clause 108 of [IEEE 802.3] FEC code word marker architecture, without any 66b alignment or 256b/257b transcoding functions and with RS(544,514) instead of RS(528,514) forward error correction.

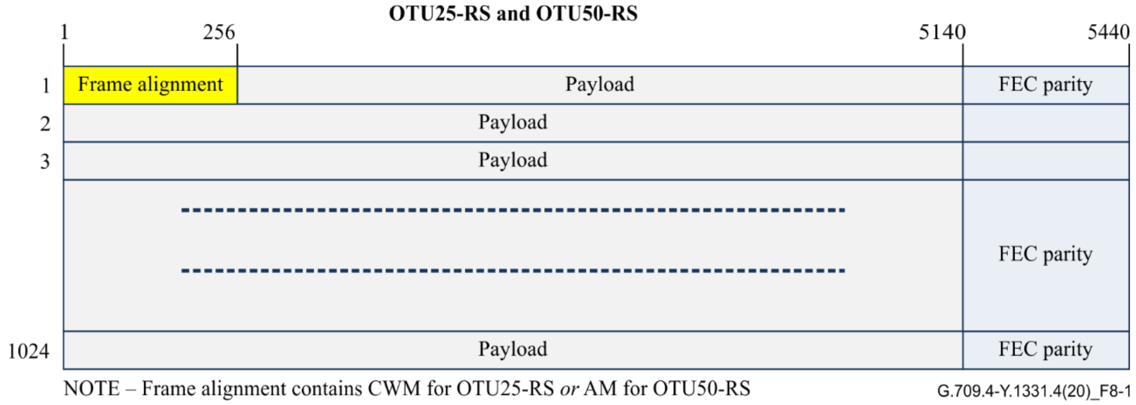

Figure 8-1 – OTU25-RS and OTU50-RS frame structure

8.2 Bit rate and frame period

The bit rate and tolerance of the OTU25-RS signal is defined in Table 8-1.

Table 8-1 – OTU25-RS ~~and OTU50-RS~~ interface bit rate~~s~~

OTU-RS type	OTU-RS nominal bit rate	OTU-RS bit-rate tolerance
OTU25-RS	255/227 × 24 883 200 kbit/s	±20 ppm
NOTE – The nominal OTU25-RS bit rate is approximately: 27 952 493.392 kbit/s.		

The frame ~~and multi-frame~~ period~~s~~ of the OTU25-RS signal is defined in Table 8-2.

Table 8-2 – OTU25-RS ~~and OTU50-RS~~ frame period~~s~~

OTU-RS type	Frame period (Note)
OTU25-RS	199.287~~8~~ µs
NOTE – The period is an approximated value, rounded to 3 decimal places.	

8.3 Overhead

The OTU25-RS frame supports CWM overhead.

8.3.1 CWM format

Code word markers are used for FEC frame alignment. The code word marker (CWM) area length for an OTU25-RS frame is defined as 256 bits, which holds four 64-bit code word markers labelled CWM0 to CWM3 (see Figure 8-2). The value of CWM0 to CWM3 is specified in Table 8-3.

NOTE – The OTU25-RS code word markers reuse the [IEEE 802.3] clause 108.5.2.4 CWM specifications.

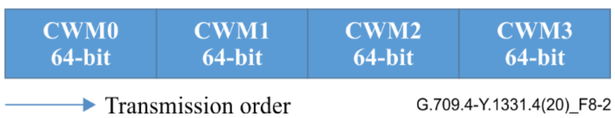

Figure 8-2 – 256-bit CWM format

Table 8-3 – CWM encoding in OTN transmission order

	CWMi Encoding[a] **{M0, M1, M2, U0, M4, M5, M6, U1}**
CWM0	83, 16, 84, CC, 7C, E9, 7B, 33
CWM1	0F, 23, 67, CC, F0, DC, 98, 33
CWM2	A3, A6, D9, CC, 5C, 59, 26, 33
CWM3	45, 9E, BC, CC, BA, 61, 43, 33
NOTE – [a] The value in each byte of this table is in MSB-first transmission order. Note this per-byte ordering is the reverse of code word marker (CWM) values in [IEEE 802.3] Clause 108.5.2.4, which uses an LSB-first bit transmission order.	

8.4 Scrambling

The OTN "frame additive" synchronous scrambler with sequence length of 65535 and generating polynomial $x^{16} + x^{12} + x^3 + x + 1$ is re-used. This is the same scrambler as used for any other OTUk or FlexO-x-<FEC> frame format.

Scrambler synchronization is similar to OTUk[NO FEC] scrambling. This means that the scrambler is synchronized using FAS of the OTU25[1] and operate the scrambler before CWM[2] and FEC parity columns insertion. FEC parity is calculated on scrambled data, so that it shall contain sufficient clock content (same concept as for FlexO-x-RS or 25GE[3] scramblers).

8.5 Forward error correction

The OTU25-RS FEC area contains the Reed-Solomon RS(544,514) FEC codes. The RS(544,514,10) FEC code shall be computed as specified in Annex A.

8.6 Interface format

An OTU25-RS interface presents the OTU25-RS signal in this format on the interface.

NOTE – This interface format is compatible and can reuse optical modules developed for IEEE 25GBASE-R, with OTU25-RS rate support.

The OTU25-RS interface format is intended for applications to be defined by application codes for metro networks.

9 OTU50-RS interface

9.1 Frame structure

The OTU50-RS frame structure is shown in Figure 8-1 and consists of 1024 rows by 5,440 1-bit columns.

It contains a frame alignment area with an alignment marker (AM) in row 1, columns 1 to 256, a RS(544,514,10) forward error correction (FEC) parity area in columns 5141 to 5440 and a (1024 × 5140 – 256 =) 5,263,104 bit payload area in the remainder of the frame.

---

[1] OTU50 in case of OTU50-RS scrambling as specified in clause 9.4.

[2] AM in case of OTU50-RS scrambling as specified in clause 9.4.

[3] 50GE in case of OTU50-RS scrambling as specified in clause 9.4.

NOTE – The OTU50-RS frame structure is derived from 50 Gbit/s Ethernet clause 134 of [IEEE 802.3cd] FEC alignment and lane architecture, without any 66b alignment or 256b/257b transcoding functions.

9.2 Bit rate and frame period

The bit rate and tolerance of the OTU50-RS signal is defined in Table 9-1.

Table 9-1 – OTU50-RS interface bit rate

OTU-RS type	OTU-RS nominal bit rate	OTU-RS bit-rate tolerance
OTU50-RS	255/227 × 49 766 400 kbit/s	±20 ppm
NOTE – The nominal OTU50-RS bit rate is approximately: 55 904 986.784 kbit/s.		

The frame ~~and multi-frame~~ period~~s~~ of the OTU50-RS signal is defined in Table 9-2.

Table 9-2 – ~~OTU25-RS and~~ OTU50-RS frame period~~s~~

OTU-RS type	Frame period (Note)
OTU50-RS	99.643 µs
NOTE – The period is an approximated value, rounded to 3 decimal places.	

9.3 Overhead

The OTU50-RS frame supports AM overhead.

9.3.1 AM format

Alignment markers are used for lane alignment, lane delineation, lane ordering and lane deskewing.

The alignment marker (AM) area length for an OTU50-RS frame is defined as 256 bits, which holds two 128-bit alignment markers #0 and #1.

An alignment marker, as shown in Figure 9-1, consists of a common portion across all lanes, a unique portion per lane and some pad bits.

– CMx = 8-bit common marker field (common across lanes) – used for aligning lanes
– UMx = 8-bit unique marker field – used for identifying lanes
– CPx = 8-bit common pad field – used for providing a DC balance when multiplexing lanes.

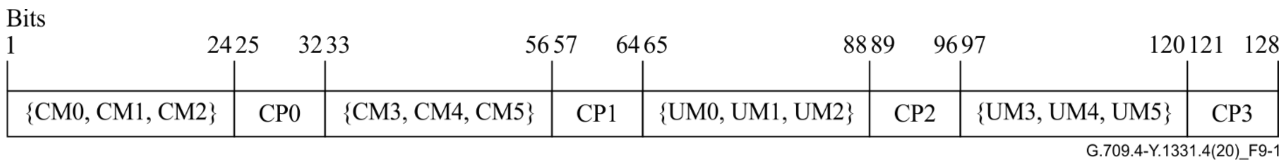

Figure 9-1 – Alignment marker format

Table 9-3 – OTU50-RS alignment marker encodings

am[i]	Encoding[1]															
	CM0	**CM1**	**CM2**	**CP0**	**CM3**	**CM4**	**CM5**	**CP1**	**UM0**	**UM1**	**UM2**	**CP2**	**UM3**	**UM4**	**UM5**	**CP3**
0	09	6E	E2	AA	F6	91	1D	55	A3	A6	D9	AA	5C	59	26	55
1	09	6E	E2	AA	F6	91	1D	55	45	9E	BC	AA	BA	61	43	55
NOTE – The value in each byte of this table is in MSB-first transmission order. Note this per-byte ordering is the reverse of alignment marker (AM) values in IEEE 802.3 Table 82-3, which uses an LSB-first bit transmission order.																

The 256-bit OTU50-RS alignment marker area contains 10-bit interleaved parts of am_0 and am_1 as illustrated in Figure 9-2. The 256 bits contain the 10-bit interleaved parts of am_0 to am_1 in the order am_0, am_1, am_0, am_1, am_0, etc. The last 16 bits contain the last 8 bits of am_0 and the last 8 bits of am_1.

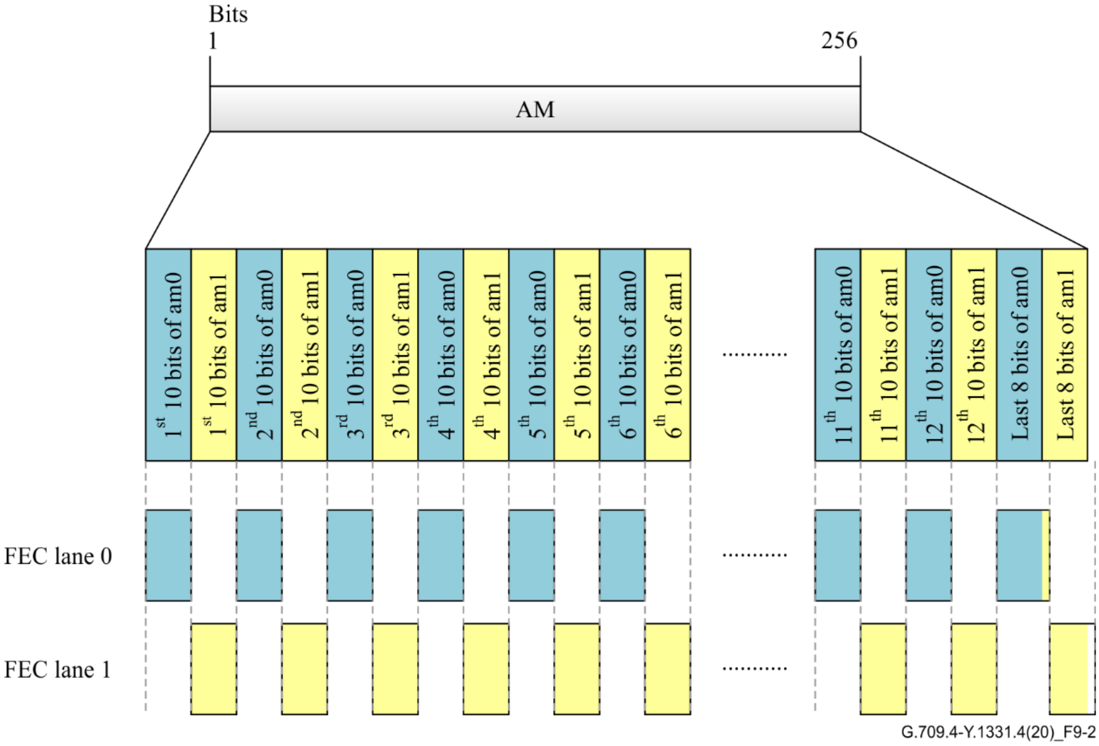

Figure 9-2 – OTU50-RS alignment marker area with two interleaved lane alignment markers

The OTU50-RS frame signal supports subsequent distribution into two logical FEC lanes, numbered 0 and 1. FEC lane 0 carries the 128-bit alignment marker #0 (am_0) as specified in Table 9-3 plus the first two bits of CP3 of alignment marker #1 as illustrated in Figure 9-2. FEC lane 1 carries the 128-bit alignment marker #1 (am_1) as specified in Table 9-3, minus the first two bits of CP3.

9.4 Scrambling

Refer to clause 8.4.

9.5 Forward error correction

The OTU50-RS FEC area contains the Reed-Solomon RS(544,514) FEC codes. The RS(544,514,10) FEC code shall be computed as specified in Annex A.

9.6 Interface format

An OTU50-RS interface presents the OTU50-RS signal in an OTL50.1-RS interface format.

NOTE 1 – This interface format is compatible and can reuse optical modules developed for IEEE 50GBASE-R, with OTU50-RS rate support.

The OTU50-RS bits are distributed to two logical OTL50.2-RS lanes, in groups of 10-bits, in a round robin distribution scheme from the lowest to the highest numbered lanes. The specific scheme of distribution is specified in clause 134 of [IEEE 802.3cd] for 50GBASE-R interface. Each OTL50.2-RS logical lane is synchronous to the OTU50-RS frame.

Each OTU50-RS frame contains 5440 × 1024 = 5,570,560 bits. Each logical OTL50.2-RS lane will carry 50% of these bits, which are 2,785,280 bits, or 278,528 10-bit blocks.

NOTE 2 – Figure 9-2 illustrates the 10-bit distribution of the alignment marker to the two logical lanes.

The physical lane of an OTL50.1-RS is generated by bit multiplexing the two logical OTL50.2-RS lanes onto the physical lane.

The tolerated skew between logical lanes in an OTL50.1-RS interface signal is at least 180 ns.

The bit rate and tolerance of the OTL50.1-RS signal are the same as the bit rate and tolerance of the OTU50-RS signal.

The OTL50.1-RS interface format is intended for applications to be defined by application codes for metro networks.

10 Mapping OTU25 and OTU50 signal into OTU25-RS and OTU50-RS

Mapping an OTU25 signal into the OTU25-RS payload area is done by means of bit-synchronous mapping of 128-bit blocks of the OTU25 frame as illustrated in Figure 10-1. The 128-bit blocks of the OTU25 frames will float in the OTU25-RS payload area.

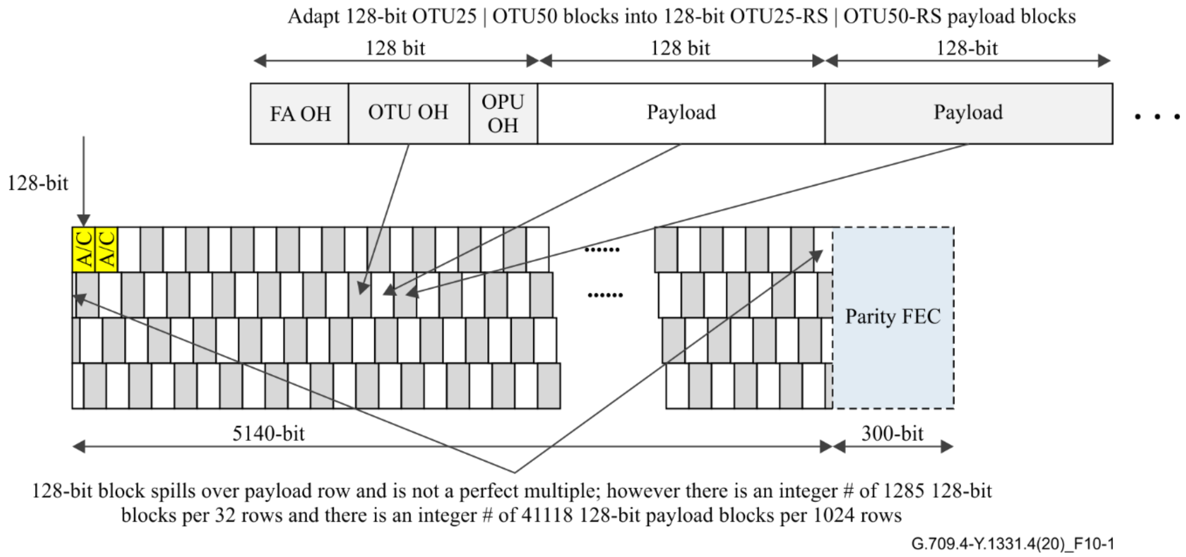

Figure 10-1 – 128-bit based mapping of OTU25 into OTU25-RS and OTU50 into OTU50-RS

Mapping an OTU50 signal into the OTU50-RS payload area is done by means of bit-synchronous mapping of 128-bit blocks of the OTU50 as illustrated in Figure 10-1. The 128-bit blocks of the OTU50 frames will float in the OTU50-RS payload area.

Annex A

Forward error correction for OTU-RS using 10-bit interleaved RS(544,514) codecs

(This annex forms an integral part of this Recommendation.)

NOTE – The OTU-RS FEC is based on RS(544, 514,10), as specified in clause 91.5.2.7 of [IEEE 802.3].

The forward error correction for the OTU-RS uses a single codec using a Reed-Solomon RS(544,514) code. The RS(544,514) code is a non-binary code (the FEC algorithm operates on 10-bit symbols) and belongs to the family of systematic linear cyclic block codes.

For FEC processing, an OTU-RS row is processed by the FEC encoder/decoder. The 10-bit FEC parity check blocks are calculated over the 10-bit information blocks 1 to 514 of each row and transmitted in 10-bit blocks 515 to 544 of the same row, as shown in Figure A.1.

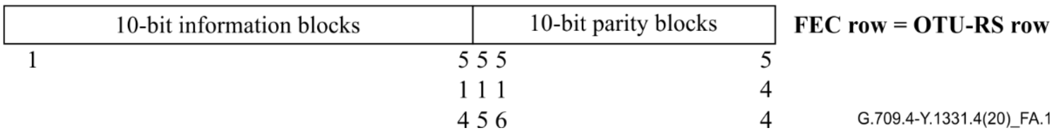

Figure A.1 – FEC row

The 10-bit blocks in an OTU-RS row are defined by: 10 × (i – 1) (for i = 1...544).

The generator polynomial of the code is given by:

$$G(z) = \prod_{i=0}^{29} \left(z - \alpha^{i}\right)$$

where α is a root of the binary primitive polynomial $x^{10} + x^3 + 1$.

The FEC code word (see Figure A.2) consists of 10-bit information blocks and parity blocks (FEC redundancy) and is represented by the polynomial:

$$C(z) = I(z) + R(z)$$

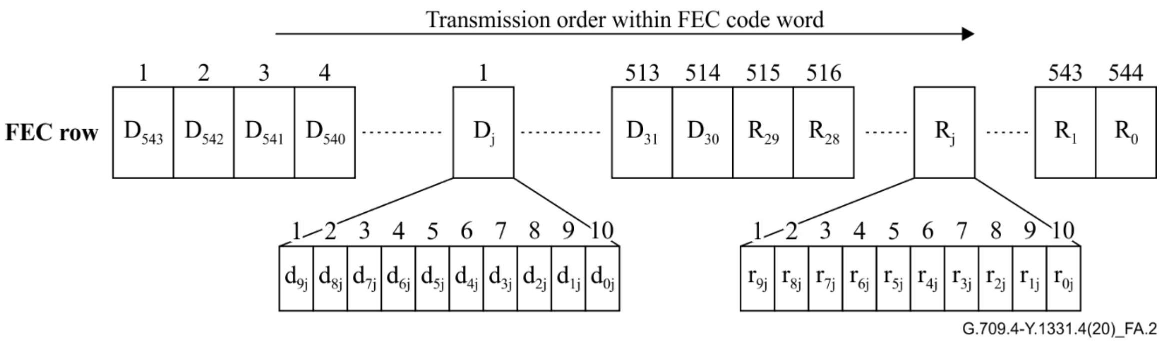

Figure A.2 – RS(544,514) FEC code word

10-bit information blocks are represented by:

$$I(z) = D_{543} \cdot z^{543} + D_{542} \cdot z^{542} + \cdots + D_{30} \cdot z^{30}$$

Where D_j (j = 30 to 543) is the 10-bit information block represented by an element out of GF(256) and:

$$D_j = d_{9j} \cdot \alpha^9 + d_{8j} \cdot \alpha^8 + \cdots + d_{1j} \cdot \alpha^1 + d_{0j}$$

Bit d_{9j} is the MSB and d_{0j} the LSB of the 10-bit information block.

D_{543} corresponds to 10-bit block 1 in the FEC row and D_{30} to 10-bit block 514.

10-bit parity blocks are represented by:

$$R(z) = R_{29} \cdot z^{29} + R_{28} \cdot z^{28} + \cdots + R_1 \cdot z^1 + R_0$$

Where R_j (j = 0 to 29) is the 10-bit parity block represented by an element out of GF(2^{10}) and:

$$R_j = r_{9j} \cdot \alpha^9 + r_{8j} \cdot \alpha^8 + \cdots + r_{1j} \cdot \alpha^1 + r_{0j}$$

Bit r_{9j} is the MSB and r_{0j} the LSB of the 10-bit parity block.

R_{29} corresponds to the 10-bit block 515 in the FEC row and R_0 to 10-bit block 544.

R(z) is calculated by:

$$R(z) = I(z) \bmod G(z)$$

where "mod" is the modulo calculation over the code generator polynomial *G(z)* with elements out of the GF(2^{10}). Each element in GF(2^{10}) is defined by the binary primitive polynomial $x^{10} + x^3 + 1$.

The Hamming distance of the RS(544,514) code is d_{min} = 31. The code can correct up to 15 symbol errors in the FEC code word when it is used for error correction. The FEC can detect up to 30 symbol errors in the FEC code word when it is used for error detection capability only.

Annex B

OTU25u-RS and OTU50u-RS interfaces

(This annex forms an integral part of this Recommendation.)

B.1 Introduction

In network applications that do not require support of all client signals, the OTU25u-RS interface may be operated at an 8.4% lower rate and the OTU50u-RS interface may be operated at a 5.2% lower rate. The bit rates of such "under-clocked" OTU25u-RS and OTU50u-RS are specified in this annex. All other OTU25-RS and OTU50-RS specifications apply for the OTU25u-RS and OTU50u-RS, with exception of the forward error correction and frame structure of the OTU25u-RS (i.e., different FEC parity area). The OTU25u-RS frame structure and forward error correction is therefore specified in this annex as well.

B.2 OTU25u-RS frame structures

The OTU25u-RS frame structure is illustrated in Figure B.1. It consists of 1024 rows by 5280 1-bit columns and a frame alignment overhead area with a CWM plus RS(528,514,10) FEC.

NOTE – The OTU25u-RS FEC is different from the OTU25-RS FEC.

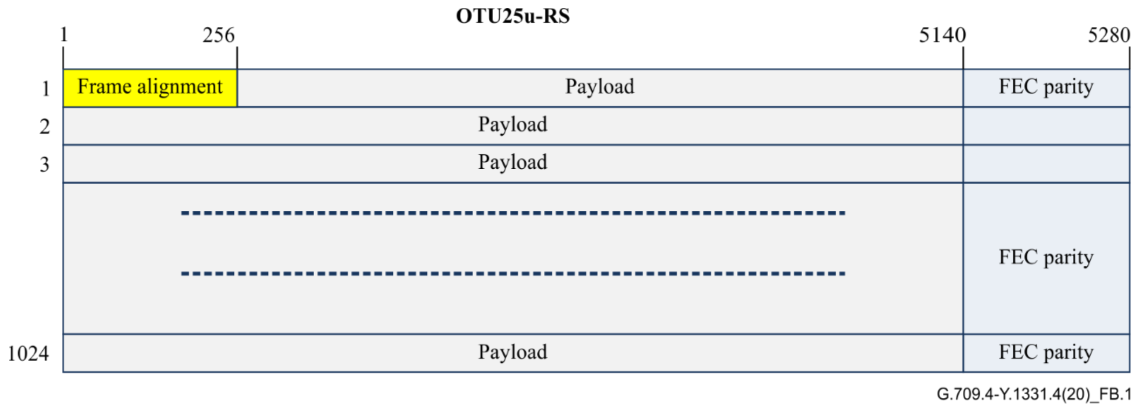

Figure B.1 – OTU25u-RS frame structure

B.3 Bit rates and frame periods

The bit rate and tolerance of the OTU25u-RS and OTU50u-RS signals are defined in Table B.1.

The frame periods of the OTU25u-RS and OTU50u-RS are defined in Table B.2.

Table B.1 – OTU25u-RS and OTU50u-RS interface bit rates

OTU-RS type	OTU-RS nominal bit rate	OTU-RS bit-rate tolerance
OTU25u-RS	660/637 × 24 883 200 kbit/s	±20 ppm
OTU50u-RS	680/637 × 49 766 400 kbit/s	
NOTE – The nominal OTU25u-RS and OTU50u-RS bit rates are approximately: 25 781 651.491 kbit/s (OTU25u-RS), 53 125 827.316 kbit/s (OTU50u-RS).		

Table B.2 – OTU25u-RS and OTU50u-RS frame periods

OTU-RS type	Frame period (Note)
OTU25u-RS	209.712 µs
OTU50u-RS	104.856 µs
NOTE – The period is an approximated value, rounded to 3 decimal places.	

B.4 OTU25u-RS forward error correction

The OTU25u-RS FEC area contains the Reed-Solomon RS(528,514) FEC codes. The RS(528,514,10) FEC code shall be computed as specified in Annex C.

B.5 Interfaces

B.5.1 OTU25u-RS

An OTU25u-RS interface presents the OTU25u-RS signal in this format on the interface.

NOTE – This interface format is compatible and can reuse optical modules developed for IEEE 25GBASE-R.

The OTU25u-RS interface format is intended for applications to be defined by application codes for metro networks.

B.5.2 OTU50u-RS

An OTU50u-RS interface presents the OTU50u-RS signal in an OTL50u.1-RS interface format.

NOTE – This interface format is compatible and can reuse optical modules developed for IEEE 50GBASE-R.

The OTL50u.1-RS interface format and tolerated skew are the same as the OTL50.1-RS interface format and tolerated skew.

The bit rate and tolerance of the OTL50u.1-RS interface signal are the same as the bit rate and tolerance of the OTU50u-RS signal.

The OTL50u.1-RS interface format is intended for applications to be defined by application codes for metro networks.

Annex C

Forward error correction for OTU-RS using 10-bit interleaved RS(528,514) codecs

(This annex forms an integral part of this Recommendation.)

NOTE – The OTU-RS FEC is based on RS(528, 514,10), as specified in clause 91.5.2.7 of [IEEE 802.3].

The forward error correction for the OTU-RS uses a single codec using a Reed-Solomon RS(528,514) code. The RS(528,514) code is a non-binary code (the FEC algorithm operates on 10-bit symbols) and belongs to the family of systematic linear cyclic block codes.

For FEC processing, an OTU-RS row is processed by the FEC encoder/decoder. The 10-bit FEC parity check blocks are calculated over the 10-bit information blocks 1 to 514 of each row and transmitted in 10-bit blocks 515 to 528 of the same row, as shown in Figure C.1.

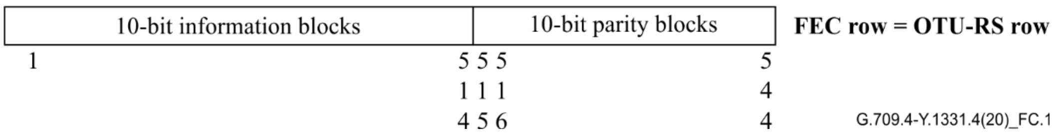

Figure C.1 – FEC row

The 10-bit blocks in an OTU-RS row are defined by: 10 × (i – 1) (for i = 1...528).

The generator polynomial of the code is given by:

$$G(Z) = \prod_{i=0}^{13}(z - \alpha^{i})$$

where α is a root of the binary primitive polynomial $x^{10} + x^{3} + 1$.

The FEC code word (see Figure C.2) consists of 10-bit information blocks and parity blocks (FEC redundancy) and is represented by the polynomial:

$$C(z) = I(z) + R(z)$$

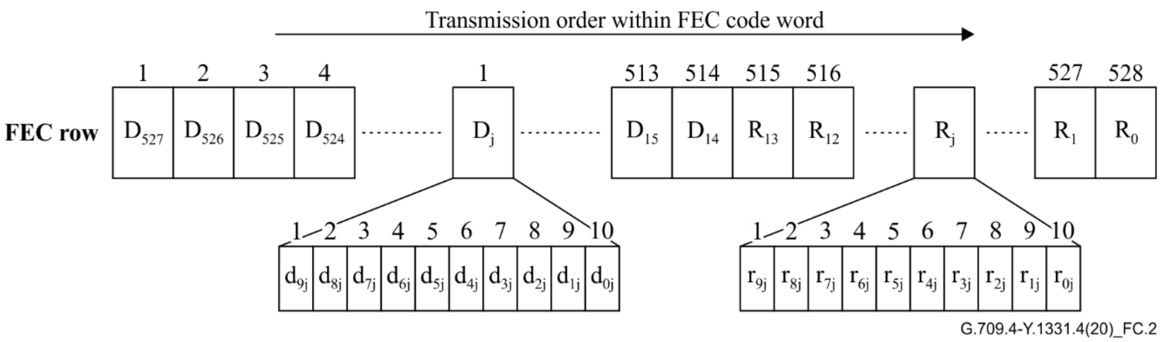

Figure C.2 – RS(544,514) FEC code word

10-bit information blocks are represented by:

$$I(z) = D_{527} \cdot z^{527} + D_{526} \cdot z^{526} + \cdots + D_{14} \cdot z^{14}$$

Where D_j (j = 15 to 527) is the 10-bit information block represented by an element out of GF(256) and:

$$D_j = d_{9j} \cdot \alpha^9 + d_{8j} \cdot \alpha^8 + \cdots + d_{1j} \cdot \alpha^1 + d_{0j}$$

Bit d_{9j} is the MSB and d_{0j} the LSB of the 10-bit information block.

D_{527} corresponds to 10-bit block 1 in the FEC row and D_{14} to 10-bit block 514.

10-bit parity blocks are represented by:

$$R(z) = R_{13} \cdot z^{13} + R_{12} \cdot z^{12} + \cdots + R_1 \cdot z^1 + R_0$$

Where R_j (j = 0 to 29) is the 10-bit parity block represented by an element out of $GF(2^{10})$ and:

$$R_j = r_{9j} \cdot \alpha^9 + r_{8j} \cdot \alpha^8 + \cdots + r_{1j} \cdot \alpha^1 + r_{0j}$$

Bit r_{9j} is the MSB and r_{0j} the LSB of the 10-bit parity block.

R_{29} corresponds to the 10-bit block 515 in the FEC row and R_0 to 10-bit block 544.

R(z) is calculated by:

$$R(z) = I(z) \bmod G(z)$$

where "mod" is the modulo calculation over the code generator polynomial *G(z)* with elements out of the $GF(2^{10})$. Each element in $GF(2^{10})$ is defined by the binary primitive polynomial $x^{10} + x^3 + 1$.

The Hamming distance of the RS(528,514) code is $d_{min} = 15$. The code can correct up to 7 symbol errors in the FEC code word when it is used for error correction. The FEC can detect up to 14 symbol errors in the FEC code word when it is used for error detection capability only.

Bibliography

[b-ITU-T G-Sup.58] ITU-T G-series Recommendations – Supplement 58 (2020), *Optical transport network module framer interfaces*.

[b-ITU-T G-Sup.67] ITU-T G-series Recommendations – Supplement 67 (2019), *Application of optical transport network Recommendations to 5G transport*.

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