International Telecommunication Union

ITU-T

TELECOMMUNICATION
STANDARDIZATION SECTOR
OF ITU

G.707/Y.1322

Corrigendum 2

(08/2005)

SERIES G: TRANSMISSION SYSTEMS AND MEDIA, DIGITAL SYSTEMS AND NETWORKS

Digital terminal equipments – General

SERIES Y: GLOBAL INFORMATION INFRASTRUCTURE, INTERNET PROTOCOL ASPECTS AND NEXT-GENERATION NETWORKS

Internet protocol aspects – Transport

Network node interface for the synchronous digital hierarchy (SDH)

Corrigendum 2

ITU-T Recommendation G.707/Y.1322 (2003) – Corrigendum 2

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ITU-T Recommendation G.707/Y.1322

Network node interface for the synchronous digital hierarchy (SDH)

Corrigendum 2

Summary

This corrigendum contains editorial and technical corrections to ITU-T Rec. G.707/Y.1322 (12/2003), Amendment 1 (08/2004) and Corrigendum 1 (06/2004):

- terms removed with reference to ITU-T Rec. G.780/Y.1351;
- VC concatenation clarification;
- additional Appendix XIX illustrating VCAT mapping.

Source

Corrigendum 2 to ITU-T Recommendation G.707/Y.1322 (2003) was approved on 22 August 2005 by ITU-T Study Group 15 (2005-2008) under the ITU-T Recommendation A.8 procedure.

FOREWORD

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The World Telecommunication Standardization Assembly (WTSA), which meets every four years, establishes the topics for study by the ITU-T study groups which, in turn, produce Recommendations on these topics.

The approval of ITU-T Recommendations is covered by the procedure laid down in WTSA Resolution 1.

In some areas of information technology which fall within ITU-T's purview, the necessary standards are prepared on a collaborative basis with ISO and IEC.

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As of the date of approval of this Recommendation, ITU had received notice of intellectual property, protected by patents, which may be required to implement this Recommendation. However, implementors are cautioned that this may not represent the latest information and are therefore strongly urged to consult the TSB patent database.

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Network node interface for the synchronous digital hierarchy (SDH)

Corrigendum 2

1) Terms to be removed because they are defined in ITU-T Rec. G.780/Y.1351

The following table identifies the target term, with appropriate replacement text for the definition.

Term	Replacement text
3.1 synchronous digital hierarchy (SDH): The SDH is a hierarchical set of digital transport structures, standardized for the transport of suitably adapted payloads over physical transmission networks.	**3.1 synchronous digital hierarchy (SDH)**: See ITU-T Rec. G.780/Y.1351.
3.2 synchronous transport module (STM): An STM is the information structure used to support section layer connections in the SDH. It consists of information payload and Section Overhead (SOH) information fields organized in a block frame structure which repeats every 125 μs. The information is suitably conditioned for serial transmission on the selected media at a rate which is synchronized to the network. A basic STM is defined at 155 520 kbit/s. This is termed STM-1. Higher capacity STMs are formed at rates equivalent to N times this basic rate. STM capacities for N=4, N=16, N=64 and N=256 are defined; higher values are under consideration. The STM-0 comprises a single administrative unit of level 3. The STM-N, N ≥ 1, comprises a single administrative unit group of level N (AUG-N) together with the SOH. The STM-N hierarchical bit rates are given in 6.3.	**3.2 synchronous transport module (STM):** See ITU-T Rec. G.780/Y.1351.

Term	Replacement text
3.3 virtual container-n (VC-n): A virtual container is the information structure used to support path layer connections in the SDH. It consists of information payload and Path Overhead (POH) information fields organized in a block frame structure which repeats every 125 or 500 µs. Alignment information to identify VC-n frame start is provided by the server network layer. Two types of virtual containers have been identified. – *Lower order virtual container-n: VC-n (n=1, 2, 3)* This element comprises a single container-n (n=1, 2, 3) plus the lower order virtual container POH appropriate to that level. – *Higher order virtual container-n: VC-n (n=3, 4)* This element comprises either a single container-n (n=3, 4) or an assembly of Tributary Unit Groups (TUG-2s or TUG-3s), together with virtual container POH appropriate to that level.	**3.3 virtual container-n (VC-n)**: See ITU-T Rec. G.780/Y.1351.
3.4 administrative unit-n (AU-n): An administrative unit is the information structure which provides adaptation between the higher order path layer and the multiplex section layer. It consists of an information payload (the higher order virtual container) and an administrative unit pointer which indicates the offset of the payload frame start relative to the multiplex section frame start. Two administrative units are defined. The AU-4 consists of a VC-4 plus an administrative unit pointer which indicates the phase alignment of the VC-4 with respect to the STM-N frame. The AU-3 consists of a VC-3 plus an administrative unit pointer which indicates the phase alignment of the VC-3 with respect to the STM-N frame. In each case, the administrative unit pointer location is fixed with respect to the STM-N frame. One or more administrative units occupying fixed, defined positions in an STM payload are termed an Administrative Unit Group (AUG). An AUG-1 consists of a homogeneous assembly of AU-3s or an AU-4.	**3.4 administrative unit-n (AU-n)**: See ITU-T Rec. G.780/Y.1351.

<table>
<tr><th>Term</th><th>Replacement text</th></tr>
<tr><td>

3.5 tributary unit-n (TU-n): A tributary unit is an information structure which provides adaptation between the lower order path layer and the higher order path layer. It consists of an information payload (the lower order virtual container) and a tributary unit pointer which indicates the offset of the payload frame start relative to the higher order virtual container frame start.

The TU-n (n=1, 2, 3) consists of a VC-n together with a tributary unit pointer.

One or more tributary units, occupying fixed, defined positions in a higher order VC-n payload is termed a Tributary Unit Group (TUG). TUGs are defined in such a way that mixed capacity payloads made up of different size tributary units can be constructed to increase flexibility of the transport network.

A TUG-2 consists of a homogeneous assembly of identical TU-1s or a TU-2.

A TUG-3 consists of a homogeneous assembly of TUG-2s or a TU-3.

</td><td>

3.5 tributary unit-n (TU-n): See ITU-T Rec. G.780/Y.1351.

</td></tr>
<tr><td>

3.6 container-n (n=1-4): A container is the information structure which forms the network synchronous information payload for a virtual container. For each of the defined virtual containers there is a corresponding container. Adaptation functions have been defined for many common network rates into a limited number of standard containers. These include those rates already defined in ITU-T Rec. G.702. Further adaptation functions will be defined in the future for new broadband rates.

</td><td>

3.6 container-n (n=1-4): See ITU-T Rec. G.780/Y.1351.

</td></tr>
<tr><td>

3.7 network node interface (NNI): The interface at a network node which is used to interconnect with another network node.

Figure 3-1 gives a possible network configuration to illustrate the location of NNI specified in this Recommendation.

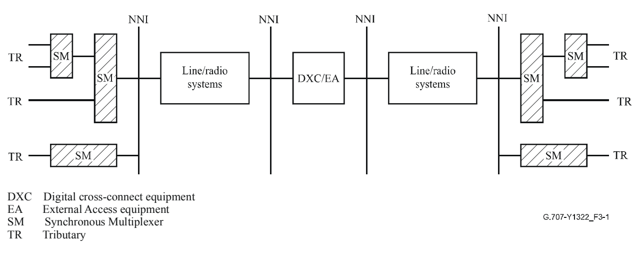

Figure 3-1/G.707/Y.1322 – Location of the NNI

</td><td>

3.7 network node interface (NNI): See ITU-T Rec. G.780/Y.1351.

Figure 3-1 gives a possible network configuration to illustrate the location of NNI specified in this Recommendation.

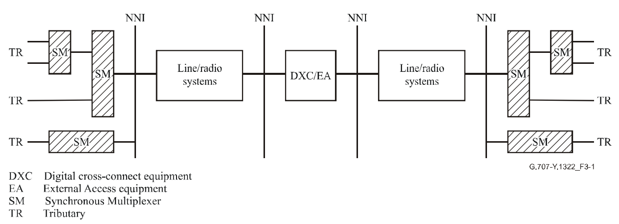

Figure 3-1/G.707/Y.1322 – Location of the NNI

</td></tr>
<tr><td>

3.8 pointer: An indicator whose value defines the frame offset of a virtual container with respect to the frame reference of the transport entity on which it is supported.

</td><td>

3.8 pointer: See ITU-T Rec. G.780/Y.1351.

</td></tr>
</table>

Term	Replacement text
3.9 concatenation: A procedure whereby a multiplicity of virtual containers is associated one with another with the result that their combined capacity can be used as a single container across which bit sequence integrity is maintained.	**3.9 concatenation**: See ITU-T Rec. G.780/Y.1351.
3.10 SDH mapping: A procedure by which tributaries are adapted into virtual containers at the boundary of an SDH network.	**3.10 SDH mapping**: See ITU-T Rec. G.780/Y.1351.
3.11 SDH multiplexing: A procedure by which multiple lower order path layer signals are adapted into a higher order path or the multiple higher order path layer signals are adapted into a multiplex section.	**3.11 SDH multiplexing**: See ITU-T Rec. G.780/Y.1351.
3.12 SDH aligning: A procedure by which the frame offset information is incorporated into the tributary unit or the administrative unit when adapting to the frame reference of the supporting layer.	**3.12 SDH aligning**: See ITU-T Rec. G.780/Y.1351.
3.13 Bit Interleaved Parity-X (BIP-X): BIP-X code is defined as a method of error monitoring. With even parity an X-bit code is generated by the transmitting equipment over a specified portion of the signal in such a manner that the first bit of the code provides even parity over the first bit of all X-bit sequences in the covered portion of the signal, the second bit provides even parity over the second bit of all X-bit sequences within the specified portion, etc. Even parity is generated by setting the BIP-X bits so that there is an even number of 1s in each monitored partition of the signal. A monitored partition comprises all bits which are in the same bit position within the X-bit sequences in the covered portion of the signal. The covered portion includes the BIP-X.	**3.13 Bit Interleaved Parity-X (BIP-X)**: See ITU-T Rec. G.780/Y.1351.
3.14 concatenation: The process of summing the bandwidth of a number of smaller containers into a larger bandwidth container. Two versions exist: – Contiguous concatenation; – Virtual concatenation.	

Term	Replacement text
3.15 shortened binary-BCH: A shortened version of the class of the block linear cyclic codes. These shortened binary BCH codes have the following common properties, i.e.: $n = 2^m - 1 - s$ $k = n - t \times m$ $d = 2 \times t + 1$ where: n the size of the whole code word; k the number of the information bits; m the parameter of the BCH code; t the number of the corrected errors within the block of the BCH code; d the minimum code distance; s the amount of information eliminated as part of the code shorting.	**3.14 shortened binary-BCH**: See Amendment 1/G.780/Y.1351.
3.16 generator polynomial: The polynomial that is used for encoding of any cyclic codes. The remainder after division of the information polynomial by generating polynomial is the redundancy part of the encoded code word.	**3.15 generator polynomial**: See ITU-T Rec. G.780/Y.1351.
3.17 systematic code: The original data bits for binary codes are unchanged by the encoding procedure. Redundant bits or symbols (parity) are added separately to each code block.	**3.16 systematic code**: See ITU-T Rec. G.780/Y.1351.

1.1) Changes to terms identified in ITU-T Rec. G.707/Y.1322, Corrigendum 1

The following table identifies the target term, with appropriate replacement text for the definition.

Term	Replacement text
3.18 tributary unit group (TUG): One or more Tributary Units, occupying fixed, defined positions in a higher order VC-n payload is termed a Tributary Unit Group (TUG). TUGs are defined in such a way that mixed capacity payloads made up of different size Tributary Units can be constructed to increase flexibility of the transport network. A TUG-2 consists of a homogeneous assembly of identical TU-1s or a TU-2. A TUG-3 consists of a homogeneous assembly of TUG-2s or a TU-3.	**3.17 tributary unit group (TUG)**: See ITU-T Rec. G.780/Y.1351.

1.2) Changes to terms identified in ITU-T Rec. G.707/Y.1322, Amendment 1

The following table identifies the target term, with appropriate replacement text for the definition.

Term	Replacement text
3.19 dSTM-12*NMi* interface: An SDH transmission interface which transports one or more TU-12, with SHDSL-based Section overhead. dSTM-12*NMi* interfaces are defined for SHDSL transport technologies. The number (N) of TU-12 in dSTM-12*NMi* interfaces provided by this Recommendation is limited to $N = 1$ to 9 inclusive. The number (M) of SHDSL wire pairs over which the dSTM-12*NMi* signal is transported is limited to $M = 1$ to 4 inclusive. The number (i) represents the presence or absence of an ($M \times i \times 8$) kbit/s DCC in the dSTM-12*NMi* signal; it is limited to $i = 0,..,7$ (single-pair mode), $i = 0,..,4$ (2-pair mode), $i = 0,..,3$ (3-pair mode) and $i = 0,1,2$ (4-pair mode) or 1. Not all combinations of N and M are allowed. Refer to Table G.1.	**3.18 dSTM-12*NMi* interface**: See Amendment 1/Rec. G.780/Y.1351.

2) Clarification of the VCAT description

Correct clause 11 as follows:

11 VC concatenation

For the transport of payloads that do not fit efficiently into the standard set of virtual containers ~~(VC-3/4/2/12/11)~~(VC-11, VC-12, VC-2, VC-3, VC-4) VC concatenation can be used. VC concatenation is defined for:

~~VC-3/4 to provide transport for payloads requiring greater capacity than one container-3/4;~~

~~VC-2 to provide transport for payloads that require capacity greater than one container-2;~~

- ~~VC-11/12 to provide transport for payloads that require capacity greater than one container-11/12.~~VC-4 – to provide transport for payloads that require capacity greater than one Container-4;
- VC-3 – to provide transport for payloads that require capacity greater than one Container-3;
- VC-2 – to provide transport for payloads that require capacity greater than one Container-2;
- VC-12 – to provide transport for payloads that require capacity greater than one Container-12;
- VC-11 – to provide transport for payloads that require capacity greater than one Container-11;

Two methods for concatenation are defined: contiguous and virtual concatenation. Both methods provide concatenated bandwidth of ~~X times container-N~~X*Container-n at the path termination. The difference is the transport between the path terminations. Contiguous concatenation maintains the contiguous bandwidth throughout the whole transport, while virtual concatenation breaks the contiguous bandwidth into individual VCs, transports the individual VCs and recombines these VCs to a contiguous bandwidth at the end point of the transmission. Virtual concatenation requires concatenation functionality only at the path termination equipment, while contiguous concatenation requires concatenation functionality at each network element.

It is possible to perform a conversion between the two types of concatenation. The conversion between virtual and contiguous VC-4 concatenation is defined in ITU-T Rec. G.783. The conversion between virtual and contiguous VC-2 concatenation is for further study.

11.1 Contiguous concatenation of X VC-4s (VC-4-Xc, X = 4, 16, 64, 256)

A VC-4-Xc provides a payload area of ~~X container-4~~X*Container-4 and is represented by a C-4-X structure as shown in Figure 11-1. One common set of POH, located in the first column, is used for the whole VC-4-Xc (e.g., the BIP-8 covers all ~~261 × X~~261*X columns of the VC-4-Xc). Columns 2 to X are fixed stuff.

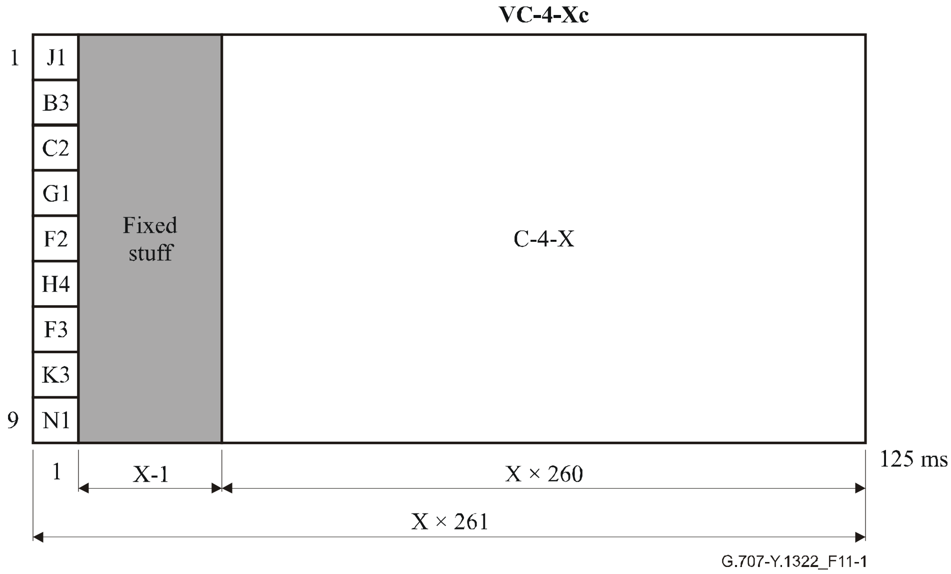

Figure 11-1/G.707/Y.1322 – VC-4-Xc structure

The VC-4-Xc is transported in X contiguous AU-4 in the STM-N signal. The first column of the VC-4-Xc is always located in the first AU-4. The pointer of this first AU-4 indicates the position of the J1 byte of the VC-4-Xc. The pointers of the AU-4 #2 to X are set to the concatenation indication (see Figure 8-3) to indicate the contiguously concatenated payload. Pointer justification is performed in common for the X concatenated AU-4s and ~~X × 3~~X*3 stuffing bytes are used.

A VC-4-Xc provides a payload capacity of ~~599 040~~599'040 kbit/s for X = 4, 2'396'160 kbit/s for X = 16, 9'584'640 kbit/s for X = 64 and 38'338'560 kbit/s for X = 256.

NOTE – High rate VC-4-Xc could be used without any constraints in point-to-point connections. SDH networks may be limited to a certain bit rate of VC-4-Xc (e.g., X ≤ 64), e.g., due to rings with MSSPRING that has to reserve 50% of the STM-N bandwidth for protection.

11.2 Virtual concatenation of X ~~VC-3/4s (VC-3/4-Xv,~~VC-3/VC-4s (VC-3-Xv/VC-4-Xv, X = 1 ... 256)

A ~~VC-3/4-Xv provides a continuous payload area of X container-3/4 (VC-3/4-Xc) with~~VC-3-Xv/VC-4-Xv provides the transport capability equivalent to X*Container-3/Container-4, which can be represented by a C-3-X/C-4-X like structure, and has a payload capacity of ~~X × 48384/149760~~X*48'384/149'760 kbit/s as ~~shown~~ depicted in Figures 11-2 and 11-3. The payload is mapped into X individual VC-3/VC-4s which form the VC-3-~~container is mapped in X individual VC-3/4s which form the VC-3/4-Xv. Each VC-3/4~~Xv/VC-4-Xv, as illustrated in Appendix XIX. Each VC-3/VC-4 has its own POH as specified in subclause 9.3.1. The H4 POH byte is used for the virtual concatenation-specific sequence and multiframe indication as defined below.

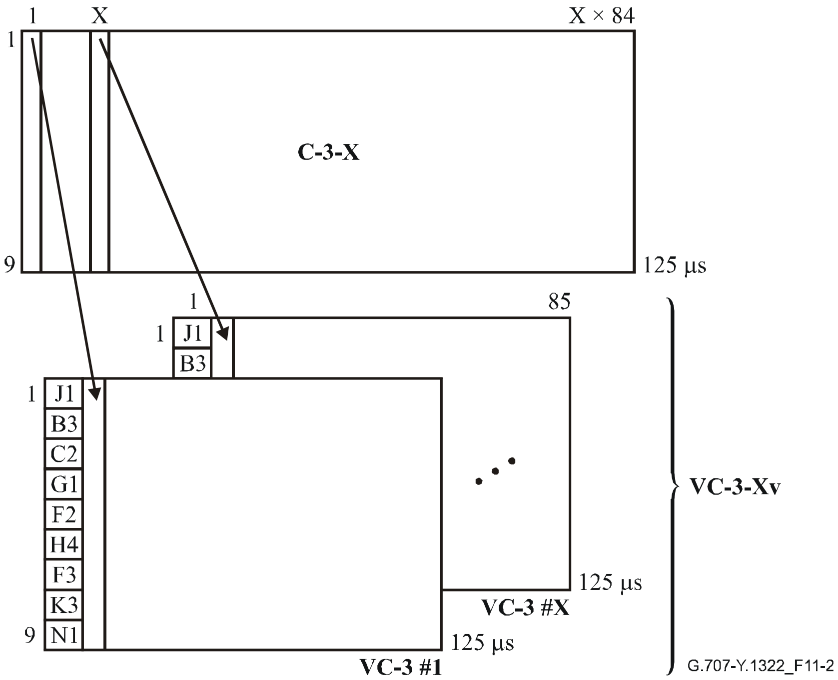

Figure 11-2/G.707/Y.1322 – VC-3-Xv structure

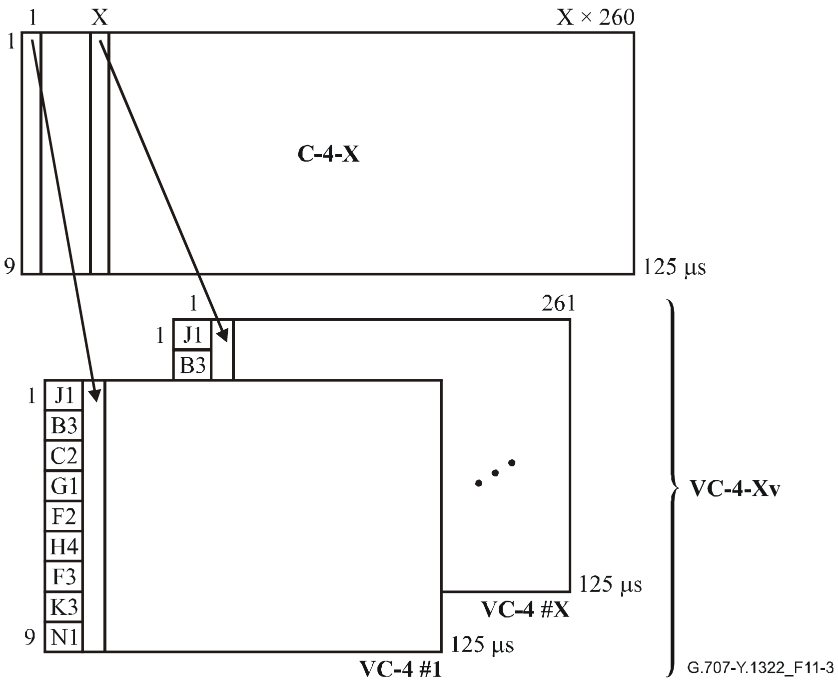

Figure 11-3/G.707/Y.1322 – VC-4-Xv structure

Each ~~VC-3/4 of the VC-3/4-Xv~~VC-3/VC-4 of the VC-3-Xv/VC-4-Xv is transported individually through the network. Due to the different propagation ~~delay of the VC-3/4s,~~delays of the VC-3s/VC-4s, a differential delay will occur between the individual ~~VC-3/4s. This~~VC-3s/VC-4s. At the path termination this differential delay has to be compensated and the individual ~~VC-3/4s~~VC-3s/VC-4s have to be realigned for access to the contiguous payload area. The realignment process has to cover at least a differential delay of 125 µs.

A two-stage 512 ms multiframe is introduced to cover differential delays of 125 µs and above (up to 256 ms). The first stage uses H4, bits 5-8 for the 4-bit multiframe indicator (MFI1). MFI1 is incremented every basic frame and counts from 0 to 15. For the 8-bit multiframe indicator of the second stage (MFI2), H4, bits 1-4 in frame 0 (MFI2 bits 1-4) and 1 (MFI2 bits 5-8) of the first multiframe are used (see Table 11-1). MFI2 is incremented once every multiframe of the first stage and counts from 0 to 255. The resulting overall multiframe is 4096 frames (= 512 ms) long.

Table 11-1/G.707/Y.1322 – VC-3-Xu/VC-4-Xv sequence and multiframe indicator H4 coding

H4 byte								1st multi-frame number	2nd multi-frame number
Bit 1	**Bit 2**	**Bit 3**	**Bit 4**	**Bit 5**	**Bit 6**	**Bit 7**	**Bit 8**		
				1st multiframe indicator MFI1 (bits 1-4)					
Sequence indicator MSB (bits 1-4)				1	1	1	0	14	n–1
Sequence indicator LSB (bits 5-8)				1	1	1	1	15	
2nd multiframe indicator MFI2 MSB (bits 1-4)				0	0	0	0	0	n
2nd multiframe indicator MFI2 LSB (bits 5-8)				0	0	0	1	1	
Reserved ("0000")				0	0	1	0	2	
Reserved ("0000")				0	0	1	1	3	
Reserved ("0000")				0	1	0	0	4	
Reserved ("0000")				0	1	0	1	5	
Reserved ("0000")				0	1	1	0	6	
Reserved ("0000")				0	1	1	1	7	
Reserved ("0000")				1	0	0	0	8	
Reserved ("0000")				1	0	0	1	9	
Reserved ("0000")				1	0	1	0	10	
Reserved ("0000")				1	0	1	1	11	
Reserved ("0000")				1	1	0	0	12	
Reserved ("0000")				1	1	0	1	13	
Sequence indicator SQ MSB (bits 1-4)				1	1	1	0	14	
Sequence indicator SQ LSB (bits 5-8)				1	1	1	1	15	
2nd multiframe indicator MFI2 MSB (bits 1-4)				0	0	0	0	0	n+1
2nd multiframe indicator MFI2 LSB (bits 5-8)				0	0	0	1	1	
Reserved ("0000")				0	0	1	0	2	

The sequence indicator ~~SQ~~(SQ) identifies the sequence/order in which the individual ~~VC-3/4s of the VC-3/4-Xv~~VC-3s/VC-4s of the VC-3-Xv/VC-4-Xv are combined to form the contiguous ~~container VC-3/4-Xc~~payload C-3-X/C-4-X like structure as shown in Figure 11-4. Each ~~VC-3/4 of a VC-3/4-Xv~~VC-3/VC-4 of a VC-3-Xv/VC-4-Xv has a fixed unique sequence number in the range of 0 to (X–1). ~~The VC-3/4 transporting the first time slot~~

The VC-4 transporting the:

- data from cols 1, X+1, 2X+1, .. 259X+1 of the C-4-X like structure has the sequence number 0;
- data from cols 2, X+2, 2X+2, .. 259X+2 of the C-4-X like structure has the sequence number 1;

and so on up to the VC-4 transporting the:

- data from cols X, X+X, 2X+X, ..259X+X of the C-4-X like structure has the sequence number (X–1).

The VC-3 transporting the:

- data from cols 1, X+1, 2X+1, … 83X+1 of the C-3-X like structure has the sequence number 0;
- data from cols 2, X+2, 2X+2, … 83X+2 of the C-3-X like structure has the sequence number 1;

and so on up to the VC-3 transporting the:

- of the C-3/4 of the C-3/4-Xc has the sequence number 0, the VC-3/4 transporting the second C-3/4 of the C-3/4-Xc has the sequence number 1 and so on up to the VC-3/4 transporting time C-3/4 X of the C-3/4-Xc withdata from cols X, X+X, 2X+X, … 83X+X of the C-3-X like structure has the sequence number (X–1).

For applications requiring fixed bandwidth, the sequence number is fixed assigned and not configurable. This allows the constitution of the VC-3/4-XvVC-3-Xv/VC-4-Xv to be checked without using the trace. The 8-bit sequence number (which supports values of X up to 256) is transported in bits 1 to 4 of the H4 bytes, using frame 14 (SQ bits 1-4) and 15 (SQ bits 5-8) of the first multiframe stage as shown in Table 11-1.

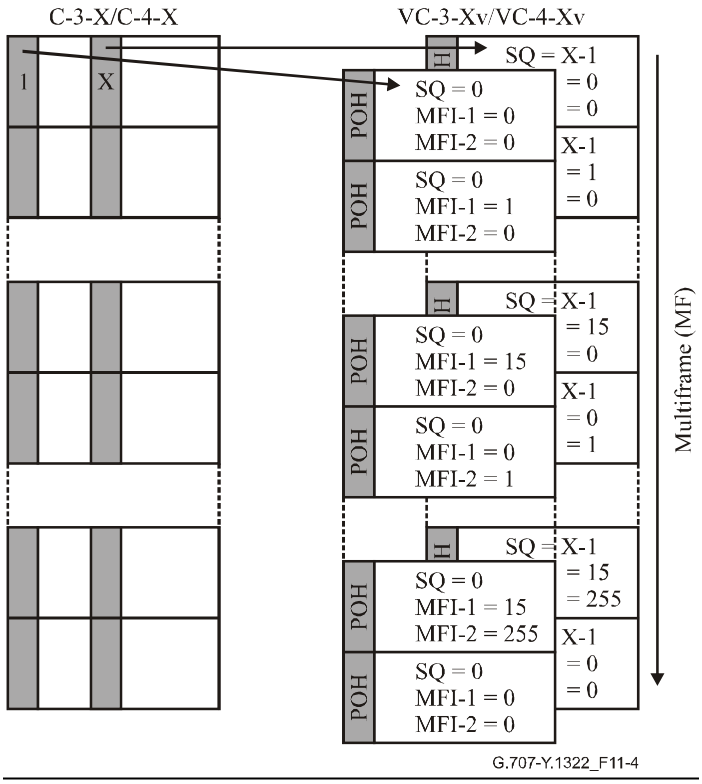

Figure 11-4/G.707/Y.1322 – ~~VC-3/4-Xv~~VC-3-Xv/VC-4-Xv multiframe and sequence indicator

11.2.1 Higher order LCAS for VC-n-Xv (n = 3, 4)

Table 11-2 depicts the modified VC-3, VC-4 H4 HO virtual concatenation 1st multiframe, as defined in 11.2, indicating the control codes used for the support of HO LCAS. See also ITU-T Rec. G.7042/Y.1305.

– Frame indicator: A combination of the 1st multiframe and the 2nd multiframe counter [0-4095].

– Sequence indicator: Number to identify each member in the VCG [0-255].

– CTRL: LCAS Control field, see Table 1/G.7042/Y.1305.

– GID: Group Identification bit.

– Member status: The status report of the individual members uses the MST-multiframe as shown in Table 11-3. The status of all members (256) is transferred in 64 ms.

– RS-Ack: Re-Sequence Acknowledge bit.

– CRC: Eight-bit CRC check for fast acceptance of Virtual Concatenation OH. With this CRC-8 the probability of an undetected error is better than 1.52×10^{-16}. The CRC generator polynomial is $x^8 + x^2 + x + 1$.

Table 11-2/G.707/Y.1322 – VC-n-Xv sequence and multiframe indicator H4 coding

Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8	1st multi-frame number	2nd multi-frame number
~~H4 byte~~								~~1st multi-frame no.~~	~~2nd multi-frame no.~~
H4 byte									
				~~1st multifr. indicator MFI1 (bits 1-4)~~					
				1st multiframe indicator MFI1 (bits 1-4)					
Sequence indicator MSBs (bits 1-4)				1	1	1	0	14	n-1
Sequence indicator LSBs (bits 5-8)				1	1	1	1	15	
~~2nd multifr. indicator MFI2 MSBs (bits 1-4)~~				~~0~~	~~0~~	~~0~~	~~0~~	~~0~~	~~n~~
2nd multiframe indicator MFI2 MSBs (bits 1-4)				0	0	0	0	0	n
~~2nd multifr. indicator MFI2 LSBs (bits 5-8)~~				~~0~~	~~0~~	~~0~~	~~1~~	~~1~~	
2nd multiframe indicator MFI2 LSBs (bits 5-8)				0	0	0	1	1	
CTRL				0	0	1	0	2	
GID ("000x")				0	0	1	1	3	
Reserved ("0000")				0	1	0	0	4	
Reserved ("0000")				0	1	0	1	5	
CRC-8				0	1	1	0	6	
CRC-8				0	1	1	1	7	
Member status MST				1	0	0	0	8	
Member status MST				1	0	0	1	9	
0	0	0	RS_Ack	1	0	1	0	10	
Reserved ("0000")				1	0	1	1	11	
Reserved ("0000")				1	1	0	0	12	
Reserved ("0000")				1	1	0	1	13	
Sequence indicator SQ MSBs (bits 1-4)				1	1	1	0	14	
Sequence indicator SQ LSBs (bits 5-8)				1	1	1	1	15	
~~2nd multifr. indicator MFI2 MSBs (bits 1-4)~~				~~0~~	~~0~~	~~0~~	~~0~~	~~0~~	~~n+1~~
2nd multiframe indicator MFI2 MSBs (bits 1-4)				0	0	0	0	0	n+1
~~2nd multifr. indicator MFI2 LSBs (bits 5-8)~~				~~0~~	~~0~~	~~0~~	~~1~~	~~1~~	
2nd multiframe indicator MFI2 LSBs (bits 5-8)				0	0	0	1	1	
CTRL				0	0	1	0	2	
0	0	0	GID	0	0	1	1	3	
Reserved ("0000")				0	1	0	0	4	
Reserved ("0000")				0	1	0	1	5	
C_1	C_2	C_3	C_4	0	1	1	0	6	
C_5	C_6	C_7	C_8	0	1	1	1	7	
Member status MST				1	0	0	0	8	

Table 11-3/G.707/Y.1322 – H4 VC-n-Xv member status

2nd multiframe frame number	Member number				
0, 32, 64, 96, 128, 160, 192, 224	0	1	2	3	MST-multiframe
	4	5	6	7	
1, 33, 65, 97, 129, 161, 193, 225	8	9	10	11	
	12	13	14	15	
. . .	. . .	. . .	. . .	. . .	
30, 62, 94, 126, 158, 190, 222, 254	240	241	242	243	
	244	245	246	247	
31, 63, 95, 127, 159, 191, 223, 255	248	249	250	251	
	252	253	254	255	

NOTE 1 – There are 8 member statuses reported per VC-n-Xv frame. The 256 members require 32 frames at a frame rate of 2 ms each. This therefore results in the member status being refreshed every 64 ms if there is only one return channel.

NOTE 2 – The interpretation of the member status bits according to this table is based on the 2nd multiframe value at the moment the member status word is received. In the case of VC-3/4 this means that first the 2nd multiframe value is read from H4[1-4][0] and H4[1-4][1] – a value between 0 and 255 – and consequently this value is used (modulo 32) as an index for this table to identify the members of which the status is received in the H4[1-4][8] and H4[1-4][9] nibbles immediately after. This is still within the same 1st multiframe, but just in the next control packet.

11.2.1.1 High order control packet

The high order control packet consists of:

- MST (Member status) field (two nibbles 1st multiframe #8 and #9);
- RS-Ack (Re-Sequence Acknowledge) bit (bit 4 of nibble 1st multiframe #10);
- SQ (Sequence Indicator) field (two nibbles 1st multiframe #14 and #15);
- MFI2 (2nd Multiframe Indicator) (two nibbles 1st multiframe #0 and #1);
- CTRL (Control) field (one nibble 1st multiframe #2);
- GID (Group Identification) bit (bit 4 of nibble 1st multiframe #3);
- The CRC-8 field is sent with one nibble in each of frame #6 and frame #7. (Note that in this paragraph, unless otherwise indicated, the frame numbers are those indicated by the 1st multiframe number field.) The CRC-8 field, $C_1C_2C_3C_4C_5C_6C_7C_8$ is the remainder of the CRC-8 calculation over the control packet. In the example of Table 11-2, the control packet bits are contained in H4[1-4] of the frames 8…15 of multiframe n and H4[1-4] of the frames 0…7 of multiframe $n + 1$, (where multiframes n and $n + 1$ are indicated by the 2nd multiframe indicator bits). The CRC-8 remainder is calculated as follows: The first 14 nibbles of the control packet bits represent a polynomial $M(x)$ of degree 55, where H4[1] of frame 8, 2nd multiframe n is the most significant bit and H4[4] of frame 5, 2nd multiframe $n + 1$ is the least significant bit. $M(x)$ is first multiplied by x^8 and then divided (modulo 2) by generator polynomial $G(x) = x^8 + x^2 + x + 1$ to produce a remainder $R(x)$ of degree 7 or less. $R(x)$ is the CRC-8 code with x^7 of $R(x)$ corresponding to C_1 as the most significant bit of the remainder and x^0 of $R(x)$ corresponding to C_8 as the least significant bit of the remainder;

- All other 1st multiframe nibbles (#11, #12, #13, #4 and #5) are reserved and should be set to "0000".

The high order control packet starts at 1st multiframe #8 and end at 1st multiframe #7 in the next multiframe as shown between the heavy lines in Table 11-2.

11.3 Contiguous concatenation of X VC-2s in a higher order VC-3 (VC-2-Xc, X = 1 … 7)

A VC-2-Xc provides a payload area of ~~X container-2~~X*Container-2 and is represented by a C-2-X structure as shown in Figure 11-5. One common set of POH, corresponding to the POH of the first VC-2, is used for the whole VC-2-Xc (e.g.~~,~~ the BIP-2 covers all ~~428 × X~~428*X bytes of the VC-2-Xc). The POH positions corresponding to VC-2 #2 to VC-2 #X are fixed stuff.

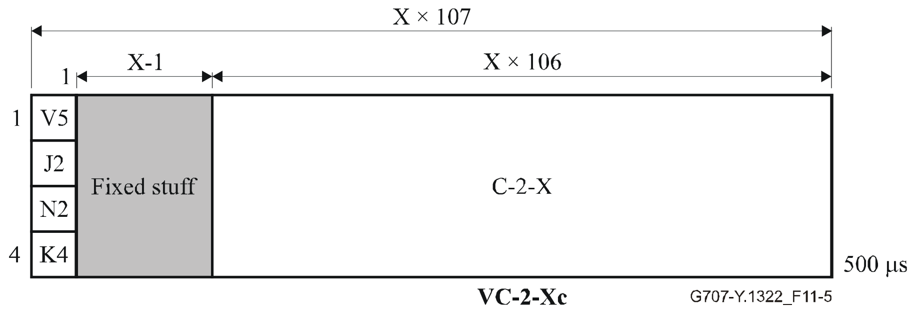

Figure 11-5/G.707/Y.1322 – VC-2-Xc structure

The VC-2-Xc is located in X contiguous TU-2 in a higher order VC-3. The first column of the VC-2-Xc is always located in the first TU-2. The pointer of this first TU-2 indicates the position of the V5 POH byte of the VC-2-Xc. The pointers of the TU-2 #2 to #X are set to the concatenation indication (see Figure 8-10) to indicate the contiguous concatenated payload. Pointer justification is performed in common for the X concatenated TU-2s and X stuffing bytes are used.

With allowed values of X between 1 and 7, the VC-2-Xc provides a payload capacity between 6784 kbit/s and 47 488 kbit/s in steps of 6784 kbit/s.

11.4 Virtual concatenation of X ~~VC-11/12/2s~~VC-11/VC-12/VC-2

A ~~VC-11/12/2-Xv provides a payload area of X container-11/12/2 as shown~~VC-11-Xv/VC-12-Xv/VC-2-Xv provides the transport capability equivalent to X*Container-11/Container-12/Container-2, which can be represented by a C-11-X/C-12-X/C-2-X like structure and has a payload capacity of X*1600/2176/6784 kbit/s, as depicted in Figures 11-6, 11-7 and 11-8. The container is mapped in X individual ~~VC-11/12/2s~~VC-11/VC-12/VC-2s which form the ~~VC-11/12/2-Xv. Each VC-11/12/2~~VC-11-Xv/VC-12-Xv/VC-2-Xv, as illustrated in Appendix XIX. Each VC-11/VC-12/VC-2 has its own POH.

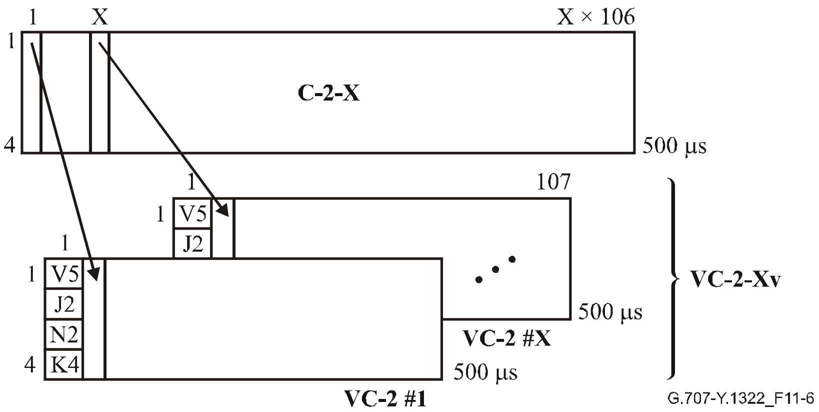

Figure 11-6/G.707/Y.1322 – VC-2-Xv structure

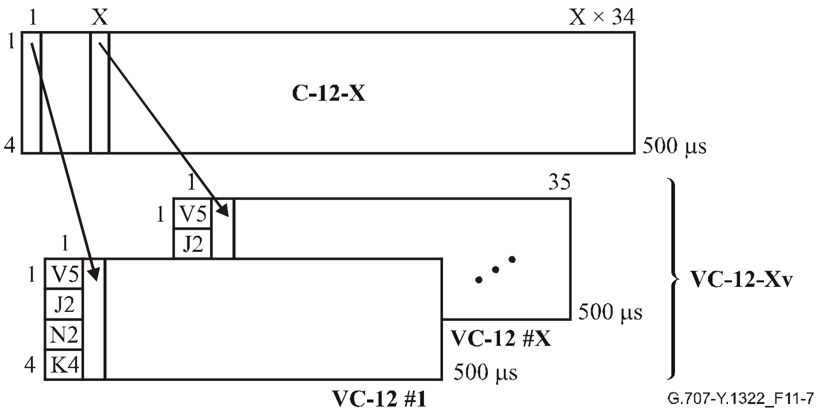

Figure 11-7/G.707/Y.1322 – VC-12-Xv structure

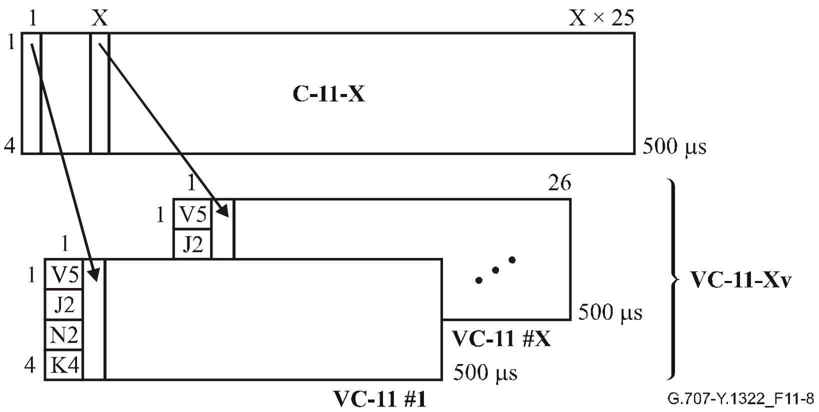

Figure 11-8/G.707/Y.1322 – VC-11-Xv structure

Each ~~VC-11/12/2 of the VC-11/12/2-Xv~~VC-11/VC-12/VC-2 of the VC-11-Xv/VC-12-Xv/VC-2-Xv is transported individually through the network. Due to ~~this,~~the different propagation delays of the VC-11/VC-12/VC-2s, a differential delay will occur between the individual ~~VC-11/12/2s and, therefore, the order and the alignment of the VC-11/12/2s will change. At the termination, the individual VC-11/12/2s have to be rearranged and realigned~~VC-11/VC-12/VC-2s. At the path termination, this differential delay has to be ~~in order to re-establish the contiguous concatenated container.~~compensated and the individual VC-11/VC-12/VC-2s have to be realigned for access to the contiguous payload area. The realignment process has to cover at least a differential delay of 125 µs.

Payload capacities are shown in Table 11-4 for ~~VC-11-Xv, VC-12-Xv and VC-2-Xv.~~VC-11-Xv, VC-12-Xv and VC-2-Xv.

~~Table 11-4/G.707/Y.1322 – Capacity of virtually concatenated VC-11/12/2-Xv~~

Table 11-4/G.707/Y.1322 – Capacity of virtually concatenated VC-11-Xv/VC-12-Xv/VC-2-Xv

	X	Capacity	In steps of
VC-11-Xv	1 to 64 (Note)	1600 kbit/s to 102 400 kbit/s	1600 kbit/s
VC-12-Xv	1 to 64	2176 kbit/s to 139 264 kbit/s	2176 kbit/s
VC-2-Xv	1 to 64	6784 kbit/s to 434 176 kbit/s	6784 kbit/s
NOTE – Limited to 64 due to: a) six bits for Sequence indicator in K4 bit 2 frame; and b) inefficient and unlikely to map more than 64 VC-11s in VC-4.			

To perform the realignment of the individual VC-ms (m = 11/12/2) that belong to a virtually concatenated group it is necessary to:

- compensate for the differential delay experienced by the individual VC-ms;
- know the individual sequence numbers of the individual VC-ms.

Bit 2 of the K4 byte of the low order VC-m POH is used to convey this information from the sending end to the receiving end of the virtually concatenated signal where the realignment process is performed. A serial string of 32 bits (over 32 four-frame multiframes) is arranged as in Figure 11-9. This string is repeated every 16 ms (32 bits × 500 µs/bit) or every 128 frames.

Bit number

1–5	6–11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
Frame count	Sequence indicator	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

R Reserved bit

Figure 11-9/G.707/Y.1322 – K4 bit 2 multiframe

The LO virtual concatenation information in K4 bit 2 has a 32-bit multiframe depicted in Figure 11-9. The phase of the LO virtual concatenation information in K4 bit 2 should be the same as for the K4 bit 1 extended signal label described in 9.3.2.4.

NOTE – Virtually concatenated ~~VC-11/12/2~~VC-11/VC-12/VC-2 must use the extended signal label. Otherwise the frame phase of the K4 bit 2 multiframe can not be established.

The frame consists of the following fields:

The LO virtual concatenation frame count is contained in bits 1 to 5. The LO virtual concatenation sequence indicator is contained in bits 6 to 11. The remaining 21 bits are reserved for future standardization, should be set to all "0"s and should be ignored by the receiver.

The LO virtual concatenation frame count provides a measure of the differential delay up to 512 ms in 32 steps of 16 ms that is the length of the multiframe (32 × 16 ms = 512 ms).

The LO virtual concatenation sequence indicator identifies the sequence/order in which the individual ~~VC-11/12/2s of the VC-11/12/2-Xv~~VC-11/VC-12/VC-2s of the VC-11-Xv/VC-12-Xv/VC-2-Xv are combined to form the contiguous ~~container VC-11/12/2-Xc~~payload C-11-X/C-12-X/C-2-X as shown in Figures 11-6 to 11-8. Each VC-11/VC-12/VC-2 of a VC-11-Xv/VC-12-Xv/VC-2-~~VC-11/12/2 of a VC-11/12/2-~~Xv has a fixed unique sequence number in the range of 0 to (X–1).

The ~~VC-1/2 transporting the first C-11/12/2 of the C-11/12/2-Xc has the sequence number 0, the VC-11/12/2 transporting the second C-11/12/2 of the C-11/12/2-Xc has the sequence number 1 and so on up to the VC-11/12/2 transporting C-11/12/2 X of the C-11/12/2-Xc with the sequence number (X–1).~~ VC-11 transporting the:

- data from cols 1, X+1, 2X+1, ….25X+1 of the C-11-X like structure has the sequence number 0;
- data from cols 2, X+2, 2X+2, … 25X+2 of the C-11-X like structure has the sequence number 1;

and so on up to the VC-11 transporting the:

- data from cols X, X+X, 2X+X, … 25X+X of the C-11-X like structure has the sequence number (X–1).

The VC-12 transporting the:

- data from cols 1, X+1, 2X+1, … 34X+1 of the C-12-X like structure has the sequence number 0;
- data from cols 2, X+2, 2X+2, … 34X+2 of the C-12-X like structure has the sequence number 1;

and so on up to the VC-12 transporting the:

- data from cols X, X+X, 2X+X, … 34X+X of the C-12-X like structure has the sequence number (X–1).

The VC-2 transporting the:

- data from cols 1, X+1, 2X+1, … 106X+1 of the C-2-X like structure has the sequence number 0;
- data from cols 2, X+2, 2X+2, … 106X+2 of the C-2-X like structure has the sequence number 1;

and so on up to the VC-2 transporting the:

- data from cols X, X+X, 2X+X, … 106X+X of the C-2-X like structure has the sequence number (X–1).

For applications requiring fixed bandwidth~~,~~ the sequence number is fixed assigned and not configurable. This allows the constitution of the ~~VC-11/12/2-Xv~~VC-11-Xv/VC-12-Xv/VC-2-Xv to be checked without using the trace.

11.4.1 Lower order LCAS, VC-m-Xv (m = 11, 12, 2)

Figure 11-10 depicts the modified K4[2] LO virtual concatenation multiframe, as defined in 11.4, indicating the control codes used for the support of LO LCAS. See also ITU-T Rec. G.7042/Y.1305.

- Frame count: The multiframe counter [0-31].
- Sequence indicator: Number to identify each member in the VCG [0-63].
- CTRL: LCAS Control field, see Table 1/G.7042/Y.1305.
- GID: Group Identification bit.
- Member status: The status report of the individual members uses the MST-multiframe as shown in Table 11-5. The status of all members (64) is transferred in 128 ms.
- RS-Ack: Re-Sequence Acknowledge bit.
- CRC: Three-bit CRC check for fast acceptance of Virtual Concatenation overhead. With this CRC-3 the probability of an undetected error in a signal with an average BER of 5.32×10^{-9}, is 4×10^{-30}. The CRC generator polynomial is $x^3 + x + 1$.

<table>
<tr><td>1</td><td>2</td><td>3</td><td>4</td><td>5</td><td>6</td><td>7</td><td>8</td><td>9</td><td>10</td><td>11</td><td>12</td><td>13</td><td>14</td><td>15</td><td>16</td><td>17</td><td>18</td><td>19</td><td>20</td><td>21</td><td>22</td><td>23</td><td>24</td><td>25</td><td>26</td><td>27</td><td>28</td><td>29</td><td>30</td><td>31</td><td>32</td></tr>
<tr><td colspan="5" rowspan="2">Frame indicator</td><td colspan="6" rowspan="2">Sequence indicator</td><td colspan="4" rowspan="2">CTRL</td><td rowspan="2">GID</td><td colspan="4" rowspan="2">Reserved "0000"</td><td rowspan="2">RS-Ack</td><td colspan="8" rowspan="2">Member status</td><td>C1</td><td>C1</td><td>C3</td></tr>
<tr><td colspan="3">CRC-3</td></tr>
</table>

Figure 11-10/G.707/Y.1322 – K4[2] VC-m-Xv supporting LCAS coding

Table 11-5/G.707/Y.1322 – LO LCAS VC-m-Xv frame-to-member number relation

<table>
<tr><th>Frame number</th><th colspan="8">Member number</th><th></th></tr>
<tr><td>0, 8, 16, 24</td><td>0</td><td>1</td><td>2</td><td>3</td><td>4</td><td>5</td><td>6</td><td>7</td><td rowspan="8">MST-multiframe</td></tr>
<tr><td>1, 9, 17, 25</td><td>8</td><td>9</td><td>10</td><td>11</td><td>12</td><td>13</td><td>14</td><td>15</td></tr>
<tr><td>2, 10, 18, 26</td><td>16</td><td>17</td><td>18</td><td>19</td><td>20</td><td>21</td><td>22</td><td>23</td></tr>
<tr><td>3, 11, 19, 27</td><td>24</td><td>25</td><td>26</td><td>27</td><td>28</td><td>29</td><td>30</td><td>31</td></tr>
<tr><td>4, 12, 20, 28</td><td>32</td><td>33</td><td>34</td><td>35</td><td>36</td><td>37</td><td>38</td><td>39</td></tr>
<tr><td>5, 13, 21, 29</td><td>40</td><td>41</td><td>42</td><td>43</td><td>44</td><td>45</td><td>46</td><td>47</td></tr>
<tr><td>6, 14, 22, 30</td><td>48</td><td>49</td><td>50</td><td>51</td><td>52</td><td>53</td><td>54</td><td>55</td></tr>
<tr><td>7, 15, 23, 31</td><td>56</td><td>57</td><td>58</td><td>59</td><td>60</td><td>61</td><td>62</td><td>63</td></tr>
<tr><td colspan="10">NOTE – There are eight member statuses reported per VC-m-Xv frame. The 64 members require eight frames at a frame rate of 16 ms each. This thus results in the member status being refreshed every 128 ms if there is only one return channel.</td></tr>
</table>

11.4.1.1 Low order control packet

The low order control packet consists of:

- MultiFrame Indicator (MFI) (five bits: 1 to 5);
- Sequence Indicator (SQ) field (six bits: 6 to 11);
- CTRL (Control) field (four bits: 12 to 15);

- GID (Group Identification) bit (one bit: 16);
- RS-Ack (Re-Sequence Acknowledge) bit (one bit: 21);
- Member status (MST) field (eight bits: 22 to 29);
- CRC-3 field (three bits: 30 to 32), $C_1C_2C_3$, is the remainder of the CRC-3 calculation over the K4[2] bits 1…32. To calculate the CRC, we regard control packet bits 1-29 as a polynomial *M(x)* where K4[2] of frame 1 is the most significant bit and K4[2] of frame 29 is the least significant bit of *M(x)*. *M(x)* is first multiplied by x^3 and then divided (modulo 2) by generator polynomial $G(x) = x^3 + x + 1$ to produce a remainder *R(x)* of degree 2 or less. *R(x)* is the CRC-3 code with x^2 of *R(x)* corresponding to C_1 as the most significant bit of the remainder and x^0 of *R(x)* corresponding to C_3 as the least significant bit of the remainder;
- All other bits (#17, #18, #19 and #20) are reserved and should be set to '0'.

The control packet for lower order LCAS starts and stops at the same frames as the original multiframe (see Figure 11-10).

3) New Appendix XIX

The following new appendix has been added to clarify the VCAT mapping order:

Appendix XIX

Mapping serial data into a VCG

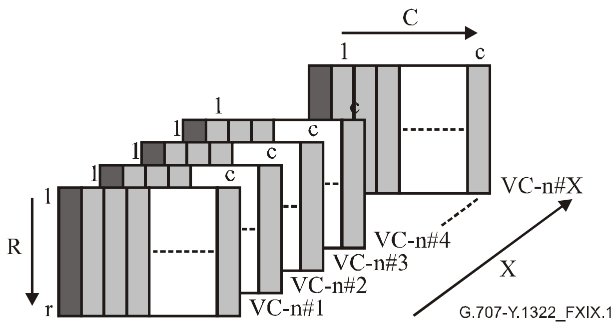

Figure XIX.1/G.707/Y.1322 – VCAT mapping order

Serial data is mapped into a VCG on an octet-by-octet basis in the following order:

1) X_{th} VC;

2) C_{th} column;

3) R_{th} row;

i.e., octet #1 maps into VC #1, column #1, row #1

octet #2 maps into VC #2, column #1, row #1

octet #3 maps into VC #3, column #1, row #1

.

.

octet #X maps into VC #X, column #1, row #1

octet #(X+1) maps into VC #1, column #2, row #1

octet #(X+2) maps into VC #2, column #2, row #1 octet #(X+3) maps into VC #3, column #2, row #1

.

.

octet #(X+X) maps into VC #X, column #2 of row #1

etc. until X*C*R octets are mapped, then the sequence is repeated.

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