INTERNATIONAL TELECOMMUNICATION UNION

ITU-T G.707/Y.1322

TELECOMMUNICATION
STANDARDIZATION SECTOR
OF ITU

Corrigendum 3
(03/2003)

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Corrigendum 3: Virtual concatenation, CRC bits allocation enhancement and sequence numbering

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ITU-T Recommendation G.707/Y.1322

Network node interface for the synchronous digital hierarchy (SDH)

Corrigendum 3

Virtual concatenation, CRC bits allocation enhancement and sequence numbering

Summary

This corrigendum for ITU-T Rec. G.707/Y.1322 clarifies some items relating to Virtual Concatenation and LCAS in order to avoid ambiguity concerning the CRC bit allocation and the definition for the LCAS control packet.

Source

Corrigendum 3 to ITU-T Recommendation G.707/Y.1322 (2000) was prepared by ITU-T Study Group 15 (2001-2004) and approved under the WTSA Resolution 1 procedure on 16 March 2003.

FOREWORD

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The World Telecommunication Standardization Assembly (WTSA), which meets every four years, establishes the topics for study by the ITU-T study groups which, in turn, produce Recommendations on these topics.

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In some areas of information technology which fall within ITU-T's purview, the necessary standards are prepared on a collaborative basis with ISO and IEC.

NOTE

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Network node interface for the synchronous digital hierarchy (SDH)

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Virtual concatenation, CRC bits allocation enhancement and sequence numbering

1) Introduction: LCAS CRC bit location clarification

In order to avoid any ambiguity concerning the CRC bit location and definition for the LCAS control packet, the following new text and corrected figures are adopted for ITU-T Rec. G.707/Y.1322. There is no technical change associated with this text or these figures.

2) Clause 11.2, Virtual concatenation of X VC-3/4s (VC-3/4-Xv, X = 1 ... 256)

In the first sentence of the first paragraph, replace "contiguous" *with* "continuous".

Change the fourth paragraph as follows:

The sequence indicator SQ identifies the sequence/order in which the individual VC-3/4s of the VC-3/4-Xv are combined to form the contiguous container ~~V~~C-3/4-Xc as shown in Figure 11-4. Each VC-3/4 of a VC-3/4-Xv has a fixed unique sequence number in the range of 0 to (X-1). The VC-3/4 transporting the first time slot of the ~~VC-3/4-Xc~~C-3/4 of the C-3/4-Xc has the sequence number 0, the VC-3/4 transporting the second C-3/4 of the C-3/4-Xc has the ~~time slot the~~ sequence number 1 and so on up to the VC-3/4 transporting ~~time slot X of the VC-3/4-Xc~~C-3/4 X of the C-3/4-Xc with the sequence number (X-1). For applications requiring fixed bandwidth the sequence number is fixed assigned and not configurable. This allows the constitution of the VC-3/4-Xv to be checked without using the trace. The 8-bit sequence number (which supports values of X up to 256) is transported in bits 1 to 4 of the H4 bytes, using frame 14 (SQ bits 1-4) and 15 (SQ bits 5-8) of the first multiframe stage as shown in Table 11-1.

3) Subclause 11.2.1, Higher order LCAS for VC-n-Xv (n = 3, 4) (see Amendment 1)

Replace Table 11-1a/G.707/Y.1322 in Amendment 1 with the following table:

Table 11-1a/G.707/Y.1322 – VC-n-Xv sequence and multiframe indicator H4 coding

H4 byte								1st multi-frame no.	2nd multi-frame no.
Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8		
				1st multifr. indicator MFI1 (bits 1-4)					
Sequence indicator MSBs (bits 1-4)				1	1	1	0	14	n-1
Sequence indicator LSBs (bits 5-8)				1	1	1	1	15	
2nd multifr. indicator MFI2 MSBs (bits 1-4)				0	0	0	0	0	n
2nd multifr. indicator MFI2 LSBs (bits 5-8)				0	0	0	1	1	
CTRL				0	0	1	0	2	
GID ("000x")				0	0	1	1	3	
Reserved ("0000")				0	1	0	0	4	
Reserved ("0000")				0	1	0	1	5	
CRC-8				0	1	1	0	6	
CRC-8				0	1	1	1	7	
Member status MST				1	0	0	0	8	
Member status MST				1	0	0	1	9	
0	0	0	RS-Ack	1	0	1	0	10	
Reserved ("0000")				1	0	1	1	11	
Reserved ("0000")				1	1	0	0	12	
Reserved ("0000")				1	1	0	1	13	
Sequence indicator SQ MSBs (bits 1-4)				1	1	1	0	14	
Sequence indicator SQ LSBs (bits 5-8)				1	1	1	1	15	
2nd multifr. indicator MFI2 MSBs (bits 1-4)				0	0	0	0	0	n+1
2nd multifr. indicator MFI2 LSBs (bits 5-8)				0	0	0	1	1	
CTRL				0	0	1	0	2	
0	0	0	GID	0	0	1	1	3	
Reserved ("0000")				0	1	0	0	4	
Reserved ("0000")				0	1	0	1	5	
C_1	C_2	C_3	C_4	0	1	1	0	6	
C_5	C_6	C_7	C_8	0	1	1	1	7	
Member status MST				1	0	0	0	8	

4) Subclause 11.2.1.1, High order control packet (see Amendment 1)

Replace the bullet on the CRC-8 with the following:

- The CRC-8 field is sent with one nibble in each of frame #6 and frame #7. (Note that in this paragraph, unless otherwise indicated, the frame numbers are those indicated by the 1st multiframe number field.) The CRC-8 field, $C_1C_2C_3C_4C_5C_6C_7C_8$ is the remainder of the CRC-8 calculation over the control packet. In the example of Table 11-2, the control packet bits are contained in H4[1-4] of the frames 8…15 of multiframe *n* and H4[1-4] of the frames 0…7 of multiframe *n* + 1, (where multiframes *n* and *n* + 1 are indicated by the 2nd multiframe indicator bits). The CRC-8 remainder is calculated as follows: The first 14 nibbles of the control packet bits represent a polynomial *M(x)* of degree 55, where H4[1] of frame 8, 2nd multiframe *n* is the most significant bit and H4[4] of frame 5, 2nd multiframe *n* + 1 is the least significant bit. *M(x)* is first multiplied by x^8 and then divided (modulo 2) by generator polynomial $G(x) = x^8 + x^2 + x + 1$ to produce a remainder *R(x)* of degree 7 or less. *R(x)* is the CRC-8 code with x^7 of *R(x)* corresponding to C_1 as the most significant bit of the remainder and x^0 of *R(x)* corresponding to C_8 as the least significant bit of the remainder;

5) Clause 11.4, Virtual concatenation of X VC-2/1s

Replace Table 11-2/G.707/Y.1322 with the following:

Table 11-2/G.707/Y.1322 – Capacity of virtually concatenated VC-1n-Xv

	X	Capacity	In steps of
VC-11-Xv	1 to 64 (Note)	1600 kbit/s to 102 400 kbit/s	1600 kbit/s
VC-12-Xv	1 to 64	2176 kbit/s to 139 264 kbit/s	2176 kbit/s
VC-2-Xv	1 to 64	6784 kbit/s to 434 176 kbit/s	6784 kbit/s
NOTE – Limited to 64 due to: a) six bits for Sequence indicator in K4 bit 2 frame, and b) inefficient and unlikely to map more than 63 VC-11s in VC-4.			

Change the last paragraph of 11.4 as follows:

The LO virtual concatenation sequence indicator identifies the sequence/order in which the individual VC-1/2s of the VC-1/2-Xv are combined to form the contiguous container ~~V~~C-1/2-Xc as shown in Figures 11-6, 11-7 and 11-8. Each VC-1/2 of a VC-1/2-Xv has a fixed unique sequence number in the range of 0 to (X-1). The VC-1/2 transporting the first ~~time slot of the V~~C-1/2 of the C-1/2-Xc has the sequence number 0, the VC-1/2 transporting the second ~~time slot~~ C-1/2 of the C-1/2-Xc has the sequence number 1 and so on up to the VC-1/2 transporting ~~time slot X of the V~~C-1/2 X of C-1/2-Xc with the sequence number (X-1). For applications requiring fixed bandwidth the sequence number is fixed assigned and not configurable. This allows the constitution of the VC-1/2-Xv to be checked without using the trace.

6) Subclause 11.4.1, Lower order LCAS, VC-m-Xv (m = 11, 12, 2)

Replace Figure 11-10/G.707/Y.1322 in Amendment 1 with the following:

<table>
<tr><td>1</td><td>2</td><td>3</td><td>4</td><td>5</td><td>6</td><td>7</td><td>8</td><td>9</td><td>10</td><td>11</td><td>12</td><td>13</td><td>14</td><td>15</td><td>16</td><td>17</td><td>18</td><td>19</td><td>20</td><td>21</td><td>22</td><td>23</td><td>24</td><td>25</td><td>26</td><td>27</td><td>28</td><td>29</td><td>30</td><td>31</td><td>32</td></tr>
<tr><td colspan="5">Frame indicator</td><td colspan="6">Sequence indicator</td><td colspan="4">CTRL</td><td>GID</td><td colspan="4">Reserved
"0000"</td><td>RS-Ack</td><td colspan="9">Member status</td><td>C_1</td><td>C_2</td><td>C_3</td></tr>
<tr><td colspan="5"></td><td colspan="6"></td><td colspan="4"></td><td></td><td colspan="4"></td><td></td><td colspan="9"></td><td colspan="3">CRC-3</td></tr>
</table>

Figure 11-10/G.707/Y.1322 – K4[2] VC-m-Xv supporting LCAS coding

7) Subclause 11.4.1.1, Low order control packet (see Amendment 1)

Replace the bullet on the CRC-3 with the following:

- CRC-3 field (three bits: 30 to 32), $C_1C_2C_3$, is the remainder of the CRC-3 calculation over the K4[2] bits 1…32. To calculate the CRC, we regard control packet bits 1-29 as a polynomial *M(x)* where K4[2] of frame 1 is the most significant bit and K4[2] of frame 29 is the least significant bit of *M(x)*. *M(x)* is first multiplied by x^3 and then divided (modulo 2) by generator polynomial $G(x) = x^3 + x + 1$ to produce a remainder *R(x)* of degree 2 or less. *R(x)* is the CRC-3 code with x^2 of *R(x)* corresponding to C_1 as the most significant bit of the remainder and x^0 of *R(x)* corresponding to C_3 as the least significant bit of the remainder;

8) New Appendix XII

Add the following new informative Appendix XII, and leave Bibliography unnumbered:

Appendix XII

Example LCAS control packet CRC calculations

XII.1 Example of CRC-8 computation for LCAS and Virtual Concatenation carried in the H4 byte (i.e., VC-3-Xv and VC-4-Xv). See Figure XII.1.

	H4[1-4] function	Most significant nibble H4[1-4]				Least significant nibble H4[5-8]				H4[5-8] value	
		bit 1	bit 2	bit 3	bit 4	bit 5	bit 6	bit 7	bit 8		
MF-2 counter = 201	Member Status [72-79]	0	1	1	0	1	0	0	0	8	LCAS control packet
		1	0	0	0	1	0	0	1	9	
	H4[1-3] = Reserved ('0') H4[4] = RS-Ack ('1')	0	0	0	1	1	0	1	0	10	
	Reserved ('0')	0	0	0	0	1	0	1	1	11	
		0	0	0	0	1	1	0	0	12	
		0	0	0	0	1	1	0	1	13	
	Sequence Number (19 = 13_{HEX})	0	0	0	1	1	1	1	0	14	
		0	0	1	1	1	1	1	1	15	
MF-2 counter = 202	MF-2 counter (202 = CA_{HEX})	1	1	0	0	0	0	0	0	0	
		1	0	1	0	0	0	0	1	1	
	Control Word ('NORM')	0	0	1	0	0	0	1	0	2	
	H4[1-3] = Reserved ('0') H4[4] = GID ('1')	0	0	0	1	0	0	1	1	3	
	Reserved ('0')	0	0	0	0	0	1	0	0	4	
		0	0	0	0	0	1	0	1	5	
	CRC-8 of previous 14 H4[1-4] nibbles	0	1	1	1	0	1	1	0	6	
		1	1	0	0	0	1	1	1	7	
	Member Status [80-87]	0	0	0	0	1	0	0	0	8	LCAS Control Packet
		1	0	0	1	1	0	0	1	9	
	H4[1-3] = Reserved ('0') H4[4] = RS-Ack ('1')	0	0	0	1	1	0	1	0	10	
	Reserved ('0')	0	0	0	0	1	0	1	1	11	
		0	0	0	0	1	1	0	0	12	
		0	0	0	0	1	1	0	1	13	
	Sequence Number (19 = 13_{HEX})	0	0	0	1	1	1	1	0	14	
		0	0	1	1	1	1	1	1	15	
MF-2 counter = 203	MF-2 counter (203 = CB_{HEX})	1	1	0	0	0	0	0	0	0	
		1	0	1	1	0	0	0	1	1	
	Control Word ('NORM')	0	0	1	0	0	0	1	0	2	
	H4[1-3] = Reserved ('0') H4[4] = GID ('0')	0	0	0	0	0	0	1	1	3	
	Reserved	0	0	0	0	0	1	0	0	4	
		0	0	0	0	0	1	0	1	5	
	CRC-8 of previous 14 H4[1-4] nibbles	0	0	1	1	0	1	1	0	6	
		1	0	0	1	0	1	1	1	7	
	Member Status [88-95]	0	0	0	0	1	0	0	0	8	
		0	0	0	0	1	0	0	1	9	

Figure XII.1/G.707/Y.1322 – High order LCAS CRC calculation example

XII.2 Example of CRC-3 computation for LCAS and Virtual Concatenation carried in bit 2 of the K4 byte (i.e., VC-2-Xv, VC12-Xv and VC-11-Xv). See Figure XII.2.

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
K4[1] 32-bit multiframe structure																															
0	1	1	1	1	1	1	1	1	1	0	Signal label extension								0	Unused						0	Unused				
K4[2] 32-bit multiframe structure																															
Multiframe-2 indicator								Sequence number			LCAS control information																				
											CTRL					GID		Reserved "0000"			RS-Ack					Member status				C_1	C_1	C_3
																													CRC-3		
Example:																															
MF-2 = 7, Sequence Number = 22, CTRL = NORM, Member Status of members 56-63																															
0	0	1	1	1	0	1	0	1	1	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	1	0
MF-2 = 8, Sequence Number = 22, CTRL = NORM, Member Status of members 0-7																															
0	1	0	0	0	0	1	0	1	1	0	0	0	1	0	1	0	0	0	0	1	0	1	0	0	1	0	0	0	0	0	1
MF-2 = 9, Sequence Number = 22, CTRL = NORM, Member Status of members 8-15																															
0	1	0	0	1	0	1	0	1	1	0	0	0	1	0	1	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1	0
MF-2 = 10, Sequence Number = 22, CTRL = NORM, Member Status of members 16-23																															
0	1	0	1	0	0	1	0	1	1	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	1

Figure XII.2/G.707/Y.1322 – Low order LCAS control packet examples including the CRC-3

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