

ITU-T

TELECOMMUNICATION
STANDARDIZATION SECTOR
OF ITU

G.7043/Y.1343

Corrigendum 1
(12/2006)

SERIES G: TRANSMISSION SYSTEMS AND MEDIA,
DIGITAL SYSTEMS AND NETWORKS

Data over Transport – Generic aspects – General

SERIES Y: GLOBAL INFORMATION
INFRASTRUCTURE, INTERNET PROTOCOL ASPECTS
AND NEXT-GENERATION NETWORKS

Internet protocol aspects – Transport

Virtual concatenation of plesiochronous digital
hierarchy (PDH) signals

Corrigendum 1

ITU-T Recommendation G.7043/Y.1343 (2004) –
Corrigendum 1

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ITU-T Recommendation G.7043/Y.1343

Virtual concatenation of plesiochronous digital hierarchy (PDH) signals

Corrigendum 1

Summary

This corrigendum provides a correction to the differential delay calculation for 34 368 kbit/s signal and modifies the text in three areas where ambiguities have been identified that could potentially lead to interworking issues. These areas pertain to MST frame alignment, the definition of a "container frame", and the proper operation of MFI2 MSBs for 1544 and 2048 kbit/s signals.

Source

Corrigendum 1 to ITU-T Recommendation G.7043/Y.1343 (2004) was approved on 14 December 2006 by ITU-T Study Group 15 (2005-2008) under the ITU-T Recommendation A.8 procedure.

FOREWORD

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In this Recommendation, the expression "Administration" is used for conciseness to indicate both a telecommunication administration and a recognized operating agency.

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Virtual concatenation of plesiochronous digital hierarchy (PDH) signals

Corrigendum 1

1) Clause 6.1.1

Add the following sentence to the end of the first paragraph in 6.1.1:

For the purpose of virtual concatenation, the 1544-kbit/s container frame is the multiframe shown in Figure 6-1.

2) Clause 6.1.2.1

Modify the heading of Figure 6-3 and add notes as follows:

MFI2 bit 8 (LSB) value	Concatenation overhead VLI octet				
	Bit 1	Bit 2	Bit 3	Bit 4	
0	0	1	2	3	Member numbers
	4	5	6	7	
1	8	9	10	11	
	12	13	14	15	

NOTE 1 – There are 8 member statuses reported per control packet. The 16 members require 2 control packets at a rate of 48 ms each for the 1544 kbit/s signal and 32 ms each for the 2048-kbit/s signal. If there is only one return channel, this results in the member status being refreshed every 96 ms for the 1544-kbit/s signal and every 64 ms for the 2048-kbit/s signal.

NOTE 2 – Since there is a maximum of 16 members, only the MFI2 bit 8 (LSB) is used to determine which member status is transmitted in the 8-bit MST field of a control packet. MFI2 bit 8 corresponds to concatenation overhead octet bit 4 when MFI1 = 1001. The interpretation of the member status bits according to this table is based on the MFI2 value at the moment the member status word is received. In other words, MFI2 bit 8 is read and used as an index into this table to identify the members for which the status will be sent in the subsequent MST field. This subsequent MST field is carried in the first 8 bits of the next control packet.

**Figure 6-3/G.7043/Y.1343 – Member status bit assignments for
 $N \times 1544/2048$ kbit/s signals**

3) Clause 6.1.2.2

Modify 6.1.2.2 as follows:

All N 1544 kbit/s member signals that constitute a VCG are aligned at their transmission from the VCG source with respect to their 1544-kbit/s clock frequency, PDH signal frame and multiframe, MFI1 and MFI2. The VCG sink can determine the differential delay that the different members encountered in the network by comparing their respective MFI1 and MFI2 values, and performing the proper realignment. Note that the four MSBs of MFI2 are not used for differential delay compensation. The maximum differential delay that can be detected is $\pm(256)(24)(125\mu\text{s})/2 = \pm 384$ ms. Note that even though they are not used for differential delay calculation, the four MFI2 MSBs shall continue to increment as part of the 12-bit MFI1-MFI2 counter.

4) Clause 6.2.1

Add the following sentence to the end of the first paragraph in 6.2.1:

For the purpose of virtual concatenation, the 2048-kbit/s container frame is the multiframe shown in Figure 6-4.

5) Clause 6.2.2.2

Modify 6.2.2.2 as follows:

The differential delay compensation for the 2048 kbit/s signal is the same as specified in 6.1.2.2 except that the clock frequency is 2048 kbit/s. Note that the four MSBs of MFI2 are not used for differential delay compensation. The maximum differential delay that can be detected is $\pm(256)(16)(125\mu\text{s})/2 = \pm 256$ ms. Note that even though they are not used for differential delay calculation, the four MFI2 MSBs shall continue to increment as part of the 12-bit MFI1-MFI2 counter.

6) Clause 6.3.1

Add the following sentence to the end of the first paragraph in 6.3.1:

For the purpose of virtual concatenation, the 34 368-kbit/s container frame is the multiframe shown in Figure 6-5.

7) Clause 6.3.2.1

Modify the heading of Figure 6-7 as follows:

Frame number (MFI1)	Concatenation overhead VLI octet				Member numbers
	Bit 1	Bit 2	Bit 3	Bit 4	
0	0	1	2	3	Member numbers
1	4	5	6	7	

**Figure 6-7/G.7043/Y.1343 – Member status bit assignments for
 $N \times 34\,368$ and $N \times 44\,736$ kbit/s signals**

8) Clause 6.3.2.2

Modify 6.3.2.2 as follows:

All N 34 368 kbit/s member signals that constitute a VCG are aligned at their transmission from the VCG source with respect to their 34 368 kbit/s clock frequency, PDH signal frame and multiframe, MFI1 and MFI2. The VCG sink can determine the differential delay that the different members encountered in the network by comparing their respective MFI1 and MFI2 values, and performing the proper realignment. The maximum differential delay that can be detected is $\pm[(536537)(8)(2^{12})]/2/34368000 = \pm 255256$ ms.

9) Clause 6.4.1

Add the following sentence to the end of the first paragraph in 6.4.1:

For the purpose of virtual concatenation, the 44 736-kbit/s container frame is the multiframe shown in Figure 6-8.

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