Ethernet's Response to the AI Industry

The IEEE 802.3 400 Gb/s/Lane Signaling Study Group

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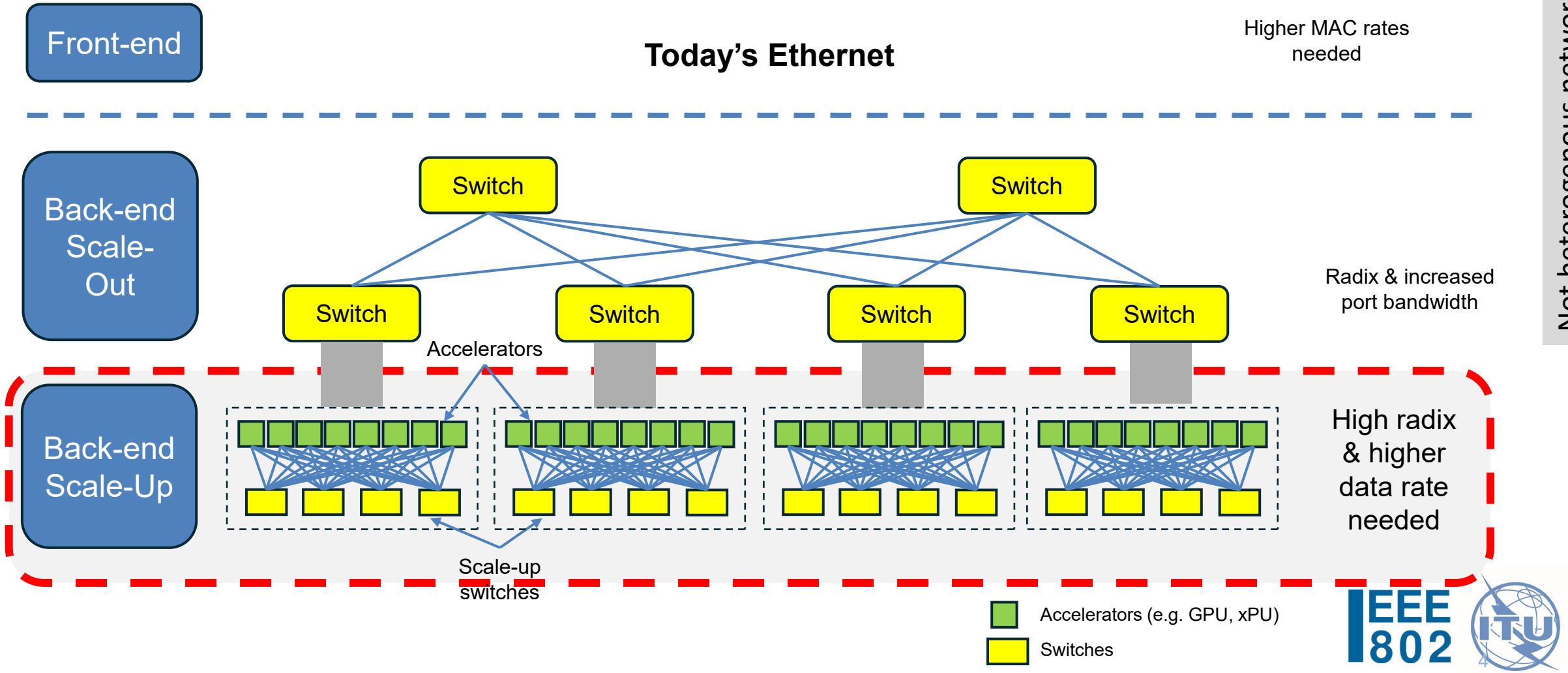
Agenda

- Focus of IEEE 802.3 400 Gb/s/lane Study Group (i.e. IEEE P802.3dv*)
- Capabilities & Architectures for Consideration
- Error Allocation

* Note: Pending Task Force formation approvals

Looking Closer at the AI Backend Network



Not heterogenous networks

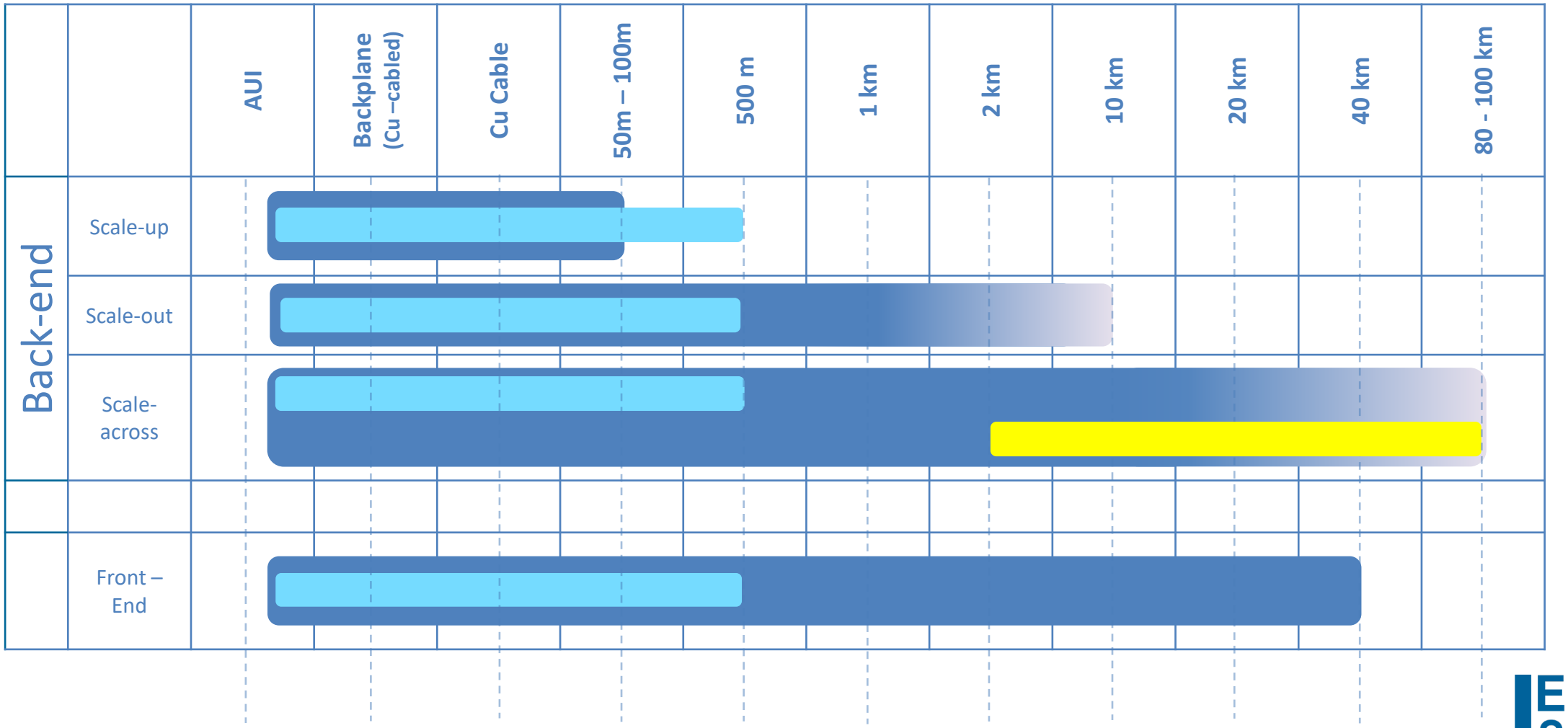
Looking Forward

- AI back-end “scale-up” networks are driving higher signaling rates first
  - Followed by scale-out
  - Then front-end networks
- Scale-up = high radix
  - Flat network, lots of one-lane and two-lane links
- Copper excels due to low cost & power and high reliability, but the reach is limited and shrinking
- Optics have a growing footprint in scale-up (and, of course, scale-out) to meet reach and cluster size requirements
  - Power optimized solutions, such as Co-packaged optics (CPO) implementations, are increasingly important

Observations based on Alan Weckel’s contribution to E4AI:

- Back-end scale out will be ~10x relative growth when compared to front end networks
- Back-end scale out will be ~100x relative growth when compared to front end networks

“AI Networks” Industry Need versus Efforts



Radix “break-out”

“Fat-Pipe” Point-to-point

Industry Need

IEEE 802.3 400GPL SG

ZR Optics – May be used as part of DWDM system

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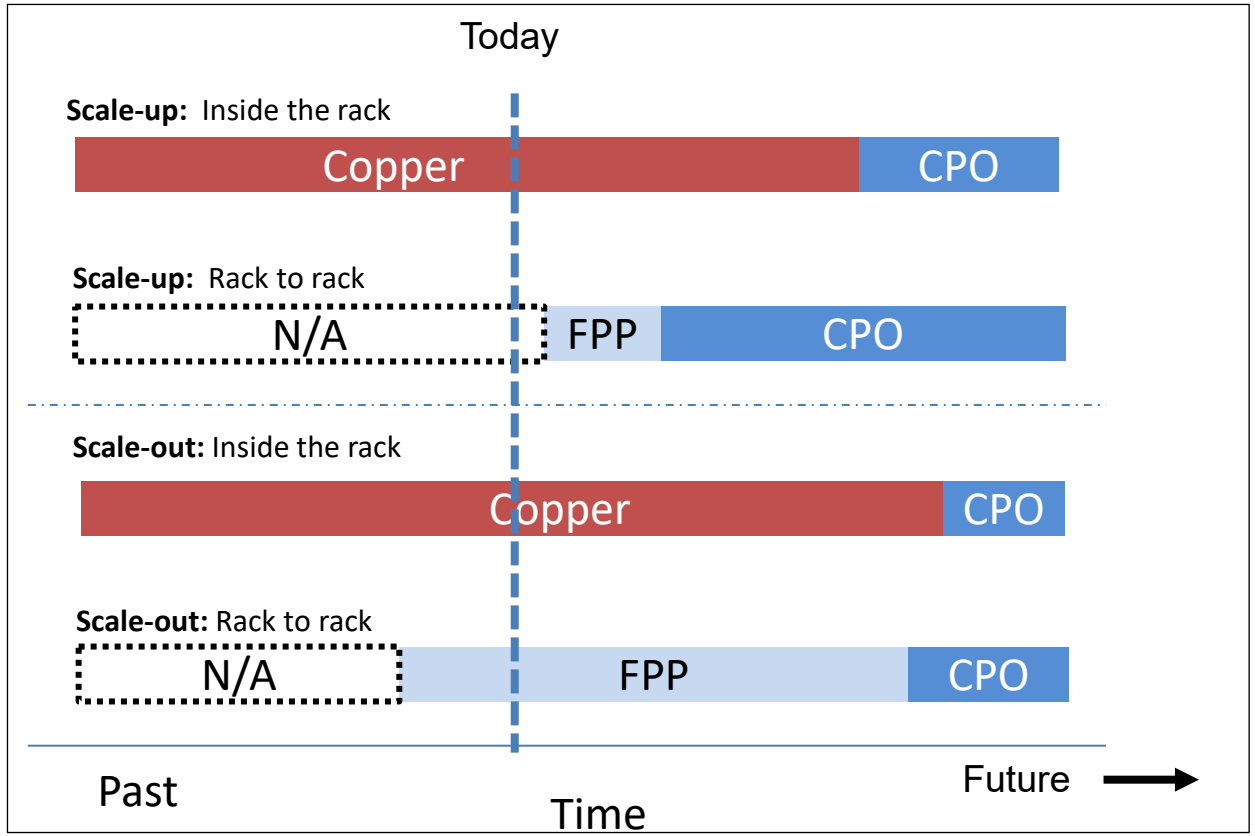
I/O Transitions for AI

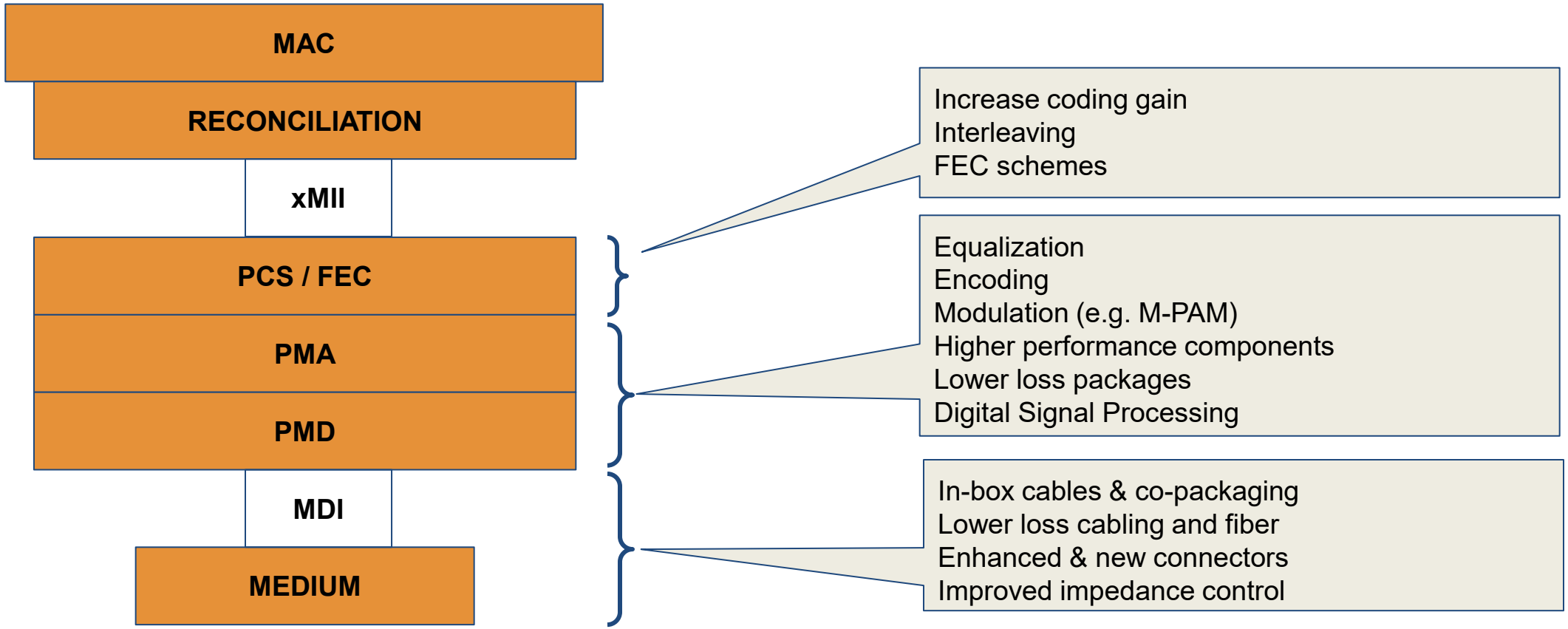
- Current and future transitions involve Copper, front panel pluggable (FPP) optics, and CPO/NPO
- Copper dominates inside-the-rack connections today but shifts toward optics over time
- Rack-to-rack connections transition from pluggable to CPO
- Market requires both copper and optical PMDs @ 400G



Based on data presented in https://www.ieee802.org/3/ad_hoc/E4AI/public/25_0327/weckel_e4ai_01_250327.pdf

Requirements for BOTH electrical and optical PMDs

Opening the Toolbox Again



SERDES Capability is a Key Enabler

Data rate per lane, Gb/s	10	25	50	100	200	400
Modulation	PAM-2	PAM-2	PAM-4	PAM-4	PAM-4	?
Nominal cable reach, m	7	5	3	2	1~2[1]	?
Technology added	DFE	RS FEC	Stronger RS FEC	Floating-tap DFE	MLSD	?
Year[2]	2007	2014	2018	2022	2026 (est.)	?

[1] Nominal cable reach is a function of host class
[2] Year of publication of the IEEE 802.3 Ethernet standard.

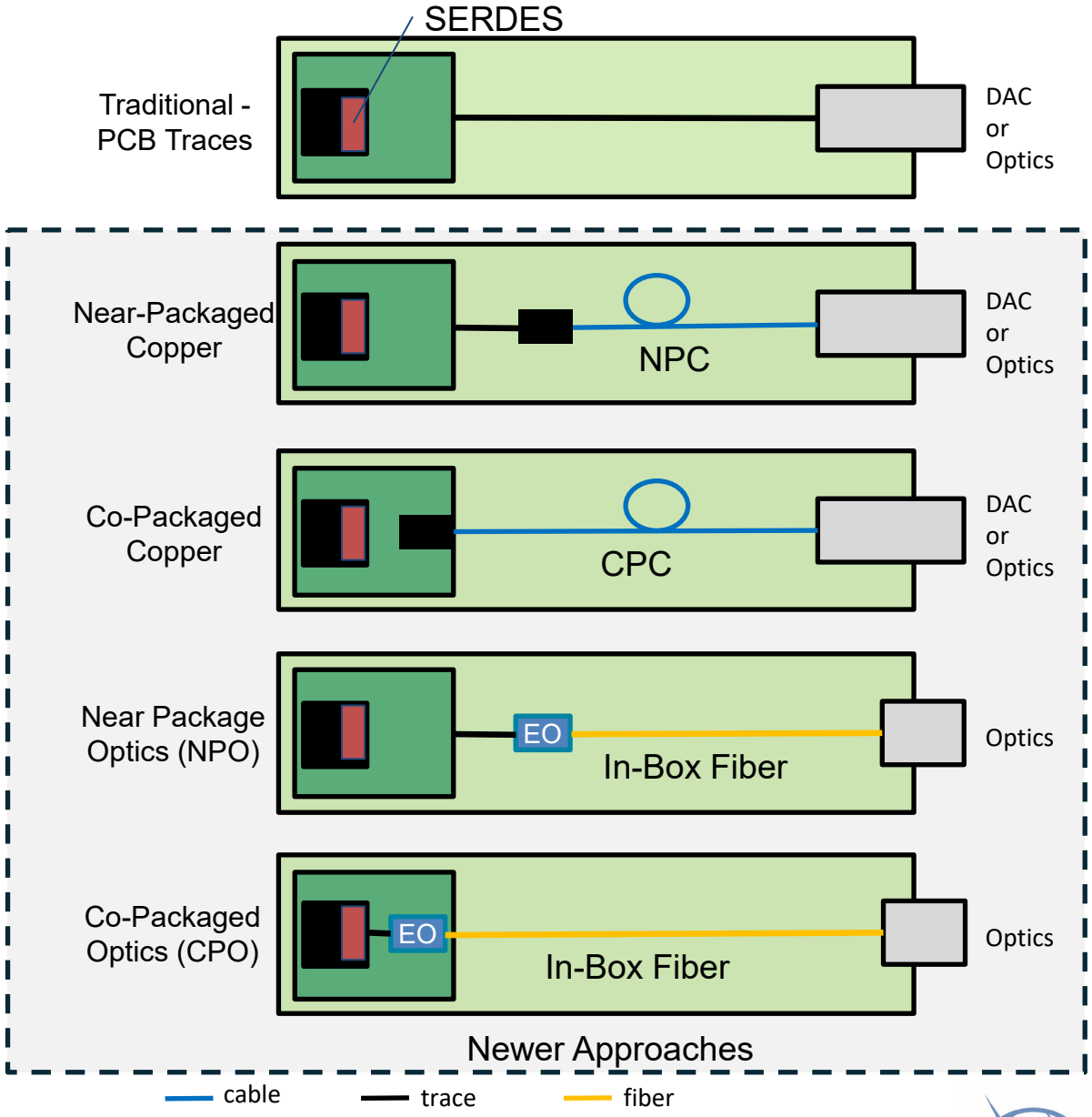
DFE = decision feedback equalizer
FEC = forward error correction
MLSD = maximum-likelihood sequence detector
RS = Reed-Solomon

- New standard for doubling the data rate every 4 years
- New capabilities added for each generation to address challenges presented by doubling the data rate
- What will be required for the next doubling of data rate? Numerous options have already been explored…

Used with permission by Adam Healey, Broadcom

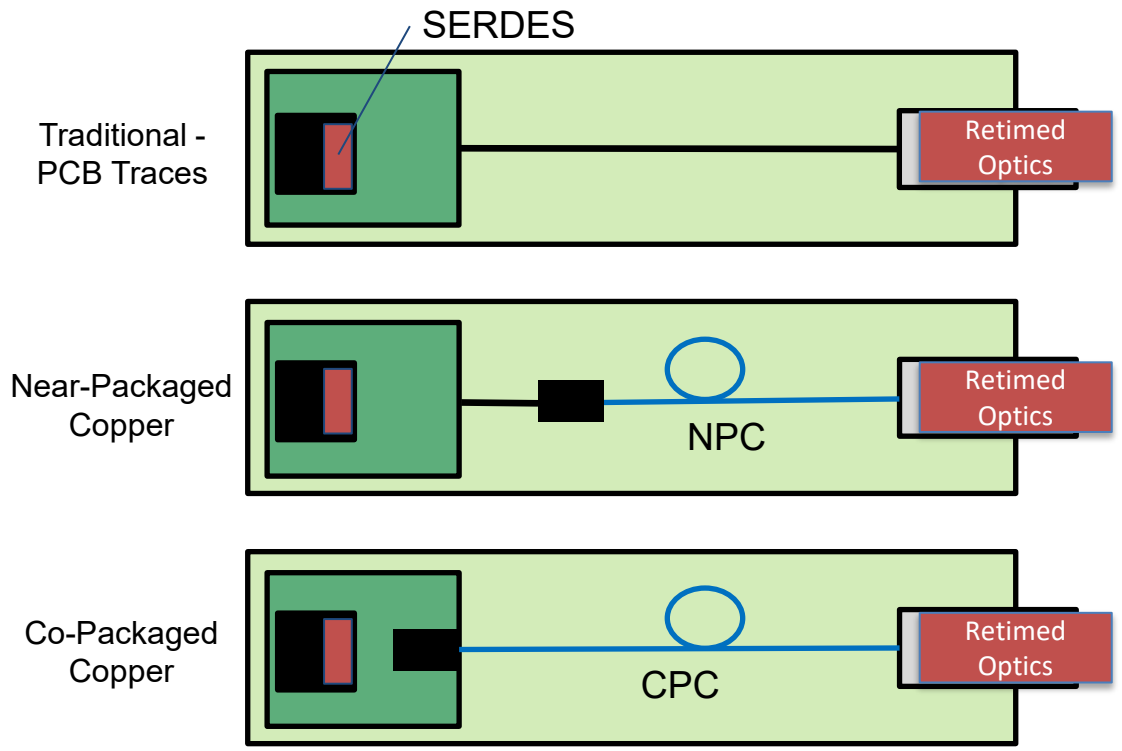
System Architectures

- Broader mix of system architectures than before
  - PCB traces to front panel pluggable (FPP)
  - Near-packaged and Co-packaged copper to FPP
  - Near-Package Optics (NPO)
  - Co-Packaged Optics (CPO)
- A variety of approaches depending on system requirements & limitations
- All need SERDES



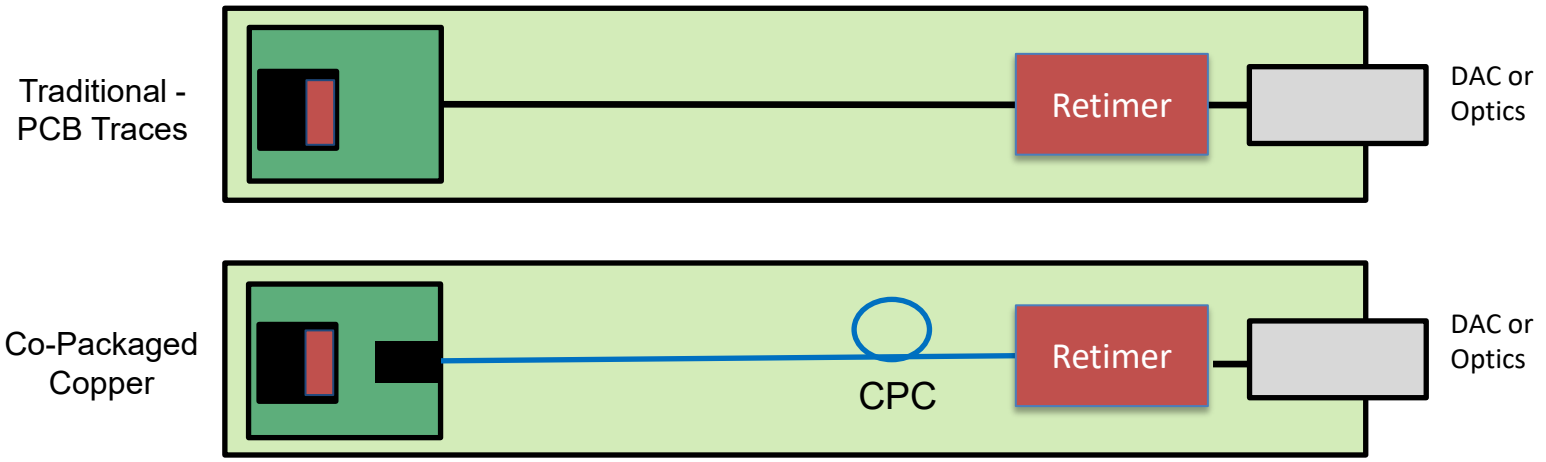
400 Gb/s/lane AUI C2M

- Evolution of AUI C2M beyond the traditional use case
- Optics physical location varies within the system
- E.g. IEEE P802.3dj Annex 176D



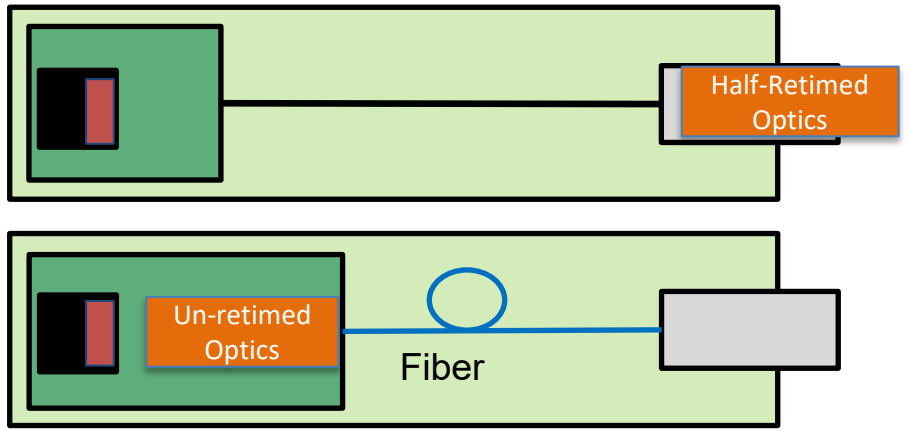
400 Gb/s/lane AUI C2C

- AUI C2C when needed for FPP support
- Support extender sublayer (XS) use case
- E.g. IEEE P802.3dj Annex 176C



Evolving Needs

- Traditional definition of AUI is blurred with new system architectures



Active Electrical Cable (AEC)

Active Copper Cable (ACC)

Frame Loss Ratio (FLR)

- Use of FEC in the PCS means that after PCS decoding, including error correction, either there are no singular errors or there is a large set of bits that are discarded when an FEC codeword is uncorrectable.
- As such, the effective BER target of 10-13 has been translated into a frame loss ratio (FLR) target at the MAC service interface as follows:
  - “The frame loss ratio for 64-octet MAC frames with minimum interpacket gap is expected to be less than 6.2 × 10–11.”

Frame Loss Ratio (FLR) Formalization

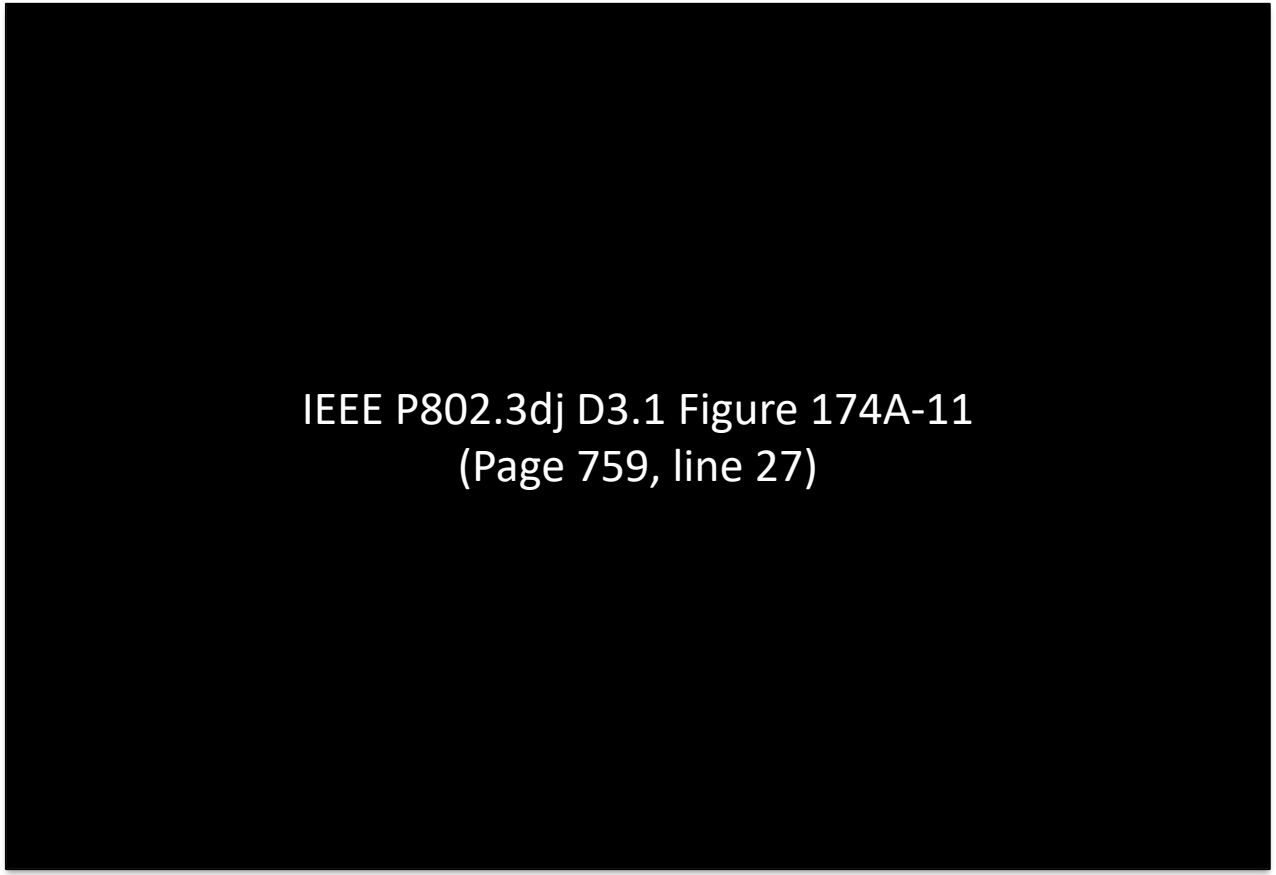
- IEEE 802.3dj (currently Draft 3.1) formalizes the allocation of error ratio to a MAC-to-MAC path. See Annex 174A.
  - It allocates a small portion for the FLR (0.1E-11) to each of the xMII Extenders leaving 6.0E-11 for the PCS-to-PCS path
  - BER and FLR is allocated to the various physical interfaces according to the table and figures that follow
  - These allocations can be readjusted inside of a system where the equipment is controlled/engineered. For instance, a PHY using co-packaged optics (CPO) could allocate 100% BER to the PMD
  - Provides methodology and metric to constrain the correlation of errors with the parameter block error ratio (BLER) to ensure the target FLR is achieved

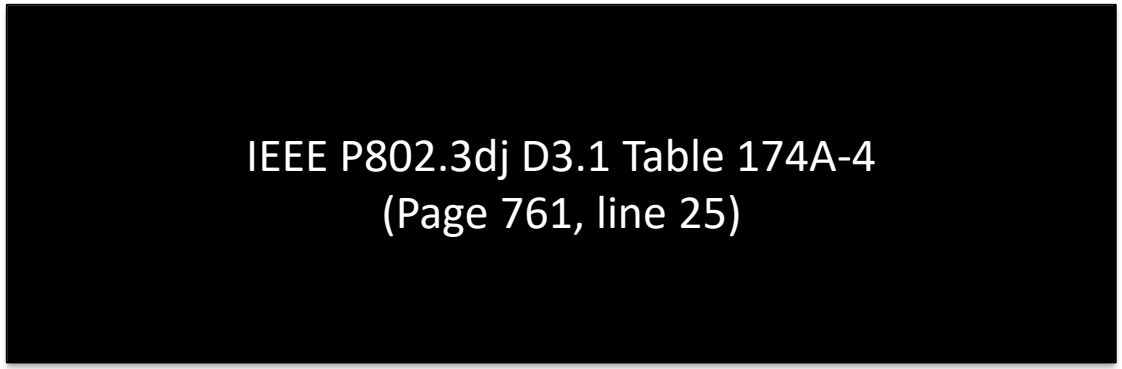
IEEE P802.3dj Annex 174 FLR Allocations

- We need to be considerate of interoperation within networks mixing 400 Gb/s/lane and previous generations of interfaces.
- A 400 Gb/s/lane PMD should work with legacy, e.g., 200 Gb/s/lane C2M and/or C2C AUI
  - the error allocation should be no worse than a 200 Gb/s/lane PMD
- A 400 Gb/s/lane AUI should work with legacy, e.g., 200 Gb/s/lane PMD a
  - the error allocation should be no worse than a 200 Gb/s/lane AUI nd AUIs

IEEE P802.3dj D3.1 Figure 174A-6
(Page 757, line 4)

800GBASE-ER1 Error Allocations





Summary

- AI scale-up networks are the fastest growing segment and require 400 Gb/s lane rates
- IEEE 802.3 400 Gb/s/lane SG (i.e. IEEE P802.3dv*) will provide electrical and optical interface building blocks for future efforts to use
- New system architectures to support with AUI C2M and AUI C2C interfaces
  - New paradigms to consider, too (e.g. NPO, CPO)
- The BER and FLR expectations at the MAC service interface should be the same as already defined for 400GE, 800GE, and 1.6TE
  - BER < 1E-13, FLR < 6.2E-11

* Note: Pending Task Force formation approvals

THANKS!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