

Photonics for AI Infrastructure – Scale Across

The Photonics Systems Group

Department of Electrical and Computer Engineering

McGill University

www.photonics.ece.mcgill.ca/Plant/Plant.html

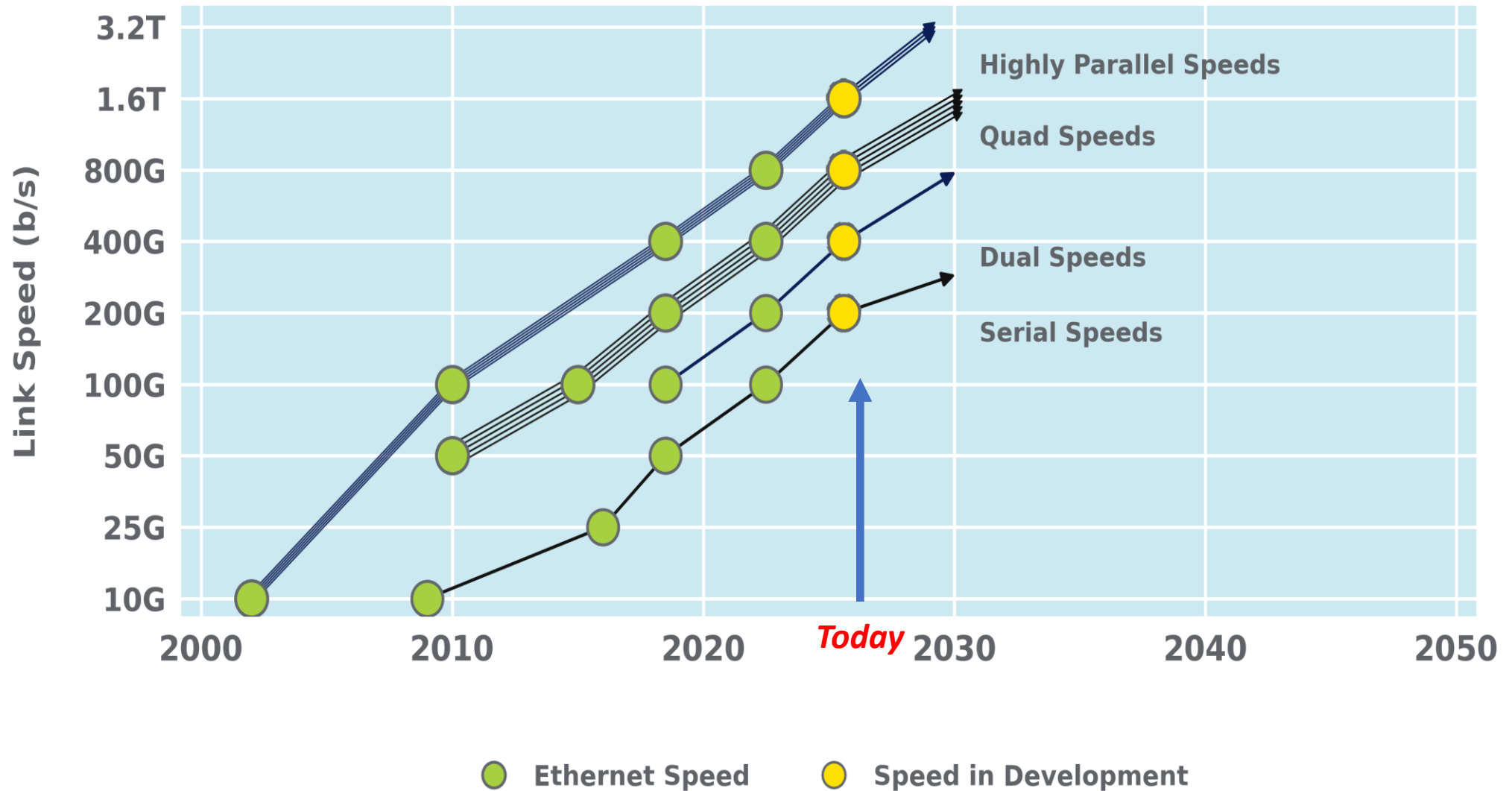
OFC

July 5, 2026

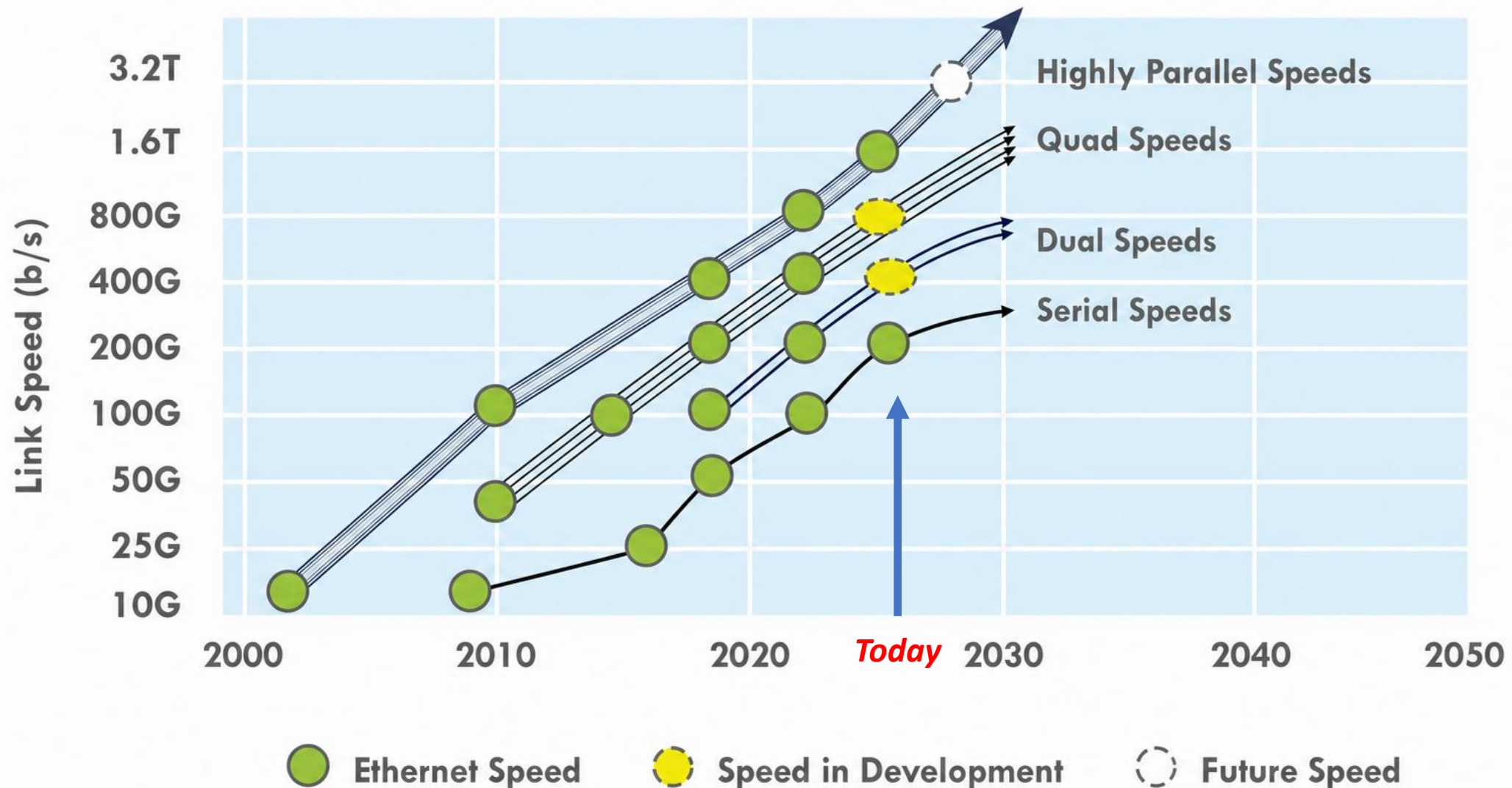
Outline

- Ethernet Roadmap
 - 2025
 - 2026
- Recent IM/DD Transmission Systems
- System Performance Analysis
- Conclusions

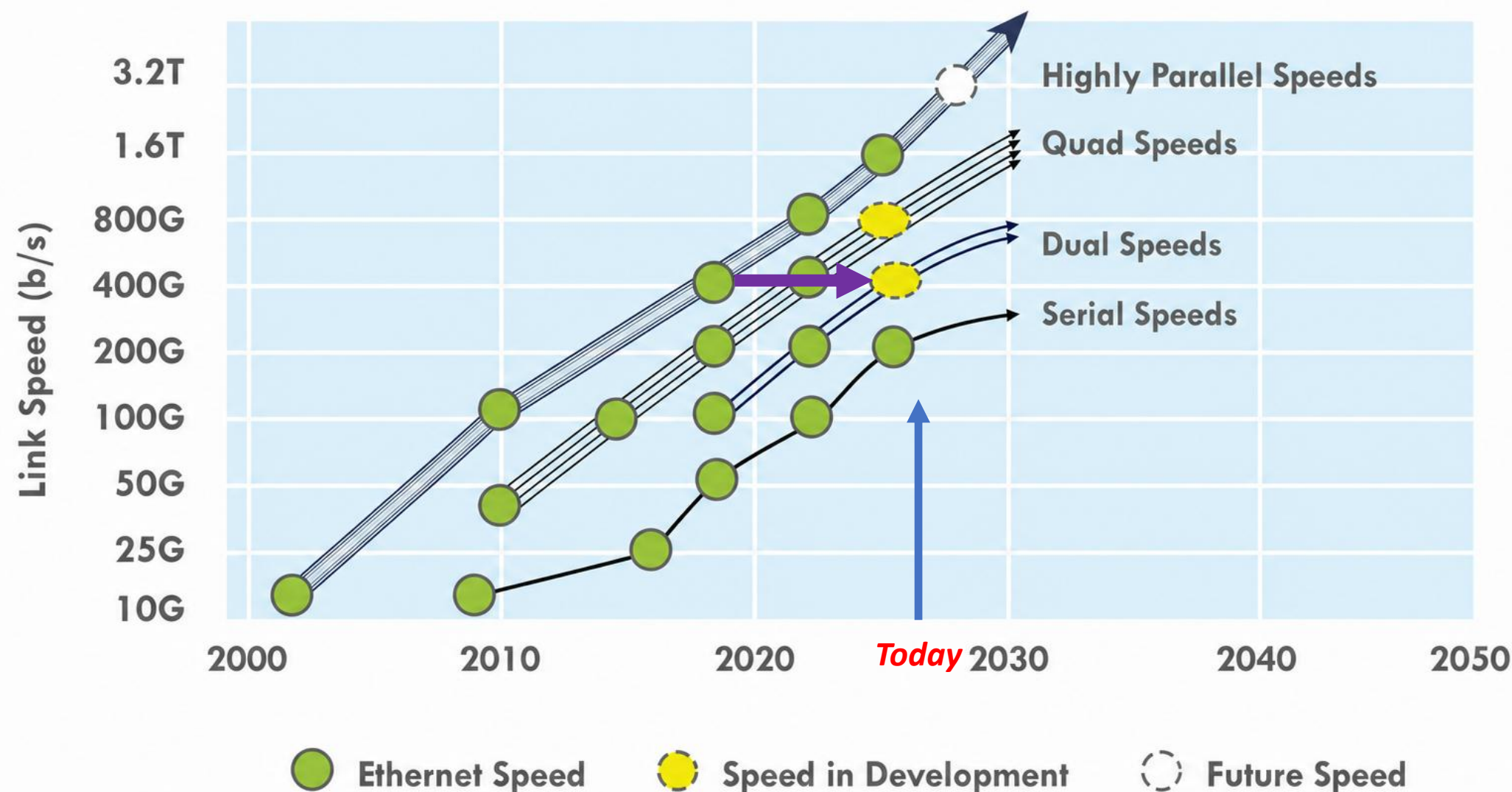
Ethernet Roadmap: Path to Single Lane (2025)



Ethernet Roadmap: Path to Single Lane (2026)

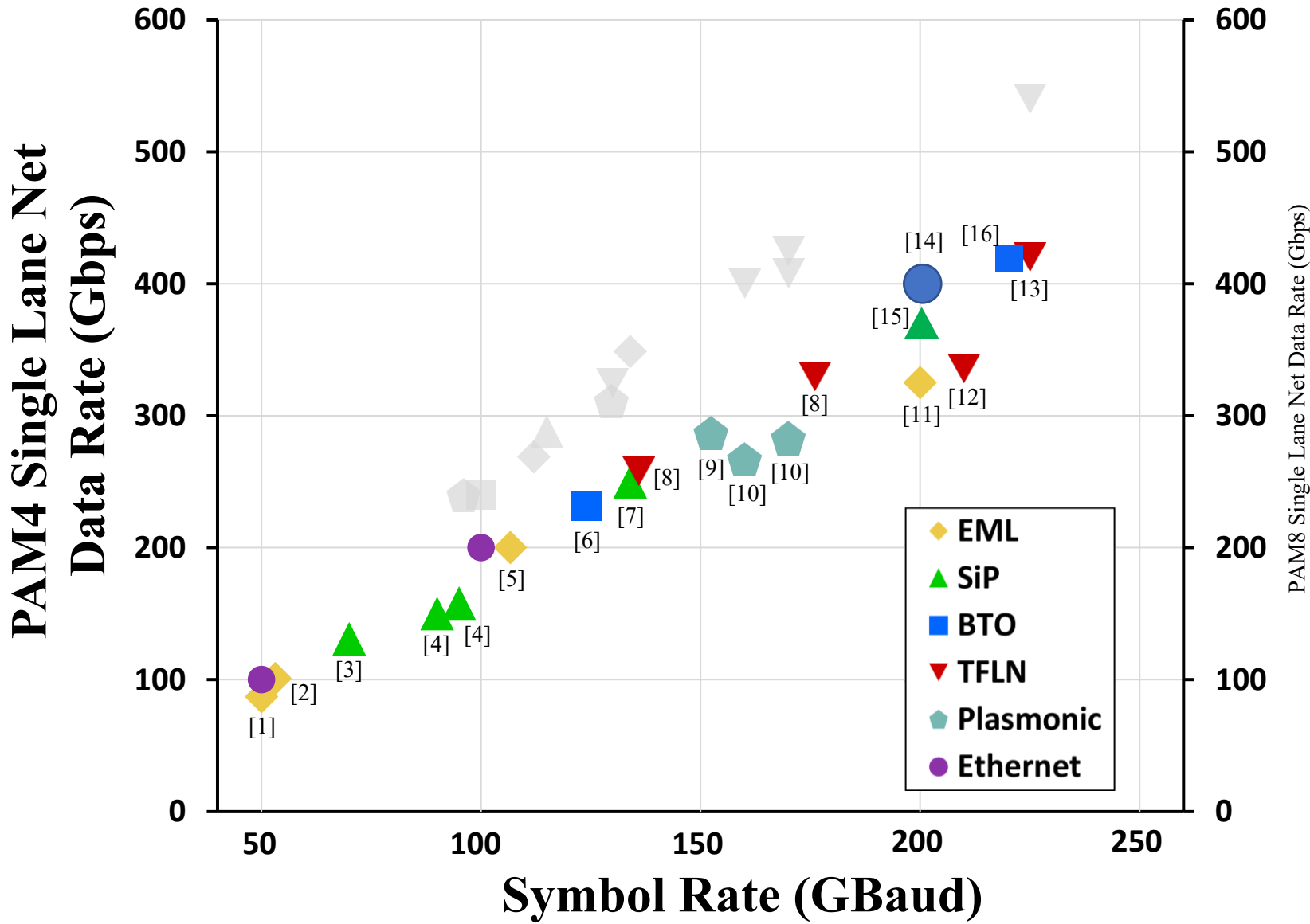


Ethernet Roadmap: Path to Single Lane (2026)



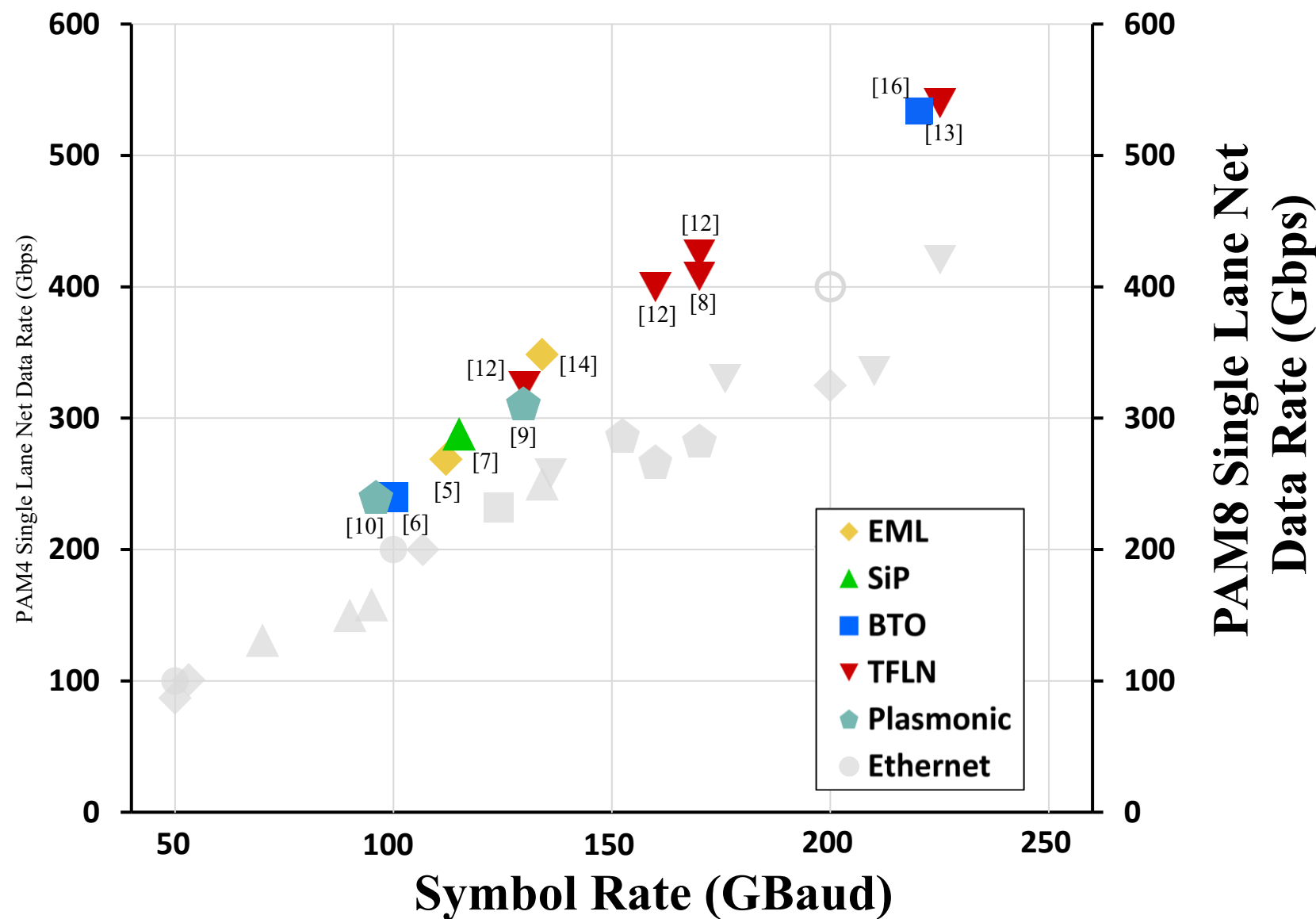
- Ethernet Alliance roadmap:
 - 200G Serial Speeds moved from Speed in Development to Ethernet Speed
 - 1.6T Highly Parallel Speeds point moved from Speed in Development to Ethernet Speed.
- CMOS ASIC scaling:
 - 3 nm-class FinFET → 2 nm-class nanosheet/GAA;
 - transistor density increased by ~15% for mixed designs and up to ~20% for logic-only blocks.
- Ethernet bandwidth scaling is being driven not only by CMOS scaling, but also by higher order modulation formats, DSP, SerDes, optical/electrical device advances, and lane parallelism.

Recent Reports: PAM4 with Six Platforms



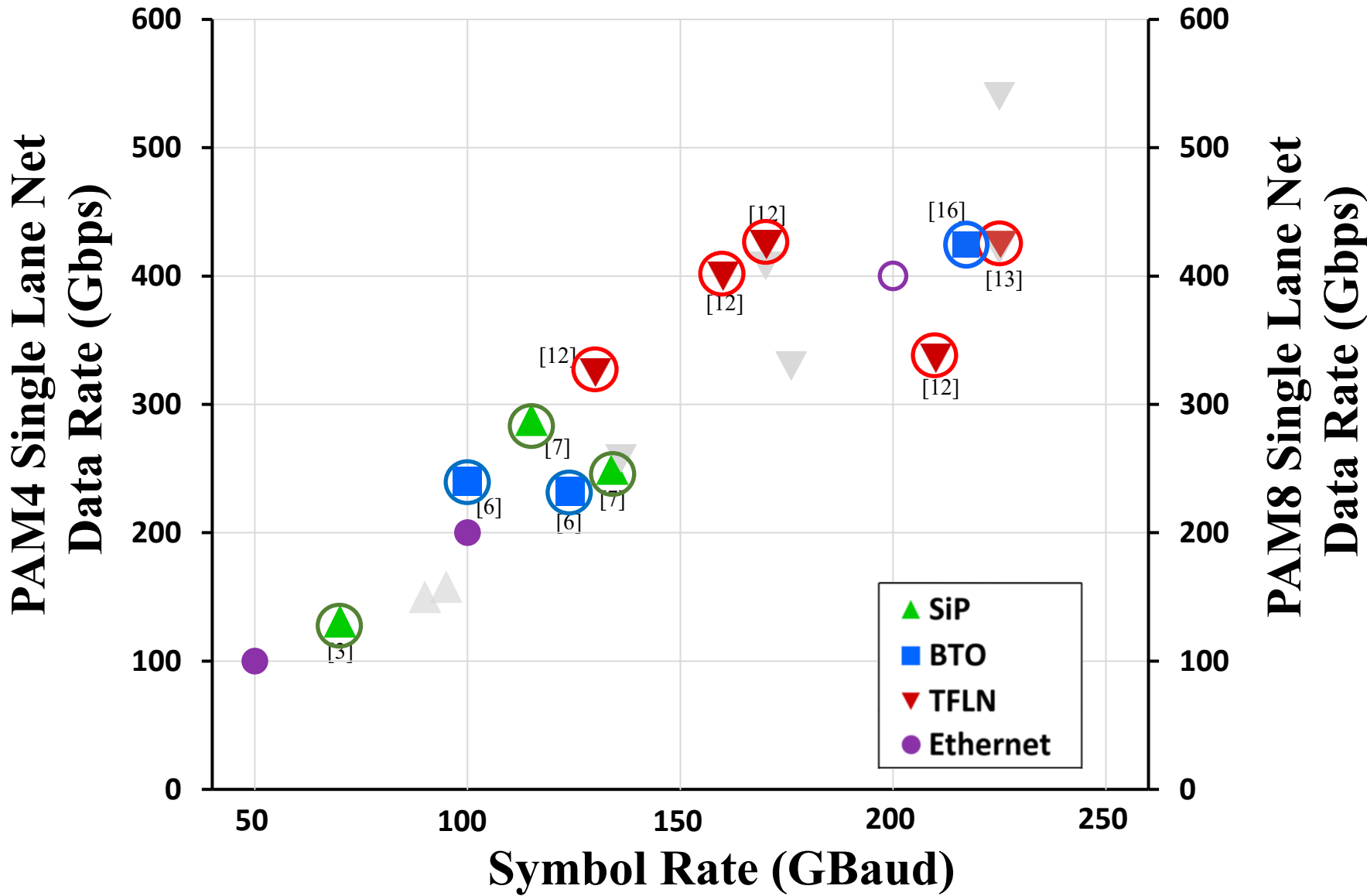
[1] J. Potet, PTL, 2022
[2] J. Y. Huh, OE, 2022
[3] E. Berikaa, PTL, 2022
[4] Z. Zhang, LPR, 2025
[5] W. Li, ECOC, 2024
[6] W. Li, JTL, 2024
[7] E. Berikaa, OFC, 2022
[8] E. Berikaa, PTL, 2023
[9] Q. Hu, JLT, 2022
[10] M. Kohli, OFC, 2024
[11] H. Asakura, ECOC, 2024
[12] C. St-Arnault, OFC, 2024
[13] C. St-Arnault, OFC, 2025
[14] OFC Exhibit Floor, 2025
[15] Po Dong, OFC 2026
[16] B. Qiu, C St-Arnault, OFC 2026

Recent Reports: PAM8 with Six Platforms



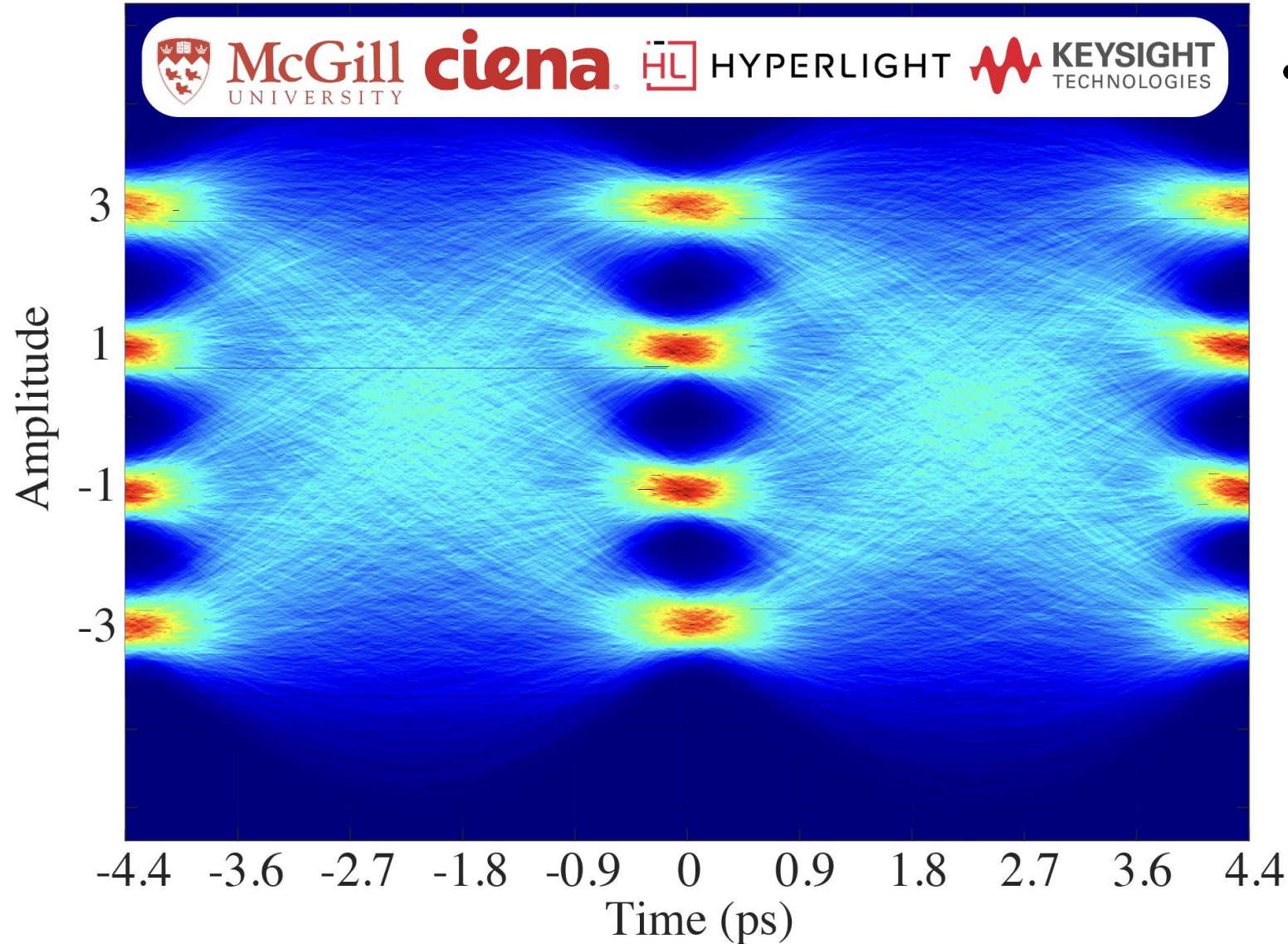
- [5] W. Li, ECOC, 2024
- [6] W. Li, JTL, 2024
- [7] E. Berikaa, OFT, 2022
- [8] E. Berikaa, PTL, 2023
- [9] Q. Hu, JLT, 2022
- [10] M. Kohli, OFC, 2024
- [12] C. St-Arnault, OFC, 2024
- [13] C. St-Arnault, OFC, 2025
- [16] B. Qiu, C. St-Arnault
OFC 2026

Recent Reports: Detailed Results



[3] E. Berikaa, PTL, 2022
[6] W. Li, JTL, 2024
[7] E. Berikaa, OFT, 2022
[12] C. St-Arnault, OFC, 2024
[13] C. St-Arnault, OFC, 2025
[16] B. Qiu, C. St-Arnault
OFC 2026

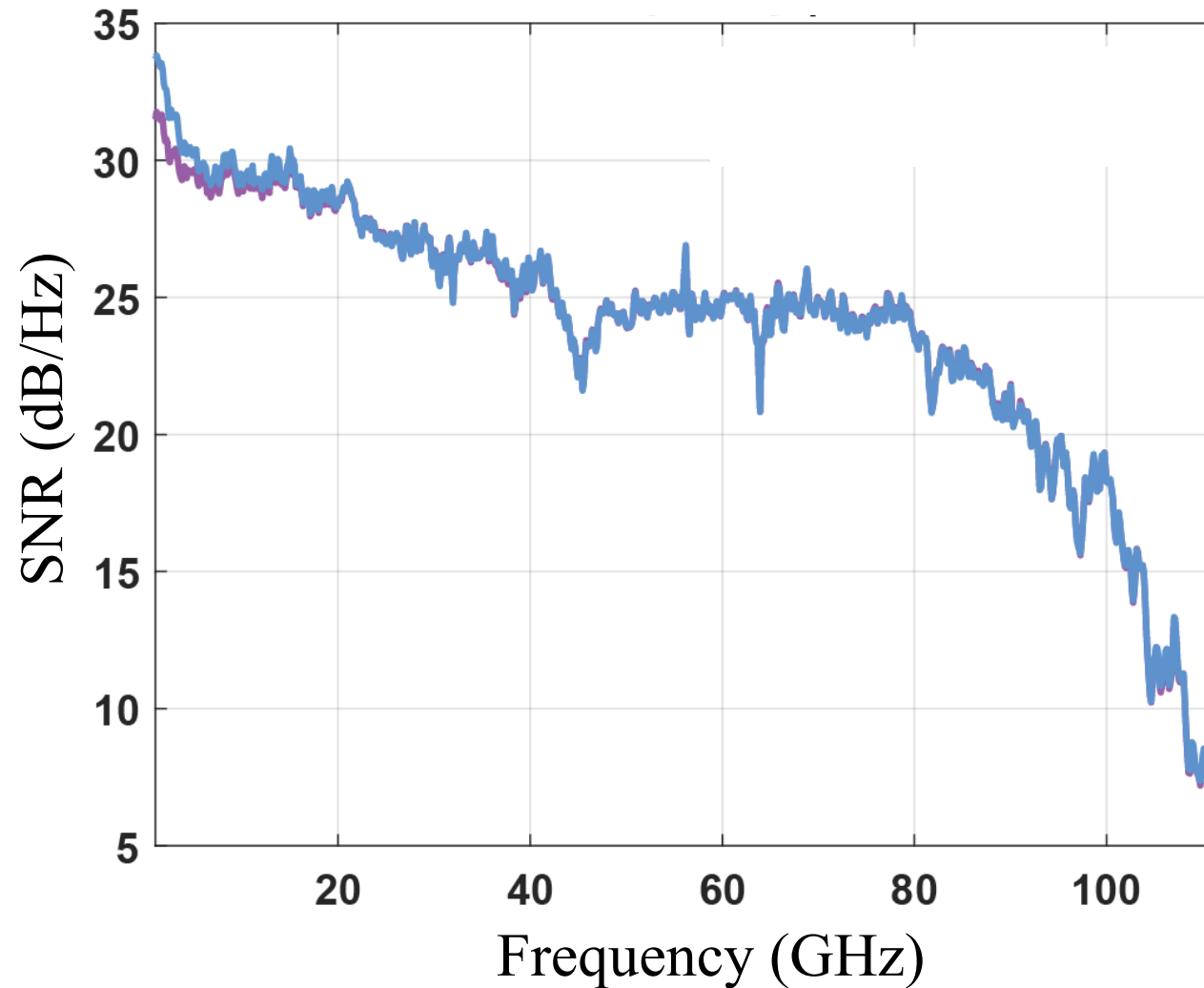
225 GBaud, 450 Gbps Transmission in O-Band



- Net 3.2 Tbps with the following two architectures:
 - 8-WDM at 2 km
 - DR8 at 500 m and 2 km

C. St-Arnault, PDP, OFC, 2025

Measured Received SNR vs. Frequency @ 225 GBaud/448 Gbps PAM4

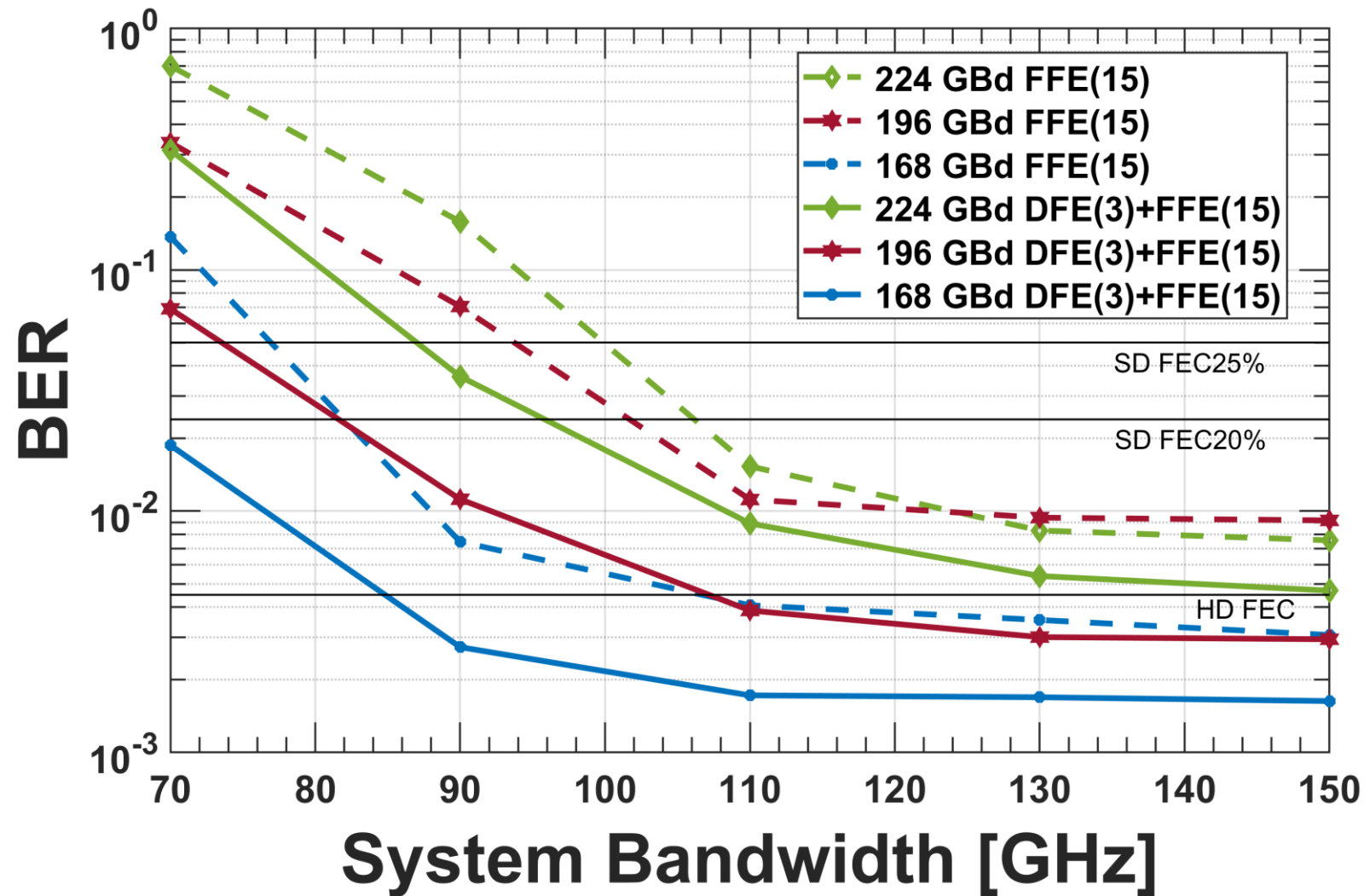


- SiP, BTO, and TFLN modulators offer unique bandwidth, drive voltage, and insertion-loss advantages
- PAM8, probabilistic shaping, and nonlinear equalizers enable high capacities under standard FEC thresholds
- Multi-wavelength channel plans achieve multi-terabit throughput
- System analysis underscores bandwidth and noise impact on performance

System Performance

Bandwidth, Noise

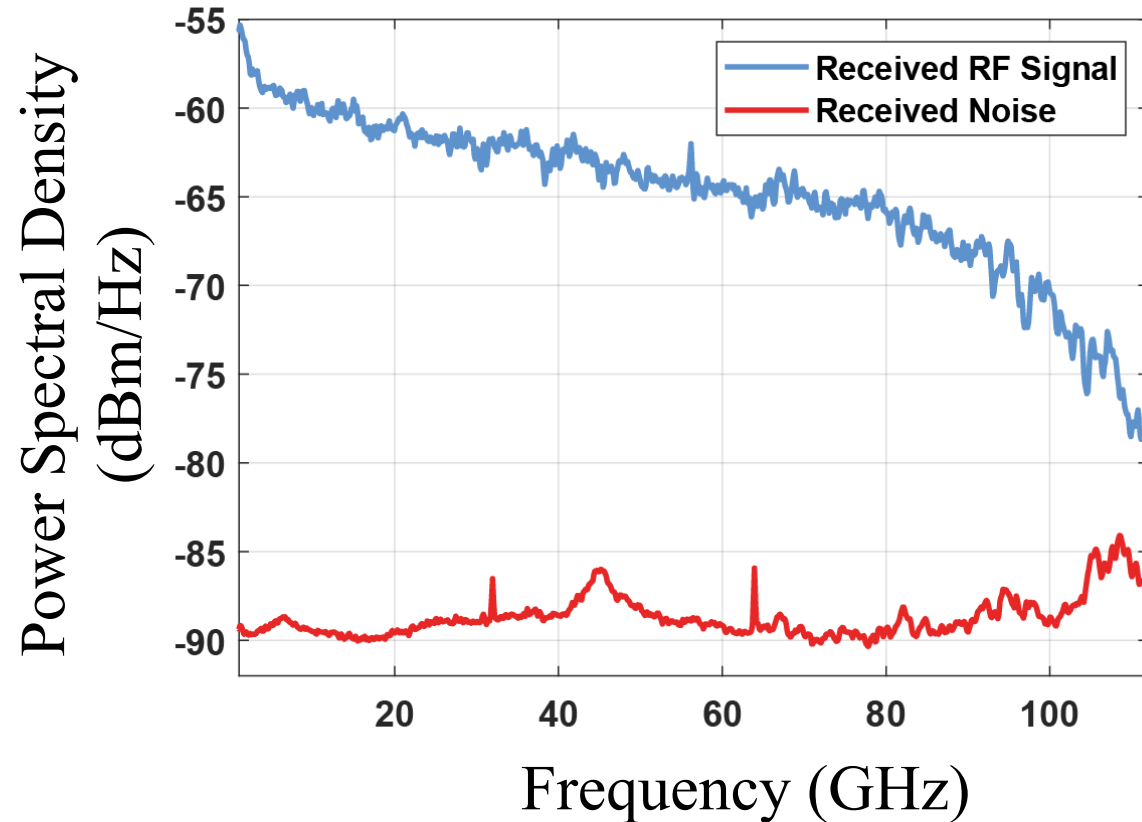
BER vs. System Bandwidth: FFE vs. DFE Comparison



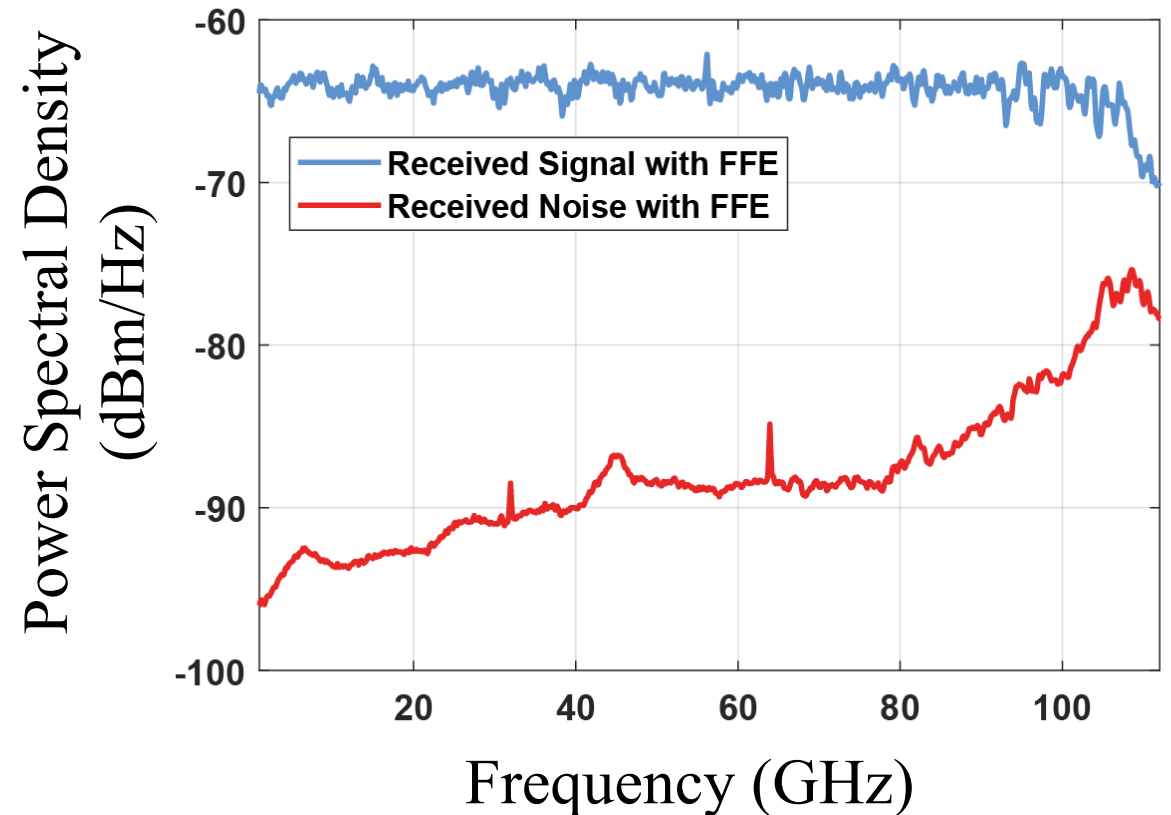
- Bandwidth simulated with a low pass root raised cosine electrical filter and a roll off factor of 0.05; cut-off frequency is 70 to 150 GHz
- Lower baud rates achieve better BER performance at a given system bandwidth
- A lower BER is obtained with increasing bandwidth; eventually saturates due to SNR

Measured Power Spectral Density vs. Frequency

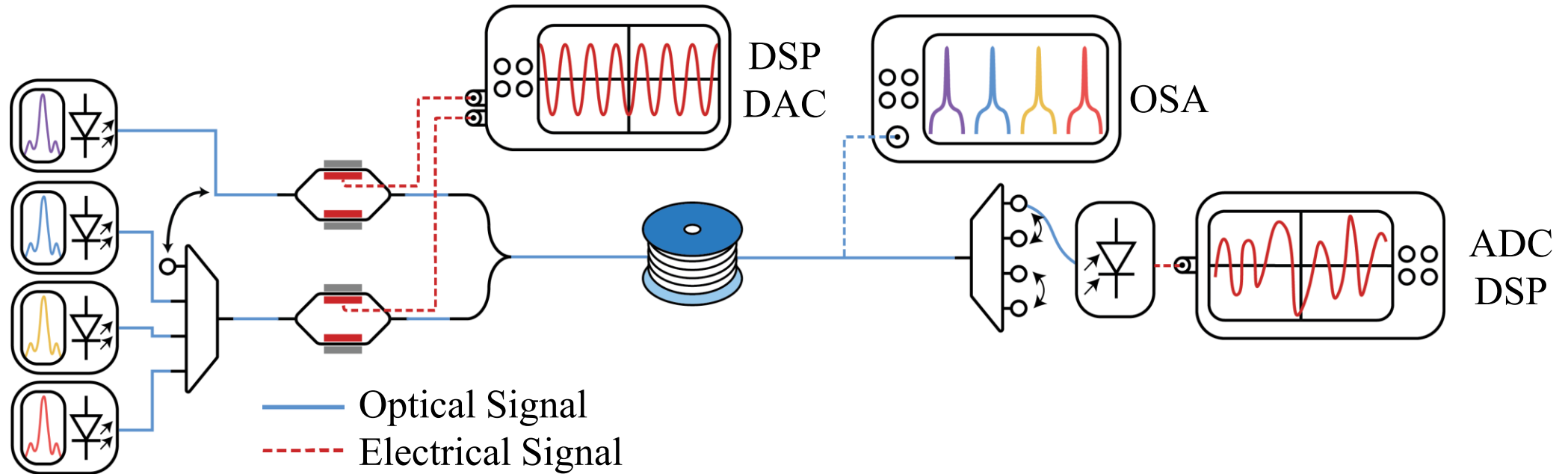
Received RF Spectrum of Signal and Noise
225 GBaud PAM4



Received RF Spectrum of Signal and Noise
after FFE 225 GBaud PAM4

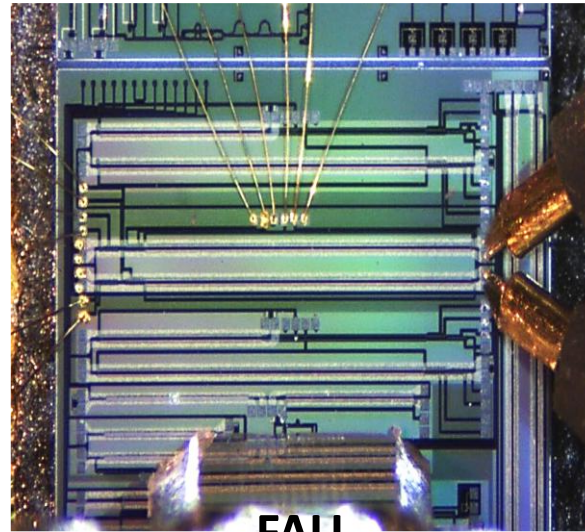
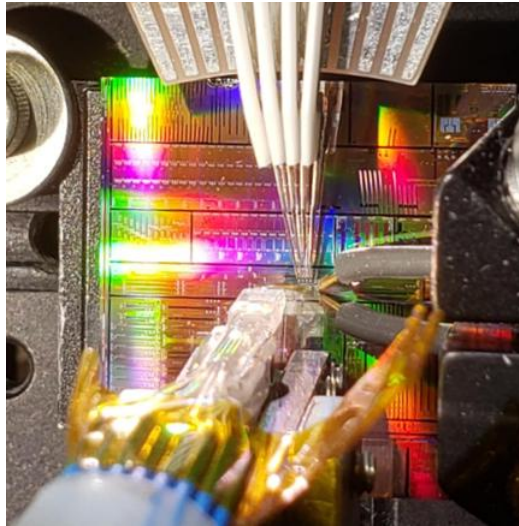


Canonical IM/DD System Setup



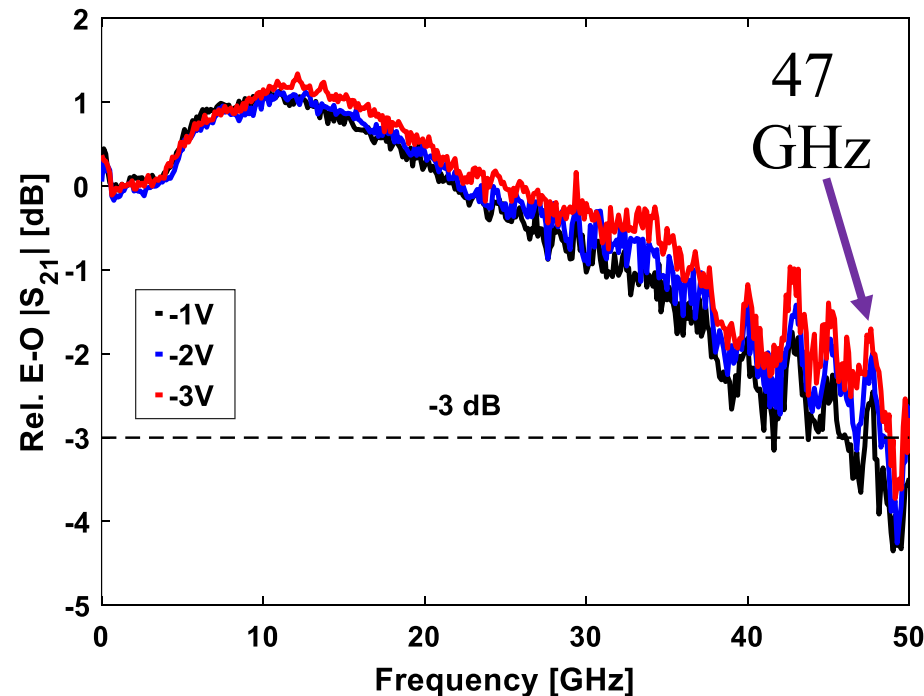
- CWDM grid: 1270 – 1330 nm ($\Delta\lambda = 20$ nm)
- LAN-WDM grid: 1295.56 – 1309.14 nm ($\Delta\lambda = 4.4$ nm)
- Launched powers ≤ 4 dBm (avoid fiber nonlinearities)
- Conventional Mach-Zehnder Modulator structures
- PAM4/PAM8 signaling
- Transmission distances ≤ 10 km (unamplified)
- Linear and Nonlinear Digital Signal Processing (DSP)
- HD-FEC (7%), SD-FEC (20%), SD-FEC (25%)

SiP – Sampling Rate, DSP Variants
Dr. Samiul Alam, Dr. Essam Berikaa
(OFT 2022, PTL 2022)

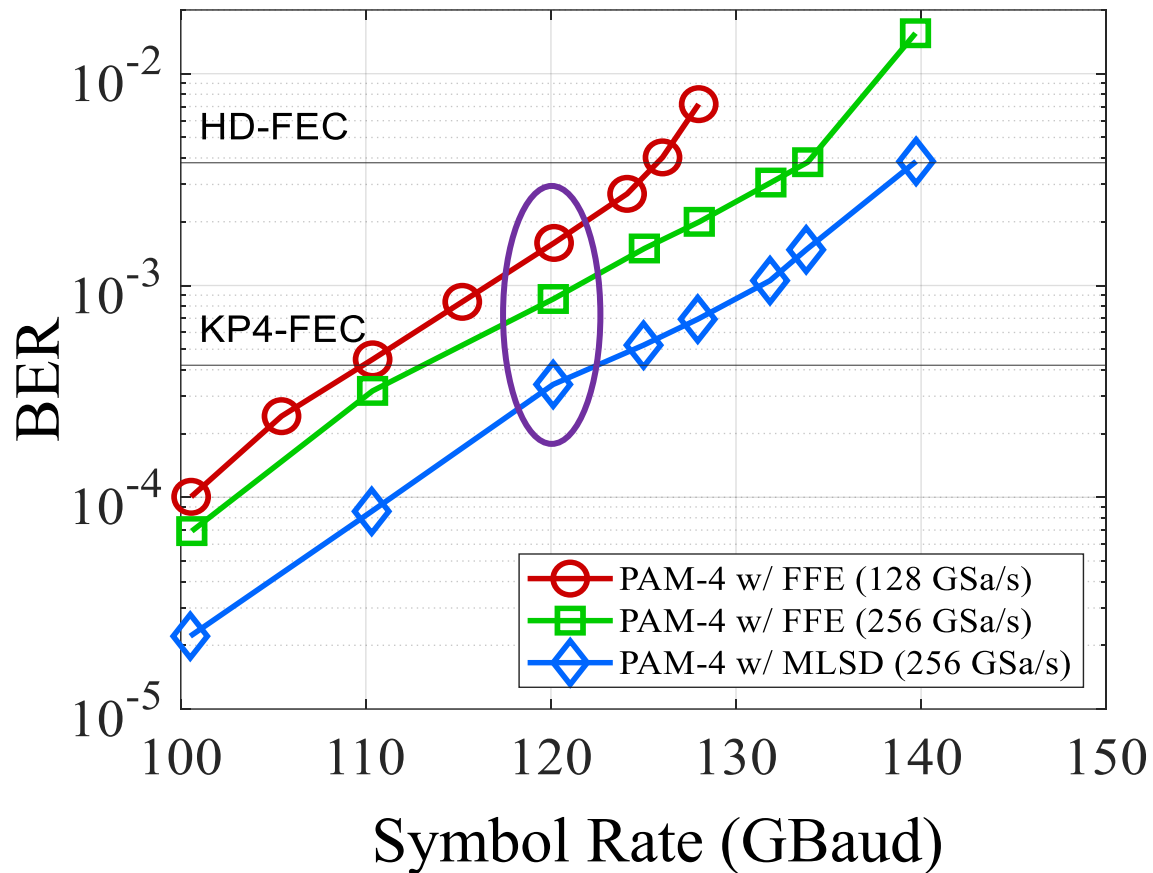


FAU

- Electrode Length: 2.5 mm
- Modulator insertion loss: 5.4 dB
- EO S21 @ 3 dB = 47 GHz
- DC $V\pi = 5.6$ Volts
- Drive voltage: 3 Vpp

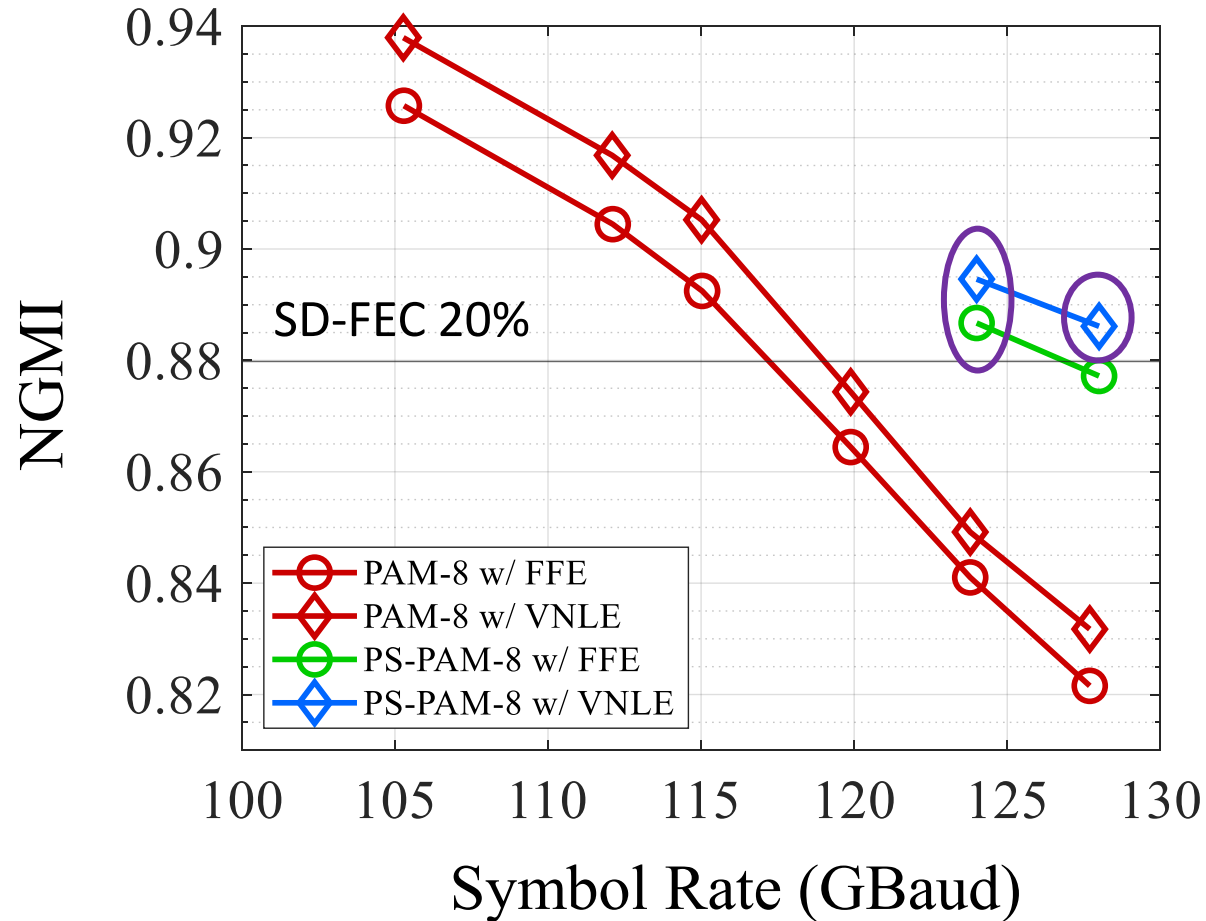


BER vs. Symbol Rate PAM4 @ 1310 nm over 2 km



- Net rates @ 120 GBaud:
 - 225 (R)
 - 225 (G)
 - 228 (B)
- At 256 GSa/s (vs. 128 GSa/s) pulse shaping flexibility increases in order to reduce PAPR
- Feed Forward Equalizer (FFE) compensates for channel induced bandwidth loss and ISI
- Maximum Likelihood Sequence Detection (MLSD) mitigates impairments most effectively to achieve best BER performance

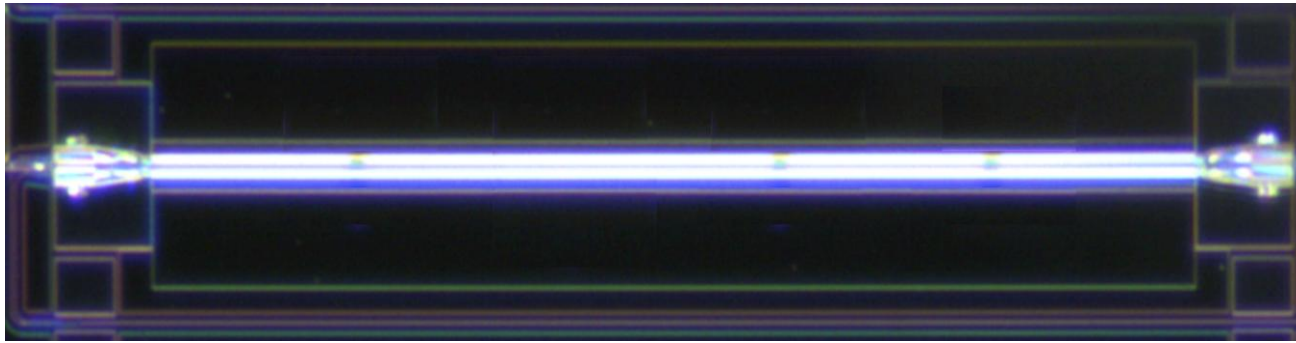
BER vs. Symbol Rate PAM8 @ 1310 nm over 2 km



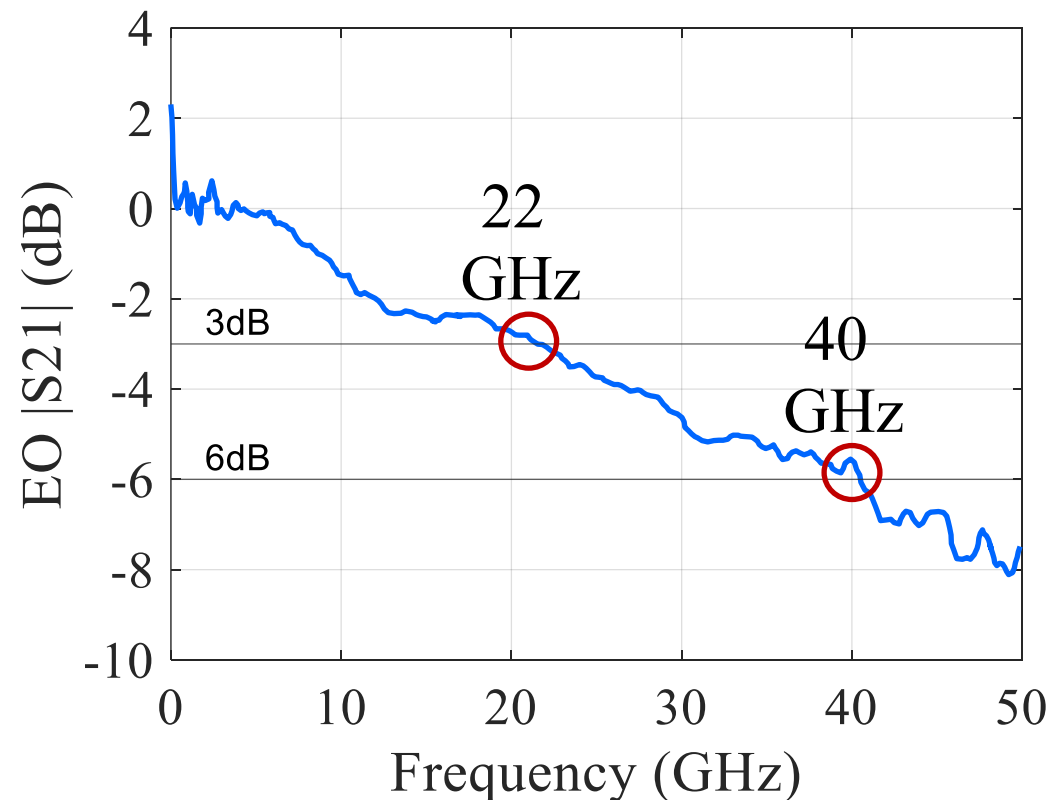
- At 124 GBaud with Probabilistic Shaping (PS) + FFE or Volterra Nonlinear Equalizer (VNLE):
 - 300 Gbps (B)
 - 300 Gbps (G)
- At 128 GBaud with PS and VNLE:
 - 310 Gbps (B)
- Several configurations possible to achieve net 300 Gbps below 20% SD-FEC

BTO – DSP Variants, λ Performance
Dr. Weijia Li
(ECOC 2023, JLT 2024)

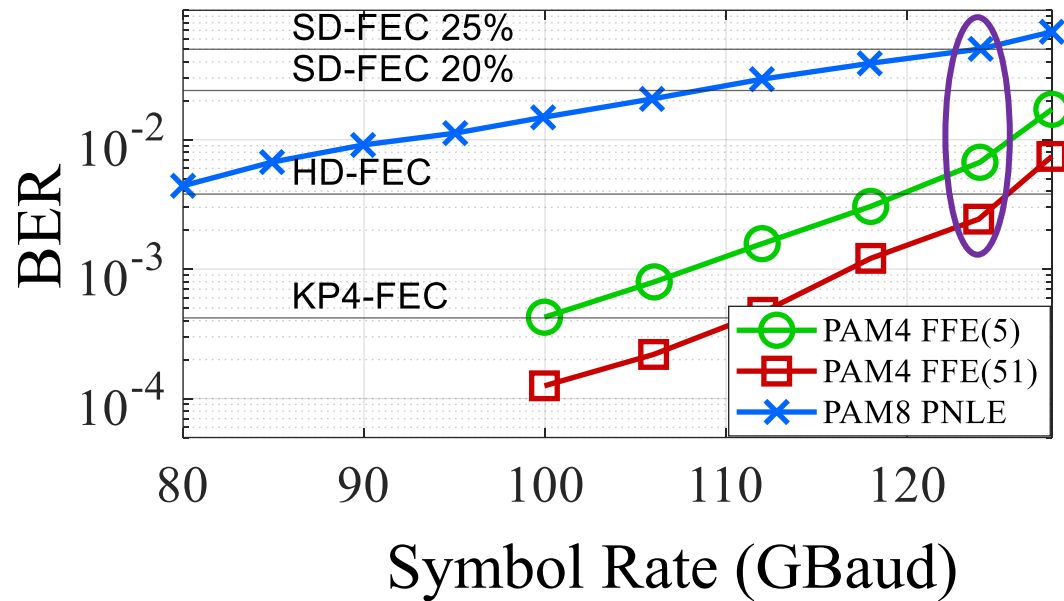
Lumiphase Barium Titanate Oxide (BTO) MZM



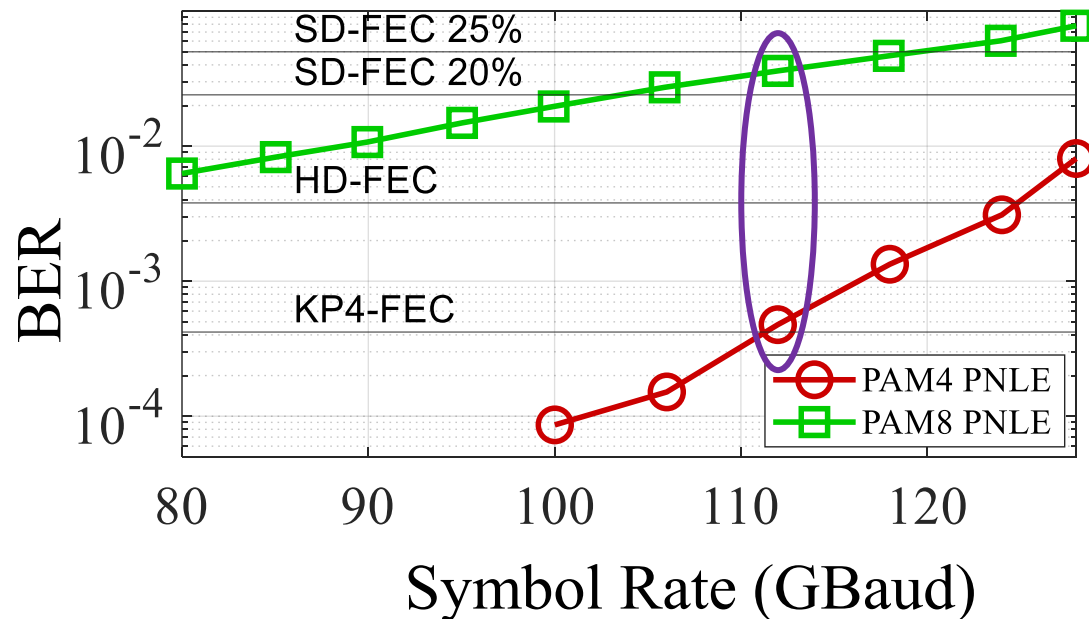
- Electrode Length: 1.5 mm
- On-chip insertion loss: ~ 2 dB
- EO S21 = 22/40 GHz @ 3/6 dB
- RF V_{π} @ 10 MHz = 3.6 V
- Drive voltages: 2 – 4 V_{pp}



BER vs. Symbol Rate @ 1310 nm

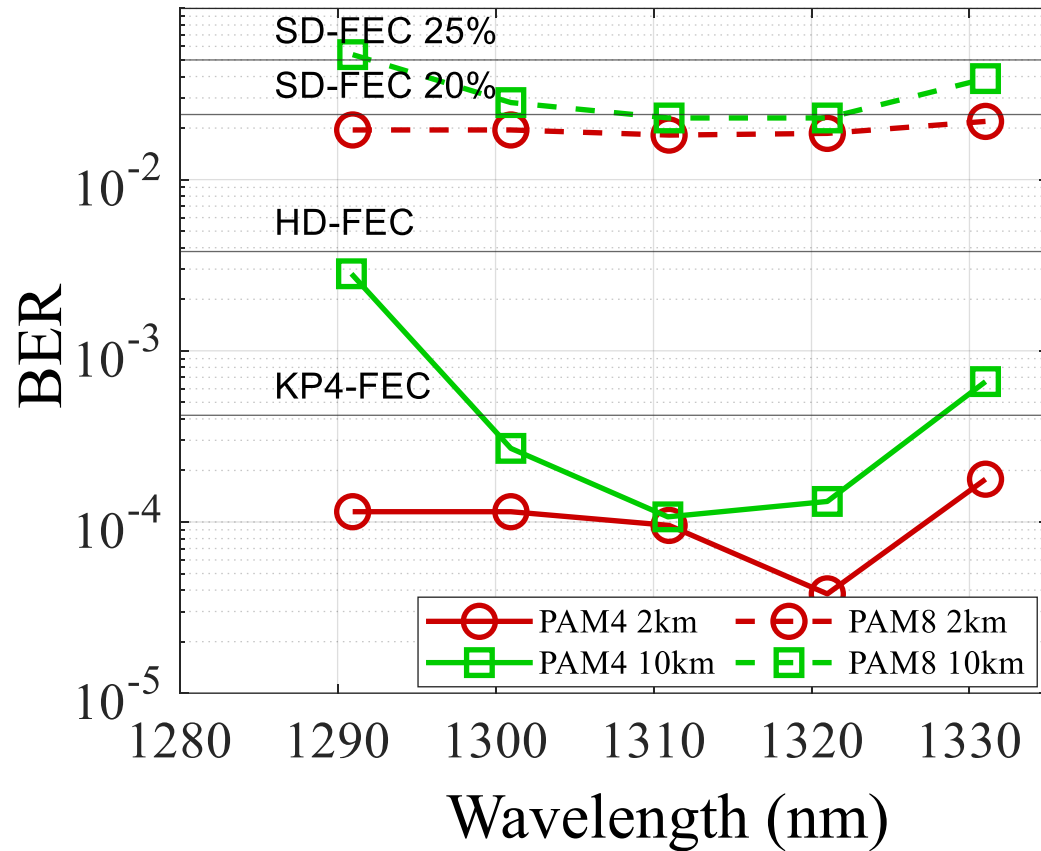


- Net rates @ 124 GBaud over 2 km:
 - 232 (R)
 - 207 (G)
 - 298 (B)
- FFE with more taps reduces BER
- Polynomial Nonlinear Equalizer (PNLE) with PAM8 increases capacity but requires stronger FEC



- Net rates @ 112 GBaud over 10 km:
 - 210 (R)
 - 269 (G)
- Here for 10 km, capacity governed by PAM order

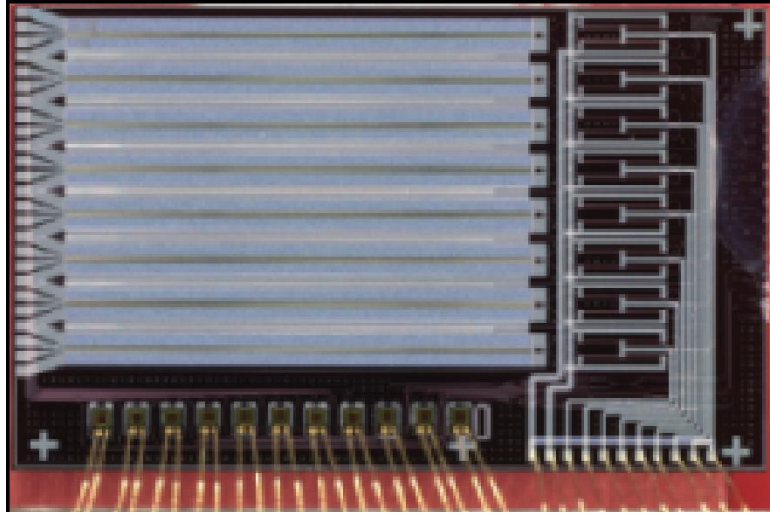
BER vs. Multi λ Transmission @ 106 Gbaud over 2/10 km



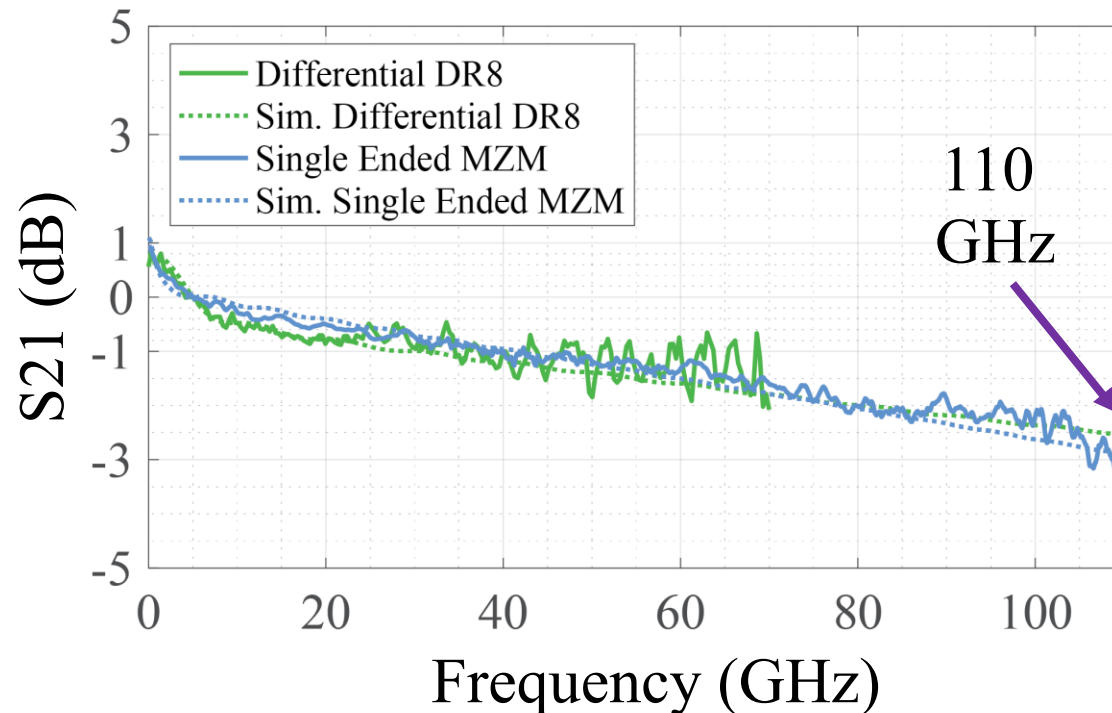
- Solid Red: PAM4 Below KP4-FEC over 2 km:
 - 201 Gbps per λ ;
- Solid Green: PAM4 Below HD-FEC over 10 km:
 - 199 Gbps per λ
- Dotted Red PAM8 Below SD-FEC 20% over 2 km:
 - 265 Gbps per λ
- Solid Green: The band edge λ 's experience increased dispersion penalties

TFLN – λ Performance, High Bauds
Mr. Charles St. Arnault
(OFC 2024 PDP, JLT 2025)

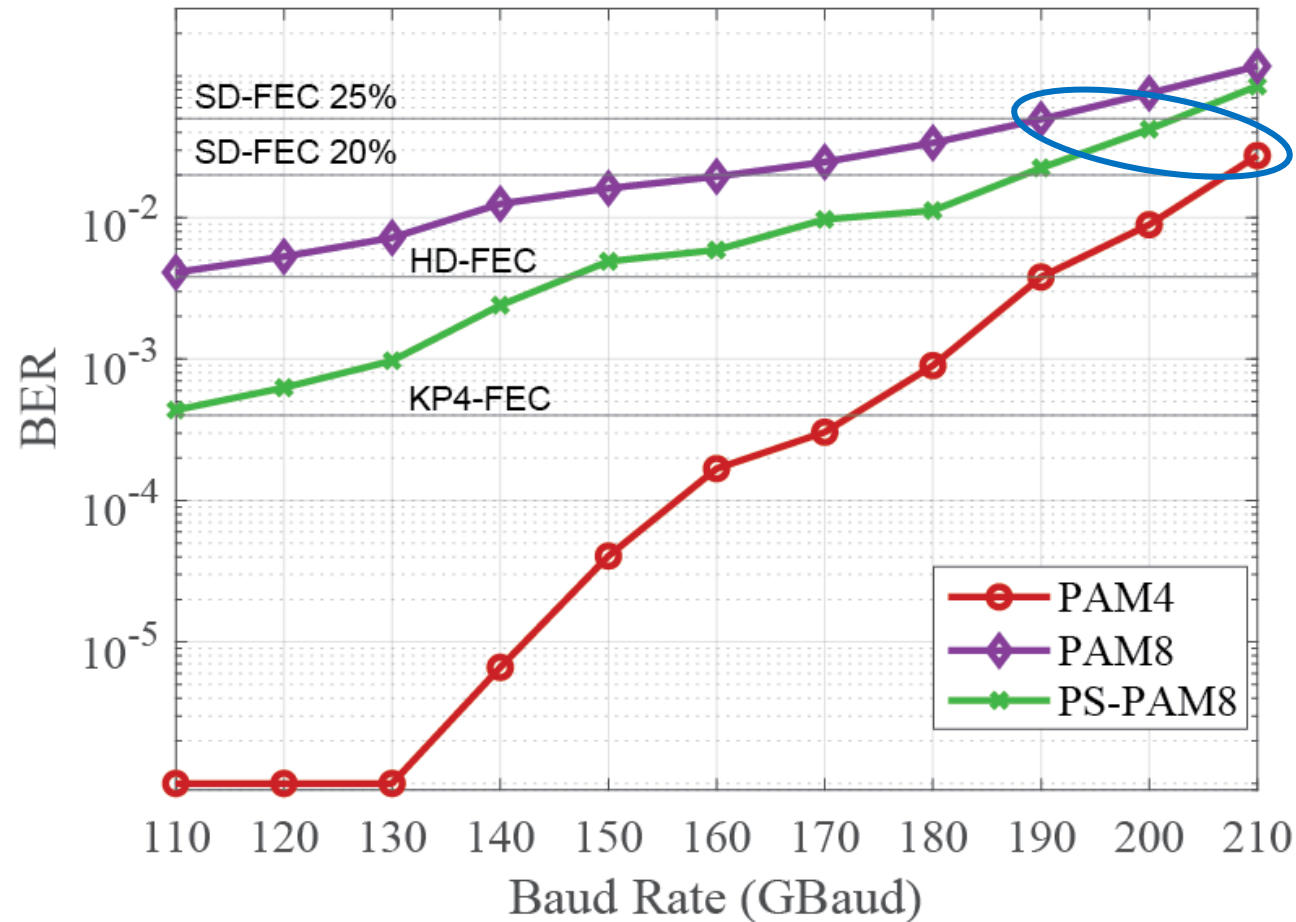
Hyperlight Thin Film Lithium Niobate (TFLN) MZM



- Electrode Length: 10 mm
- On-chip insertion loss:
 < 0.1 dB/cm (almost lossless)
- EO S21 3 dB > 110 GHz
- RF $V_{\pi} = 1.5$ V low MHz
- Drive voltages: < 1 V_{pp} @ 2 km;
2 V_{pp} @ 10 km



BER vs. Symbol Rate @ 1310 nm over 10 km

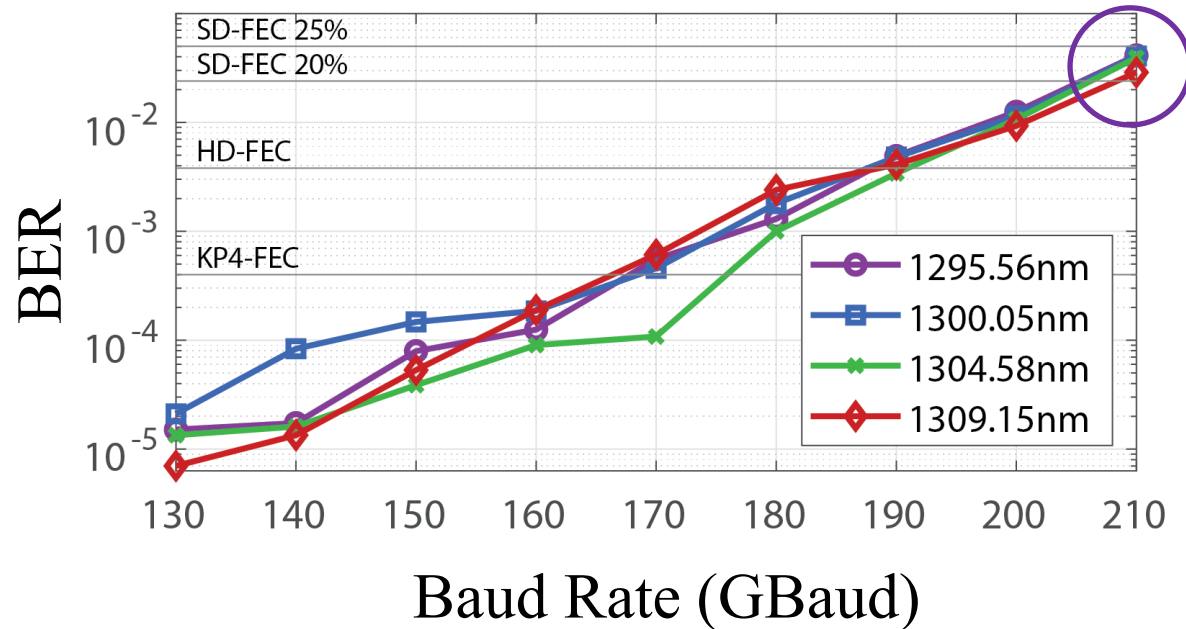


- Net rates:
 - 336 Gbps @ 210 GBaud PAM4 (R)
 - 443 Gbps @ 200 GBaud Probabilistically Shaped-PAM8 (G)
 - 456 Gbps @ 190 GBaud PAM8 (P)
- Increases capacity by with increasing PAM order and employing polynomial nonlinear equalizers to mitigate linear and nonlinear impairments

BER vs. Symbol Rate vs. λ @ PAM4

Net 1.33 Tbps:
4 x 336 Gbps/ λ
210 GBaud

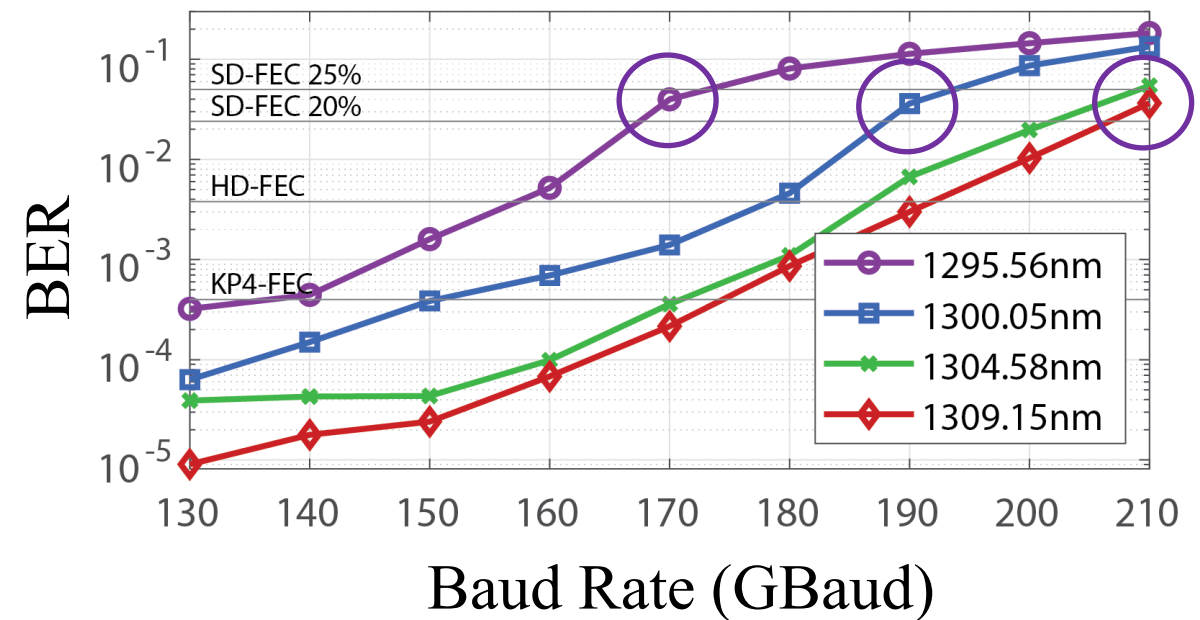
PAM4 | 2 km



Net 1.25 Tbps:

272 Gbps @ 1295 nm @ 170 GBaud
304 Gbps @ 1300 nm @ 190 GBaud
336 Gbps/ λ for 2 λ s @ 210 GBaud

PAM4 | 10 km

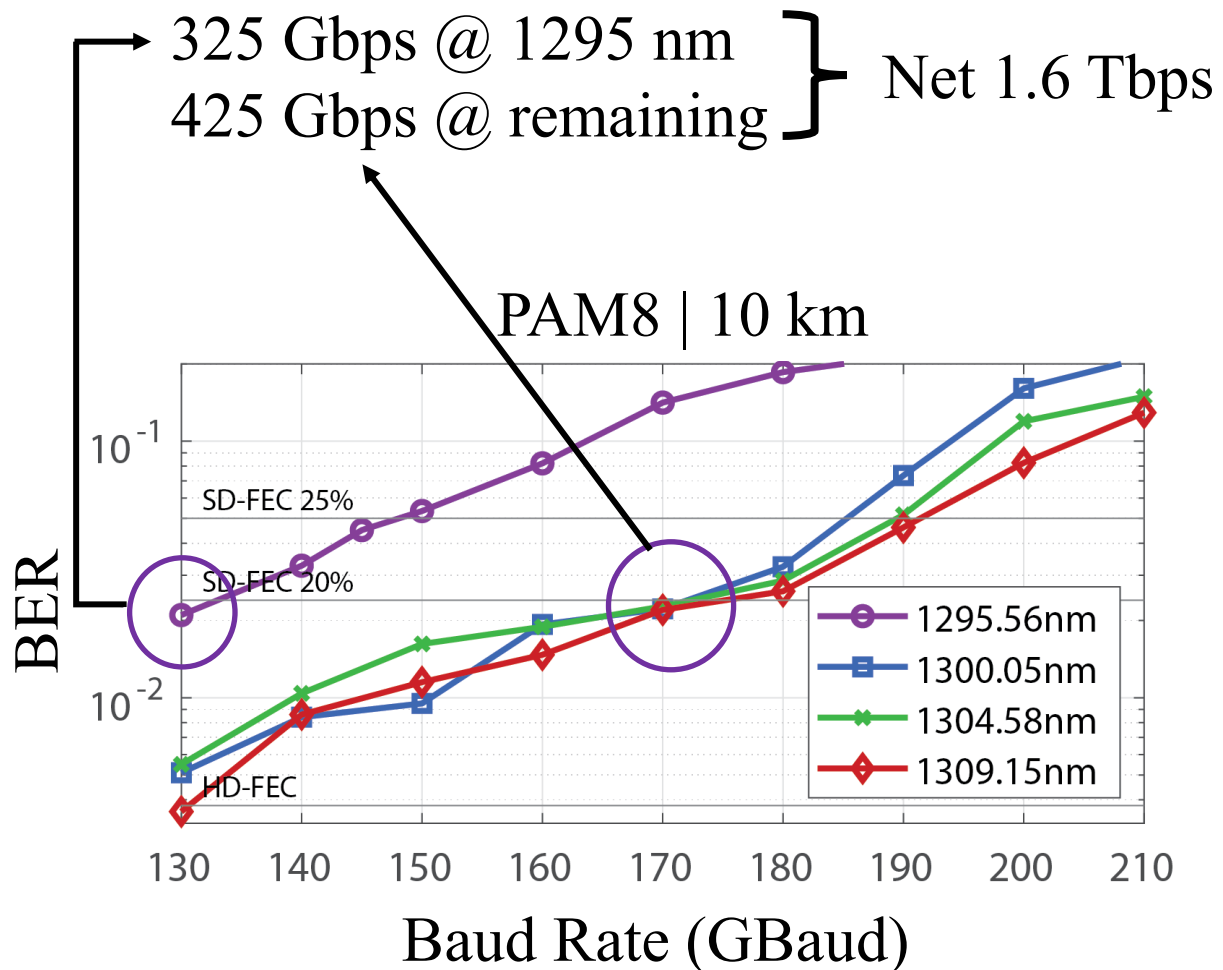
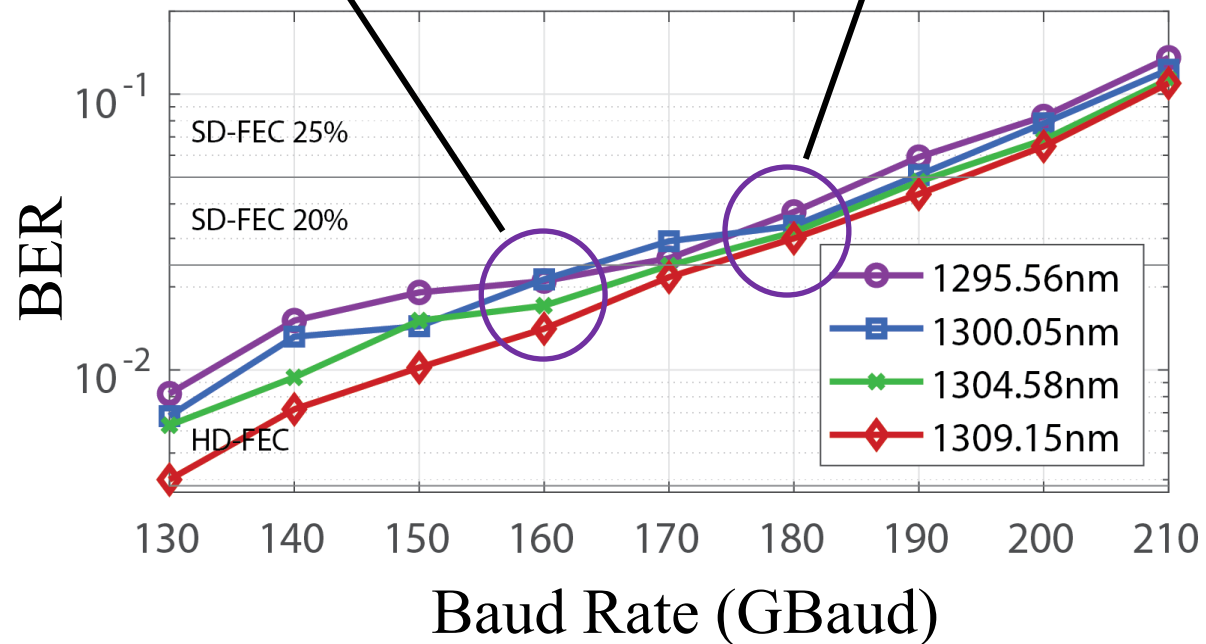


BER vs. Symbol Rate vs. λ @ PAM8

Net 1.6T: 4 x 400G
160 GBaud

Net 1.72T: 4 x 432G
180 GBaud

PAM8 | 2 km



References



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- [12] C. St-Arnault et al., "Net 1.6 Tbps (4 $\times$ 400Gbps/ λ) O-Band IM/DD Transmission Over 2 km Using Uncooled DFB Lasers on the LAN-WDM grid and Sub-1V Drive TFLN Modulators," OFC 2024, PDP, pp. 1-3.
- [13] C. St-Arnault et al., "Net 3.2 Tbps 225 GBaud PAM4 O-Band IM/DD 2 km Transmission Using FR8 and DR8 with a CMOS 3 nm SerDes and TFLN Modulators," OFC 2025, PDP, pp. 1-3.