AXONAL NETWORKS

# Digital Photonics for High-Radix Switches in AI Data Centers

# Outline

Motivation and background

paraDOX™: A scalable switch architecture

Re-Thinking Computing

Digital Photonics

2 x 2 Switch Gen. 1
Digital Photonics

2 x 2 Switch Gen. 2
Digital Photonics

Towards higher radix switches
Digital Photonics

## Key takeaways

- We discussed why AI networking is becoming one of the primary bottlenecks in the continued scaling of AI infrastructure.
- paraDOX™ enables scalable, high-radix switching for AI data centers.
- Digital Photonics offers a promising path toward low-power, scalable paraDOX™ implementations.
- I presented the most compact silicon photonic logic gate based on microring modulators, as a building block for a 16×16 Banyan subswitch for paraDOX™ 256×256.

# Motivation and background

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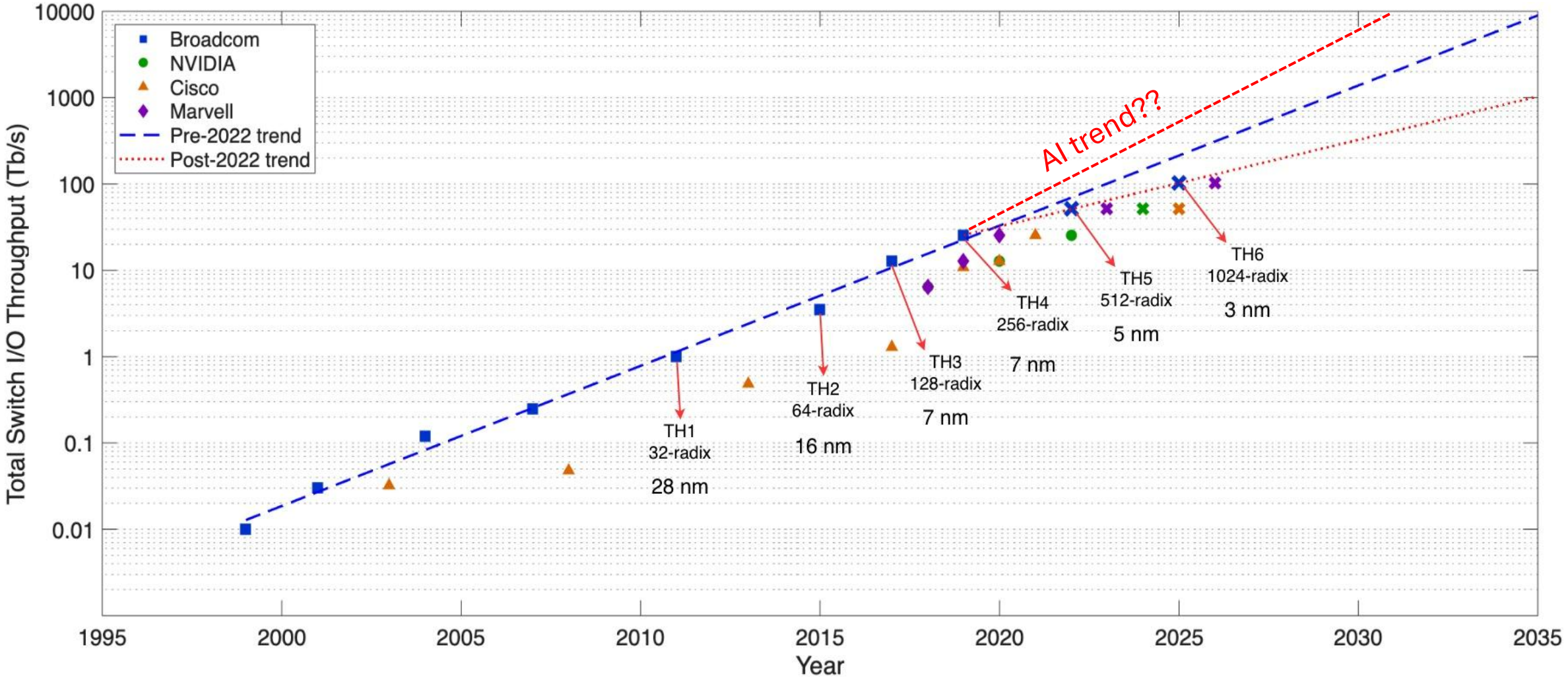
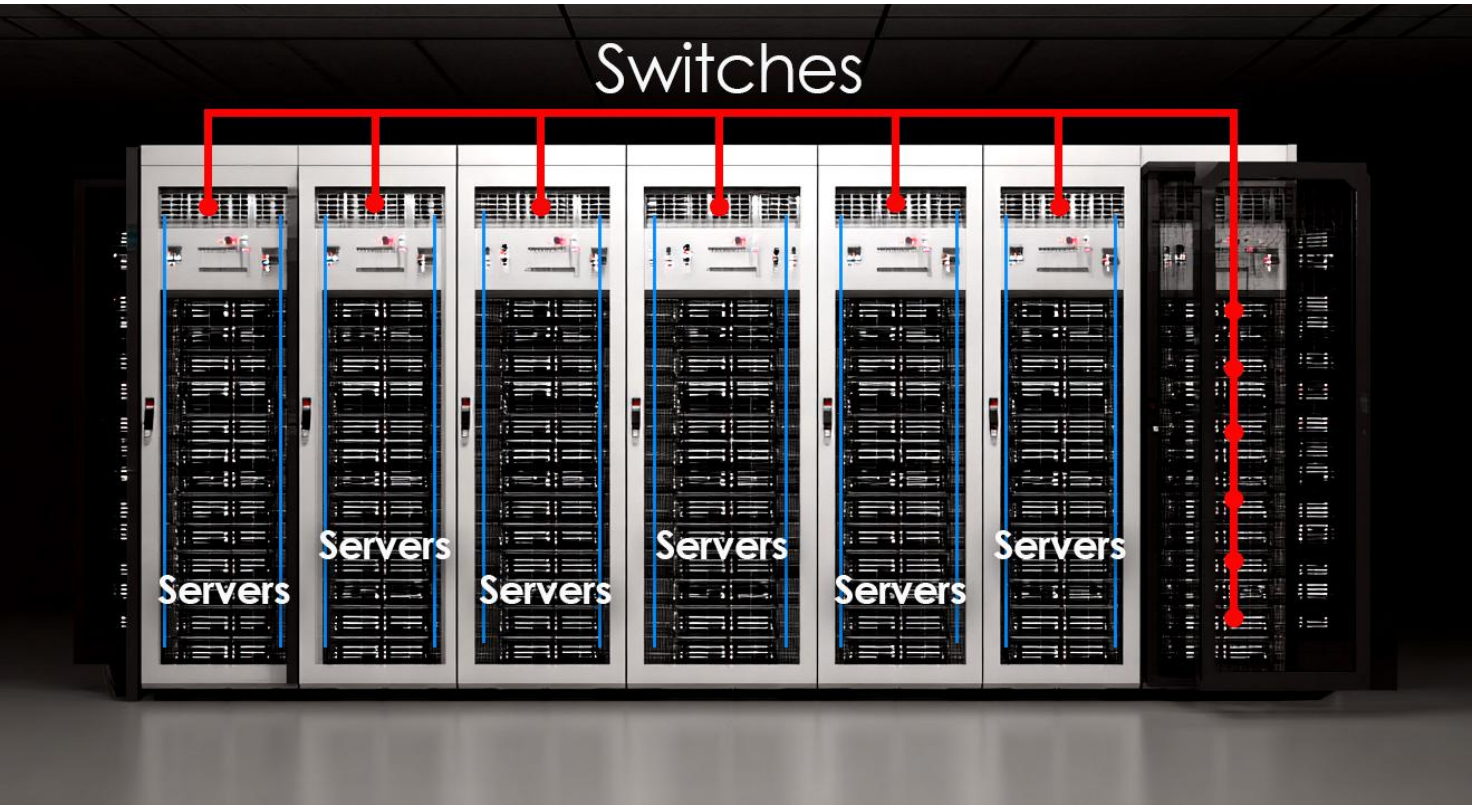
# Evolution of AI cluster scale

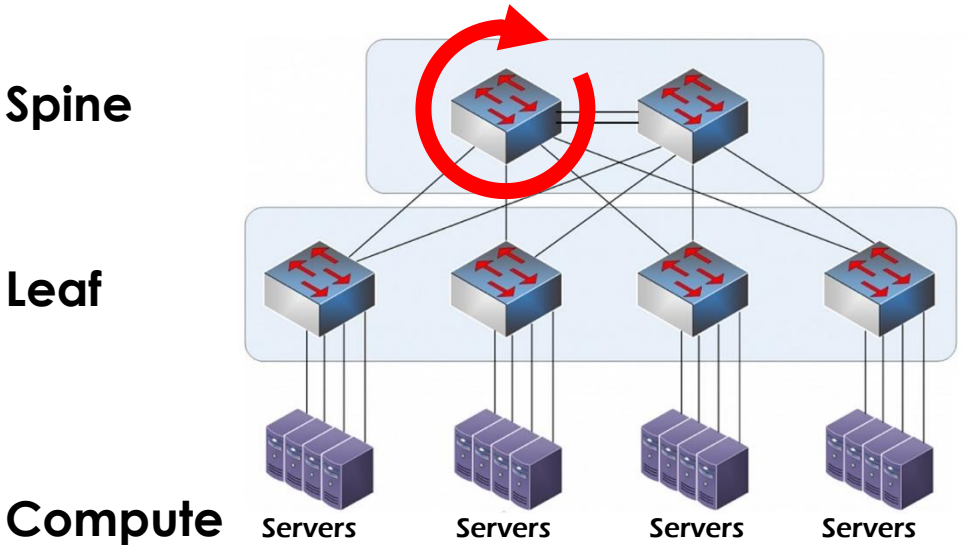



Next 5-7 years… We will need over 10,000-Tbps

# Network Architectures




Data centers typically use **high-radix switches** to move data.

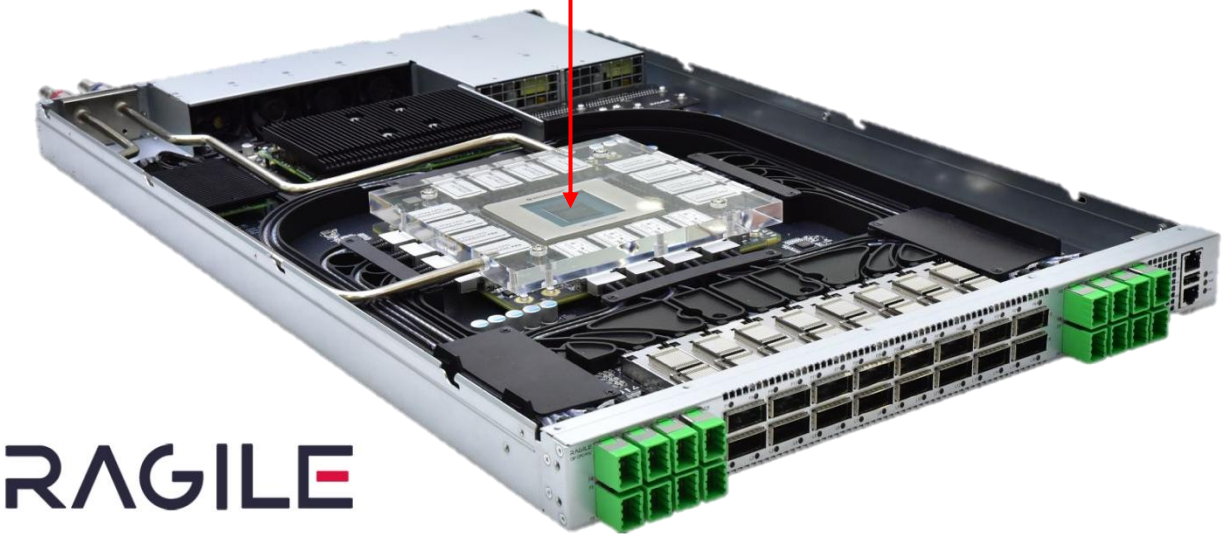


# High Radix Switches

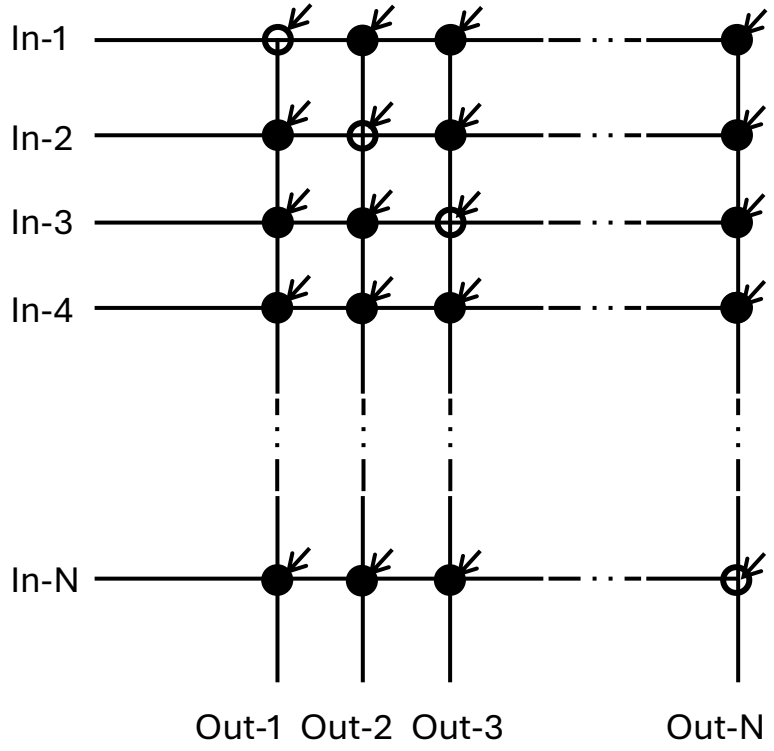
- Use 256 channels at 200GbE. to move 51.2-Tbps total aggregate bandwidth

BROADCOM® intel

- The Broadcom® BCM78900 chip connected to Intel CPO's and pluggable OSFPs



RAGILE




Assuming linear scaling

>1 Trillion for 4,096 x 4,096

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# paraDOX™: A scalable switch architecture

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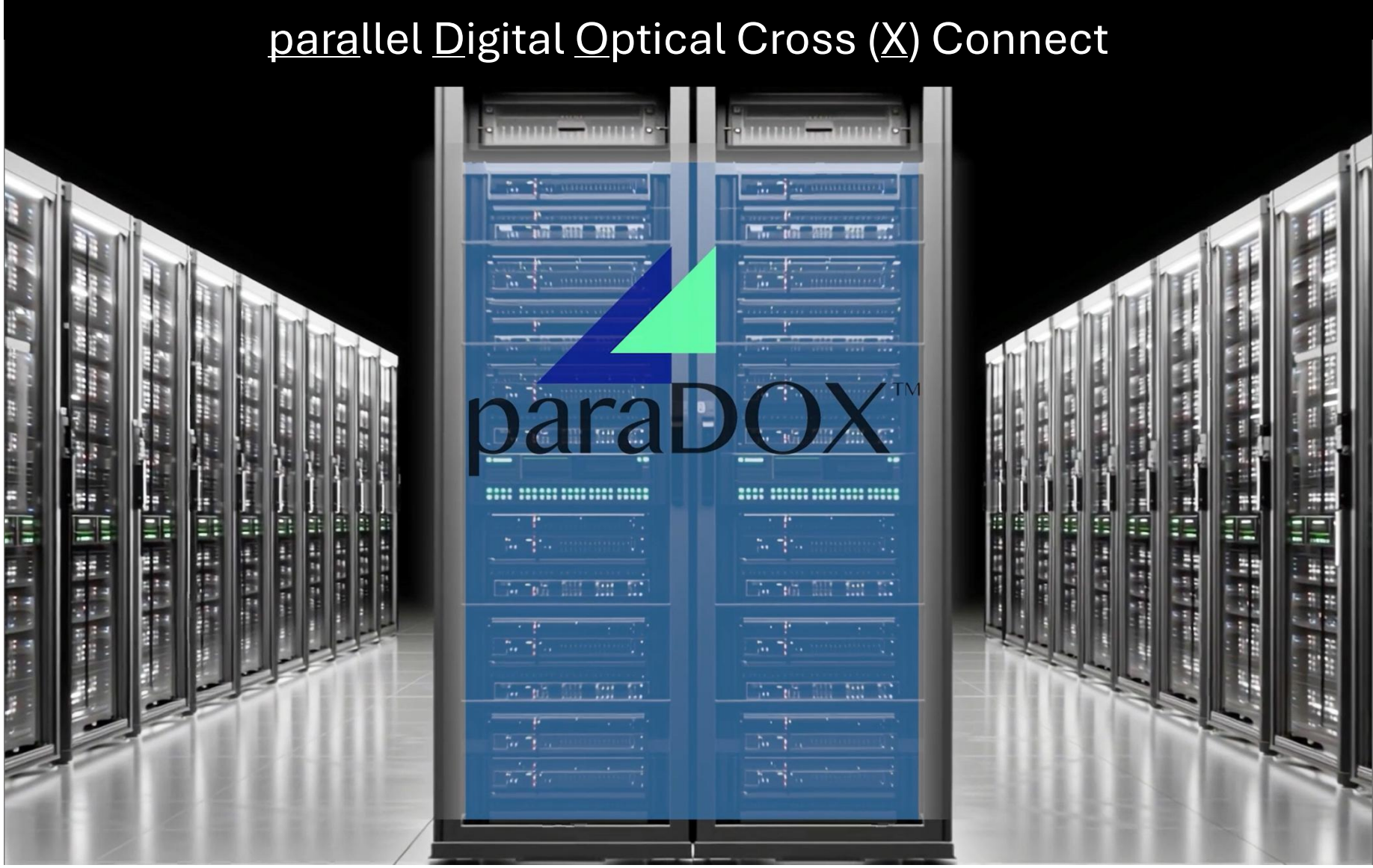
paraDOX™

parallel Digital Optical Cross (X) Connect



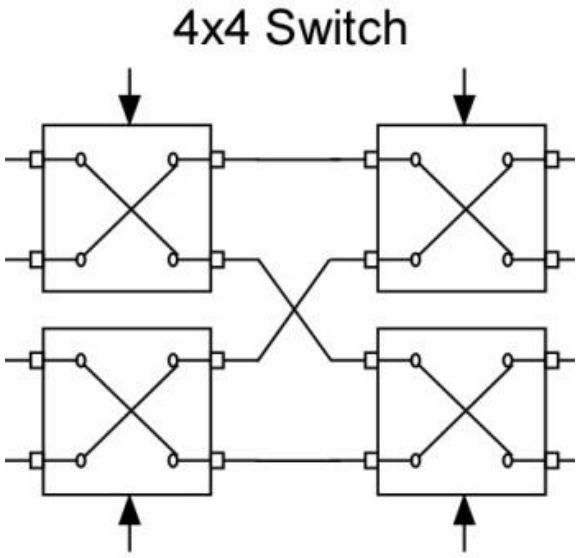

**4,096 x 4,096**
**16,384 x 16,384**
**:**
**Radix**

PATENTED

A **NEW** Packet Switching **Architecture**

# Hybrid Idea

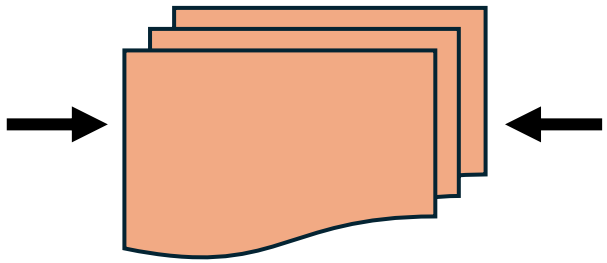
- Based on a Statistical Observation of performance…



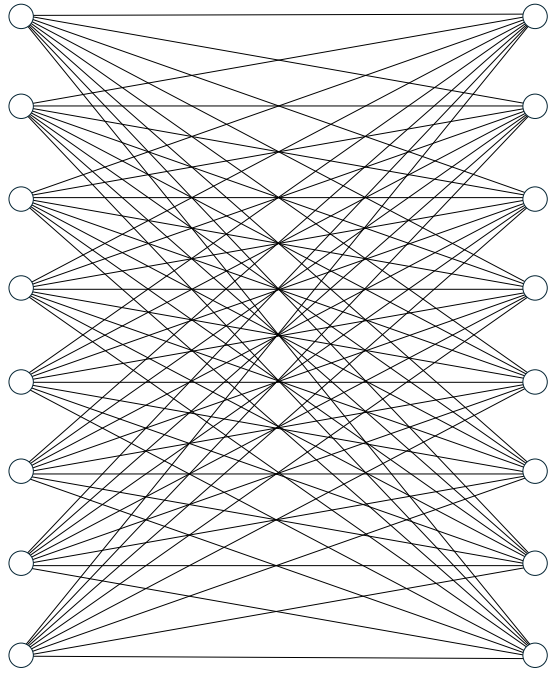

$$P_b = 1 - \prod_{i=1}^{s} \left(1 - \frac{a}{2^i}\right)$$

Banyans

| Banyan size | Saturation at load (from simulations) |
|---|---|
| 4×4 | $a = 0.44$ |
| 8×8 | $a = 0.37$ |
| 16×16 | $a = 0.28$ |



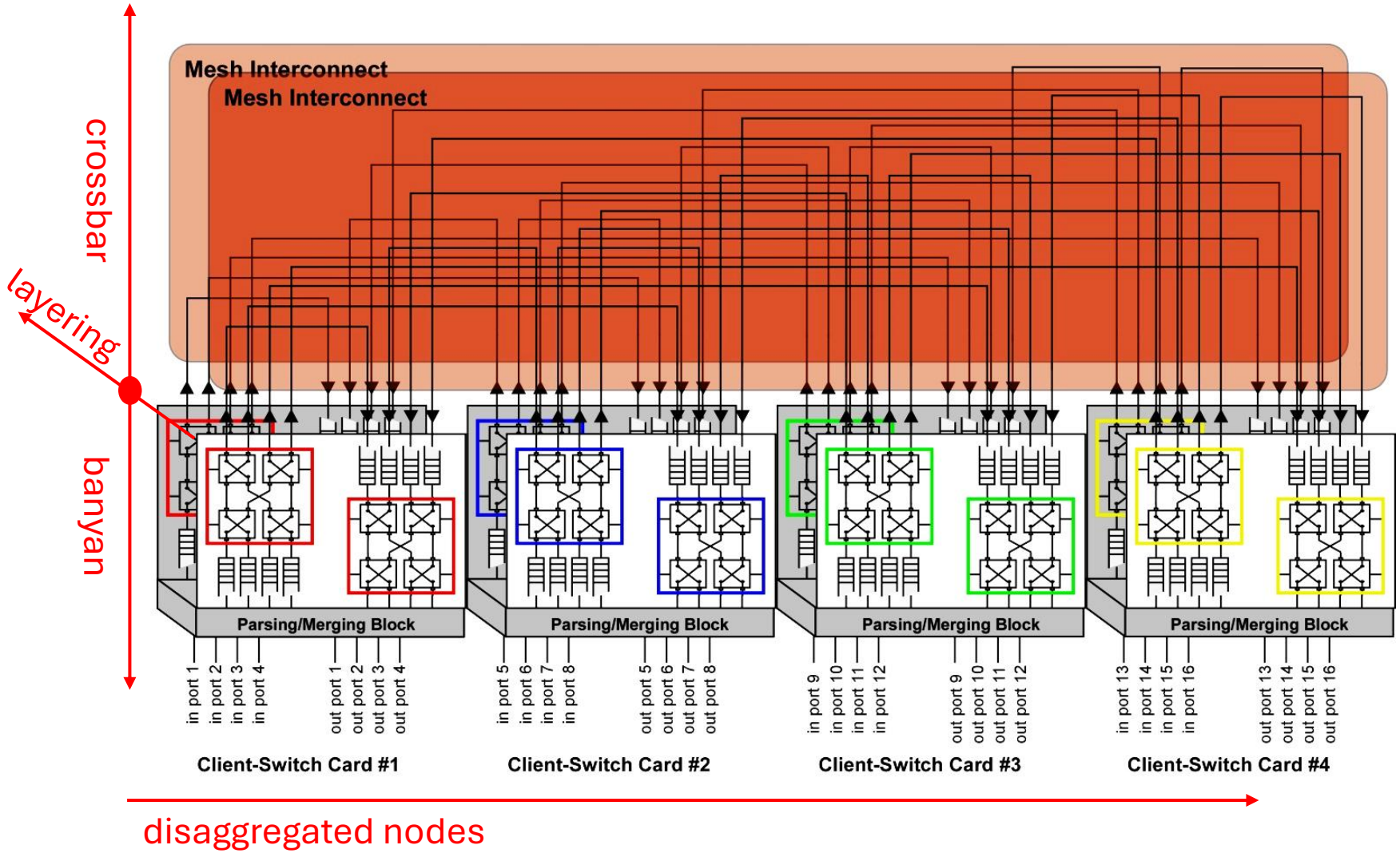
Spatial Division Multiplexing



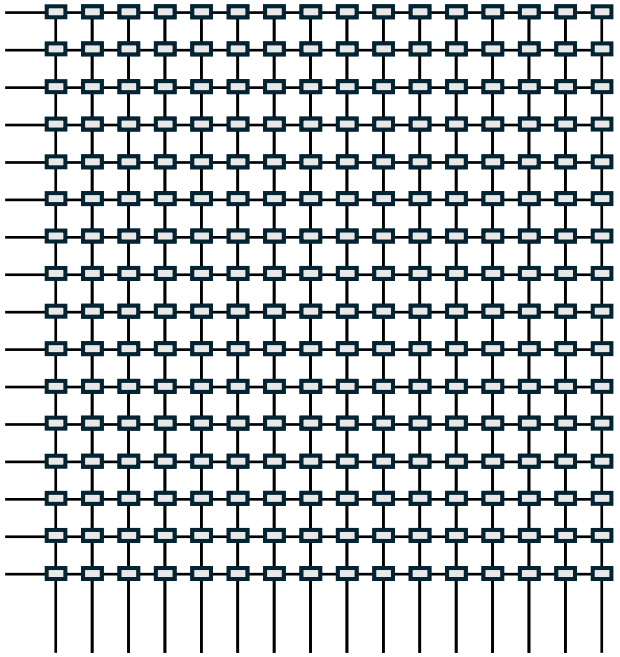
Fiber mesh

# Building paraDOX™: A 16x16 Switch

- paraDOX™ combines the best of crossbar and banyan switches
- By adding Spatial-Division-Multiplexing (SDM)in layers
- And disaggregated nodes.

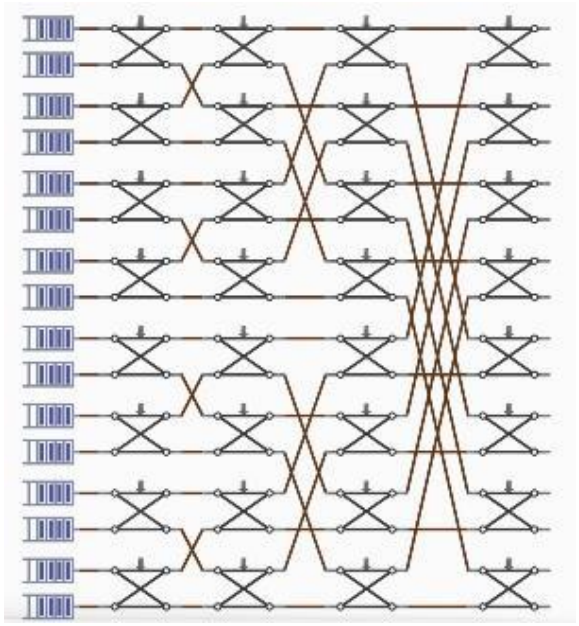


# Architecture Comparison



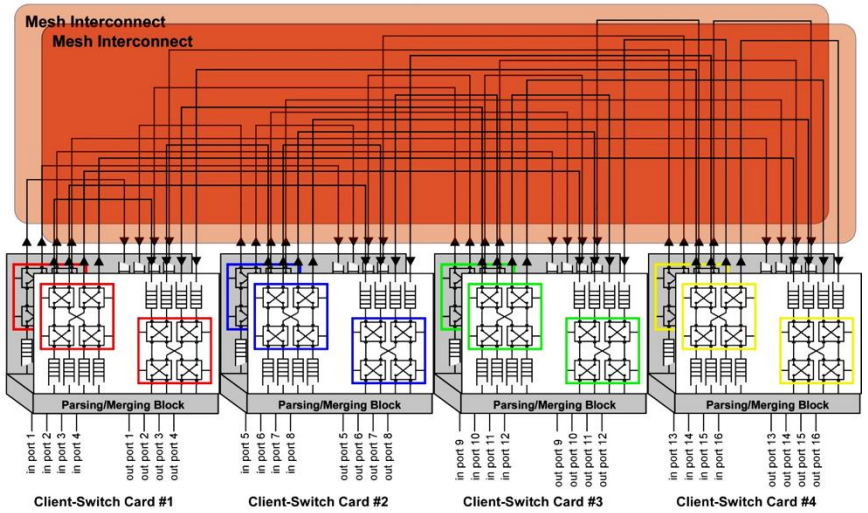
CROSSBAR

(e.g.: Broadcom Tomahawks)



BANYAN

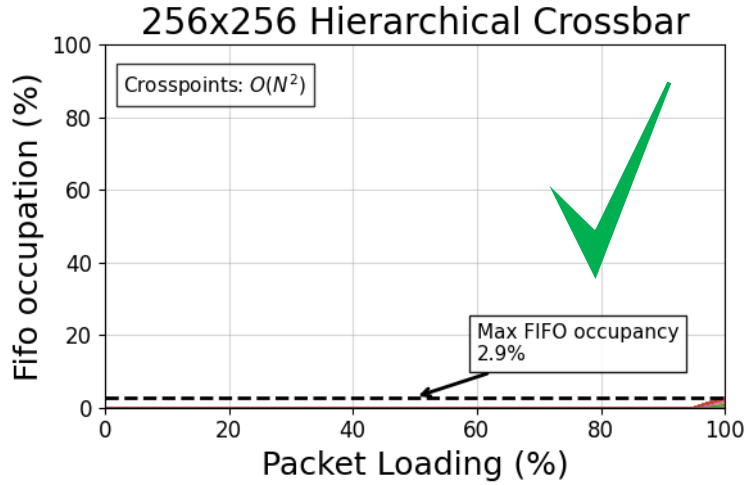
(60's – 70's Telephony Networks)

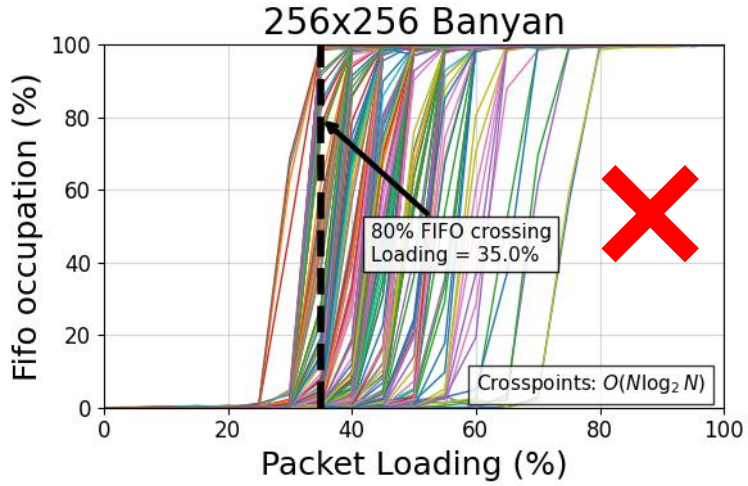


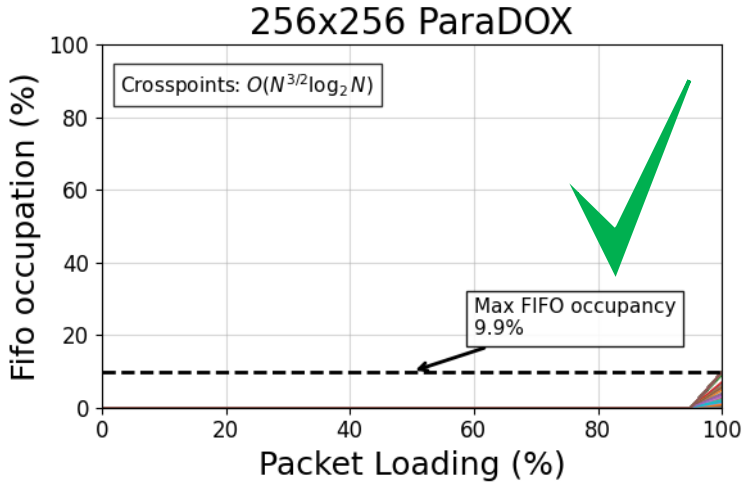

paraDOX

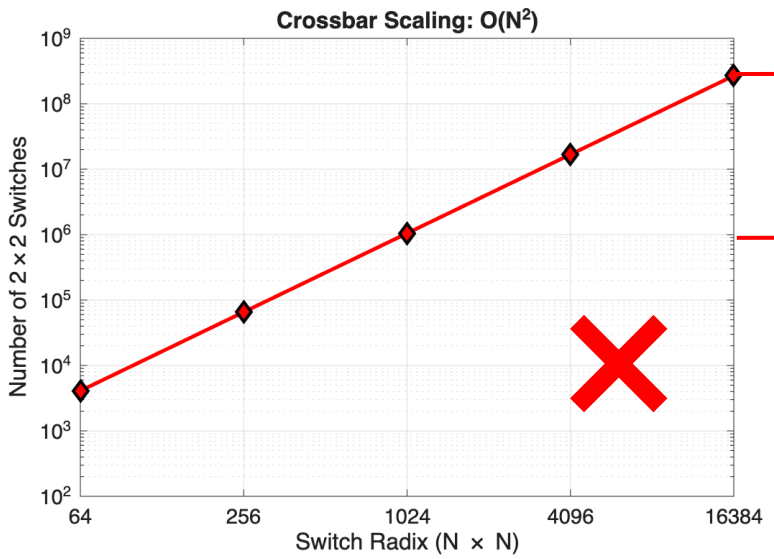
( Efficient Hybrid )

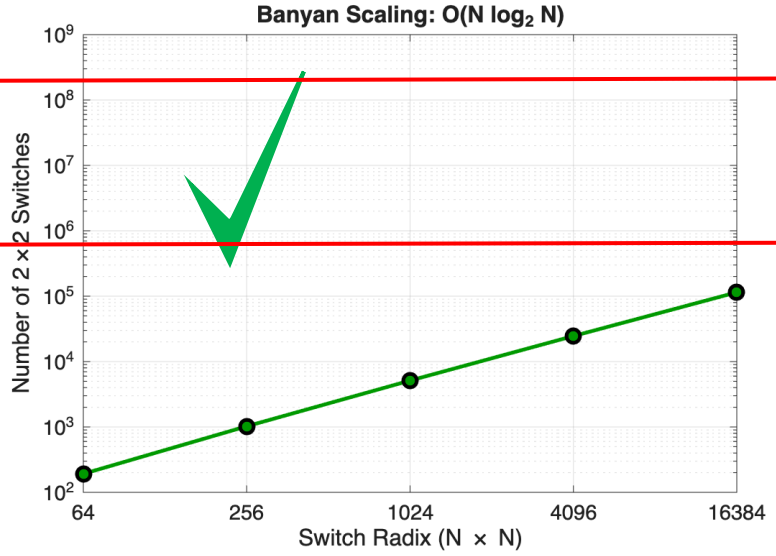
# Contention Performance and Scaling

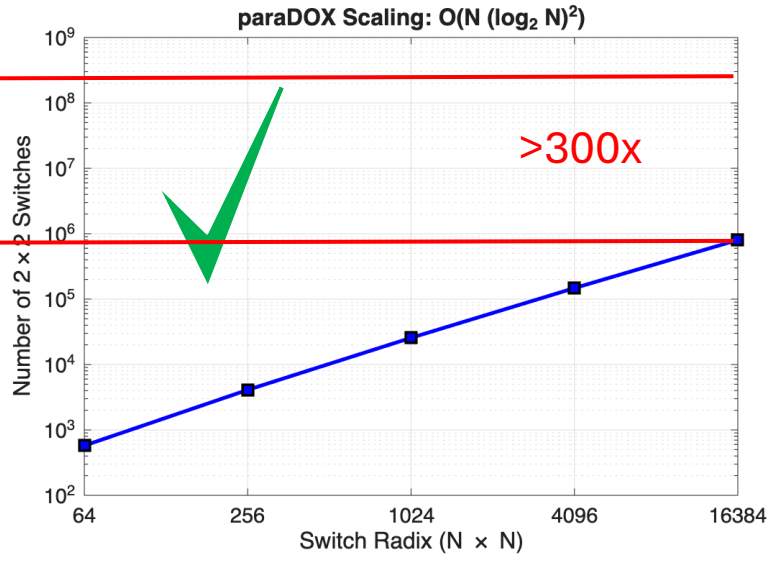


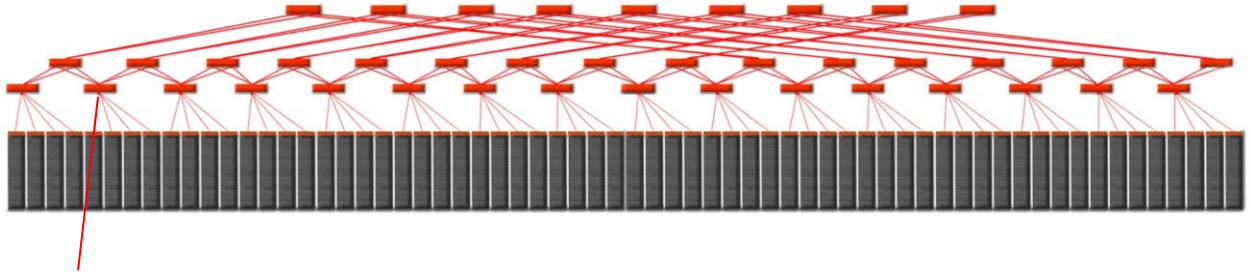



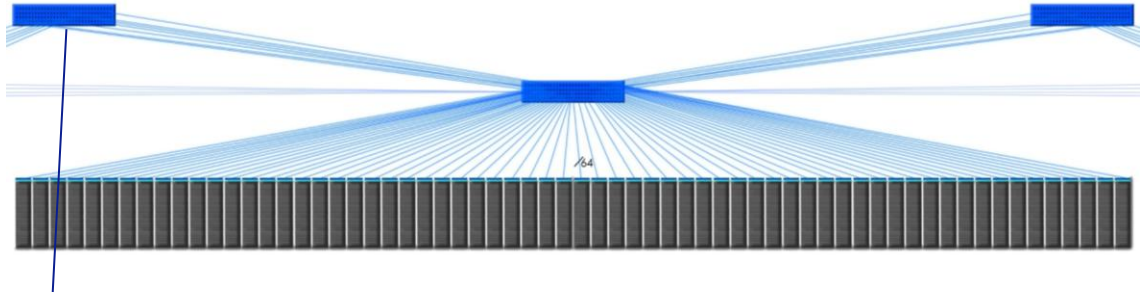



# Scale-out: Power Comparison



**256-radix switches in a leaf-spine architecture**
Result in high latency, high power and increased complexity.



**4096-radix paradox switch in a leaf-spine architecture**
Reduces the number of switches by an order of magnitude.

| | | | Tomahawk 5 - 256 | |
|---|---|---|---|---|
| AMD MI400 Server | GPUs | QSFPs (for GPU) | Switches | OSFPs (for Switch) |
| 512 | 4096 | 1024 | 16 | 512 |
| 4096 | 32768 | 8192 | 128 | 4096 |
| 40960 | 327680 | 81920 | 1280 | 40960 |
| 409600 | 3276800 | 819200 | 12800 | 409600 |
| | | | | |
| | | | paraDOX-4096 | |
| 512 | 4096 | 1024 | 1 | 0 |
| 4096 | 32768 | 8192 | 8 | 0 |
| 40960 | 327680 | 81920 | 80 | 0 |
| 409600 | 3276800 | 819200 | 800 | 0 |

AMD AI NIC Pollara 400 Adapter Cable Guide Cable Guide
DAC and AOC Cable Configurations for AI NIC • AMD AI NIC Pollara 400 Adapter Cable Guide Cable Guide (XAPP1404) • Reader • AMD Technical Information Portal

Switch Chips : 12,800 x 500W = 6.4 MW
Transceivers (OSFP) : 409,600 x 30 W = 12.3 MW
TOTAL : 18.7 MW

Switch Chips : 800 x 2000W* = 1.6 MW
Transceivers (OSFP) : 0 MW
TOTAL : 1.6 MW

**90 % Reduction in Network Power**

*** Early Estimate for Digital Photonics**

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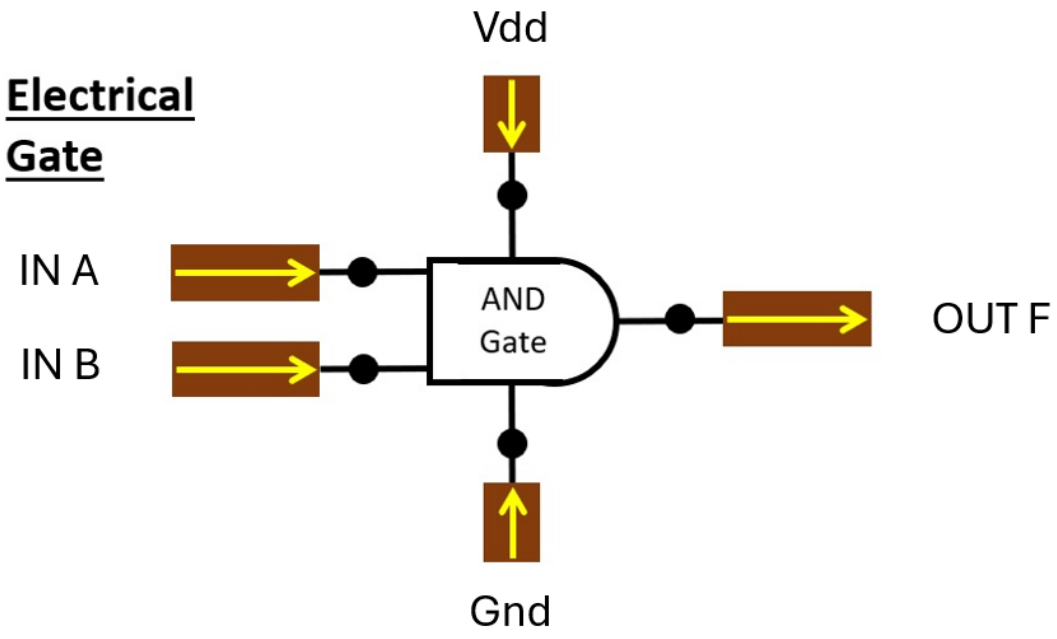
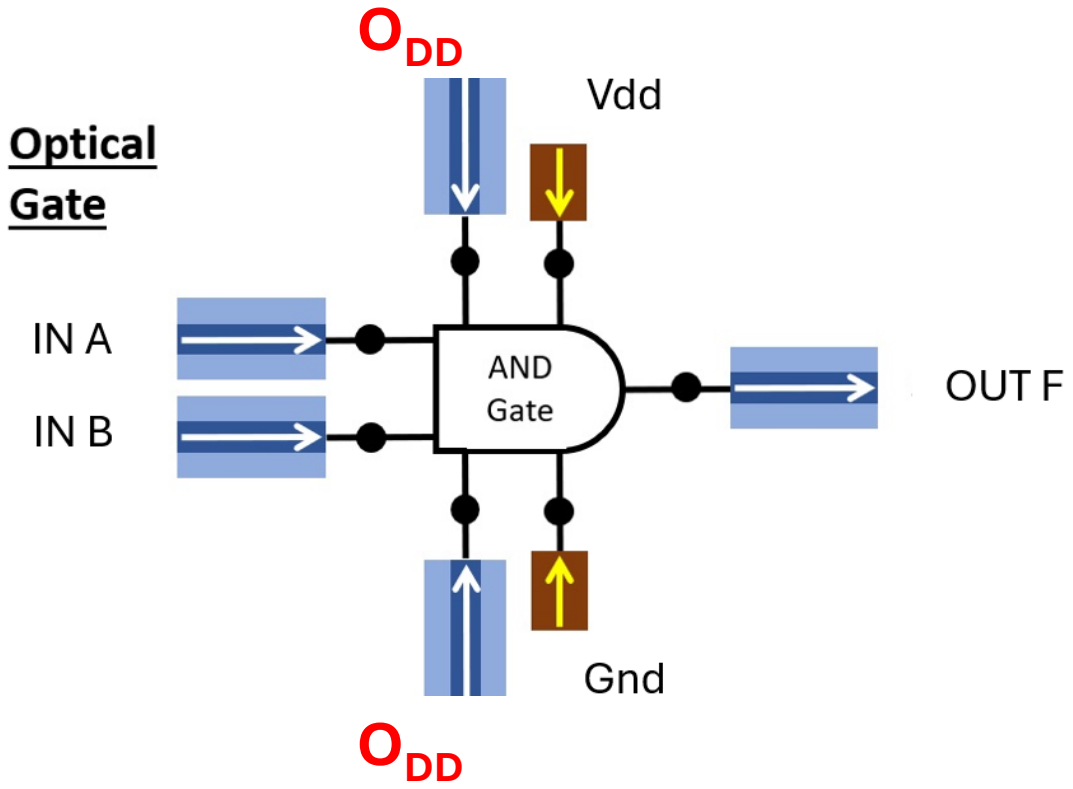
# Re-Thinking Computing

## Digital Photonics

# Digital Photonics

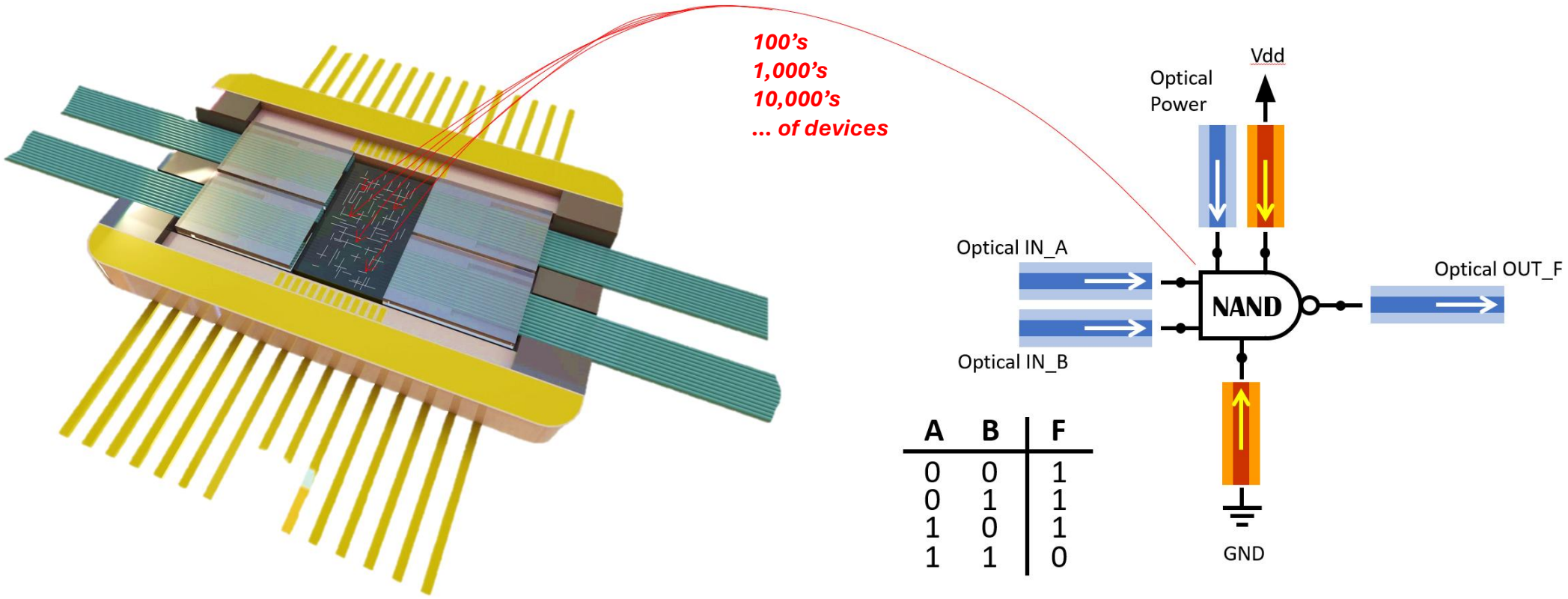


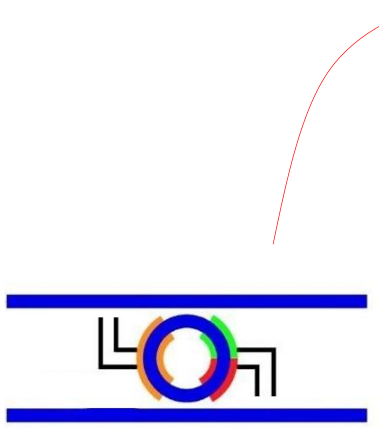

- Traditional Electrical CMOS with Power and Ground
- Optical Logic Gate that avoids cascading issues by supplying Optical Power ($O_{DD}$) – but still uses some electrical…

# Digital Photonic Chips

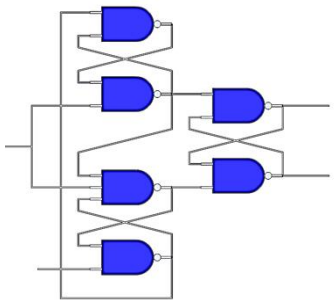
Using many hundreds or thousands of MRM-based optical logic gates, small/medium scale integrated "optical" circuit (SSI / MSI) digital chips can be made… connected with optical fiber… with no electrical noise, no DSP and no transceivers.



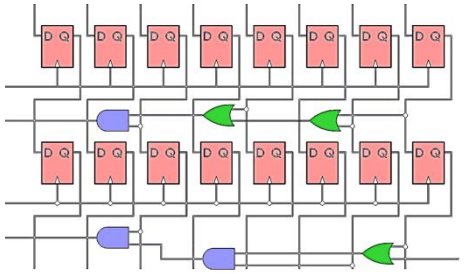
# Digital Photonic Processing



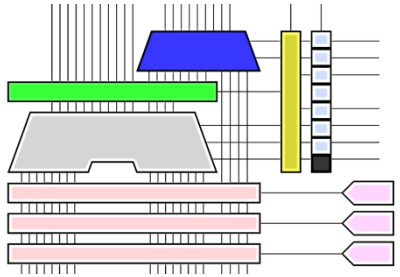
Optical Logic Gate



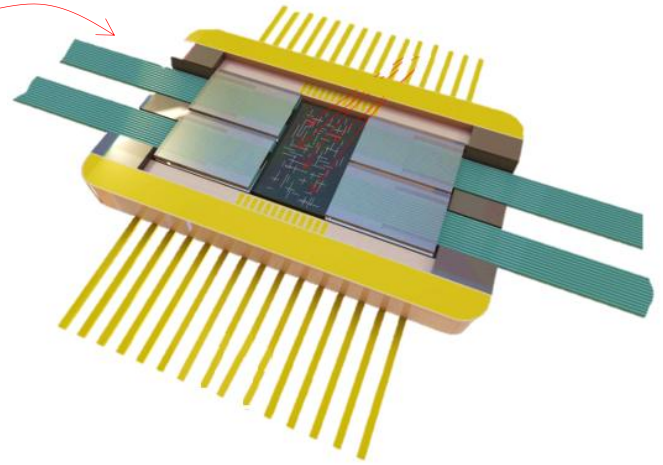
Optical DFF



Optical Registers



Optical Functions

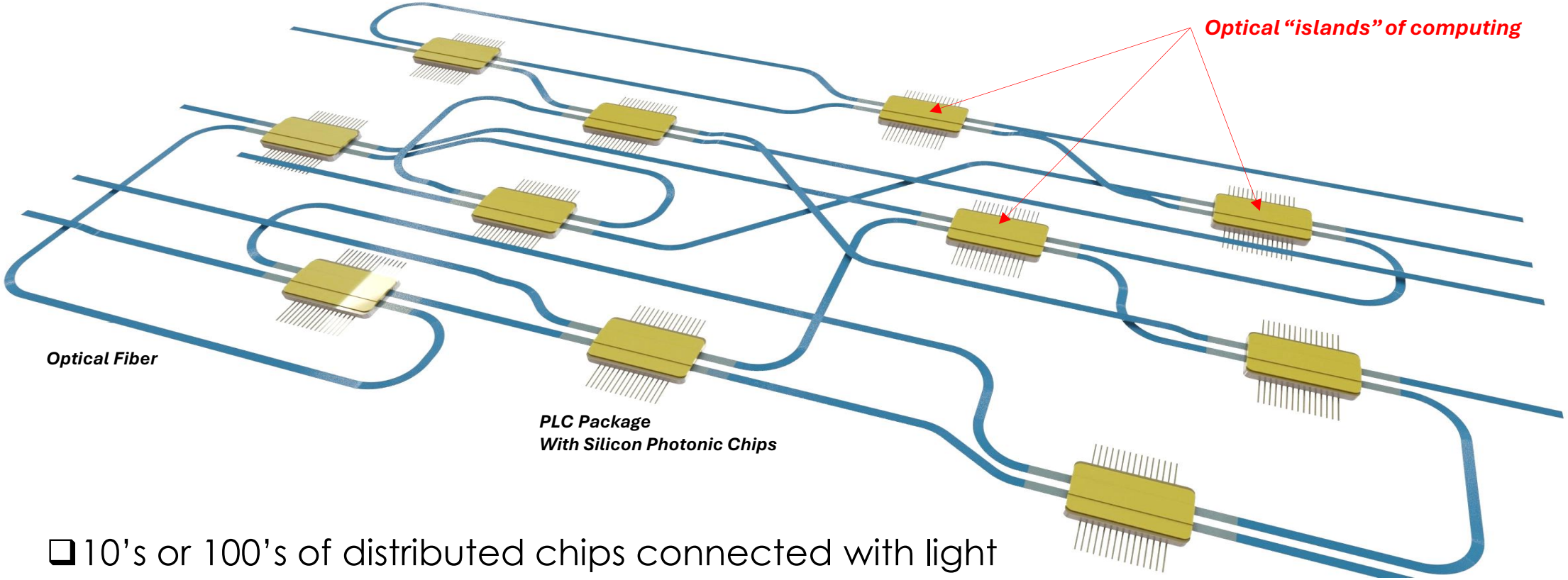


Optical Microchips

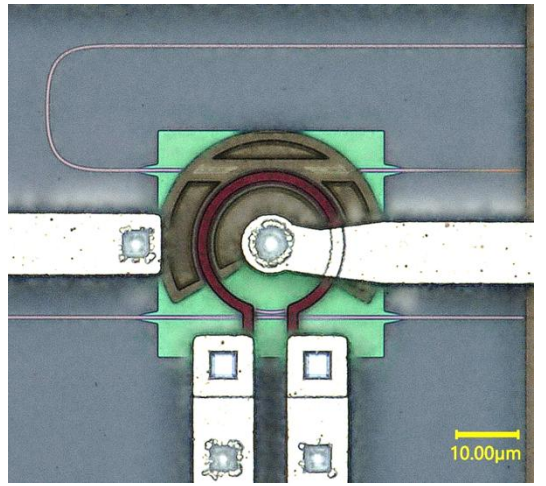
- Intelligent switching functions can be built using Optical Logic… enough to implement the paraDOX architecture up to 4,096 x 4,096 or more.

# Distributed Optical Processing

- **All** signals … **all** data … **all** control … **all** with **light**…



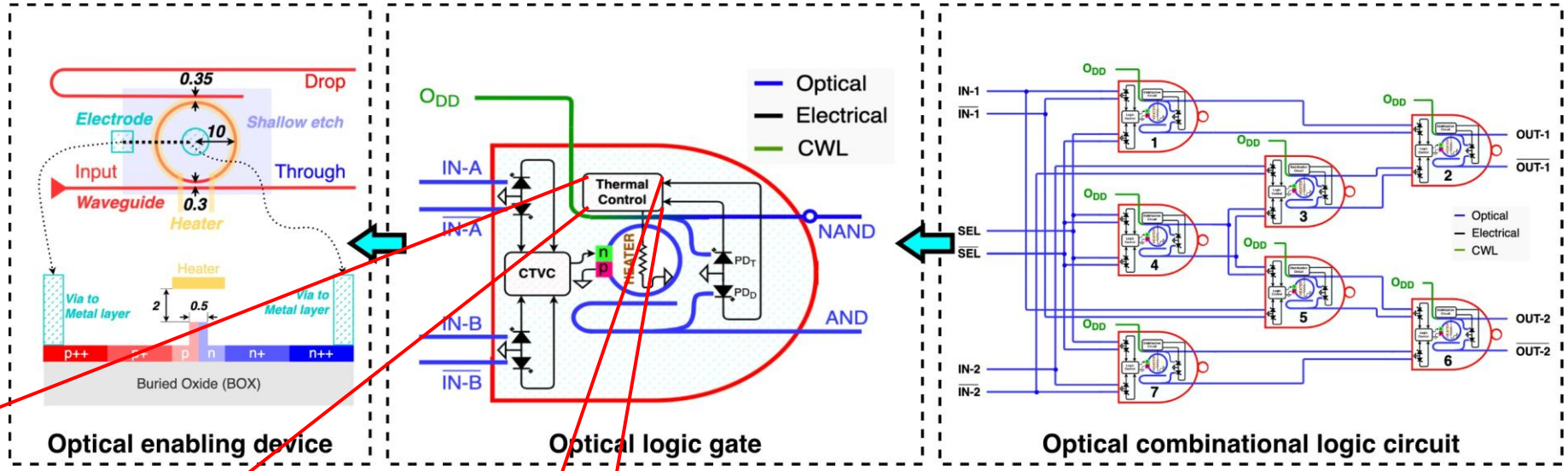

- ❑ 10's or 100's of distributed chips connected with light
- ❑ Removes the power density and each chip can be cooled using simple air conduction



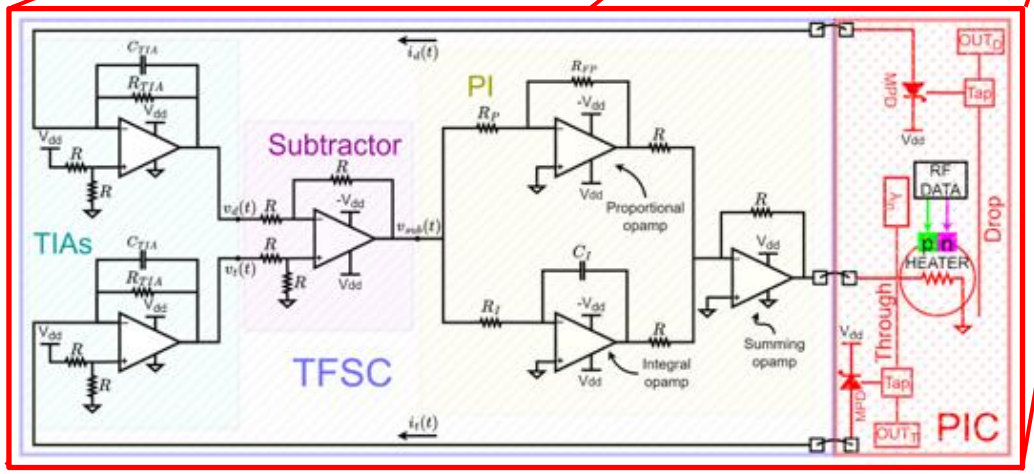

# 2 x 2 Switch Gen. 1

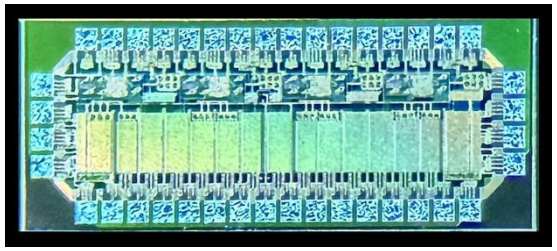
## Digital Photonics

# Based on Stabilized SiPhot MRM's

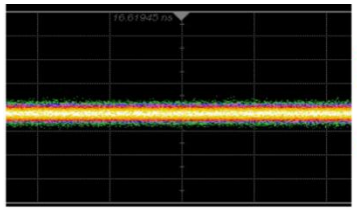



PATENTED

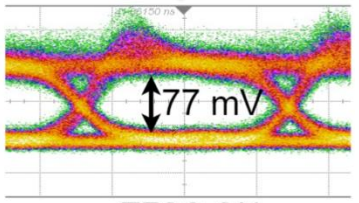


180nm CMOS Quad MRM
Thermal Feedback Stabilization Circuit (TFSC)



TFSC OFF



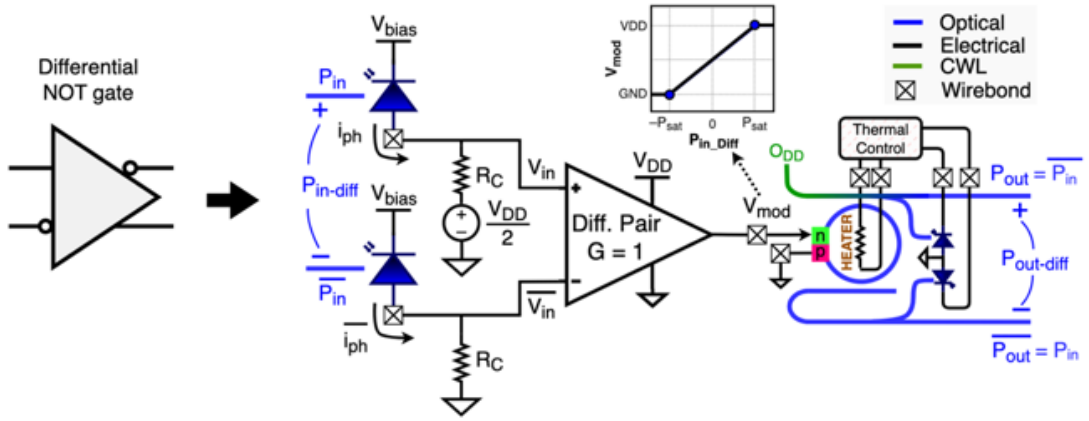

TFSC ON

Self-referenced. Compensates process and thermal variations, laser wavelength and power drifts. ~70 transistors.

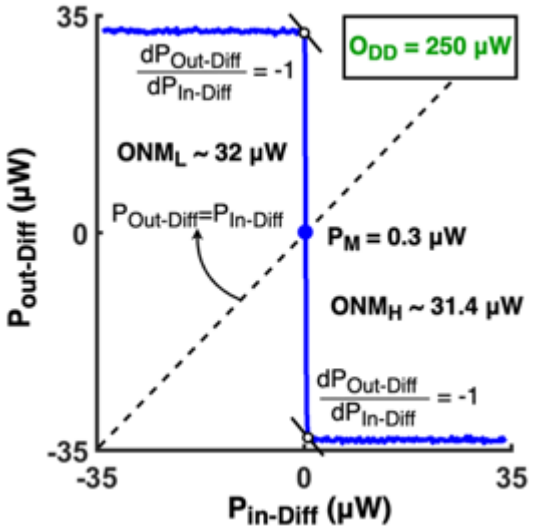
International patent application: **PCT/CA2025/050148**

# Optical MRM Gate Characterization

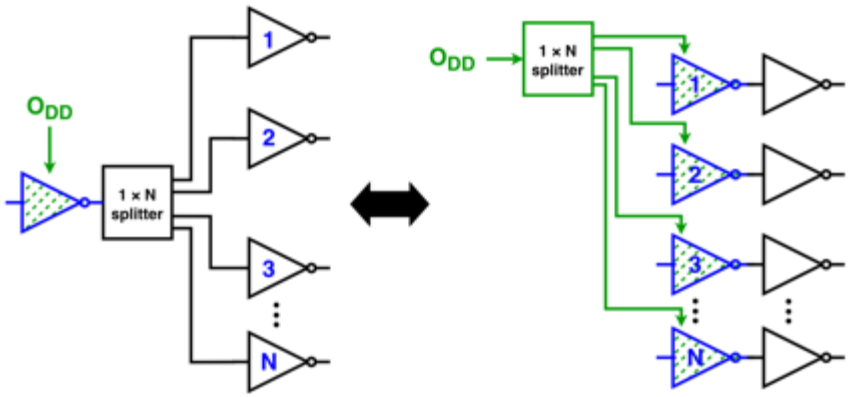
- PCB + PIC experimental setup
- Optical NOT gate $P_{in}$ corresponds to $P_{out}$ of previous MRM
- PTC, ONM and fanout measurements



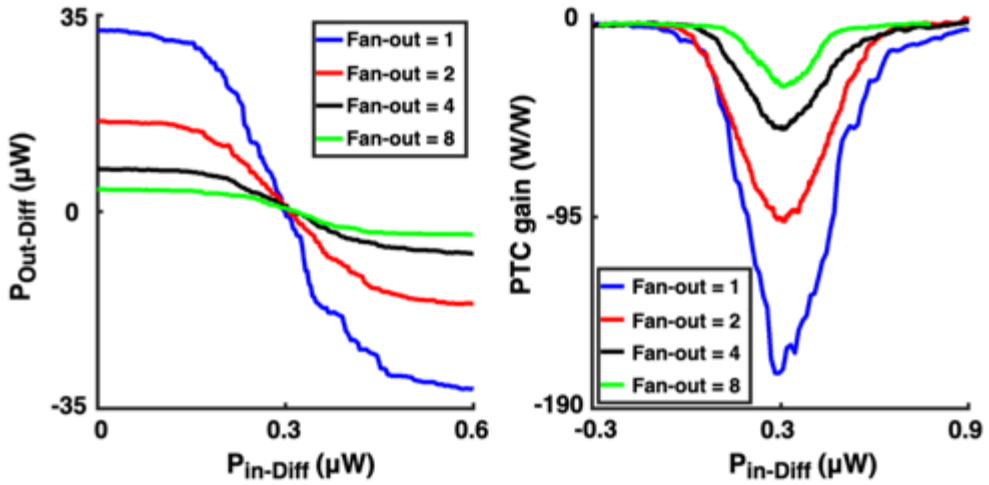

**Power transfer characteristic**
**ONM = 12.5% of $O_{DD}$**




**Fanout context**



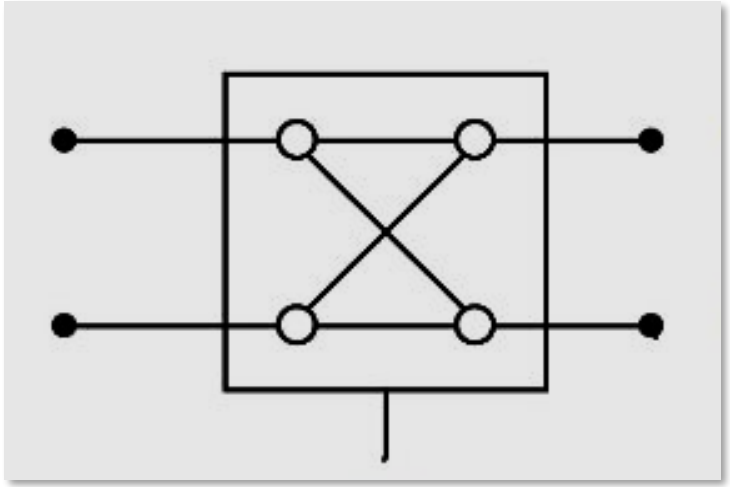

**Fanout = 4 to 8**



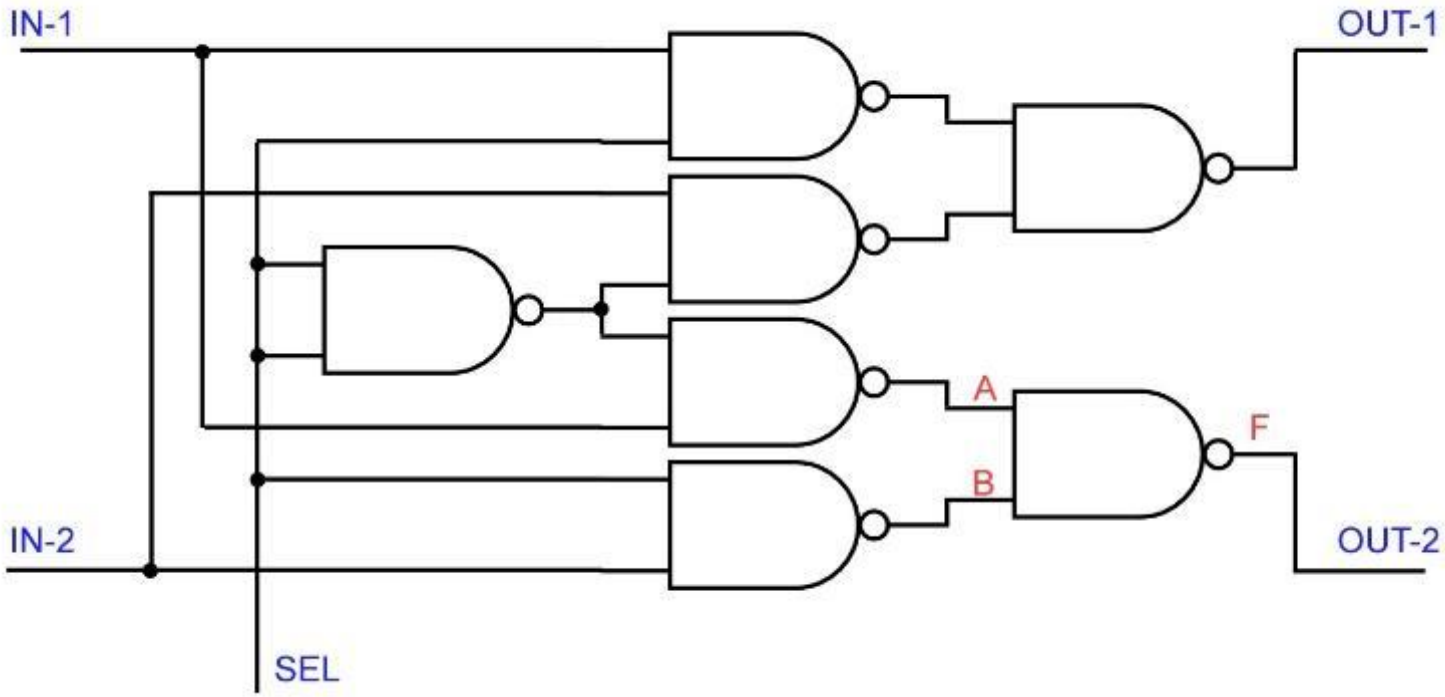

**J. Garcia-Echeverría**, *Scalable optical computing with stabilized silicon photonic microrings*, Ph.D. Thesis, McGill University.

# First Prototype Example

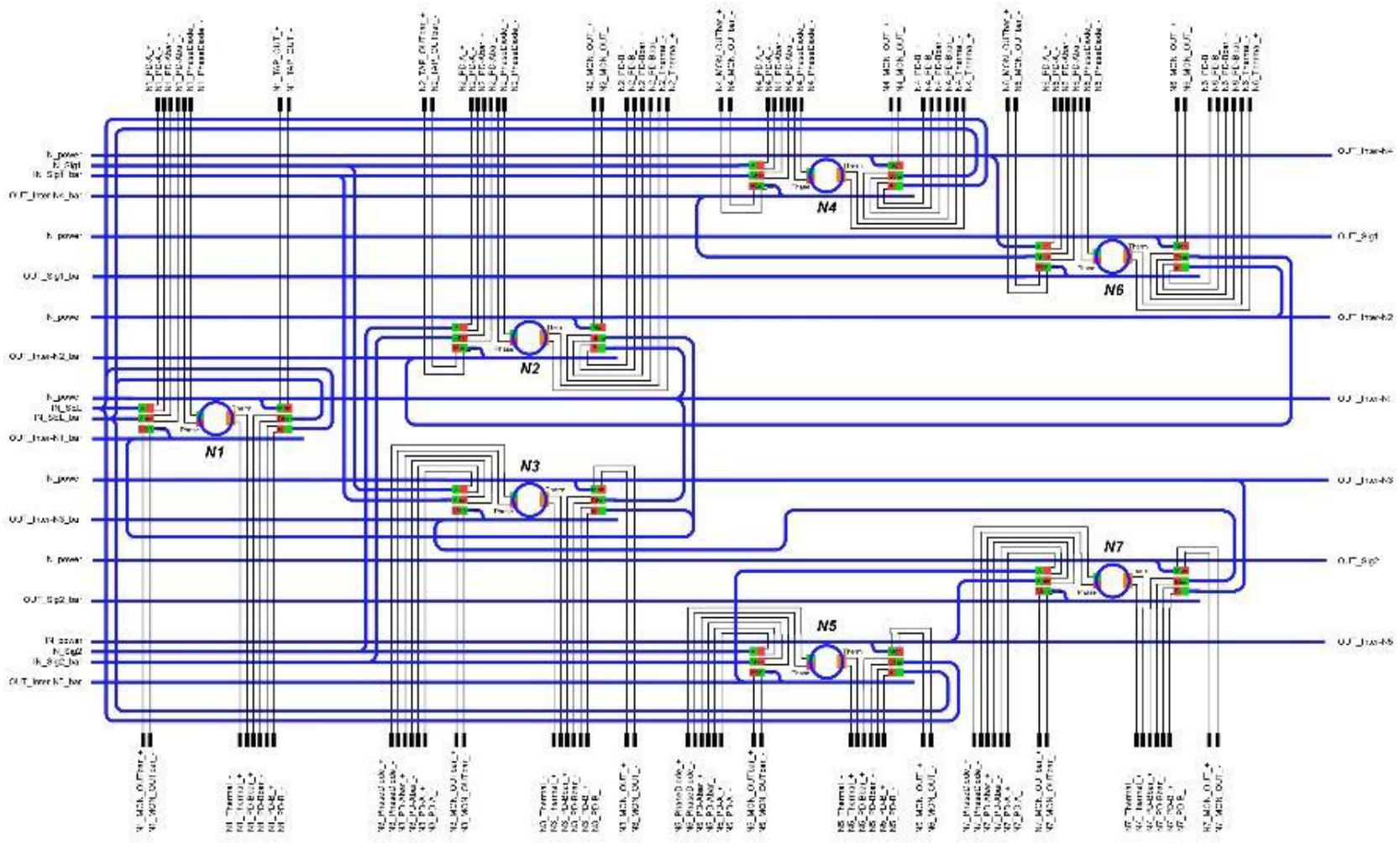
2 x 2 Crosspoint Switch

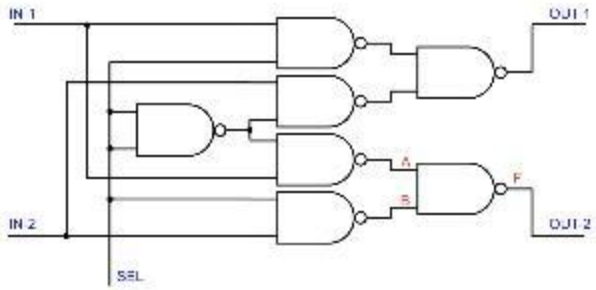


(x7) NAND-2 Gate Implementation:



# 2x2 NAND Switch (using MRM's)




- OLG chip implements the 7 NAND gate.
- Important feature – each NAND gate gets its own optical power… NO power cascading problems…

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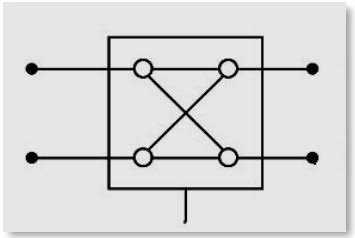
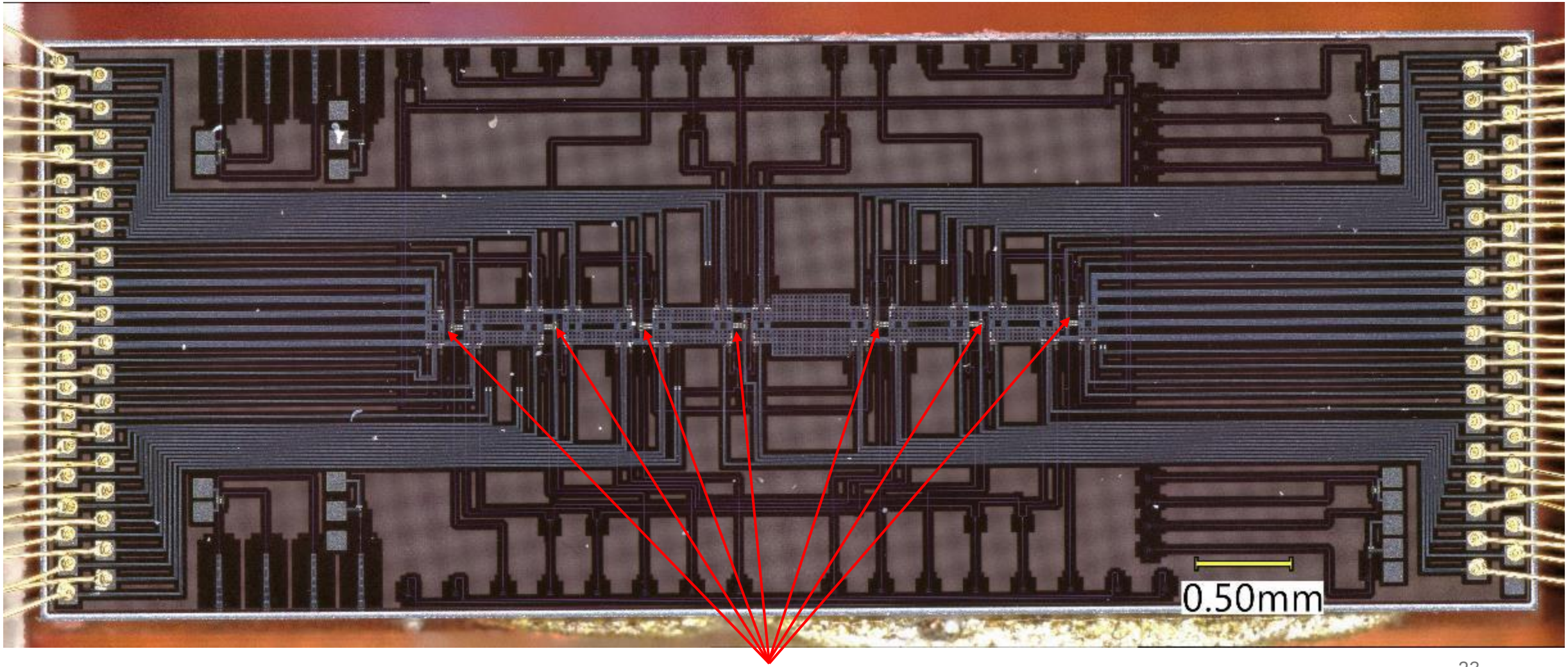


# 2x2 optical logic switch

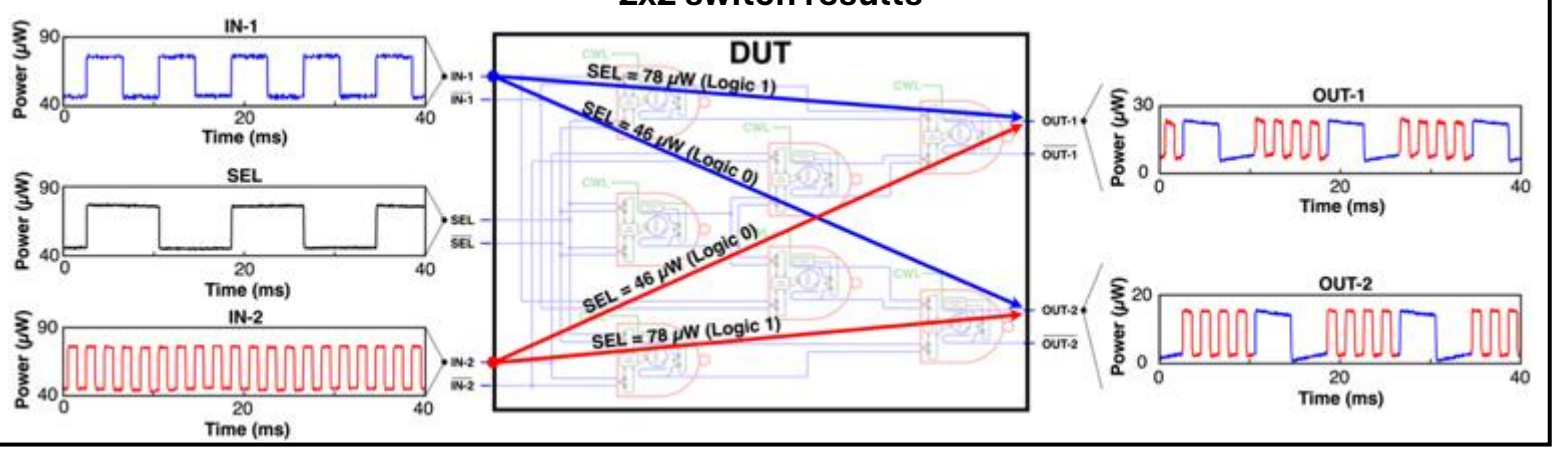



Optical Logic Gates

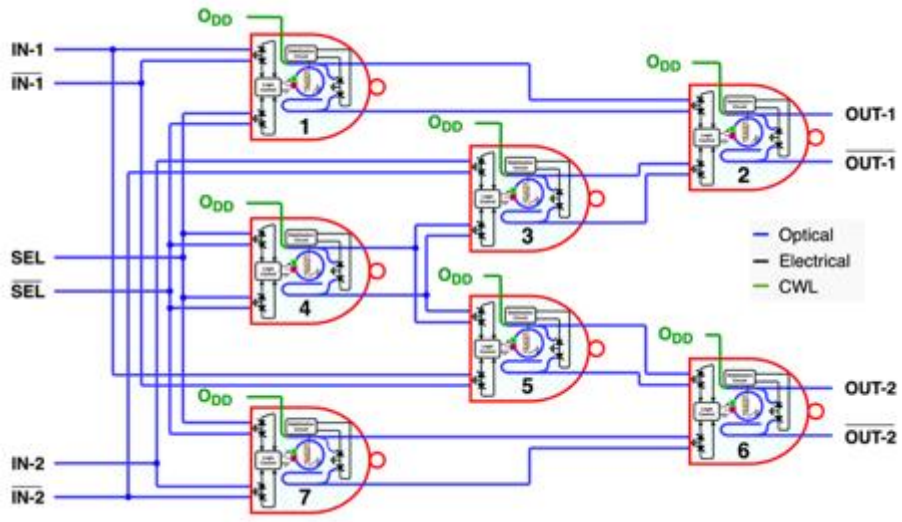
# Experimental results: 2x2 MRM switch

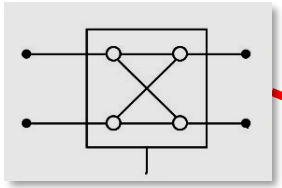
- Experimental setup
- Combinational logic circuit includes cascade of 3 OLG and a fanout of 2
- Switch Cross and Bar operation demonstrated succesfully

**2x2 switch results**

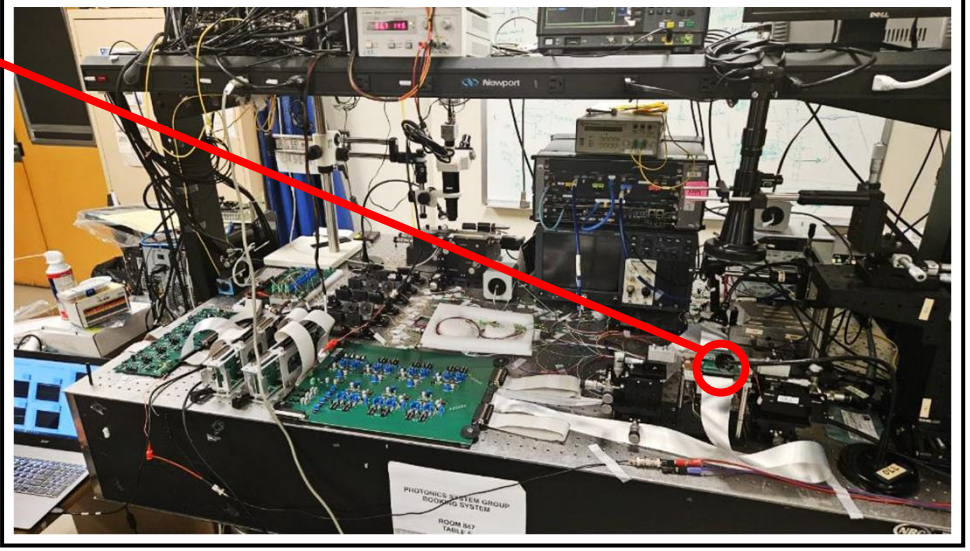



**2x2 switch based on MRM NAND gates**

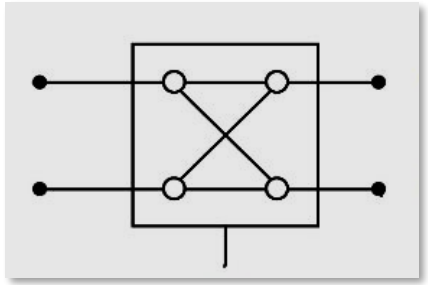


**2x2 switch experimental setup**

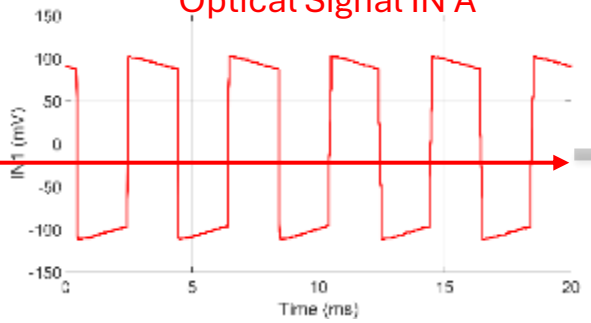


# 2 x 2 cross state



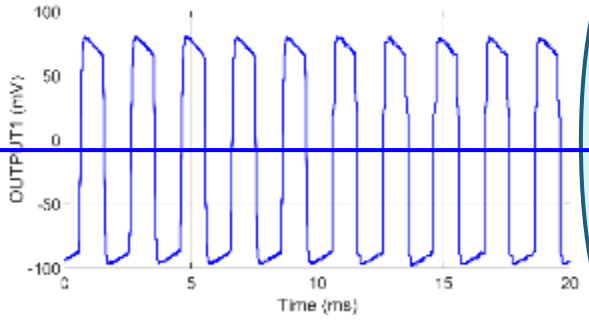
Optical Fiber

Optical Signal IN A




Optical Fiber

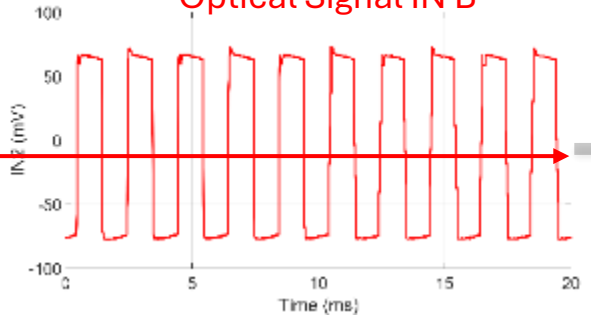
Optical Signal OUT B




2×2 NAND based switch

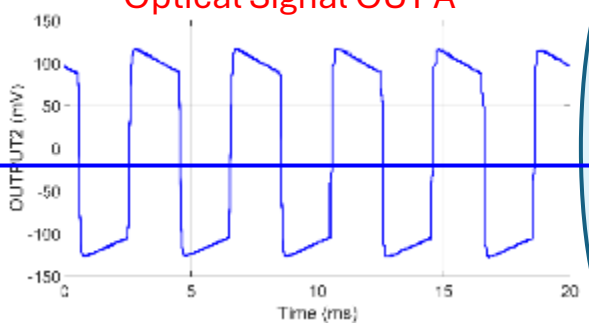
Optical Fiber

Optical Signal IN B




Optical Fiber

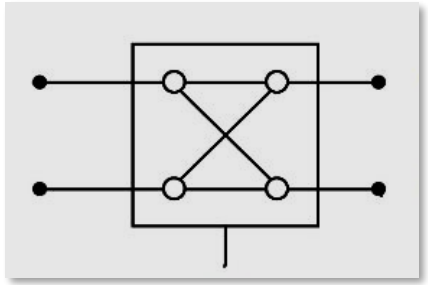
Optical Signal OUT A




SEL=0

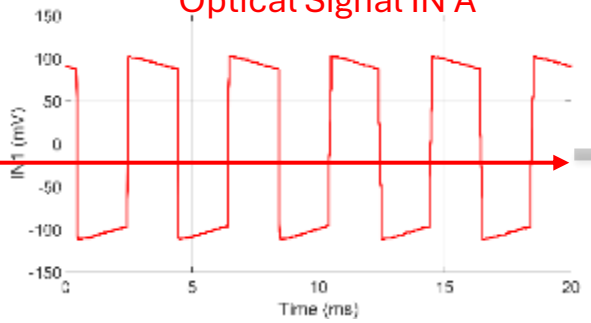
Optical Fiber

# 2 x 2 through state



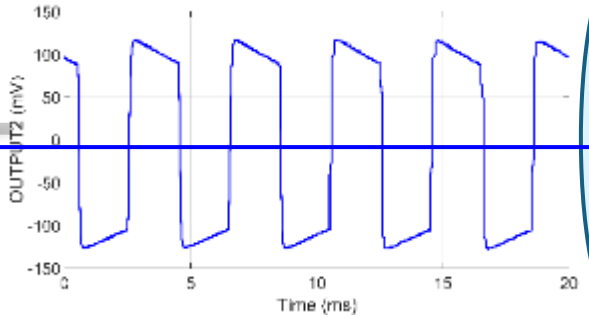
Optical Fiber

Optical Signal IN A




Optical Fiber

Optical Signal OUT A

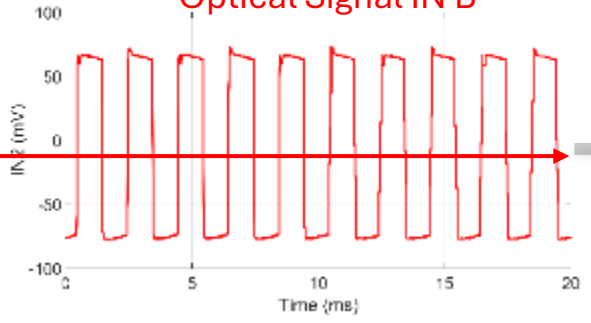



Optical Fiber

2×2 NAND based switch

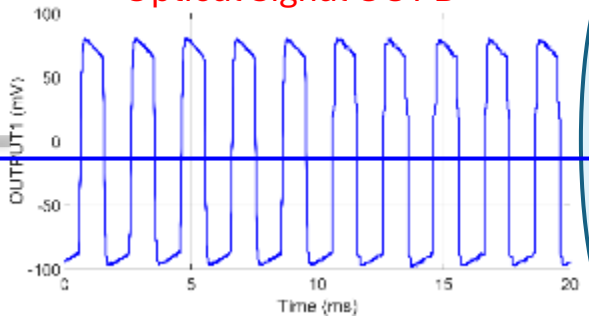
Optical Fiber

Optical Signal IN B




Optical Fiber

Optical Signal OUT B




Optical Fiber

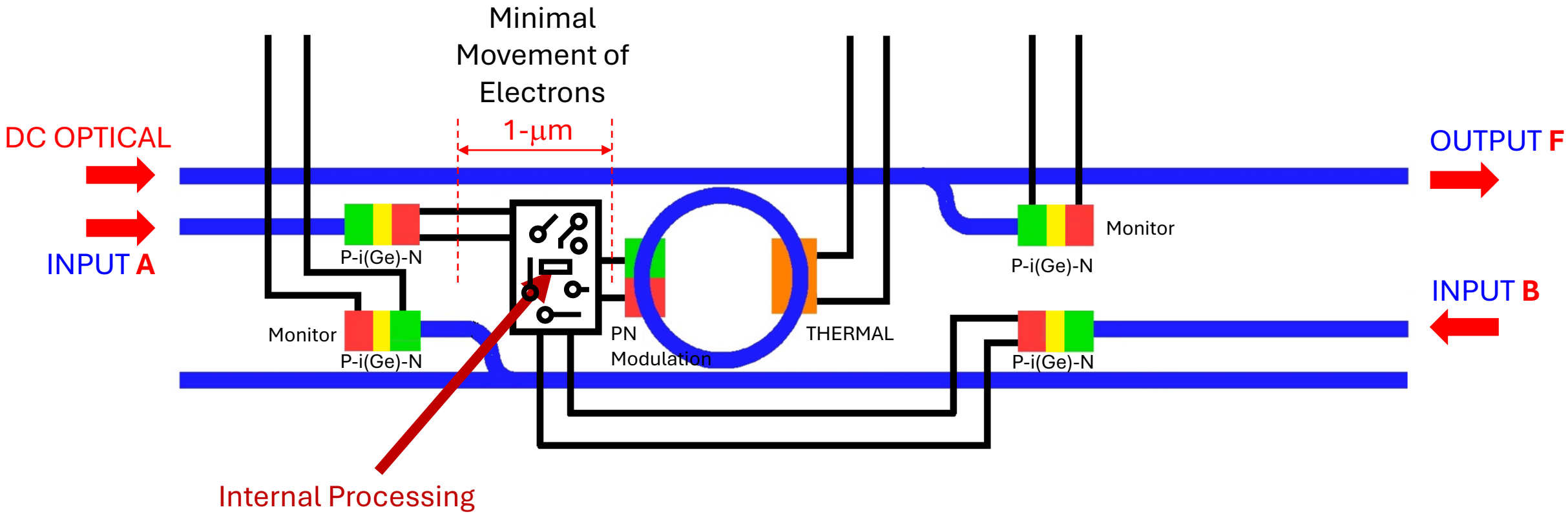
SEL=1

Optical Fiber

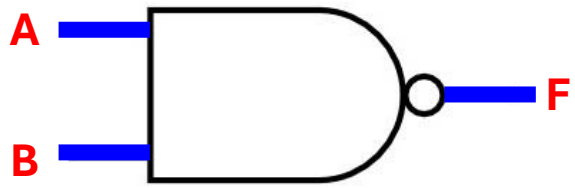

# 2 x 2 Switch Gen. 2

## Digital Photonics

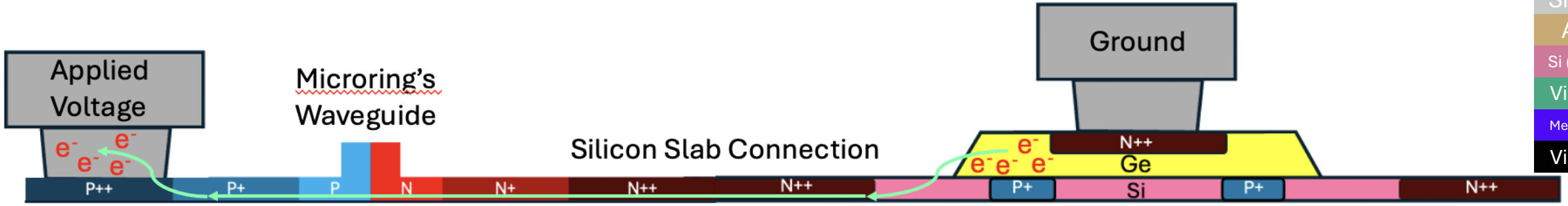
# Integrated **Optical MRM NAND Gate**




- Combines optical i/o with electrical i/o
- Electrical operates control and logical function



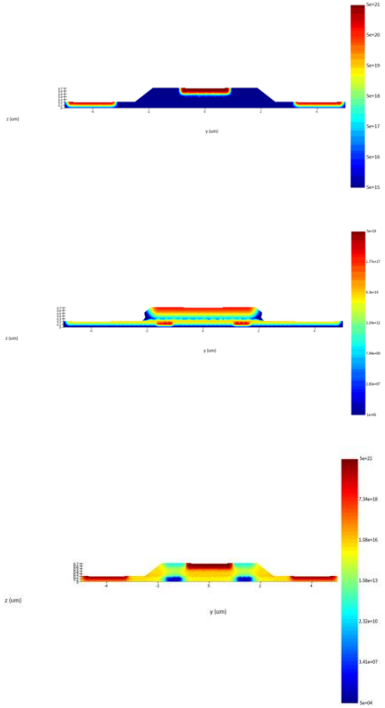
# Axonal compact logic gate



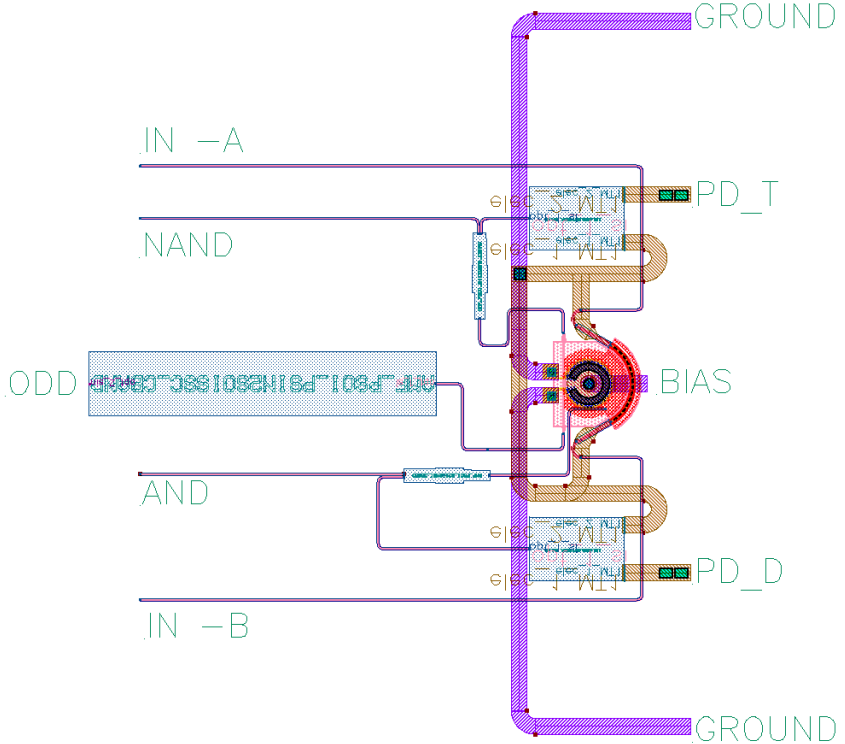

- Scalable Digital Photonics
- Fully integrated logic gate in SiPhot platform
- Bent Phototransistor + Microring modulator
- Fiber to the transistor (FTTT)
- Single MRM logic gate

PATENTED

**USPTO Application Number: 64/046,202**



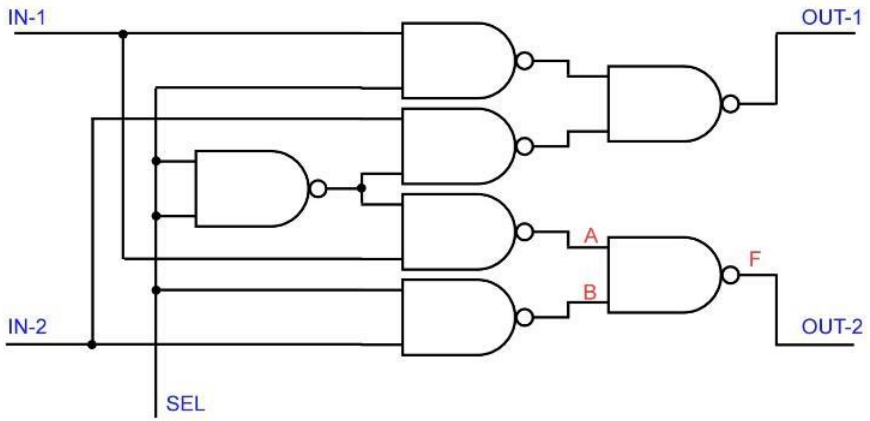
**Lumerical Charge simulations**



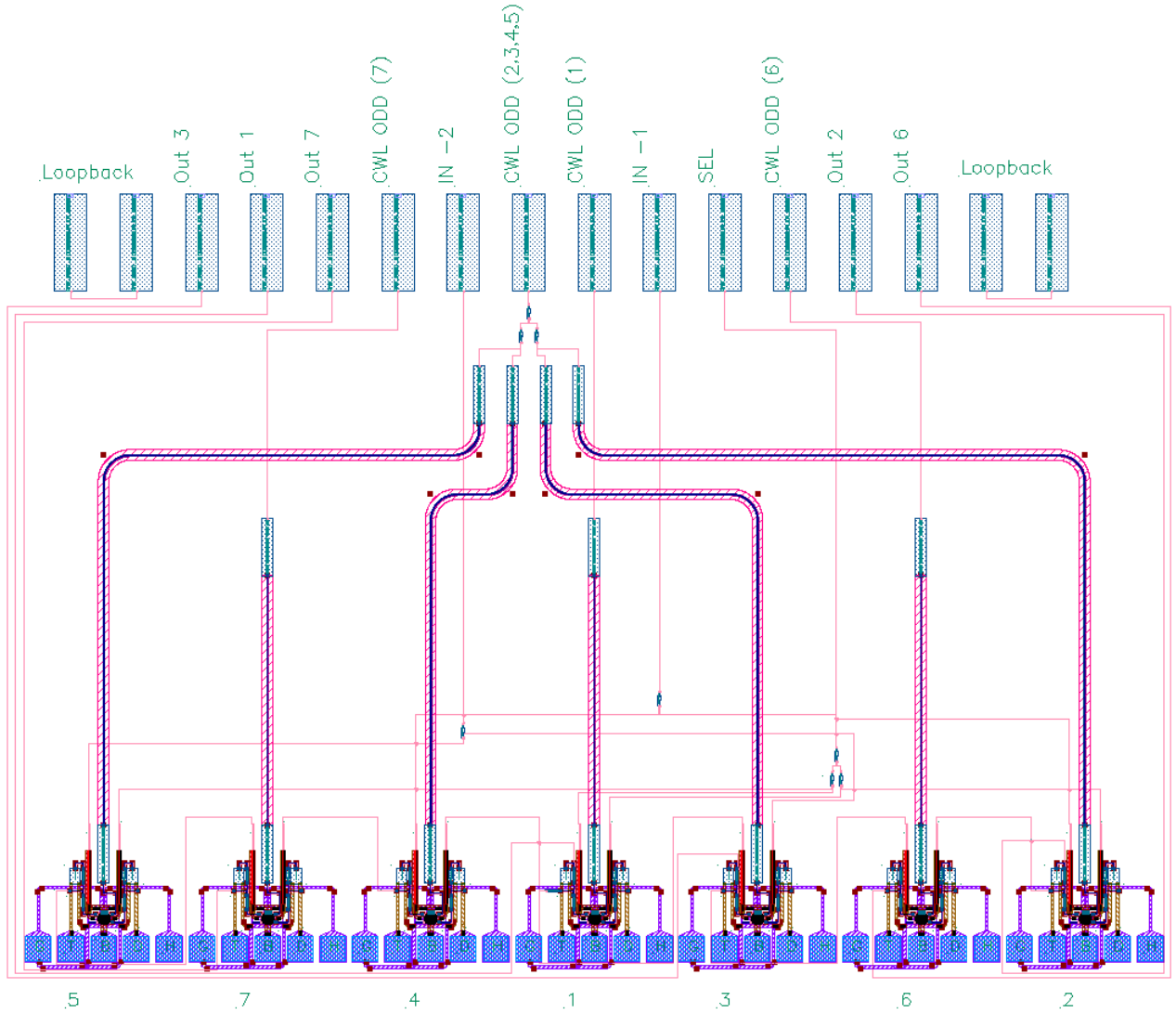

**Layout of compact logic gate**

# Digital photonics: 2x2 switch

- A digital photonics implementation of a 2x2 switch
- Disaggregated optical packet switch
- High-radix switches

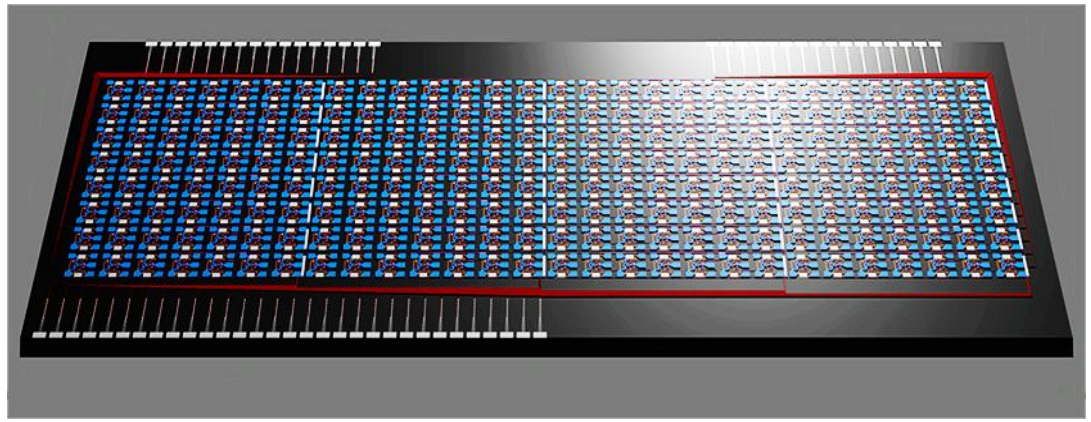



**Electrical implementation of 2x2 switch**




**Optical implementation of 2x2 switch**

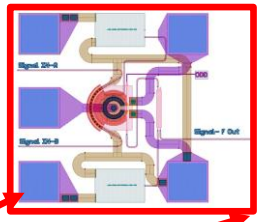
AXONAL NETWORKS



# Towards higher radix switches

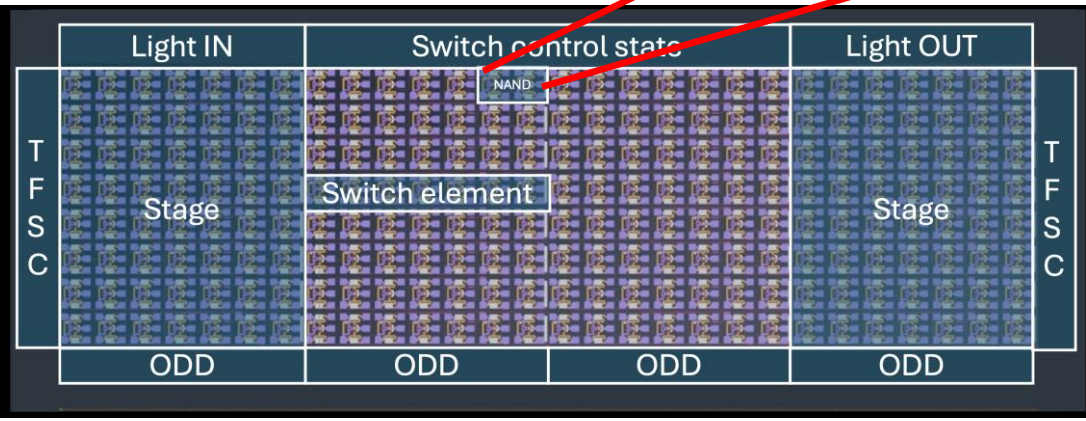
## Digital Photonics

# Axonal towards paraDOX-4096

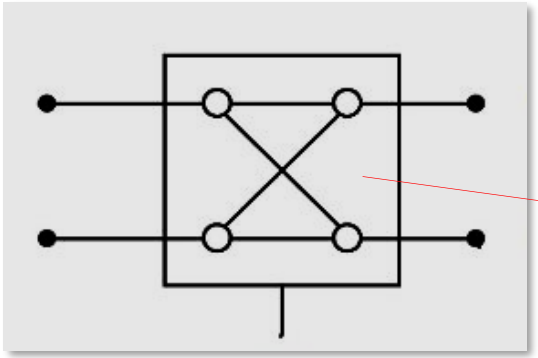


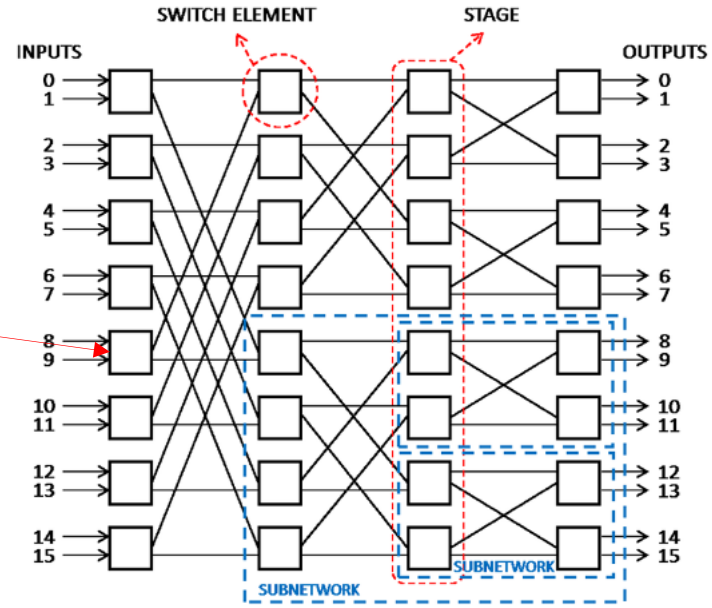
## SiPhot 16x16 Banyan Switch

224 Optical NAND Gates

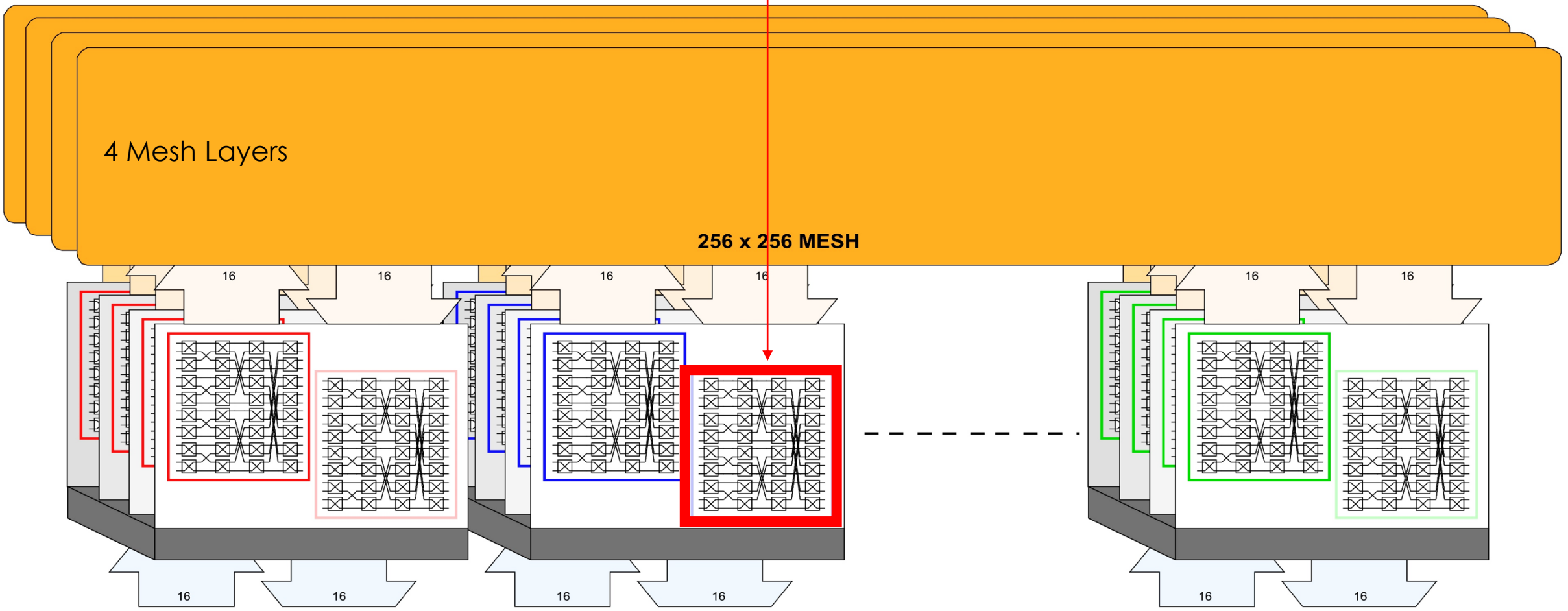



- Expanding on the 2x2 switch, the next prototype will be to create the 16 x 16 Banyan.





# 16 x 16 Banyan's for 256 x 256 paraDOX™



# Key takeaways

- We discussed why AI networking is becoming one of the primary bottlenecks in the continued scaling of AI infrastructure.
- paraDOX™ enables scalable, high-radix switching for AI data centers.
- Digital Photonics offers a promising path toward low-power, scalable paraDOX™ implementations.
- I presented the most compact silicon photonic logic gate based on microring modulators, as a building block for a 16×16 Banyan subswitch for paraDOX™ 256×256.


Connecting logic
with light