

Memristive technologies in spatial artificial intelligence architectures: A comprehensive review of advantages, bottlenecks, and mitigation strategies

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Space-based Artificial Intelligence (AI) and orbital edge computing are constrained by the physical limitations of traditional memory devices. Conventional architectures face the dual challenges of the von Neumann “memory wall” and strict operational requirements of space environments regarding energy, thermal dissipation, and radiation tolerance. Memristive In-Memory Computing (IMC) and In-Sensor-Memory Computing (ISMC) address these challenges by co-locating data storage and executing analog Matrix Vector Multiplication (MVM) within crossbar arrays. This review evaluates memristive technologies tailored for spatial AI architectures. We compare emerging Non-Volatile Memory (NVM) technologies under space environments based on their radiation tolerance and power consumption. Based on these trade-offs, Resistive Random Access Memory (RRAM) is highlighted as a primary option for orbital edge computing hardware. We discuss its structural radiation-tolerance mechanisms and low-power characteristics (exceeding 10 TOPS/W) across critical aerospace applications, including on-board hyperspectral image processing, autonomous deep-space asteroid navigation, and satellite cognitive radio orchestration. Despite these characteristics, implementing RRAM in flight-ready hardware is hindered by physical and architectural non-idealities. We trace accuracy degradation pathways from device-level variations to array-level parasitic and thermal constraints. To address these constraints, we present hardware-software co-design strategies that combine One-Selector-One-Memristor (1S1R) topologies and vertical thermal conduits (TSVs) with algorithmic compensations, including closed-loop write-verify schemes, bit-slicing, ensemble averaging, and dynamic Analog-to-Digital Converter (ADC) reference scaling. Based on these developments, we also provide an outlook on deploying neuromorphic processors in future orbital and deep-space missions.

Keywords: Edge computing, in-memory computing, RRAM, space environments, spatial AI

1. INTRODUCTION

As advanced deep space exploration and earth observation missions demand greater on-board autonomy, integrating Artificial Intelligence (AI) into space environments has become a key focal point in modern aerospace engineering [1, 2]. Next generation orbital systems and space-ground networks must process large datasets from hyperspectral and navigation sensors in real time [3]. This paradigm shifts edge computing applications directly into space, enabling spacecraft to perform tasks such as precision asteroid landing, autonomous Guidance, Navigation, and Control (GNC), and image classification without relying on high latency downlinks to earth [4]. However, deploying these intensive capabilities is strictly constrained by the rigid Size, Weight, Power, and Cost (SWaP-C) limitations of satellite payloads [5, 6].

Standard artificial neural network hardware is inherently inefficient in this context due to the physical separation of sensing, memory, and processing components, a classic limitation known as the von Neumann bottleneck or the “memory wall” [7]. The frequent data transfer across the memory bus elevates energy consumption and latency, with data movement between memory arrays and processors (such as CPUs or GPUs) accounting for up to 90% of total system energy [8]. While terrestrial edge computing effectively addresses this bottleneck through parallelized GPUs or Application-Specific Integrated Circuits (ASICs), adapting these Commercial-Off-The-Shelf (COTS) processors for space payloads presents significant trade-offs [2]. For instance, high performance architectures like the NVIDIA Jetson Orin series deliver substantial throughput (measured in TOPS), but their power consumption frequently exceeds the electrical and thermal budgets allocated to small satellites [5].

In addition to power constraints, the space environment introduces radiation hazards, including galactic cosmic rays and solar proton events. Standard CMOS logic and charge-based memories are susceptible to radiation-induced data corruption and transient faults [9]. Conversely, legacy radiation-hardened processors (such as the BAE RAD750 or LEON3/LEON4 series) provide high reliability, but their computational performance, typically capped between 50 and 400 DMIPS, is insufficient to handle the intensive matrix-multiplication workloads required for deep learning inference [6]. Implementing physical shielding or structural redundancy protocols to safeguard standard processors introduces substantial overhead, further exacerbating SWaP-C constraints [10].

To reconcile the need for high computational throughput with environmental survivability, researchers are investigating In-Sensor Memory Computing (ISMC) architectures based on Non-Volatile Memory (NVM) devices, specifically memristors or Resistive Random Access Memory (RRAM) [11]. Memristors operate as artificial synapses that simultaneously store data and execute analog Matrix Vector Multiplications (MVMs) in situ. By co-locating storage and computation within unified crossbar arrays, these architectures execute MVMs directly in the analog domain via Ohm’s and Kirchhoff’s laws [12]. This approach effectively mitigates the memory wall, yielding high energy efficiency with performance metrics approaching 150 TOPS/W [8]. Furthermore, because memristors rely on physical atomic reconfiguration rather than trapped electronic charge, their state retention mechanisms offer inherent resilience against ionizing radiation [13]. Consequently, memristive ISMC architectures present a promising framework for efficient and autonomous orbital edge intelligence.

The following analysis evaluates memristor technologies within spatial AI architectures, focusing on their energy efficiency and radiation tolerance. It also examines the

physical bottlenecks, hardware non-idealities, and thermal constraints associated with these devices, alongside the mitigation strategies required for reliable deployment in space environments.

2. MEMRISTIVE IN-MEMORY COMPUTING

Leon Chua proposed the memristor in 1971 as the fourth fundamental passive circuit element, linking magnetic flux (Φ) and electric charge (q) through the relationship $M(q) = d\Phi/dq$ [14]. Modern resistive switching devices rely on a Metal-Insulator-Metal (MIM) structure, operating by changing the resistance of a dielectric layer between two electrodes. While conventional NAND flash memory stores data by trapping electrons in a floating silicon gate, a memristor stores information by forming and breaking nanoscale Conductive Filaments (CFs) inside an insulating matrix, such as HfO_2 , TiO_2 , or Ta_2O_5 [7]. Applying an electric field causes oxygen ions to migrate toward the anode, leaving behind positively charged oxygen vacancies that group together to create a continuous conductive filament connecting the electrodes. This process transitions the device from a High Resistance State (HRS) to a Low Resistance State (LRS) during the “SET” operation. Reversing the voltage polarity pushes the ions back to recombine with the vacancies, breaking the filament and returning the device to the HRS during the “RESET” operation [15]. Because the conductive filament’s width and density depend on the applied voltage and compliance current, memristors achieve multiple stable conductance states. This analog tunability allows a single device to represent specific synaptic weights in an Artificial Neural Network (ANN), supporting high density neuromorphic processing that mimics biological plasticity [16, 17, 8].

In typical In-Sensor Memory Computing (ISMC) architectures, memristors form a passive crossbar array where WL and BL intersect perpendicularly, placing a device at every junction. When input voltage vectors, representing sensor data or neural network activations, are applied to the WL, the currents passing through the memristors sum automatically along the BL [18]. The total current I_j on the j -th BL is calculated as

$$I_j = \sum_i V_i G_{ij}, \quad (1)$$

where the input voltage V_i applied to the specific word-line is multiplied by the analog conductance of the memristor at that intersection.

This architecture performs Multiply-Accumulate (MAC) operations in a single clock cycle with $O(1)$ time complexity, avoiding the digitization, bus routing, and data-fetching delays inherent to the von Neumann architecture [19, 20]. Furthermore, integrating ISMC with 2D material-based optoelectronic synapses adds direct environmental

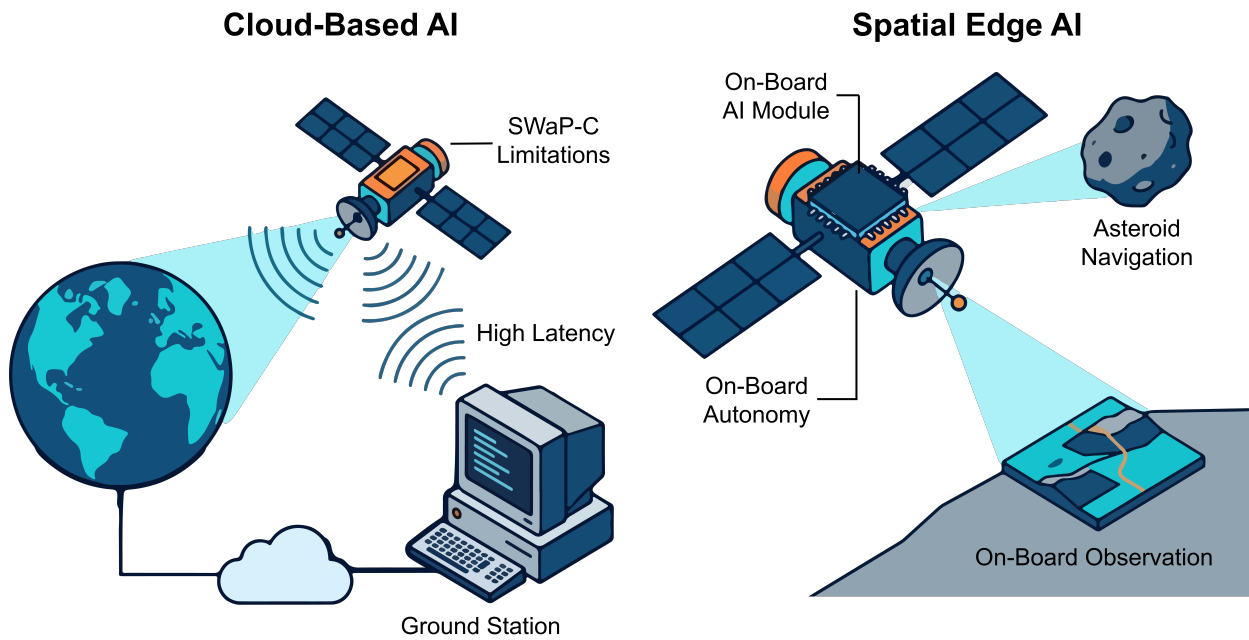


Figure 1 – Configurations of cloud-based and autonomous spatial edge AI. The conventional cloud-based framework relies on continuous telemetry to ground-based processors, causing communication delays. The spatial edge AI framework deploys computing units directly on the satellite to perform in-situ data processing for celestial navigation and orbital mapping.

sensing capabilities, where capturing light, gas, or radiation immediately changes the crossbar’s conductance to create a unified sense-compute-memory loop [12].

3. INTRINSIC ADVANTAGES OF MEMRISTIVE HARDWARE IN SPACE ENVIRONMENTS

Deploying artificial intelligence in space is fundamentally bottlenecked by two hardware constraints: severe ionizing radiation (GCRs, SPEs) that induces TID and SEE degradation [21, 22, 23], and the stringent power budgets of small satellite platforms [24]. Memristive in-memory computing offers a unified solution to these challenges. Physically, memristors exhibit a high degree of intrinsic radiation tolerance that compares favorably with charge-based space-grade microelectronics [10]. Architecturally, this paradigm eliminates energy-intensive memory-bus data shuttling [25]. Furthermore, advanced materials engineering (e.g., Ag/TiO₂/Pt synaptic emulators) enables sub-3V, nanosecond-regime switching with ultra-low operational power down to ~3.76 pJ/spike [26, 27, 28].

3.1 Intrinsic radiation hardness: From charge vulnerability to structural immunity

The deployment of conventional microelectronics in space is constrained by their reliance on stored charge.

In traditional floating-gate NAND flash, Dynamic RAM (DRAM), and advanced CMOS logic, binary data depends on maintaining isolated electron packets [10]. When ionizing radiation passes through the silicon dioxide (SiO₂) dielectric layer, it generates electron hole pairs. Highly mobile electrons exit the oxide quickly, but heavier holes possess low mobility and become trapped at defect centers near the Si/SiO₂ interface [29]. This accumulated positive charge density (Q_{ox}) shifts the transistor’s threshold voltage (V_{th}), governed by the relationship:

$$\Delta V_{th} = \frac{Q_{ox}}{C_{ox}}, \quad (2)$$

where C_{ox} is the oxide capacitance. As a result, a Total Ionizing Dose (TID) between 100 and 300 krad (Si) typically causes logic failure, data corruption, and parasitic leakage [30]. Additionally, heavy ion strikes create transient charge tracks that induce Single Event Upsets (SEUs) and Single Event Latch-ups (SELs) [31]. While radiation-tolerant Field Programmable Gate Arrays (FPGAs), such as the Microchip RTG4, withstand TID up to 300 krad (Si), they require extensive Triple Modular Redundancy (TMR) [32]. This mitigation strategy significantly increases the power and mass budgets of satellite payloads [33].

Emerging non-volatile memories, including memristive ReRAM, Phase Change Memory (PCM), and Magnetoresistive RAM (MRAM), overcome these vulnerabilities by storing data through structural, phase, or magnetic configurations rather than isolated charge [34, 35]. In memristors, the resistance state depends on the physi-

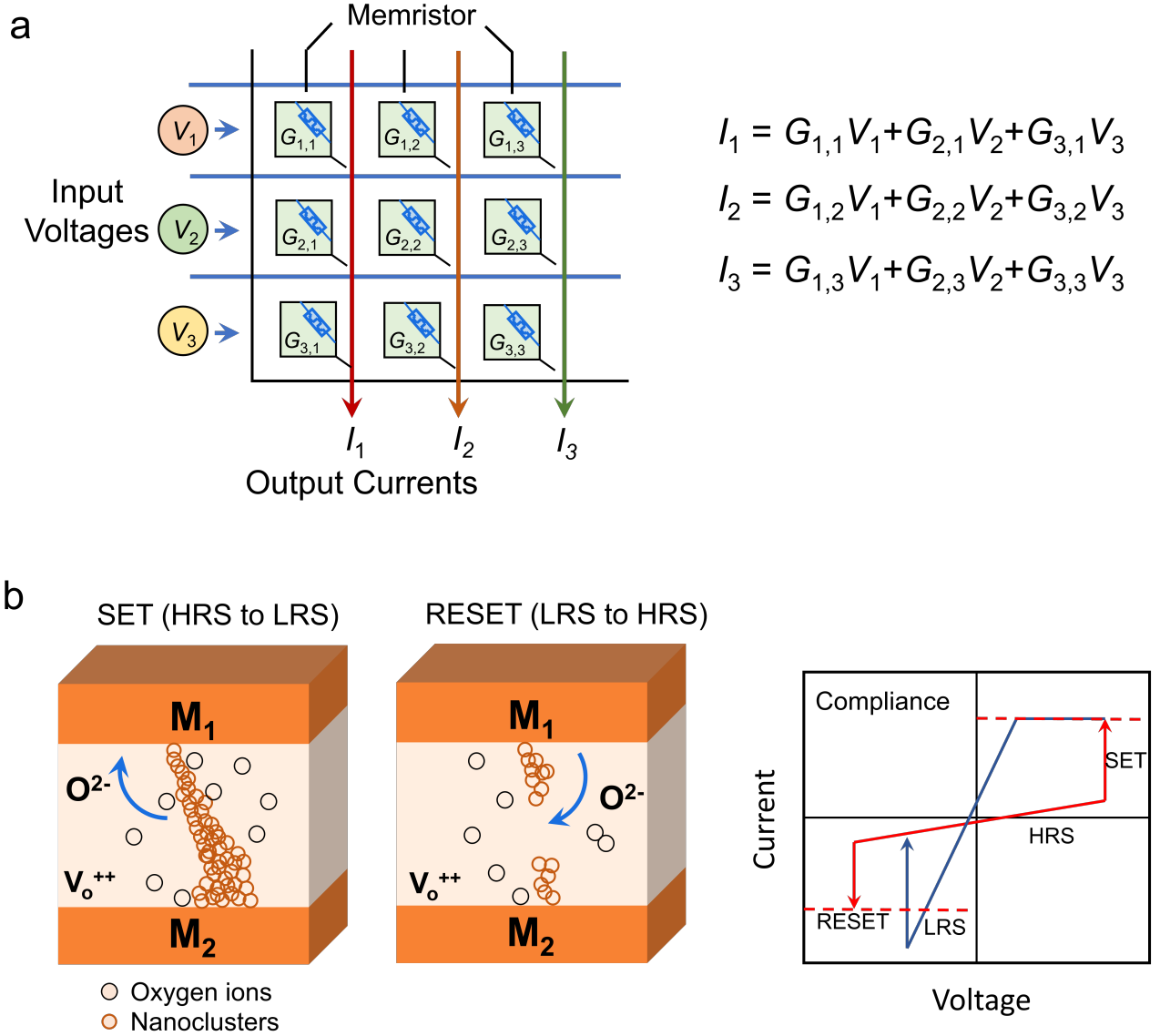


Figure 2 – Circuitry and device-level architectures of RRAM-based computing. (a) Analog Matrix Vector Multiplication (MVM) mapping via memristor crossbar arrays. (b) Bipolar filamentary memristor resistive switching, showing the transition of conductive pathways under positive and negative bias.

cal arrangement of metallic atoms or oxygen vacancies. Because they store information through atomic or ionic reconfiguration rather than trapped electronic charge, the memristive storage element is comparatively insensitive to the charge-trapping and interface-charging mechanisms that dominate total dose degradation in conventional devices [10]. This intrinsic tolerance, however, is a device-level property and should be distinguished from array-level computational stability and system-level space reliability, which are additionally governed by peripheral-circuit robustness, crossbar parasitics, and thermal management. Empirical studies show that HfO_2 and TaO_x -based memristors tolerate TID exposures exceeding 1 Mrad (Si), well above the requirements for standard Low Earth Orbit (LEO) or Geostationary Orbit (GEO) missions [22, 36]. For example, $\text{Ag}/\text{AlO}_x/\text{Pt}$

ReRAM devices exposed to high-dose γ -ray radiation maintain stable Low Resistance State (LRS), SET, and RESET voltages [37]. Researchers attribute this stability to a hybrid filament model, where radiation-induced trapped holes interact with mobile metal ions (e.g., Ag^+) to reinforce existing conductive filaments rather than disrupt them. Beyond TID tolerance, memristors resist atomic displacement damage from heavy ion and proton bombardment [36]. HfO_2 -based crossbar arrays operate stably under 10 keV to 300 keV proton irradiation at fluences up to 10^{12} cm^{-2} , with accelerated aging tests projecting data retention exceeding 14 years post-irradiation [38]. While extreme proton fluences may cause minor structural defects that slightly decrease maximum endurance cycles, the devices retain their non-volatility, analog state stability, and Matrix Vector Multiplication (MVM) accu-

racy, outperforming standard solid-state drives under equivalent conditions. It should be noted, however, that this structural tolerance applies only to the memristive storage element itself. The peripheral CMOS circuits that drive and read the crossbar, row and column decoders, sense amplifiers, and ADCs/DACs, remain susceptible to heavy ion Single Event Effects (SEEs), as evidenced by the single event functional interrupts observed in radiation testing of a production embedded ReRAM [39].

3.2 Comparative analysis of emerging NVMs in radiation environment

The performance landscape of emerging non-volatile memory variants reveals distinct architectural trade-offs for aerospace implementation.

As summarized in Table 1, MRAM provides high endurance and inherent resistance to single event upsets due to its magnetic storage mechanism. However, flipping its magnetic domains, even in Spin-Transfer Torque variants, requires high driving currents. This requirement restricts its scalability and power efficiency for deep learning applications [10, 34]. Alternatively, Phase Change Memory (PCM) offers high bit densities but incurs significant thermal overhead and latency during the melting and quenching phases of chalcogenide glass (e.g., $\text{Ge}_2\text{Sb}_2\text{Te}_5$) [15]. Compared to these alternatives, memristors provide a practical solution for neural network acceleration in space environments. They balance radiation tolerance and dense crossbar scalability with low read and write power consumption [11].

3.3 Ultra-low power characteristics and hardware benchmarking

The strict power budgets of small satellites, often constrained to a few available watts for entire scientific subsystems, mandate highly-efficient data processing hardware [24]. Memristive in-memory computing architectures improve power efficiency by eliminating energy-intensive data transfer between memory and processing units. At the device level, memristors operate at logic levels below 3 V and perform state transitions within the nanosecond regime [27]. Material engineering advancements, including precision two-step growth techniques using strontium-doped titanium, have reduced switching currents by several orders of magnitude compared to initial metal oxide devices, significantly lowering resistive Joule heating [25]. Research into synaptic emulation using Ag/TiO₂/Pt memristors demonstrates energy consumption as low as ~3.76 pJ/spike [28]. These efficiency metrics make memristive hardware a suitable substrate for neuromorphic computing, enabling complex tasks such as autonomous navigation and satellite resource

orchestration within the power constraints of orbital environments.

At the system level, fully integrated memristive Systems-on-Chip (SoCs) demonstrate remarkable leaps in the critical metric of Tera-Operations Per Second per Watt (TOPS/W) [16]. While highly-optimized COTS edge processors, such as the NVIDIA Jetson Orin series, deliver up to 275 sparse TOPS, they typically operate in the range of 1 to 5 TOPS/W (with AGX Orin at 3.33 TOPS/W) under heavy thermal loads that require active cooling [43, 44, 45]. In contrast, memristive architectures benchmark substantially higher [19, 46, 47]. Recent hardware implementations of non-volatile Resistive Random Access Memory (ReRAM) Computing-In-Memory (CIM) macros report energy efficiencies ranging from 11.91 to 251 TOPS/W for multi-bit configurations, soaring to a staggering 1286.4 TOPS/W for highly-optimized low precision operations [45].

A practical benchmark demonstrating this extreme efficiency is the STELLAR (Sign- and Threshold-based Learning) architecture [19]. Monolithically integrating 160,000 memristor units onto a 28 nm CMOS logic layer, STELLAR enables on-chip edge learning by circumventing the power-prohibitive data movement inherent to conventional backpropagation. By utilizing a cycle-parallel conductance tuning scheme to avoid hardware-heavy write-verification processes [20], the framework achieves a 35-fold energy efficiency improvement over equivalent digital accelerators. Crucially, it reduces energy consumption by 97% for real-time edge tasks, maintaining software-equivalent accuracy under a total power envelope strictly below 10 mW. Such a reduction in energy consumption makes this paradigm uniquely suited for Spatial AI applications, where space-borne platforms must adapt to dynamically changing environments under rigid Size, Weight, and Power (SWaP) envelopes without relying on high-latency cloud connectivity.

4. APPLICATIONS OF MEMRISTIVE SPATIAL AI

The combination of radiation tolerance, parallel execution, and energy efficiency makes memristive architectures suitable for spatial AI processing. By eliminating the delays associated with data telemetry and ground-based computing, these hardware subsystems enable real-time, on-board data analysis directly on spacecraft. Based on these device-level capabilities, the following sections examine the deployment of memristor-enabled architectures across critical aerospace applications, focusing on the conversion of raw sensor data into autonomous operational decisions in orbit. At the device level, the radiation tolerance of RRAM storage elements has already been demonstrated in space via flight experiments [49].

Table 1 – Comprehensive comparative assessment of standard and emerging memory technologies under ionizing radiation and spatial constraints.

Memory Technology	Fundamental Storage Mechanism	Radiation Tolerance	Approx. TID Static Error Threshold	Write Power / Latency
CMOS [29]	Active Charge (Flip-Flops)	Low	<200 krad (Si)	Moderate / Very Fast
NAND Flash [40]	Trapped Charge (Floating Gate)	Low/Moderate	<50 Mrad (Si)	High / Slow
PCM (Phase Change) [35]	Chalcogenide Phase Transition	High	>2 Mrad (Si)	Very High / Slow
STT-MRAM [41]	Magnetic Polarization	Very High	>10 Mrad	High / Fast
RRAM [22, 42]	Conductive Filament (Structural)	Very High	TaO _x : >18 Mrad (Si); HfO _x : >7 Mrad (SiO ₂)	Ultra-Low / Fast

Table 2 – Quantitative benchmarking of legacy space-grade processors, commercial edge AI modules, and emerging memristive ISMC architectures.

Processing Architecture	Target Application Domain	Performance (TOPS/DMIPS)	Energy Efficiency (TOPS/W)
BAE RAD750 / LEON4 [6]	Space-Grade General Logic	~400 DMIPS	N/A (Insufficient for AI)
Microchip RTG4 FPGA [32]	Space-Grade DSP / Logic	~0.5 TOPS	<0.1 TOPS/W
NVIDIA Jetson AGX Orin [45]	Terrestrial Edge AI	~275 TOPS	3–5 TOPS/W
Intel Movidius Myriad [48]	Low-Power Edge Vision	~1 TOPS	~1 TOPS/W
Memristive ISMC (RRAM) [6, 19]	On-Board / In-Sensor AI	Highly Scalable	36–146 TOPS/W

At the architecture level, however, memristive in-memory computing is still advancing toward flight qualification, from the first satellite-oriented RRAM subsystem designs [50] to recent interfacial engineering that yields memristors stable up to 700 °C [51]. The following scenarios illustrate how this device-level headway is progressively translated into aerospace applications, at different stages of maturity.

4.1 On-board hyperspectral imaging and cloud detection

A primary operational constraint for Earth Observation (EO) nanosatellites is the high volume of raw data generated by hyperspectral imaging sensors, which frequently exceeds the available downlink Radio Frequency (RF) bandwidth [52]. Satellites often transmit high resolution imagery obscured by atmospheric cloud cover, leading to inefficient use of bandwidth, onboard energy, and ground processing resources [48]. The European Space Agency (ESA) addressed this issue during the PhiSat-1 mission by deploying the “CloudScout” Convolutional Neural Network (CNN) [53, 54]. Operating on an Intel Movidius Myriad 2 Vision Processing Unit (VPU), CloudScout performed on-board image analysis to discard frames with over 70% cloud coverage, achieving 92% accuracy with a 1% false-positive rate. However, using conventional VPUs or COTS FPGAs requires continuous active power and localized radiation shielding due to Single Event Upset (SEU) susceptibility [43, 55].

Deploying the CloudScout algorithm on a memristive In-Sensor Memory Computing (ISMC) architecture allows

the image processing to occur directly at the sensing node [8]. Memristor-based analog crossbars process image arrays in parallel, eliminating data transfer across an external memory bus. Recent hardware implementations of bio-inspired in-sensor computing have demonstrated a reduction in the Energy Delay Product (EDP) by over three orders of magnitude (1 000-fold) compared to traditional von Neumann sensory architectures, drastically accelerating the front-end intelligent sensing pipeline [28]. Furthermore, developing multimodal in-sensor computing through 2D material-based heterojunction optoelectronic synapses enables direct feature computation upon photon capture [8, 56, 57]. This hardware framework provides real-time detection of specific spectral signatures, such as volcanic eruptions, greenhouse gas leaks, and atmospheric particulate matter, enabling autonomous spatial AI inference independent of terrestrial cloud servers or digital accelerators [58].

4.2 Autonomous asteroid navigation and gravimetry

Autonomous navigation and gravimetry are major computational requirements in deep space exploration. Proximity operations near unmapped asteroids require spacecraft to reconstruct three-dimensional topologies and compute irregular gravitational potentials dynamically. During these missions, such as asteroid sample returns or planetary defense kinetic impactors, severe communication latencies prevent ground-in-the-loop control. Consequently, spacecraft must autonomously map ter-

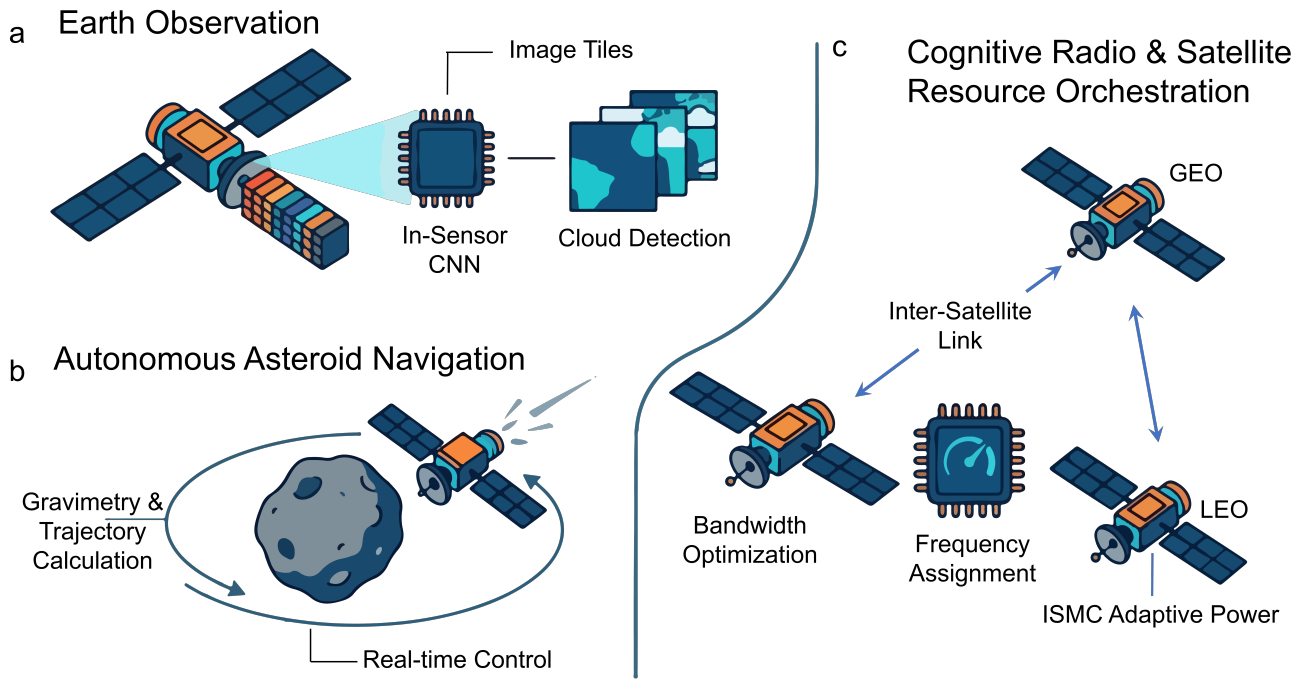


Figure 3 – Applications of memristive spatial AI architectures. (a) Edge sensory processing for cloud detection. (b) Real-time closed-loop control and orbit estimation near celestial bodies. (c) Dynamic spectrum optimization and link parameter assignment in multi-orbit constellations.

rain and model non-spherical gravitational fields in real time to calculate orbital insertions [59, 60]. To support this level of autonomy, machine learning architectures like Sinusoidal Representation Networks (SIRENs) and Guidance & Control Networks (G&CNETs) are used to approximate gravitational fields and generate landing trajectories. Recent research demonstrates the feasibility of porting these neural models onto memristive crossbar accelerators [11]. While traditional Extended Kalman Filtering involves sequential mathematical logic, processing dynamic parameter linearizations directly on analog memristors allows spacecraft to perform real-time parameter estimation and autonomous navigation with lower latency. For instance, hardware-level simulations of asteroid missions demonstrate that by deploying periodic activation functions (SIRENs) and layer-wise temporal averaging on RRAM-based neural networks, the evaluation test loss for guidance and control drops sharply from 0.07 to 0.01, while asteroid geodesy task errors decrease from 0.3 to 0.007, which confirms the stability of this architecture for onboard spatial AI applications. Furthermore, recent algorithm device co-designs utilize memristive spiking neural networks to accelerate real-time trajectory pathfinding, resolving large-scale shortest-path graph queries natively via parallel spike traveling with an exceptional energy efficiency of 517.82 GTEPS/W [61].

4.3 Cognitive radio and satellite resource orchestration

The proliferation of commercial mega-constellations in Low Earth Orbit (LEO) restricts available Radio Frequency (RF) spectrum resources [55]. To mitigate signal interference and ensure transmission quality, future networks require AI-driven Cognitive Radio (CR) systems to allocate spectrum resources [62, 63]. In these systems, memristor-based neural networks process spectral maps to classify signal interference or anomalous users in real-time. Due to their parallel analog computing capabilities, memristive accelerators could perform real-time inference to optimize Inter-Satellite Links (ISL). This would allow the hardware to execute adaptive power allocation, frequency assignment, and multi-beam handovers within microseconds [64, 65]. Consequently, this architecture supports reliable spectrum sharing between primary Geostationary (GEO) and secondary LEO satellites, driving spatial AI resource orchestration without exceeding the limited power budgets of spacecraft or introducing digital processing delays. In contrast to the hardware prototypes and hardware-level simulations described in the preceding scenarios, memristive approaches to cognitive radio and spectrum orchestration remain at an earlier stage of validation, supported primarily by architecture-level proposals [64] and algorithm-level simulation platforms [65].

5. HARDWARE BOTTLENECKS AND SPACE DEPLOYMENT CHALLENGES

While memristive technologies offer substantial theoretical advantages, integrating analog memory arrays into mission-critical space subsystems is limited by several physical and architectural bottlenecks.

5.1 Device non-idealities

While memristive crossbars offer substantial advantages, their practical deployment is constrained by device-level non-idealities arising from the stochastic formation of conductive filaments within amorphous dielectrics [15, 66]. This physical randomness manifests across three distinct dimensions: first, the precise morphology of oxygen vacancy filaments fluctuates with each switching cycle, and lithographic variations prevent uniform resistance across the array. This Device-to-Device (D2D) and Cycle-to-Cycle (C2C) variability, which can reach a 35% coefficient of variation, introduces unpredictable analog read noise into neural network forward inference [44]. Second, once programmed to a specific analog weight, conductive filaments are susceptible to thermodynamic relaxation, where concentration gradients cause atoms to diffuse over time and induce continuous conductance drift [67]. Third, extensive SET/RESET cycling causes structural degradation, resulting in irreversible hardware faults where devices become permanently stuck in High Resistance States (HRS) or Low Resistance States (LRS) [68].

In spatial AI applications, these physical imperfections lead to system-level vulnerabilities. For multi-year deep space missions, continuous thermodynamic conductance drift erodes the pretrained synaptic weights of the neural network, degrading on-board inference accuracy over extended operational timelines [11]. Concurrently, C2C noise and stuck-at defects corrupt real-time sensor processing pipelines. When sensitive control algorithms, such as Guidance & Control Networks (G&CNETs) for autonomous asteroid navigation, are subjected to this analog stochasticity, the network outputs deviate from deterministic precision requirements. Without architectural or algorithmic intervention, this accuracy degradation can cause miscalculations during orbital insertions or hazard mapping, violating the strict safety constraints of aerospace operations.

5.2 Parasitic effects and sneak-path currents

When memristors are arranged in high density, passive crossbar arrays without individual selectors (a 1R configuration), executing a read or write operation on a targeted cell routes unintended currents through adjacent, unse-

lected cells via parallel pathways. This parasitic leakage is defined in circuit design as the sneak-path current [69]. As the physical dimensions of the crossbar scale up to accommodate larger neural network models, the number of alternative parallel pathways increases, expanding the sneak-path distribution across the array [70]. These sneak paths reduce the array's read margin, increasing the computational difficulty for peripheral sensing circuits to distinguish between the High Resistance State (HRS) and Low Resistance State (LRS) of a selected cell. Furthermore, this leakage increases static power consumption, counteracting the primary energy efficiency advantages of the hardware. The propagation of these unintended currents also induces parasitic voltage drops (IR drops) across the metallic interconnects, causing signal attenuation at the far ends of the bitlines and wordlines [71]. For spatial AI architectures requiring deterministic calculations, unmitigated sneak paths distort voltage delivery and restrict the operational scale of passive arrays. In addition to these parasitic effects, the peripheral circuits of large-scale crossbar arrays face another reliability challenge in the space environment: heavy ion Single Event Effects (SEEs). A heavy ion striking the access transistors adjacent to a high resistance state cell can erroneously program it into the low resistance state ($368 \text{ k}\Omega \rightarrow 51 \text{ k}\Omega$) [72], and even radiation-hardened commercial ADCs exhibit a single event transient cross-section of $3.7 \times 10^{-4} \text{ cm}^2$ [73]. Since the number of vulnerable peripheral transistors grows with array size, SEE hardening of these circuits is a prerequisite for system-level reliability.

5.3 Thermal dynamics and 3D integration constraints

To increase computational density per unit area, advanced In-Sensor Memory Computing (ISMC) designs utilize Monolithic 3D Heterogeneous Integration (3D-HI). Vertically stacking sensors, RRAM crossbars, and CMOS peripheral logic shortens the physical distance between sensory nodes and computing cores, minimizing data movement latency and interconnect energy consumption [8]. However, this high packing density introduces thermal management challenges that are amplified in the vacuum of space, where convective heat transfer is absent [74]. Thermal energy generated within the core of a 3D Integrated Circuit (3D-IC) must dissipate solely via conduction toward specialized satellite radiators [75]. Consequently, the densely packed RRAM crossbars executing parallel matrix multiplications generate localized thermal hotspots. Differing Coefficients of Thermal Expansion (CTE) among the stacked heterogeneous semiconductor layers induce thermomechanical stress, which can degrade nanoscale interconnects and lead to layer delamination [76].

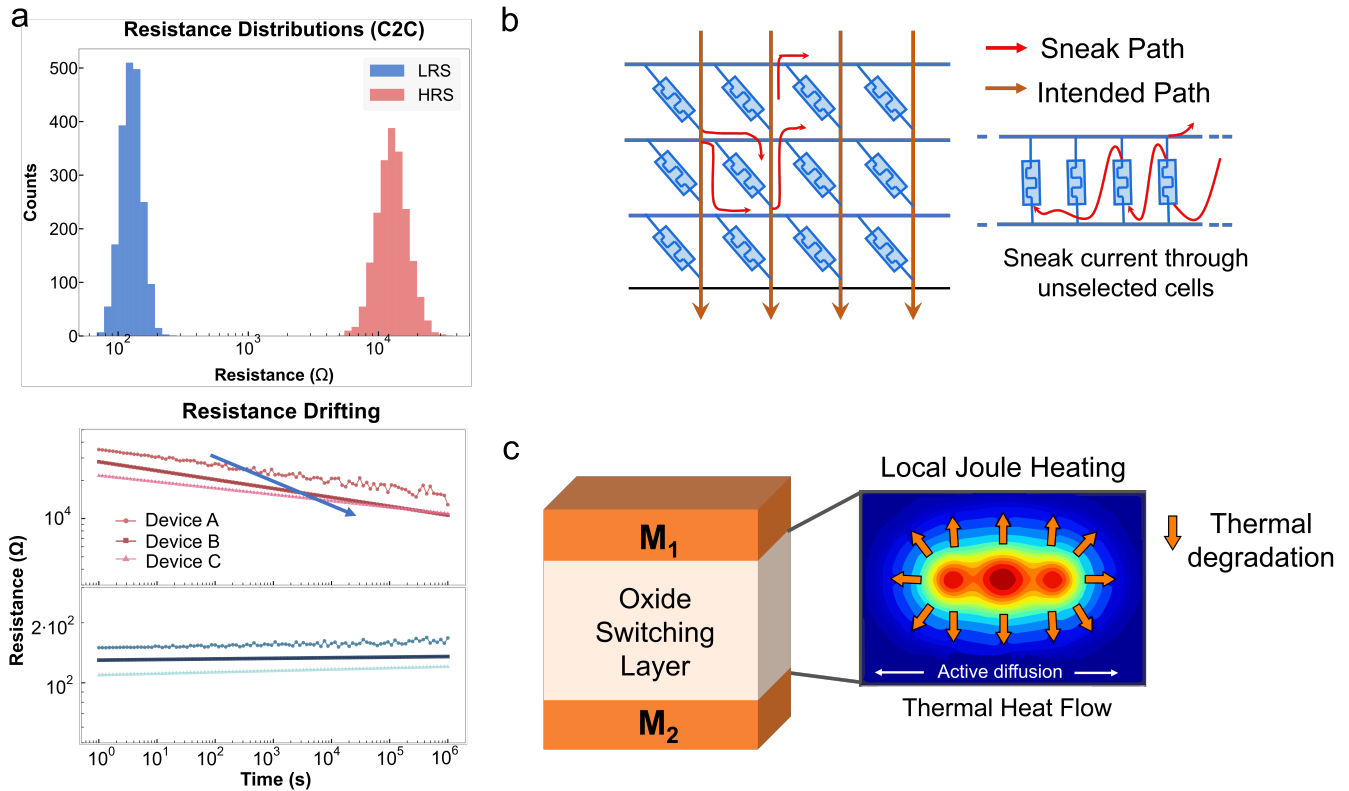


Figure 4 – Primary hardware bottlenecks in RRAM-based architectures. (a) Device-level variations and temporal resistance drifting. (b) Array-level sneak-path leakage where unintended currents bypass target cells and flow through unselected neighbors in passive crossbar configurations. (c) Localized thermal dynamics displaying Joule heating within the oxide switching layer under applied electric fields.

Beyond physical degradation, these unmitigated thermal spikes alter the algorithmic performance of the memristive array. Because memristor state switching depends on thermally-activated ionic mobility, temperature fluctuations directly modify the device's conductance. This thermal conductance shift restricts the precision of multi-level cell configurations. Empirical data indicates that for 4-bit analog RRAMs, thermal drift can exceed the 1 μ S conductance separation margin between adjacent weight states. When executing forward inference for deep learning models, such as ResNet-18, these uncontrolled shifts in synaptic weights distort the network's mathematical mapping, causing classification accuracy to decline from a baseline of 90.64% to negligible levels. Therefore, without conductive cooling solutions or thermal mitigation strategies, the thermal bottlenecks of 3D-HI limit the deployment of high density spatial AI architectures [77].

6. STATE-OF-THE-ART MITIGATION STRATEGIES

To secure the viability of memristive AI accelerators for spaceflight, aerospace researchers and microelectronics engineers have formulated robust hardware-software co-design strategies targeting the aforementioned bottlenecks.

To mitigate parasitic sneak-path currents, passive 1R crossbars can be replaced by active One-Transistor-One-Memristor (1T1R) or high-density One-Selector-One-Memristor (1S1R) architectures [45]. In the 1T1R configuration, a series access transistor functions as a voltage-gated barrier, isolating leakage currents in unselected cells [78]. For large-scale crossbar expansion without the area penalty of bulky CMOS transistors, 1S1R configurations employ highly nonlinear, two-terminal selector devices, such as niobium dioxide (NbO₂) threshold switches. These selectors block low-voltage sneak paths while permitting access at operational switching voltages, reducing sneak-path currents by up to 200 $\times$ to enable 4k $\times$ 4k crossbar scaling [79]. Concurrently, to manage localized heating within 3D-HI computing nodes, Through-Silicon Vias (TSVs) are implemented as vertical thermal conduits. These vias conduct heat from internal tiers toward embedded micro-channel cold plates or Liquid Metal Polymer (LMP) heat spreaders to maintain the array within thermal limits [75]. Beyond the array itself, the peripheral circuits that drive and sense the crossbar also demand radiation hardening: Radiation-Hardened-By-Design (RHBD) comparators based on a redundant latch topology raise the critical charge for upset at an area overhead of approximately 1.4 $\times$, substantially more efficient than Triple Modular Redundancy (TMR), which typically triples area and power and leaves

the majority voter as a potential single point of failure [80]; error-correction coding provides an additional architectural-level safeguard. Such technologies, both array-level topologies and peripheral-circuit hardening, provide the baseline survivability required for hardware operating on spacecraft in the vacuum of space, where convective cooling is absent.

Beyond hardware modifications, software algorithms designed with analog awareness protect against variability and conductance drift. To address programming stochasticity and Device-to-Device (D2D) variation, peripheral circuits can use iterative write-verify feedback loops, applying closed-loop micro-pulses to tune memristor conductance to target values [81, 82]. Furthermore, bit slicing techniques can limit the impact of temporal drift. Instead of mapping a high-precision weight to a single, drift-susceptible memristor, the weight is distributed across multiple lower-precision cells. Consequently, if an individual device undergoes thermodynamic relaxation, only a fraction of the total synaptic weight is altered [83]. For multi-year deep space missions where ground-based recalibration is impossible, this architectural resilience prevents model accuracy degradation and preserves the long-term robustness of the on-board system.

At runtime, stochastic and thermal errors can be managed statistically to meet aerospace reliability requirements. Layer and temporal ensemble averaging introduce algorithmic redundancy; processing inputs through parallel network layers and averaging the analog outputs cancels out uncorrelated read noise and isolated stuck-at defects. In simulated asteroid navigation tasks using SIRENs, combining bit slicing with temporal averaging reduced task loss from 0.3 down to 0.007, approaching high-precision software baselines [11]. Additionally, because localized thermal variations cause correlated conductance drift across adjacent cells, dynamic calibration of peripheral Analog-to-Digital Converters (ADCs) can compensate for temperature fluctuations. Scaling the ADC reference voltages based on real-time die temperature telemetry restores classification accuracy from a 66.4% drop back to a 1.4% degradation at 85 °C [77]. As discussed above, dynamic ADC reference scaling is effective against the correlated, reversible component of drift [77]. However, over multi-year deep-space missions, the accumulated conductance degradation additionally contains an irreversible, cell-by-cell component, endurance cycling and long-term retention progressively shift and broaden the intermediate-level conductance distributions [84], which cannot be reversed by a single global adjustment of the ADC reference. Three complementary approaches have been reported to address this irreversible degradation: improving robustness at the state-assignment level, where storing fewer bits per cell lowers the bit-error rate to zero across all tested radiation intensities [50]; reprogramming or rewriting drifted cells, which reverts radiation and time-induced shifts but re-

mains constrained by limited write endurance [50, 85]; and low overhead digital calibration that compensates drift without rewriting the array, still at the prototype stage [85, 86].

Taken together, the hardware topologies, statistical averaging, and calibration schemes discussed above allow memristive systems to execute latency-critical AI tasks with stable accuracy. It should nevertheless be noted that these mitigation strategies are not cost-free: as with any error-mitigation technique, write-verify schemes, redundant-cell configurations, and on-chip learning architectures improve accuracy or energy efficiency at the price of additional area, energy, or latency overhead [87], which should be weighed against the power and area constraints of a given mission.

7. CONCLUSION

Integrating memristive technologies into spatial AI frameworks addresses the limitations of the conventional von Neumann architecture. By unifying data storage and matrix vector computations at the physical device level, memristive crossbars improve energy efficiency. This architecture allows complex deep learning models, such as hyperspectral cloud detection algorithms and real-time asteroid gravimetry networks, to operate directly on power-constrained orbital platforms. Furthermore, because data retention relies on structural filamentary pathways rather than stored charge, memristors exhibit high tolerance to the Total Ionizing Dose (TID) and Single Event Effects (SEE) that degrade standard CMOS processors in space environments.

However, deploying these analog memory arrays into flight-ready hardware requires addressing native device bottlenecks. The stochastic formation of conductive filaments, temporal conductance drift, and thermal concentrations within 3D integrated circuits limit deterministic operations. Research demonstrates that deploying active array topologies to isolate leakage currents, combined with hardware-aware algorithmic calibrations, such as bit slicing, ensemble averaging, and dynamic ADC scaling, can compensate for these non-idealities while maintaining low power consumption. As fabrication techniques for memristive materials and monolithic CMOS integration methodologies advance, neuromorphic hardware can support the transition from ground-reliant telemetry to decentralized, autonomous space-borne edge computing, expanding the capabilities of next generation deep space exploration.

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