FUNDAMENTAL LIMITS OF HIGH-EFFICIENCY SILICON AND COMPOUND SEMICONDUCTOR POWER AMPLIFIERS IN 100-300 GHZ BANDS

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Abstract *– This paper reviews the requirements for future digital arrays in terms of power amplifier requirements for output power and efficiency and the device technologies that will realize future energy-efficient communication and sensing electronics for the upper millimeter-wave bands (100-300 GHz). Fundamental device technologies are reviewed to compare the needs for compound semiconductors and silicon processes. Power amplifier circuit design above 100 GHz is reviewed based on load line and matching element losses. We present recently presented class-A and class-B PAs based on a InP HBT process that have demonstrated record efficiency and power around 140 GHz while discussing circuit techniques that can be applied in a variety of integrated circuits.*

Keywords – Digital array, high-efficiency, millimeter-wave, power amplifier

1. INTRODUCTION

Frequencies between 100-300 GHz, known as Upper millimeter-Wave (UmmW) bands, offer an opportunity for convergence of communication and sensing systems to support future high-throughput backhaul and radar applications [1]. In particular, frequency bands located at 140 and 220 GHz feature O2 and H2O absorption windows for low propagation loss in outdoor channel environments [2]. Digital array applications in UmmW bands require mature electronic and packaging technologies and previously Integrated Circuits (IC) demonstrated poor power efficiency and higher package costs when compared to lower millimeter-wave (LmmW) bands (28/39/60 GHz). While other bands, including the 60 GHz bands offer substantial bandwidth, the high absorption at 60 GHz prohibits energy efficient operation over more than a kilometer and UmmW offers opportunity for high-bandwidth.

Moreover, the UmmW bands offer shorter wavelength relative to LmmW and this feature allows more Transmit (TX) and Receive (RX) elements within a given aperture area. The array spacing at 140 GHz would be approximately 1 mm and, therefore, a 1cm x 1cm array could host around 100 elements while a 28 GHz array might have only 4 elements in the same aperture area. Consequently, the UmmW beam-former array will contain a relatively large number of steerable elements that might be packed into the small form factor, controlled with independent digitally-controlled Baseband (BB) and Intermediate Frequency (IF), and this poses a large-scale integration challenge that must be solved with unified design that includes IC, packaging, and device technologies.

The large number of array elements in the UmmW array suggests design architecture based on digital array techniques rather than traditional RF beam-forming approaches that leverage signal processing techniques based on massive MIMO (mMIMO) for higher spatial resolution than conventional MIMO systems [3]. Reusing time-frequency resources across multiple users can ultimately support higher spectral efficiency across a network and with the available bandwidth in UmmW devices link capacity might approach 1 Terabit/second [4]. Moreover, a large number of antennas will focus energy into small regions in the space. Thus, in theory, the transmit power can be reduced while maintaining a high Signal-to-Noise Ratio (SNR), resulting in higher spatial energy efficiency. Of course, there is a circuit overhead to generate the RF signals across the mMIMO array which scales linearly with the number of elements. At some point, a larger array incurs substantial power consumption penalties. Early demonstrations of mMIMO in sub-6 GHz based on commercially-available software-defined radios require kilowatts in signal processing [5].

Early work on line-of-sight MIMO in millimeter-wave bands was demonstrated nearly a decade

ago [4]. As millimeter-wave systems are reaching commercial adoption based on RF beam-formers, interest has pivoted into the further capabilities of digital beam-formers in conventional 5G bands for mMIMO and preliminary studies have begun to demonstrate multi-beam test beds [4]. However, the feasibility of mMIMO systems above 100 GHz requires evaluation of the benefit from both signal processing and the short wavelength of the signals, particularly for systems where area is a limitation.

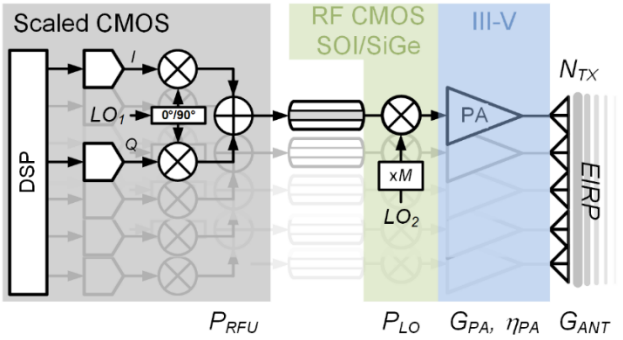

Fig. 1 - Architectural partition for large-scale integration of transmitters in UMMW bands where 2D arrays prohibit direct integration of the full transceiver behind a single antenna element.

The architecture of a UmmW digital beam-former is illustrated in Fig. 1 to move the DSP and Intermediate Frequency (IF) signal generation blocks in scaled CMOS away from the 2D transmit (or receive) front end in an array. An RF upconverter allows the IF (or baseband) to be shifted to the RF band where a Power Amplifier (PA) generates the appropriate output power level. This architecture might be substantially different than a sub-6 GHz or 28 GHz array where the element spacing is relaxed relative to the amount of integration on a single silicon chip and multiple polarizations and even transmit/receive might be fit within a single array site.

This paper reviews the Transmitter (TX) and PA constraints for digital beam-formers that would support future mMIMO deployments and details the output power requirements and how these can be translated into an efficient PA design using commercially available III-V and Si transistor technologies today [6]. Recent work supports the possible rapid improvement in circuit design above 100 GHz that may usher in an era of energy efficient communication and sensing electronics for the UmmW bands. Section 2 will review the digital beam-former architecture and highlight the different demands in the Base Station (BS) and the User Equipment (UE). Section 3 reviews the fundamental limits on efficiency for device technologies above 100 GHz and highlights the transistor improvements. Section 4 discusses advanced III-V transistor nodes and the possibilities in these nodes. Section 5 discusses how attempts to seek optimal transistor embedding networks to improve gain struggle to improve efficiency, and Section 6 presents recent work that has demonstrated how one particular process, InP HBT, has the potential to significantly increase efficiency in the 100-300 GHz bands.

2. DIGITAL BEAM-FORMING

In the UmmW bands, the BS and UE for a communication link would have different requirements for the PA. To produce multiple beams for different users, the digital beam-former in the BS is illustrated in Fig. 1. As opposed to an RF beam-former, each PA is supported by an individual pair of DACs and RF Upconverter (RFU) unit. The architecture translates into higher Peak to-Average Power Ratio (PAPR) requirements in the digital beam-former for the PA. By simulating the sum of random uncorrelated QPSK waveforms associated with several users, the aggregate PAPR asymptotically approaches 12 dB. High PAPR suggests relatively high peak power and linearity requirements for the PA.

The UmmW band poses a unique problem for the packaging of a digital transmit array. To occupy a 2D array site of only 1mm by 1mm, very compact electronic ICs must fit into a 2-Dimensional (2D) array without a 3D packaging solution [7]. More importantly, the power consumption of a UmmW front end is constrained to prevent a substantial thermal load that must be dissipated with the small area with the large numbers of elements.

The PA poses the most significant problem for the energy efficiency of a UmmW digital beam-forming array. While an all-silicon solution might be attractive to integrate the large number of elements, the PA performance in silicon processes is limited in terms of output power and efficiency. Prior work demonstrated single digit efficiency in CMOS and SiGe processes for 15-20 dBm output power in the power amplifier [8][9][10]. With single digit efficiency, the power requirements across 100s of elements are tremendous, particularly given the dense array of power amplifiers at 140 GHz, and lends to an insurmountable heat removal challenge. Consequently, the transmit digital beam-former illustrated in Fig. 1 might include a III-V PA if the

power and efficiency of another device technology supports the requirements.

A notional link between a BS and UE can be mathematically analyzed to understand the digital beam-former power consumption. As more channels are added, the digital beam-former increases the RFU and DAC power linearly. However, the PA output power decreases given a fixed EIRP constraint.

By adding the power consumption of the RFU (which includes DAC and IF signal generation) and the LO power (which includes LO distribution, multiplier, buffer and mixer power consumption), an optimization is found based on basic circuit parameters for the PA (drain) efficiency and the overhead of the per-element RF upconversion.

$$N_{OPT} = \sqrt{\frac{\eta_{MOD} EIRP}{\eta_{PA} G_{ANT} (P_{RFU}+P_{LO})}} \qquad (1)$$

Minimum energy is found when the PA power consumption offsets the overhead power consumption for the RFU and DAC. Not only is the power consumption significantly reduced, the size of the array can be reduced by a factor of two through the smaller number of elements. When we consider this optimization in terms of the number of elements, the optimum output power per element is

$$P_{OUT,OPT} = \frac{\eta_{PA}}{\eta_{MOD}} (P_{RFU} + P_{LO}) \qquad (2)$$

Consequently, the optimum output power is a fraction of the DC power consumed in the RFU and LO based on the PA efficiency.

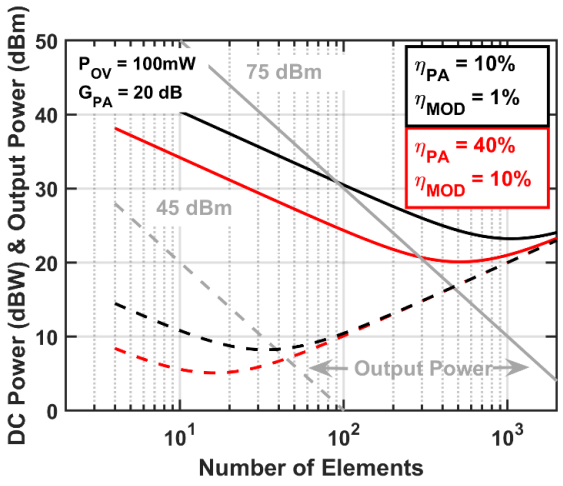

Fig. 2 - Optimization of the number of elements under different EIRP conditions demonstrating the output power per element in dBm and the total array power consumption in dBW. (Assumes G_{ANT} = 5 dB).

As an example, the minimum energy of the TX array is plotted in terms of the number of elements in Fig. 2. A total overhead power consisting of the RFU and LO is assumed to be 100 mW. Additionally, we assume the PA gain is 20 dB. Using current state-of-the-art numbers for the DC to RF efficiency of the modulator and the PA, 1% and 10%, respectively, the base station (EIRP = 75 dBm) is optimized for more than 1000 elements. Moreover, the minimum power is around 220 W. As expected from (2), the output power per PA is around 10 dBm based on the overhead of 100 mW and the efficiency of 10%. On the other hand, if the PA efficiency is improved to 40%, the number of elements reduces (by roughly a factor of 2) but the optimum PA output power increases to around 16 dBm.

On the other hand, the UE (EIRP = 45 dBm) is minimized for 32 elements at a total power of 7 W and output power per element again of 10 dBm. This is the same as the BS since the assumptions in (2) do not change between the BS and UE in this exercise. With improvements in the PA efficiency, the number of elements decreases to 16 elements and the overall power is around 3 W and the average power per element is again 16 dBm. The critical insight is that improvements in efficiency also increase the average output power demands per element.

While these power consumptions for the array might seem high, considering that the BS MIMO beam-former could support more than 100 users (load factor of ¼), the power is amortized by the throughput to each user. If each user receives a 10Gb/s QPSK stream, the overall energy efficiency of each BS beam amounts to around 200 pJ/b which is comparable to the energy efficiency of communications at lower frequency bands. Notably, the UE achieves similar energy efficiency.

Consequently, the PA requirements in the BS or UE are not excessively different nor are they particularly onerous from the standpoint of design compared to LmmW. Most interestingly, the design demands higher output power per element as the efficiency improves and suggests examination of the device technologies for the TX PA. For the purposes of further analysis, we will consider a peak power of 20 dBm as a target per element output power to account for the PAPR.

3. POWER AMPLIFIER CONSTRAINTS

The Power Added Efficiency (PAE) and output power are directly related to properties of the

underlying device technology. The PAE can be expressed in terms of several factors.

$$\mathrm{PAE} = \eta\left(1-\frac{1}{G}\right)\left(1-\frac{V_K}{V_{DD}}\right)\left(\frac{Q_o}{Q_o+Q_t}\right) \quad (3)$$

The PAE depends on the drain efficiency, η, the operating gain of the PA (G), the knee (V_K) and supply voltage (V_{DD}) of the device, and the loss factor for matching the load line of the device to the load impedance, which is expressed above in terms of a impedance transformation quality factor, (Q_t), and passive element quality factor (Q_o). Consequently, the knee voltage relative to the supply voltage imposes a penalty on the available PAE. Additionally, the impedance transformation between the load line of the transistor and the output impedance, e.g. 50 Ohms, reduces the maximum efficiency.

The drain efficiency is determined by the biasing of the PA as well as the harmonic tuning at the load. With only matching of the load line of the device to the load and no additional voltage waveform shaping at the PA output, the gate bias determines the drain efficiency as a class of operation. The conduction angle, θ, of the drain current captures the maximum drain efficiency. When the device is conducting during the entire period (θ = 2π), the transistor is operating in class A with maximum drain efficiency of 50%. If the bias is reduced such that the transistor conducts half the time (θ = π/2), the drain current is class B and the maximum drain efficiency increases to 78%. Unfortunately, the reduced conduction in class B also reduces that transistor gain. Conduction angles between class A and B are referred to as AB.

The available power gain produces a limitation in PAE at bands near the maximum cutoff frequency of the transistor, fmax. For PAs operating above 100 GHz, fmax is often not much larger than the frequency of operation based on currently available device technologies. The available gain is, therefore, limited and the class of operation can be chosen as part of the optimization process.

Fig. 3 indicates the theoretical PAE as a function of the conduction angle. Note that several parameters in (3) are functions of θ, including the shape factor, but also the gain and impedance matching. As the θ reduces from class A to class B and beyond into class C, the PAE increases and then collapses as the gain drops. Notably, several factors in the PAE change as a function of the θ. The load-line impedance increases the loss of the matching network. Moreover, as one moves from LmmW bands at 60 GHz to the UmmW bands at 140 and 220 GHz, the optimum conduction angle moves away from class B bias towards the class A bias. The maximum possible PAE drops from more than 40% to 30% at 140 GHz. When the PA design targets 220 GHz, the maximum PAE becomes around 17%.

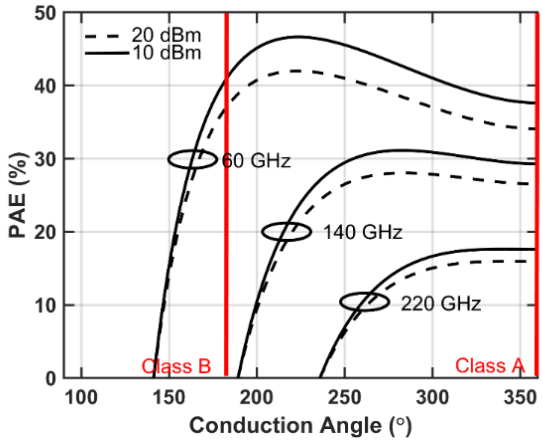

Fig. 3 - PAE as a function of power amplifier conduction angle for upper millimeter-wave frequencies. (f_{max}/f_T = 400 GHz, V_K = 0.7, V_{DD} = 2.5, Q = 10).

We can also compare output power requirements in the previous section for 20 dBm and 10 dBm output power. At 60 GHz, the lower power PA is capable of 7% better efficiency. However, once we reach 220 GHz, the benefit of the reduced output power is smaller. The difference in the PAE achievable with different power levels is attributed to the change in the impedance matching networks and additional losses. Consequently, the dominant performance limitation on PAE for UmmW PAs is the available gain to realize high efficiency at the moderate output powers described in Section 2. We will investigate approaches to improve the gain while optimizing the PAE factors in (3) in the next two sections.

4. UMMW SEMICONDUCTOR TECHNOLOGY COMPARISON

We can study approximate parameters of available processes to understand the PAE limit in (3) with different trade-offs in terms of available gain, voltage handling requirements, and load-line matching conditions for a given matching or output power condition.

We assume that the passive elements have similar quality factor. Table 1 illustrates sample characteristics of different transistor technologies that are available for operation above 100 GHz in III-V and SiGe/SOI CMOS technologies. Si CMOS

technologies at 22-nm and 28-nm might also be considered for the benefit of digital integration but typically do not offer substantially different performance in UmmW bands than 65-nm or CMOS SOI processes and the process parameters are generic. The roadmap of RF-optimized InP HBT processes has been discussed in [11] and [12]. Current 250-nm InP HBT processes are capable of fmax exceeding 600 GHz while being relatively mature with commercial applications. Scaling to 130-nm and beyond can yield fmax exceeding 1 THz. The evolution of SiGe HBTs has also produced remarkable fmax increases that have reached similar speeds to InP [13]. SiGe BiCMOS processes have been optimized for digital and RF performance [14]. Current processes offer several differentiated HBTs in a single process optimized for breakdown and fT/fmax. CMOS SOI processes based on partially depleted SOI substrates have evolved from a digital process to RF-optimized approaches with high-resistivity substrates and RF back end-of-the-line [15]. CMOS and CMOS SOI offer similar supply and knee voltage. The 40-nm GaN HEMT process is described in [16] and offers a 400-GHz fmax. The characteristics of the different processes is summarized in Table 1 with an emphasis on commercially available processes with the highest f_{max}.

Table 1 - Comparison of UMMW semiconductor device technologies

Technology	f_{max} (GHz)	V_{SUP} (V)	V_K (V)	I_{MAX} (A/mm)	P_{RF} (W/mm)	R_{LL} (Ωmm)
InP HBT	600	2.5	0.7	3	1.4	1.2
SiGe HBT	450	1.3	0.5	2.2	0.44	0.7
CMOS	310	1.1	0.3	1	0.2	1.6
GaN HEMT	400	12	2	1.6	4.0	12.5

Based on the supply voltage and the knee voltage, the maximum output power can be calculated from $P_{RF} = \frac{1}{4}(V_{DD} - V_K)I_{MAX}$ while the load-line resistance is $R_{LL} = 2(V_{DD} - V_K)/I_{MAX}$. The RF output power and load-line resistance is shown in Table 1 when normalized to 1 mm. The high supply voltage of the GaN HEMT due to breakdown characteristics suggests high power density and load-line resistance relative to the other processes.

We compare these technologies in two different ways to understand device selection for high efficiency. On one hand, we would choose a device that offers a load line close to 50 Ohm to avoid loss in the matching network. On the other hand, we consider a power target and investigate the required size of the transistor. A larger transistor introduces design challenges to distribute the RF power into and out of the transistor. A large device, relative to the wavelength, typically incurs a drop in the potential fmax. At 140 GHz, a device width/length of more than 200 um would pose significant conditions to distribute the signal.

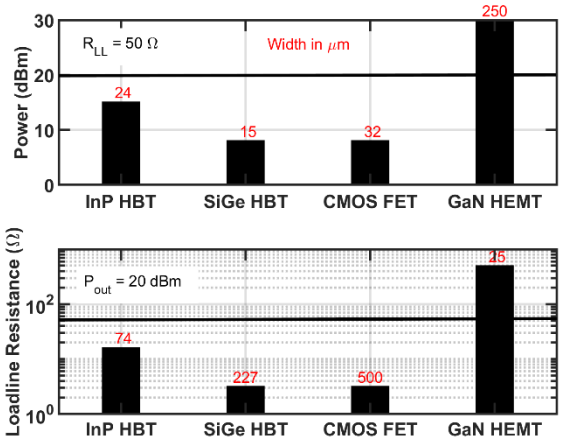

Fig. 4 - Comparison of process technology trade-offs under fixed resistance (50 Ohm) and fixed power (20 dBm) conditions.

First, to minimize the loss of the impedance matching to the load line, we might choose the device geometry (i.e. width) to provide a 50 Ohm load line. The top plot in Fig. 4 indicates the output power that is developed by each device technology. For instance, the InP process will produce 15 dBm while the SiGe process will produce roughly 6 dBm. The GaN HEMT would deliver around 30 dBm output power. For a 20-dBm target power outlined in Section 2, the InP HBT and GaN HEMT are closest to the target for a 50-Ohm match.

Table 2 - Theoretical efficiency bounds for 20 dBm output power at 140 GHz

Technology	InP HBT	SiGe HBT	CMOS FET	GaN HEMT
PAE (Q = 1000)	45%	34%	32%	43%
PAE (Q = 10)	39%	24%	23%	34%
Conduction Angle	203°	222°	260°	232°

Second, we might also compare the technologies for a fixed output power such as 20 dBm in Fig. 4. The device presenting a load-line matching condition closest to 50 Ohms is the most desirable from the standpoint of PAE. Notably, the InP HBT is the best choice as GaN HEMT presents a large load-line

resistance while a CMOS FET is a very low load-line matching.

Based on these process parameters and the analysis of dependence on conduction angle, a preliminary estimate of the PAE can be gathered for different technologies in Table 2 along with the optimal conduction angle. These values were calculated based on equation (3) and searching for the maximum PAE versus conduction angle as shown from Fig. 3. Since both the shape factor, gain, and impedance transformation depend on conduction angle, we must consider all these factors to understand the class of operation that will achieve the highest PAE. The PAE is computed for a passive quality factor of 10 and 1000. Notably, InP can theoretically reach more than 40% efficiency with a deep class AB/B bias while GaN might approach similar efficiency. Silicon processes should be able to exceed 30%.

5. THEORETICAL COMPARISONS AGAINST PUBLISHED WORK

To compare the insights into the device performance bounds on published PAs above 100 GHz, we surveyed PA results from all published work including CMOS, SOI CMOS, SiGe HBTS, InP HBTs, GaN HEMTs, and GaAs mHEMTs during the previous two decades to establish trends and future development possibilities for more efficient radio and millimeter-wave systems in the UmmW (100-300 GHz) band.

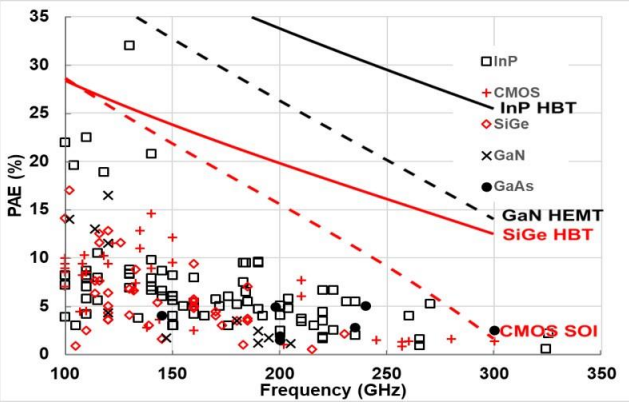

Fig. 5 - PAE versus frequency for PAs in the 100-300 GHz range. The solid and dashed lines indicate the theoretical bounds for the various technologies described in Table 2 as a funtion of frequency.

The PAE theoretical trend is illustrated in Fig. 5 as the solid and dashed lines and indicates that across this band InP HBTs hold significant promise for high PAE compared to other technologies. Above 100 GHz, recent work based on a class-B biased InP HBT has reported 32% efficiency and the design of this PA will be discussed in the next section [17]. Other recent work based on class-A InP HBT PAs has achieved higher output power (20 dBm) at slightly lower efficiency (20%) [16]. The InP HBT has consistently demonstrated the highest efficiency to 300 GHz due to the high fmax and, consequently, gain. Additionally, the InP HBT has a reasonable load-line matching condition for moderate power levels. This feature has been used to demonstrate wideband PAs above 100 GHz to cover waveguide bands [19][20].

For bands below 150 GHz, GaN, SiGe, CMOS have also been demonstrating promising results and could with future circuit and device development push beyond 20% PAE. Above 200 GHz, there remains no clear discrimination between the PAE of the various technologies at this point in time.

The significant gap between the theoretical bounds and the measured PAs raises substantial questions about the potential for practical high efficiency PAs and motivates the central theme of this paper. There are several explanations for the theoretical/measured gap. First, the gain near compression drops for most device technologies and, therefore, a maximum gain calculated from extrapolating the f_{max} is likely not accurate at high-frequency. For example, InP HBTs have different f_{max} based on the device load line. Second, modeling of transistors above 100 GHz is not extremely accurate due to the lack of direct model verification through load pull and other conventional PA design techniques. Effects, such as source/emitter inductance, impact the available gain. Additionally, passives are typically more lossy than anticipated due to the higher series resistance due to current crowding at high frequencies and the skin effect. Vias between metal layers or thru-substrate vias also play a dramatic role in the loss of passives above 100 GHz.

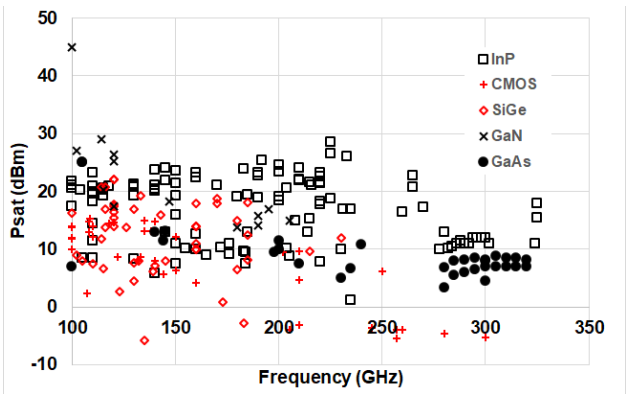

Fig. 6 - Psat versus frequency for PAs in the 100-300 GHz range

The saturated output power is plotted over the UmmW band in Fig. 6. The highest output power is demonstrated with GaN HEMTs up to 140 GHz and InP HBTs above 140 GHz. The rapid drop in power for GaN is due to the limited fmax of the technology. Optimizing GaN HEMTs for high-breakdown tends to also compromise the gate-drain capacitance parasitics that impact millimeter-wave performance. Recent work on N-polar GaN may offer new device physics for millimeter-wave operation [21]. Above 250 GHz, the InP HBT and GaAs mHEMT stand out as the only technologies that generate reasonable output power. SiGe has provided competitive performance in bands between 100 and 200 GHz [9]. Silicon technologies have to date only offered very limited power above 200 GHz. Recent work on Gmax-boosted approaches has pushed the output power towards 10 dBm with limited efficiency [22].

6. AN INP UMMW POWER AMPLIFIER

To demonstrate a high-efficiency PA design above 100 GHz, we have demonstrated circuit design techniques to maximize efficiency based on the 250-nm InP HBT process with f_{max} of approximately 600 GHz. As described previously, this InP HBT process offers a PAE as high as 45% due to 1) the high fmax and 2) load-line matching conditions close to 50 Ohms for an output power of 15 dBm.

Theoretically, the fmax is invariant to the choice of CE or CB configuration. While Common-Emitter (CE) amplifiers are conventionally used in PA design, we compare the MAG of CE and Common-Base (CB) amplifiers in the InP HBT process in Fig. 7 over a range of collector bias conditions at 140 GHz and 220 GHz. Generally, we observe that the gain remains relatively high in all cases but sharply reduces below a certain current density threshold. This substantial reduction in gain occurs when the K stability factor becomes imaginary. Over a range of collector biases between 0.1 mA/um and 3 mA/um (Imax), the CB provides 5dB higher than the CE transistor at both frequency bands. At 140 GHz, the CB provides higher gain close to the class-B biasing condition (Ic of zero) and the gain increases slightly as we shift to class A. The additional gain allows optimization for class-B operation in CB that would not be possible in CE.

Examining the 220 GHz operation, the CB gain drops 2 dB relative to 140 GHz. However, the gain of the CE transistor drops substantially (4 dB) as the desired collector bias shifts towards class-A. The gain at 220 GHz is 7 dB higher for the CB compared to the CE stage.

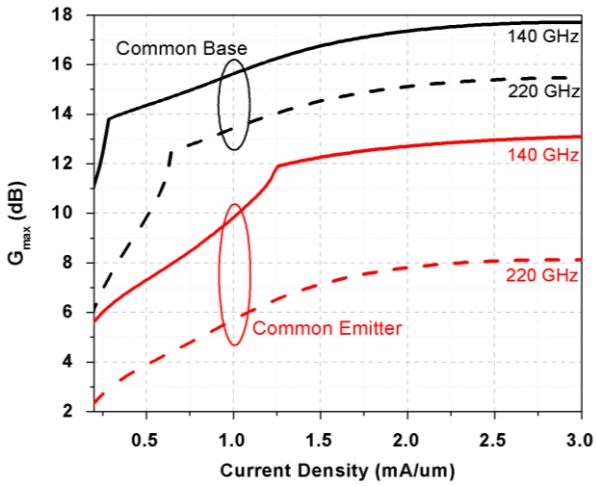

Fig. 7 - Common-base versus common-emitter for a constant collector-emitter voltage for a 0.25um InP HBT process.

The CB HBT provides higher MAG over the millimeter-wave band since the feedback parasitics in the CB amplifier are due to the collector-emitter capacitance, CCE, compared to the larger collector-base capacitance, CCB. Feedback current in the CB HBT is therefore much smaller than in the CE topology and the PA is unconditionally stable without additional stabilization. Base inductance typically impacts the stability of the CB configuration; however, the InP HBT process allows that the base can be directly connected to ground to eliminate any bypass capacitance requirement to produce an AC ground at the base node and the potential base inductance to connect to the bypass capacitor.

The InP HBT offers a physics-based scalable model that allows accurate load pull simulation of the CB device. A 4-finger by 4um (16 um total) CE or CB HBT emitter length produces a 100-Ohm load-line impedance for maximum gain and efficiency. Based on this transistor periphery, the output power, PAE, and gain at peak PAE for the CE and CB amplifier are plotted at 140 GHz in Fig. 8 as a function of the quiescent collector current (normalized by length) under the condition of fixed 2.5-V collector-emitter voltage. Note that the DC current differs significantly from the quiescent current as the PA shifts from class-B to class-A where the ratio of IDC/IQ approaches unity.

The peak output power is 16 dBm at class A for CE and drops to around 14 dBm under the class B bias. The CB configuration produces similar or slightly lower output power than the CE amplifier. Both

configurations indicate identical PAE, which points to an invariance between CE and CB, that ranges from 46% in deep class AB and drops to 35% at class A. The gain of the PA at peak efficiency demonstrates that the CB offers significantly more gain than CE. Consequently, the CE has higher collector efficiency under the range of quiescent collector currents than CB but the higher gain of CB results in similar PAE.

The schematic of the pseudo-differential, common-base class-B PA is illustrated in Fig. 9 along with a chip microphotograph of the stage. The class-B voltage bias is provided to the emitter through the balun. The PA occupies an area of 0.4mm by 0.5mm to easily fit with the 140 GHz the grid spacing.

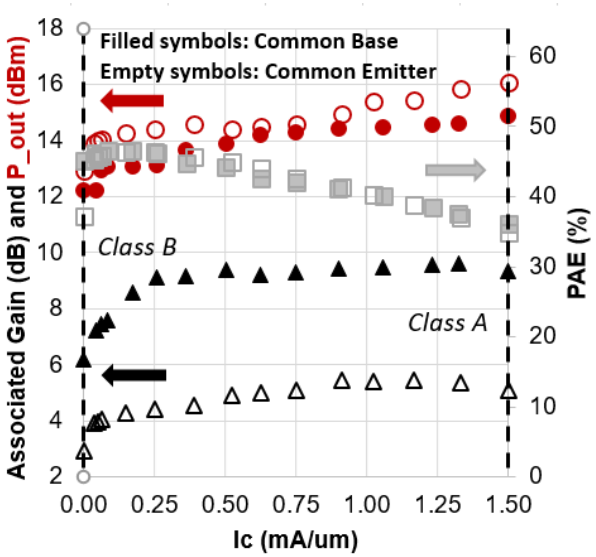

Fig. 8 - Gain, output power, and PAE at 140 GHz as a function of the quiescent collector current for the common-emitter and common-base amplifier for Vce = 2.5 V.

For CB HBTs, the ratio of impedance seen into the collector and at the output of the emitter is related directly to the power gain when IE ~ IC for sufficiently large. To increase the output power, two common-base stages are used as a pseudo-differential output PA. A low-loss sub-quarter wavelength balun was used at the input and the output to match the pseudo-differential PA at the input and output [7][23]. The balun places constraints on the maximum gain that can be realized from a CB amplifier. To provide 6 dB gain, we choose the impedance of emitter port to be close to 25 and for the 100-Ohm collector impedance. A series inductor at the output transforms the load impedance to 50 Ohms.

Fig. 10 plots the PAE and gain as a function of Pout at 130 GHz at a class-B collector bias current density of 203uA/um.

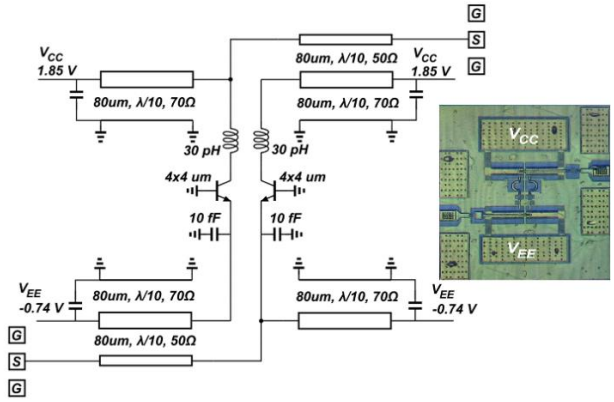

Fig. 9 – Pseudo-differential, common-base InP HBT class-B PA at 140 GHz. The area of the die on the right is 0.4 x 0.5 mm.

The peak PAE occurs at 0.3 dB higher output power. The PA exhibits a peak gain of 7 dB which occurs at Pout of 13 dBm with 1 dB of gain expansion due to the class-B biasing. The output loss of the matching network was measured through test structures to be around 1dB which raises questions about why the measured class-B gain is less than the maximum available gain indicated in Fig. 7. The explanation is partially explained when referring back to Fig. 8 which plotted the gain associated with the common-base device under the matching conditions for high efficiency. Here, the common-base device has only around 9 dB of gain near the class-B bias, corroborating the measured PA operating gain.

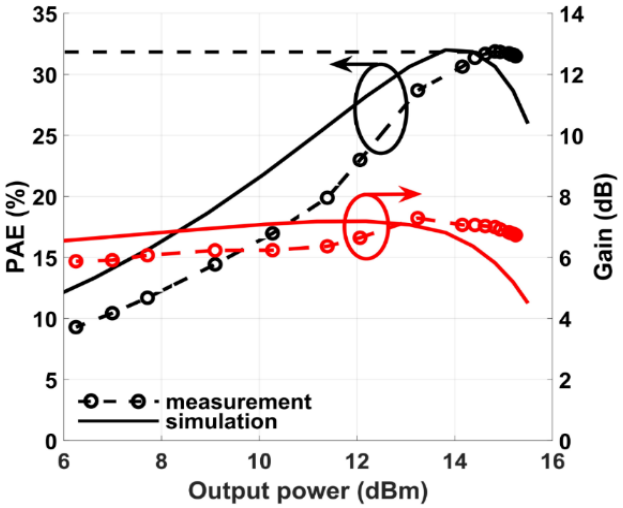

Fig. 10 - PAE and gain as a function of output power for VCC = 2.5 V at 130 GHz. From [15].

The PA achieves 32% peak PAE with 15.3-dBm saturated output power. The 1-dB power bandwidth covers 122 GHz to 146 GHz and is consistent with the measured 3-dB bandwidth from the S-parameters. The input power across the band is calibrated between 8 dBm and 8.7 dBm with variation due to the probe loss variation over the band.

To achieve higher output power, recent work has also investigated low-loss power combining from PA cells designed for high power. Fig. 11 illustrates the 8-way combined power amplifier, where each PA is based on common-base, class-A stages [24]. As opposed to the previous design where the power was combined through pseudo-differential stages (Fig. 10), power combining across two CB HBTs is performed to prevent a large emitter length device (lower left of Fig. 11). The output power combiner must be low loss for high PAE and compact for a small die area. While Wilkinson combiners are broadband, an 8:1 Wilkinson combiner requires 14 λ/4 transmission-lines with lossy, high-impedance lines. The proposed combiner is designed for a 50-Ω load without including the shunt inductive lines tuning Ccb. At the PA output, short 50-Ω transmission line sections (TL1) combine the outputs of the two 4×6um cells. At each consecutive level of combining, the characteristic impedance is divided in half, resulting in wider transmission lines and lengths that are minimized for smallest losses. A final impedance transformation from 12.5Ω to 50Ω requires a λ/4 line (TL3) having 35Ω characteristic impedance.

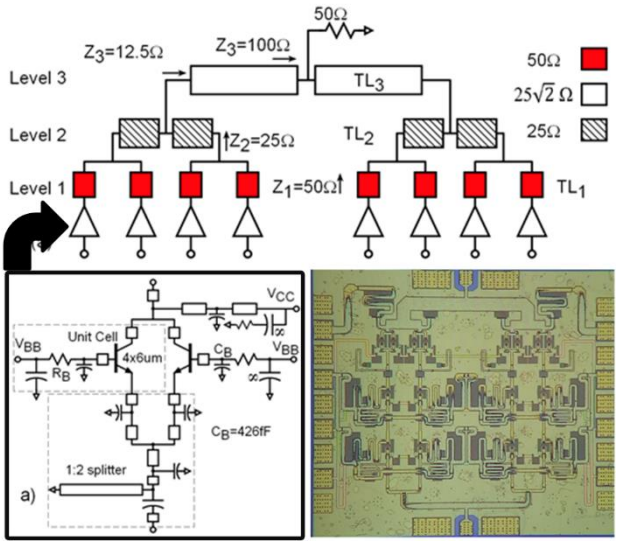

Fig. 11 - Power-combined, common-base InP HBT class-A PA at 140 GHz. The area is 1.23mm× 1.09mm.

Fig. 12 plots the PAE and gain as a function of Pout at 140 GHz at a class-A collector bias current density of 1.14mA/um. The three-stage PA has 23 dBm peak power with 17.8% Power Added Efficiency (PAE) and 16.5dB associated large-signal gain at 131GHz. At 131GHz, the small-signal gain is 21.9dB. The small-signal 3dB-bandwidth is 125.8-145.8GHz.

While the class-B PA and power-combined class-A PA offer state-of-the-art performance for high-efficiency and high-power, we continue to see opportunities to continue improving the PAE towards 40% at power levels exceeding 20 dBm.

While this work has not addressed trade-offs between power combining and device scaling in single-ended and differential PA designs, there remain significant research insights to be gathered about the losses and area efficiency of the various approaches. The power combiners in Fig. 11 occupy substantial area that might not satisfy the area constraints in a digital beam-former. Nonetheless, PA cells that are designed for a 50 Ohm load can be less risky than attempting to scale the device to meet similar power requirements.

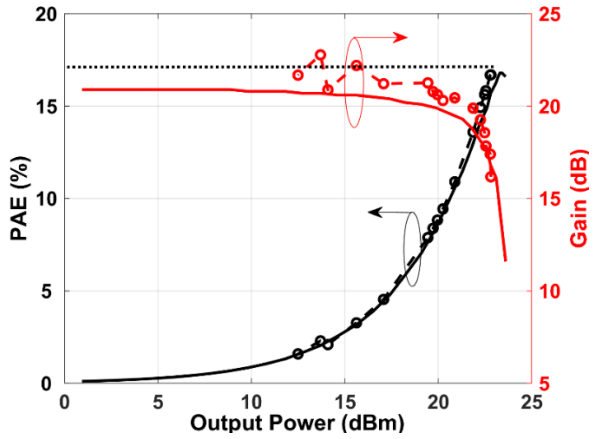

Fig. 12 - PAE and gain as a function of output power for VCC = 2.43 V at 140 GHz. From [28].

7. CONCLUSION

This paper has reviewed the requirements for power amplifiers in digital beam-forming arrays in frequency bands between 100 and 300 GHz. Efficiency will play a critical role in reducing the thermal load for front-end packaging due to high power density. We review the optimization of PAs in gain-limited operation and available device technologies above 100 GHz for PAs to construct PAE bounds on efficiency and compare recent published work to these bounds to demonstrate the potential for future research. Recent demonstrations of class-A and class-B power amplifiers in the 120-140 GHz range have set records for efficiency at 20% and 30%, respectively, which were substantial improvements over prior work. Further improvements in efficiency above 100 GHz are possible in all technologies and the frequency bands between 100-300 GHz may be as energy efficient as lower millimeter-wave bands while offering support of massive MIMO.

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REFERENCES

[1] M. J. W. Rodwell, "100-340GHz Spatially Multiplexed Communications: IC, Transceiver, and Link Design," Signal Processing Advances in Wireless Communications (SPAWC), Cannes, France, 2019, pp. 1-5.

[2] "CCIR Doc. Rep. 719-3,"Attenuation by Atmospheric Gases," ITU 1990."

[3] E. G. Larsson et al., ''Massive MIMO for next generation wireless systems,'' IEEE Communications Magazine, vol. 52, no. 2, pp. 186–195, Feb. 2014.

[4] E. Torkildson et al., "Indoor Millimeter Wave MIMO: Feasibility and Performance," IEEE Trans. on Wireless Communications, vol. 10, no. 12, pp. 4150 – 4160, Nov. 2011.

[5] L. Kuai et al. "A N260 Band 64 Channel Millimeter Wave Full-Digital Multi-Beam Array for 5G Massive MIMO Applications," IEEE Access, August 2020.

[6] J. Buckwalter et al. "Prospects for High-Efficiency Silicon and lll-V Power Amplifiers and Transmitters in 100-300 GHz Bands," Custom Integrated Circuits Conference (CICC), Austin, TX, 2021.

[7] M. Bao, Z. S. He and H. Zirath, "A 100–145 GHz Area-efficient Power Amplifier in a 130 nm SiGe Technology," 12th European Microwave Integrated Circuits Conference (EuMIC), Nuremberg, 2017, pp. 277-280.

[8] H. Lin and G. M. Rebeiz, "A 110–134-GHz SiGe Amplifier with Peak Output Power of 100-120 mW," IEEE Transactions on Microwave Theory and Techniques, vol. 62, no. 12, pp. 2990-3000, Dec. 2014.

[9] S. Daneshgar and J. Buckwalter, "Compact Series Power Combining Using Subquarter-Wavelength Baluns in Silicon Germanium at 120 GHz," IEEE Transactions on Microwave Theory and Techniques, vol. 66, no. 11, pp. 4844-4859, Nov. 2018.

[10] D. Simic and P. Reynaert, "A 14.8 dBm 20.3 dB Power Amplifier for D-band Applications in 40 nm CMOS," IEEE Radio Frequency Integrated Circuits Symposium (RFIC).

[11] M. Rodwell et al. "InP Bipolar ICs: Scaling Roadmaps, Frequency Limits, Manufacturable Technologies," Proceedings of the IEEE, vol. 96, no. 2, pp. 271-287, Feb. 2008.

[12] M. Urteaga et al., "InP HBT Technologies for THz Integrated Circuits," Proceedings of the IEEE, vol. 105, no. 6, pp. 1051-1068, June 2017.

[13] J. Böck et al., "SiGe HBT and BiCMOS process integration optimization within the DOTSEVEN project," IEEE Bipolar/BiCMOS Circuits and Technology Meeting – BCTM, October 2015.

[14] R. A. Camillo-Castillo et al., "SiGe HBTs in 90nm BiCMOS technology demonstrating 300GHz/420GHz fT/fMAX through reduced Rb and Ccb parasitics," IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM) 2013.

[15] O. Inac et al., "45-nm CMOS SOI Technology Characterization for Millimeter-Wave Applications," IEEE Transactions on Microwave Theory and Techniques, vol. 62, no. 6, pp. 1301-1311, 2014.

[16] K. Shinohara et al., "220 GHz fT and 400 GHz fmax in 40-nm GaN DHHEMTs with re-grown Ohmic," in IEDM Tech. Dig., 2010, pp. 672-675.

[17] K. Ning et al., "A 130-GHz Power Amplifier in a 250-nm InP Process with 32% PAE," 2020 IEEE Radio Frequency Integrated Circuits Symposium (RFIC) June 2020.

[18] A. Ahmed et al., "A 140GHz power amplifier with 20.5dBm output power and 20.8% PAE in 250-nm InP HBT technology," IEEE/MTT-S International Microwave Symposium (IMS) June 2020.

[19] Z. Griffith et al. "A 115–185 GHz 75–115 mW High-Gain PA MMIC in 250-nm InP HBT," 2019 49th European Microwave Conference (EuMC).

[20] Z. Griffith, M. Urteaga and P. Rowell, "A 140-GHz 0.25-W PA and a 55-135 GHz 115-135 mW PA, High-Gain, Broadband Power Amplifier MMICs in 250-nm InP HBT," 2019 IEEE MTT-S International Microwave Symposium (IMS), Boston, MA, USA, 2019, pp. 1245-1248.

[21] B. Romanczyk et al., "N-Polar GaN-on-Sapphire Deep Recess HEMTs With High W-Band Power Density, IEEE Electron Device Letters, vol. 41, no. 11, November 2020.

[22] H. Bameri and O. Momeni, "An Embedded 200 GHz Power Amplifier with 9.4 dBm Saturated Power and 19.5 dB Gain in 65 nm CMOS," IEEE Radio Frequency Integrated Circuits Symposium (RFIC), June 2020.

[23] H-C Park et al., "Millimeter-Wave Series Power Combining Using Sub-Quarter-Wavelength Baluns," IEEE Journal of Solid-State Circuits, vol. 49, no. 10, pp. 2089-2102, October 2014.

[24] A. Ahmed et al., "A 200mW D-band Power Amplifier with 17.8% PAE in 250-nm InP HBT Technology," 2020 15th European Microwave Integrated Circuits Conference (EuMIC).

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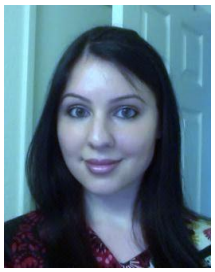

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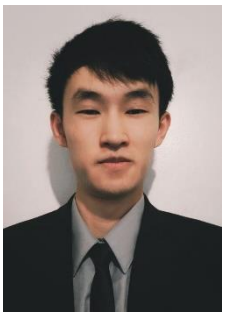

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