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ITU-T G.707

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SERIES G: TRANSMISSION SYSTEMS AND MEDIA

Digital transmission systems – Terminal equipments – General

Network node interface for the synchronous digital hierarchy (SDH)

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ITU-T RECOMMENDATION G.707

NETWORK NODE INTERFACE FOR THE SYNCHRONOUS DIGITAL HIERARCHY (SDH)

Summary

This Recommendation is a merged revised version of Recommendations G.707, G.708 and G.709 that were approved in Helsinki (03/93) by the WTSC.

This Recommendation provides the requirements for the STM-N signals at the Network Node Interface of a synchronous digital network, including B-ISDN in terms of:

– bit rates;

– frames structures;

– formats for mapping and multiplexing PDH and ATM elements;

– functionalities of the overheads.

Source

ITU-T Recommendation G.707 was revised by ITU-T Study Group 15 (1993-1996) and was approved under the WTSC Resolution N°. 1 procedure on the 19th of March 1996.

FOREWORD

ITU (International Telecommunication Union) is the United Nations Specialized Agency in the field of telecommunications. The ITU Telecommunication Standardization Sector (ITU-T) is a permanent organ of the ITU. Some 179 member countries, 84 telecom operating entities, 145 scientific and industrial organizations and 38 international organizations participate in ITU-T which is the body which sets world telecommunications standards (Recommendations).

The approval of Recommendations by the Members of ITU-T is covered by the procedure laid down in WTSC Resolution No. 1 (Helsinki, 1993). In addition, the World Telecommunication Standardization Conference (WTSC), which meets every four years, approves Recommendations submitted to it and establishes the study programme for the following period.

In some areas of information technology which fall within ITU-T's purview, the necessary standards are prepared on a collaborative basis with ISO and IEC.

NOTE

In this Recommendation, the expression "Administration" is used for conciseness to indicate both a telecommunication administration and a recognized operating agency.

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Introduction

Since they have first been approved Recommendations G.707, G.708 and G.709 have formed together a coherent set of documents containing the basic specifications for the development of Synchronous Digital Hierarchy Network Node Interfaces. While revising these three Recommendations, ITU-T have brought quite a number of changes (new features have been added, original ones have been differently specified) to the documents. It has therefore been felt necessary to restructure the Recommendations and the solution that consisted of merging them in a single Recommendation has been favoured. This has led to developing a new G.707 Recommendation with the aim of removing the redundancy contained in some clauses of G.708 and G.709 and with the intention of facilitating the access to the information contained herein.

Recommendation G.707

NETWORK NODE INTERFACE FOR THE SYNCHRONOUS DIGITAL HIERARCHY (SDH)

(revised in 1996)

1 Scope

Network Node Interface (NNI) specifications are necessary to enable interconnection of Synchronous Digital Hierarchy (SDH) networks elements for the transport of different types of payloads.

Therefore, this Recommendations specifies:

– the bit rates for STM-N signals;

– the frames structures for STM-N signals;

– the formats for mapping and multiplexing PDH and ATM elements into an STM-N frame;

– the functionalities to be implemented in the different overheads of an STM-N frame;

at the NNI of a synchronous digital network, including B-ISDN.

2 References

The following Recommendations and other references contain provisions which, through reference in this text, constitute provisions of this Recommendation. At the time of publication, the editions indicated were valid. All Recommendations and other references are subject to revision: all users of this Recommendation are therefore encouraged to investigate the possibility of applying the most recent edition of the Recommendations and other references listed below. A list of the currently valid ITU-T Recommendations is regularly published.

– CCITT Recommendation G.702 (1988), *Digital hierarchy bit rates*.

– CCITT Recommendation G.703 (1991), *Physical/electrical characteristics of hierarchical digital interfaces*.

– ITU-T Recommendation G.704 (1995), *Synchronous frame structures used at 1544, 6312, 2048, 8448 and 44 736 kbit/s hierarchical levels*.

– ITU-T Recommendation G.783 (1994), *Characteristics of Synchronous Digital Hierarchy (SDH) equipment functional blocks*.

– CCITT Recommendation G.802 (1988), *Interworking between networks based on different digital hierarchies and speech encoding laws*.

– ITU-T Recommendation G.803 (1993), *Architectures of transport networks based on the Synchronous Digital Hierarchy (SDH)*.

– ITU-T Recommendation G.831 (1993), *Management capabilities of transport networks based on Synchronous Digital Hierarchy (SDH)*.

– ITU-T Recommendation G.957 (1995), *Optical interfaces for equipments and systems relating to the synchronous digital hierarchy*.

– ITU-T Recommendation I.432 (1993), *B-ISDN User-Network Interface – Physical layer specification*.

– ITU-T Recommendation O.181 (1996), *Equipment to assess error performance on STM-N interfaces*.

– ITU-R Recommendation F.750, *Architectures and functional aspects of radio-relay systems for SDH based networks*.

– ITU-R Recommendation S.1149, *Network architecture and equipment functional aspects of digital satellite systems in the FSS forming part of SDH transport networks*.

3 Terms and definitions

For the purposes of this Recommendation, the following definitions apply.

3.1 synchronous digital hierarchy (SDH): The SDH is a hierarchical set of digital transport structures, standardized for the transport of suitably adapted payloads over physical transmission networks.

3.2 synchronous transport module (STM): An STM is the information structure used to support section layer connections in the SDH. It consists of information payload and Section Overhead (SOH) information fields organized in a block frame structure which repeats every 125 µs. The information is suitably conditioned for serial transmission on the selected media at a rate which is synchronized to the network. A basic STM is defined at 155 520 kbit/s. This is termed STM-1. Higher capacity STMs are formed at rates equivalent to N times this basic rate. STM capacities for N=4, N=16 and N=64 are defined; higher values are under consideration.

The STM-1 comprises a single Administrative Unit Group (AUG) together with the SOH. The STM-N contains N AUGs together with SOH. The STM-N hierarchical bit rates are given in 6.3.

3.3 virtual container-n (VC-n): A Virtual Container is the information structure used to support path layer connections in the SDH. It consists of information payload and Path Overhead (POH) information fields organized in a block frame structure which repeats every 125 or 500 µs. Alignment information to identify VC-n frame start is provided by the server network layer.

Two types of Virtual Containers have been identified.

– Lower order Virtual Container-n: VC-n (n=1, 2, 3)

  This element comprises a single Container-n (n=1, 2, 3) plus the lower order Virtual Container POH appropriate to that level.

– Higher order Virtual Container-n: VC-n (n=3, 4)

  This element comprises either a single Container-n (n=3, 4) or an assembly of Tributary Unit Groups (TUG-2s or TUG-3s), together with Virtual Container POH appropriate to that level.

3.4 administrative unit-n (AU-n): An Administrative Unit is the information structure which provides adaptation between the higher order path layer and the multiplex section layer. It consists of an information payload (the higher order Virtual Container) and an Administrative Unit pointer which indicates the offset of the payload frame start relative to the multiplex section frame start.

Two Administrative Units are defined. The AU-4 consists of a VC-4 plus an Administrative Unit pointer which indicates the phase alignment of the VC-4 with respect to the STM-N frame. The AU-3 consists of a VC-3 plus an Administrative Unit pointer which indicates the phase alignment of the VC-3 with respect to the STM-N frame. In each case the Administrative Unit pointer location is fixed with respect to the STM-N frame.

One or more Administrative Units occupying fixed, defined positions in an STM payload are termed an Administrative Unit Group (AUG).

An AUG consists of a homogeneous assembly of AU-3s or an AU-4.

3.5 tributary unit-n (TU-n): A Tributary Unit is an information structure which provides adaptation between the lower order path layer and the higher order path layer. It consists of an information payload (the lower order Virtual Container) and a Tributary Unit pointer which indicates the offset of the payload frame start relative to the higher order Virtual Container frame start.

The TU-n (n=1, 2, 3) consists of a VC-n together with a Tributary Unit pointer.

One or more Tributary Units, occupying fixed, defined positions in a higher order VC-n payload is termed a Tributary Unit Group (TUG). TUGs are defined in such a way that mixed capacity payloads made up of different size Tributary Units can be constructed to increase flexibility of the transport network.

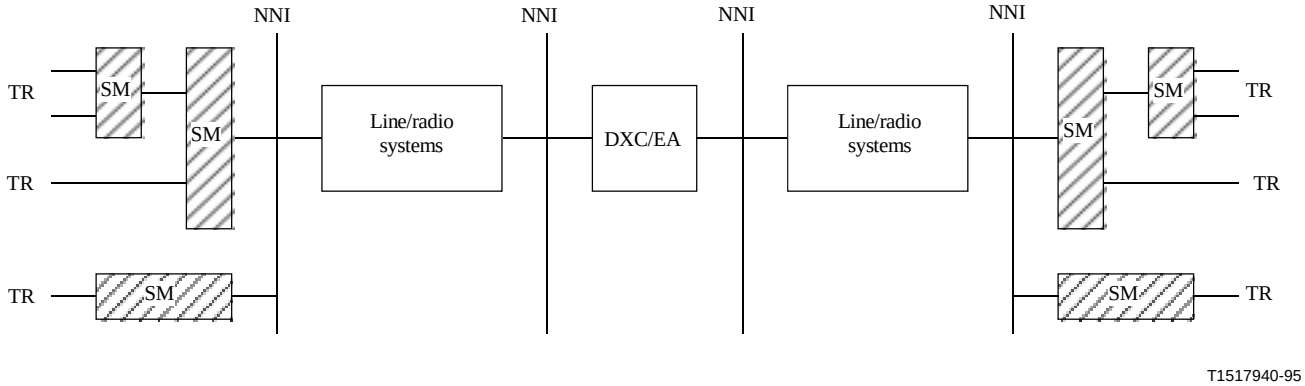
A TUG-2 consists of a homogeneous assembly of identical TU-1s or a TU-2.

A TUG-3 consists of a homogeneous assembly of TUG-2s or a TU-3.

3.6 container-n (n=1-4): A container is the information structure which forms the network synchronous information payload for a Virtual Container. For each of the defined Virtual Containers there is a corresponding container. Adaptation functions have been defined for many common network rates into a limited number of standard containers. These include those rates already defined in Recommendation G.702. Further adaptation functions will be defined in the future for new broadband rates.

3.7 network node interface (NNI): The interface at a network node which is used to interconnect with another network node.

Figure 3-1 gives a possible network configuration to illustrate the location of NNI specified in this Recommendation.



DXC Digital cross-connect equipment

EA External Access equipment

SM Synchronous Multiplexer

TR Tributary

FIGURE 3-1/G.707

Location of the NNI

3.8 pointer: An indicator whose value defines the frame offset of a Virtual Container with respect to the frame reference of the transport entity on which it is supported.

3.9 concatenation: A procedure whereby a multiplicity of Virtual Containers is associated one with another with the result that their combined capacity can be used as a single container across which bit sequence integrity is maintained.

3.10 SDH mapping: A procedure by which tributaries are adapted into Virtual Containers at the boundary of an SDH network.

3.11 SDH multiplexing: A procedure by which multiple lower order path layer signals are adapted into a higher order path or the multiple higher order path layer signals are adapted into a multiplex section.

3.12 SDH aligning: A procedure by which the frame offset information is incorporated into the Tributary Unit or the Administrative Unit when adapting to the frame reference of the supporting layer.

4 Acronyms and abbreviations

For the purposes of this Recommendation, the following abbreviations are used:

AIS	Alarm Indication Signal
APId	Access Point Identifier
APS	Automatic Protection Switching
ATM	Asynchronous Transfer Mode
AU-n	Administrative Unit-n
AUG	Administrative Unit Group
BIP-X	Bit Interleaved Parity-X
CAS	Channel Associated Signalling
CRC-N	Cyclic Redundancy Check-N
DCC	Data Communication Channel
FEBE	Far End Block Error (renamed as REI)
FERF	Far End Receive Failure (renamed as RDI)
HEC	Header Error Control
HOVC	Higher Order Virtual Container
IEC	Incoming Error Count
ISF	Incoming Signal Failure
ISDN	Integrated Services Digital Network
ISID	Idle Signal Identification
LAPD	Link Access Protocol for D-channel
LCD	Loss of Cell Delineation
LOP	Loss of Pointer
MS-AIS	Multiplex Section Alarm Indication Signal
MSOH	Multiplex Section Overhead

MS-RDI	Multiplex Section Remote Defect Indication
MS-REI	Multiplex Section Remote Error Indication
MSTE	Multiplex Section Terminating Element
NDF	New Data Flag
NNI	Network Node Interface
ODI	Outgoing Defect Indication
OEI	Outgoing Error Indication
PDH	Plesiochronous Digital Hierarchy
PLM	Payload Mismatch
POH	Path Overhead
PTE	Path Terminating Element
PTR	Pointer
RDI	Remote Defect Indication (former FERF)
REI	Remote Error Indication (former FEBE)
RFI	Remote Failure Indication
RSOH	Regenerator Section Overhead
SDH	Synchronous Digital Hierarchy
SLM	Signal Label Mismatch
SOH	Section Overhead
STM(-N)	Synchronous Transport Module (-N)
TCM	Tandem Connection Monitoring
TC-RDI	Tandem Connection Remote Defect Indication
TC-REI	Tandem Connection Remote Error Indication
TCOH	Tandem Connection Overhead
TCT	Tandem Connection Trace
TCTE	Tandem Connection Terminating Element
TIM	Trace Identifier Mismatch
TSID	Test Signal Identification
TTI	Trail Trace Identifier
TU-n	Tributary Unit-n
TUG(-n)	Tributary Unit Group (-n)
UNEQ	Unequipped
VC-n	Virtual Container-n

5 Conventions

The order of transmission of information in all the diagrams in this Recommendation is first from left to right and then from top to bottom. Within each byte the most significant bit is transmitted first. The most significant bit (bit 1) is illustrated at the left in all the diagrams.

6 Basic Multiplexing principles

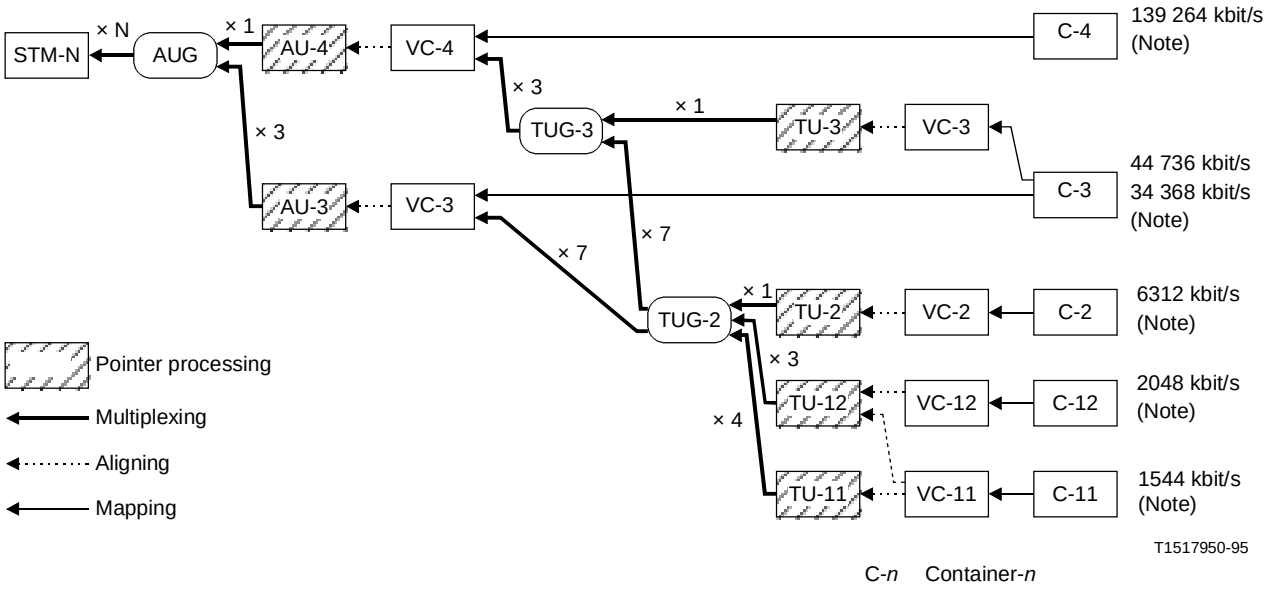
6.1 Multiplexing structure

Figure 6-1 shows the relationship between various multiplexing elements that are defined below, and illustrates possible multiplexing structures.

Figures 6-2, 6-3, 6-4 and 6-5 are examples of how various signals are multiplexed using these multiplexing elements.

Details of the multiplexing method and mappings are given in clauses 7 and 10.

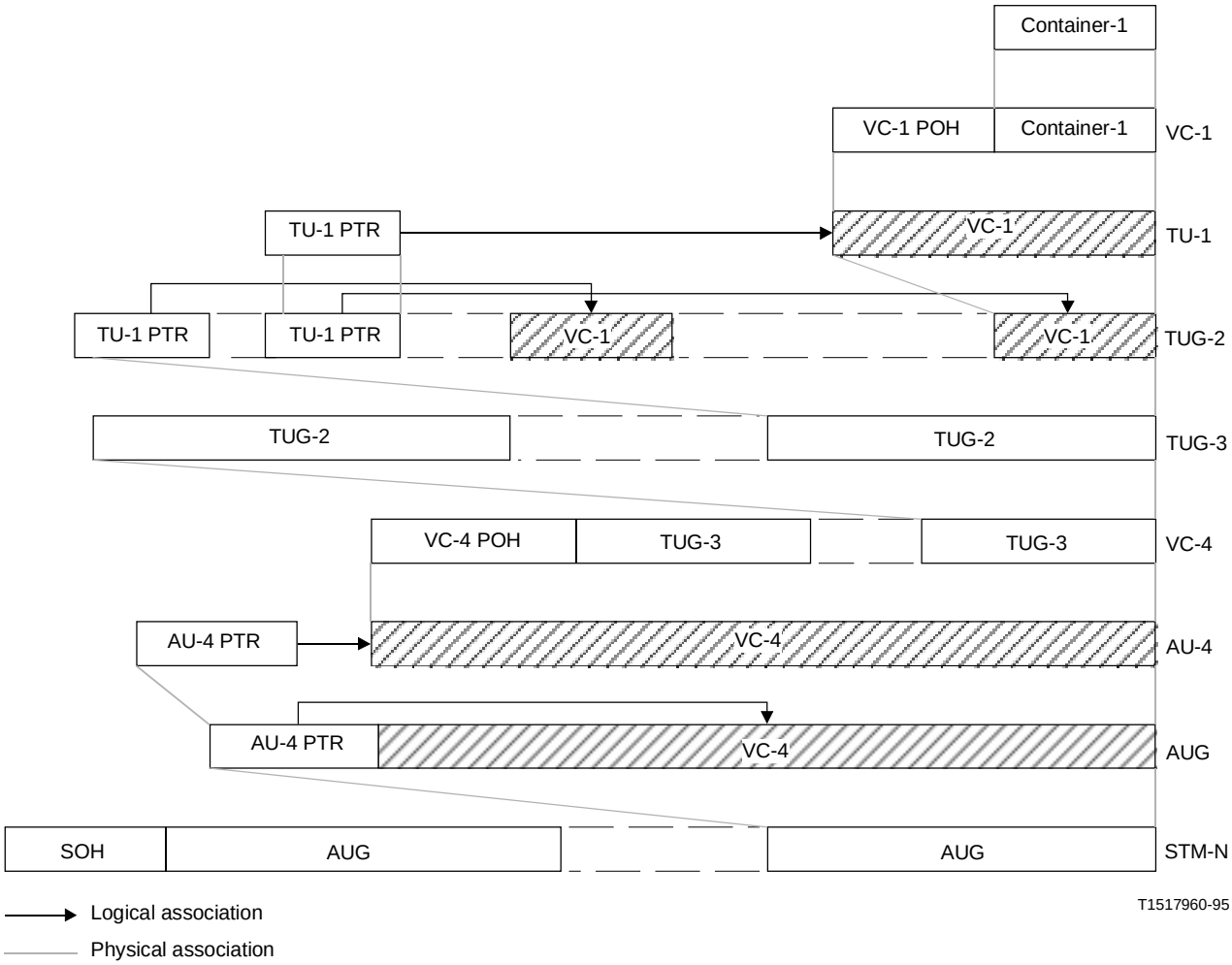
Descriptions of the various multiplexing elements are given in clauses 8 to 10.



NOTE – G.702 tributaries associated with containers C-*x* are shown. Other signals, e.g. ATM, can also be accommodated (see 10.2).

FIGURE 6-1/G.707

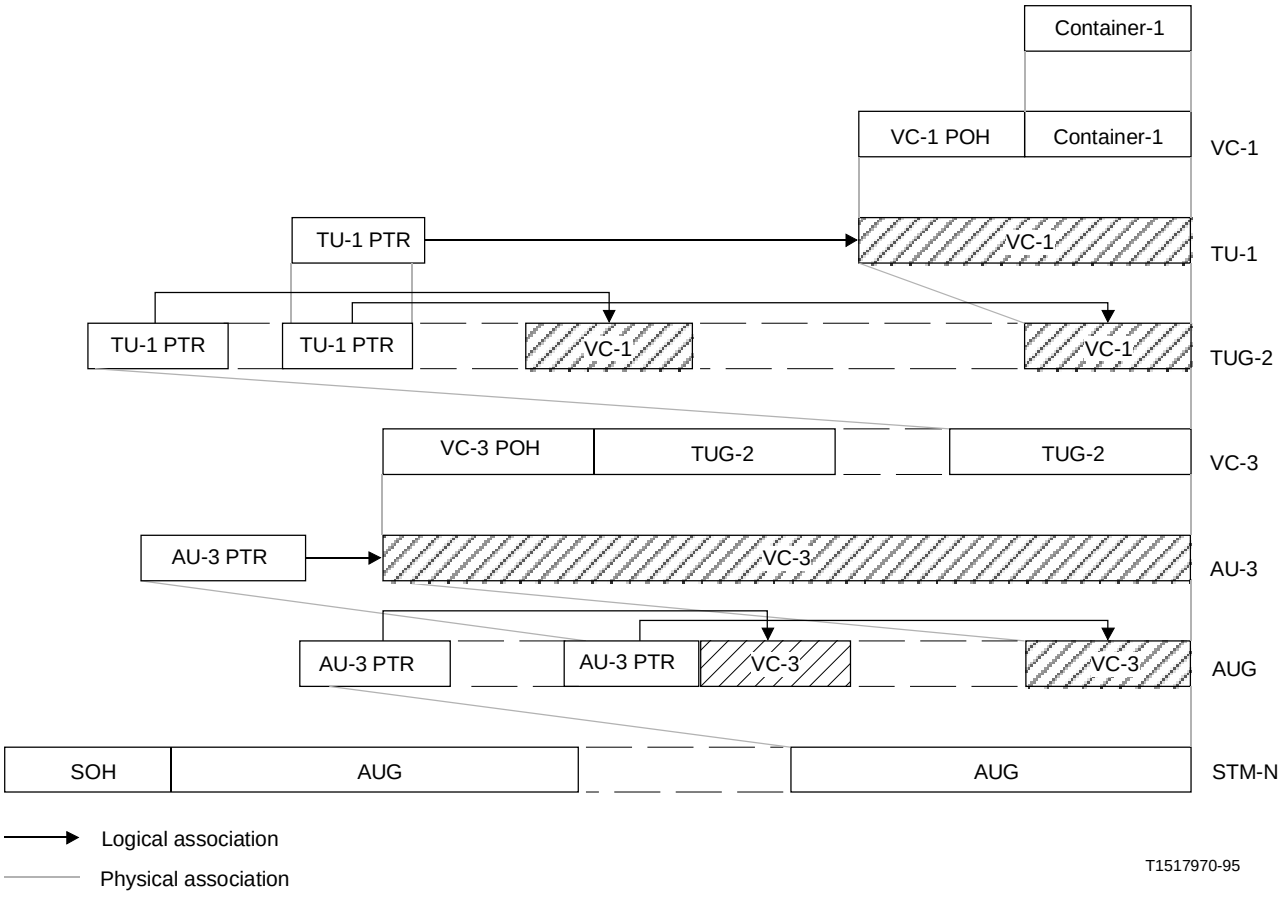
Multiplexing structure



NOTE – Unshaded areas are phase aligned. Phase alignment between the unshaded and shaded areas is defined by the pointer (PTR) and is indicated by the arrow.

FIGURE 6-2/G.707

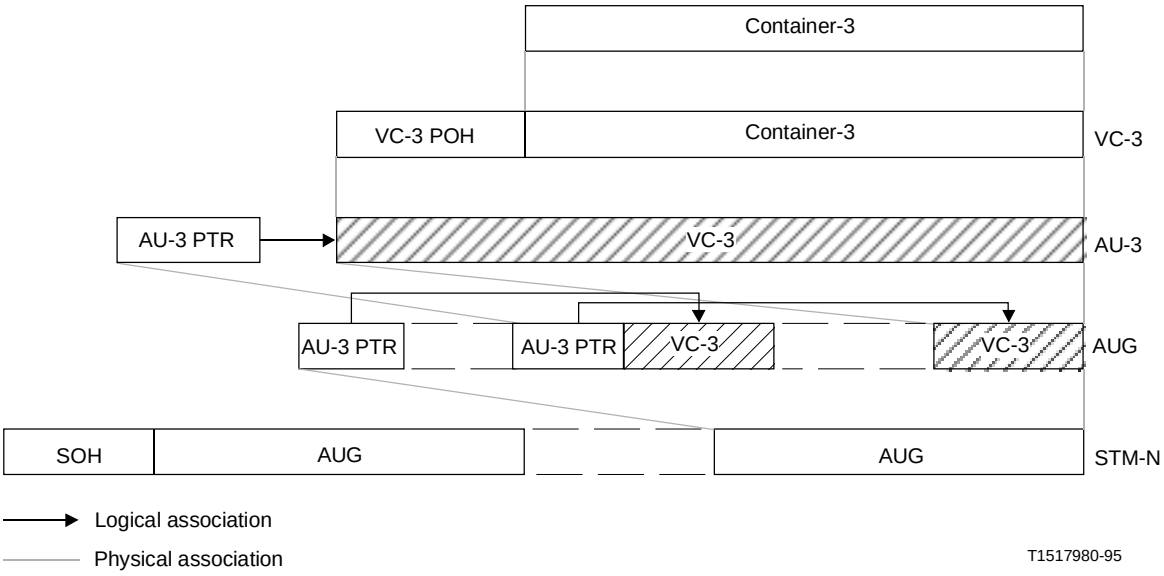
Multiplexing method directly from Container-1 using AU-4



NOTE – Unshaded areas are phase aligned. Phase alignment between the unshaded and shaded areas is defined by the pointer (PTR) and is indicated by the arrow.

FIGURE 6-3/G.707

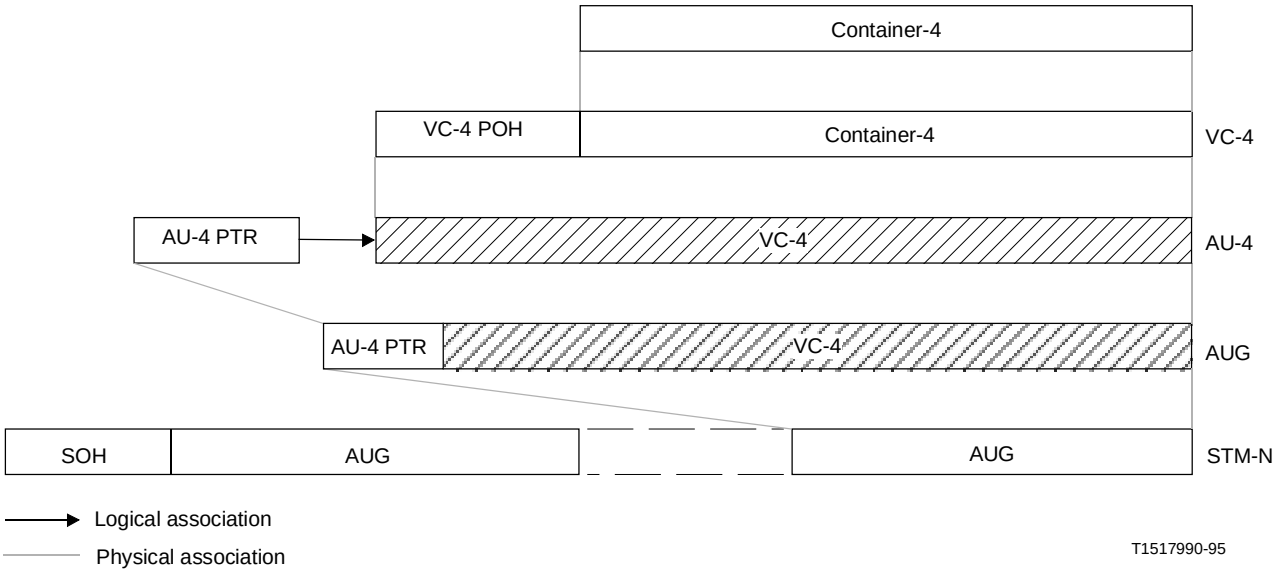
Multiplexing method directly from Container-1 using AU-3



NOTE – Unshaded areas are phase aligned. Phase alignment between the unshaded and shaded areas is defined by the pointer (PTR) and is indicated by the arrow.

FIGURE 6-4/G.707

Multiplexing method directly from Container-3 using AU-3



NOTE – Unshaded areas are phase aligned. Phase alignment between the unshaded and shaded areas is defined by the pointer (PTR) and is indicated by the arrow.

FIGURE 6-5/G.707

Multiplexing method directly from Container-4 using AU-4

6.2 Basic frame structure

STM-N frame structure is shown in Figure 6-6. The three main areas of the STM-N frame are indicated:

– SOH;

– Administrative Unit pointer(s);

– Information payload.

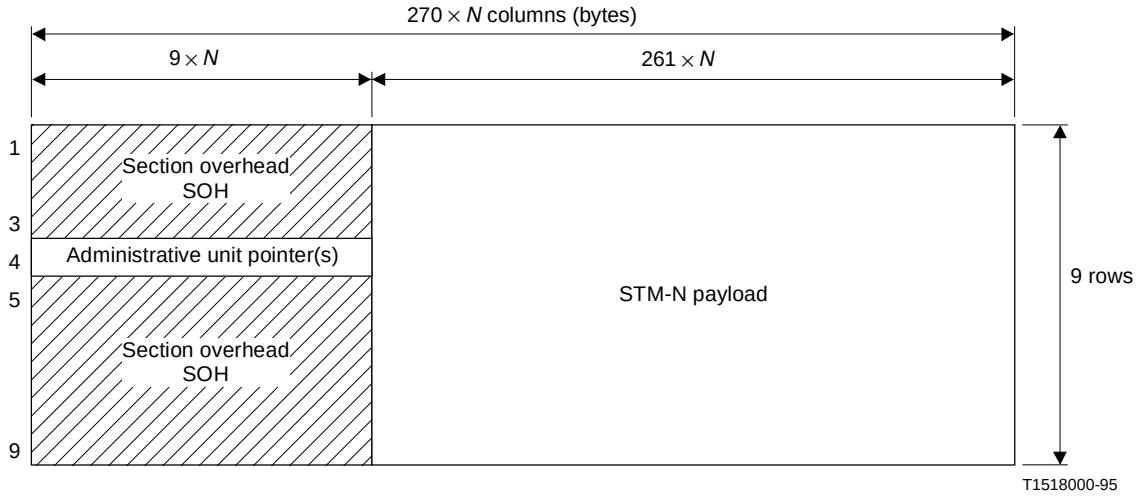


FIGURE 6-6/G.707

STM-N frame structure

6.2.1 Section overhead

Rows 1-3 and 5-9 of columns 1 to 9 × N of the STM-N in Figure 6-6 are dedicated to the SOH.

The allocation of SOH capacity and an explanation of the overhead functions are given in clause 9.

6.2.2 Administrative Unit pointers

Row 4 of columns 1 to 9 × N in Figure 6-6 is available for Administrative Unit pointers. The application of pointers and their detailed specifications are given in clause 8.

6.2.3 Administrative Units in the STM-N

The STM-N payload can support N AUGs where each AUG may consist of:

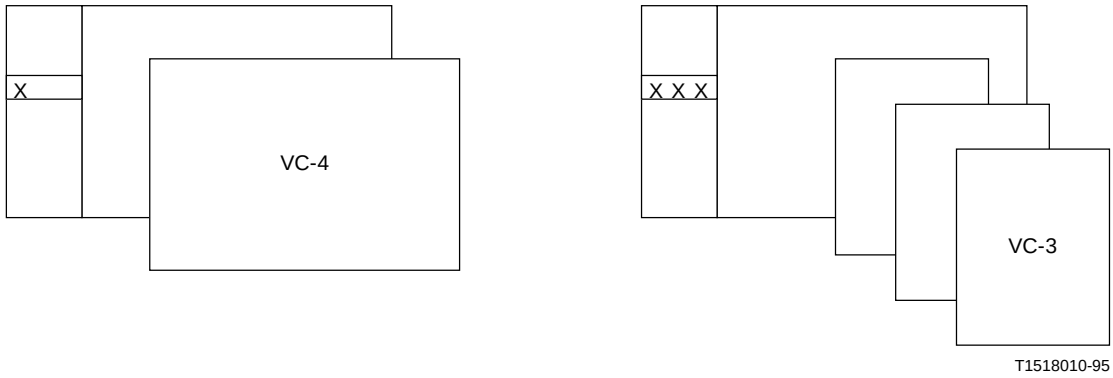
– one AU-4; or

– three AU-3s.

The VC-n associated with each AU-n does not have a fixed phase with respect to the STM-N frame. The location of the first byte of the VC-n is indicated by the AU-n pointer. The AU-n pointer is in a fixed location in the STM-N frame. Examples are illustrated in Figures 6-2, 6-3, 6-4, 6-5, 6-6, 6-7 and 6-8.

The AU-4 may be used to carry, via the VC-4, a number of TU-ns (n=1, 2, 3) forming a two-stage multiplex. An example of this arrangement is illustrated in Figures 6-7 a) and 6-8 a). The VC-n associated with each TU-n does not have a fixed phase relationship with respect to the start of the VC-4. The TU-n pointer is in a fixed location in the VC-4 and the location of the first byte of the VC-n is indicated by the TU-n pointer.

The AU-3 may be used to carry, via the VC-3, a number of TU-ns (n=1, 2) forming a two-stage multiplex. An example of this arrangement is illustrated in Figures 6-7 b) and 6-8 b). The VC-n associated with each TU-n does not have a fixed phase relationship with respect to the start of the VC-3. The TU-n pointer is in a fixed location in the VC-3 and the location of the first byte of the VC-n is indicated by the TU-n pointer.

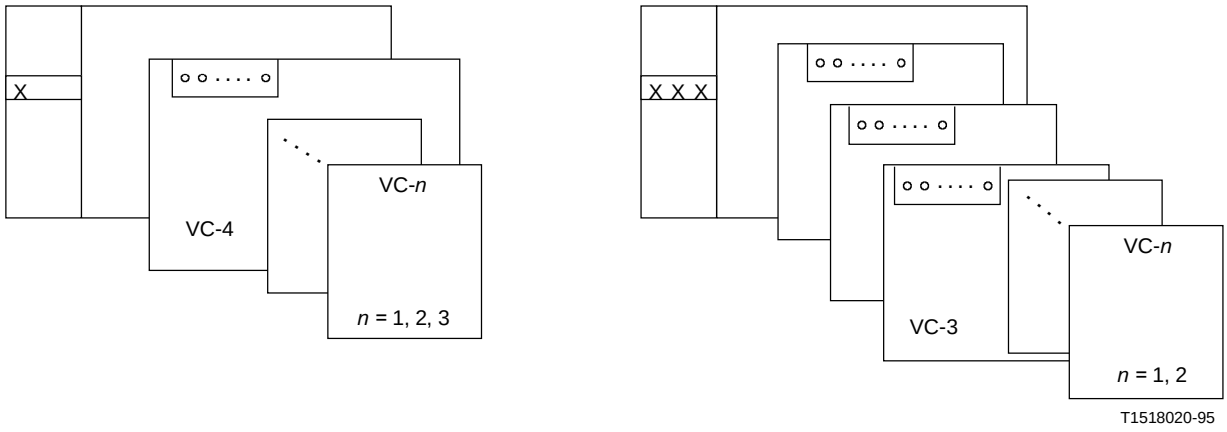


a) STM-1 with one AU-4 **b) STM-1 with three AU-3s**

X AU-*n* pointer
AU-*n* AU-*n* pointer + VC-*n* (see clause 8)

FIGURE 6-7/G.707

Administrative Units in STM-1 frame



a) STM-1 with one AU-4 containing TUs **b) STM-1 with three AU-3s containing TUs**

X AU-*n* pointer
o TU-*n* pointer
AU-*n* AU-*n* pointer + VC-*n* (see clause 8)
TU-*n* TU-*n* pointer + VC-*n* (see clause 8)

FIGURE 6-8/G.707

Two-stage multiplex

6.2.4 Maintenance signals

6.2.4.1 Alarm Indication Signals

An Alarm Indication Signal (AIS) is a signal sent downstream as an indication that an upstream defect has been detected.

6.2.4.1.1 MS-AIS

The Multiplex Section AIS (MS-AIS) is specified as all "1"s in the entire STM-N, excluding the STM-N RSOH.

6.2.4.1.2 AU/TU-AIS

The Administrative Unit AIS (AU-AIS) is specified as all "1"s in the entire AU-n (n=3, 4, 4-Xc), including the AU-n pointer.

The Tributary Unit AIS (TU-AIS) is specified as all "1"s in the entire TU-n (n=1, 2, 3), including the TU-n pointer.

6.2.4.1.3 VC-AIS

An AU/TU-AIS incoming to a Tandem Connection (TC) is translated into a Virtual Container AIS (VC-AIS) within the Tandem Connection because a valid AU-n/TU-n pointer is needed for Tandem Connection Monitoring (TCM).

VC-n (n=3, 4, 4-Xc) AIS is specified as all "1"s in the entire VC-n with a valid network operator byte N1 - supporting TCM functionality - and a valid Error Detection Code in the B3 byte.

VC-n (n=1, 2) AIS is specified as all "1"s in the entire VC-n with a valid network operator byte N2 - supporting TCM functionality - and a valid Error Detection Code in bits 1 and 2 of V5 byte.

6.2.4.2 Unequipped VC-n signal

6.2.4.2.1 Case of network supporting the transport of Tandem Connection signals

For the case of networks supporting the transport of Tandem Connection signals, the VC-n (n=3, 4) or VC-4-Xc unequipped signal is a signal having an all "0"s in the higher order virtual container path signal label byte (C2), the Tandem Connection Monitoring byte (N1) and the path trace byte (J1), and a valid BIP-8 byte (B3). The virtual container payload and the remaining path overhead bytes are unspecified.

For the case of networks supporting the transport of Tandem Connection signals, the VC-n (n=1, 2) unequipped signal is a signal having an all "0"s in the lower order virtual container path signal label (bits 5, 6, 7 of byte V5), the Tandem Connection Monitoring byte (N2) and the path trace byte (J2), and a valid BIP-2 (bits 1, 2 of byte V5). The virtual container payload and the remaining path overhead bytes are unspecified.

These signals indicate to downstream transport processing functions (refer to Recommendation G.803) that the virtual container is unoccupied, not connected to a path termination source function. Additional information on the quality is only available by means of the BIP monitoring.

Within a Tandem Connection, an unequipped VC-n signal generated before the Tandem Connection will have a valid (non all "0"s) Tandem Connection Monitoring byte (N1, N2).

6.2.4.2.2 Case of network not supporting the transport of Tandem Connection signals

For the case of networks not supporting the transport of Tandem Connection signals, the VC-n (n=3, 4) or VC-4-Xc unequipped signal is a signal having an all "0"s in the higher order virtual container path signal label byte (C2) and the path trace byte (J1), and a valid BIP-8 byte (B3). The virtual container payload and the remaining path overhead bytes are unspecified.

For the case of networks not supporting the transport of Tandem Connection signals, the VC-n (n=1, 2) unequipped signal is a signal having an all "0"s in the lower order virtual container path signal label (bits 5, 6, 7 of byte V5) and the path trace byte (J2), and a valid BIP-2 (bits 1, 2 of byte V5). The virtual container payload and the remaining path overhead bytes are unspecified.

6.2.4.3 Supervisory-unequipped VC-n signal

6.2.4.3.1 Case of network supporting the transport of Tandem Connection signals

For the case of networks supporting the transport of Tandem Connection signals, the VC-n (n=3, 4) or VC-4-Xc supervisory-unequipped signal is a signal having an all "0"s in the higher order virtual container path signal label byte (C2) and the Tandem Connection Monitoring byte (N1), a valid BIP-8 byte (B3), a valid path trace identifier byte (J1), and a valid path status byte (G1). The virtual container payload is unspecified. The content of the remaining path overhead bytes F2, H4, F3 and K3 is for further study.

The VC-n (n=3, 4) supervisory-unequipped signal is an enhanced unequipped VC-n signal.

For the case of networks supporting the transport of Tandem Connection signals, the VC-n (n=1, 2) supervisory-unequipped signal is a signal having an all "0"s in the lower order virtual container path signal label (bits 5, 6, 7 of byte V5) and the Tandem Connection Monitoring byte (N2), a valid BIP-2 (bits 1, 2 of byte V5), a valid path trace byte (J2), and valid path status (bits 3 and 8 of byte V5). The virtual container payload is unspecified. The content of the remaining path overhead bytes/bits V5 bit 4 and K4 is for further study.

The VC-n (n=1, 2) supervisory-unequipped signal is an enhanced unequipped VC-n signal.

These signals indicate to downstream transport processing functions (refer to Recommendation G.803) that the virtual container is unoccupied, and sourced by a supervisory generator. Additional information on quality, source and status of the connection is available by means of the bit error, path trace and path status indications.

Within a Tandem Connection, a supervisory-unequipped VC-n signal generated before the Tandem Connection will have a valid (non all "0"s) Tandem Connection Monitoring byte (N1, N2).

6.2.4.3.2 Case of network not supporting the transport of Tandem Connection signals

For the case of networks not supporting the transport of Tandem Connection signals, the VC-n (n=3, 4) or VC-4-Xc supervisory-unequipped signal is a signal having an all "0"s in the higher order virtual container path signal label byte (C2), a valid BIP-8 byte (B3), a valid path trace identifier byte (J1), and a valid path status byte (G1). The virtual container payload is unspecified. The content of the remaining path overhead bytes F2, H4, F3, K3 and N1 is for further study.

For the case of networks not supporting the transport of Tandem Connection signals, the VC-n (n=1, 2) supervisory-unequipped signal is a signal having an all "0"s in the lower order virtual container path signal label (bits 5, 6, 7 of byte V5), a valid BIP-2 (bits 1, 2 of byte V5), a valid path trace byte (J2), and valid path status (bits 3 and 8 of byte V5). The virtual container payload is unspecified. The content of the remaining path overhead bytes/bits V5 bit 4, N2 and K4 is for further study.

6.3 Hierarchical bit rates

The first level of the synchronous digital hierarchy shall be 155 520 kbit/s.

Higher synchronous digital hierarchy bit rates shall be obtained as integer multiples of the first level bit rate and shall be denoted by the corresponding multiplication factor of the first level rate.

The bit rates listed in Table 1 below constitute the synchronous digital hierarchy:

TABLE 1/G.707

SDH hierarchical bit rates

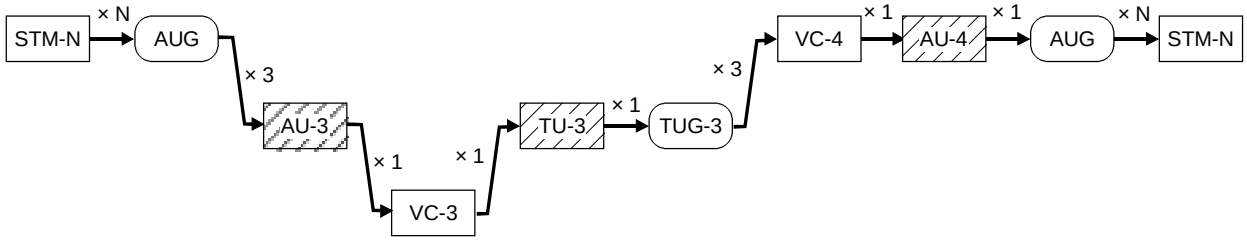
Synchronous digital hierarchy level	Hierarchical bit rate (kbit/s)
1	155 520
4	622 080
16	2 488 320
64	9 953 280
NOTE – The specification of levels higher than 64 requires further study.	

6.4 Interconnection of STM-Ns

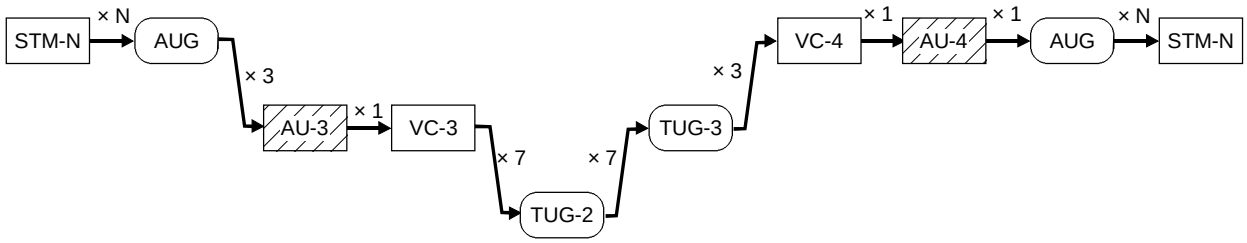
The SDH is designed to be universal, allowing transport of a large variety of signals including all those specified in Recommendation G.702. However, different structures can be used for the transport of Virtual Containers. The following interconnection rules will be used:

a) The rule for interconnecting two AUGs based upon two different types of Administrative Unit, namely AU-4 and AU-3, will be to use the AU-4 structure. Therefore, the AUG based upon AU-3 will be demultiplexed to the VC-3 or TUG-2 level according to the type of the payload, and remultiplexed within an AUG via the TUG-3/VC-4/AU-4 route. This is illustrated in Figures 6-9 a) and 6-9 b).

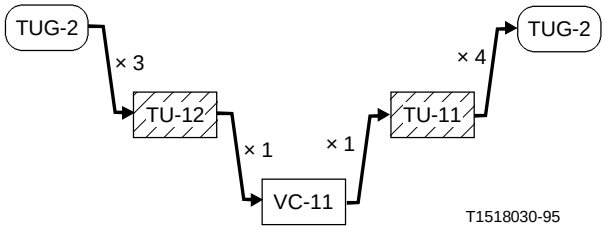
b) The rule for interconnecting VC-11s transported via different types of Tributary Unit, namely TU-11 and TU-12, will be to use the TU-11 structure. This is illustrated in Figure 6-9 c). VC-11, TU-11 and TU-12 are described in the following subclauses.



a) Interconnection of VC-3 with C-3 payload



b) Interconnection of TUG-2



c) Interconnection of VC-11

FIGURE 6-9/G.707

Interconnection of STM-Ns

This SDH interconnection rule does not modify the interworking rules defined in Recommendation G.802 for networks based upon different Plesiochronous Digital Hierarchies and speech encoding laws.

NOTE – The need for specifying rules for interconnection between networks using different types of concatenation (see 8.3.6) is for further study.

6.5 Scrambling

The STM-N (N = 1, 4, 16, 64) signal must have sufficient bit timing content at the NNI. A suitable bit pattern, which prevents a long sequence of "1"s or "0"s is provided by using a scrambler.

The operation of the scrambler shall be functionally identical to that of a frame synchronous scrambler of sequence length 127 operating at the line rate.

The generating polynomial shall be $1 + X^6 + X^7$. Figure 6-10 gives a functional diagram of the frame synchronous scrambler.

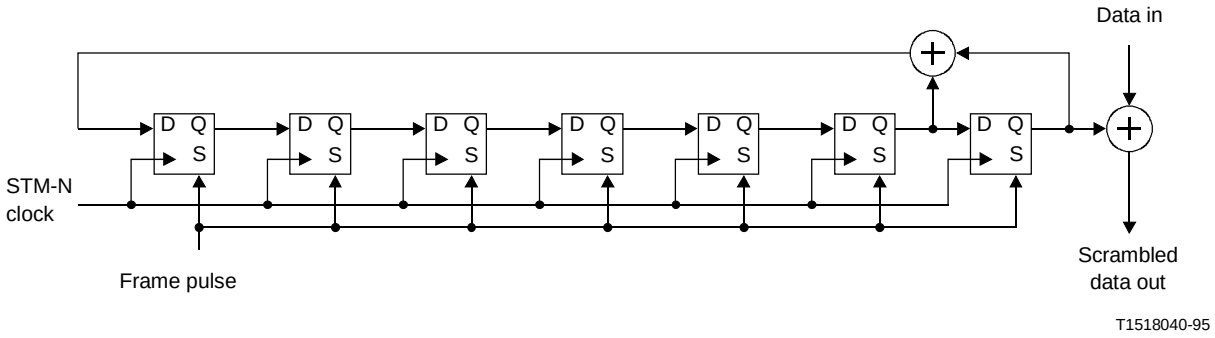


FIGURE 6-10/G.707

Frame synchronous scrambler
(functional diagram)

The scrambler shall be reset to "1111111" on the most significant bit of the byte following the last byte of the first row of the STM-N SOH. This bit, and all subsequent bits to be scrambled shall be added modulo 2 to the output from the X^7 position of the scrambler. The scrambler shall run continuously throughout the complete STM-N frame.

The first row of the STM-N SOH ($9 \times N$ bytes, including the A1 and A2 framing bytes) shall not be scrambled.

NOTE – Care should be taken in selecting the binary content of the Z0 bytes and of the bytes reserved for national use which are excluded from the scrambling process of the STM-N signal to ensure that long sequences of "1"s or "0"s do not occur.

6.6 Physical specification of the NNI

Specifications for physical electrical characteristics of the NNI are contained in Recommendation G.703.

Specifications for physical optical characteristics of the NNI are contained in Recommendation G.957.

6.7 Frame structure for 51 840 kbit/s interface

Low/medium capacity SDH transmission systems based on radio and satellite technologies which are not designed for the transmission of STM-1 signals shall operate at a bit rate of 51 840 kbit/s across digital sections. However, this bit rate does not represent a level of the SDH or a NNI bit rate.

The recommended frame structure for 51 840 kbit/s signal for use in low/medium capacity radio (ITU-R Recommendation F.750) and satellite digital (ITU-R Recommendation S.1149) sections is given in Annex A.

7 Multiplexing method

7.1 Multiplexing of Administrative Units into STM-N

7.1.1 Multiplexing of Administrative Unit Groups (AUGs) into STM-N

The arrangement of N AUGs multiplexed into the STM-N is shown in Figure 7-1. The AUG is a structure of 9 rows by 261 columns plus 9 bytes in row 4 (for the AU-n pointers). The STM-N consists of an SOH as described in 9.2 and a structure of 9 rows by $N \times 261$ columns with $N \times 9$ bytes in row 4 (for the AU-n pointers). The N AUGs are one-byte interleaved into this structure and have a fixed phase relationship with respect to the STM-N.

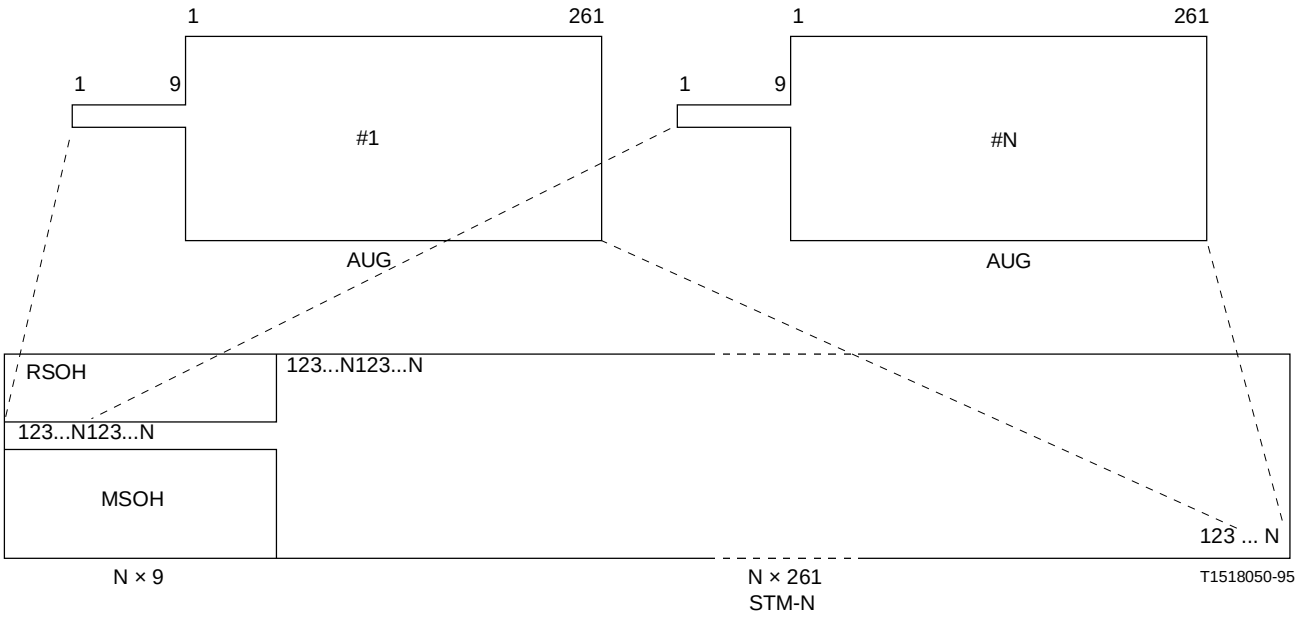


FIGURE 7-1/G.707

Multiplexing of N AUGs into STM-N

7.1.2 Multiplexing of an AU-4 via AUG

The multiplexing arrangement of a single AU-4 via the AUG is depicted in Figure 7-2. The 9 bytes at the beginning of row 4 are allocated to the AU-4 pointer. The remaining 9 rows by 261 columns is allocated to the Virtual Container-4 (VC-4). The phase of the VC-4 is not fixed with respect to the AU-4. The location of the first byte of the VC-4 with respect to the AU-4 pointer is given by the pointer value. The AU-4 is placed directly in the AUG.

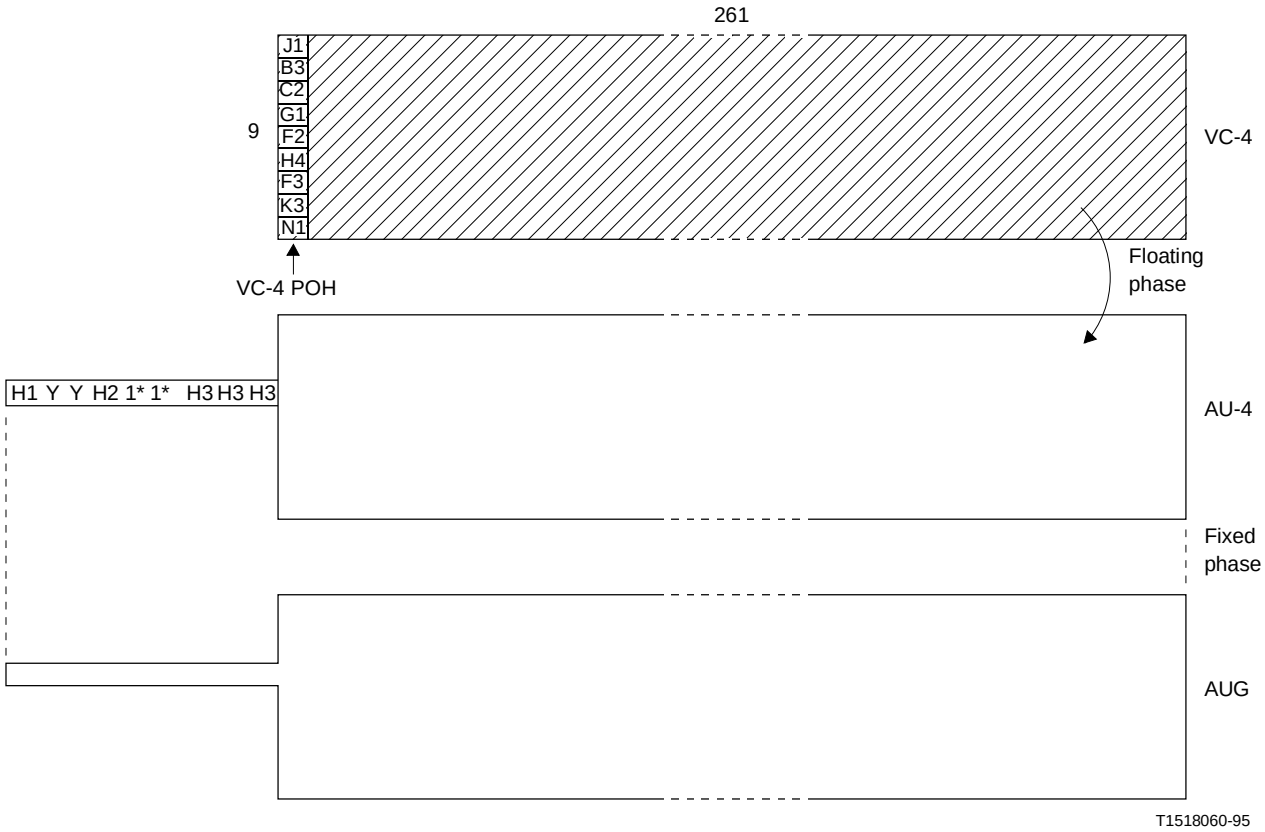
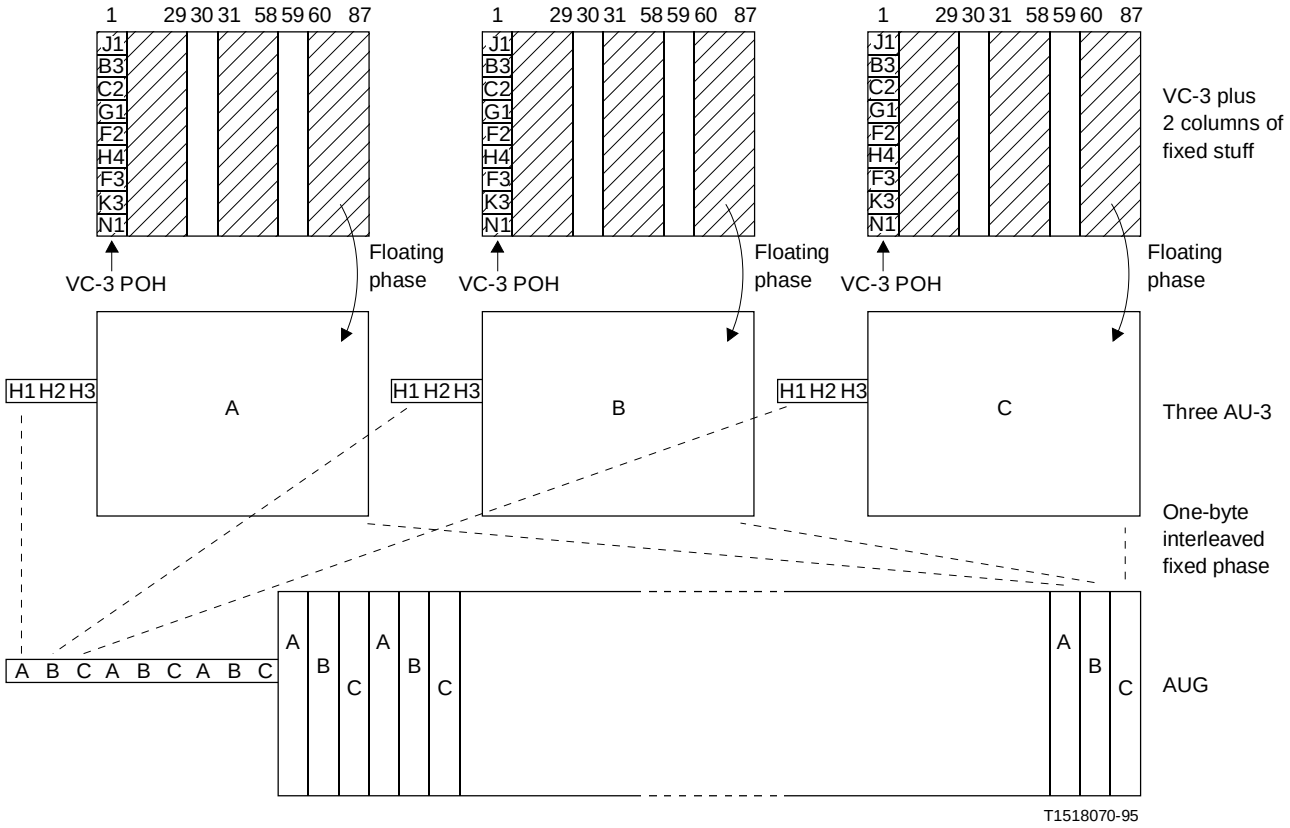


FIGURE 7-2/G.707

Multiplexing of AU-4 via AUG

7.1.3 Multiplexing of AU-3s via AUG

The multiplexing arrangement of three AU-3s via the AUG is depicted in Figure 7-3. The 3 bytes at the beginning of row 4 are allocated to the AU-3 pointer. The remaining 9 rows by 87 columns is allocated to the VC-3 and two columns of fixed stuff. The byte in each row of the two columns of fixed stuff of each AU-3 shall be the same. The phase of the VC-3 and the two columns of fixed stuff is not fixed with respect to the AU-3. The location of the first byte of the VC-3 with respect to the AU-3 pointer is given by the pointer value. The three AU-3s are one-byte interleaved in the AUG.



NOTE – The byte in each row of the two columns of fixed stuff of each AU-3 shall be the same.

FIGURE 7-3/G.707

Multiplexing of AU-3s via AUG

7.2 Multiplexing of Tributary Units into VC-4 and VC-3

7.2.1 Multiplexing of Tributary Unit Group-3s (TUG-3s) into a VC-4

The arrangement of three TUG-3s multiplexed in the VC-4 is shown in Figure 7-4. The TUG-3 is a 9-row by 86-column structure. The VC-4 consists of one column of VC-4 POH, two columns of fixed stuff and a 258-column payload structure. The three TUG-3s are single byte interleaved into the 9-row by 258-column VC-4 payload structure and have a fixed phase with respect to the VC-4.

As described in 7.1, the phase of the VC-4 with respect to the AU-4 is given by the AU-4 pointer.

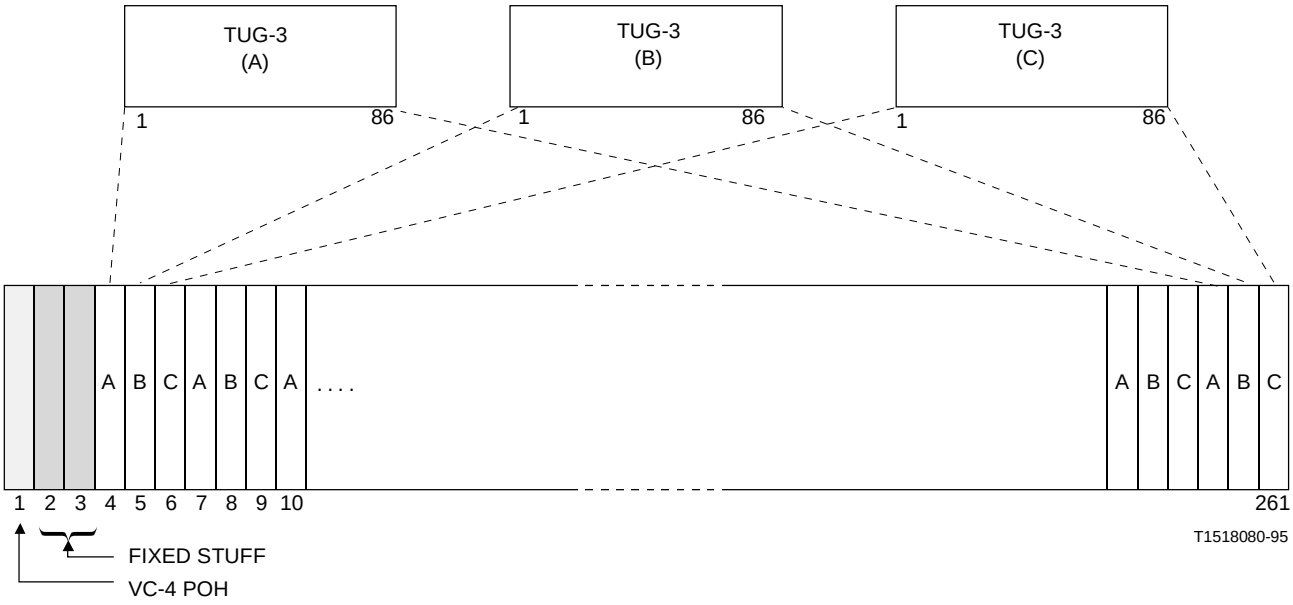


FIGURE 7-4/G.707

Multiplexing of three TUG-3s into a VC-4

7.2.2 Multiplexing of a TU-3 via TUG-3

The multiplexing of a single TU-3 via the TUG-3 is depicted in Figure 7-5. The TU-3 consists of the VC-3 with a 9-byte VC-3 POH and the TU-3 pointer. The first column of the 9-row by 86-column TUG-3 is allocated to the TU-3 pointer (bytes H1, H2, H3) and fixed stuff. The phase of the VC-3 with respect to the TUG-3 is indicated by the TU-3 pointer.

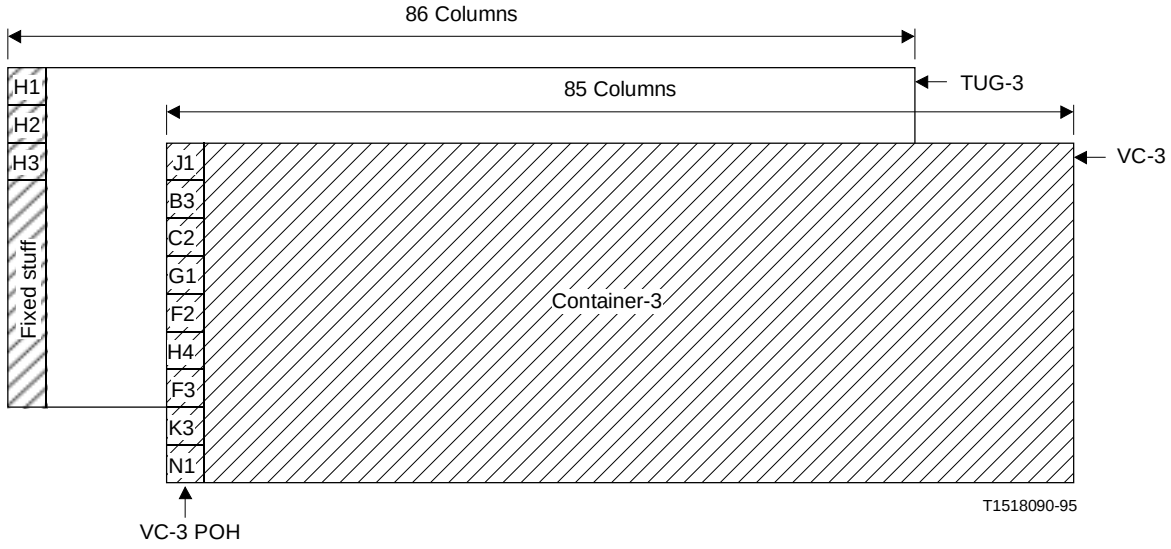


FIGURE 7-5/G.707

Multiplexing of a TU-3 via a TUG-3

7.2.3 Multiplexing of TUG-2s via a TUG-3

The multiplexing structure for the TUG-2 via the TUG-3 is depicted in Figure 7-6. The TUG-3 is a 9-row by 86-column structure with the first two columns of fixed stuff.

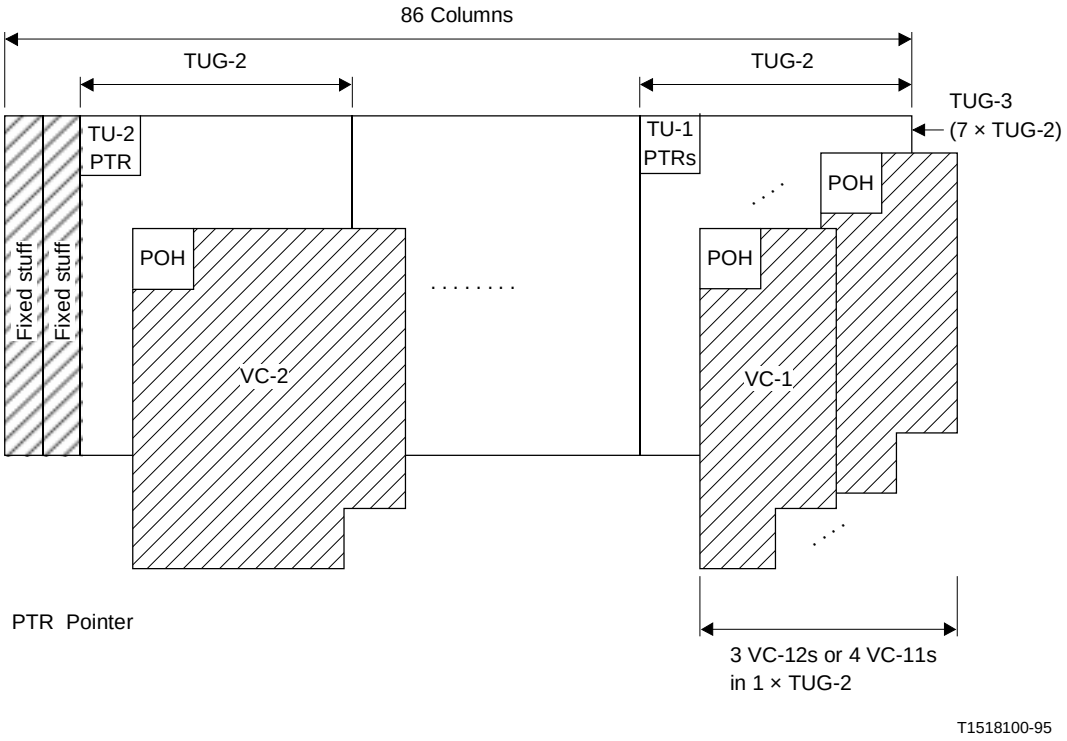


FIGURE 7-6/G.707

Multiplexing of seven TUG-2s via a TUG-3

A group of seven TUG-2s can be multiplexed via the TUG-3.

The arrangement of seven TUG-2s multiplexed via the TUG-3 is depicted in Figure 7-7. The TUG-2s are one-byte interleaved in the TUG-3.

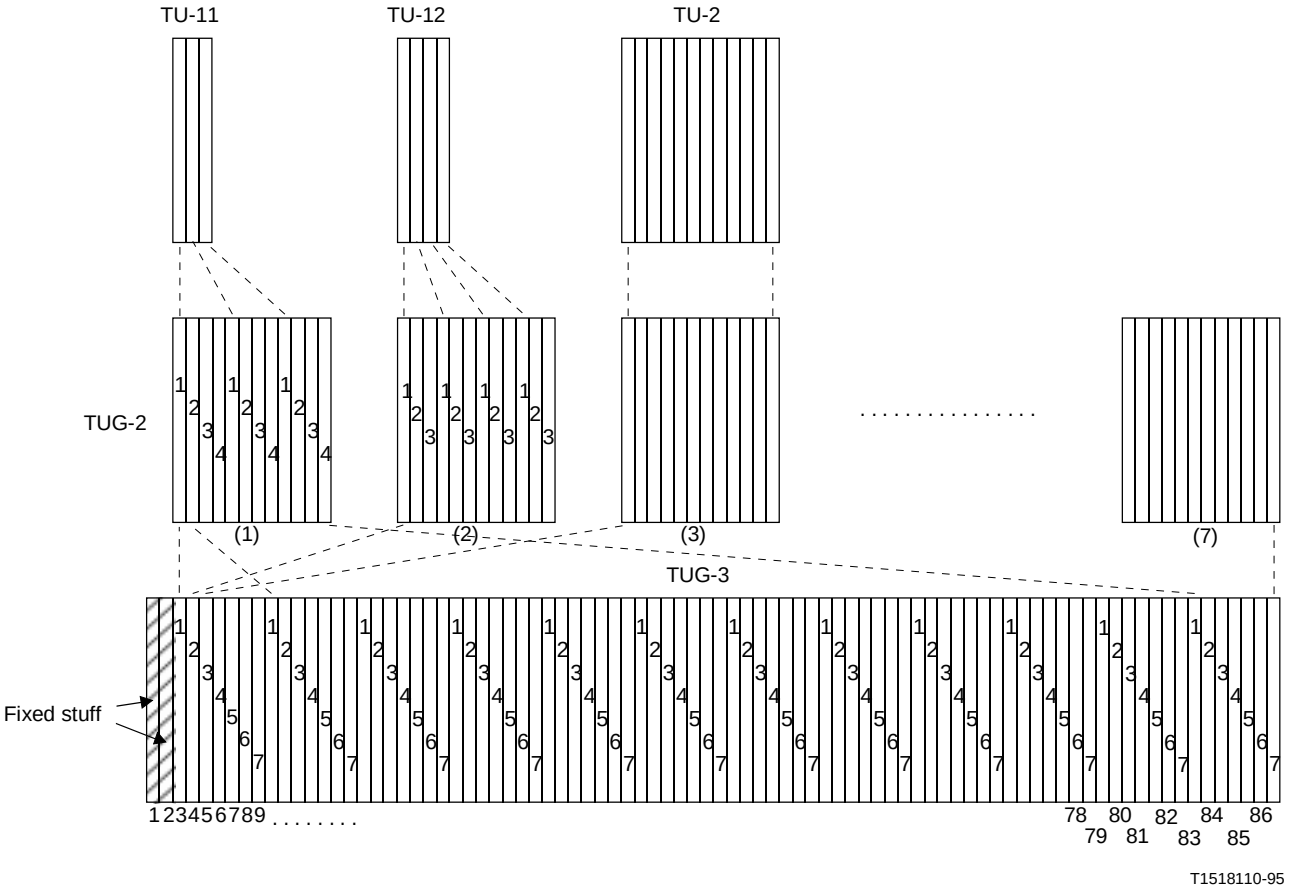


FIGURE 7-7/G.707

Multiplexing of seven TUG-2s via a TUG-3

7.2.4 Multiplexing of TUG-2s into a VC-3

The multiplexing structure for TUG-2s into a VC-3 is depicted in Figure 7-8. The VC-3 consists of VC-3 POH and a 9-row by 84-column payload structure. A group of seven TUG-2s can be multiplexed into the VC-3.

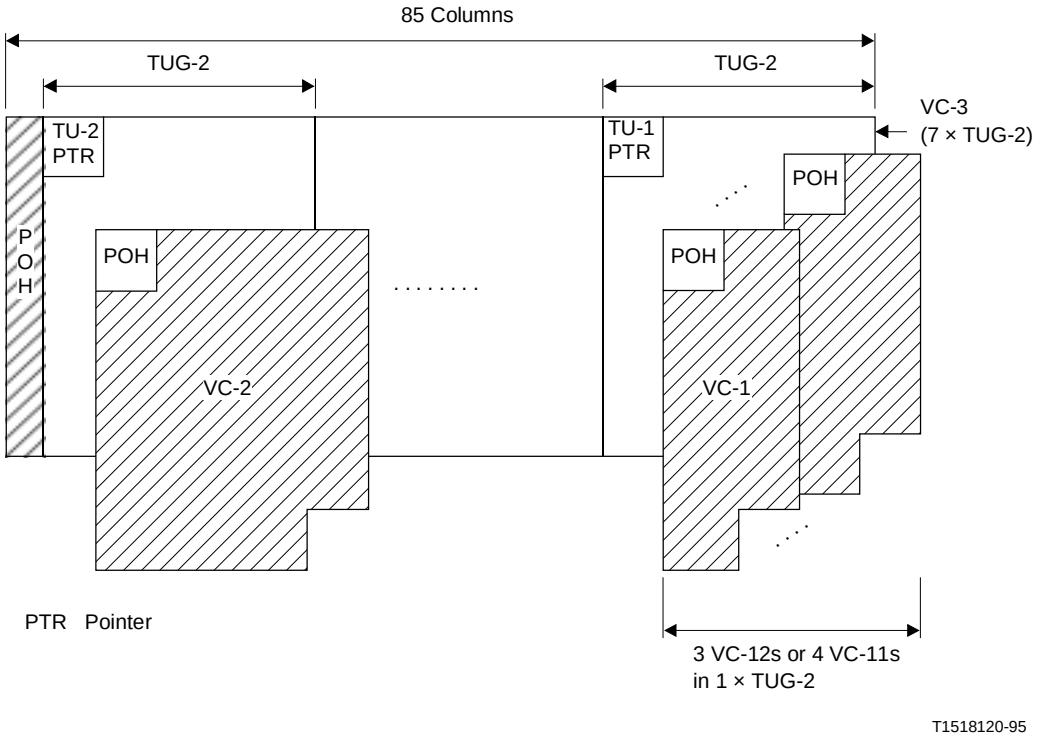


FIGURE 7-8/G.707

Multiplexing of seven TUG-2s into a VC-3

The arrangement of seven TUG-2s multiplexed into the VC-3 is depicted in Figure 7-9. The TUG-2s are one-byte interleaved in the VC-3. An individual TUG-2 has a fixed location in the VC-3 frame.

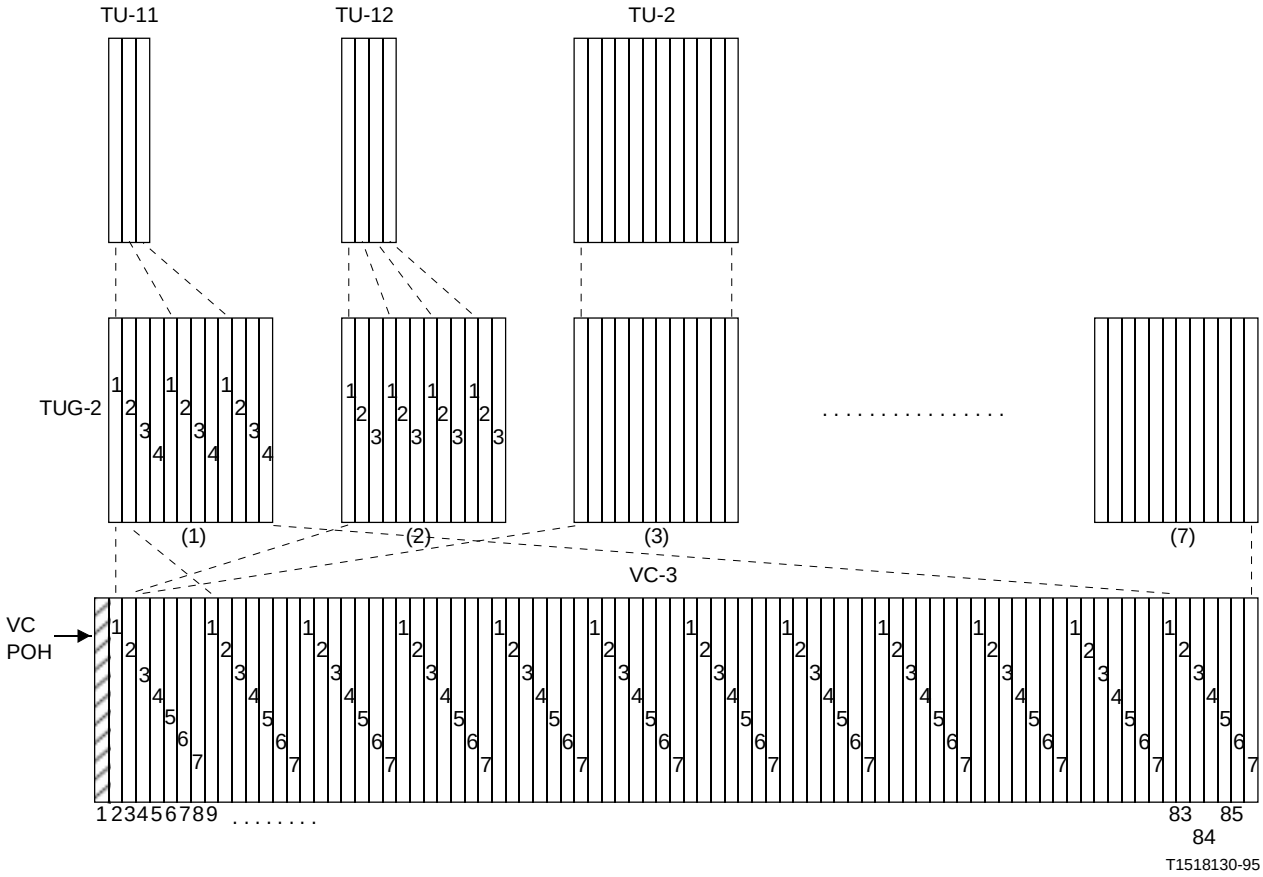


FIGURE 7-9/G.707

Arrangement of seven TUG-2s multiplexed into a VC-3

7.2.5 Multiplexing of a TU-2 via TUG-2s

The multiplexing arrangement of a single TU-2 via the TUG-2 is depicted in Figure 7-9.

7.2.6 Multiplexing of TU-1s via TUG-2s

The multiplexing arrangements of four TU-11s or three TU-12s via the TUG-2 are depicted in Figure 7-9. The TU-1s are one-byte interleaved in the TUG-2.

7.3 AU-n/TU-n numbering scheme

An STM-1 frame comprises 270 columns (numbered 1 to 270). The first nine columns contain the SOH with the remaining 261 columns containing the data payload. In the case of an AU-4 structured frame, the payload columns may be addressed by means of a three figure address (K, L, M) where K represents the TUG-3 number, L the TUG-2 number, and M the TU-1 number. Refer to Figures 7-10 and 7-11 and Table 2a. In the case of an AU-3 structured frame, only L and M coordinates are used. Refer to Figures 7-12 and Table 2b.

In order to provide a simple and convenient means of determining the total tributary capacity, i.e. the number of lower order tributaries provided, the payload columns are allocated a Time Slot number. The number of Time Slots per tributary in each frame is determined by the payload configuration.

Time Slots (TS) are numbered from left to right in the VC-4/VC-3 as shown in Figures 7-10 to 7-12. For example in a VC-4, TS1 of a TU-12 starts in column 10, TS2 in column 11, and so on until TS63 is in column 72. In a VC-3, TS1 of a TU-11 starts in column 2, TS2 in column 3 … and TS28 in column 29.

7.3.1 Numbering of AU-4s in an STM-N signal

There are N AU-4s (VC-4s) in an STM-N signal; they should be numbered as follows:

– AU-4 (VC-4) #1: indicated by the first pointer in the STM-N SOH;

– AU-4 (VC-4) #2: indicated by the second pointer in the STM-N SOH;

– AU-4 (VC-4) #3: indicated by the third pointer in the STM-N SOH;

– …

– AU-4 (VC-4) #N: indicated by the Nth pointer in the STM-N SOH;

7.3.2 Numbering of TU-3s in a VC-4

The VC-4 can comprise three TUG-3s which shall be numbered #1, #2, and #3.

– TUG-3 #1 [Corresponding to TUG-3 (A) in Figure 7-4] is accommodated in columns 4, 7, 10, …, 259 of the VC-4;

– TUG-3 #2 [Corresponding to TUG-3 (B) in Figure 7-4] is accommodated in columns 5, 8, 11, …, 260 of the VC-4;

– TUG-3 #3 [Corresponding to TUG-3 (C) in Figure 7-4] is accommodated in columns 6, 9, 12, …, 261 of the VC-4;

Each TUG-3 can comprise a TU-3.

Thus any TU-3 can be allocated a three figure address in the form #K, #L, #M, where K designates the TUG-3 number (1 to 3), L and M are always 0. The location of the columns in the VC-4 occupied by TU-3(K,0, 0) is given by the formula:

Xth column = $4 + [K-1] + 3*[X-1]$ For X = 1 to 86

Thus TU-3(1, 0, 0) resides in columns 4, 7, 10, …, 259 of the VC-4, and TU-3(3, 0, 0) resides in columns 6, 9, 12, …, 261 of the VC-4.

7.3.3 Numbering of TU-2s in a VC-4

Each TUG-3 can comprise seven TUG-2s which shall be numbered #1 to #7 and each TUG-2 can comprise a TU-2.

Thus any TU-2 can be allocated a three figure address in the form #K, #L, #M, where K designates the TUG-3 number (1 to 3), L designates the TUG-2 number (1 to 7), and M is always 0. The location of the columns in the VC-4 occupied by TU-2 (K, L, 0) is given by the formula:

Xth column = $10 + [K-1] + 3*[L-1] + 21*[X-1]$ For X = 1 to 12

Thus TU-2(1, 1, 0) resides in columns 10, 31, 52, 73, 94, 115, 136, 157, 178, 199, 220 and 241 of the VC-4, and TU-2(3, 7, 0) resides in columns 30, 51, 72, 93, 114, 135, 156, 177, 198, 219, 240 and 261 of the VC-4. A full listing of the location of the TU-2 columns within the VC-4 frame is given in Appendix I.

7.3.4 Numbering of TU-12s in a VC-4

Each TUG-3 can comprise seven TUG-2s which shall be numbered #1 to #7 and each TUG-2 can comprise three TU-12s which shall be numbered #1 to #3.

Thus any TU-12 can be allocated a number in the form #K, #L, #M, where K designates the TUG-3 number (1 to 3), L designates the TUG-2 number (1 to 7), and M designates the TU-12 number (1 to 3). The location of the columns in the VC-4 occupied by TU-12 (K, L, M) is given by the formula:

Xth column = 10 + [K–1] + 3*[L–1] + 21*[M–1] + 63*[X–1] for X=1 to 4

Thus TU-12(1, 1, 1) resides in columns 10, 73, 136, and 199 of the VC-4, and TU-12(3, 7, 3) resides in columns 72, 135, 198 and 261 of the VC-4. A full listing of the location of the TU-12 columns within the VC-4 frame is given in Appendix II.

7.3.5 Numbering of TU-11s in a VC-4

Each TUG-3 can comprise seven TUG-2s which shall be numbered #1 to #7 and each TUG-2 can comprise four TU-11s which shall be numbered #1 to #4.

Thus any TU-11 can be allocated a number in the form #K, #L, #M, where K designates the TUG-3 number (1 to 3), L designates the TUG-2 number (1 to 7), and M designates the TU-11 number (1 to 4). The location of the columns in the VC-4 occupied by TU-11 (K, L, M) is given by the formula:

Xth column = 10 + [K–1] + 3*[L–1] + 21*[M–1] + 84*[X–1] for X=1 to 3

Thus TU-11(1, 1, 1) resides in columns 10, 94 and 178 of the VC-4, and TU-11(3, 7, 4) resides in columns 93, 177 and 261 of the VC-4. A full listing of the location of the TU-11 columns within the VC-4 frame is given in Appendix III.

7.3.6 Numbering of AU-3s in an STM-N signal

There are N × 3 AU-3s (VC-3s) in an STM-N signal; they should be numbered as follows:

– AU-3 (VC-3) #1: indicated by the first pointer in the STM-N SOH;

– AU-3 (VC-3) #2: indicated by the second pointer in the STM-N SOH;

– AU-3 (VC-3) #3: indicated by the third pointer in the STM-N SOH;

– …

– AU-3 (VC-3) #N × 3: indicated by the N × 3 th pointer in the STM-N SOH.

7.3.7 Numbering of TU-2s in a VC-3

As shown in Figures 7-8 and 7-9, a VC-3 can comprise seven TUG-2s which shall be numbered from #1 to #7. Each TUG-2 can comprise a TU-2.

Thus any TU-2 can be allocated a two-figure address in the form #L, #M, where L designates the TUG-2 number (1 to 7) and M is always 0. The location of the columns in the VC-3 occupied by TU-2(L, 0) is given by the formula:

Xth column = 2 + *[L–1] + 7*[X–1] For X = 1 to 12

Thus TU-2(1, 0) resides in columns 2, 9, … and 79 of the VC-3, and TU-2(7, 0) resides in columns 8, 15, …. and 85 of the VC-3. A full listing of the location of the TU-12 columns with the VC-3 frame is given in Appendix IV.

7.3.8 Numbering of TU-12s in a VC-3

Each TUG-2 can comprise three TU-12s which shall be numbered #1 to #3.

Thus any TU-12 can be allocated a two-figure address in the form #L, #M, where L designates the TUG-2 number (1 to 7) and M designates the TU-12 number (1 to 3). The location of the columns in the VC-3 occupied by TU-11(L, M) is given by the formula:

Xth column = 2 + *[L–1] + 7*[M–1] + 21*[X–1] For X = 1 to 4

Thus TU-12(1, 1) resides in columns 2, 23, 44 and 65 of the VC-3, and TU-11(7, 3) resides in columns 22, 43, 64 and 85 of the VC-3. A full listing of the location of the TU-12 columns with the VC-3 frame is given in Appendix V.

7.3.9 Numbering of TU-11s in a VC-3

Each TUG-2 can comprise four TU-11s which shall be numbered #1 to #4.

Thus any TU-11 can be allocated a two-figure address in the form #L, #M, where L designates the TUG-2 number (1 to 7) and M designates the TU-11 number (1 to 4). The location of the columns in the VC-3 occupied by TU-11(L, M) is given by the formula:

Xth column = 2 + *[L–1] + 7*[M–1] + 28*[X–1] For X = 1 to 3

Thus TU-11(1, 1) resides in columns 2, 30 and 58 of the VC-3, and TU-11(7, 4) resides in columns 29, 57 and 85 of the VC-3. A full listing of the location of the TU-11 columns with the VC-3 frame is given in Appendix VI.

NOTE – The Time Slot number contained in the diagrams below should not be interpreted as the tributary port number.

An external tributary signal may be assigned to a particular payload capacity using a connection function.

For example at the VC-12 level,

– Tributary #1 – TU-12 (1, 1, 1)
– Tributary #2 – TU-12 (1, 1, 2)
– Tributary #3 – TU-12 (1, 1, 3)
– Tributary #4 – TU-12 (1, 2, 1)
– :
– Tributary #63 - TU-12 (3, 7, 3)

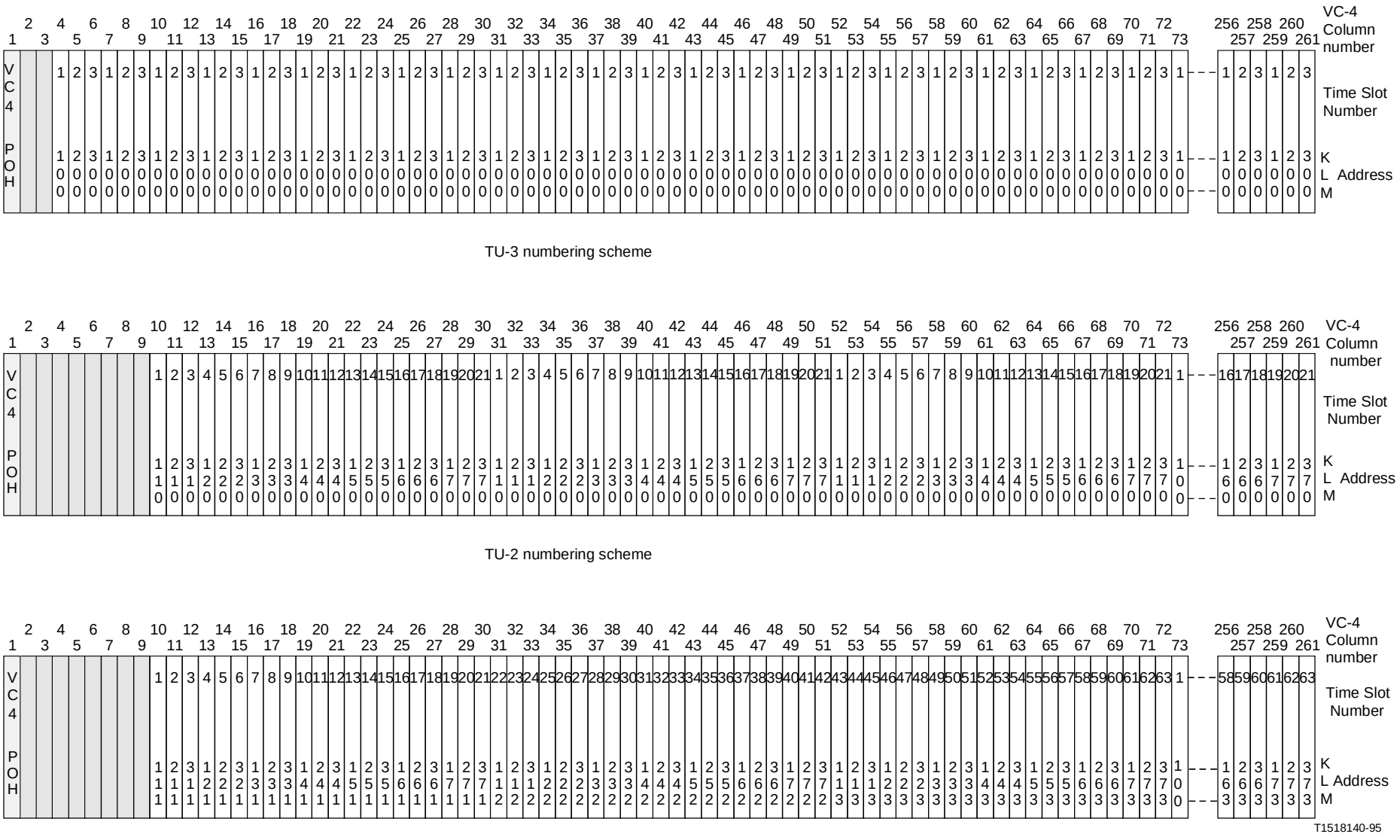


FIGURE 7-10/G.707

TU-3, TU-2 and TU-12 numbering scheme within a VC-4

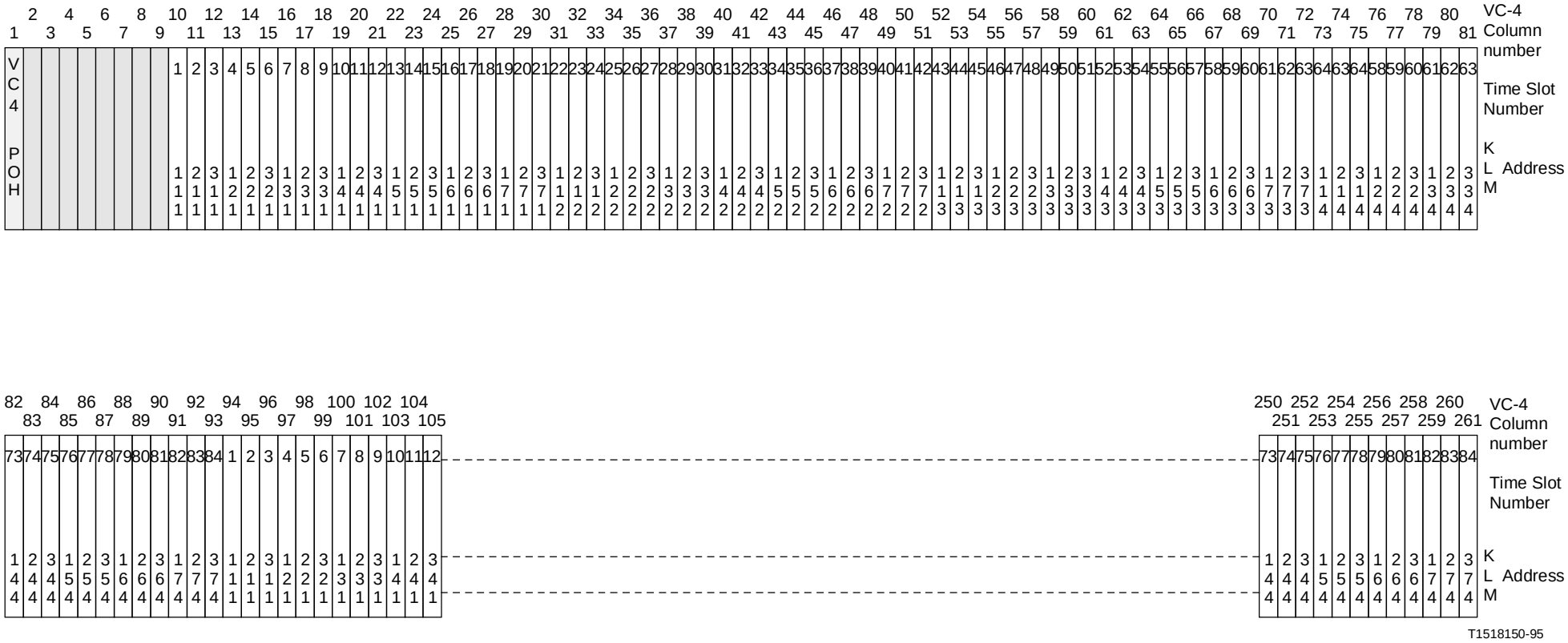


FIGURE 7-11/G.707

TU-11 numbering scheme within a VC-4

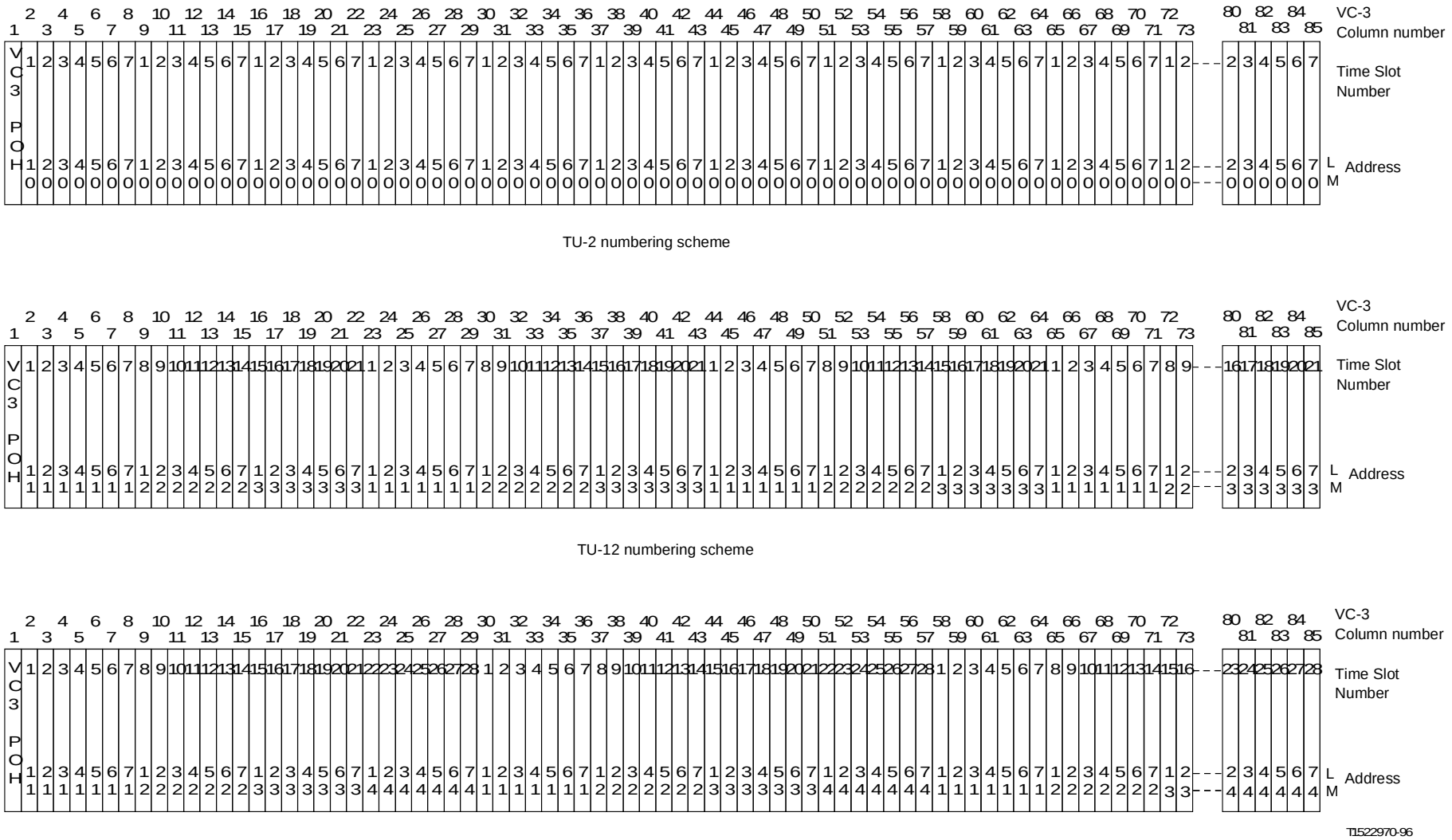


FIGURE 7-12/G.707

TU-2, TU-12 and TU-11 numbering scheme within a VC-3

TABLE 2a/G.707

Allocation of TU-n capacity to Time Slots within a VC-4

Address #					Address #					Address #				
TU-3	TU-2	TU-12	TU-11	TS#	TU-3	TU-2	TU-12	TU-11	TS#	TU-3	TU-2	TU-12	TU-11	TS#
100	110	111	111	1	200	210	211	211	2	300	310	311	311	3
		112	112	22			212	212	23			312	312	24
		113	113	43			213	213	44			313	313	45
			114	64				214	65				314	66
	120	121	121	4		220	221	221	5		320	321	321	6
		122	122	25			222	222	26			322	322	27
		123	123	46			223	223	47			323	323	48
			124	67				224	68				324	69
	130	131	131	7		230	231	231	8		330	331	331	9
		132	132	28			232	232	29			332	332	30
		133	133	49			233	233	50			333	333	51
			134	70				234	71				334	72
	140	141	141	10		240	241	241	11		340	341	341	12
		142	142	31			242	242	32			342	342	33
		143	143	52			243	243	53			343	343	54
			144	73				244	74				344	75
	150	151	151	13		250	251	251	14		350	351	351	15
		152	152	34			252	252	35			352	352	36
		153	153	55			253	253	56			353	353	57
			154	76				254	77				354	78
	160	161	161	16		260	261	261	17		360	361	361	18
		162	162	37			262	262	38			362	362	39
		163	163	58			263	263	59			363	363	60
			164	79				264	80				364	81
	170	171	171	19		270	271	271	20		370	371	371	21
		172	172	40			272	272	41			372	372	42
		173	173	61			273	273	62			373	373	63
			174	82				274	83				374	84

Address = TUG-3#, TUG-2#, TUG-1# = #K, #L, #M

TABLE 2b/G.707

Allocation of TU-n capacity to Time Slots within a VC-3

Address #

TU-2	TU-12	TU-11	TS#
10	11	11	1
	13	13	8
	13	13	15
		14	22
20	21	21	2
	22	22	9
	23	23	16
		24	23
30	31	31	3
	32	32	10
	33	33	17
		34	24
40	41	41	4
	42	42	11
	43	43	18
		44	25
50	51	51	5
	52	52	12
	53	53	19
		54	26
60	61	61	6
	62	62	13
	63	63	20
		64	27
70	71	71	7
	72	72	14
	73	73	21
		74	28
Address = TUG-2#, TUG-1# = #L, #M			

8 Pointers

8.1 AU-n pointer

The AU-n pointer provides a method of allowing flexible and dynamic alignment of the VC-n within the AU-n frame.

Dynamic alignment means that the VC-n is allowed to "float" within the AU-n frame. Thus, the pointer is able to accommodate differences, not only in the phases of the VC-n and the SOH, but also in the frame rates.

8.1.1 AU-n pointer location

The AU-4 pointer is contained in bytes H1, H2 and H3 as shown in Figure 8-1. The three individual AU-3 pointers are contained in three separate H1, H2 and H3 bytes as shown in Figure 8-2.

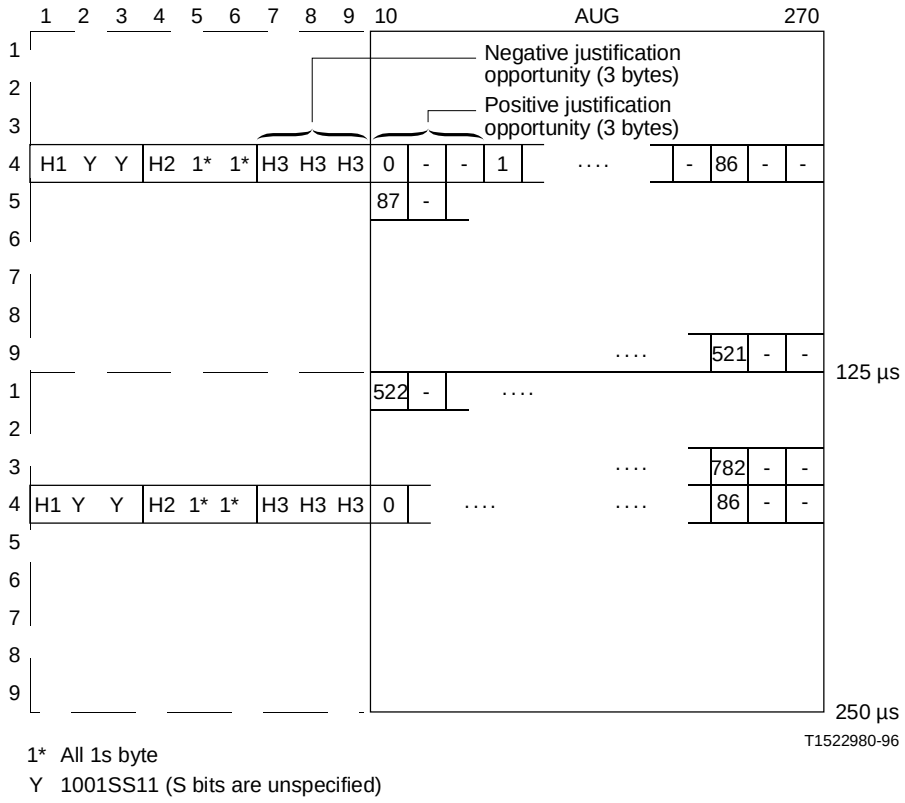


FIGURE 8-1/G.707

AU-4 pointer offset numbering

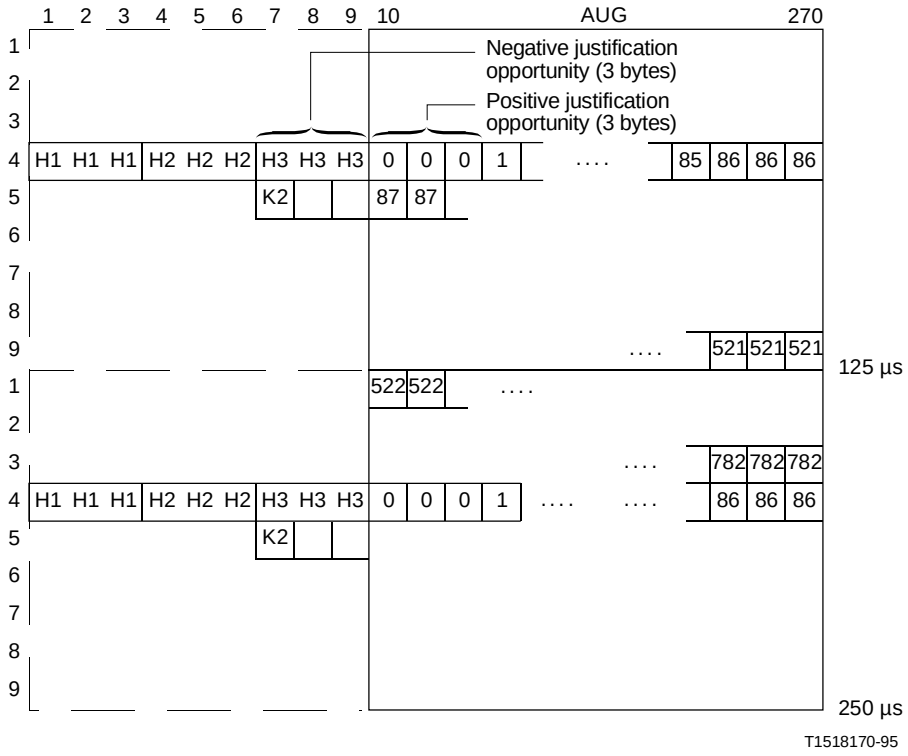


FIGURE 8-2/G.707

AU-3 pointer offset numbering

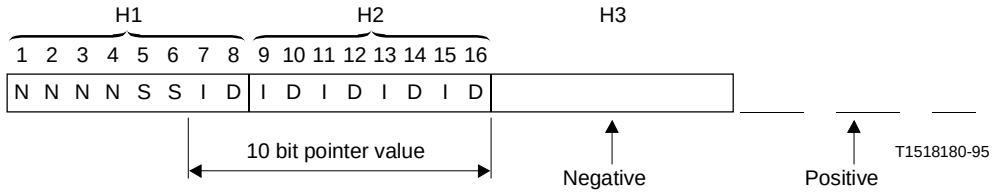
8.1.2 AU-n pointer value

The pointer contained in H1 and H2 designates the location of the byte where the VC-n begins. The two bytes allocated to the pointer function can be viewed as one word as shown in Figure 8-3. The last ten bits (bits 7-16) of the pointer word carry the pointer value.

As illustrated in Figure 8-3, the AU-4 pointer value is a binary number with a range of 0 to 782 which indicates the offset, in three byte increments, between the pointer and the first byte of the VC-4 (see Figure 8-1). Figure 8-3 also indicates one additional valid pointer, the Concatenation Indication. The Concatenation Indication is indicated by "1001" in bits 1-4, bits 5-6 unspecified, and ten "1"s in bits 7-16. The AU-4 pointer is set to Concatenation Indication for AU-4 concatenation (see 8.1.7).

As illustrated in Figure 8-3, the AU-3 pointer value is also a binary number with a range of 0 to 782. Since there are three AU-3s in the AUG, each AU-3 has its own associated H1, H2 and H3 bytes. As shown in Figure 8-2, the H bytes are shown in sequence. The first H1, H2, H3 set refers to the first AU-3, and the second set to the second AU-3, and so on. For the AU-3s, each pointer operates independently.

In all cases, the AU-n pointer bytes are not counted in the offset. For example, in an AU-4, the pointer value of 0 indicates that the VC-4 starts in the byte location that immediately follows the last H3 byte, whereas an offset of 87 indicates that the VC-4 starts three bytes after the K2 byte.



I Increment
D Decrement
N New data flag

New data flag

– Enabled when at least 3 out of 4 bits match "1001"
– Disabled when at least 3 out of 4 bits match "0110"
– Invalid with other codes

Negative justification

– Invert 5 D-bits
– Accept majority vote

Pointer value (b7-b16)

– Normal range is:
for AU-4, AU-3: 0-782 decimal
for TU-3: 0-764 decimal

Positive justification

– Invert 5 I-bits
– Accept majority vote

Concatenation indication

– 1001SS1111111111 (SS bits are unspecified)

SS bits	AU-*n*/TU-*n* type
10	AU-4, AU-3, TU-3

NOTE – The pointer is set to all "1"s when AIS occurs.

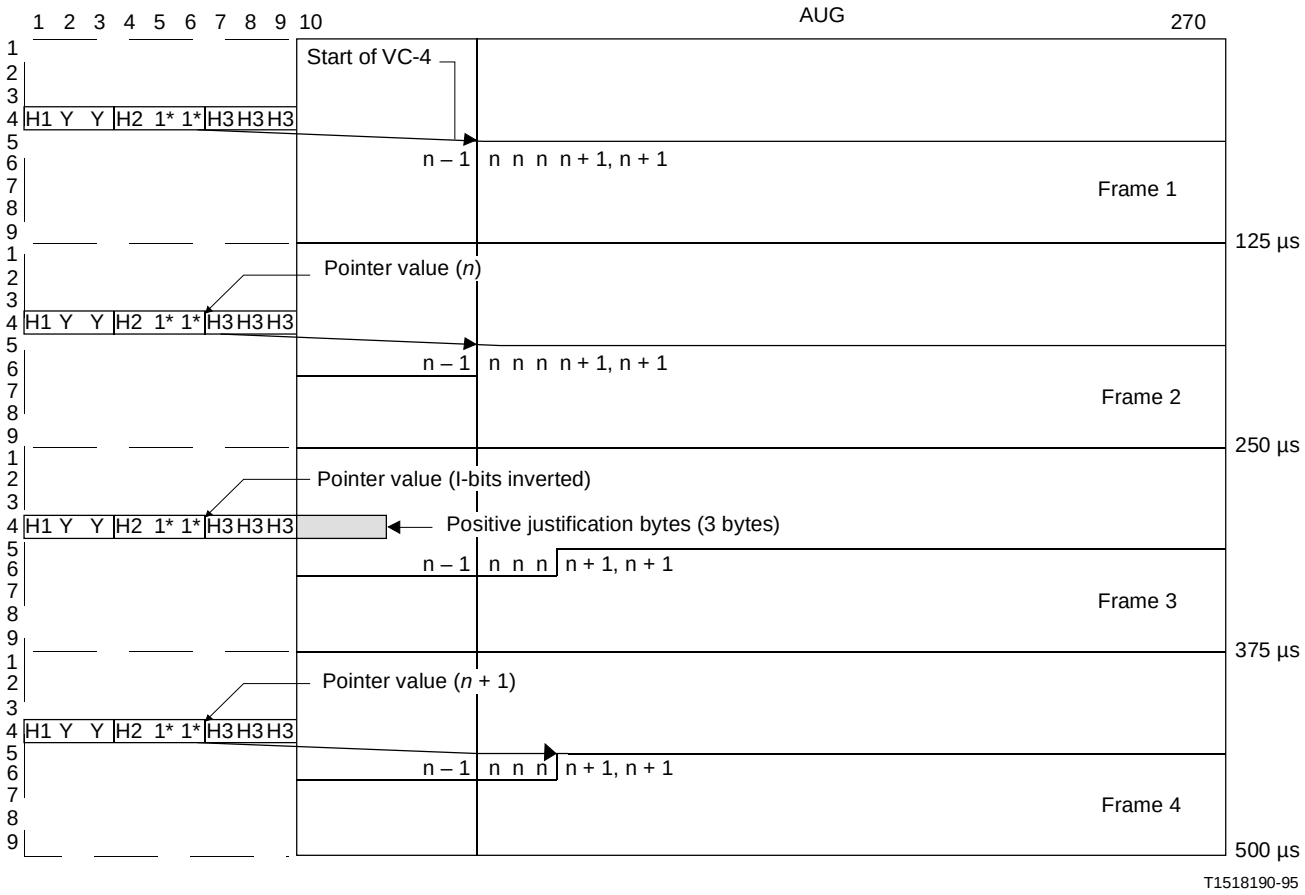
FIGURE 8-3/G.707

AU-n/TU-3 pointer (H1, H2, H3) coding

8.1.3 Frequency justification

If there is a frequency offset between the frame rate of the AUG and that of the VC-n, then the pointer value will be incremented or decremented as needed, accompanied by a corresponding positive or negative justification byte or bytes. Consecutive pointer operations must be separated by at least three frames (i.e. every fourth frame) in which the pointer value remains constant.

If the frame rate of the VC-n is too slow with respect to that of the AUG, then the alignment of the VC-n must periodically slip back in time and the pointer value must be incremented by one. This operation is indicated by inverting bits 7, 9, 11, 13 and 15 (I-bits) of the pointer word to allow 5-bit majority voting at the receiver. Three positive justification bytes appear immediately after the last H3 byte in the AU-4 frame containing inverted I-bits. Subsequent pointers will contain the new offset. This is illustrated in Figure 8-4.



1* All 1s byte
Y 1001SS11 (S bits are unspecified)

FIGURE 8-4/G.707

AU-4 pointer adjustment operation – positive justification

For AU-3 frames, a positive justification byte appears immediately after the individual H3 byte of the AU-3 frame containing inverted I-bits. Subsequent pointers will contain the new offset. This is illustrated in Figure 8-5.

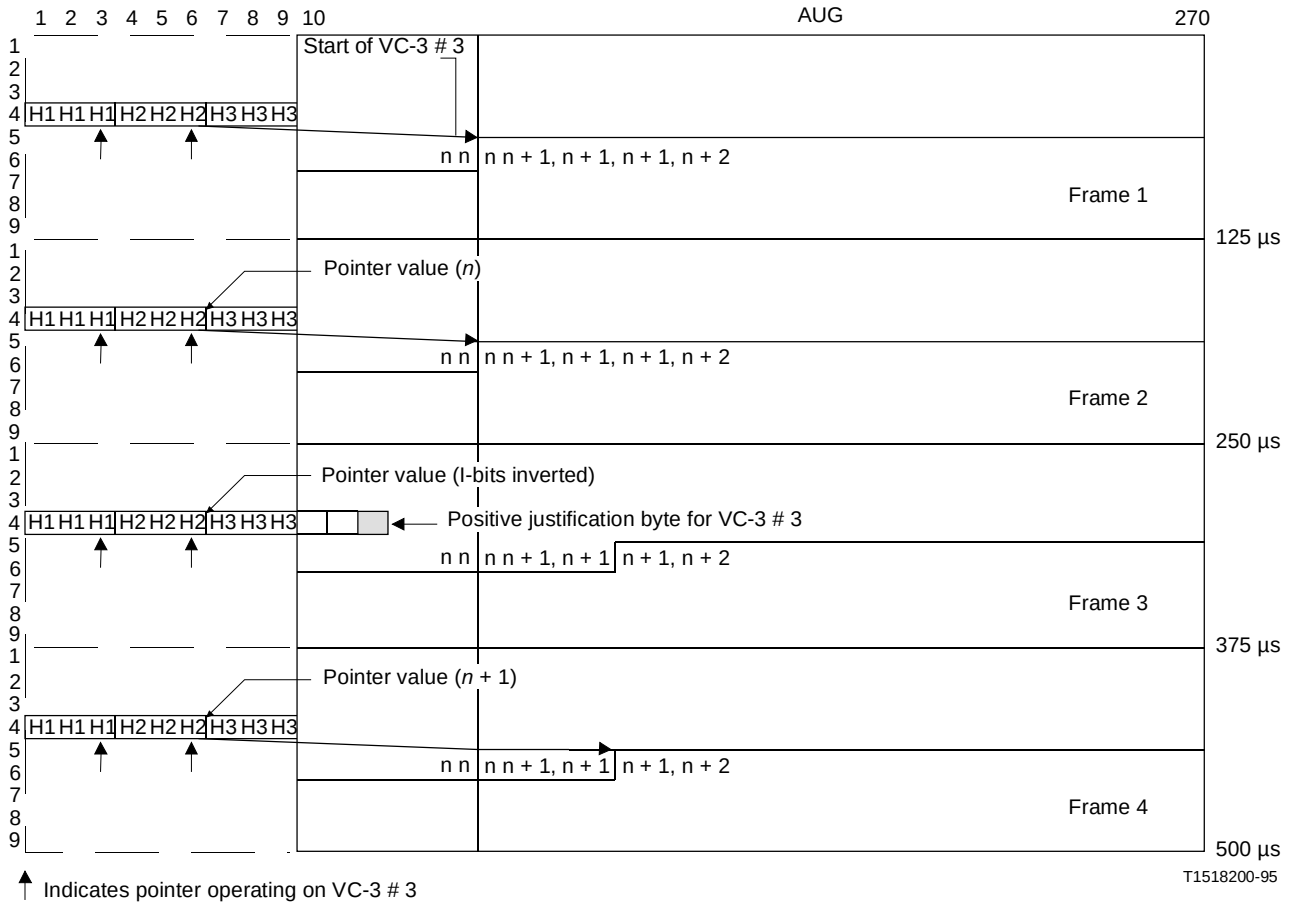
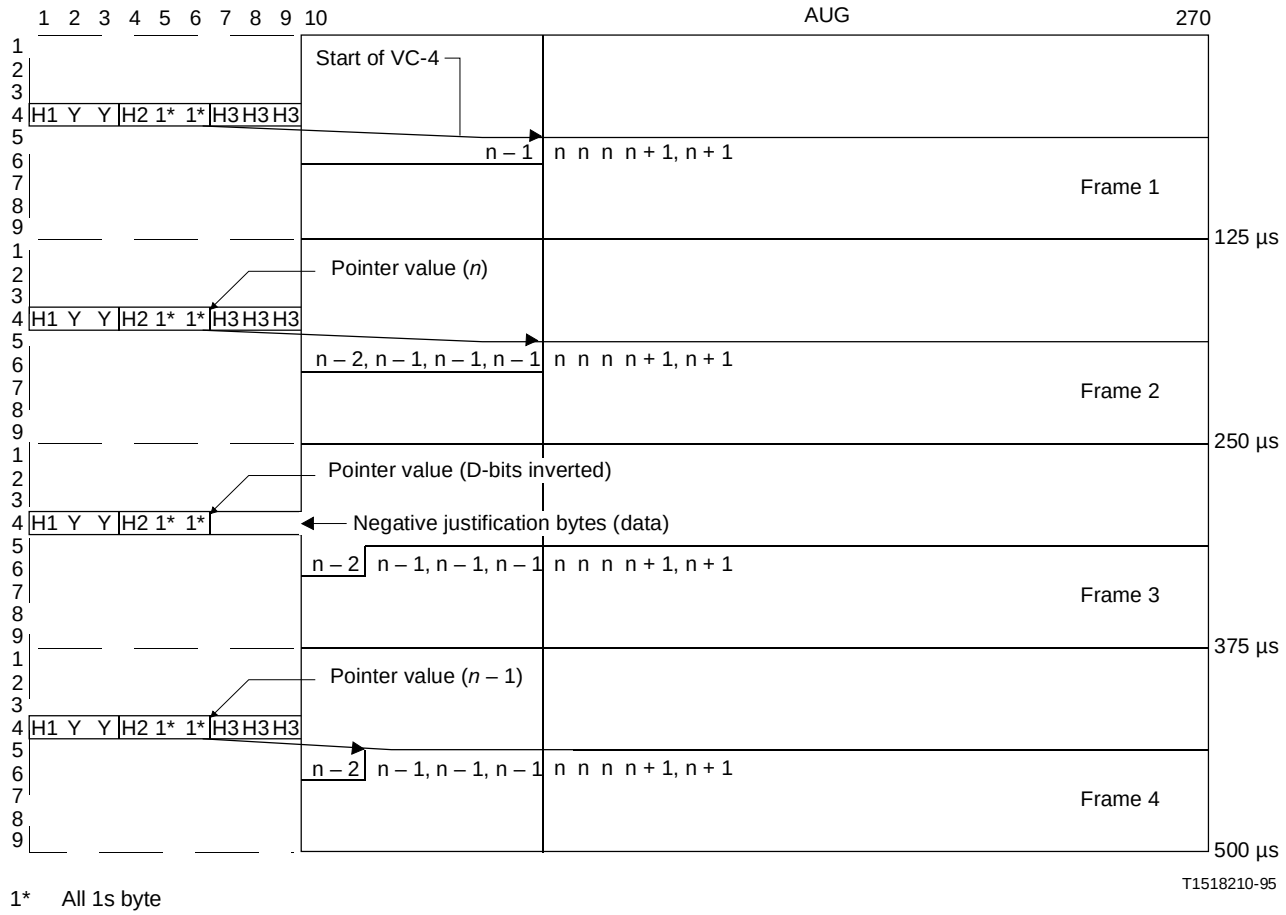


FIGURE 8-5/G.707

AU-3 pointer adjustment operation – positive justification

If the frame rate of the VC-n is too fast with respect to that of the AUG, then the alignment of the VC-n must periodically be advanced in time and the pointer value must be decremented by one. This operation is indicated by inverting bits 8, 10, 12, 14 and 16 (D-bits) of the pointer word to allow 5-bit majority voting at the receiver. Three negative justification bytes appear in the H3 bytes in the AU-4 frame containing inverted D-bits. Subsequent pointers will contain the new offset. This is illustrated in Figure 8-6.



1* All 1s byte
Y 1001SS11 (S bits are unspecified)

FIGURE 8-6/G.707

AU-4 pointer adjustment operation – negative justification

For AU-3 frames, a negative justification byte appears in the individual H3 byte of the AU-3 frame containing inverted D-bits. Subsequent pointers will contain the new offset. This is illustrated in Figure 8-7.

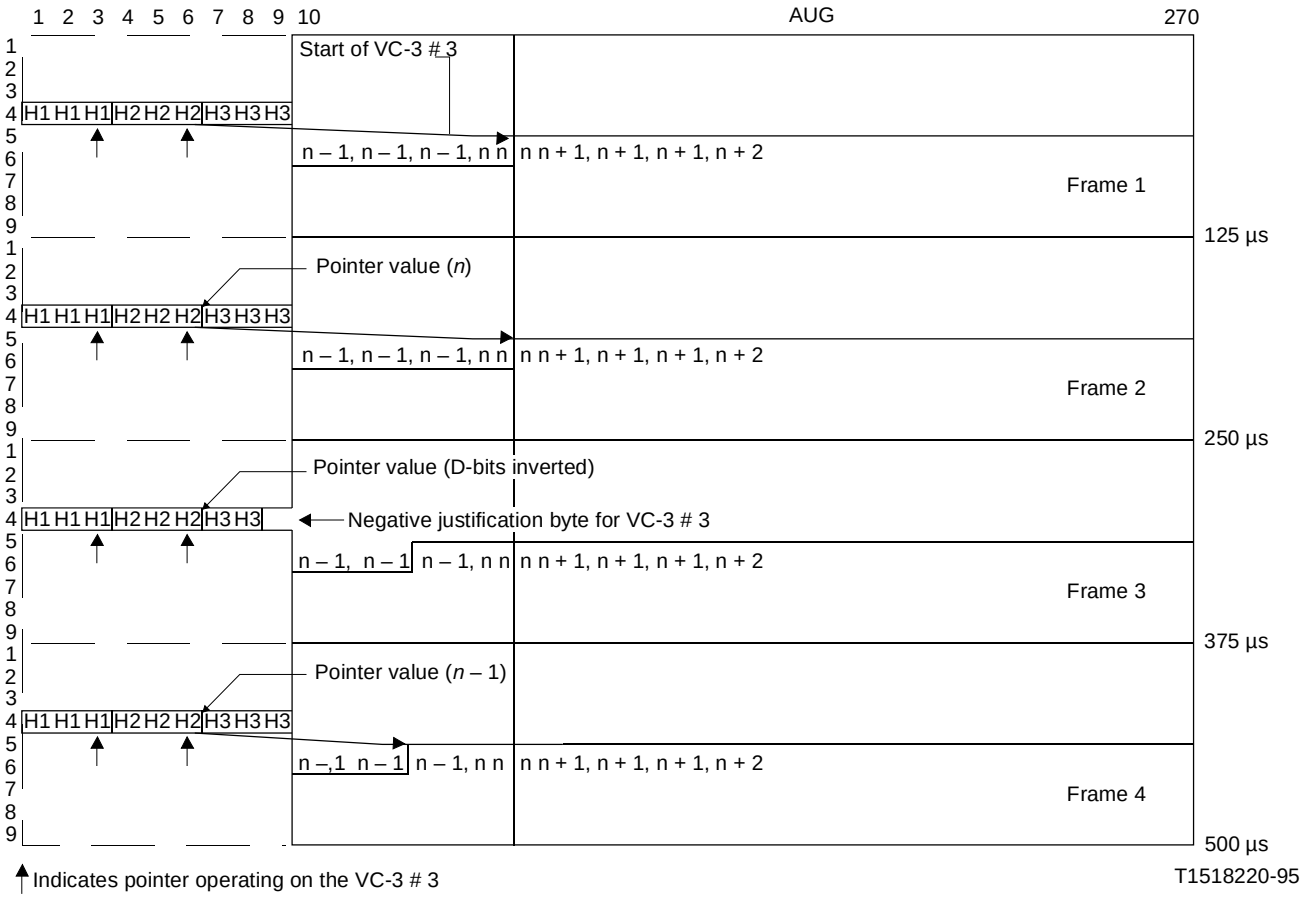


FIGURE 8-7/G.707

AU-3 pointer adjustment operation – negative justification

8.1.4 New Data Flag (NDF)

Bits 1-4 (N-bits) of the pointer word carry an NDF which allows an arbitrary change of the pointer value if that change is due to a change in the payload.

Four bits are allocated to the flag to allow error correction. Normal operation is indicated by a "0110" code in the N-bits. NDF is indicated by inversion of the N-bits to "1001". An NDF should be interpreted as enabled when three or more of the four bits match the pattern "1001". An NDF should be interpreted as disabled when three or more of the four bits match the pattern "0110". The remaining values (i.e. "0000", "0011", "0101", "1010", "1100" and "1111") should be interpreted as invalid. The new alignment is indicated by the pointer value accompanying the NDF and takes effect at the offset indicated.

8.1.5 Pointer generation

The following summarizes the rules for generating the AU-n pointers.

1) During normal operation, the pointer locates the start of the VC-n within the AU-n frame. The NDF is set to "0110".

2) The pointer value can only be changed by operation 3, 4 or 5.

3) If a positive justification is required, the current pointer value is sent with the I-bits inverted and the subsequent positive justification opportunity is filled with dummy information. Subsequent pointers contain the previous pointer value incremented by one. If the previous pointer is at its maximum value, the subsequent pointer is set to zero. No subsequent increment or decrement operation is allowed for at least three frames following this operation.

4) If a negative justification is required, the current pointer value is sent with the D-bits inverted and the subsequent negative justification opportunity is overwritten with actual data. Subsequent pointers contain the previous pointer value decremented by one. If the previous pointer value is zero, the subsequent pointer is set to its maximum value. No subsequent increment or decrement operation is allowed for at least three frames following this operation.

5) If the alignment of the VC-n changes for any reason other than rules 3 or 4, the new pointer value shall be sent accompanied by NDF set to "1001". The NDF only appears in the first frame that contains the new values. The new location of the VC-n begins at the first occurrence of the offset indicated by the new pointer. No subsequent increment or decrement operation is allowed for at least three frames following this operation.

8.1.6 Pointer interpretation

The following summarizes the rules for interpreting the AU-n pointers.

1) During normal operation, the pointer locates the start of the VC-n within the AU-n frame.

2) Any variation from the current pointer value is ignored unless a consistent new value is received three times consecutively or it is preceded by one of the rules 3, 4 or 5. Any consistent new value received three times consecutively overrides (i.e. takes priority over) rules 3 or 4.

3) If the majority of the I-bits of the pointer word are inverted, a positive justification operation is indicated. Subsequent pointer values shall be incremented by one.

4) If the majority of the D-bits of the pointer word are inverted, a negative justification operation is indicated. Subsequent pointer values shall be decremented by one.

5) If the NDF is interpreted as enabled, then the coincident pointer value shall replace the current one at the offset indicated by the new pointer value unless the receiver is in a state that corresponds to a loss of pointer.

8.1.7 AU-4 concatenation

AU-4s can be concatenated together to form an AU-4-Xc (X concatenated AU-4s) which can transport payloads requiring greater capacity than one Container-4 capacity.

8.1.7.1 Concatenation of contiguous AU-4s

A concatenation indication, used to show that the multi Container-4 payload carried in a single VC-4-Xc should be kept together, is contained in the AU-4 pointer. The capacity available for the mapping, the multi Container-4, is X times the capacity of the Container-4 (e.g. 599 040 Mbit/s for X = 4 and 2 396 160 kbit/s for X = 16). Columns 2 to X of the VC-4-Xc are specified as fixed stuff. The first column of the VC-4-Xc is used for the POH. The POH is assigned to the VC-4-Xc (e.g. the BIP-8 covers 261 X columns of the VC-4-Xc). The VC-4-Xc is illustrated in Figure 8-8.

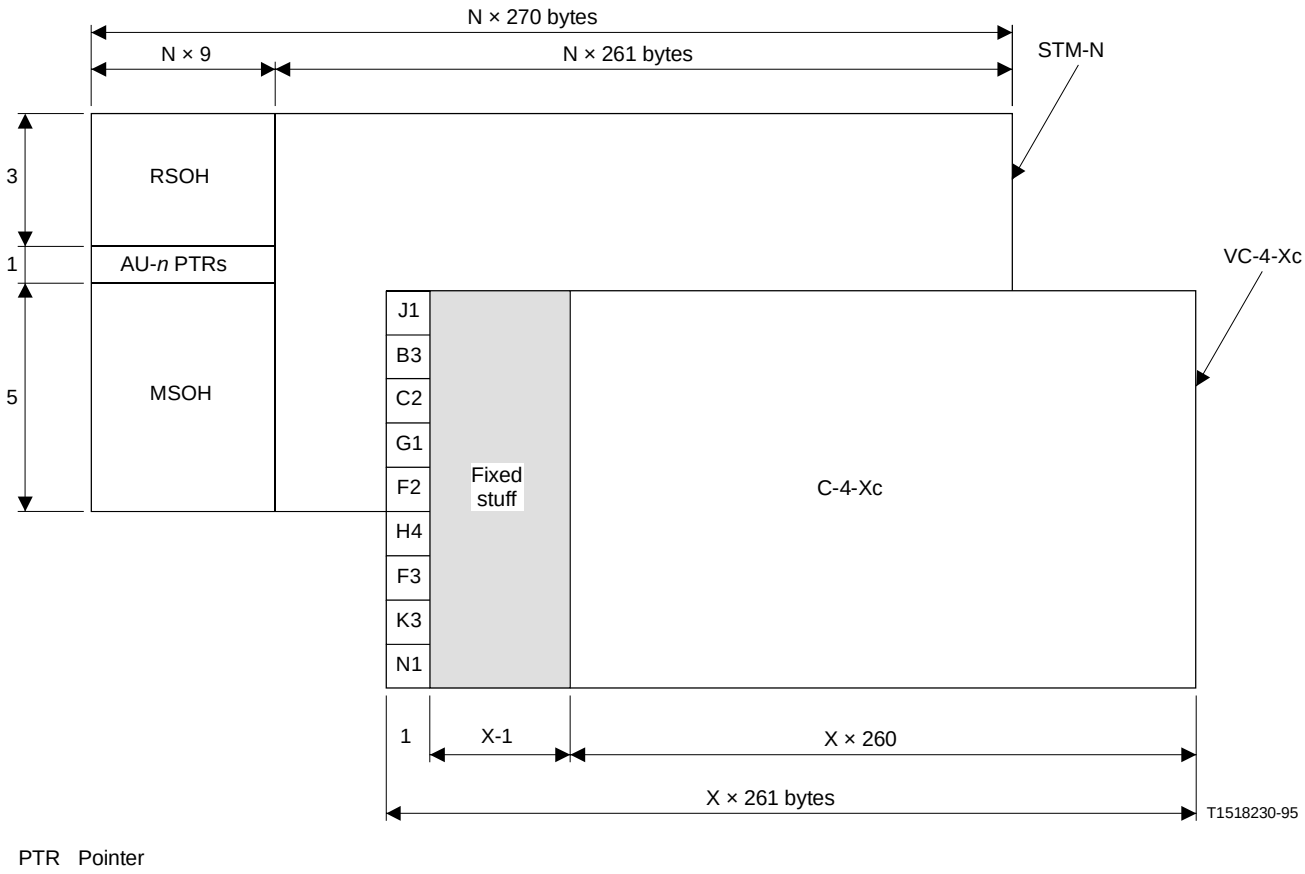


FIGURE 8-8/G.707

VC-4-Xc structure

The first AU-4 of an AU-4-Xc shall have a normal range of pointer values. All subsequent AU-4s within the AU-4-Xc shall have their pointer set to Concatenation Indication "1001" in bits 1-4, bits 5-6 unspecified, and ten "1"s in bits 7-16. The Concatenation Indication indicates that the pointer processors shall perform the same operations as performed on the first AU-4 of the AU-4-Xc.

8.1.7.2 Virtual concatenation of AU-4s

The virtual concatenation method for TU-2s is defined in 8.3.6.2. The details and the extensibility of the virtual concatenation method to the AU-4s are under study.

8.2 TU-3 pointer

The TU-3 pointer provides a method of allowing flexible and dynamic alignment of VC-3 within the TU-3 frame, independent of the actual content of the VC-3.

8.2.1 TU-3 pointer location

Three individual TU-3 pointers are contained in three separate H1, H2 and H3 bytes as shown in Figure 8-9.

8.2.2 TU-3 pointer value

The TU-3 pointer value contained in H1 and H2 designates the location of the byte where the VC-3 begins. The two bytes allocated to the pointer function can be viewed as one word as shown in Figure 8-3. The last ten bits (bits 7-16) of the pointer word carry the pointer value.

The TU-3 pointer value is a binary number with a range of 0-764 which indicates the offset between the pointer and the first byte of the VC-3 as shown in Figure 8-9.

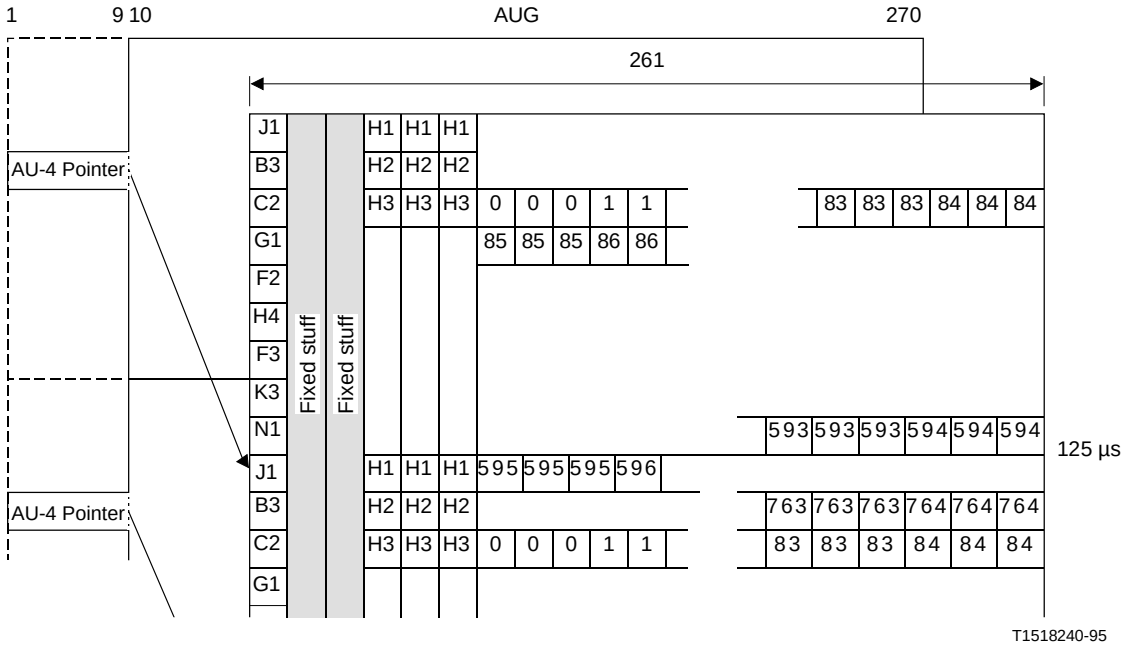


FIGURE 8-9/G.707

TU-3 pointer offset numbering

8.2.3 Frequency justification

If there is a frequency offset between the TU-3 frame rate and that of the VC-3, then the pointer value will be incremented or decremented as needed accompanied by a corresponding positive or negative justification byte. Consecutive pointer operations must be separated by at least three frames in which the pointer value remains constant.

If the frame rate of the VC-3 is too slow with respect to that of the TU-3 frame rate, then the alignment of the VC-3 must periodically slip back in time and the pointer must be incremented by one. This operation is indicated by inverting bits 7, 9, 11, 13 and 15 (I-bits) of the pointer word to allow 5-bit majority voting at the receiver. A positive justification byte appears immediately after the individual H3 byte in the TU-3 frame containing inverted I-bits. Subsequent TU-3 pointers will contain the new offset.

If the frame rate of the VC-3 is too fast with respect to that of the TU-3 frame rate, then the alignment of the VC-3 must be periodically advanced in time and the pointer must be decremented by one. This operation is indicated by inverting bits 8, 10, 12, 14 and 16 (D-bits) of the pointer word to allow 5-bit majority voting at the receiver. A negative justification byte appears in the individual H3 byte in the TU-3 frame containing inverted D-bits. Subsequent TU-3 pointers will contain the new offset.

8.2.4 New Data Flag (NDF)

Bits 1-4 (N-bits) of the pointer word carry an NDF which allows an arbitrary change of the value of the pointer if that change is due to a change in the VC-3.

Four bits are allocated to the flag to allow error correction. Normal operation is indicated by a "0110" code in the N-bits. NDF is indicated by inversion of the N-bits to "1001". An NDF should be interpreted as enabled when three or more of the four bits match the pattern "1001". An NDF should be interpreted as disabled when three or more of the four bits match the pattern "0110". The remaining values (i.e. "0000", "0011", "0101", "1010", "1100" and "1111") should be interpreted as invalid. The new alignment is indicated by the pointer value accompanying the NDF and takes effect at the offset indicated.

8.2.5 Pointer generation

The following summarizes the rules for generating the TU-3 pointers:

1) During normal operation, the pointer locates the start of the VC-3 within the TU-3 frame. The NDF is set to "0110".

2) The pointer value can only be changed by operation 3, 4 or 5.

3) If a positive justification is required, the current pointer value is sent with the I-bits inverted and the subsequent positive justification opportunity is filled with dummy information. Subsequent pointers contain the previous pointer value incremented by one. If the previous pointer is at its maximum value, the subsequent pointer is set to zero. No subsequent increment or decrement operation is allowed for at least three frames following this operation.

4) If a negative justification is required, the current pointer value is sent with the D-bits inverted and the subsequent negative justification opportunity is overwritten with actual data. Subsequent pointers contain the previous pointer value decremented by one. If the previous pointer value is zero, the subsequent pointer is set to its maximum value. No subsequent increment or decrement operation is allowed for at least three frames following this operation.

5) If the alignment of the VC-3 changes for any reason other than rules 3 or 4, the new pointer value shall be sent accompanied by the NDF set to "1001". The NDF only appears in the first frame that contains the new value. The new VC-3 location begins at the first occurrence of the offset indicated by the new pointer. No subsequent increment or decrement operation is allowed for at least three frames following this operation.

8.2.6 Pointer interpretation

The following summarizes the rules for interpreting the TU-3 pointers:

1) During normal operation the pointer locates the start of the VC-3 within the TU-3 frame.

2) Any variation from the current pointer value is ignored unless a consistent new value is received three times consecutively or it is preceded by one of rules 3, 4 or 5. Any consistent new value received three times consecutively overrides (i.e. takes priority over) rules 3 or 4.

3) If the majority of the I-bits of the pointer word are inverted, a positive justification is indicated. Subsequent pointer values shall be incremented by one.

4) If the majority of the D-bits of the pointer word are inverted, a negative justification is indicated. Subsequent pointer values shall be decremented by one.

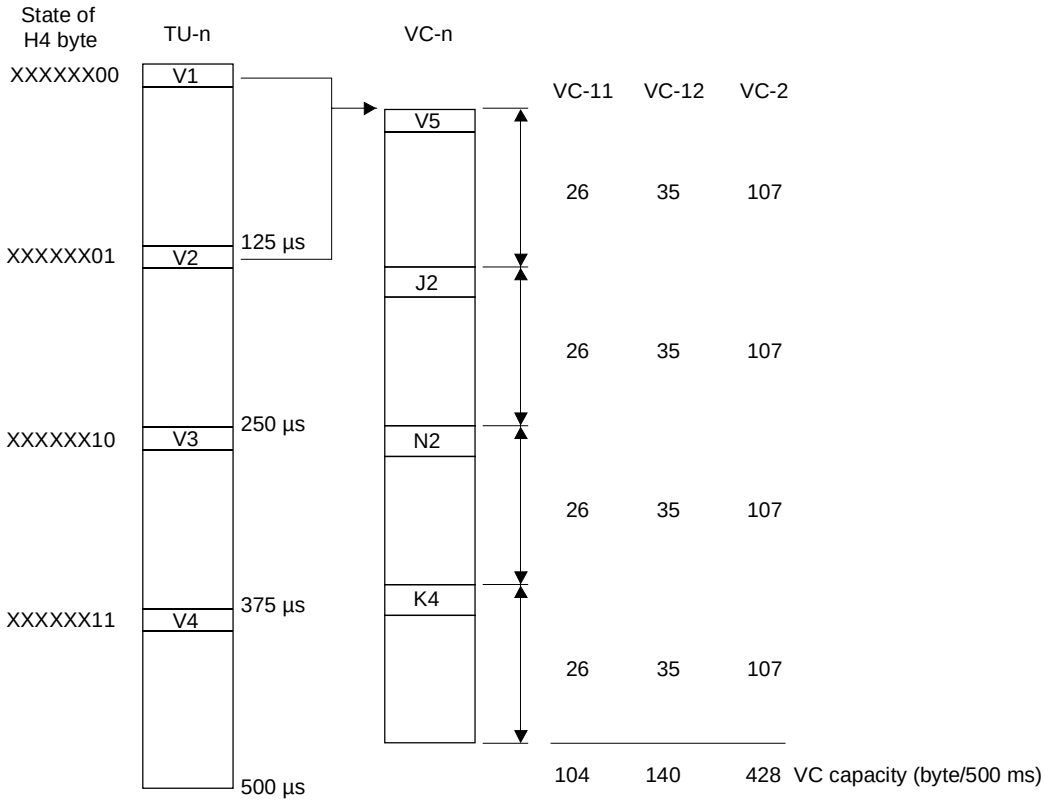
5) If the NDF is interpreted as enabled, then the coincident pointer value shall replace the current one at the offset indicated by the new pointer value unless the receiver is in a state that corresponds to a loss of pointer.

8.3 TU-2/TU-1 pointer

The TU-1 and TU-2 pointers provide a method of allowing flexible and dynamic alignment of the VC-2/VC-1 within the TU-1 and TU-2 multiframes, independent of the actual contents of the VC-2/VC-1.

8.3.1 TU-2/TU-1 pointer location

The TU-2/TU-1 pointers are contained in the V1 and V2 bytes as illustrated in Figure 8-10.



TU Tributary unit
VC Virtual container
V1 VC Pointer 1
V2 VC Pointer 2
V3 VC Pointer 3 (action)
V4 Reserved

NOTE – V1, V2, V3 and V4 bytes are part of the TU-n and are terminated at the pointer processor.

FIGURE 8-10/G.707

Virtual Container mapping in multiframed Tributary Unit

8.3.2 TU-2/TU-1 pointer value

The Tributary Unit pointer word is shown in Figure 8-11. The two S bits (bits 5 and 6) indicate the Tributary Unit type.

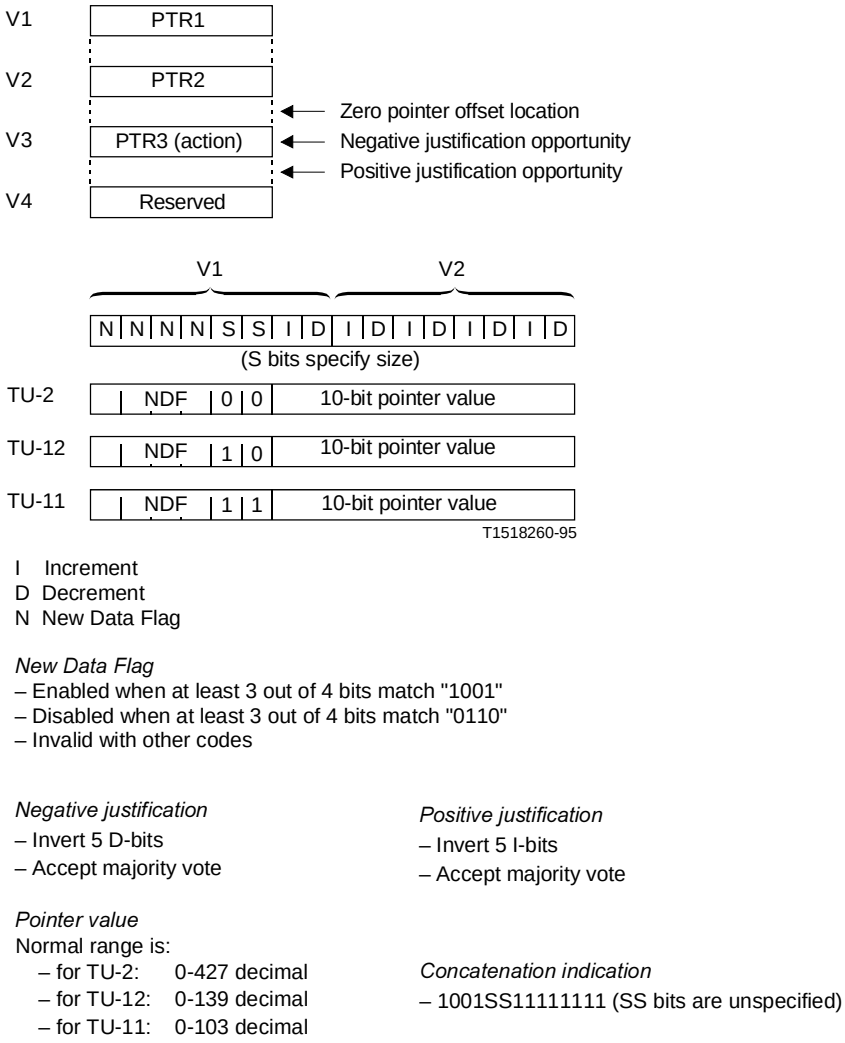


FIGURE 8-11/G.709

TU-2/TU-1 pointer coding

The pointer value (bits 7-16) is a binary number which indicates the offset from V2 to the first byte of the VC-2/VC-1. The range of the offset is different for each of the Tributary Unit sizes as illustrated in Figure 8-12. The pointer bytes are not counted in the offset calculation.

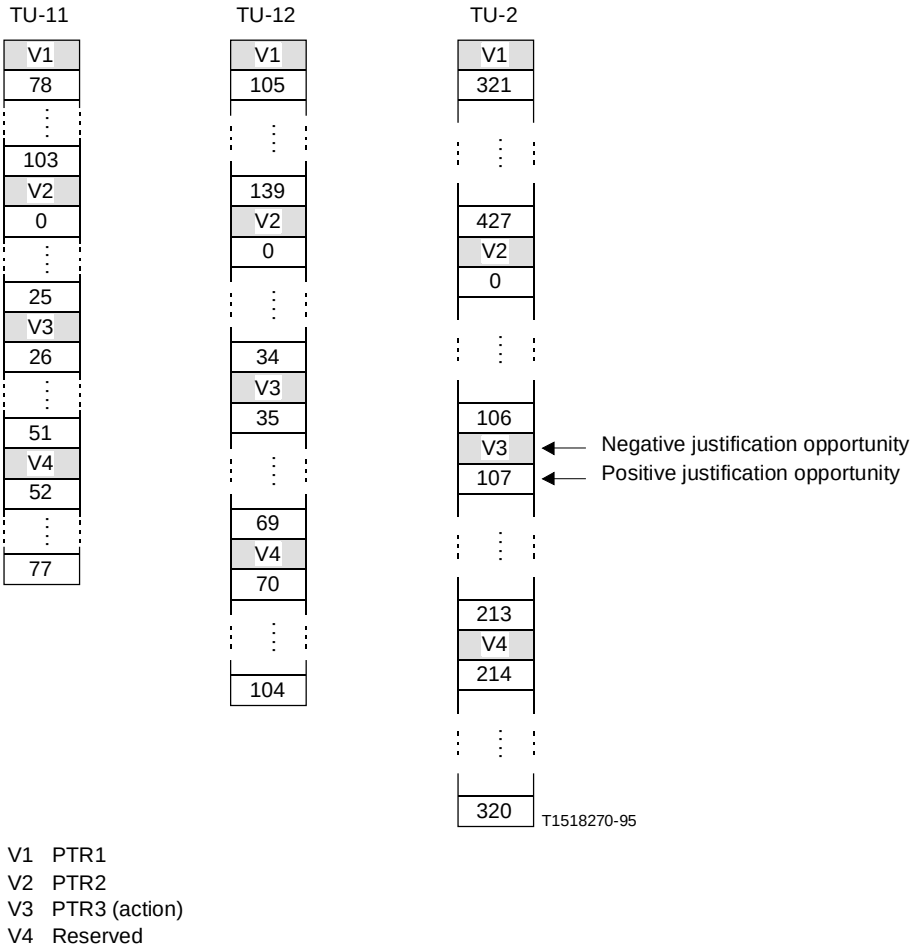


FIGURE 8-12/G.707

TU-2/TU-1 pointer offsets

8.3.3 TU-2/TU-1 frequency justification

The TU-2/TU-1 pointer is used to frequency justify the VC-2/VC-1 exactly in the same way that the TU-3 pointer is used to frequency justify the VC-3. A positive justification opportunity immediately follows the V3 byte. Additionally, V3 serves as the negative justification opportunity such that when the opportunity is taken, V3 is overwritten by data. This is also shown in Figure 8-12. The indication of whether or not a justification opportunity has been taken is provided by the I- and D-bits of the pointer in the current Tributary Unit multiframe. The value contained in V3 when not being used for a negative justification is not defined. The receiver is required to ignore the value contained in V3 whenever it is not used for negative justification.

8.3.4 New Data Flag (NDF)

Bits 1-4 (N-bits) of the pointer word carry an NDF. It is the mechanism which allows an arbitrary change of the value of a pointer.

As with the TU-3 pointer NDF, the normal value is "0110", and the value "1001" indicates a new alignment for the VC-n, and possibly new size. An NDF should be interpreted as enabled when three or more of the four bits match the pattern "1001". An NDF should be interpreted as disabled when three or more of the four bits match the pattern "0110". The remaining values (i.e. "0000", "0011", "0101", "1010", "1100" and "1111") should be interpreted as invalid. The new alignment is indicated by the pointer value and size value accompanying the NDF and takes effect at the offset indicated.

8.3.5 TU-2/TU-1 pointer generation and interpretation

The rules for generating and interpreting the TU-2/TU-1 pointer for the VC-2/VC-1 are an extension to the rules provided in 8.2.5 and 8.2.6 for the TU-3 pointer with the following modifications:

– The term TU-3 is replaced with TU-2/TU-1 and the term VC-3 is replaced with VC-2/VC-1.

8.3.6 TU-2 concatenation

TU-2s may be concatenated to form a TU-2-mc (m concatenated TU-2s) when a payload requires more than a Container-2. This forms a multi Container-2 payload which is carried in a single VC-2-mc. The rules by which TU-2s can be concatenated are separated into two categories:

– concatenation of contiguous TU-2s in the higher order VC-3;

– virtual concatenation of TU-2s in the higher order VC-4.

8.3.6.1 Concatenation of contiguous TU-2s in the higher order VC-3

TU-2s are contiguous in time in the higher order VC-3. The first TU-2 of an TU-2-mc shall have a normal range of pointer values. All subsequent TU-2s within the TU-2-mc shall have their pointer set to the Concatenation Indication ("1001" in bits 1-4, bits 5-6 unspecified, and all ones in bits 7-16 of the TU-2 pointer). The Concatenation Indication indicates that the TU-2 pointer processor performs all the operations as indicated by the first TU-2 pointer in the TU-2-mc.

With this type of concatenation the VC-2-mc contains a single Virtual Container POH which appears in VC-2 #1 of the VC-2-mc.

NOTE – With virtual concatenation (see 8.3.6.2), the available capacity of the VC-2-mc is lower than that with contiguous concatenation due to the fact that with the virtual concatenation each VC-2 carries its own POH contrary to contiguous concatenation where only the VC-2 # 1 of the VC-2-mc carries its own POH. In order to be able to interconnect VC-2-mcs using different types of concatenation, the mapping of signals in VC-2-mcs should be based on the lower available capacity, namely the capacity of VC-2-mc based on virtual concatenation. Stuffing bytes should be inserted in the VC-2-mc payload based upon contiguous concatenation to accommodate the difference in capacity.

8.3.6.2 Virtual concatenation of TU-2s in the higher order VC-4

This method of concatenation allows for the transport of a single VC-2-mc in $m \times$ TU-2 without the use of Concatenation Indication in the pointer bytes. The method only requires the path termination equipment to provide concatenation functionality.

Virtual concatenation requires the concatenated Tributary Unit signals at the origin of the path to be launched with the same pointer value. The so formed Tributary Units at each interface shall be kept in a single higher order VC-4.

When the higher order VC-4 is terminated, the restrictions that apply in passing the concatenated Tributary Units from one interface to another is that all of the concatenated Tributary Units are connected to a single higher order VC-4 and that the time sequencing of the concatenated Tributary Units is not altered.

Differences in delay of the individual concatenated VC-2 signals may occur due to pointer processing at intermediate equipment. The maximum difference in pointer value within a concatenated group at any interface is for further study. At the path termination the VC-2-mc can be reconstructed by using the pointer values for alignment.

Each concatenated VC-2 signal will carry its own POH. At the VC-2-mc path termination, the individual BIP-2s are aggregated to give a single BIP error monitor.

8.3.7 TU-2/TU-1 sizes

Bits 5 and 6 of TU-2/TU-1 pointer indicate the size of the TU-n. Three sizes are currently provided; they are defined in Table 3 below:

TABLE 3/G.707

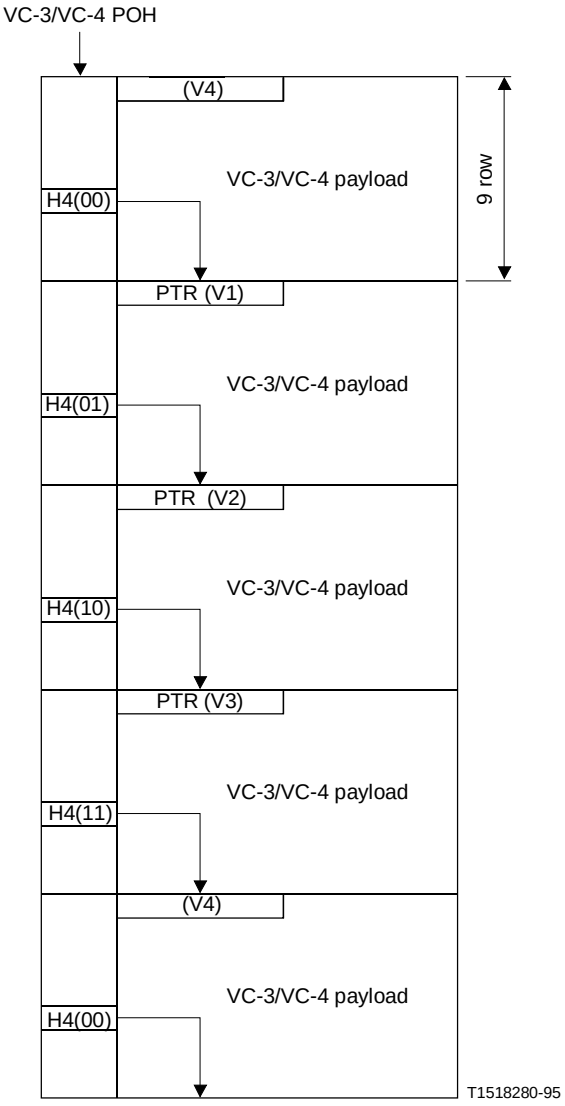
TU-2/TU-1 sizes

Size	Designation	TU-n pointer range (in 500 µs)
00	TU-2	0-427
10	TU-12	0-139
11	TU-11	0-103
NOTE – This technique is only used at the TU-2/TU-1 levels.		

8.3.8 TU-2/TU-1 multiframe indication byte

TU-2/TU-1 multiframe indication byte (H4) relates to the lowest level of the multiplexing structure and provides a 500 µs (4-frame) multiframe identifying frames containing the TU-2/TU-1 pointers. Figure 8-10 shows the VC-2/VC-1 mapping in the multiframed TU-2/TU-1.

The value of the H4 byte, read from the VC-4/VC-3 POH, identifies the frame phase of the next VC-4/VC-3 payload as shown in Figure 8-13. The coding of the H4 byte is illustrated in Figure 8-14.



In H4 (XY), XY represent bits 7 and 8 of H4

FIGURE 8-13/G.707

TU-1/2 500 µs multiframe indication using H4 byte

H4 bits 1 2 3 4 5 6 7 8	Frame N°	Time
X X X X X X 0 0	0	0
X X X X X X 0 1	1	
X X X X X X 1 0	2	
X X X X X X 1 1	3	500 µs TU-n multiframe

X undefined content

FIGURE 8-14/G.707

Tributary Unit multiframe indicator byte (H4) coding sequence

9 Overhead bytes description

9.1 Types of overhead

Several types of overhead have been identified for application in the SDH.

9.1.1 SOH

SOH information is added to the information payload to create an STM-N. It includes block framing information and information for maintenance, performance monitoring and other operational functions. The SOH information is further classified into Regenerator Section Overhead (RSOH) which is terminated at regenerator functions and Multiplex Section Overhead (MSOH) which passes transparently through regenerators and is terminated where the AUGs are assembled and disassembled.

The rows 1-3 of the SOH are designated as RSOH while rows 5-9 are designated to be MSOH. This is illustrated in Figure 9-2 for the case of STM-1.

The SOH description is given in 9.2.

9.1.2 Virtual Container POH

Virtual Container POH provides for integrity of communication between the point of assembly of a Virtual Container and its point of disassembly. Two categories of Virtual Container POH have been identified:

– *Higher order Virtual Container POH (VC-4/VC-3 POH)*

  VC-3 POH is added to either an assembly of TUG-2s or a Container-3 to form a VC-3. VC-4 POH is added to either an assembly of TUG-3s or a Container-4 to form a VC-4. Amongst the functions included within this overhead are Virtual Container path performance monitoring, alarm status indications, signals for maintenance purposes and multiplex structure indications (VC-4/VC-3 composition).

– *Lower order Virtual Container POH (VC-3/VC-2/VC-1 POH)*

  Lower order VC-n (n = 1, 2, 3) POH is added to the Container-n to form a VC-n. Among the functions included in this overhead are Virtual Container path performance monitoring, signals for maintenance purposes and alarm status indications.

The POH descriptions are given in 9.3.

9.2 SOH description

9.2.1 SOH bytes location

The location of SOH bytes within an STM-N frame is identified by a three-coordinate vector S (a, b, c) where a (1 to 3, 5 to 9) represents the row number, b (1 to 9) represents a multi-column number and c (1 to N) represents the depth of the interleave within the multi-column. This is illustrated in Figure 9-1.

The relationship between the row and column numbers and the coordinates is given by:

- Row = a
- Column = N (b–1) + c

For example the K1 byte in an STM-1 is located at S (5, 4, 1) or at [5, 4] in [row, column] notation.

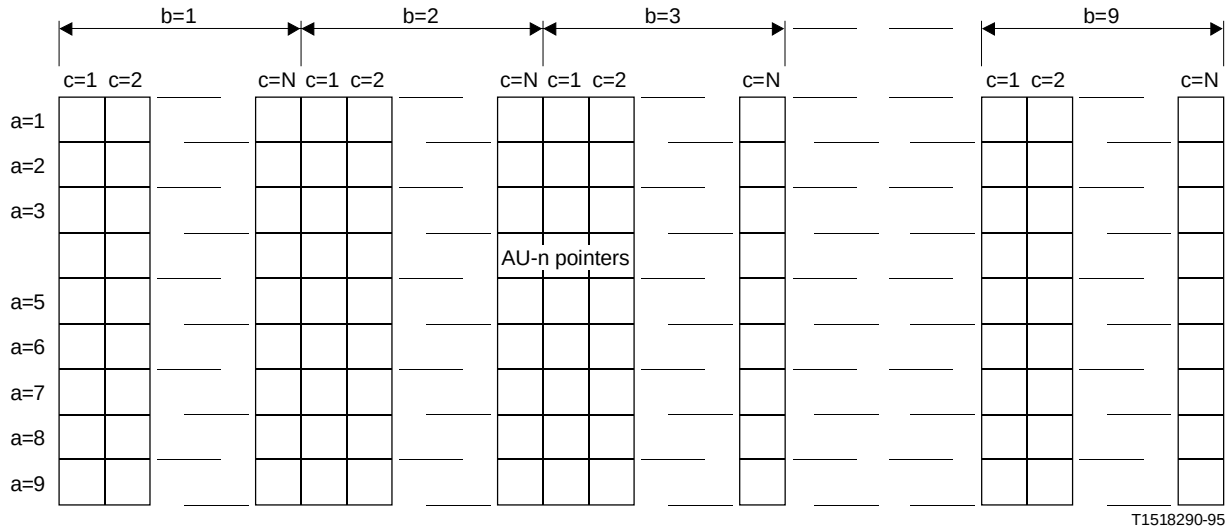
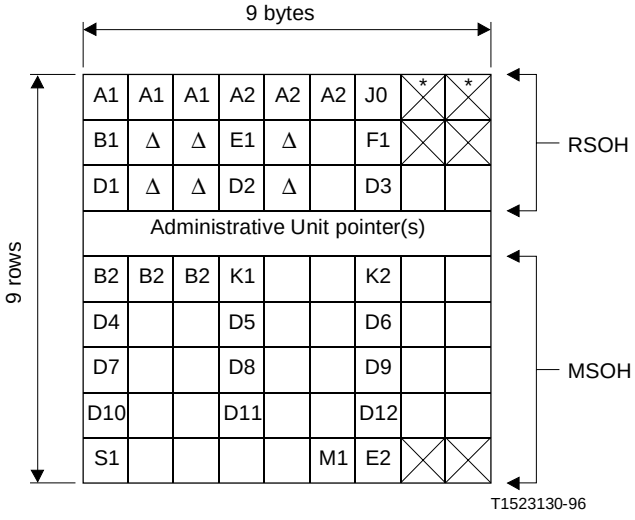


FIGURE 9-1/G.707

Numbering of SOH byte locations for STM-N

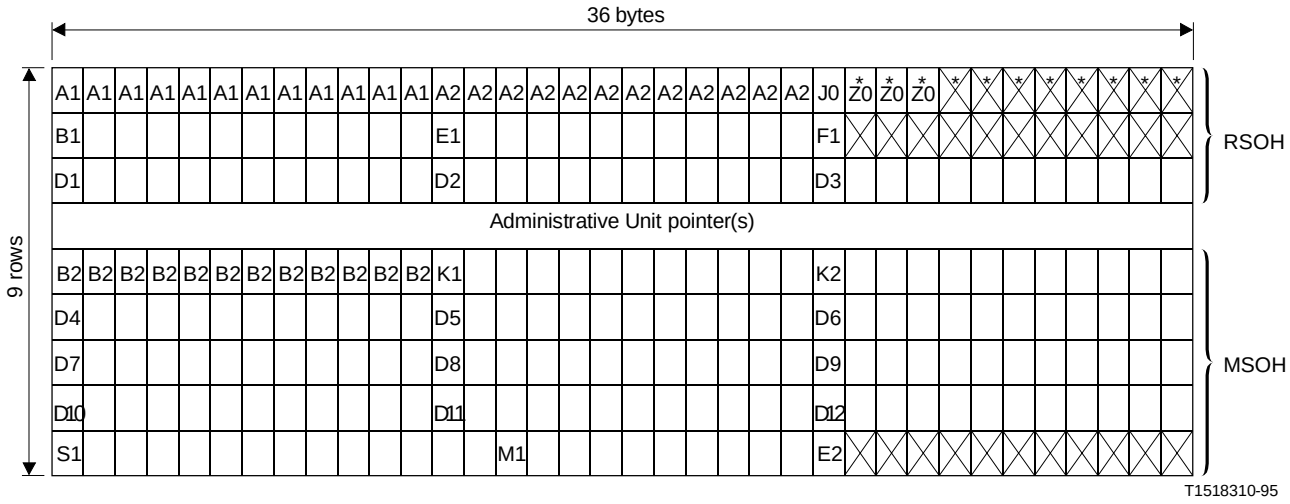
The assignment of the various SOH bytes in the STM-1/4/16/64 frames is illustrated in Figures 9-2, 9-3, 9-4 and 9-5.



NOTE – All unmarked bytes are reserved for future international standardization (for media dependent, additional national use and other purposes).

FIGURE 9-2/G.707

STM-1 SOH



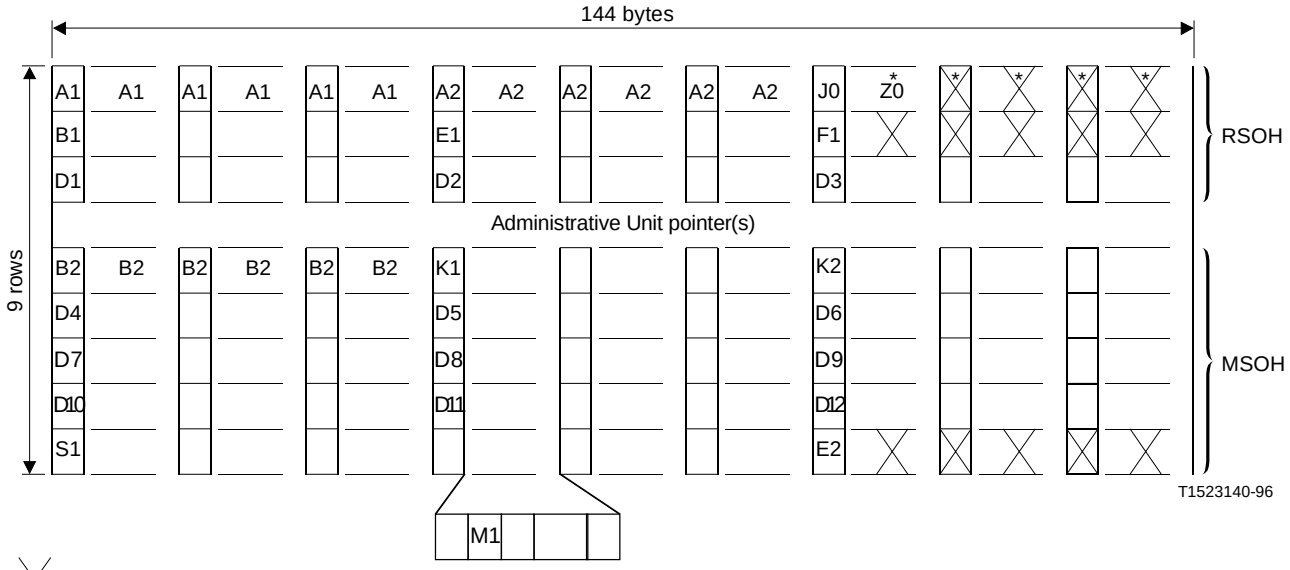
Bytes reserved for national use

* Unscrambled bytes. Therefore care should be taken with their content

NOTE – All unmarked bytes are reserved for future international standardization (for media dependent, additional national use and other purposes).

FIGURE 9-3/G.707

STM-4 SOH



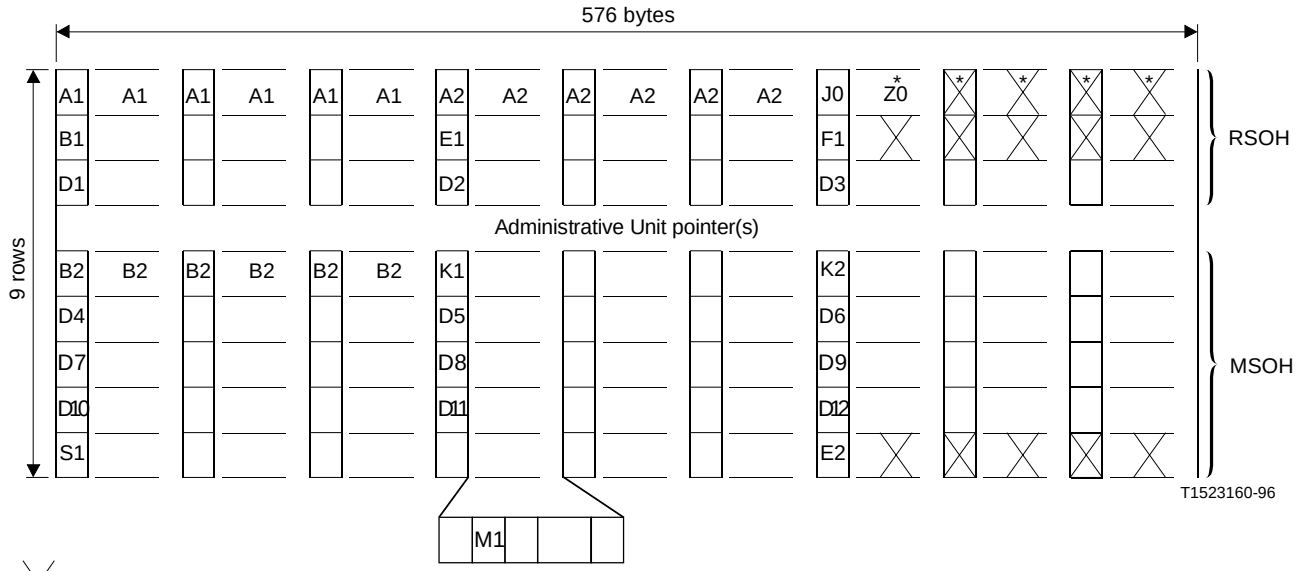
Bytes reserved for national use

* Unscrambled bytes. Therefore care should be taken with their content

NOTE – All unmarked bytes are reserved for future international standardization (for media dependent, additional national use and other purposes).

FIGURE 9-4/G.707

STM-16 SOH



Bytes reserved for national use

* Unscrambled bytes. Therefore care should be taken with their content

NOTE – All unmarked bytes are reserved for future international standardization (for media dependent, additional national use and other purposes).

FIGURE 9-5/G.707

STM-64 SOH

9.2.2 SOH bytes description

9.2.2.1 Framing: A1, A2

Two types of bytes are defined for framing:

– A1: 11110110

– A2: 00101000

The frame alignment word of an STM-N frame is composed of $3 \times N$ A1 bytes followed by $3 \times N$ A2 bytes.

9.2.2.2 Regenerator Section Trace: J0

The J0 byte located at S (1, 7, 1) or [1, 6N+1] in an STM-N is allocated to a Regenerator Section Trace. This byte is used to transmit repetitively a Section Access Point Identifier so that a section receiver can verify its continued connection to the intended transmitter. Within a national network, or within the domain of a single operator, this Section Access Point Identifier may use either a single byte (containing the code 0-255) or the Access Point Identifier format as defined in clause 3/G.831. At international boundaries, or at the boundaries between the networks of different operators, the format defined in clause 3/G.831 shall be used unless otherwise mutually agreed by the operators providing the transport.

A 16-byte frame is defined for the transmission of Section Access Point Identifiers where these conform to the definition contained in clause 3/G.831. The first byte of the string is a frame start marker and includes the result of a CRC-7 calculation over the previous frame. The following 15 bytes are used for the transport of 15 T.50 characters (international Reference Version) required for the Section Access Point Identifier. The 16-byte frame description is given in Table 4 below:

TABLE 4/G.707

16-byte frame for Trail APId

Byte #	Value (bit 1, 2, … ,8)							
1	1	C_1	C_2	C_3	C_4	C_5	C_6	C_7
2	0	X	X	X	X	X	X	X
3	0	X	X	X	X	X	X	X
:	:				:			
16	0	X	X	X	X	X	X	X

NOTES

1 $C_1C_2C_3C_4C_5C_6C_7$ is the result of the CRC-7 calculation over the previous frame. $C_1$is the MSB. The description of this CRC-7 calculation is given in Annex B.

2 0XXXXXXX represents a T.50 character.

In the case of interworking of equipment implementing the STM identifier functionality (see Note) and equipment employing the Regenerator Section Trace function, the latter shall interpret the pattern "0000001" in J0 as "Regenerator Section Trace - unspecified". This unspecified Regenerator Section Trace can also be used if no use of the Regenerator Section Trace is made.

NOTE – STM identifier: C1

In earlier versions of the Recommendation, the content of bytes located at S (1, 7, 1) or [1, 6N+1] to S (1, 7, N) or [1, 7N] was defined as a unique identifier indicating the binary value of the multi-column, interleave depth coordinate, c. It may have been used to assist in frame alignment.

9.2.2.3 Spare: Z0

These bytes, which are located at positions S (1, 7, 2) or [1, 6N+2] to S (1, 7, N) or [1, 7N], are reserved for future international standardization.

In case of interworking of equipment implementing the STM identifier functionality (see Note) and equipment employing the Regenerator Section Trace function, these bytes shall be as defined in the note below.

NOTE – STM identifier: C1

In earlier versions of the Recommendation, the content of bytes located at S (1, 7, 1) or [1, 6N+1] to S (1, 7, N) or [1, 7N] was defined as a unique identifier indicating the binary value of the multi-column, interleave depth coordinate, c. It may have been used to assist in frame alignment.

9.2.2.4 BIP-8: B1

One byte is allocated for regenerator section error monitoring. This function shall be a Bit Interleaved Parity 8 (BIP-8) code using even parity. The BIP-8 is computed over all bits of the previous STM-N frame after scrambling and is placed in byte B1 of the current frame before scrambling. (For details of the scrambling process see 6.5.)

NOTE – Bit Interleaved Parity-X (BIP-X) code is defined as a method of error monitoring. With even parity an X-bit code is generated by the transmitting equipment over a specified portion of the signal in such a manner that the first bit of the code provides even parity over the first bit of all X-bit sequences in the covered portion of the signal, the second bit provides even parity over the second bit of all X-bit sequences within the specified portion, etc. Even parity is generated by setting the BIP-X bits so that there is an even number of 1s in each monitored partition of the signal. A monitored partition comprises all bits which are in the same bit position within the X-bit sequences in the covered portion of the signal. The covered portion includes the BIP-X.

9.2.2.5 Orderwire: E1, E2

These two bytes may be used to provide orderwire channels for voice communication. E1 is part of the RSOH and may be accessed at regenerators. E2 is part of the MSOH and may be accessed at multiplex section terminations.

9.2.2.6 User channel: F1

This byte is reserved for user purposes (e.g. to provide temporary data/voice channel connections for special maintenance purposes).

9.2.2.7 Data Communication Channel (DCC): D1-D12

A 192 kbit/s channel is defined using bytes D1, D2 and D3 as a Regenerator Section DCC.

A 576 kbit/s channel is defined using bytes D4 to D12 as a Multiplex Section DCC.

9.2.2.8 BIP-N×24: B2

The B2 bytes are allocated for a multiplex section error monitoring function. This function shall be a Bit Interleaved Parity N × 24 code (BIP-N × 24) using even parity. The BIP-N × 24 is computed over all bits of the previous STM-N frame except for the first three rows of SOH and is placed in bytes B2 of the current frame before scrambling.

9.2.2.9 Automatic Protection Switching (APS) channel: K1, K2 (b1-b5)

Two bytes are allocated for APS signalling for the protection of the multiplex section. The bit assignments for these bytes and the bit oriented protocol are given in Annex A/G.783.

9.2.2.10 MS-RDI: K2 (b6-b8)

The Multiplex Section Remote Defect Indication (MS-RDI) is used to return an indication to the transmit end that the received end has detected an incoming section defect or is receiving MS-AIS. MS-RDI is generated by inserting a "110" code in positions 6, 7 and 8 of the K2 byte before scrambling.

9.2.2.11 Synchronization status: S1 (b5-b8)

Bits 5 to 8 of byte S (9, 1, 1) or [9, 1] are allocated for Synchronization Status Messages. Table 5 gives the assignment of bit patterns to the four synchronization levels agreed to within ITU-T. Two additional bit patterns are assigned: one to indicate that quality of the synchronization is unknown and the other to signal that the section should not be used for synchronization. The remaining codes are reserved for quality levels defined by individual Administrations.

TABLE 5/G.707

Assignment of bit patterns

S1 bits b5-b8	SDH synchronization quality level description
0000	Quality unknown (Existing Sync. Network)
0001	Reserved
0010	Rec. G.811
0011	Reserved
0100	Rec. G.812 transit
0101	Reserved
0110	Reserved
0111	Reserved
1000	Rec. G.812 local
1001	Reserved
1010	Reserved
1011	Synchronous Equipment Timing Source (SETS)
1100	Reserved
1101	Reserved
1110	Reserved
1111	Do not use for synchronization (Note)
NOTE – This message may be emulated by equipment failures and will be emulated by a Multiplex Section AIS signal. The assignment of the Do not use for Synchronization quality level message is mandatory because the receipt of a Multiplex Section AIS is not necessarily interpreted as an indication of a physical failed synchronization source interface port. This assignment allows this state to be recognized without interaction with the Multiplex Section AIS detection process.	

9.2.2.12 MS-REI: M1

One byte is allocated for use as a Multiplex Section REI (Remote Error Indication).

NOTE 1 – Interworking of equipment that supports MS-REI and equipment that does not support MS-REI cannot be achieved automatically.

For STM-N levels this byte conveys the count (in the range of [0, 255]) of interleaved bit blocks that have been detected in error by the BIP-24×N (B2). For rates of STM-16 and above, this value shall be truncated to 255.

STM-1, M1 generation: the byte shall be set to convey the count of interleaved bit blocks that have been detected in error by the BIP-24 in the range of [0, 24].

STM-1, M1 interpretation: the value in the byte shall be interpreted, for interworking with equipment generating a 7 bit code that represents the number of BIP-24 violations, as follows:

M1[2-8] code, bits 234 5678	Code interpretation
000 0000	0 BIP violations
000 0001	1 BIP violation
000 0010	2 BIP violations
000 0011	3 BIP violations
:	:
001 1000	24 BIP violations
001 1001	0 BIP violations
001 1010	0 BIP violations
:	:
111 1111	0 BIP violations
NOTE – Bit 1 of byte M1 is ignored.	

STM-4, M1 generation: the byte shall be set to convey the count of interleaved bit blocks that have been detected in error by the BIP-96 in the range of [0, 96].

STM-4, M1 interpretation: the value in the byte shall be interpreted, for interworking with equipment generating a 7-bit code that represents the number of BIP-96 violations, as follows:

M1[2-8] code, bits 234 5678	Code interpretation
000 0000	0 BIP violations
000 0001	1 BIP violation
000 0010	2 BIP violations
000 0011	3 BIP violations
000 0100	4 BIP violations
000 0101	5 BIP violations
:	:
110 0000	96 BIP violations
110 0001	0 BIP violations
110 0010	0 BIP violations
:	:
111 1111	0 BIP violations
NOTE – Bit 1 of byte M1 is ignored.	

STM-16, M1 generation: the byte shall be set to convey the count of interleaved bit blocks that have been detected in error by the BIP-384 (in the range of [0, 255]) where the value conveyed is truncated at 255.

STM-16, M1 interpretation: the value in the byte shall be interpreted as follows:

M1[1-8] code, bits 1234 5678	Code interpretation
0000 0000	0 BIP violations
0000 0001	1 BIP violation
0000 0010	2 BIP violations
0000 0011	3 BIP violations
0000 0100	4 BIP violations
0000 0101	5 BIP violations
:	:
1111 1111	255 BIP violations

STM-64, M1 generation: the byte shall be set to convey the count of interleaved bit blocks that have been detected in error by the BIP-1536 (in the range of [0, 255]) where the value conveyed is truncated at 255.

STM-64, M1 interpretation: the value in the byte shall be interpreted as follows:

M1[1-8] code, bits 1234 5678	Code interpretation
0000 0000	0 BIP violations
0000 0001	1 BIP violation
0000 0010	2 BIP violations
0000 0011	3 BIP violations
0000 0100	4 BIP violations
0000 0101	5 BIP violations
:	:
1111 1111	255 BIP violations

NOTE 2 – The Multiplex Section block structure is still under discussion in Study Group 13. The description given above for the MS-REI is relevant for an STM-N Multiplex Section block structure of 24×N blocks. Appendix VIII, provided for information, contains a possible definition of M1 which would be applicable if a N block structure were defined.

9.2.3 Reduced SOH functionalities interface

For some applications (e.g. intra-station interface), an interface with reduced SOH functionalities can be used. The SOH bytes to be used for this interface are given in Table 6 below:

TABLE 6/G.707

Reduced SOH functionalities interface

SOH bytes	Optical interface	Electrical interface
A1, A2	Required	Required
J0-Z0/C1	(Note 1)	(Note 1)
B1	Not applicable	Not applicable
E1	Optional	Optional
F1	Not applicable	Not applicable
D1-D3	Not applicable	Not applicable
B2	Required	Required
K1, K2 (APS)	Optional	Not applicable
K2 (MS-AIS)	(Note 2)	(Note 2)
K2 (MS-RDI)	Required	Required
D4-D12	Not applicable	Not applicable
S1	(Note 2)	(Note 2)
M1	(Note 2)	(Note 2)
E2	Not applicable	Not applicable
Other bytes	Not applicable	Not applicable

NOTES

1 For equipment implementing an STM identifier (bytes C1) function, the use of byte S (1, 7, 1) is optional for STM-1 and the use of bytes S (1, 7, 1) to S (1, 7, N) is required for STM-4/16/64. For equipment implementing a Regenerator Section Trace (bytes J0) and spare (bytes Z0) functions, the use of Z0 bytes S (1, 7, 2) to S (1, 7, N) requires further study. Refer also to 9.2.2.2 and 9.2.2.3.

2 Requires further study.

3 The following definitions apply:

– Required: these signals at the interface shall contain valid information as defined by this Recommendation.

– Optional: valid information may or may not be present in these signals. Use of these functions shall be a local matter.

– Not applicable: this function is not defined at the interface.

9.3 POH descriptions

9.3.1 VC-4-Xc/VC-4/VC-3 POH

The VC-4-Xc POH is located in the first column of the 9-row by X × 261-column VC-4-Xc structure.

The VC-4 POH is located in the first column of the 9-row by 261-column VC-4 structure.

The VC-3 POH is located in the first column of the 9-row by 85-column VC-3 structure.

The VC-4-Xc/VC-4/VC-3 POH consists of 9 bytes denoted J1, B3, C2, G1, F2, H4, F3, K3 and N1 (see Figures 8-8, 7-2 and 7-3). These bytes are classified as follows:

– Bytes or bits used for end-to-end communication with independent payload function: J1, B3, C2, G1, K3 (b1-b4).

– Payload type specific bytes: H4, F2, F3.

– Bits reserved for future international standardization: K3 (b5-b8).

– Byte which can be overwritten in an operator domain (without affecting the end-to-end performance monitoring facility of the byte B3): N1.

NOTE – Payload dependent and payload independent information is communicated by different codings in C2 byte and bits 5 to 7 of G1 byte.

9.3.1.1 Path trace: J1

This is the first byte in the Virtual Container; its location is indicated by the associated AU-n (n = 3, 4) or TU-3 pointer. This byte is used to transmit repetitively a Path Access Point Identifier so that a path receiving terminal can verify its continued connection to the intended transmitter. Within a national network or within the domain of a single operator, this Path Access Point Identifier may use either a 64-byte free format string or the Access Point Identifier format as defined in clause 3/G.831. At international boundaries, or at the boundaries between the networks of different operators, the format defined in clause 3/G.831 shall be used unless otherwise mutually agreed by the operators providing the transport. Where the format as defined in clause/G.831 is transferred in the 64-byte field, it shall be repeated four times.

A 16-byte frame is defined for the transmission of Access Point Identifiers where these conform to the definition contained in clause 3/G.831. This 16-byte frame is identical to the 16-byte frame defined in 9.2.2.2 for the description of the byte J0.

9.3.1.2 Path BIP-8: B3

One byte is allocated in each VC-4-Xc/VC-4/VC-3 for a path error monitoring function. This function shall be a BIP-8 code using even parity. The path BIP-8 is calculated over all bits of the previous VC-4-Xc/VC-4/VC-3 before scrambling. The computed BIP-8 is placed in the B3 byte of the current VC-4-Xc/VC-4/VC-3 before scrambling.

9.3.1.3 Signal label: C2

One byte is allocated to indicate the composition or the maintenance status of the VC-4-Xc/VC-4/VC-3. Table 7 below, which is based on Hex code, provides codes for this byte.

TABLE 7/G.707
C2 byte coding

MSB 1 2 3 4	LSB 5 6 7 8	Hex code (Note 1)	Interpretation
0 0 0 0	0 0 0 0	00	Unequipped or supervisory-unequipped (Note 2)
0 0 0 0	0 0 0 1	01	Equipped - non-specific (Note 3)
0 0 0 0	0 0 1 0	02	TUG structure
0 0 0 0	0 0 1 1	03	Locked TU-n (Note 4)
0 0 0 0	0 1 0 0	04	Asynchronous mapping of 34 368 kbit/s or 44 736 kbit/s into the Container-3
0 0 0 1	0 0 1 0	12	Asynchronous mapping of 139 264 kbit/s into the Container-4
0 0 0 1	0 0 1 1	13	ATM mapping
0 0 0 1	0 1 0 0	14	MAN (DQDB) mapping (Note 5)
0 0 0 1	0 1 0 1	15	FDDI mapping (Note 5)
1 1 1 1	1 1 1 0	FE	Test signal, O.181 specific mapping (Note 6)
1 1 1 1	1 1 1 1	FF	VC-AIS (Note 7)

MAN Metropolitan Area Network

DQDB Distributed Queue Dual Bus

FDDI Fibre Distributed Data Interface

NOTES

1 There are 245 spare codes left for future use.

2 Value "0" indicates "VC-4-Xc/VC-4/VC-3 path unequipped or supervisory-unequipped". This value shall be originated if the section is complete but there is no VC-4-Xc/VC-4/VC-3 path originating equipment.

3 Value "1" is only to be used in cases where a mapping code is not defined in the above table. For interworking with old equipment (i.e. designed to transmit only the values "0" and "1"), the following conditions apply:

– for backward compatibility, old equipment shall interpret any value received other than value "0" as an equipped condition;

– for forward compatibility, when receiving value "1" from old equipment, new equipment shall not generate a signal label mismatch alarm.

4 The code "03" shall, for backward compatibility purposes, continue to be interpreted as previously defined even if the locked mode byte synchronous mappings are not defined any more.

5 Mapping for MAN (DQDB) and FDDI are for further study.

6 Any mapping defined in Recommendation O.181 which does not correspond to a mapping defined in Recommendation G.707 falls in this category.

7 Only for networks supporting the transport of Tandem Connection signals.

8 Identification of the payload as whether it is AU-4 or AU-3 structured can be indicated by checking for the Y bytes in the AU-n pointer area.

9.3.1.4 Path status: G1

One byte is allocated to convey the path status and performance back to a VC-4-Xc/VC-4/VC-3 trail termination source as detected by a trail termination sink. This feature permits the status and performance of the complete duplex trail to be monitored at either end, or at any point along that trail. The allocation of bits in G1 is illustrated in Figure 9-6.

Bits 1 through 4 convey the count of interleaved-bit blocks that have been detected in error by the trail termination sink using the path BIP-8 code (B3). This count has nine legal values, namely 0-8 errors. The remaining seven possible values represented by these four bits can only result from some unrelated condition and shall be interpreted as zero errors.

Bit 5 is set to 1 to indicate a VC-4-Xc/VC-4/VC-3 path Remote Defect Indication (RDI), otherwise it is set to 0. The VC-4-Xc/VC-4/VC-3 path RDI is sent back towards the trail termination source if either an AU-4-Xc/AU-4/AU-3 or TU-3 server signal failure or trail signal failure is being detected by the trail termination sink. RDI does not indicate remote payload or adaptation defects. Connectivity and server defects are indicated by RDI; for further detail see Recommendation G.783.

Bits 6 and 7 are reserved for an optional use described in VII.1. If this option is not used, bits 6 and 7 shall be set to 00 or 11. A receiver is required to be able to ignore the contents of these bits. The use of the optional function is at the discretion of the owner of the trail termination source generating the G1 byte.

Bit 8 is allocated for future use. This bit has no defined value. The receiver is required to ignore its content.

FIGURE 9-6/G.707

VC-4-Xc/VC-4/VC-3 path status (G1)

NOTE – For backward compatibility with equipment complying with the 1993 version of Recommendation I.432, new equipment may use "100" or "111" codes in bits 5 to 7 of G1 to indicate a remote Loss of Cell Delineation (LCD). New equipment may do this only when interworking with old equipment.

9.3.1.5 Path user channels: F2, F3

These bytes are allocated for user communication purposes between path elements and are payload dependent.

9.3.1.6 Position indicator: H4

This byte provides a generalized position indicator for payloads and can be payload specific (e.g. H4 can be used as a multiframe position indicator for the VC-2/VC-1).

9.3.1.7 Automatic Protection Switching (APS) channel: K3 (b1-b4)

These bits are allocated for APS signalling for protection at the VC-4/3 path levels.

9.3.1.8 Network operator byte: N1

This byte is allocated to provide a Tandem Connection Monitoring (TCM) function. The details concerning the two possible implementations of the HO-TCM function are given in Annexes C and D.

9.3.1.9 Spare: K3 (b5-b8)

These bits are allocated for future use. These bits have no defined value. The receiver is required to ignore their content.

9.3.2 VC-2/VC-1 POH

The bytes V5, J2, N2 and K4 are allocated to the VC-2/VC-1 POH. The V5 byte is the first byte of the multiframe and its position is indicated by the TU-2/TU-1 pointer. The position of these bytes in the multiframe is given in Figure 8-10.

NOTE – Payload dependent and payload independent information is communicated by different codings in bits 5 to 7 of V5 and 5 to 7 of K4.

9.3.2.1 V5 byte

The byte V5 provides the functions of error checking, signal label and path status of the VC-2/VC-1 paths. The bit assignments of the V5 byte are specified in the following paragraphs and are illustrated in Figure 9-7.

Bits 1 and 2 are used for error performance monitoring. A Bit Interleaved Parity (BIP) scheme is specified. Bit 1 is set such that parity of all odd number bits (1, 3, 5 and 7) in all bytes in the previous VC-2/VC-1 is even and bit 2 is set similarly for the even number bits (2, 4, 6 and 8).

Note that the calculation of the BIP-2 includes the VC-2/VC-1 POH bytes but excludes bytes V1, V2, V3 (except when used for negative justification) and V4.

Bit 3 is a VC-2/VC-1 path Remote Error indication (REI) indication that is set to one and sent back towards a VC-2/VC-1 path originator if one or more errors were detected by the BIP-2, and is otherwise set to zero.

Bit 4 is a VC-2/VC-1 path Remote Failure Indication (RFI). This bit is set to one if a failure is declared, otherwise it is set to zero. The VC-2/VC-1 path RFI is sent back by the VC-2/VC-1 termination.

NOTE – A failure is a defect that persists beyond the maximum time allocated to the transmission system protection mechanisms.

Bits 5 through 7 provide a VC-2/VC-1 signal label. Eight binary values are possible in these three bits. Value 000 indicates "VC-2/VC-1 path unequipped or supervisory-unequipped". Value 001 is used by old equipment to indicate "VC-2/VC-1 path equipped-non-specific payload". Other values are used by new equipment to indicate specific mappings as shown in Figure 9-7. The remaining value is reserved to be defined for a specific VC-2/VC-1 mapping. Any value received, other than 000, indicates an equipped VC-2/VC-1 path.

Bit 8 is set to 1 to indicate a VC-2/VC-1 path Remote Defect Indication (RDI), otherwise it is set to zero. The VC-2/VC-1 path RDI is sent back towards the trail termination source if either a TU-2/TU-1 server signal failure or trail signal failure condition is being detected by the trail termination sink. RDI does not indicate remote payload or adaptation defects. Connectivity and server defects are indicated by RDI; for further detail see Recommendation G.783.

BIP-2		REI	RFI	Signal Label			RDI
1	2	3	4	5	6	7	8

Virtual Container path REI coding: 0 = 0 errors

1 = 1 or more errors

Virtual Container path Signal Label coding :

b5	b6	b7	Meaning
0	0	0	Unequipped or supervisory-unequipped
0	0	1	Equipped - non-specific (Note 1)
0	1	0	Asynchronous
0	1	1	Bit synchronous (Note 2)
1	0	0	Byte synchronous
1	0	1	Reserved for future use
1	1	0	Test signal, O.181 specific mapping (Note 3)
1	1	1	VC-AIS (Note 4)

NOTES

1 Value "1" is only to be used in cases where a mapping code is not defined in the above table. For interworking with old equipment (i.e. designated to transmit only the values "0" and "1"), the following conditions apply:

– For backward compatibility, old equipment shall interpret any value received other than "0" as an equipped condition.

– For forward compatibility, when receiving value "1" from old equipment, new equipment shall not generate a Signal Label Mismatch alarm.

2 In the case of a VC-12, the code "3" shall, for backward compatibility purposes, continue to be interpreted as previously defined even if the bit synchronous mapping of 2048 kbit/s signal is not defined anymore.

3 Any mapping defined in Recommendation O.181 which does not correspond to a mapping defined in Recommendation G.707 falls in this category.

4 Only for networks supporting the transport of Tandem Connection signals.

FIGURE 9-7/G.707

VC-2/VC-1 POH V5 byte

9.3.2.2 Path Trace: J2

Byte J2 is used to transmit repetitively a Low Order Path Access Point Identifier so that a path receiving terminal can verify its continued connection to the intended transmitter. This Path Access Point Identifier uses the format defined in clause 3/G.831. A 16-byte frame is defined for the transmission of Path Access Point Identifiers. This 16-byte frame is identical to the 16-byte frame defined in 9.2.2.2 for the description of the byte J0.

NOTE – Additional text needs to be provided to cover interworking aspects.

9.3.2.3 Network operator byte: N2

This byte is allocated to provide a Tandem Connection Monitoring (TCM) function. The details concerning the implementation of the LO-TCM are given in Annex E.

9.3.2.4 Automatic Protection Switching (APS) channel: K4 (b1-b4)

These bits are allocated for APS signalling for protection at the lower order path level.

9.3.2.5 Reserved: K4 (b5-b7)

Bit 5 to 7 of K4 are reserved for an optional use described in VII.2 of Appendix VII. If this option is not used, these bits shall be set to "000" or "111". A receiver is required to be able to ignore the contents of these bits. The use of the optional function is at the discretion of the owner of the trail termination source generating the K4 byte.

9.3.2.6 Spare: K4 (b8)

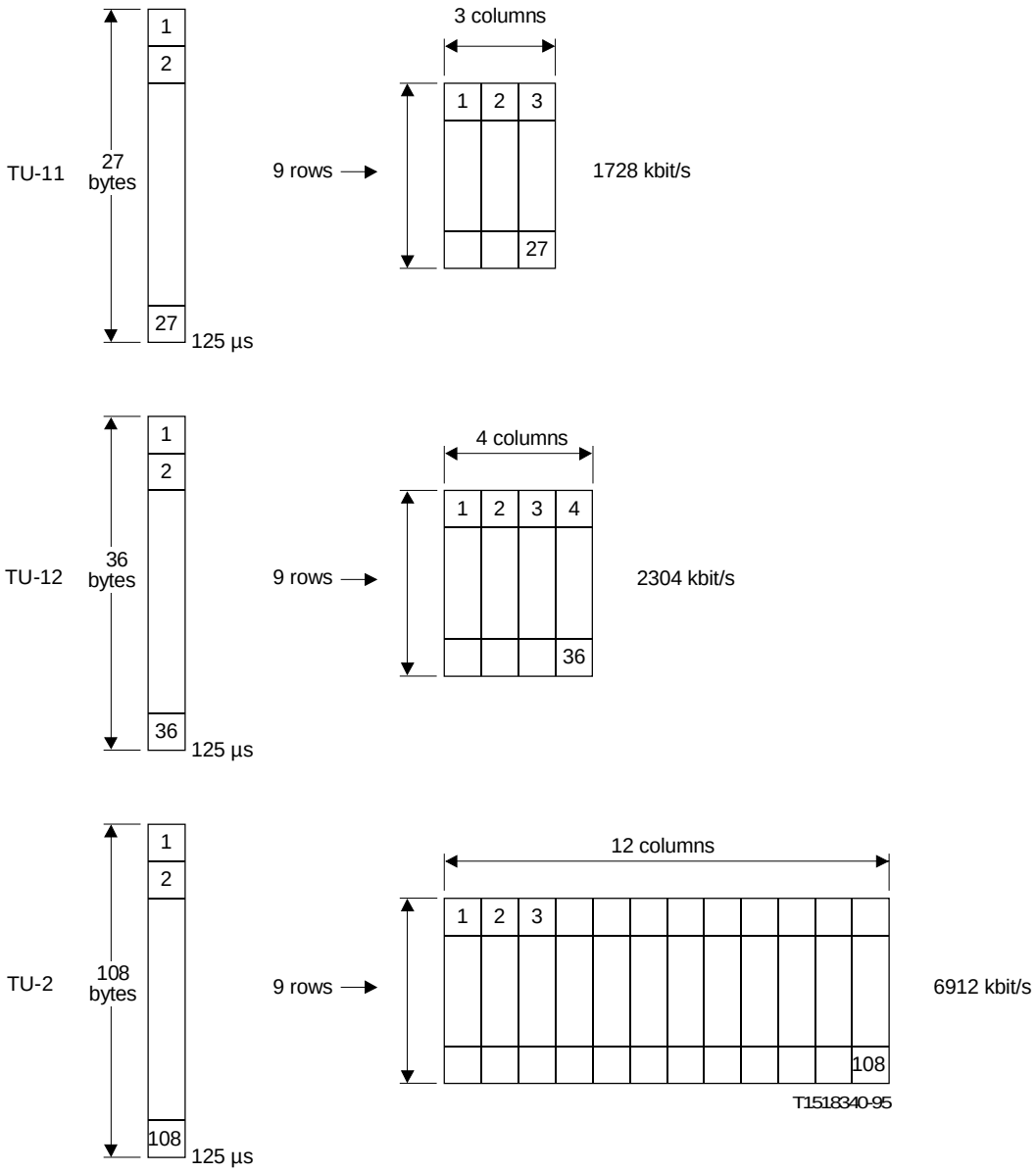
This bit is allocated for future use. This bit has no defined value. The receiver is required to ignore its content.

10 Mapping of tributaries into VC-n

10.1 Mapping of G.702 type signals

Accommodation of asynchronous and synchronous tributaries presently defined in Recommendation G.702 shall be possible.

Figure 10-1 shows TU-1 and TU-2 sizes and formats.



NOTE – The tributary unit pointer bytes (V1-V4) are located in byte 1 (using a four frame multiframe).

FIGURE 10-1/G.707

TU-1 and TU-2 sizes and formats

10.1.1 Mapping into VC-4

10.1.1.1 Asynchronous mapping of 139 264 kbit/s

One 139 264 kbit/s signal can be mapped into a VC-4 of an STM-1 frame as shown in Figures 10-2 and 10-3.

The VC-4 consists of a 9-byte (1 column) Path Overhead (POH) plus a 9-row by 260-column payload structure as shown in Figure 10-2.

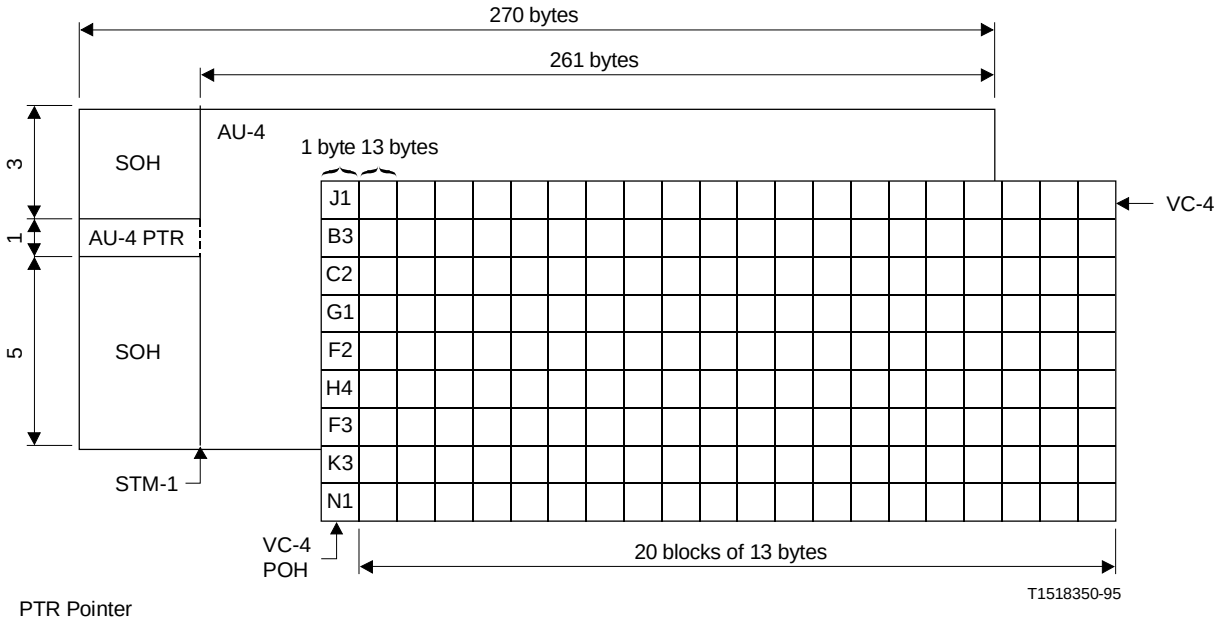


FIGURE 10-2/G.707

Multiplexing of VC-4 into STM-1 and block structure of VC-4 for asynchronous mapping of 139 264 kbit/s

This payload can be used to carry one 139 264 kbit/s signal:

– Each of the nine rows is partitioned into 20 blocks, consisting of 13 bytes each (Figure 10-2).

– In each row, one justification opportunity bit (S) and five justification control bits (C) are provided (Figure 10-3).

– The first byte of each block consists of:

  • either eight data bits (D) (byte W); or

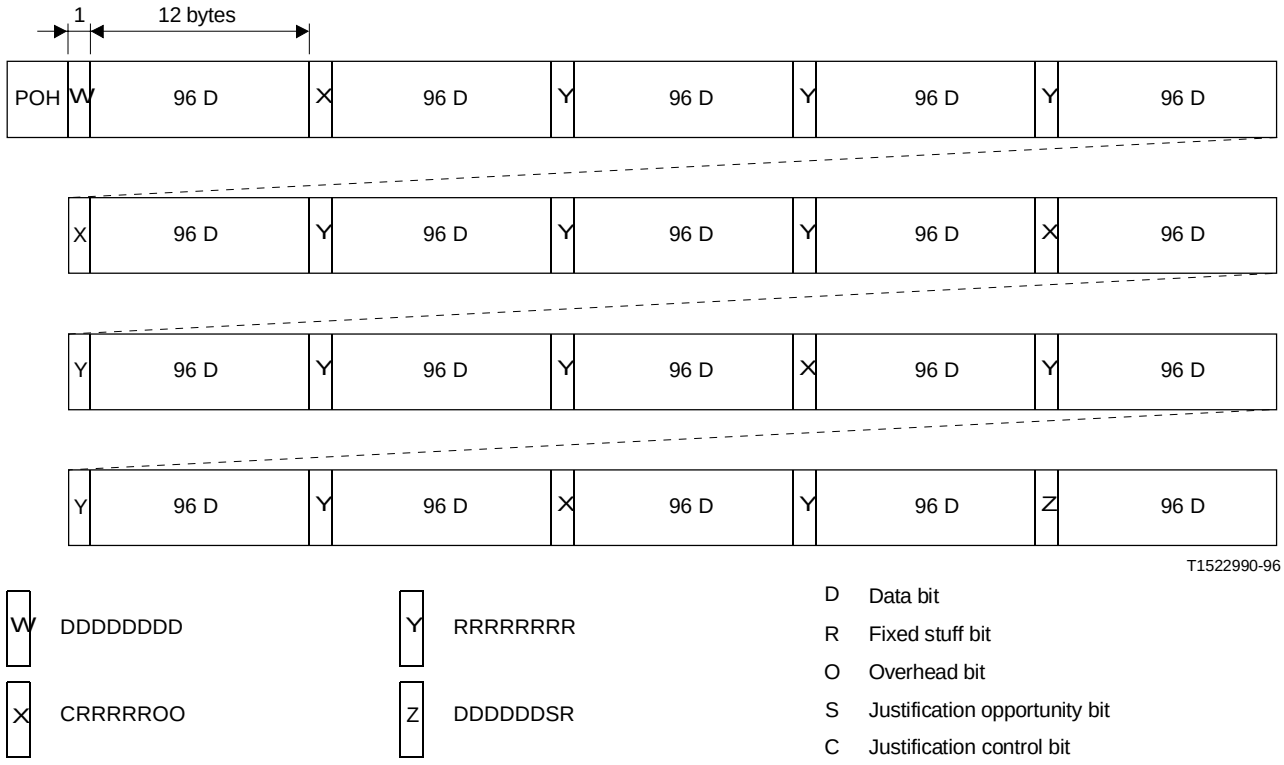
  • eight fixed stuff bits (R) (byte Y); or

  • one justification control bit (C) plus five fixed stuff bits (R) plus two overhead bits (O) (byte X); or

  • six data bits (D) plus one justification opportunity bit (S) plus one fixed stuff bit (R) (byte Z).

– The last 12 bytes of one block consist of data bits (D).

The sequence of all these bytes is shown in Figure 10-3.



NOTE – This figure shows one row of the nine-row VC-4 container structure.

FIGURE 10-3/G.707

Asynchronous mapping of 139 264 kbit/s tributary into VC-4

The overhead bits (O) are reserved for further overhead communication purposes.

The set of five justification control bits (C) in every row is used to control the corresponding justification opportunity bit (S). CCCCC = 00000 indicates that the S bit is an information bit, whereas CCCCC = 11111 indicates that the S bit is a justification bit.

Majority vote should be used to make the justification decision in the desynchronizer for protection against single and double bit errors in the C bits.

The value contained in the S bit when used as justification bit is not defined. The receiver is required to ignore the value contained in this bit whenever it is used as a justification bit.

10.1.2 Mapping into VC-3

10.1.2.1 Asynchronous mapping of 44 736 kbit/s

One 44 736 kbit/s signal can be mapped into a VC-3 as shown in Figure 10-4.

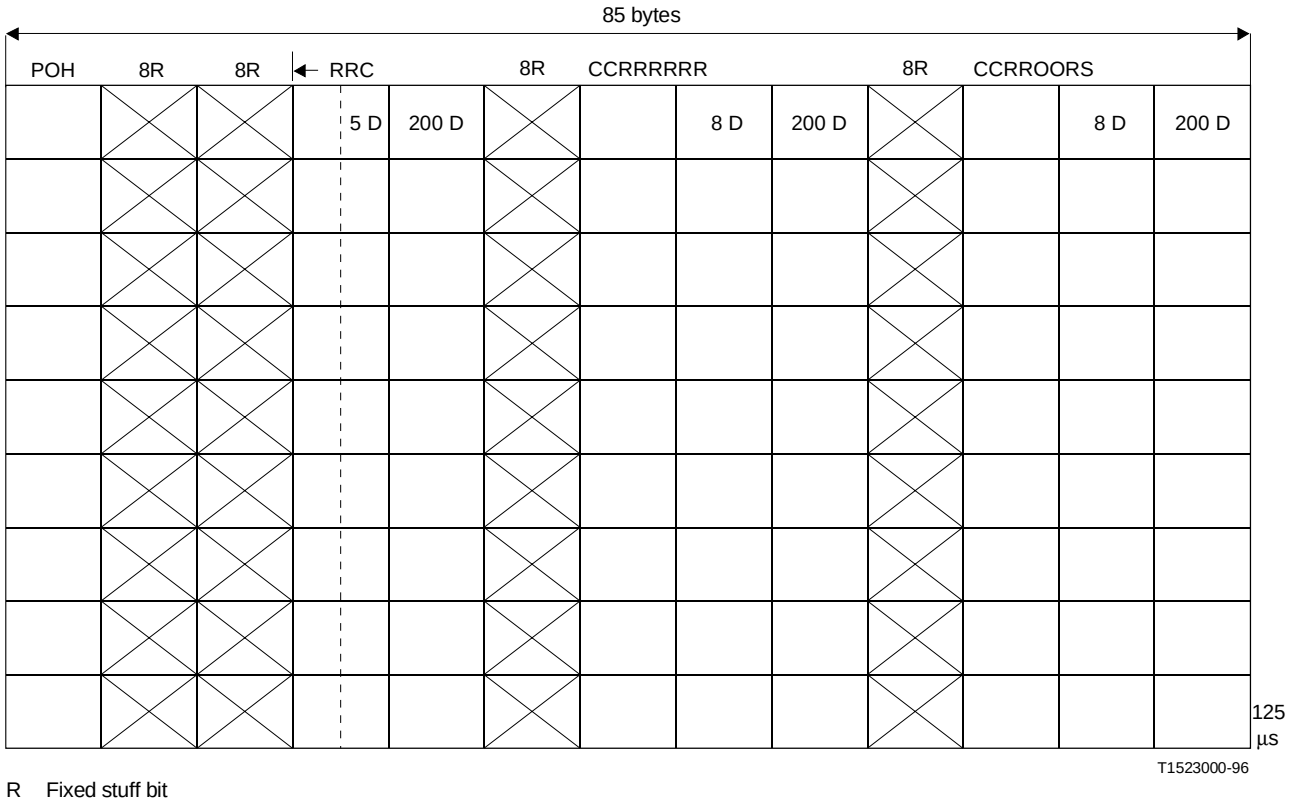


FIGURE 10-4/G.707

Asynchronous mapping of 44 736 kbit/s tributary into VC-3

The VC-3 consists of nine subframes every 125 µs. Each subframe consists of one byte of VC-3 POH, 621 data bits, a set of five justification control bits, one justification opportunity bit and two overhead communication channel bits. The remaining bits are Fixed Stuff (R) bits. The O bits are reserved for future overhead communication purposes.

The set of five justification control bits is used to control the justification opportunity (S) bit. CCCCC = 00000 indicates that the S bit is a data bit, whereas CCCCC = 11111 indicates that the S bit is a justification bit. Majority vote should be used to make the justification decision in the desynchronizer for protection against single and double bit errors in the C bits.

The value contained in the S bit when used as justification bits is not defined. The receiver is required to ignore the value contained in this bit whenever it is used as a justification bit.

10.1.2.2 Asynchronous mapping of 34 368 kbit/s

One 34 368 kbit/s signal can be mapped into a VC-3 as shown in Figure 10-5.

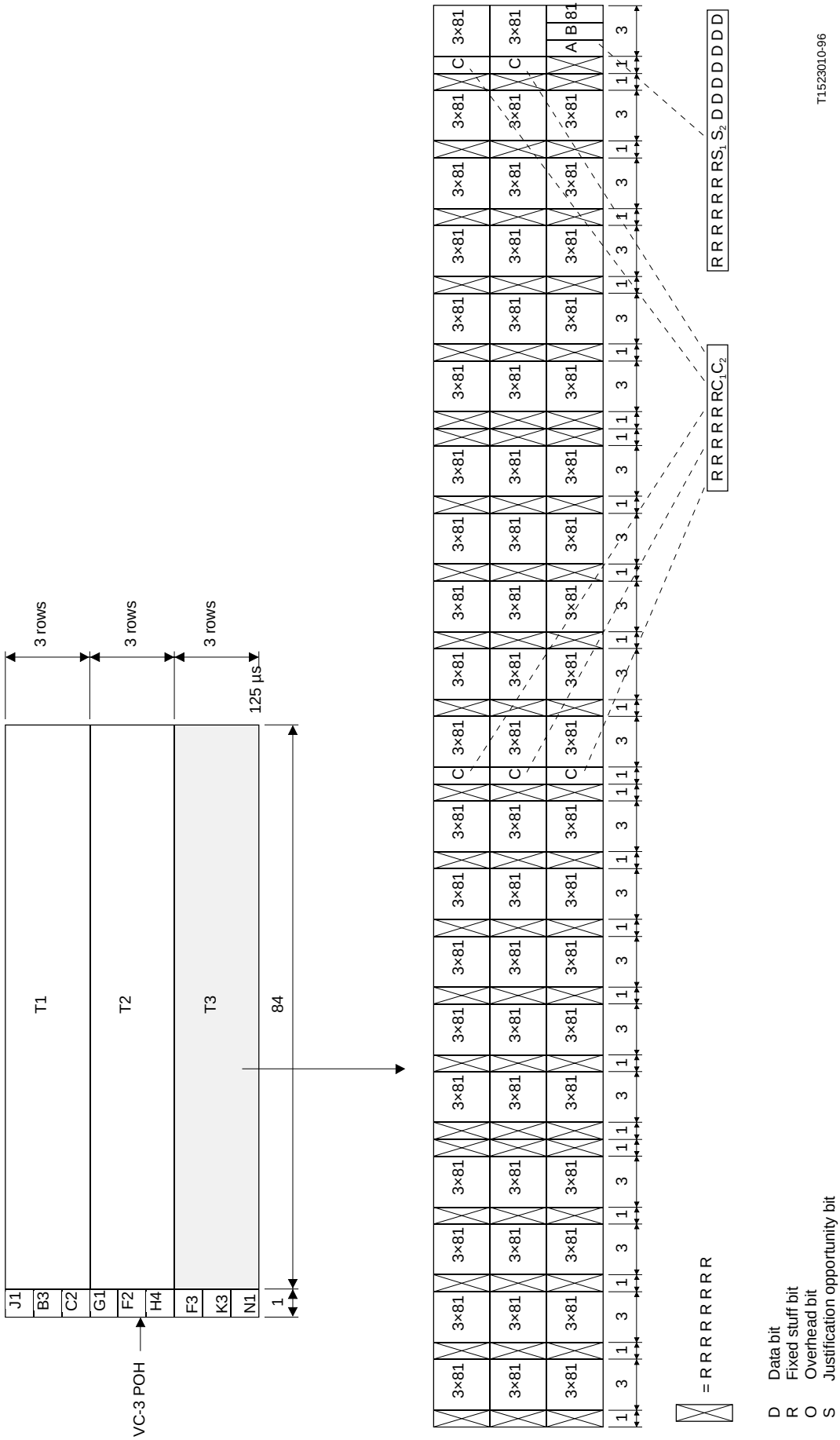


FIGURE 10-5/G.707

Asynchronous mapping of 34 368 kbit/s tributary into VC-3

In addition to the VC-3 POH, the VC-3 consists of a payload of 9×84 bytes every 125 µs. This payload is divided in three subframes, each subframe consisting of:

– 1431 data bits (D);

– two sets of five justification control bits (C_1, C_2);

– two justification opportunity bits (S_1, S_2);

– 573 fixed stuff bits (R).

Two sets of five justification control bits C_1 and C_2 are used to control the two justification opportunity bits S_1 and S_2, respectively.

$C_1C_1C_1C_1C_1$ = 00000 indicates that S_1 is a data bit while $C_1C_1C_1C_1C_1$ = 11111 indicates that S_1 is a justification bit. C_2 bits control S_2 in the same way. Majority vote should be used to make the justification decision in the desynchronizer for protection against single and double bit errors in the C bits.

The value contained in S_1 and S_2 when they are justification bits is not defined. The receiver is required to ignore the value contained in these bits whenever they are used as justification bits.

NOTE – The same mapping could be used for bit or byte synchronous 34 368 kbit/s. In these cases, S_1 bit should be a fixed stuff and S_2 bit a data bit. By setting the C_1 bits to 1 and the C_2 bits to 0, a common desynchronize could be used for both asynchronous and synchronous 34 368 kbit/s mappings.

10.1.3 Mapping into VC-2

10.1.3.1 Asynchronous mapping of 6312 kbit/s

One 6312 kbit/s signal can be mapped into a VC-2. Figure 10-6 shows this over a period of 500 µs.

V5	D D D D D D D R	(24 × 8) D	R R R R R R R R	
R R R R R R R R	C_1C_2 O O O O D R	(24 × 8) D	R R R R R R R R	
D D D D D D D D	C_1C_2 O O O O D R	(24 × 8) D	R R R R R R R R	
R R R R R R R R	C_1C_2 D D D S_1S_2 R	(24 × 8) D		125 µs
J2	D D D D D D D R	(24 × 8) D	R R R R R R R R	
R R R R R R R R	C_1C_2 O O O O D R	(24 × 8) D	R R R R R R R R	
D D D D D D D D	C_1C_2 O O O O D R	(24 × 8) D	R R R R R R R R	
R R R R R R R R	C_1C_2 D D D S_1S_2 R	(24 × 8) D		250 µs
N2	D D D D D D D R	(24 × 8) D	R R R R R R R R	
R R R R R R R R	C_1C_2 O O O O D R	(24 × 8) D	R R R R R R R R	
D D D D D D D D	C_1C_2 O O O O D R	(24 × 8) D	R R R R R R R R	
R R R R R R R R	C_1C_2 D D D S_1S_2 R	(24 × 8) D		375 µs
K4	D D D D D D D R	(24 × 8) D	R R R R R R R R	
R R R R R R R R	C_1C_2 O O O O D R	(24 × 8) D	R R R R R R R R	
D D D D D D D D	C_1C_2 O O O O D R	(24 × 8) D	R R R R R R R R	
R R R R R R R R	C_1C_2 D D D S_1S_2 R	(24 × 8) D		500 µs

D Data bit
S Justification opportunity bit
R fixed stuff bit
C Justification control bit
O Overhead bit

FIGURE 10-6/G.707

Asynchronous mapping of 6312 kbit/s tributary

In addition to the VC-2 POH, the VC-2 consists of 3152 data bits, 24 justification control bits, eight justification opportunity bits and 32 overhead communication channel bits. The remaining are Fixed Stuff bits (R). The O bits are reserved for future overhead communication purposes.

Two sets (C_1, C_2) of three justification control bits are used to control the two justification opportunities S_1 and S_2, respectively.

$C_1C_1C_1$ = 000 indicates that S_1 is a data bit while $C_1C_1C_1$ = 111 indicates that S_1 is a justification bit. C_2 bits control S_2 in the same way. Majority vote should be used to make the justification decision in the desynchronizer for protection against single bit error in the C bits.

The value contained in S_1 and S_2 when they are justification bits is not defined. The receiver is required to ignore the value contained in these bits whenever they are used as justification bits.

10.1.3.2 Bit synchronous mapping of 6312 kbit/s

The bit synchronous mapping for 6312 kbit/s tributaries is shown in Figure 10-7.

Note that a common desynchronizer can be used for both asynchronous and bit synchronous mapping.

V5	D D D D D D D R	(24 × 8) D	R R R R R R R R	
R R R R R R R R	1 Ø O O O O D R	(24 × 8) D	R R R R R R R R	
D D D D D D D D	1 Ø O O O O D R	(24 × 8) D	R R R R R R R R	
R R R R R R R R	1 Ø D D D R D R	(24 × 8) D		125 µs
J2	D D D D D D D R	(24 × 8) D	R R R R R R R R	
R R R R R R R R	1 Ø O O O O D R	(24 × 8) D	R R R R R R R R	
D D D D D D D D	1 Ø O O O O D R	(24 × 8) D	R R R R R R R R	
R R R R R R R R	1 Ø D D D R D R	(24 × 8) D		250 µs
N2	D D D D D D D R	(24 × 8) D	R R R R R R R R	
R R R R R R R R	1 Ø O O O O D R	(24 × 8) D	R R R R R R R R	
D D D D D D D D	1 Ø O O O O D R	(24 × 8) D	R R R R R R R R	
R R R R R R R R	1 Ø D D D R D R	(24 × 8) D		375 µs
K4	D D D D D D D R	(24 × 8) D	R R R R R R R R	
R R R R R R R R	1 Ø O O O O D R	(24 × 8) D	R R R R R R R R	
D D D D D D D D	1 Ø O O O O D R	(24 × 8) D	R R R R R R R R	
R R R R R R R R	1 Ø D D D R D R	(24 × 8) D		500 µs

D Data bit

R fixed stuff bit

O Overhead bit

FIGURE 10-7/G.707

Bit synchronous mapping of 6312 kbit/s tributary

10.1.3.3 Byte synchronous mapping of 6312 kbit/s

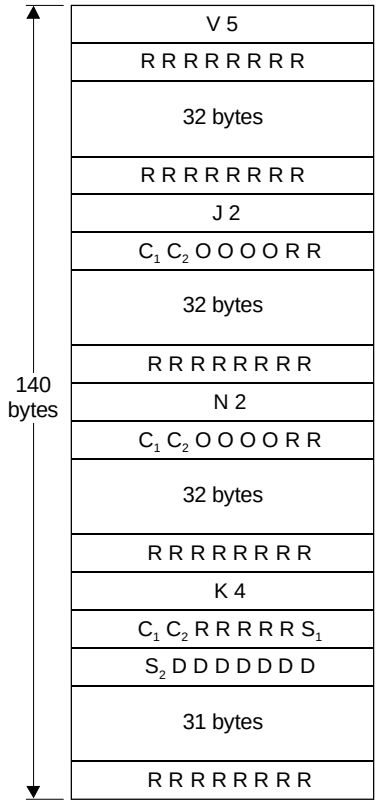
For further study.

10.1.4 Mapping into VC-12

NOTE – Refer to clause 7/G.803 for recommended selection criteria on the choice of primary rate mapping.

10.1.4.1 Asynchronous mapping of 2048 kbit/s

One 2048 kbit/s signal can be mapped into a VC-12. Figure 10-8 shows this over a period of 500 µs.



D Data bit
R Fixed stuff bit
O Overhead bit
S Justification opportunity bit
C Justification control bit

FIGURE 10-8/G.707

Asynchronous mapping of 2048 kbit/s tributary

In addition to the VC-1 POH, the VC-12 consists of 1023 data bits, six justification control bits, two justification opportunity bits and eight overhead communication channel bits. The remaining are Fixed Stuff bits (R). The O bits are reserved for future overhead communication purposes.

Two sets (C_1, C_2) of three justification control bits are used to control the two justification opportunities S_1 and S_2, respectively. $C_1C_1C_1 = 000$ indicates that S_1 is a data bit while $C_1C_1C_1 = 111$ indicates that S_1 is a justification bit. C_2 controls S_2 in the same way. Majority vote should be used to make the justification decision in the desynchronize for protection against single bit errors in the C bits.

The value contained in S_1 and S_2 when they are justification bits is not defined. The receiver is required to ignore the value contained in these bits whenever they are used as justification bits.

10.1.4.2 Byte synchronous mapping of 2048 kbit/s

Figure 10-9 shows byte synchronous mapping for G.704 structured 2048 kbit/s tributaries employing, for example, Common Channel Signalling (CCS) or Channel Associated Signalling (CAS).

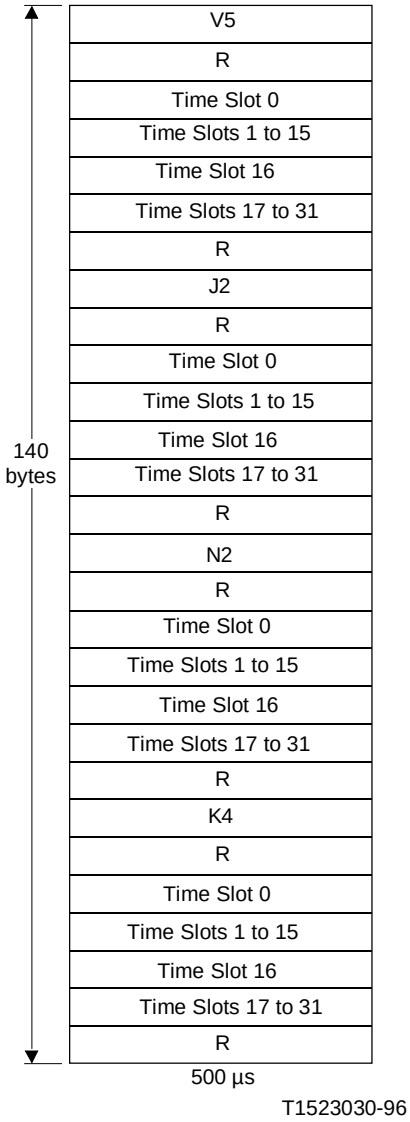
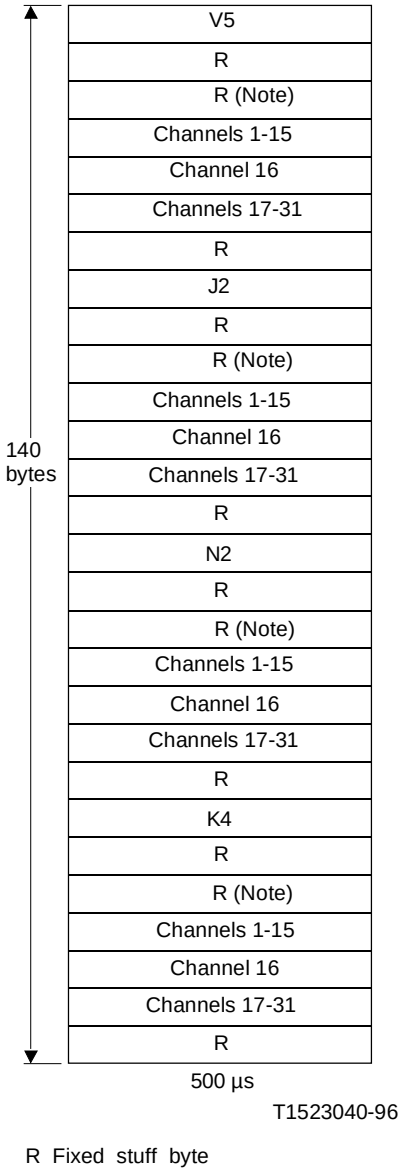


FIGURE 10-9/G.707

Byte synchronous mapping for 2048 kbit/s tributary
(30 channels with Common Channel Signalling or Channel Associated Signalling)

10.1.4.3 Byte synchronous mapping of 31 × 64 kbit/s

Byte synchronous mapping of 31 × 64 kbit/s tributaries is shown in Figure 10-10.



NOTE - Inserting here a Time Slot 0 according to Recommendation G.704 would result in the 2048 kbit/s mapping described in Figure 10-9.

FIGURE 10-10/G.707

Byte synchronous mapping for 31 × 64 kbit/s

10.1.5 Mapping into VC-11

NOTE – Refer to clause 7/G.803 for recommended selection criteria on the choice of primary rate mapping.

10.1.5.1 Asynchronous mapping of 1544 kbit/s

One 1544 kbit/s signal can be mapped into a VC-11. Figure 10-11 shows this over a period of 500 µs.

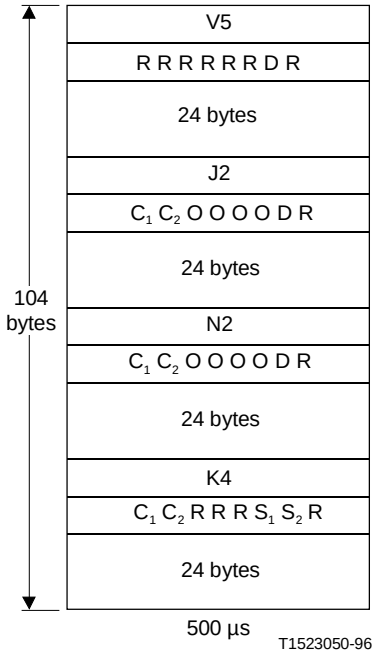


FIGURE 10-11/G.707

Asynchronous mapping of 1544 kbit/s tributary

In addition to the VC-1 POH, the VC-11 consists of 771 data bits, six justification control bits, two justification opportunity bits and eight overhead communication channel bits. The remaining are fixed stuff bits (R). The O bits are reserved for future communication purposes.

Two sets (C_1,C_2) of three justification control bits are used to control the two justification opportunities, S_1 and S_2, respectively.

$C_1C_1C_1$ = 000 indicates that S_1 is a data bit while $C_1C_1C_1$ = 111 indicates that S_1 is a justification bit. C_2 controls S_2 in the same way. Majority vote should be used to make the justification decision in the desynchronizer for protection against single bit errors in the C bits.

The value contained in S_1 and S_2 when they are justification bits is not defined. The receiver is required to ignore the value contained in these bits whenever they are used as justification bits.

10.1.5.2 Bit synchronous mapping of 1544 kbit/s

The bit synchronous mapping for 1544 kbit/s tributaries is shown in Figure 10-12.

Note that a common desynchronizer can be used for both asynchronous and bit synchronous mappings.

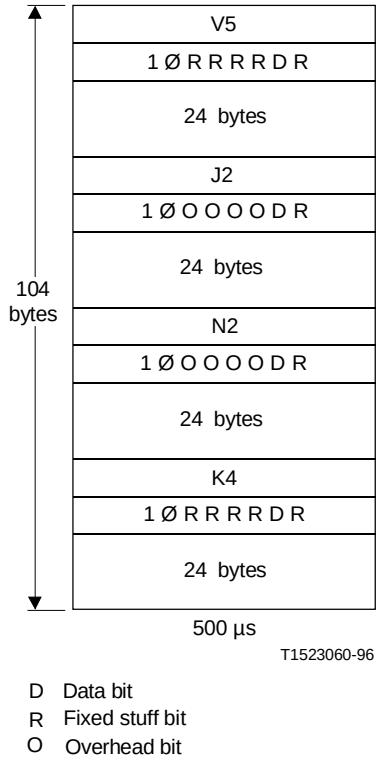
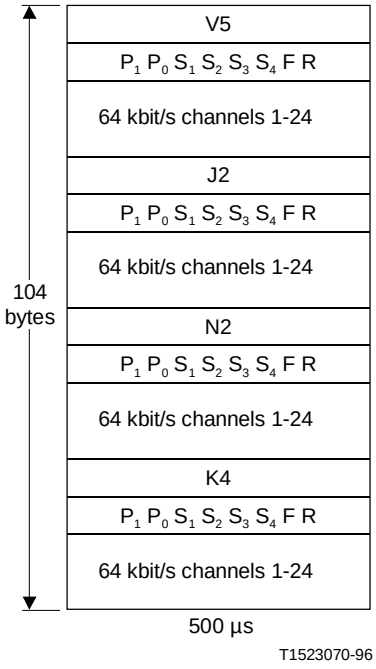


FIGURE 10-12/G.707

Bit synchronous mapping for 1544 kbit/s tributary

10.1.5.3 Byte synchronous mapping of 1544 kbit/s

The byte synchronous mapping for 1544 kbit/s tributaries is shown in Figure 10-13.



F 1544 kbit/s tributary frame bit
S Signalling bits
P_1 P_0 Signalling phase indicator
P_1 P_0 00 on the first signalling byte of the multiframe

FIGURE 10-13/G.707

Byte synchronous mapping for 1544 kbit/s tributary

The S_1, S_2, S_3 and S_4 bits contain the signalling for the 24×64 kbit/s channels. The phase of the signalling bits can be indicated in the P_1 and P_0 bits. This is illustrated in Figure 10-14. The usage of the P bits is optional, since the common channel signalling methods and some of the channel associated signalling methods (Recommendation G.704) do not need the P bits. The out slot signalling assignments for one of the channel associated signalling methods is shown in Figure 10-15.

2 state				4 state				16 state					
S_1	S_2	S_3	S_4	S_1	S_2	S_3	S_4	S_1	S_2	S_3	S_4	P_1	P_0
A_1	A_2	A_3	A_4	A_1	A_2	A_3	A_4	A_1	A_2	A_3	A_4	0	0
A_5	A_6	A_7	A_8	A_5	A_6	A_7	A_8	A_5	A_6	A_7	A_8	0	0
A_9	A_{10}	A_{11}	A_{12}	A_9	A_{10}	A_{11}	A_{12}	A_9	A_{10}	A_{11}	A_{12}	0	0
A_{13}	A_{14}	A_{15}	A_{16}	A_{13}	A_{14}	A_{15}	A_{16}	A_{13}	A_{14}	A_{15}	A_{16}	0	0
A_{17}	A_{18}	A_{19}	A_{20}	A_{17}	A_{18}	A_{19}	A_{20}	A_{17}	A_{18}	A_{19}	A_{20}	0	0
A_{21}	A_{22}	A_{23}	A_{24}	A_{21}	A_{22}	A_{23}	A_{24}	A_{21}	A_{22}	A_{23}	A_{24}	0	0
A_1	A_2	A_3	A_4	B_1	B_2	B_3	B_4	B_1	B_2	B_3	B_4	0	1
A_5	A_6	A_7	A_8	B_5	B_6	B_7	B_8	B_5	B_6	B_7	B_8	0	1
A_9	A_{10}	A_{11}	A_{12}	B_9	B_{10}	B_{11}	B_{12}	B_9	B_{10}	B_{11}	B_{12}	0	1
A_{13}	A_{14}	A_{15}	A_{16}	B_{13}	B_{14}	B_{15}	B_{16}	B_{13}	B_{14}	B_{15}	B_{16}	0	1
A_{17}	A_{18}	A_{19}	A_{20}	B_{17}	B_{18}	B_{19}	B_{20}	B_{17}	B_{18}	B_{19}	B_{20}	0	1
A_{21}	A_{22}	A_{23}	A_{24}	B_{21}	B_{22}	B_{23}	B_{24}	B_{21}	B_{22}	B_{23}	B_{24}	0	1
A_1	A_2	A_3	A_4	A_1	A_2	A_3	A_4	C_1	C_2	C_3	C_4	1	0
A_5	A_6	A_7	A_8	A_5	A_6	A_7	A_8	C_5	C_6	C_7	C_8	1	0
A_9	A_{10}	A_{11}	A_{12}	A_9	A_{10}	A_{11}	A_{12}	C_9	C_{10}	C_{11}	C_{12}	1	0
A_{13}	A_{14}	A_{15}	A_{16}	A_{13}	A_{14}	A_{15}	A_{16}	C_{13}	C_{14}	C_{15}	C_{16}	1	0
A_{17}	A_{18}	A_{19}	A_{20}	A_{17}	A_{18}	A_{19}	A_{20}	C_{17}	C_{18}	C_{19}	C_{20}	1	0
A_{21}	A_{22}	A_{23}	A_{24}	A_{21}	A_{22}	A_{23}	A_{24}	C_{21}	C_{22}	C_{23}	C_{24}	1	0
A_1	A_2	A_3	A_4	B_1	B_2	B_3	B_4	D_1	D_2	D_3	D_4	1	1
A_5	A_6	A_7	A_8	B_5	B_6	B_7	B_8	D_5	D_6	D_7	D_8	1	1
A_9	A_{10}	A_{11}	A_{12}	B_9	B_{10}	B_{11}	B_{12}	D_9	D_{10}	D_{11}	D_{12}	1	1
A_{13}	A_{14}	A_{15}	A_{16}	B_{13}	B_{14}	B_{15}	B_{16}	D_{13}	D_{14}	D_{15}	D_{16}	1	1
A_{17}	A_{18}	A_{19}	A_{20}	B_{17}	B_{18}	B_{19}	B_{20}	D_{17}	D_{18}	D_{19}	D_{20}	1	1
A_{21}	A_{22}	A_{23}	A_{24}	B_{21}	B_{22}	B_{23}	B_{24}	D_{21}	D_{22}	D_{23}	D_{24}	1	1

T1518470-95

FIGURE 10-14/G.707

Out slot signalling assignments
(24-channel signalling operations)

Frame number	n	n + 1	n + 2	n + 3	n + 4	n + 5	n + 6	n + 7
Use of S_i bits (i = 1, 2, 3, 4)	F_s	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	X
(Notes 1, 4)	(Note 2)	(Note 3)						(Note 5)

NOTES

1 Each S_i (i = 1, 2 , 3, 4) constitutes an independent signalling multiframe over eight frames. S_i includes the phase indicator in itself so that the PP bits cannot be used for the phase indicator.

2 The F_s bit is either alternate 0, 1 or the following 48-bit digital pattern:

A101011011 0000011001 1010100111 0011110110 10000101

For the 48-bit digital pattern, the A-bit is usually fixed to state 1 and is reserved for optional use. The pattern is generated according to the following primitive polynomial (refer to Recommendation X.50):

$$X^7 + X^4 + 1$$

3 Y_j bit (j = 1 to 6) carries channel associated signalling or maintenance information. When the 48-bit pattern is adopted as F_s frame alignment signal, each Y_j bit (j = 1 to 6) can be multiframed, as follows:

$$Y_{j1}, Y_{j2}, \ldots, Y_{j12}$$

Y_{j1} bit carries the following 16-bit frame alignment pattern generated according to the same primitive polynomial as for the 48-bit pattern.

A011101011011000

The A-bit is usually fixed to 1 and is reserved for optional use. Each Y_{ji} (i = 2 to 12) bit carries channel associated signalling for sub-rate circuits and/or maintenance information.

4 S_i bits (F_s, Y_1, …, Y_6 and X) all at state 1 indicates Alarm Indication Signal (AIS) for six 64 kbit/s channels.

5 The X-bit is usually fixed to state 1. When backward AIS for six 64 kbit/s channels is required, the X-bit is set to state 0.

FIGURE 10-15/G.707

Out slot signalling assignments
(24-channel signalling operations)

10.1.6 VC-11 to VC-12 conversion for transport by a TU-12

When transporting a VC-11 in a TU-12, the VC-11 is adapted by adding fixed stuff with even parity as shown in Figure 10-16. Thus the resulting TU-12 payload can be monitored and cross-connected in the network as though it were a VC-12 with its BIP value unchanged while preserving end-to-end integrity of the real VC-11 path.

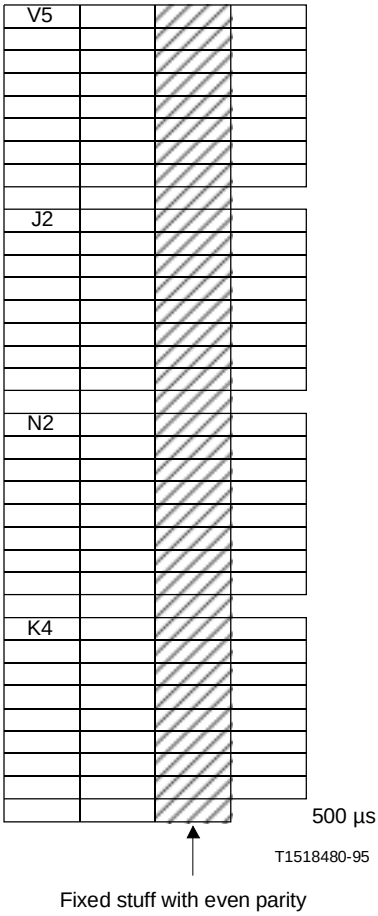


FIGURE 10-16/G.707

Conversion of VC-11 to VC-12 for transport by TU-12

10.2 Mapping of ATM cells

The mapping of ATM cells is performed by aligning the byte structure of every cell with the byte structure of the Virtual Container used including the concatenated structure (VC-x or VC-x-mc, x≥1). Since the relevant Container-x or Container-x-mc capacity may not be an integer multiple of the ATM cell length (53 bytes), a cell is allowed to cross the Container-x frame boundary.

The ATM cell information field (48 bytes) shall be scrambled before mapping into the VC-x or VC-x-mc. In the reverse operation, following termination of the VC-x or VC-x-mc signal, the ATM cell information field will be descrambled before being passed to the ATM layer. A self-synchronizing scrambler with generator polynomial $x^{43} + 1$ shall be used. The scrambler operates for the duration of the cell information field. During the 5-byte header the scrambler operation is suspended and the scrambler state retained. The first cell transmitted on start-up will be corrupted because the descrambler at the receiving end will not be synchronized to the transmitter scrambler. Cell information field scrambling is required to provide security against false cell delineation and cell information field replicating the STM-N frame alignment word.

When the VC-x or VC-x-mc is terminated, the cell must be recovered. The ATM cell header contains a Header Error Control (HEC) field which may be used in a similar way to a frame alignment word to achieve cell delineation. This HEC method uses the correlation between the header bits to be protected by the HEC (32 bits) and the control bit of the HEC (8 bits) introduced in the header after computation with a shortened cyclic code with generating polynomial $g(x) = x^8 + x^2 + x + 1$.

The remainder from this polynomial is then added to the fixed pattern "01010101" in order to improve the cell delineation performance. This method is similar to conventional frame alignment recovery where the alignment word is not fixed but varies from cell to cell.

More information on HEC cell delineation is given in Recommendation I.432.

10.2.1 Mapping into VC-4-Xc

The ATM cell stream is mapped into a Container-4-Xc with its byte boundaries aligned with the Container-4-Xc byte boundaries. The Container-4-Xc is then mapped into VC-4-Xc together with the VC-4-Xc POH and (X–1) columns of fixed stuff (see Figure 10-17). The ATM cell boundaries are thus aligned with the VC-4-Xc byte boundaries. Since the Container-4-Xc capacity (X × 2340 bytes) is not an integer multiple of the cell length (53 bytes), a cell may cross a Container-4-Xc frame boundary.

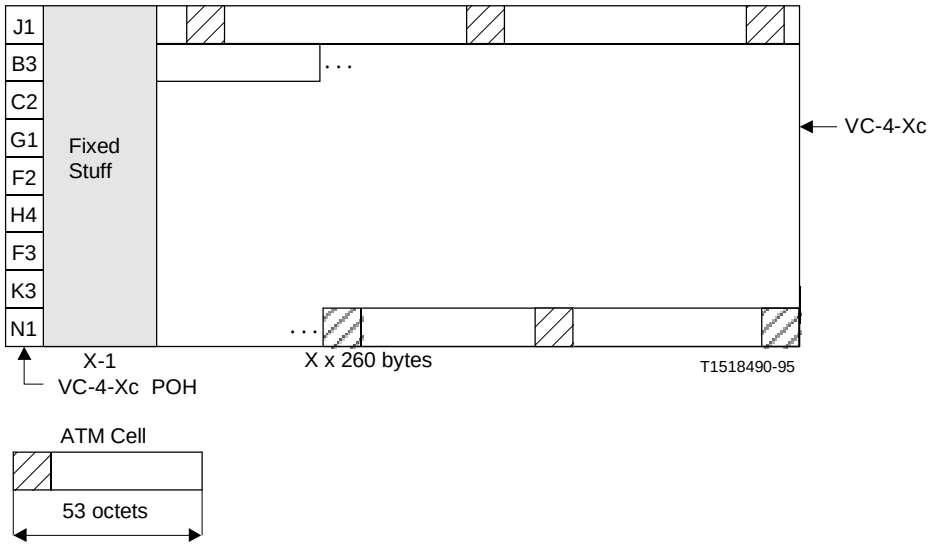


FIGURE 10-17/G.707

Mapping of ATM cells into VC-4-Xc

10.2.2 Mapping into VC-4/VC-3

The ATM cell stream is mapped into Container-4/Container-3 with its byte boundaries aligned with the Container-4/Container-3 byte boundaries. The Container-4/Container-3 is then mapped into VC-4/VC-3 together with the VC-4/VC-3 POH (see Figure 10-18). The ATM cell boundaries are thus aligned with the VC-4/VC-3 byte boundaries. Since the C-4/C-3 capacity (2340/756 bytes respectively) is not an integer multiple of the cell length (53 bytes), a cell may cross a Container-4/Container-3 frame boundary.

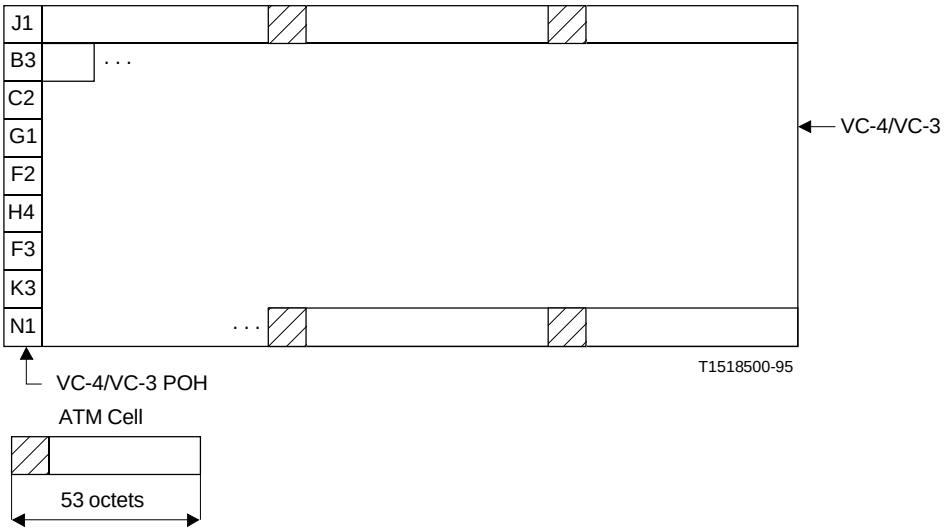


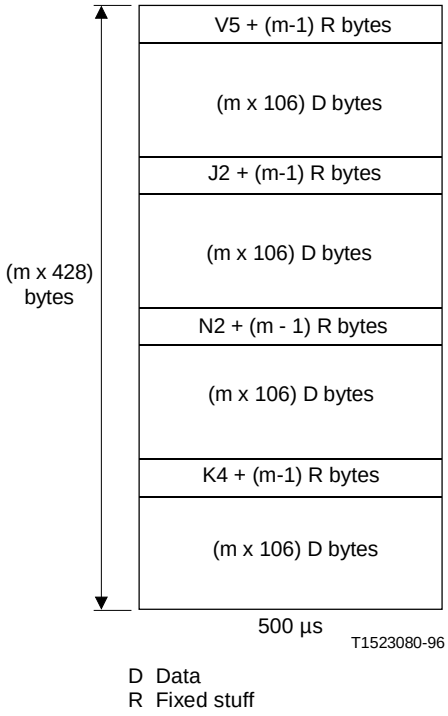
FIGURE 10-18/G.707

Mapping of ATM cells into VC-4/VC-3

10.2.3 Mapping into VC-2-mc

Figure 10-19 shows the mapping for an ATM cell stream with a data rate of $m \times 6.784$ Mbit/s where "m" can take any integer value between 2 and 7 inclusive for contiguous concatenation, and between 2 and 21 inclusive for virtual concatenation.

The VC-2-mc structure is organized as a four-frame multiframe. The frames of the multiframe consist of one byte of VC-2-mc POH, (m–1) stuff bytes and ($m \times 106$) bytes of payload area except in the case of virtual concatenation, when the frames consist of m independent bytes of VC-2-mc POH and ($m \times 106$) bytes of payload area. ATM cells are loaded into the VC-2-mc payload area with the boundaries of the cells aligned with any VC-2-mc byte boundary. Because the VC-2-mc payload space is equivalent of exactly ($m \times 2$) ATM cells per 125 µs frame, the alignment between ATM cell boundaries and the VC-2-mc structure will remain constant from frame to frame. Cells can cross VC-2-mc frame boundaries.



NOTE - In the case of virtual concatenation, the frames contain m independent VC-2-mc POH bytes.

FIGURE 10-19/G.707

Mapping of ATM cells into VC-2-mc using contiguous concatenation

10.2.4 Mapping into VC-2

Figure 10-20 shows the mapping for an ATM cell stream with a data rate of 6.784 Mbit/s.

The VC-2 structure is organized as a four-frame multiframe. The frames of the multiframe consist of one byte of VC-2 POH and 106 bytes of payload area. ATM cells are loaded into the VC-2 payload area with the boundaries of the cells aligned with any VC-2 byte boundary. Because the VC-2 payload space is equivalent of exactly two ATM cells per 125 µs frame, the alignment between ATM cell boundaries and the VC-2 structure will remain constant from frame to frame. Cells can cross VC-2 frame boundaries.

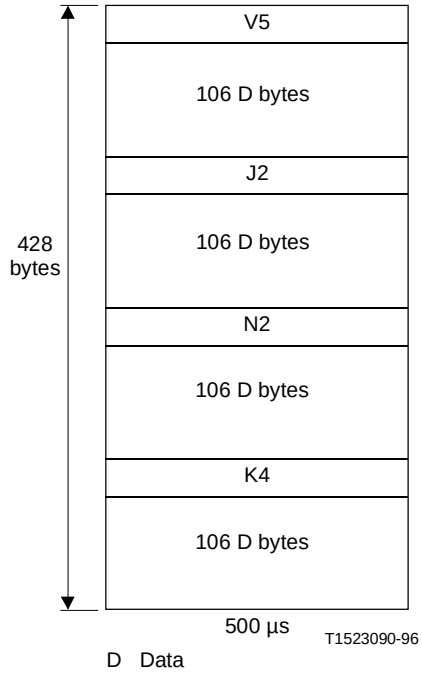


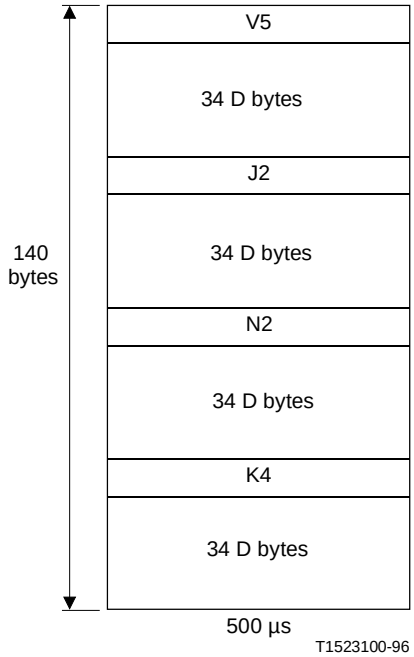
FIGURE 10-20/G.707

Mapping of ATM cells into VC-2

10.2.5 Mapping into VC-12/VC-11

Figures 10-21 and 10-22 show the mapping for ATM cell streams with data rates of 2.176 Mbit/s and 1.600 Mbit/s into VC-12 and VC-11, respectively.

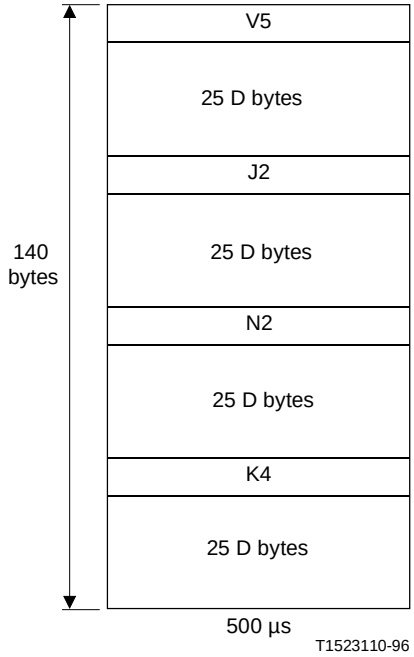
In floating TU-n mode, the VC-12/VC-11 structure is organized as four frame multiframe. The frames of the multiframe consist of one byte of VC-12/VC-11 POH and 34 or 25 bytes, respectively, of payload area. ATM cells are loaded into the VC-12/VC-11 payload area with the boundaries of the cells aligned with any VC-12/VC-11 byte boundary. Because the VC-12/VC-11 payload space is not related to the size of an ATM cell (53 bytes), the alignment between ATM cell boundaries and the VC-12/VC-11 structure will change from frame to frame in a sequence repeating every 53 frames. Cells can cross VC-12/VC-11 frame boundaries.



D Data

FIGURE 10-21/G.707

Mapping of ATM cells into VC-12



D Data

FIGURE 10-22/G.707

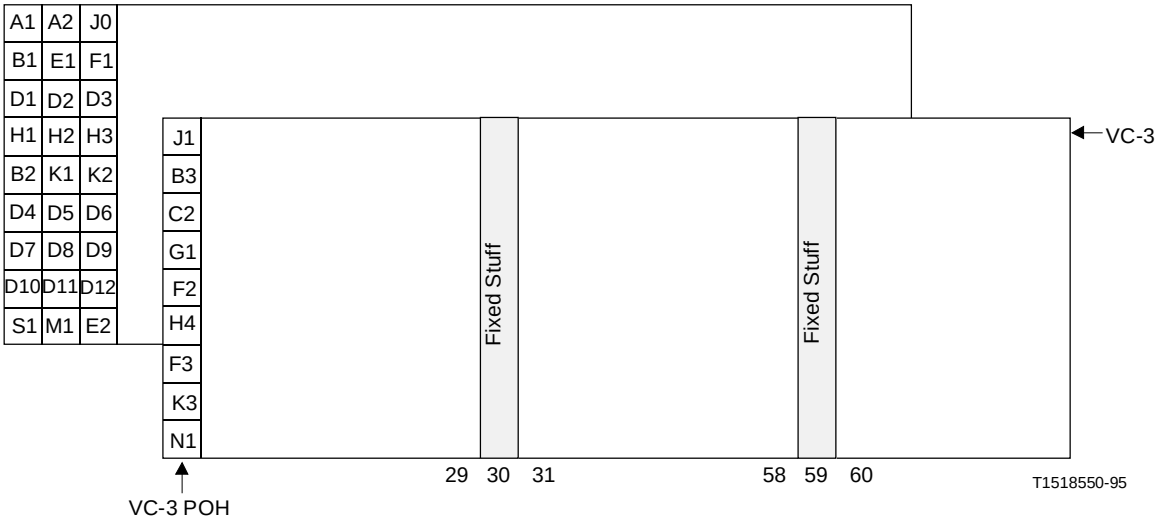
Mapping of ATM cells into VC-11

Annex A

Recommended frame structure for digital section operating at 51 840 kbit/s

(This Annex forms an integral part of this Recommendation)

Figure A.1 illustrates the frame structure to be used for systems operating at 51 840 kbit/s.



NOTES

1 M1 position is not the same position [9, 3N+3] as in a STM-N frame.
2 Fixed stuff columns are not part of the VC-3.

FIGURE A.1/G.707

Frame structure for 51 840 kbit/s signal

Annex B

CRC-7 polynomial algorithm

(This Annex forms an integral part of this Recommendation)

B.1 Multiplication/division process

A particular CRC-7 word is the remainder after multiplication by X^7 and then division (modulo 2) by the generator polynomial $X^7 + X^3 + 1$, of the polynomial representation of the previous Trail Trace Identifier multiframe (TTI).

When representing the contents of the block as a polynomial, the first bit in the block, i.e. byte 1 bit 1 should be taken as being the most significant bit. Similarly, C_1 is defined to be the most significant bit of the remainder and C_7 the last significant bit of the remainder.

B.2 Encoding procedure

Contrary to example CRC-4 procedure in 2 Mbit/s signals, the CRC-7 word is static because the data is static (the TTI represents the source address). This means that the CRC-7 checksum can be calculated *a priori* over the TTI multiframe. For consistency with existing Recommendations, the CRC-7 checksum is to be calculated over the previous multiframe. In theory this means that the 16-byte string that is loaded in a device for repetition transmission should have the checksum as the last byte although in practice it does not really matter because the TTI is static.

The encoding procedure is as follows:

i) The CRC-7 bits in the TTI are replace by binary 0s.

ii) The TTI is then acted upon by the multiplication/division process referred to in B.1.

iii) The remainder resulting from the multiplication/division process is inserted into the CRC-7 location.

The CRC-7 bits generated do not affect the result of the multiplication/division process because, as indicated in i) above, the CRC-7 bit positions are initially set to 0 during the multiplication/division process.

B.3 Decoding procedure

The decoding procedure is as follows:

i) A received TTI is acted upon by the multiplication/division process referred to in B.1 after having its CRC-7 bits extracted and replaced by 0s.

ii) The remainder resulting from the division process is then compared on a bit-by-bit basis with the CRC-7 bits received.

iii) If the remainder calculated in the decoder exactly corresponds to the CRC-7 bits received, it is assumed that the checked TTI is error free.

Annex C

VC-4-Xc/VC-4/VC-3 Tandem Connection Monitoring protocol: option 1

(This Annex forms an integral part of this Recommendation)

This subclause describes the Tandem Connection Overhead layer for SDH. The Tandem Connection sub-layer is an optional sub-layer which falls between the multiplex section and path layers defined in this Recommendation. This overhead sub-layer deals with the reliable transport of path layer payload and its overhead across a network. The use of Tandem Connection is application specific and at the discretion of the carrier. It is expected that the principal applications for Tandem Connection will be in the inter-office network and that Tandem Connections will generally not be used in applications such as the subscriber access network.

C.1 Tandem Connection Overhead – Byte location

The N1 byte in the path overhead in each HOVC of the Tandem Connection is defined as Tandem Connection Overhead (TCOH). Bits 1-4 of this byte in each HOVC of the Tandem Connection are used to provide a Tandem Connection Incoming Error Count (IEC), which is defined below. The remaining four bits in byte N1 of the first VC-n within the Tandem Connection are used to provide an end to end data link.

NOTE – Applications currently under consideration may require some LAPD messages generated before the originating TCTE to be transferred through the Tandem Connection data link. This is for further study.

Figure C.1 shows the Tandem Connection overheads for an STM-1 rate Tandem Connection made up of a bundle of 3 VC-3 HO paths.

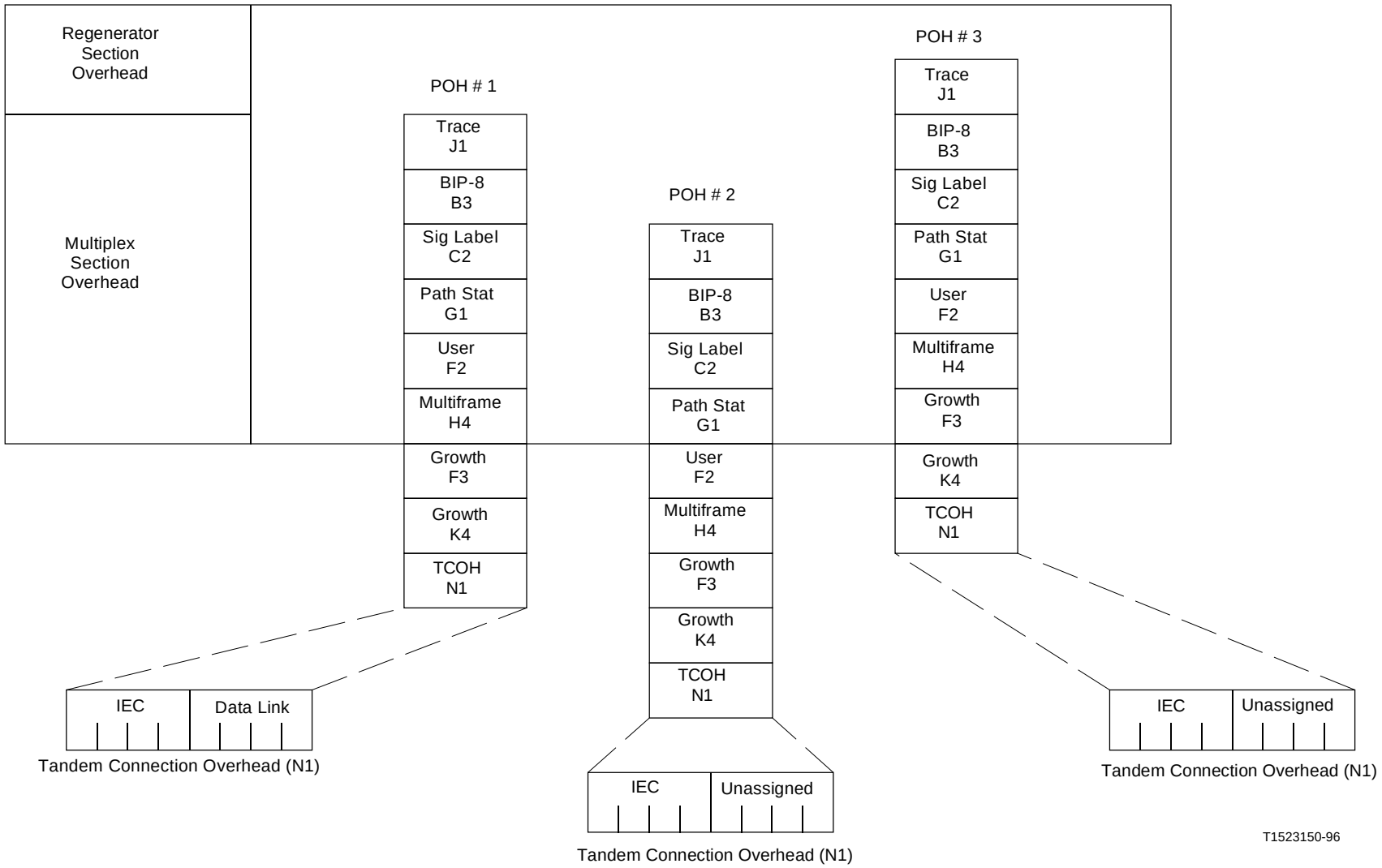


FIGURE C.1/G.707

Tandem Connection Overhead in STM-1 rate (AU-3 based) Tandem Connection

C.2 Definitions

C.2.1 tandem connection (TC): A Tandem Connection is defined as a group of Higher Order VC-ns which are transported and maintained together through one or more tandem line systems, with the constituent HOVC payload capacities unaltered. Note that in support of the layered overhead approach used in SDH, the Tandem Connection sub-layer falls between the multiplex section and path overhead layers (i.e. the original Regenerator section, Multiplex section, and Path functional overhead layering evolves to Regenerator section, Multiplex section, Tandem Connection, and Path layers).

C.2.2 tandem connection terminating element (TCTE): The element which originates/terminates the Tandem Connection. A Multiplex Section Terminating Element (MSTE) or a Path Terminating Element (PTE) may also be a TCTE.

C.3 Tandem Connection Bundling

Tandem Connection maintenance may be performed on a single Higher Order VC-n or on a bundle with a capacity of N STM-1s where N is any of the allowed SDH hierarchy levels defined in 6.3. The size of bundles supported is application specific and an equipment issue. The following subclause describes how Tandem Connection bundling is achieved.

C.3.1 Bundling of VC-3s within an STM-1

The bytes from bundled VC-3s within an STM-1 shall be contiguous at the STM-1 level, but are not contiguous when interleaved to higher levels. The first VC-n of the bundle shall contain the Tandem Connection data link.

Figure C.2 illustrates this for a Tandem Connection at the STM-1 rate.

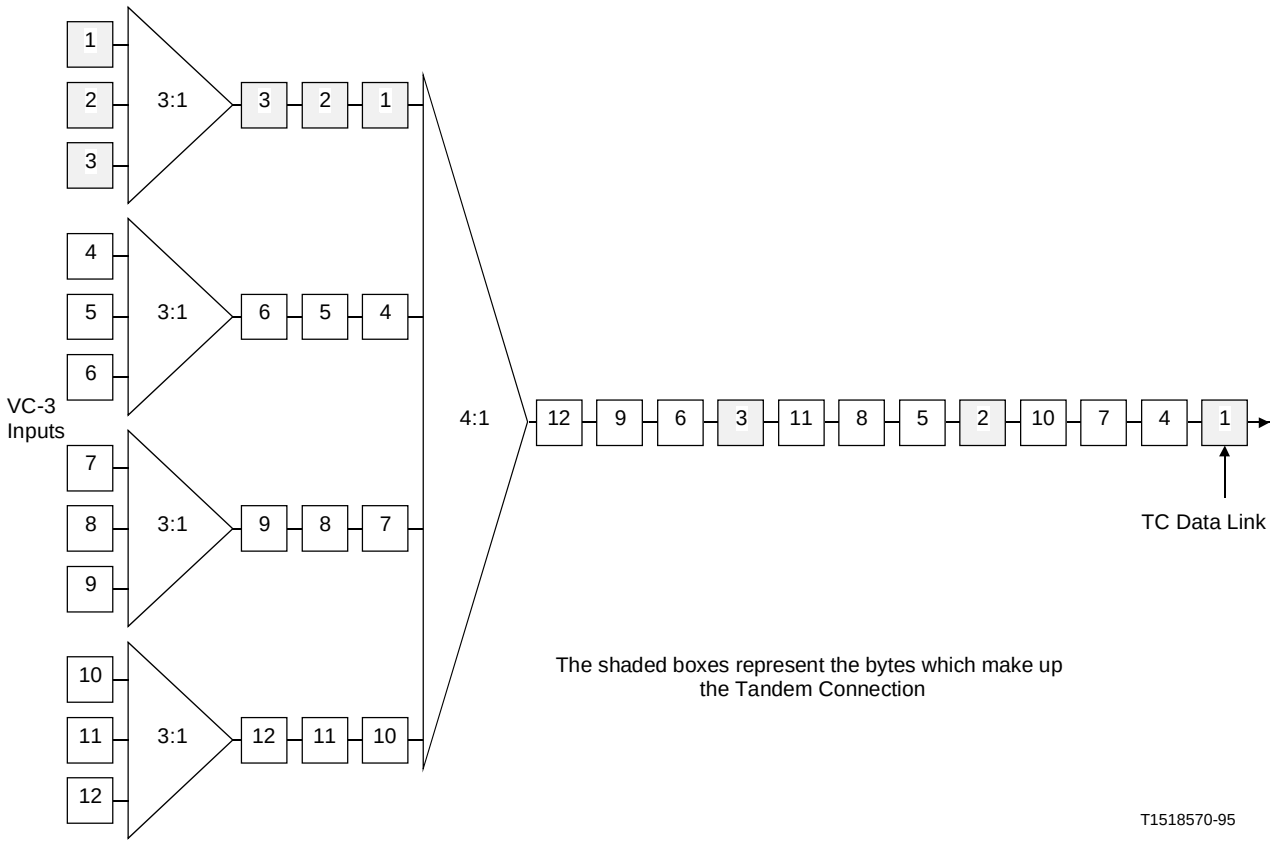


FIGURE C.2/G.707

Example of an STM-1 rate Tandem Connection within an STM-N

C.3.2 Bundling of VC-3s within an STM-N (N>1)

Bundles of VC-3s within an STM-N (N is any of the allowed SDH hierarchy levels defined in 6.3) consist of multiples of STM-1s. The bytes from the constituent STM-1s shall be contiguous. The first HOVC of the Tandem Connection shall contain the Tandem Connection data link.

C.3.3 Tandem Connection Bundle Contents

A Tandem Connection bundle at the STM-N rate (N is any of the allowed SDH hierarchy levels defined in 6.3) may carry 3×N VC-3s or combinations of VC-4-Mcs (M≤N; M=1, 4, 16) including one VC-4-Xc as per the concatenation mechanism defined in 8.1.7 (e.g. an STM-4 Tandem Connection could carry 12 VC-3s, or 4 VC-4s, or one VC-4-4c, or 2 VC-4-4cs and 6 VC-3s, etc.). Note that a VC-4-Mc shall be contained wholly within a single Tandem Connection.

Figure C.3 illustrates this for an STM-4 rate Tandem Connection made up of four VC-4s.

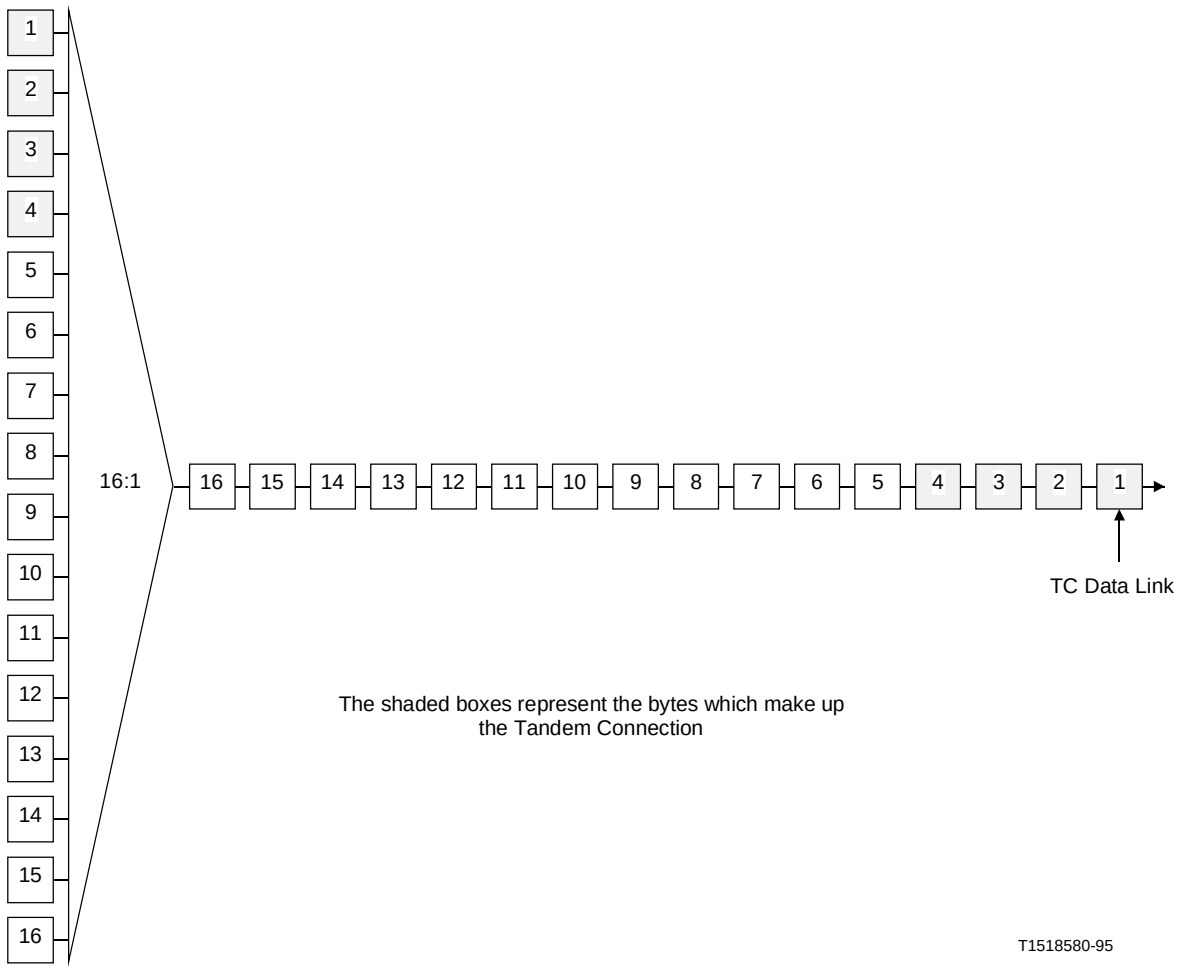


FIGURE C.3/G.707

Example of an STM-4 rate Tandem Connection within an STM-16

C.3.4 Tandem Connection bundles in higher rate signals

A bundle of HOVCs forming a Tandem Connection may be multiplexed into a higher rate STM-N as per the multiplexing procedure defined in this Recommendation.

C.4 Incoming Error Count (IEC)

In order to continually assess the Tandem Connection signal quality, the B3 bytes in the VC-n overhead of each of the HOVCs that make up the Tandem Connection signal are used to determine the number of errors which have accumulated in the Tandem Connection. In order to account for any errors that may be present in a VC-n at the originating end of the Tandem Connection, the number of errors detected in the incoming VC-n at the originating end of the Tandem Connection is written into bits 1-4 of byte N1 in the next frame. This procedure is carried out for each of the VC-ns that make up the Tandem Connection.

The Tandem Connection signal may then be carried through the network by STM-M SDH line system (of equal or higher transport rate), or number of SDH line systems in tandem where the Tandem Connection is made at the Tandem Connection, or higher, level (e.g. a VC-3 Tandem Connection may be cross-connected at the VC-3 rate or higher, and a TCB at the STM-4 rate may be cross-connected at the STM-4 rate or higher). At the terminating TCTE (far end of the Tandem Connection), the B3 byte in each of the constituent HOVCs is again used to calculate the number of errors which have accumulated. The magnitude (absolute value) of the difference between this calculated number of errors and the number of errors written into the IEC at the originating end is then used to determine the error performance of the Tandem Connection for each transmitted SDH frame. Note that the B3 byte data and the IEC read in the current frame both apply to the previous frame.

On the outgoing side of the terminating TCTE, the IEC (first four bits of N1 byte) of all constituent HOVCs shall be set to all 0s. As a default, the Tandem Connection data link (last four bits of N1 in the first HOVC) shall be set to all 0s.

NOTE – Applications currently under consideration may require some messages in the Tandem Connection data link to be forwarded on beyond the terminating TCTE. This is for further study.

The unassigned bits (last four bits in the remaining Z5 bytes) shall be passed through unaltered. B3 shall then be compensated as defined in the following subclause.

C.5 B3 Compensation

Since the B3 parity check is taken over the VC-n payload and Path Overhead (including N1), writing into N1 at the originating TCTE will affect the path parity calculation. Unless this is compensated for, a device which monitors path parity within the Tandem Connection (e.g. a bridging monitor) may incorrectly count errors. The B3 parity byte should always be consistent with the current state of the VC-n. Therefore, whenever N1 is written, B3 shall be modified to compensate for the change in the N1 value. Since the B3 value in a given frame reflects a parity check over the previous frame (including the B3 byte in that frame), the changes made to the B3 byte in the previous frame shall also be considered in the compensation of B3 for the current frame. Therefore, the following equation shall be used for B3 compensation:

$$B3'(t) = B3(t-1) \oplus B3'(t-1) \oplus N1(t-1) \oplus N1'(t-1) \oplus B3(t)$$

Where:

B3	=	the existing B3 value in the incoming signal.
B3’	=	the new (compensated) B3 value.
N1	=	the existing N1 value in the incoming signal.
N1’	=	the new value written into the N1 Byte (IEC plus data link at the originating TCTE, or all 0s at the terminating TCTE).
$\oplus$	=	exclusive OR operator.
t	=	the time of the current frame.
t–1	=	the time of the previous frame.

C.6 Data link

Bits 5-8 of the N1 byte in the first VC-n of the Tandem Connection are designated as a 32 kbit/s Tandem Connection data link. The remaining four bits in byte N1 of the remaining VC-ns are unassigned and must not be altered by the TCTE. The signal format used on the Tandem Connection

data link is comprised of messages that use a subset of the LAPD protocol (unnumbered, unacknowledged frame).

NOTE – If future applications require LAPD messages generated and terminated outside the Tandem Connection to be transferred through the Tandem Connection data link, the above statement does not require that these messages also be un-numbered and unacknowledged.

When these LAPD messages are not being transmitted (i.e. the data link is idle), LAPD flags (01111110) shall be continuously transmitted.

Currently, four messages are defined below to support Tandem Connection maintenance.

- Tandem Connection Trace.
- Tandem Connection Idle signal ID.
- Tandem Connection Test signal ID.
- Tandem Connection Far End One Second Performance Report Message.

In practice, the Tandem Connection Trace, Idle signal ID, or Test signal ID message is transmitted continuously at a minimum rate of once per second. The Tandem Connection Far End One Second Performance Report Message is transmitted continuously at a rate of once per second.

Operation, administration, and maintenance of the network may cause messages, other than those defined above, to appear on the Tandem Connection data link. Network terminal and monitoring equipment should be able to disregard any such undefined messages. Such undefined message use must not interfere with the transmission of the messages defined in this Recommendation. Use of the Tandem Connection data link for other terminal-to-terminal messages beyond the described set is for future study.

C.6.1 Format of the LAPD messages

The format of the LAPD messages uses a subset of the full Q.921/LAPD capabilities. The message structure is shown Figure C.4. This message structure is that of a Q.921/LAPD, un-numbered and unacknowledged frame. The source of the LAPD messages shall generate the FCS and the zero stuffing required for transparency. Zero stuffing by a transmitter prevents the occurrence of the flag pattern (01111110) in the bits between the opening and closing flags of a Q.921/LAPD frame by inserting a zero after any sequence of five consecutive ones. A receiver removes a zero following five consecutive ones.

There is no requirement for the boundaries of the LAPD octets and the N1 byte to coincide. The bits of the LAPD octet shall be transmitted in the order shown in Figure C.4, within the N1 byte. Thus, bits n, n+1, n+2, and n+3 of an arbitrary LAPD octet would be loaded into bits 5, 6, 7, and 8, respectively, of the N1 byte.

C.6.2 Tandem Connection Trace, Idle Signal, and Test Signal Identification Messages

The Tandem Connection identification messages discussed below shall be transmitted a minimum of once per second and shall use only the SAPI/TEI values shown in Figure C.4. The contents of the 76-octet information field is shown in Figure C.5 and is discussed in the following subclause.

NOTE – Note that the Tandem Connection Trace message length of 76 bytes may be changed to 64 bytes to be consistent with the SDH path trace (J1 Byte), once the content of the J1 Byte message (under study) has been standardized.

The Tandem Connection Trace (TCT), Idle Signalidentification (ISID), and Test Signalidentification (TSID) messages all use the same 76-octet structure made up of 6 data elements. Each data element, except the first, is a fixed length word made up of ASCII characters. The first data element is one byte long and defines the type of identification message being transmitted. The next four data elements identify the type of terminal equipment and the equipment location that sourced the identification message. Finally, given that terminal equipment may source more than one Tandem Connection signal, the final data element identifies a specific Tandem Connection signal.

The first five data elements have the same meaning for all three messages, and will be defined first. The sixth data element is different for each of the messages (see Figure C.5). The data elements are designed to accommodate codes that are widely used in facility networks.

The first five data elements, common to all three identification messages, are defined as follows.

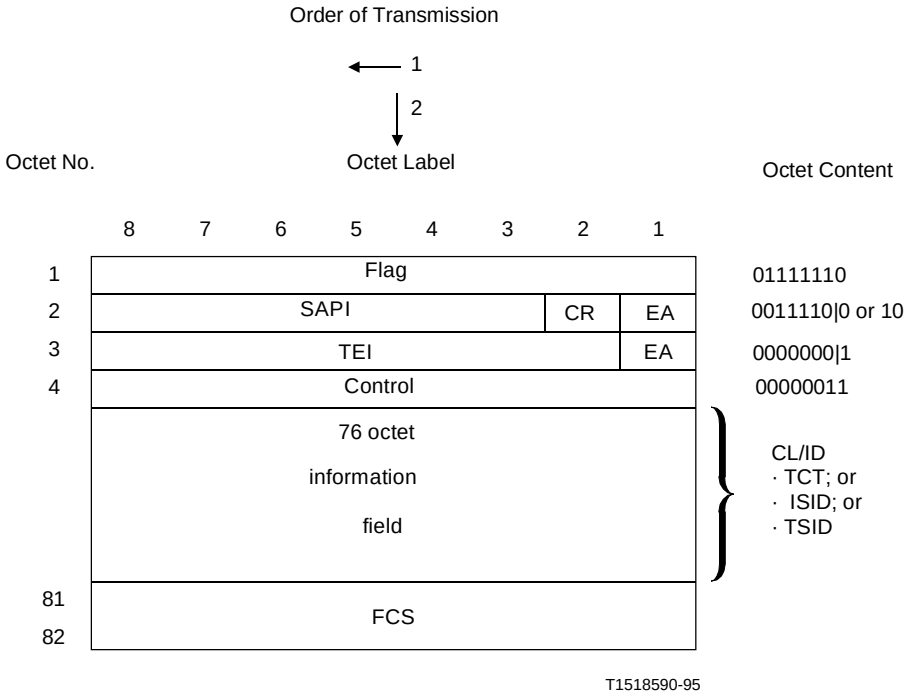
TYPE The Type code is a one octet code used to identify a particular type of identification message. Specific values are shown in Figure C.5.

EIC The Equipment Identification Code (up to 10 characters) describes a specific piece of equipment.

LIC The Location Identification Code (up to 11 characters) describes a specific location.

FIC The Frame Identification Code (up to 10 characters) identifies where the equipment is located within a building at a given location.

UNIT A code (up to 6 characters) that identifies the equipment location within a bay.



Flag	Interpretation
01111110	Interframe Fill Octet Sequence

SAPI|CR|EA	Interpretation
00111100	SAPI=15, CR=0 (DTE), EA=0
00111110	SAPI=15, CR=1 (Carrier), EA=0

TEI|EA	Interpretation
00000001	TEI=0, EA=1

Control	Interpretation
00000011	Unacknowledged Information Transfer

N octet information field	Interpretation
Path ID	Common Language Identifier
Idle SIG. ID	
Test SIG. ID	

FCS	Interpretation
Variable	CRC-16 Frame Check Sequence

FIGURE C.4/G.707

Q.921/LAPD message structure

Tandem Connection Trace

Data elements	Binary value	
TYPE	0011 1000	Connection ID
EIC	XXXX XXXX..XXXX	10 Octets
LIC	XXXX XXXX..XXXX	11 Octets
FIC	XXXX XXXX..XXXX	10 Octets
UNIT	XXXX XXXX..XXXX	6 Octets
FI	XXXX XXXX..XXXX	38 Octets

Idle Signal Identification

Data elements	Binary value	
TYPE	0011 0100	Idle ID
EIC	XXXX XXXX..XXXX	10 Octets
LIC	XXXX XXXX..XXXX	11 Octets
FIC	XXXX XXXX..XXXX	10 Octets
UNIT	XXXX XXXX..XXXX	6 Octets
PORT No.	XXXX XXXX..XXXX	38 Octets

Test Signal Identification

Data elements	Binary value	
TYPE	0011 0010	Test ID
EIC	XXXX XXXX..XXXX	10 Octets
LIC	XXXX XXXX..XXXX	11 Octets
FIC	XXXX XXXX..XXXX	10 Octets
UNIT	XXXX XXXX..XXXX	6 Octets
GEN No.	XXXX XXXX..XXXX	38 Octets

T1518600-95

FIGURE C.5/G.707

Tandem Connection trace-idle signal and test signal identification messages

The final data element for the Tandem Connection Trace message is the Facility Identification code:

FI The Facility Identification code (up to 38 characters) identifies a specific Tandem Connection.

The final data element for the Idle Signal identification message is the port number:

PORT No. The PORT number is the designation of the equipment port that initiates the Idle signal.

The final data element for the Test Signal identification message is the generator number:

GEN No. The number of the Test Signal generator that initiates the test signal.

The ASCII null character shall be used to indicate the end of the string when the full length of the data element is not needed for a given word. The remaining bit positions of the data element may contain ones, zeros, or any combination of ones and zeros.

In those cases where all the data elements are not needed for a given message, the first octet of the data element shall contain the ASCII null character. The remaining bit-positions of the data element may contain ones, zeros, or any combination of ones and zeros.

C.6.3 The far-end performance report message

The Tandem Connection far end one second performance report message discussed below shall be transmitted once per second and shall use only the SAPI/TEI values shown in Figure C.6. The phase of the 1-second report periods with respect to the occurrence of error events is arbitrary in that the 1-second timing does not depend on the time of occurrence of any error event.

The performance report contains performance information for each of the four previous 1-second intervals. This is illustrated in Figure C.6, octets 5 through 20, and by an example in Figure C.7. Counts of events shall be accumulated in each contiguous 1-second interval. At the end of each 1-second interval, a modulo-4 counter shall be incremented, and the appropriate performance bits shall be set in the t_0 octets (octets 5 through 8 in Figure C.6). These octets and the octets that carry the performance bits of the preceding three 1-second intervals form the performance report message.

C.6.3.1 Elements of the far-end performance report message

Occurrences of performance anomalies, defects, failures, and status conditions indicate the overall quality of transmission on a Tandem Connection. The Tandem Connection anomalies, defects, failures and status conditions that shall be detected and reported are:

– Tandem Connection error event;
– Tandem Connection AIS/LOP defect;
– Tandem Connection AIS failure;
– Tandem Connection LOP failure;
– Tandem Connection Idle signal received condition;
– Tandem Connection Test signal received condition;
– Tandem Connection Count Type Indicator (CTI).

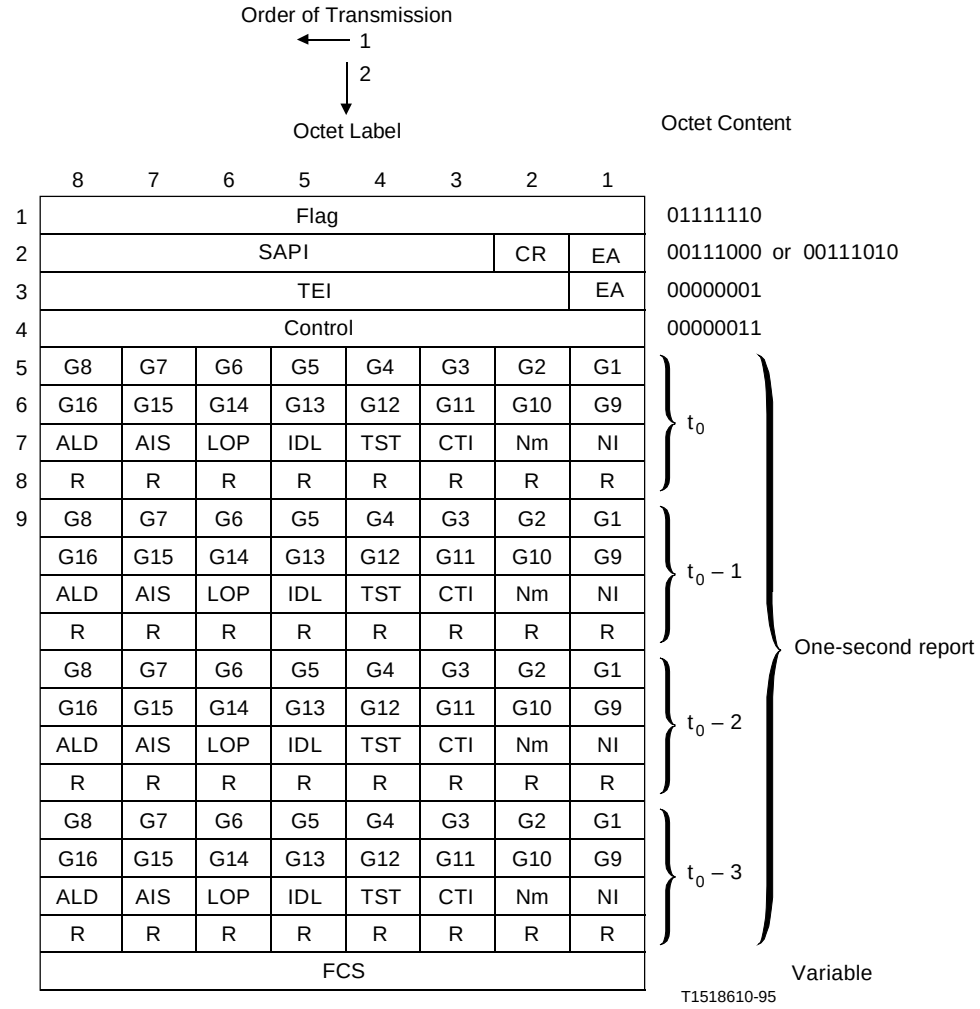
These Tandem Connection events and conditions are defined in the following subclauses.

C.6.3.2 Tandem Connection error event

A Tandem Connection error event is detected by comparing the calculated number of errors received at the end of the Tandem Connection, using the B3 byte, with the incoming error count contained in the Tandem Connection Overhead (i.e. bits 1-4 of the N1 byte), for each of the signals that make up the Tandem Connection.

C.6.3.3 Tandem Connection AIS/LOP defect

AU-n AIS defect and AU-n LOP defect are defined in Recommendation G.783. The occurrence of either one of these defects, in at least one of the signals that make up the Tandem Connection, constitutes a Tandem Connection AIS/LOP defect.



Address	Interpretation
00111000	SAPI=14, C/R=0 (User) EA=0
00111010	SAPI=14, C/R=1 (Carrier) EA=0
00000001	TEI=0, EA=1

Control	Interpretation
00000011	Unacknowledged Information Transfer

One-second report	Interpretation
G G8	LSB of 2-Byte Tandem Connection Error Event Counter
G9 G16	MSB of 2-Byte Tandem Connection Error Event Counter
ALD = 1	Tandem Connection AIS/LOP Defect
AIS = 1	Tandem Connection AIS Failure Condition
LOP = 1	Tandem Connection LOP Failure Condition
IDL = 1	Tandem Connection Idle Signal Received
TST = 1	Tandem Connection Test Signal Received
CTI = 0	Error Event Counts are Bit Error Counts
R = 0	Reserved (Default value is 0)
NmNI = 00, 01, 10, 11	One-second report modulo 4 counter

FCS	Interpretation
Variable	CRC-16 Frame Check Sequence

FIGURE C.6/G.707

SDH Tandem Connection Far-End performance report message status

	$t = t_0$	$t = t_0 + 1$	$t = t_0 + 2$	$t = t_0 + 3$
Flag	01111110	01111110	01111110	01111110
Address Octet 1	00111000	00111000	00111000	00111000
Address Octet 2	00000001	00000001	00000001	00000001
Control	00000011	00000011	00000011	00000011
Message Octet 1	**11111111**	00000000	00000000	00000000
Message Octet 2	**00000000**	00000000	00000000	00000000
Message Octet 3	**00000000**	10000001	10000010	00100011
Message Octet 4	**00000000**	00000000	00000000	00000000
Message Octet 5	11110000	**11111111**	00000000	00000000
Message Octet 6	00000000	**00000000**	00000000	00000000
Message Octet 7	00000011	**00000000**	10000001	10000010
Message Octet 8	00000000	**00000000**	00000000	00000000
Message Octet 9	00001111	11110000	**11111111**	00000000
Message Octet 10	00000000	00000000	**00000000**	00000000
Message Octet 11	00000010	00000011	**00000000**	10000001
Message Octet 12	00000000	00000000	**00000000**	00000000
Message Octet 13	00000000	00001111	11110000	**11111111**
Message Octet 14	00000000	00000000	00000000	**00000000**
Message Octet 15	00000001	00000010	00000011	**00000000**
Message Octet 16	00000000	00000000	00000000	**00000000**
FCS Octet 1	xxxxxxxx	xxxxxxxx	xxxxxxxx	xxxxxxxx
FCS Octet 2	xxxxxxxx	xxxxxxxx	xxxxxxxx	xxxxxxxx

NOTES

$t = t_0 - 3$:	Tandem Connection error count = 0;	all other parameters = 0; N(t) = 1
$t = t_0 - 2$:	Tandem Connection error count = 15;	all other parameters = 0; N(t) = 2
$t = t_0 - 1$:	Tandem Connection error count = 240;	all other parameters = 0; N(t) = 3
$t = t_0$:	Tandem Connection error count = 255;	all other parameters = 0; N(t) = 0
$t = t_0 + 1$:	AUS/LOP defect detected;	all other parameters = 0; N(t) = 1
$t = t_0 + 2$:	AUS/LOP defect detected;	all other parameters = 0; N(t) = 2
$t = t_0 + 3$:	LOP failure detected;	all other parameters = 0; N(t) = 3

FIGURE C.7/G.707

Example of an SDH Tandem Connection Far-End performance report message status

C.6.3.4 Tandem Connection AIS failure

A Tandem Connection AIS failure is declared if the AU-n AIS defect is present, in at least one of the signals that make up the Tandem Connection, for a period T, where T is 2.5 ± 0.5 seconds.

C.6.3.5 Tandem Connection LOP failure

A Tandem Connection LOP failure is declared if the AU-n LOP defect is present, in at least one of the signals that make up the Tandem Connection, for a period T, where T is 2.5 ± 0.5 seconds.

C.6.3.6 Tandem Connection Idle signal received condition

A Tandem Connection Idle signal received condition occurs when a valid Tandem Connection Idle signal is detected at the end of a Tandem Connection.

C.6.3.7 Tandem Connection Test signal received condition

A Tandem Connection Test signal received condition occurs when a valid Tandem Connection test signal is detected at the end of a Tandem Connection.

C.6.3.8 Tandem Connection Count Type Indicator

The Tandem Connection Count Type Indicator is set to 0 to indicate that the Tandem Connection IEC contains a count of the number of bit errors (not block errors) which were detected in the previous one second interval.

C.6.4 Special carrier applications

A carrier may require the use of the Tandem Connection data link for purposes related to the provisioning or maintenance of the Tandem Connection or SDH network. Such uses may cause interruptions, delays, or reduction of throughput on the Tandem Connection data link, but shall not impact the timely transmission of the LAPD messages defined above.

The LAPD messages defined above should be constructed and inserted on the data link by the source terminal (TCTE) that constructs the Tandem Connection signal whether it is a carrier (CR=1) or a DTE (CR=0) terminal. The messages should be delivered without alteration to the TCTE that sinks the information payload of the Tandem Connection signal.

C.7 Treatment of Incoming Signal Failures

AU-n (n=3, 4) AIS is specified as all 1s in the entire AU-n, including the AU-n pointer. Since the AU-n pointer is invalid during AIS, the HOVC POH cannot be accessed. Without the following changes, the Tandem Connection overhead would be lost during signal failures.

When there is a failure on an incoming signal at the origination point of a Tandem Connection (originating TCTE), the pointers should be re-established within the Tandem Connection (in order to locate the Tandem Connection overhead). A new Incoming Signal Failure (ISF) indicator shall be set within the Tandem Connection to indicate that there was a signal failure before the Tandem Connection, and AU-n AIS shall be inserted in the appropriate signal(s) at the end of the Tandem Connection.

The following subclauses discuss the treatment of signal failures which occur before and within the Tandem Connection, respectively.

C.7.1 Signal failures before the Tandem Connection

Figure C.8 illustrates Tandem Connections with incoming signal failures. For transmission from left to right, when there is a signal failure on an incoming AU-n at the originating TCTE, that TCTE will insert a valid pointer value in H1, H2, and H3. With this pointer value, the originating TCTE will locate B3 and the TCOH. An incoming error count of 15 (1111) will be written into the IEC (bits 1-4 of the TCOH), and, for the first HOVC only, the data link will be written into bits 5-8 of the TCOH.

All 1s will be written into the remainder of the HOVC, except for B3. B3 shall be calculated in order to provide even parity over the previous frame.

Within the Tandem Connection, no special treatment is necessary. AU-ns which entered with a signal failure will have valid pointers within the Tandem Connection (inserted by the originating TCTE). Regenerator section and/or multiplex section terminating equipment within the Tandem Connection will see valid pointers and will treat the signals as if they were carrying traffic.

At the end of the Tandem Connection, the terminating TCTE will interpret an IEC value of 15 as an Incoming Signal Failure (ISF) indication. When an ISF indication is received, the terminating TCTE will insert AU-n AIS on the appropriate outgoing signals. For Tandem Connection error calculations, ISF values of 9 through 15 will be interpreted as zero incoming errors (IEC=0)

NOTE – IEC values of 9 through 14 are reserved for future standardization.

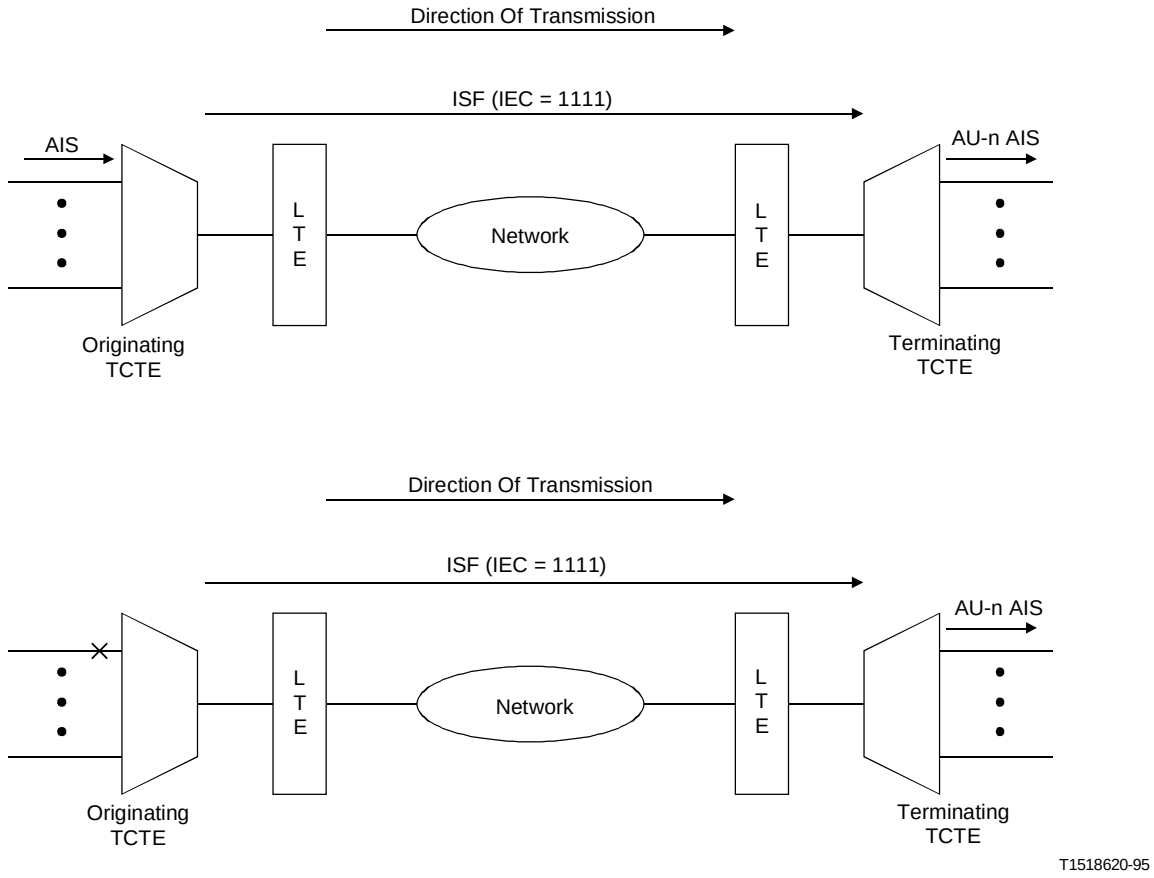


FIGURE C.8/G.707

Tandem Connection with Incoming Signal Failures

C.7.2 Signal failures within the Tandem Connection

Figure C.9 illustrates signal failures within a Tandem Connection. No special treatment is required for these failures. Regenerator section and/or multiplex section terminating equipment within the Tandem Connection will respond to signal failures. If AU-n AIS is received at the terminating TCTE, it will indicate a signal failure within the Tandem Connection.

NOTE – As discussed above, signal failures before the originating TCTE will be converted to ISF by the originating TCTE. Therefore, AU-n AIS at the terminating TCTE indicates a failure inside the Tandem Connection.

When the terminating TCTE receives a signal failure, it will insert AIS in the appropriate outgoing AU-ns, and will return the appropriate message to the originating TCTE via the Tandem Connection Far-End Performance Report Message.

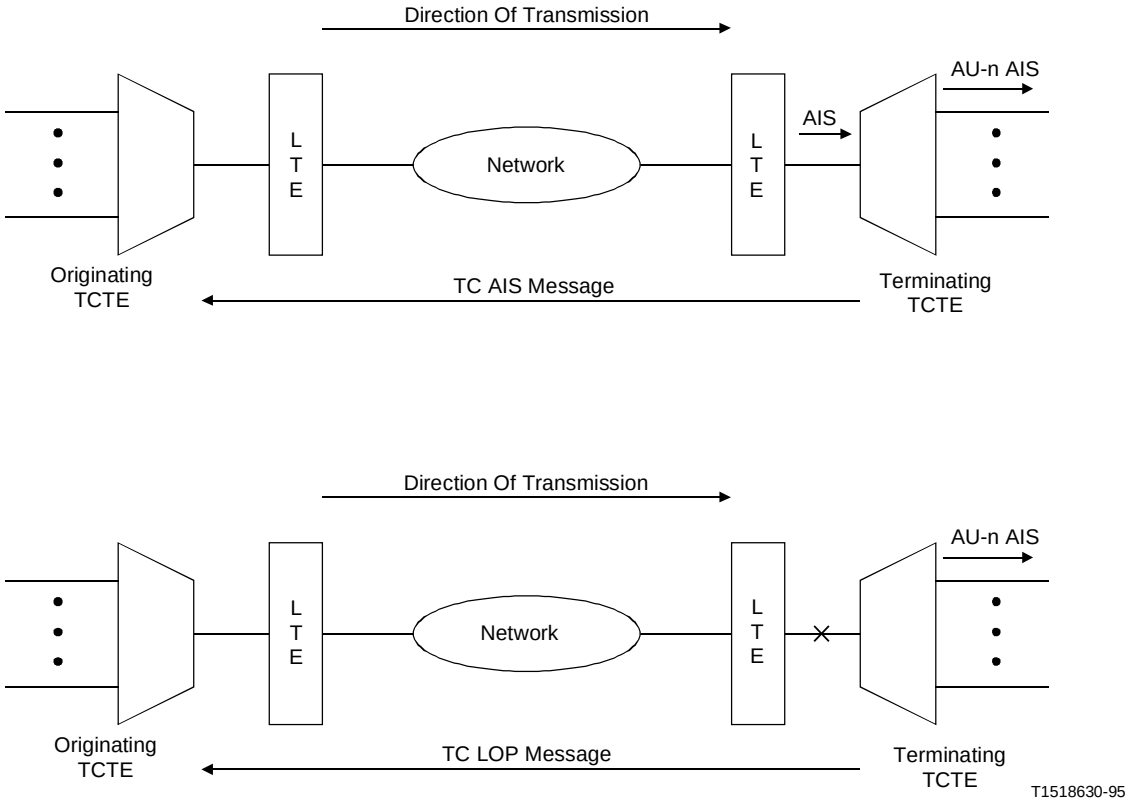


FIGURE C.9/G.707

Signal failures within the Tandem Connection

C.8 Tandem Connection Idle Signal

Tandem Connection Idle Signal is defined as a Tandem Connection with all constituent signal labels set to "Unequipped" (C2=00), and a valid Idle Signal ID message on the Tandem Connection data link (per C.6).

C.9 Tandem Connection test signal

Tandem Connection test signal is defined as any valid Tandem Connection signal with a valid Tandem Connection Test Signal ID.

Annex D

VC-4/VC-3 Tandem Connection Monitoring protocol: option 2

(This Annex forms an integral part of this Recommendation)

D.1 N1 byte structure

N1 is allocated for Tandem Connection Monitoring for the VC-4 and VC-3 levels. The structure of the N1 byte is given in Table D.1.

- Bits 1-4 are used as an Incoming Error Count (IEC); the coding is given in Table D.2.
- Bit 5 operates as the TC-REI of the Tandem Connection to indicate errored blocks caused within the Tandem Connection.
- Bit 6 operates as the OEI to indicate errored blocks of the egressing VC-n.
- Bits 7-8 operate in a 76 multiframe as:
  - the access point identifier of the Tandem Connection (TC-APId); it complies with the generic 16-byte string format given in 9.2.2.2.
  - the TC-RDI, indicating to the far end that defects have been detected within the Tandem Connection at the near end Tandem Connection sink.
  - the ODI, indicating to the far end that AU/TU-AIS has been inserted into the egressing AU-n/TU-n at the TC-sink due to defects before or within the Tandem Connection.
  - reserved capacity (for future standardization).

The structure of the multiframe is given in Tables D.3 and D.4.

TABLE D.1/G.707

N1 byte structure

b1	b2	b3	b4	b5	b6	b7	b8
IEC				TC-REI	OEI	TC-APId, TC-RDI ODI, reserved	

TABLE D.2/G.707

IEC coding

Number of BIP-8 violations	b1	b2	b3	b4
0	1	0	0	1
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
Incoming AIS	1	1	1	0
NOTE – To guarantee a non all-zeroes N1 byte independent of the incoming signal status, it is required that the IEC code field contains at least one "1". When zero errors in the BIP-8 of the incoming signal are detected then an IEC code is inserted with "1"s in it. In this manner, it is possible for the Tandem Connection sink at the tail end of the Tandem Connection link to use the IEC code field to distinguish between unequipped conditions started within or before the Tandem Connection.				

TABLE D.3/G.707

b7-b8 multiframe structure

Frame #	Bits 7 and 8 definition
1-8	Frame Alignment Signal: 1111 1111 1111 1110
9-12	TC-APId byte #1 [1 $C_1C_2C_3C_4C_5C_6C_7$]
13-16	TC-APId byte #2 [0 X X X X X X X]
17-20	TC-APId byte #3 [0 X X X X X X X]
:	:
:	:
:	:
65-68	TC-APId byte #15 [0 X X X X X X X]
69-72	TC-APId byte #16 [0 X X X X X X X]
73-76	TC-RDI, ODI and Reserved (see Table D.4)

TABLE D.4/G.707

Structure of frames # 73 - 76 of the b7-b8 multiframe

TC-RDI, ODI and reserved capacity		
Frame #	b7 definition	b8 definition
73	Reserved (default = "0")	TC-RDI
74	ODI	Reserved (default = "0")
75	Reserved (default = "0")	Reserved (default = "0")
76	Reserved (default = "0")	Reserved (default = "0")

D.2 TCM functionality at the Tandem Connection source

- If no valid AU-n/TU-n enters the Tandem Connection at the TC-source then a valid pointer is inserted. This results in a VC-AIS signal as described in 6.2.4.1.3 being inserted; the IEC is set to "incoming AIS" code (see Table D.2).
- If a valid AU-n/TU-n enters the Tandem Connection, then an even BIP-8 is computed for each bit n of every byte of the VC-n in the preceding frame including B3 and compared with byte B3 recovered from the current frames to determine the number of BIP violations arriving at the Tandem Connection source. This value is coded into bits 1 to 4 as shown in Table D.2.
  - In both cases bits 4-8 are assembled and transmitted according to Tables D.1, D.3 and D.4. The bits TC-REI, TC-RDI, OEI, ODI are set to "1" if the corresponding anomaly or defect is detected at the associated TC-sink of the reverse direction.
  - The BIP-8 is compensated according to the algorithm described in D.4

NOTE – If an unequipped or supervisory unequipped signal enters a Tandem Connection, then the N1 and B3 bytes are overwritten with values not equal to all zeroes.

D.3 TCM functionality at the Tandem Connection sink

- If no valid AU-n/TU-n arrives at the TC-sink, the corresponding defect caused within the Tandem Connection is declared. The TC-RDI and ODI bits are set to 1 in the reverse direction and an AU/TU-AIS is inserted in the egressing AU-n/TU-n.
- If a valid AU-n/TU-n is present at the TC-sink the N1 byte is monitored:
  - An "all-zeroes" N1-byte indicates a dis- or misconnection within the Tandem Connection. In this case the TC-RDI and ODI bits are set to 1 in the reverse direction and an AU/TU-AIS is inserted in the egressing AU-n/TU-n.
  - The multiframe in bits 7 and 8 is recovered and the contents are interpreted. If the multiframe cannot be found, the TC-RDI and ODI bits are set to 1 in the reverse direction and AU/TU-AIS is inserted in the egressing AU-n/TU-n.
  - The TC-APId is recovered and compared with the expected TC-APId. In the case of a mismatch, the TC-RDI and ODI bits are set to 1 in the reverse direction and AU/TU-AIS is inserted in the egressing AU-n/TU-n.
  - The IEC field is interpreted according to the Table D.5.

An "incoming AIS"-code indicates that a defect has already occurred before the Tandem Connection. In this case only the ODI-bit is set to 1 in the reverse direction and AU/TU-AIS is inserted in the egressing AU-n/TU-n.

The even BIP-8 parity is computed for each bit n of every byte of the VC-n in the preceding frame including B3 and compared with byte B3 recovered from the current frames to determine the number of BIP violations. The OEI bit is set to 1 in the reverse direction if the number of determined BIP-violations is greater than zero. Furthermore this value is compared with the number of BIP-violations retrieved from IEC of the current frame. If the difference is not equal to zero, an errored block caused within the Tandem Connection is declared and a TC-REI bit is signalled in the reverse direction.

If TU-n/AU-AIS is not inserted by the Tandem Connection sink, the N1 Byte is set to all zeroes and the BIP is compensated according to the algorithm described in D.4.

TABLE D.5/G.707

IEC code interpretation

b1	b2	b3	b4	IEC code interpretation
0	0	0	0	0 BIP violations
0	0	0	1	1 BIP violation
0	0	1	0	2 BIP violations
0	0	1	1	3 BIP violations
0	1	0	0	4 BIP violations
0	1	0	1	5 BIP violations
0	1	1	0	6 BIP violations
0	1	1	1	7 BIP violations
1	0	0	0	8 BIP violations
1	0	0	1	0 BIP violations
1	0	1	0	0 BIP violations
1	0	1	1	0 BIP violations
1	1	0	0	0 BIP violations
1	1	0	1	0 BIP violations
1	1	1	0	0 BIP violations Incoming AIS
1	1	1	1	0 BIP violations

D.4 BIP-8 compensation

Since the BIP-8 parity check is taken over the VC-n (including N1), writing into N1 at the TC-source or TC-sink will affect the VC-4/VC-3 path parity calculation. Because the BIP-8 parity should always be consistent with the current state of the VC-n, the BIP has to be compensated each time N1 byte is modified. Since the BIP-8 value in a given frame reflects the parity check over the previous frame, the changes made to BIP-8 bits in the previous frame shall also be considered in the compensation of BIP-8 in the current frame. Therefore the following equation shall be used for compensation of the individual bits of the BIP-8:

$$B3[i]'(t) = B3[i](t-1) \oplus B3[i]'(t-1) \oplus N1[i](t-1) \oplus N1[i]'(t-1) \oplus B3[i](t)$$

Where:

B3[i] = the existing B3[i] value in the incoming signal

B3[i]' = the new (compensated) B3[i] value.

. N1[i] = the existing N1[i] value in the incoming signal.

N1[i]' = the new value written into the N1[i] bit.

$\oplus$ = exclusive OR operator.

t = the time of the current frame.

t–1 = the time of the previous frame.

Annex E

VC-2/VC-1 Tandem Connection Monitoring protocol

(This Annex forms an integral part of this Recommendation)

E.1 N2 byte structure

N2 is allocated for Tandem Connection Monitoring for the VC2, VC-12 and VC-11 level. The structure of the N2 byte is given in Table E.1.

- Bits 1-2 are used as an even BIP-2 for the Tandem Connection.
- Bit 3 is fixed to "1". This guarantees that the contents of N2 is not all zeroes at the TC-source. This enables the detection of an unequipped or supervisory unequipped signal at the Tandem Connection sink without the need of monitoring further OH-bytes.
- Bit 4 operates as an "incoming AIS" indicator.
- Bit 5 operates as the TC-REI of the Tandem Connection to indicate errored blocks caused within the Tandem Connection.
- Bit 6 operates as the OEI to indicate errored blocks of the egressing VC-n.
- Bits 7-8 operate in a 76 multiframe as:
  - the access point identifier of the Tandem Connection (TC-APId); it complies with the generic 16-byte string format given in 9.2.2.2;
  - the TC-RDI, indicating to the far end that defects have been detected within the Tandem Connection at the near end Tandem Connection sink;
  - the ODI, indicating to the far end that TU-AIS has been inserted at the TC-sink into the egressing TU-n due to defects before or within the Tandem Connection;
  - reserved capacity (for future standardization).

The structure of the multiframe is given in Tables E.2 and E.3.

TABLE E.1/G.707

N2 byte structure

b1	b2	b3	b4	b5	b6	b7	b8
BIP-2		"1"	Incoming AIS	TC-REI	OEI	TC-APId, TC-RDI ODI, reserved	

TABLE E.2/G.707

b7-b8 multiframe structure

Frame #	b7-b8 definition
1-8	Frame Alignment Signal: 1111 1111 1111 1110
9-12	TC-APId byte #1 [1 $C_1C_2C_3C_4C_5C_6C_7$]
13-16	TC-APId byte #2 [0 X X X X X X X]
17-20	TC-APId byte #3 [0 X X X X X X X]
:	:
:	:
:	:
65-68	TC-APId byte #15 [0 X X X X X X X]
69-72	TC-APId byte #16 [0 X X X X X X X]
73-76	TC-RDI, ODI and Reserved (See Table E.3)

TABLE E.3/G.707

Structure of frames # 73 - 76 of the b7-b8 multiframe

TC-RDI, ODI and reserved capacity		
Frame #	b7 definition	b8 definition
73	Reserved (default = "0")	TC-RDI
74	ODI	Reserved (default = "0")
75	Reserved (default = "0")	Reserved (default = "0")
76	Reserved (default = "0")	Reserved (default = "0")

E.2 TCM functionality at the Tandem Connection source

- If no valid TU-n is entering the Tandem Connection at the TC-source, a valid pointer is inserted. This results in a VC-AIS signal as described in 6.2.4.1.3 are inserted and bit 4 is set to "1". Even BIP-2 parity is calculated over the inserted VC-AIS signal and written into bits 1-2 of N2.
- If a valid TU-n is entering the Tandem Connection at the Tandem Connection source then even BIP-2 parity is calculated over the incoming valid VC-n or the inserted VC-AIS signal and written into bits 1-2 of N2.
  - In both cases bits 4-8 are assembled and transmitted according Tables E.1, E.2 and E.3. The bits TC-REI, TC-RDI, OEI, ODI are set to "1" if the corresponding anomaly or defect is detected at the associated TC-sink of the reverse direction.
  - The original BIP-2 is compensated according to the algorithm described in E.4.

NOTE – In an unequipped or supervisory unequipped signal entering a Tandem Connection, the N2 and V5 bytes are overwritten with values not equal to all zeroes.

E.3 TCM functionality at the Tandem Connection sink

If no valid TU-n is present at the TC-sink, a defect caused within the Tandem Connection is stated and the TC-RDI and ODI conditions apply. Outgoing the Tandem Connection a TU-AIS is inserted.

If a valid TU-n is present at the TC-sink, the N2 byte is monitored:

– An "all-zeroes" N1-byte indicates a dis- or misconnection within the Tandem Connection. In this case the TC-RDI and ODI-bits are set to 1 in the reverse direction and TU-AIS is inserted in the egressing TU-n.

– Bit 4 of the received N2 set to "1" indicates that a defect has already occurred before the Tandem Connection. In this case the ODI bit is set to 1 in the reverse direction and TU-AIS is inserted in the egressing TU-n.

– The multiframe in bits 7 and 8 is recovered and the contents are interpreted. If the multiframe cannot be found the TC-RDI and ODI bits are set to 1 in the reverse direction and TU-AIS is inserted in the egressing TU-n.

– The TC-APId is recovered and compared with the expected TC-APId. In the case of a mismatch, the TC-RDI and ODI bits are set to 1 in the reverse direction and TU-AIS is inserted in the egressing TU-n.

The even BIP-2 is computed for each bit pair of every byte of the preceding VC-n including V5 and compared with the BIP-2 retrieved from the V5-byte. A difference not equal to zero indicates that the VC-n has been corrupted and then the OEI bit is set to "1" in the reverse direction. Furthermore the actual BIP-2 is compared with the BIP-2 retrieved from the N2-byte. A difference not equal to zero indicates that the VC-n has been corrupted within the Tandem Connection and then the TC-REI is set to "1" in the reverse direction.

If TU-AIS is not inserted at the Tandem Connection sink then the N2-Byte is set to all zeroes and the BIP is compensated according to the algorithm described in E.4.

E.4 BIP-2 compensation

Since the BIP-2 parity check is taken over the VC-n (including N2), writing into N2 at the TC-source or TC-sink will affect the VC-2/VC-12/VC-11 path parity calculation. Unless this is compensated the error monitoring mechanism of BIP-2 is corrupted. Because the parity should always be consistent with the current state of the VC-n, the BIP has to be compensated each time N2-byte is modified. Since the BIP-2 value in a given frame reflects the parity check over the previous frame, the changes made to BIP-2 bits in the previous frame shall also be considered in the compensation of BIP-2 in the current frame. Therefore the following equation shall be used for compensation of the individual bits of the BIP-2:

$$V5[1]'(t) = V5[1](t-1) \oplus V5[1]'(t-1) \oplus N2[1](t-1) \oplus N2[3](t-1) \oplus N2[5](t-1) \oplus N2[7](t-1) \oplus N2[1]'(t-1) \oplus N2[3]'(t-1) \oplus N2[5]'(t-1) \oplus N2[7]'(t-1) \oplus V5[1](t)$$

$$V5[2]'(t) = V5[2](t-1) \oplus V5[2]'(t-1) \oplus N2[2](t-1) \oplus N2[4](t-1) \oplus N2[6](t-1) \oplus N2[8](t-1)$$

⊕ N2[2]'(t–1) ⊕ N2[4]'(t–1) ⊕ N2[6]'(t–1) ⊕ N2[8]'(t–1)

⊕ V5[2](t)

Where:

V5[i] = the existing V5[i] value in the incoming signal.

V5[i]' = the new (compensated) V5[i] value.

N2[i] = the existing N2[i] value in the incoming signal.

N2[i]' = the new value written into the N2[i] bit.

⊕ = exclusive OR operator.

t = the time of the current frame.

t–1 = the time of the previous frame.

Appendix I

Relationship between TU-2 address and location of columns within a VC-4

(This Appendix does not form an integral part of this Recommendation)

Table I.1 below shows the relationship between TU-2 address and location of columns within a VC-4.

TABLE I.1/G.707

Relationship between TU-2 address and location of columns within a VC-4

TU-2 address			TU-2 column number											
K	L	M	1	2	3	4	5	6	7	8	9	10	11	12
1	1	0	10	31	52	73	94	115	136	157	178	199	220	241
1	2	0	13	34	55	76	97	118	139	160	181	202	223	244
1	3	0	16	37	58	79	100	121	142	163	184	205	226	247
1	4	0	19	40	61	82	103	124	145	166	187	208	229	250
1	5	0	22	43	64	85	106	127	148	169	190	211	232	253
1	6	0	25	46	67	88	109	130	151	172	193	214	235	256
1	7	0	28	49	70	91	112	133	154	175	196	217	238	259
2	1	0	11	32	53	74	95	116	137	158	179	200	221	242
2	2	0	14	35	56	77	98	119	140	161	182	203	224	245
2	3	0	17	38	59	80	101	122	143	164	185	206	227	248
2	4	0	20	41	62	83	104	125	146	167	188	209	230	251
2	5	0	23	44	65	86	107	128	149	170	191	212	233	254
2	6	0	26	47	68	89	110	131	152	173	194	215	236	257
2	7	0	29	50	71	92	113	134	155	176	197	218	239	260
3	1	0	12	33	54	75	96	117	138	159	180	201	222	243
3	2	0	15	36	57	78	99	120	141	162	183	204	225	246
3	3	0	18	39	60	81	102	123	144	165	186	207	228	249

TABLE I.1/G.707 (concluded)

Relationship between TU-2 address and location of columns within a VC-4

TU-2 address			TU-2 column number											
3	4	0	21	42	63	84	105	126	147	168	189	210	231	252
3	5	0	24	45	66	87	108	129	150	171	192	213	234	255
3	6	0	27	48	69	90	111	132	153	174	195	216	237	258
3	7	0	30	51	72	93	114	135	156	177	198	219	240	261

Appendix II

Relationship between TU-12 address and location of columns within a VC-4

(This Appendix does not form an integral part of this Recommendation)

Table II.1 below shows the relationship between TU-12 address and location of columns within a VC-4.

TABLE II.1/G.707

Relationship between TU-12 address and location of columns within a VC-4

TU-12 address			TU-12 column number			
K	L	M	1	2	3	4
1	1	1	10	73	136	199
1	1	2	31	94	157	220
1	1	3	52	115	178	241
1	2	1	13	76	139	202
1	2	2	34	97	160	223
1	2	3	55	118	181	244
1	3	1	16	79	142	205
1	3	2	37	100	163	226
1	3	3	58	121	184	247
1	4	1	19	82	145	208
1	4	2	40	103	166	229
1	4	3	61	124	187	250
1	5	1	22	85	148	211
1	5	2	43	106	169	232
1	5	3	64	127	190	253
1	6	1	25	88	151	214
1	6	2	46	109	172	135
1	6	3	67	130	193	256
1	7	1	28	91	154	217
1	7	2	49	112	175	238
1	7	3	70	133	196	259

TABLE II.1/G.707 (continued)

Relationship between TU-12 address and location of columns within a VC-4

TU-12 address			TU-12 column number			
2	1	1	11	74	137	200
2	1	2	32	95	158	221
2	1	3	53	116	179	242
2	2	1	14	77	140	203
2	2	2	35	98	161	224
2	2	3	56	119	182	245
2	3	1	17	80	143	206
2	3	2	38	101	164	227
2	3	3	59	122	185	248
2	4	1	20	83	146	209
2	4	2	41	104	167	230
2	4	3	62	125	188	251
2	5	1	23	86	149	212
2	5	2	44	107	170	233
2	5	3	65	128	191	254
2	6	1	26	89	152	215
2	6	2	47	110	173	236
2	6	3	68	131	194	257
2	7	1	29	92	155	218
2	7	2	50	113	176	239
2	7	3	71	134	197	260
3	1	1	12	75	138	201
3	1	2	33	96	159	222
3	1	3	54	117	180	243
3	2	1	15	78	141	204
3	2	2	36	99	162	225
3	2	3	57	120	183	246
3	3	1	18	81	144	207
3	3	2	39	102	165	228
3	3	3	60	123	186	249
3	4	1	21	84	147	210
3	4	2	42	105	168	231
3	4	3	63	126	189	252
3	5	1	24	87	150	213
3	5	2	45	108	171	234

TABLE II.1/G.707 (concluded)

Relationship between TU-12 address and location of columns within a VC-4

TU-12 address			TU-12 column number			
3	5	3	66	129	192	255
3	6	1	27	90	153	216
3	6	2	48	111	174	237
3	6	3	69	132	195	258
3	7	1	30	93	156	219
3	7	2	51	114	177	240
3	7	3	72	135	198	261

Appendix III

Relationship between TU-11 address and location of columns within a VC-4

(This Appendix does not form an integral part of this Recommendation)

Table III.1 below shows the relationship between TU-11 address and location of columns within a VC-4.

TABLE III.1/G.707

Relationship between TU-11 address and location of columns within a VC-4

TU-11 address			TU-11 column number		
K	L	M	1	2	3
1	1	1	10	94	178
1	1	2	31	115	199
1	1	3	52	136	220
1	1	4	73	157	241
1	2	1	13	97	181
1	2	2	34	118	202
1	2	3	55	139	223
1	2	4	76	160	244
1	3	1	16	100	184
1	3	2	37	121	205
1	3	3	58	142	226
1	3	4	79	163	247
1	4	1	19	103	187
1	4	2	40	124	208
1	4	3	61	145	229
1	4	4	82	166	250
1	5	1	22	106	190
1	5	2	43	127	211

TABLE III.1/G.707 (continued)

Relationship between TU-11 address and location of columns within a VC-4

TU-11 address			TU-11 column number		
1	5	3	64	148	232
1	5	4	85	169	253
1	6	1	25	109	193
1	6	2	46	130	214
1	6	3	67	151	135
1	6	4	88	172	256
1	7	1	28	112	196
1	7	2	49	133	217
1	7	3	70	154	238
1	7	4	91	175	259
2	1	1	11	95	179
2	1	2	32	116	200
2	1	3	53	137	221
2	1	4	74	158	242
2	2	1	14	98	182
2	2	2	35	119	203
2	2	3	56	140	224
2	2	4	77	161	245
2	3	1	17	101	185
2	3	2	38	122	206
2	3	3	59	143	227
2	3	4	80	164	248
2	4	1	20	104	188
2	4	2	41	125	209
2	4	3	62	146	230
2	4	4	83	167	251
2	5	1	23	107	191
2	5	2	44	128	212
2	5	3	65	149	233
2	5	4	86	170	254
2	6	1	26	110	194
2	6	2	47	131	215

TABLE III.1/G.707 (concluded)

Relationship between TU-11 address and location of columns within a VC-4

TU-11 address			TU-11 column number		
2	6	3	68	152	236
2	6	4	89	173	257
2	7	1	29	113	197
2	7	2	50	134	218
2	7	3	71	155	239
2	7	4	92	176	260
3	1	1	12	96	180
3	1	2	33	117	201
3	1	3	54	138	222
3	1	4	75	159	243
3	2	1	15	99	183
3	2	2	36	120	204
3	2	3	57	141	225
3	2	4	78	162	246
3	3	1	18	102	186
3	3	2	39	123	207
3	3	3	60	144	228
3	3	4	81	165	249
3	4	1	21	105	189
3	4	2	42	126	210
3	4	3	63	147	231
3	4	4	84	168	252
3	5	1	24	108	192
3	5	2	45	129	213
3	5	3	66	150	234
3	5	4	87	171	255
3	6	1	27	111	195
3	6	2	48	132	216
3	6	3	69	153	237
3	6	4	90	174	258
3	7	1	30	114	198
3	7	2	51	135	219
3	7	3	72	156	240
3	7	4	93	177	261

Appendix IV

Relationship between TU-2 address and location of columns within a VC-3

(This Appendix does not form an integral part of this Recommendation)

Table IV.1 below shows the Relationship between TU-2 address and location of columns within a VC-3.

TABLE IV.1/G.707

Relationship between TU-2 address and location of columns within a VC-3

TU-2 address		TU-2 column number											
L	M	1	2	3	4	5	6	7	8	9	10	11	12
1	0	2	9	16	23	30	37	44	51	58	65	72	79
2	0	3	10	17	24	31	38	45	52	59	66	73	80
3	0	4	11	18	25	32	39	46	53	60	67	74	81
4	0	5	12	19	26	33	40	47	54	61	68	75	82
5	0	6	13	20	27	34	41	48	55	62	69	76	83
6	0	7	14	21	28	35	42	49	56	63	70	77	84
7	0	8	15	22	29	36	43	50	57	64	71	78	85

Appendix V

Relationship between TU-12 address and location of columns within a VC-3

(This Appendix does not form an integral part of this Recommendation)

Table V.1 below shows the relationship between TU-12 address and location of columns within a VC-3.

TABLE V.1/G.707

Relationship between TU-12 address and location of columns within a VC-3

TU-12 address		TU-12 column number			
L	M	1	2	3	4
1	1	2	23	44	65
1	2	9	30	51	72
1	3	16	37	58	79
2	1	3	24	45	66
2	2	10	31	52	73
2	3	17	38	59	80
3	1	4	25	46	67
3	2	11	32	53	74
3	3	18	39	60	81
4	1	5	26	47	68

TABLE V.1/G.707 (concluded)

Relationship between TU-12 address and location of columns within a VC-3

TU-12 address		TU-12 column number			
4	2	12	33	54	75
4	3	19	40	61	82
5	1	6	27	48	69
5	2	13	34	55	76
5	3	20	41	62	83
6	1	7	28	49	70
6	2	14	35	56	77
6	3	21	42	63	84
7	1	8	29	50	71
7	2	15	36	57	78
7	3	22	43	64	85

Appendix VI

Relationship between TU-11 address and location of columns within a VC-3

(This Appendix does not form an integral part of this Recommendation)

Table VI.1 below shows the relationship between TU-11 address and location of columns within a VC-3.

TABLE VI.1/G.707

Relationship between TU-11 address and location of columns within a VC-3

TU-11 address		TU-11 column number		
L	M	1	2	3
1	1	2	30	58
1	2	3	31	59
1	3	5	33	61
1	4	7	35	63
2	1	4	32	60
2	2	12	40	68
2	3	18	46	74
2	4	24	52	80
3	1	6	34	62
3	2	13	41	69
3	3	19	47	75
3	4	25	53	81
4	1	8	36	64

TABLE VI.1/G.707 (concluded)

Relationship between TU-11 address and location of columns within a VC-3

TU-11 address		TU-11 column number		
4	2	14	42	70
4	3	20	48	76
4	4	26	54	82
5	1	9	37	65
5	2	15	43	71
5	3	21	49	77
5	4	27	55	83
6	1	10	38	66
6	2	16	44	72
6	3	22	50	78
6	4	28	56	84
7	1	11	39	67
7	2	17	45	73
7	3	23	51	79
7	4	29	57	85

Appendix VII

Enhanced Remote Defect Indication (RDI)

(This Appendix does not form an integral part of this Recommendation)

As an option, equipment may provide additional defect differentiation among the remote detected defects. This appendix provides the detail for that option.

VII.1 VC-4-Xc/VC-4/VC-3 paths

As described in 9.3.1.4, byte G1 is allocated to convey back to a VC-4-Xc/VC-4/VC-3 trail termination source the status and performance of the complete trail. Bits 5 to 7 of byte G1 may provide a remote defect indication with additional differentiation between the remote payload defect (LCD), server defects (AIS, LOP) and the remote connectivity defects (TIM, UNEQ). The optional codes from Table VII.1 will be used. Use of the "010" code to indicate payload defects does not imply a requirement to use the "101" and "110" codes to distinguish between server and connectivity defects.

TABLE VII.1/G.707

G1 (b5-b7) coding and interpretation

b5	b6	b7	Meaning	Triggers
0	0	0	No remote defect	No remote defect
0	0	1	No remote defect	No remote defect
0	1	1	No remote defect	No remote defect
0	1	0	Remote payload defect	LCD (Note 1)
1	0	0	Remote defect	AIS, LOP TIM, UNEQ (or PLM, LCD) (Note 2)
1	1	1	Remote defect	AIS, LOP TIM, UNEQ (or PLM, LCD) (Note 2)
1	0	1	Remote server defect	AIS, LOP (Note 3)
1	1	0	Remote connectivity defect	TIM, UNEQ

NOTES

1 LCD is the only currently defined payload defect and is applicable to ATM equipment only.

2 Old equipment may include LCD or PLM as a trigger condition. PLM and UNEQ have previously been covered by SLM.

3 Remote server defect defined in server signal failure defined in Recommendation G.783.

For these optional codes, bit 7 is always set to the inverse of bit 6 to allow equipment which supports this feature to identify that it is interworking with equipment that uses the single bit RDI defined in 9.3.1.4. In such a case equipment at both ends will interpret only bit 1-5 of G1.

VII.2 VC-2/VC-1 paths

As described in 9.3.2.1, bits 3, 4 and 8 of byte V5 are allocated to convey back to a VC-2/VC-1 trail termination source the status and performance of the complete trail. Bits 5 to 7 of byte K4 may provide a remote defect indication with additional differentiation between the remote payload defect (LCD), server defects (AIS, LOP) and the remote connectivity defects (TIM, UNEQ). The optional codes from Table VII.2 will be used. Use of the "010" code to indicate payload defects does not imply a requirement to use the "101" and "110" codes to distinguish between server and connectivity defects.

TABLE VII.2/G.707

K4 (b5-b7) coding and interpretation

b5	b6	b7	Meaning	Triggers
0	0	0	No remote defect	No remote defect
0	0	1	No remote defect	No remote defect
0	1	1	No remote defect	No remote defect
0	1	0	Remote payload defect	LCD (Note 1)
1	0	0	Remote defect	AIS, LOP TIM, UNEQ (or PLM, LCD) (Note 2)
1	1	1	Remote defect	AIS, LOP TIM, UNEQ (or PLM, LCD) (Note 2)
1	0	1	Remote server defect	AIS, LOP (Note 3)
1	1	0	Remote connectivity defect	TIM, UNEQ

NOTES

1 LCD is the only currently defined payload defect and is applicable to ATM equipment only.

2 Old equipment may include LCD or PLM as a trigger condition. PLM and UNEQ have previously been covered by SLM.

3 Remote server defect defined in server signal failure defined in Recommendation G.783.

For these optional codes, bit 7 is always set to the inverse of bit 6 to allow equipment which supports this feature to identify that it is interworking with equipment that uses the single bit RDI defined in 9.3.2.1. In such a case equipment at both ends will interpret only V5.

Appendix VIII

A possible future definition of MS-REI

(This Appendix does not form an integral part of this Recommendation)

This informative appendix contains a possible definition of an MS-REI which may be applicable if a N block structure is defined for the Multiplex Section block structure of an STM-N.

For STM-N levels M1 byte conveys the count (0 to N) of interleaved bit blocks that have been detected in error. Each of the N interleaved bit blocks is controlled by a BIP-24 error detection code; the generic i-th (i = 1..N) interleaved bit block is controlled by S(5, 1, i), S(5, 2, i) and S(5, 3, i) bytes (in row, column notation [5, i], [5, N+i] and [5, 2N+i]).

STM-1, M1 generation: the byte shall be set to "0000 0001" if one or more errors were detected by the BIP-24 process, and shall be set to all zeros "0000 0000" otherwise.

STM-1, M1 interpretation: the value in the byte shall be interpreted, for interworking with equipment generating a code that represents the number of BIP-24 violations, as follows:

M1[2-8] code, bits 234 5678	Code interpretation
000 0000	0 errored blocks
000 0001	1 errored block
000 0010	1 errored block
000 0011	1 errored block
:	:
001 1000	1 errored block
001 1001	0 errored blocks
001 1010	0 errored blocks
:	:
111 1111	0 errored blocks
NOTE – Bit 1 of byte M1 is ignored.	

STM-4, M1 generation: the byte shall be set to one of the values in the table below if one or more BIP violations were detected, and shall be set to all zeros "0000 0000" otherwise.

Number of errored blocks	M1[1-8] code, bits 1234 5678
0 errored block	0000 0000
1 errored block	0000 0001
2 errored blocks	0000 0010
3 errored blocks	0000 0011
4 errored blocks	0000 0100

STM-4, M1 interpretation: the value in the byte shall be interpreted, for interworking with equipment generating a 7-bit code that represents the number of BIP-96 violations, as follows:

M1[2-8] code, bits 234 5678	Code interpretation
000 0000	0 errored blocks
000 0001	1 errored block
000 0010	2 errored blocks
000 0011	3 errored blocks
000 0100	4 errored blocks
000 0101	4 errored blocks
:	:
110 0000	4 errored blocks
110 0001	0 errored blocks
110 0010	0 errored blocks
:	:
111 1111	0 errored blocks
NOTE – Bit 1 of byte M1 is ignored.	

STM-16, M1 generation: the byte shall be set to one of the values in the table below if one or more BIP violations were detected, and shall be set to all zeros "0000 0000" otherwise.

Number of errored blocks	M1[1-8] code, bits 1234 5678
0 errored block	0000 0000
1 errored block	0000 0001
2 errored blocks	0000 0010
3 errored blocks	0000 0011
:	:
:	:
16 errored blocks	0001 0000

STM-16, M1 interpretation: the value in the byte shall be interpreted as follows:

M1[1-8] code, bits 1234 5678	Code interpretation
0000 0000	0 errored blocks
0000 0001	1 errored block
0000 0010	2 errored blocks
0000 0011	3 errored blocks
0000 0100	4 errored blocks
0000 0101	5 errored blocks
:	:
0001 0000	16 errored blocks
0001 0001	0 errored blocks
0001 0010	0 errored blocks
:	:
1111 1111	0 errored blocks

STM-64, M1 generation: the byte shall be set to one of the values in the table below if one or more BIP violations were detected, and shall be set to all zeros "0000 0000" otherwise.

Number of errored blocks	M1[1-8] code, bits 1234 5678
0 errored block	0000 0000
1 errored block	0000 0001
2 errored blocks	0000 0010
3 errored blocks	0000 0011
:	:
:	:
64 errored blocks	1000 0000

STM-64, M1 interpretation: the value in the byte shall be interpreted as follows:

M1[1-8] code, bits 1234 5678	Code interpretation
0000 0000	0 errored blocks
0000 0001	1 errored block
0000 0010	2 errored blocks
0000 0011	3 errored blocks
0000 0100	4 errored blocks
0000 0101	5 errored blocks
:	:
1000 0000	64 errored blocks
1000 0001	0 errored blocks
1000 0010	0 errored blocks
:	:
1111 1111	0 errored blocks

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