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SYNCHRONOUS DATA TRANSMISSION AT A DATA SIGNALLING RATE HIGHER THAN 72 kbit/s USING 60-108 kHz GROUP BAND CIRCUITS

ITU-T Recommendation V.37

(Extract from the *Blue Book*)

NOTES

1 ITU-T Recommendation V.37 was published in Fascicle VIII.1 of the *Blue Book*. This file is an extract from the *Blue Book*. While the presentation and layout of the text might be slightly different from the *Blue Book* version, the contents of the file are identical to the *Blue Book* version and copyright conditions remain unchanged (see below).

2 In this Recommendation, the expression "Administration" is used for conciseness to indicate both a telecommunication administration and a recognized operating agency.

Recommendation V.37

SYNCHRONOUS DATA TRANSMISSION AT A DATA SIGNALLING RATE HIGHER THAN 72 kbit/s USING 60-108 kHz GROUP BAND CIRCUITS

(Geneva, 1980; amended at Malaga-Torremolinos, 1984 and at Melbourne, 1988)

1 Introduction

On leased circuits, considering that there exist and will come into being other modems with features designed to meet the requirements of Administrations and users, this Recommendation in no way restricts the use of any other modems.

The only group reference pilot frequency which can be used in conjunction with this modem is 104.08 kHz.

The modem is intended to be used on group band circuits not necessarily conforming to [1].

Principal characteristics:

a) transmission of any type of high-speed synchronous data in duplex constant carrier mode on 4-wire (60-108 kHz) group band circuits;

b) primary data signalling rates up to 144 kbit/s;

c) inclusion of an automatic adaptive equalizer;

d) class IV partial response pulse amplitude single sideband signalling and modulation;

e) optional inclusion of an overhead-free multiplexer combining existing data signalling rates;

f) optional voice channel.

2 Data signalling rates

2.1 The recommended synchronous data signalling rates are 96 kbit/s, 112 kbit/s, 128 kbit/s and 144 kbit/s. For some applications with agreement from the Administration, data signalling rates up to 168 kbit/s are applicable. (See the Note to § 7.)

2.2 The permitted tolerance for all data signalling rates is $\pm 5 \times 10^{-5}$.

3 Scrambler/descrambler

In order to be bit sequence independent, to avoid high amplitude spectral components on the line, and to allow the automatic equalizer to remain converged, the data should be scrambled and descrambled by means of the logical arrangements described in Appendix I.

4 Encoding method

The binary bit stream A, delivered by the scrambler, to be transmitted is divided into consecutive groups of 2 bits A_1 and A_2 (dibits), A_1 being the first in time delivered by the scrambler.

An amplitude level B is assigned to each dibit (A) as shown in Table 1/V.37.

TABLE 1/V.37

A_1	A_2	Equivalent B amplitude level
0	0	0
0	1	+1
1	1	+2
1	0	+3

A pre-encoder circuit converts the stream B into another quaternary stream C which conforms to the relation:

$$C_i = B_i \oplus C_{i-2}$$

where

$\oplus$ represents the modulo 4 sum

and the subscript i represents the i^{th} element of B or C.

The resulting quaternary stream C can be processed to form a baseband signal.

5 Baseband signal shaping

The equivalent baseband signal shaping process is based upon the binary coded partial response pulse, often referred to as class IV, whose time and spectral function are defined by:

$$g(t) = \frac{2}{\pi} \cdot \frac{\sin \frac{\pi}{T} t}{\left(\frac{t}{T}\right)^2 - 1}$$

and

$$G(f) = \begin{cases} 2\,T j \sin 2\,\pi\,T f\,, & |f| \leqslant \dfrac{1}{2\,T} \\ 0\,, & |f| > \dfrac{1}{2\,T} \end{cases}$$

respectively, where $1/T$ denotes the modulation rate.

The reference to equivalent baseband signals recognizes that the modem implementation may be such that the binary signal at the input and output of the modem is converted to and from the line signal without appearing as an actual baseband signal.

The baseband signal formed by the processes described above will present 7 levels (see Table 2/V.37).

The baseband signal shaping is performed in the transmitter,

TABLE 2/V.37

Level	Bit value	
	A_1	A_2
+3	1	0
+2	1	1
+1	0	1
0	0	0
-1	1	0
-2	1	1
-3	0	1

6 Line signal in the 60-108 kHz band (at the line output of the modem)

6.1 In the 60-108 kHz band, the line signal should correspond to a single sideband signal with its carrier frequency pilot and timing pilot at frequencies as specified in Table 3/V.37.

6.2 The amplitude of the theoretical line signal spectrum, corresponding to a quaternary symbol (+1) appearing at the output of the encoder, is sinusoidal. The zeros and maxima of the theoretical line spectrum are shown in Table 3/V.37.

TABLE 3/V.37

Data rate (kbit/s)	Zeros at (kHz)	Maxima at (KHz)	Pilot carrier frequency	Timing pilot frequency
144	64 and 100	82	100 kHz	64 kHz
128	68 and 100	84	100 kHz	68 kHz
112	72 and 100	86	100 kHz	72 kHz
96	76 and 100	88	100 kHz	76 kHz
168 (optional)	62 and 104	83	104 kHz	62 kHz

6.3 In the 60-108 kHz band, amplitude distortion of the real spectrum relative to the theoretical spectrum as defined under § 6.2 above is not to exceed ± 1 dB; the group-delay distortion is not to exceed 15 μs. These two requirements are to be met for each frequency band centred on one of the maxima mentioned in § 6.2 and whose width is equal to 80% of the frequency band used.

6.4 The nominal level of the line data signal should be -6 dBm0. The actual level should be within ± 1 dB of the nominal level.

6.5 A pilot carrier at the same frequency as the modulated carrier (100 kHz ± 2 Hz) at the transmitter and with a level of -9 ± 0.5 dB relative to the actual level mentioned under § 6.4 above, should be added to the line signal. The relative phase between the modulated carrier and the pilot carrier at the transmitter should be time invariant.

Note - For the optional data signalling rate of 168 kbit/s, the pilot carrier should be 104 kHz ± 2 Hz.

6.6 A timing pilot at a frequency difference from the carrier equal to half the modulation rate at the transmitter with a level of -12 ± 0.5 dB relative to the actual level mentioned under § 6.4 above, should be added to the line signal.

The relationship between the timing pilot and the pilot carrier should remain time invariant at the transmitter.

7 Group reference pilot

7.1 Provision should be made for facilitating the injection of a group reference pilot of 104.08 kHz from an external source.

7.2 The protection of the group reference pilot should conform to Recommendation H.52 [2].

Note - Group reference pilot must be removed from the channel for operation at 168 kbit/s.

8 Optional voice channel

The service speech channel may be an integral part of the application of this system and is used on an optional basis. The channel corresponds to channel 1 of a 12 channel SSB-AM system in the 104-108 kHz band (virtual carrier at 108 kHz). It can transmit continuous voice at a mean level of maximum -15 dBm0 or pulsed signalling tones according to the individual specifications.

To avoid overloading of the system by peak signals, a limiter shall be used with cut-off levels above +3 dBm0.

To avoid stability problems, the channel shall be connected to 4-wire equipment only.

The transmit filter shall be such that any frequency applied to the transmit input terminals at a level of -15 dBm0 will not cause a level exceeding:

a) -73 dBm0p in the adjacent group;

b) -61 dBm0 in the vicinity (± 25 Hz) of the pilot 104.08 kHz;

c) -55 dBm0 in the data band between 64 and 101 kHz. When the 168 kbit/s data signalling rate is used this requirement applies between 62 and 104 kHz.

The voiceband is sufficiently protected if the same filter is used in the receive direction of the channel. The attenuation/frequency characteristic, measured between the voice-frequency input and the group band output or the group input and the voice-frequency output, with respect to the value at 800 Hz is limited by:

-1 dB over the 300-3400 Hz band,

+2 dB between 540 and 2280 Hz.

Note - When the modem is installed at the repeater station, the voice channel should be extended to the customer's premises.

9 Adjacent channel interference

In the bands 36-60 kHz and 108-132 kHz the adjacent channel interference should conform to Recommendation H.52 [2].

10 Line characteristics

The modem will allow proper operation of data signalling rates up to 128 kbit/s over a circuit of similar construction as the Hypothetical Reference Circuit as specified in reference [3].

Note 1 - Reference [3] specifies a maximum number of 8 through-group filters, but this figure is subject to further study and possible amendment.

Note 2 - The modem will allow operation over a circuit having a maximum number of 5 through-group filters at 144 kbit/s.

Note 3 - The line characteristics for operation at 168 kbit/s are not specified.

11 Synchronizing signals

Transmission of synchronizing signals is initiated by the modem. When the receiving modem detects a condition which requires resynchronizing, it shall turn circuit 106 OFF and generate synchronizing signals.

The synchronizing signals for all data signalling rates are divided into three segments as indicated in Table 4/V.37.

TABLE 4/V.37

	Segment 1	Segment 2	Segment 3	Total of segments 1, 2 and 3	
Type of line signals	Only carrier and timing pilots	Carrier and timing pilots and alternation of levels (± 2)	Carrier and timing pilots and scrambled all binary ONEs	Data signalling rates (kbit/s)	Approximate time (s)
Number of symbol intervals	10 240	4096	262 144	96	5.76
				112	4.93
				128	4.32
				144	3.84
				168	3.29

11.1 Segment 1 transmits the carrier pilot, the timing pilot and data signal corresponding with the dibits (0, 0) applied at the input of the encoder.

11.2 Segment 2 consists of the carrier pilot, the timing pilot and an alternation between two signal levels (+2) and (-2) corresponding with the dibits (1, 1) applied at the input of the encoder.

11.3 Segment 3 consists of the carrier pilot, the timing pilot and scrambled all binary ONEs.

At the beginning of this segment:

- the scrambler shift register must be set to all 0s (see Appendix I);
- the adverse state detector counter must be set to all 1s (see Appendix I);
- the pre-encoder must be set to all 0s.

The equivalent baseband signal processed at the beginning of Segment 3 consists of a succession of 15 levels (0) followed by levels (+ 1), (0), (- 1), (+ 1), (0), (- 1), (+ 1), (0), (- 1), (+ 1), (+ 1), (- 1) . . . .

11.4 Circuit 106 is turned ON at the end of segment 3 and the user’s data may appear at the input of the scrambler.

12 Optional multiplexing

Multiplexing options shall be separately available to combine nominally available group band data rates of 48, 56, 64 or 72 kbit/s into a single aggregate bit stream for transmission as shown in Table 3/V.37. These multiplexers should be of a synchronous, overhead-free, bit interleave design. Using modem internal processing signals, multiplexers shall require no framing, allowing each subchannel to be a full one-half of the composite bit rate.

The two port multiplexer uses the bits from port A and B for bits A_1 and A_2 respectively of the dibits defined in § 4.

12.1 *Transmit buffers*

In the transmitter of each multiplex port, there shall be a data buffer of suitable capacity. In this way, both phase variations and, within certain limits, frequency deviations are absorbed. The buffer shall be initialized when an OFF to ON condition of circuit 105 occurs and may be repositioned in the event of a buffer overflow.

Note - The buffer may reinitialize upon a DCE resynchronization signal.

12.2 *Transmit port timing arrangements*

Table 5/V.37 shows all possible combinations of port and main DCE transmit timing clock arrangements.

TABLE 5/V.37

Source of port transmitter signal element timing (used to clock in circuit 103)	Source of DCE internal transmitter element timing (internal transmit clock)	Port transmit buffer
114 (DCE source)	Internal (Independent timing)	Not required
	External [a] (Circuit 113 of selected port)	Not required
	Receiver timing (Loopback timing)	Not required
113 (DTE source) [a]	Internal (Independent timing)	Required
	External [a] (Circuit 113 of selected port)	Required for all ports except port supplying circuit 113 to DCE
	Received timing (Loopback timing)	Required

[a] In these applications a source could also be another DCE.

13 Digital interface requirements

13.1 *List of interchange circuits* (see Table 6/V.37)

The interchange circuit table is valid for the main channel or the subchannel interfaces.

TABLE 6/V.37

Interchange circuit (see Note 1)		Remark
102 102a 102b	Signal ground or common return DTE commun return DCE common return	See Note 2 See Note 3 See Note 3
103 104	Transmitted data Received data	
105 106 107 109	Request to send Ready for sending Data set ready Data channel received line signal detector	See Note 4 See Note 4 and 5
113 114 115 128	Transmitter signal element timing (DTE source) Transmitter signal element timing (DCE source) Receiver signal element timing (DCE source) receiver signal element timing (DTE source)	See Note 4
140 141 142	Loop-back/Maintenance test Local loop-back Test indicator	See Note 4 See Note 6

Note 1 - When the modem is installed at the repeater station, this interface should appear at the customer's premises without restrictions regarding the data signalling rate and the provision of the voice channel. The method to achieve this is subject to national regulations.

Note 2 - The provision of this conductor is optional.

Note 3 - Interchange circuits 102a and 102b are required where the electrical characteristics defined in Recommendation V.10 are used.

Note 4 - Not essential in subchannel.

Note 5 - During the synchronisation process of the main modem, the OFF condition of circuit 106 is signalled at all port interface.

Note 6 - Circuit 142 is present on all ports of the multiplexer, but may be activated on an individual port basis for individual port tests. All are activated simultaneously for entire modem test.

13.2 *Electrical characteristics*

Use of electrical characteristics conforming to Recommendation V.10 and/or V.11 is recommended together with the use of the connector and pin assignment plan specified by ISO 4902.

i) Concerning circuits 103, 104, 113, 114 and 115, both the generators and the receivers shall be in accordance with Recommendation V.11.

ii) In the case of circuits 105, 106, 107 and 109, generators shall comply with Recommendation V.10 or alternatively Recommendation V.11. The receivers shall comply with Recommendation V.10, category 1, or V.11 without termination.

iii) In the case of all other circuits, Recommendation V.10 applies, with receivers configured as specified by Recommendation V.10 for category 2.

Note - For an interim period the connector and contact-assignment plan specified in ISO 2593 and commonly referred to as the "V.35 interface" may optionally be used. In this case electrical characteristics may be either V.11 for circuits 103, 104, 113, 114 and 115 together with V.10 (receivers configured as specified in category 2) for all other circuits, or V.35 Appendix II together with V.28 respectively.

14 Optional PCM interface alternative

The recommended data signalling rate is synchronous at 64 kbit/s.

For those synchronous networks requiring the end-to-end transmission of both the 8 kHz and 64 kHz timing together with the data at 64 kbit/s, an internal data signalling rate of 72 kbit/s is suggested.

The corresponding data format shall be obtained by inserting one extra bit (E) just before the first bit of each octet of the 64 kbit/s data stream.

The bits E convey alignment and housekeeping information, according to the pattern shown in Figure 1/V.37.

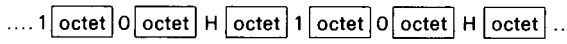


FIGURE 1/V.37

The use of the housekeeping bits H is determined with bilateral agreement between Administrations. When not used these bits should be assigned the value 1. A framing strategy is not specified in this Recommendation.

When the transmission of the 8 kHz timing is not required, the data signalling rate may be 64 kbit/s.

The interfaces shall comply with the functional requirements given in Recommendation G.703 [4] for the 64 kbit/s interface. The electrical characteristics may comply with reference [5].

If an end-to-end transmission of an 8 kHz timing signal is not used, an 8 kHz timing across the interface will not be supplied nor utilized by the modem.

15 Threshold and response times of circuit 109

15.1 *Threshold*

For a data line signal level greater than -13 dBm0, circuit 109 is ON. For a data line signal level less than -18 dBm0, circuit 109 is OFF.

Note - The corresponding levels for the pilot carrier are -22 dBm0 and -27 dBm0 respectively.

The condition of circuit 109 for levels between the above levels is not specified, except that the signal detector shall exhibit a hysteresis action such that the level at which the OFF to ON transition occurs is at least 2 dB greater than that for the ON to OFF transition. To measure the thresholds of the detector, a modulated data signal

with its carrier and timing pilots at the levels specified in §§ 6.5 and 6.6 above should be used.

15.2 *Response times*

ON to OFF: 15 to 50 ms.

OFF to ON:

1) For initial equalization, circuit 109 must be ON prior to user data appearing on circuit 104.

2) For re-equalization during data transfer, circuit 109 will be maintained in the ON condition. During this period, circuit 104 may be clamped to the binary 1 condition.

3) After a line signal interruption that lasts more than the ON to OFF response time:

   a) when no new equalization is needed, the exact figure is under study;

   b) when a new equalization is needed, circuit 109 must be ON prior to user data appearing in circuit 104.

The response times of circuit 109 are the time intervals between the appearance or disappearance of the line signal at the reception input terminals of the modem and the occurrence of the corresponding ON or OFF condition on circuit 109.

The line signal level should be within the range from 3 dB above the actual threshold of the line signal detector at reception and the maximum permissible level of the signal at reception.

16 Response times of circuit 106

ON to OFF response time less than or equal to 2 ms

OFF to ON response time less than or equal to 2 ms.

17 Equalizer

An automatic adaptive equalizer shall be provided in the receiver.

The receiver shall incorporate a means of detecting loss of equalization and initiating a synchronizing signal sequence in its associated local transmitter.

The receiver shall incorporate a means of detecting a synchronizing signal sequence from the remote transmitter and initiating a synchronizing signal sequence in its associated local transmitter, which may be initiated at any time during the reception of the synchronizing signal sequence.

Either modem can initiate the synchronizing signal sequence. The synchronizing signal is initiated when the receiver has detected a loss of equalization. Having initiated a synchronizing signal, the modem expects a synchronizing signal from the remote transmitter.

If the modem does not receive a synchronizing signal from the remote transmitter within a time interval equal to the maximum expected two-way propagation delay plus twice the synchronizing signal detection time, it transmits another synchronizing signal.

If the modem fails to synchronize on the received signal sequence, it transmits another synchronizing signal.

If a modem receives a synchronizing signal when it has not initiated a synchronizing signal and the receiver properly synchronizes, it returns only one synchronizing sequence.

18 Additional information for the designer

18.1 *Input level variation*

The step-change in the input level is, under normal conditions, smaller than ± 0.1 dB. The gradual input level change is smaller than ± 6 dB and includes the tolerance of the transmitter output level.

18.2 *Interference from adjacent group bands*

A sinusoidal signal of + 10 dBm0 in the frequency bands of 36-60 kHz and 108-132 kHz can appear together with the data line signal at the input of the receiver.

APPENDIX I

(to Recommendation V.37)

Scrambling process

I.1 *Definitions*

I.1.1 **applied data bit**

The data bit which has been applied to the scrambler but has not affected the transmission at the time of consideration.

I.1.2 **next transmitted bit**

The bit which will be transmitted as a result of scrambling the applied data bit.

I.1.3 **earlier transmitted bits**

Those bits which have been transmitted earlier than the next transmitted bit. They are numbered sequentially in reverse time order, i.e. the first earlier transmitted bit is that immediately preceding the next transmitted bit.

I.1.4 **adverse state**

The presence of any one of certain repetitive patterns in the earlier transmitted bits.

I.2 *Scrambling process*

The binary value of the next transmitted bit shall be such as to produce odd parity when considered together with the twentieth and third earlier transmitted bits and the applied data bit unless an adverse state is apparent, in which case the binary value of the next transmitted bit shall be such as to produce even instead of odd parity.

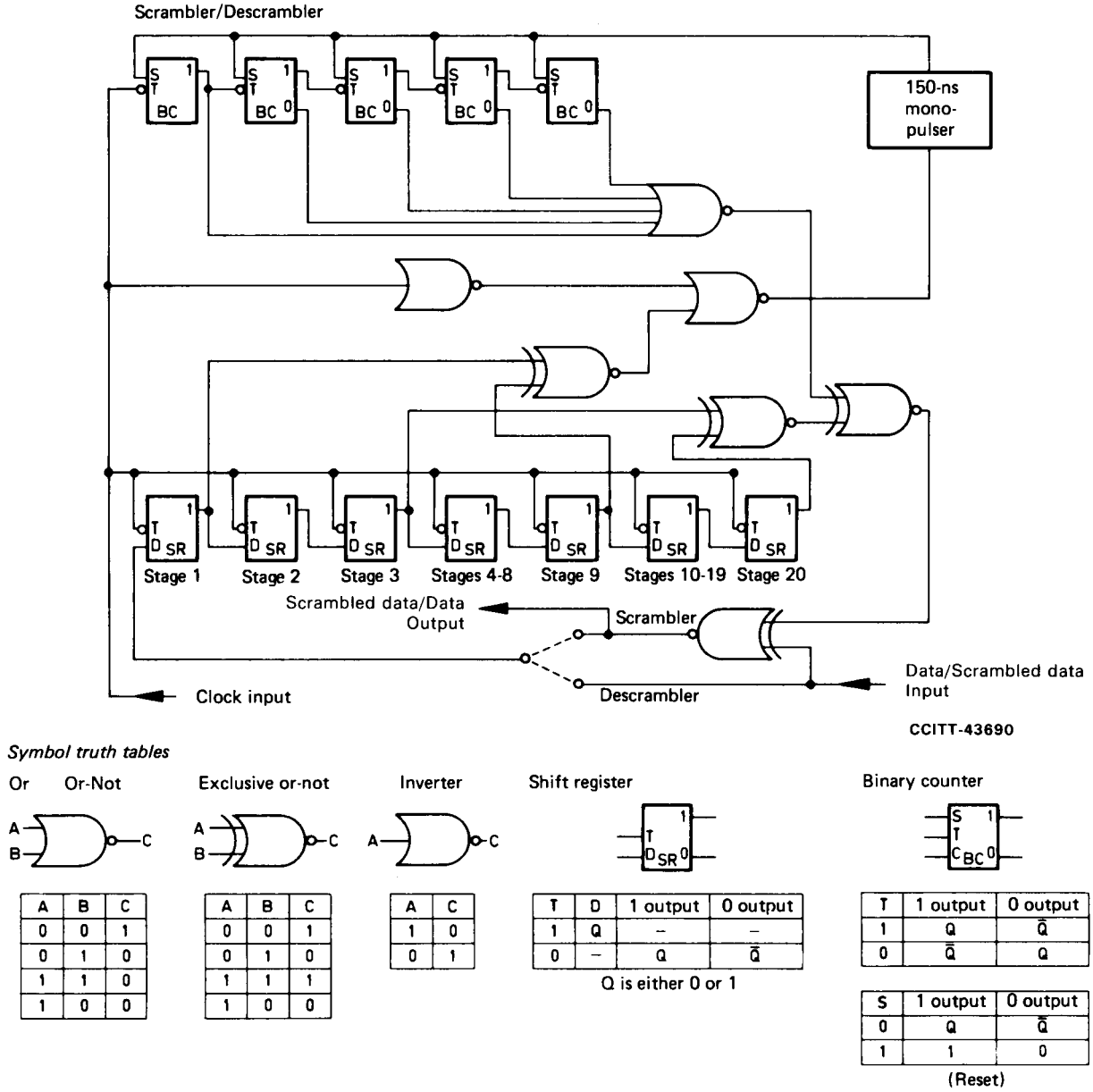
An adverse state shall be apparent only if the binary values of the p^{th} and $(p + 8)^{th}$ earlier transmitted bits have not differed from one another when p represents all the integers from 1 to q inclusive. The value of q shall be such that, for $p = (q + 1)$, the p^{th} and $(p + 8)^{th}$ earlier transmitted bits had opposite binary values and $q = (31 + 32\ r)$, r being 0 or any positive integer.

At the time of commencement, i.e. when no earlier bits have been transmitted, an arbitrary 20-bit pattern may be assumed to represent the earlier transmitted bits. At this time also it may be assumed that the p^{th} and $(p + 8)^{th}$ earlier transmitted bits have had the same binary value when p represents all the integers up to any arbitrary value. Similar assumptions may be made for the descrambling process at commencement.

Note 1 - From this it can be seen that received data cannot necessarily be descrambled correctly until at least 20 bits have been correctly received and any pair of these bits, separated from each other by seven other bits have differed in binary value from one another.

Note 2 - It is not possible to devise a satisfactory test pattern to check the operation of the Adverse State Detector (ASD) because of the large number of possible states in which the 20 state shift register can be at the commencement of testing. For those modems in which it is possible to bypass the scrambler and the descrambler and to strap the scrambler to function as a descrambler, the following method may be used. A 1 : 1 test pattern is transmitted with the ASD of the scrambler bypassed. If the ASD of the descrambler is functioning correctly the descrambled test pattern will contain a single element error every 32 bits, i.e. 180 000 errors per minute for a modem operating at 96 kbit/s indicates that the descrambler is functioning correctly. The operation of the ASD of the scrambler may be checked in a similar manner with the scrambler strapped as a descrambler and the descrambler bypassed.

I.3 Figure I-1/V.37 is given as an indication only, since with another technique this logical arrangement might take another form.



A	B	C
0	0	1
0	1	0
1	1	0
1	0	0

A	B	C
0	0	1
0	1	0
1	1	1
1	0	0

A	C
1	0
0	1

T	D	1 output	0 output
1	Q	–	–
0	–	Q	$\bar{Q}$

T	1 output	0 output
1	Q	$\bar{Q}$
0	$\bar{Q}$	Q

S	1 output	0 output
0	Q	$\bar{Q}$
1	1	0

Note – Negative-going transitions of clocks (i.e. 1 to 0 transitions) coincide with data transitions. This is self-synchronizing.

FIGURE I-1/V.37

An example of scrambler and descrambler circuitry

References

[1] CCITT Recommendation *Characteristics of group links for the transmission of wide-spectrum signals,* Vol. III, Fascicle III.4, Rec. H.14, § 2.

[2] CCITT Recommendation *Transmission of wide-spectrum signals (data, facsimile, etc.) on wideband group links,* Vol. III, Fascicle III.4, Rec. H.52.

[3] CCITT Recommendation *Characteristics of group links for the transmission of wide-spectrum signals,* Vol. III, Fascicle III.4, Rec. H.14, § 3.

[4] CCITT Recommendation *Physical/electrical characteristics of hierarchical digital interfaces,* Vol. III, Fascicle III.3, Rec. G.703, § 1.

[5] *Ibid.,* § 1.2.